Costa Rica Institute of Technology

Electronics Engineer School

Feed Forward Equalization Simulation Model for High-Speed Channel Applications

Graduation Project report to qualify for the title of Electronic Engineer, Licentiate Degree.

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El Tribunal Evaluador aprueba la defensa del proyecto de graduación denominado Modelado a nivel de simulación de un ecualizador lineal (FFE) para aplicaciones en canales de alta velocidad, realizado por la señorita Rebeca Castro Artavia y, hace constar que cumple con las normas establecidas por la Escuela de Ingeniería Electrónica del Instituto Tecnológico de Costa Rica.

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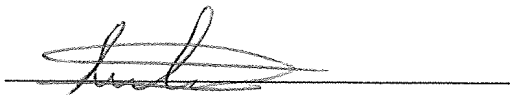

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Abstract

This thesis describes the development of simulation models of FFE stages (Feed Forward Equalizer) in transmitters for high-speed channel analysis. The implementation of this equalizer was performed using two different tools: ADS (Advance Design System) by Keysight, which is a commercial tool and SPITDS (Signal and Power Integrity Time Domain Simulator), which is a simulator developed by the Institute of Electromagnetic Theory at the Technical University of Hamburg in Germany.

Additionally, the LMS (Least Mean Square) algorithm was implemented in MATLAB and ADS to adjust the equalizer coefficients, in order to have a better signal recovery. Different channels were designed to make comparisons and verify the performance of different implementations of FFE with LMS. Both implementations of the Feed Forward Equalizer and LMS algorithm worked properly, which allows the application of the equalization FFE and the calculation of the equalizer coefficients for signal integrity analysis.

Key words: Feed Forward Equalizer, Least Mean Square algorithm, tap, equalization.

Resumen

Esta tesis describe el desarrollo del modelo a nivel de simulación de un ecualizador FFE en transmisores para canales de alta velocidad. La implementación de este ecualizador se realizó utilizando dos herramientas distintas: ADS la cual es una herramienta comercial de la compañía Keysight y SPITDS que es un simulador desarrollado por el Instituto de Teoría Electromagnética de la Universidad Técnica de Hamburgo en Alemania.

Además, se implementó el algoritmo LMS en MATLAB y en ADS para ajustar los coeficientes del ecualizador de manera tal que se pueda tener una mejor recuperación de la señal. Se diseñaron diferentes canales para realizar comparaciones y verificar el funcionamiento de las diferentes implementaciones de FFE con LMS. Ambas implementaciones del ecualizador FFE y de el algoritmo LMS funcionaron adecuadamente, lo que permite la aplicación de la ecualización FFE y el cálculo de los coeficientes del ecualizador para el análisis de integridad de señales.

Palabras claves: Ecualizador FFE, algoritmo de mínimos cuadrados medios, coeficientes, ecualización

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1 Introduction

The demand of higher data transmission rates in a communication system with a combination of integrate circuit (IC) scaling is driving the data transmission to multi-gigabit per second data rates. Unfortunately, the high speed communication is limited by channel distortions and inter-symbol interference (ISI), which one major contributors to the signal degradation through a channel. ISI is typically non-ideal and its frequency response is band-limited, mainly due frequency-dependent attenuation and reflections. These are undesired effects because impacts the shape of the pulse that arrives at the receiver and do not allow a good data transmission. Because of that, different equalization techniques are applied in order to mitigate the ISI and compensate channel losses.

TEC and TUHH has been carrying out joint research for high-speed channel analysis. This work is a contribution to these research efforts by the development of a Feed Forward Equalizer (FFE) simulation model for high-speed channel analysis. The development was done using different implementations and software tools. The first implementation was made in Advanced Design System (ADS) which is a commercial tool, a second implementation was carried out in the Signal and Power Integrity Time Domain Simulator (SPITDS), an in-house tool at Hamburg University of Technology (TUHH).

In addition, the least means square (LMS) algorithm was implemented in order to adjust the equalizer tap values to get a better signal recovery according to the channel characteristics. The algorithm was developed using two different tools: ADS and MATLAB.

Different channel models are designed and used for test the FFE and LMS adaptation algorithm. Both FFE and LMS implementations are compared in order to verify their correct operation.

The implementation of FFE equalizer in SPITDS, and the LMS adaptation algorithm in MATLAB was developed in the Institute of Electromagnetic Theory at the

Technical University of Hamburg, Germany, in cooperation with the Costa Rica Institute of Technology. With this work, the equalizer function (FFE) was added to the tool (SPITDS) that TUHH has been developing in recent years, so that it can equalize the simulated channel, facilitating research on the equalization topic.

1.1 Objectives

Develop a Feed-Forward Equalizer simulation model for high-speed channels analysis using for the implementation the software Advanced Design System (ADS) and the Signal and Power Integrity Time Domain Simulator (SPITDS).

1.1.1 Specific Objectives

- Define the transmission driver architecture with linear equalization (FFE), suitable for high-speed channel simulations.
- Design a simulation model of a transmission driver with linear equalization (FFE) at a system level with the software Advanced Design System (ADS) and Signal and Power Integrity Time Domain Simulator (SPITDS).
- Validate the equalizer implementations for high-speed channel simulations.

1.2 Work Structure

This work is organized in six chapters. After a brief introduction in Chapter 1, Chapter 2 discusses the fundamentals of high speed channels, where the main concerns in relation to high speed serial links, equalization, and the application of adaptive algorithms for the equalizer are explained. Chapter 3 presents the implementation of the 4 tap FFE in ADS, for differential and single-ended links, and a FFE for an arbitrary number of taps in SPITDS. The development of a LMS adaptation algorithm in ADS and MATLAB for both FFE implementations. An explanation of models links used for the test of the results of the algorithm applied at the FFE is also included. Chapter 4 explains the different channel models: the backplane simulated links with models were taken from [1] and the semianalytical models designed with stub effect in Multilayer Substrate Simulator (MLSS), another in-house tool of TUHH. In addition, the main simulation results are discussed. Chapter 5 presents the conclusions and recommendations for further research.

2 High Speed Links Fundamentals

This chapter explains the main concepts around the high speed serial links and unwanted effects in the channel produced when muti-gigabit data rate is used for the transmission. In addition, equalizer fundaments, different implementations for the equalizer, and the techniques applied for adapt the tap values of the equalizer.

2.1 High Speed Serial Links Overview

The increase demand of high performance in integrated circuits (IC) is causing that the industry moves towards high-speed communication technology. For this reason, many companies are implementing changes in circuit designs to improve their performance and achieve efficient communication. An example is a transition from parallel to high speed serial I/O solutions in way to simplify system design, have more capability to increase the bandwidth, scalability and cost reduction [2] and implementation of active equalization techniques.

A high-speed serial link or SerDes is a serial transceiver that on the transmitter side converts parallel data into a serial data stream and on the receiver side converts the serial data back to parallel [3]. A typical high-speed serial link is shown in Figure 2.1, consisting of a transmitter with serial parallel input data, equalizers at transmitter (TX), the communication channel, a receiver driver, equalizers at receiver (Rx). and the deserialized parallel output data. These systems are typical asynchronous; the clock must be recovered accurately the received signal. That and the increasing the data rate makes serial link communications so challenging to implement but also so powerful.

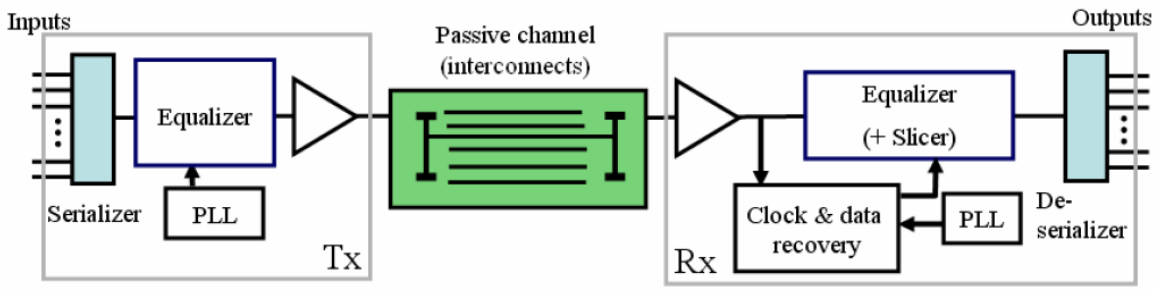


Figure 2.1 Diagram of a high-speed serial link (SerDes) taken from [4].

Some examples of interconnect standards are PCI Express Gen 3 (8 Gb/s), IEEE 802.3ap 10BASE-KR (10 Gb/s), Fiber Channel 16GFC (14 Gb/s), SATA3 (6 Gb/s), USB3 (4.8 Gb/s), Infiniband10Gbps), and upcoming IEEE 802.3ba (40–100 Gb/s), which is defining the 40/100 GbE protocols [3]. For interconnections from processor to peripheral PCI Express Gen 3 (8 Gb/s), Infiniband (10Gbps), USB3 (4.8Gbps) are used. For storage is common used SATA3 (6Gbps), Fiber Channel (20Gbps) and for networks interconnections Ethernet (1, 10Gbps, up to 100Gbps) are used [5].

The need for higher-speed links in communication system causes a growing number of interconnects that operate at rising data rates [6]. The muti-gigabit data rate in transmissions is predominantly limited for different issues, reflections for impedance discontinuities, crosstalk, high-frequency losses, skin effect, and dielectric losses. The impedance discontinuities due to the material properties of the connectors, vias etc., introduce losses and reflections. Crosstalk occurs due to both capacitive and inductive coupling between neighboring signal lines. The high-frequency loss of electrical traces, which commonly manifests low-pass filter behavior, becomes a serious threat for high speed transmissions. The skin effect is when the high frequency currents tend to travel not only in the whole cross section of the conductor, but also on the surface. This effect increases the resistance, reduces the effective conductive of the trace, causing reflections and more attenuation in the signal. This skin effect is proportional to the square root of frequency [7]. All of these effects causes the inter symbol interference (ISI) and it's the major obstacles for the high speed data links. The PDN (power distribution network) is another noise and further degradation element that can couple.

These effects can be mitigated by appropriate design of the transmission line, which a correct selection of the stackup, substrate, vias types, size, number and position of ground vias and power vias, routing of signals paths, etc. But when the links work in muti-gigabit data rate and these changes in the design are not enough for mitigate these effects and active equalization techniques are required for compensate the channel degradation [4] and mitigate the ISI [8].

2.2 Equalization Overview

In general, the channel response of interconnects resembles a low-pass filter response. This is not a desired effect, and in order to compensate the high speed attenuation due to this low-pass transfer characteristic, several equalizing techniques are applied [9].

The equalization techniques can be applied at the transmitter equalization and receiver equalization side. Typically, this kind of equalization de-emphasize the low frequency component or emphasize the high frequency component of the signal [12].

A typical transmitter current and voltage mode driver are shown in Figure 2.3. The current mode drivers are more commonly implemented. These drivers usually use controlled output stage to supply a fixed output swipe on the channel [12].

Figure 2.4 shown a typical circuit used for a high speed receiver with binary differential signaling which the major advantage is that the incoming data is compares with an inherent threshold, whereas single-ended signaling requires careful threshold generation [12].

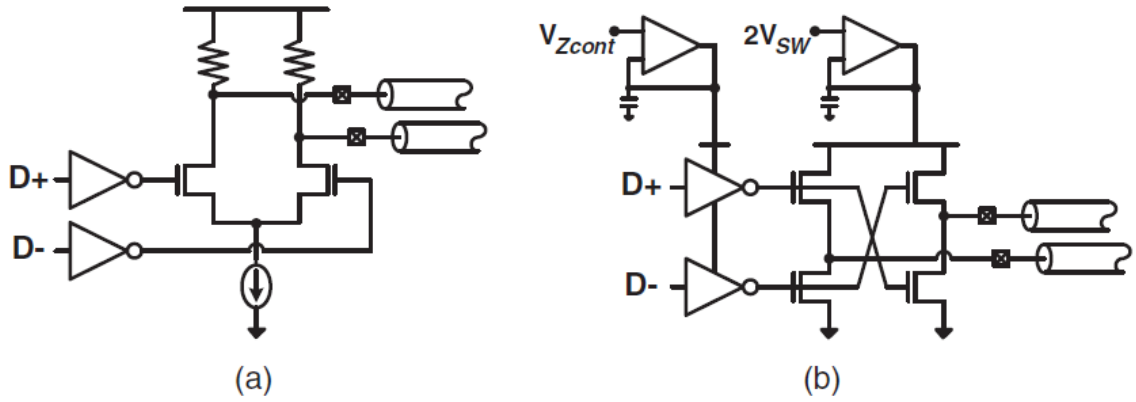


Figure 2.2 Typical transmitter topology. (a) current mode driver. (b) Voltage mode driver taken from [12].

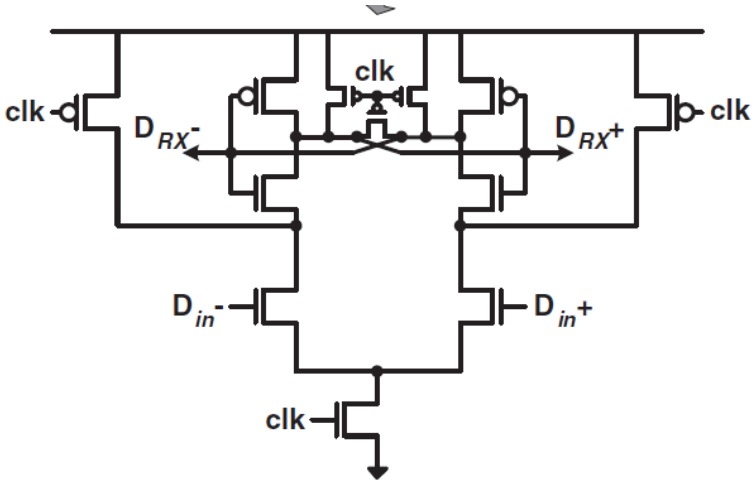


Figure 2.3 Typical receiver input stage with regenerative latch taken from [12].

Equalization is a powerful technique to restore distorted signals, which employs passive component as an equalizer applied to wired transmission channels [10]. The equalizers counteract the channel degradation by emphasizing the high-frequency components of the signal [4]. The transfer functions of the system are multiplied by the equalizer transfer function which ideally is the inverse of the channel transfer function [11] like it is shown in Figure 2.2.

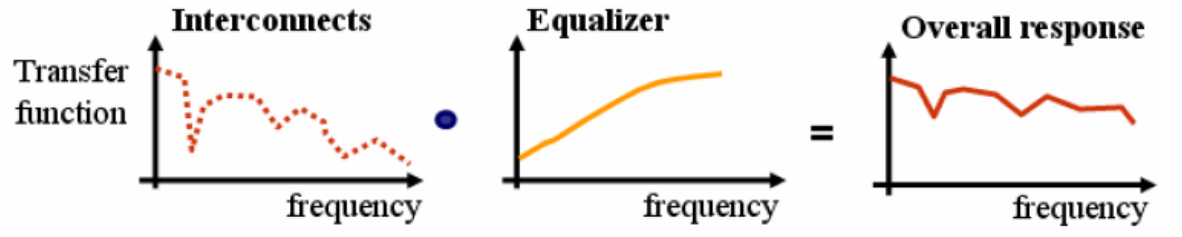


Figure 2.4 Concept of effect of the equalizer taken from [4].

This compensation of the channel degradation comes at expense of a reduced signal to noise radio (SNR), because the attenuation of the low frequencies signals components in order to match the high frequency channel attenuated components [11].

The equalization can be analyzed in a frequency domain or a time domain perspective. From time-domain analysis, the equalization reduces the amplitude of the pulse response that is propagated out of its ideal position and cause interference with other symbols. In the frequency domain analysis, the equalization helps compensate the low pass filter channel response by increasing the high frequency components of the transmitted signal, lowering the low frequency ones [8].

There are different combinations but equalization techniques commonly applied at the transmitter side is Feed Forward Equalization (FFE), and at the receiver side are Continuous Time Linear Equalizer (CTLE) and Decision Feedback Equalizer (DFE) [13]. The Figure 2.5 show a high serial link diagrams using this kind of the equalization at the same link.

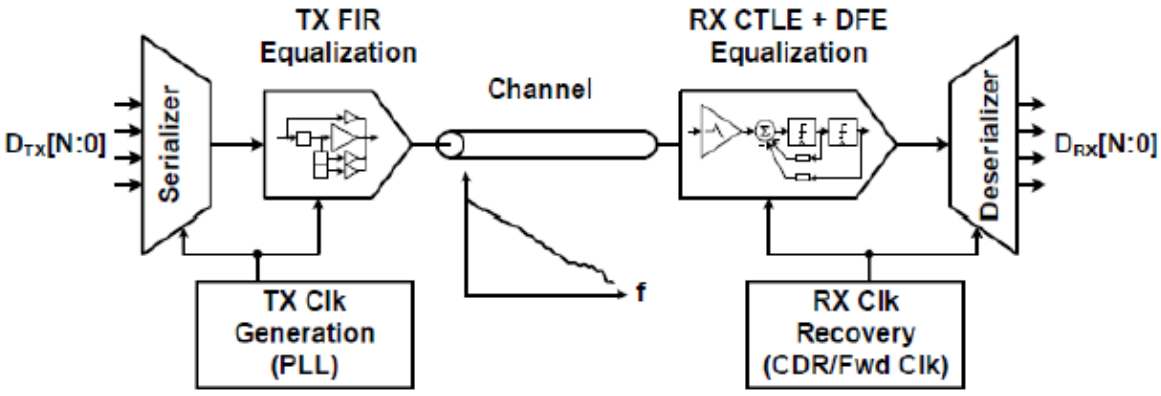


Figure 2.5 High speed serial link with TX FFE equalization and RX CTLE and DFE equalization taken from [13].

Continuous Time Linear Equalizer

The CLTE commonly used a linear passive or active filter as shown in Figure 2.6. Both implementation can realize high pass transfer function for compensate the channel distortions. This linear equalizer cancel both precursor and long tail of ISI. Some disadvantages are the amplification of the noise and crosstalk, limited order compensation, and difficulty tuning [13].

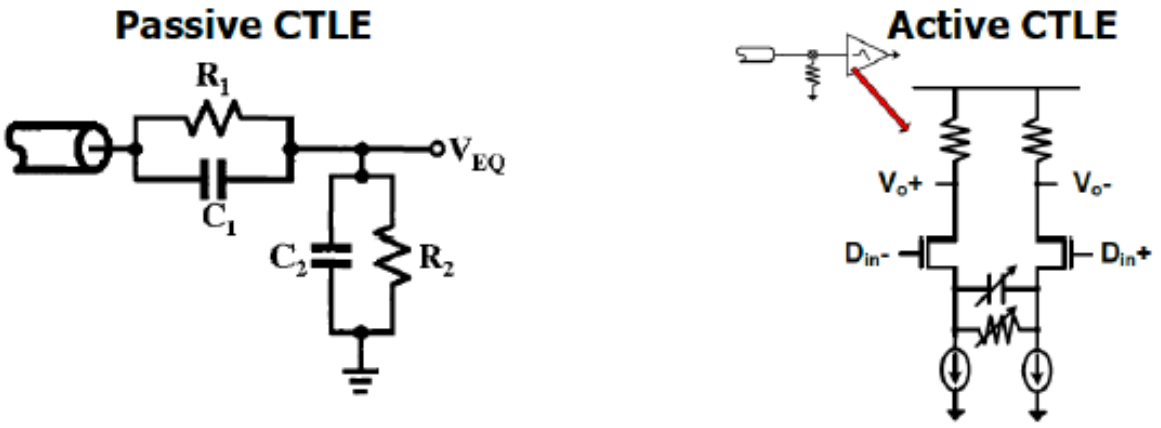


Figure 2.6 Receiver CLTE equalization taken from [13]. (a) passive. (b) active.

Decision Feedback Equalizer

The DFE is a nonlinear equalizer which does not have the same problem as the linear equalizer because does not directly amplify the crosstalk or the signal noise. This equalizer compensates the channel distortions eliminating noise amplification and using a linear combinations of past decisions [7].

A DFE is shown in Figure 2.7, this equalization technique is mostly used in the receiver side. The DFE through an FIR filter and the feedback the input can cancel the post-cursor ISI. The Tap coefficients for this equalizer can be adaptively tuned. A disadvantages for this equalization techniques are the high chance for the error propagation, the critical timing path for the feedback [12].

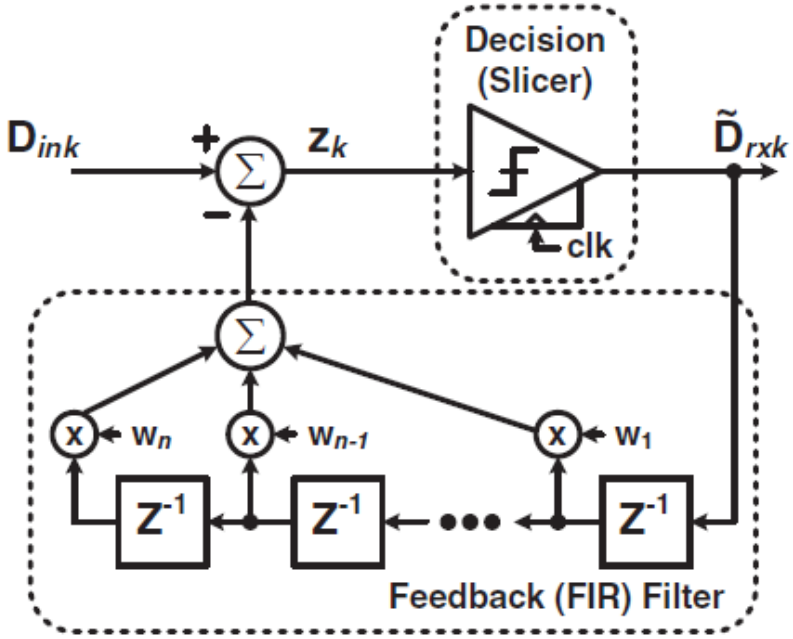


Figure 2.7 Common implementation of a receiver DFE.

Feed Forward Equalization

The FFE is a linear equalizer which the typical implementation is a finite impulse response (FIR) filter shown in Figure 2.8. This equalization technique applied pre-emphasis, predistorting or shaping the pulse over several bit times in order to pre-compensate the channel distortion of a signal [12].

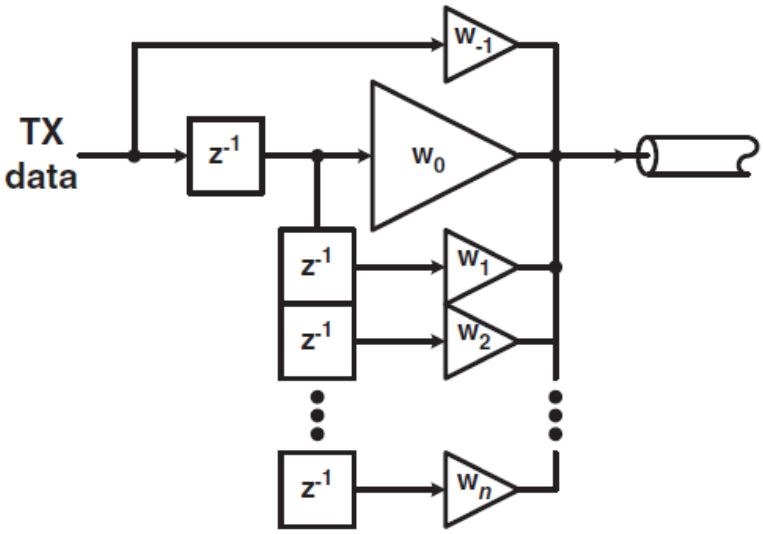


Figure 2.8 Common implementation of a transmitter FFE equalization taken from [12].

In the time domain the waveform with pre-emphasis appears as overshoot or undershoot. In Figure 2.9 the effect of the FFE equalization is illustrated. The blocks represent the delay applied per tap. This delay usually is a unit interval. The tap values are represented with an arrow. The input signal from the transmitter pass through each delay and is multiplied by the respective taps values predistorting the signal.

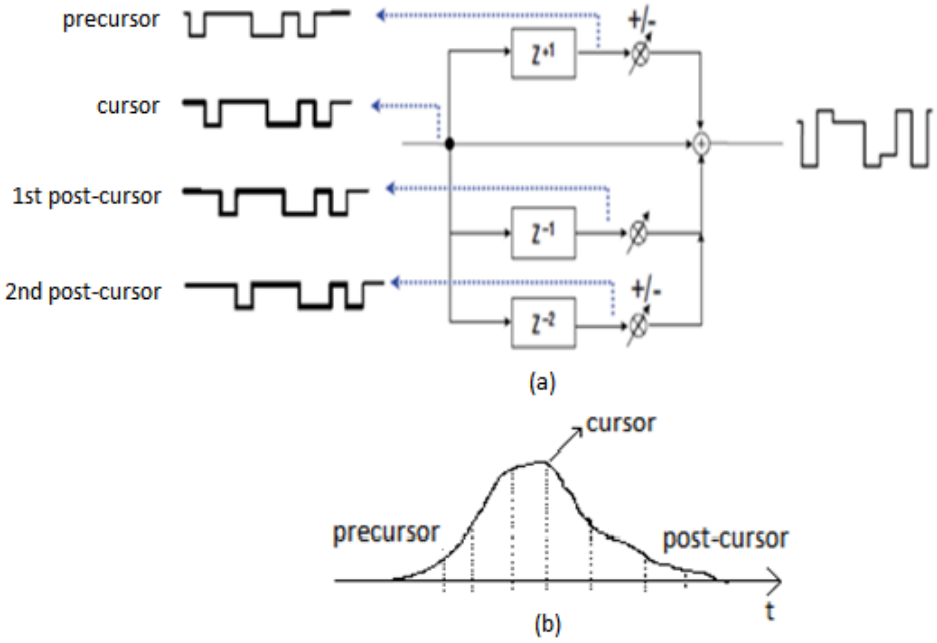


Figure 2.9 Predistortion of the signal by 4 taps FFE taken from [14] (a). Impulse response equalization effect (b).

The amplitude of the equalizer signal to counteract the losses and distortions depends of the number and values of the precursors (pre-tap), post-cursors (post-tap) and cursor (main tap) of the equalizer. Where in an impulse response analysis the cursor is aligned with the maximum amplitude of the signal, the precursors affect the amplitude of the signal before that the cursor and the post-cursors affect the amplitude of the signal at a time interval after of the cursor.

FFE equalization cannot fully compensate the channel distortion because are not ideal equalization [15]. Some disadvantages of FFE equalization are the power requirements, increased electromagnetic interference (EMI) [7] and that the low frequency content is attenuated. Nevertheless, it allows the matched filter to be realized digitally, also adapt for channel variations, can cancel pre-cursor ISI, and the noise is not amplified [13].

This equalizer technique could also be implemented at the receiver but a common problem is that high frequency noise and crosstalk are amplified. The principal advantage of implemented the equalization at the transmitter side is that is more easy to build high speed digital analog converter than the analog to digital converters at the receiver side [12].

2.3 Adaptive Equalization for Linear Equalizers

Different algorithms to adjust the taps values (tap adaptation) are used. The different algorithms present some limitation and advantages in comparison with other algorithms. The principal challenge is to select the best algorithm for the linear equalizer due to the wide variety. It requires knowledge of the computational cost, performance, and robustness for make a decision. The main algorithms used for the adaption equalization are the least mean square (LMS) and Recursive Least Square Algorithm (RLS) [9].

Least Mean Squares Algorithm (LMS)

The Least Mean Square algorithm minimizes the mean square error at the receiver center eye. It is used to find the coefficients for minimization of the error signal with is the difference between the desired signal and the actual signal [15]. LMS algorithm is a simple but it converges slowly and its complexity grows linearly with the number of weights [6]. Figure 2.10 shows the typical implementation for a LMS in a FFE.

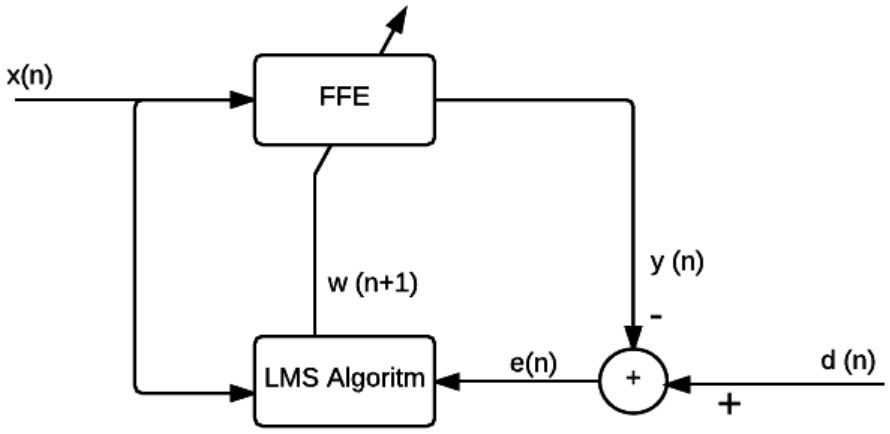


Figure 2.10 Block diagram of LMS algorithm applied at an adaptive FFE.

LMS algorithm estimate the error signal by comparing the equalized signal (output of the equalizer) with a desired signal (Equation (1)) and the calculations of the taps values as follows in the Equation (2) [6].

$$e\ (n) = \ d\ (n) - y\ (n) \qquad (1)$$

$$w\ \ (n+1) = \ w\ (n) + \mu * e\ (n) * sign(x(n)) \qquad (2)$$

where:

e (n) = error signal
d (n) = desired signal vector
y (n) = equalizer output vector
μ = step size adaptation
w (n+1) = new tap value at time (n + 1) vector
w (n) = tap value at time (n)
x(n) = [x(n) x(n-1) … x(n-p)] = input signal vector

The step size must be a value between 0 and 1. If becomes μ smaller, the correction to the filter weights gets smaller for each sample and error falls more slowly. But, for a larger μ changes the weights more for each step so the error falls more rapidly, but the resulting error does not approach the ideal solution as closely or might not converge. For the calculation of the error is important the signals are synchronized.

The LMS algorithm is relatively simple to understand and is powerful enough to assess the practical benefits that can be achieved in an adaptive application. It will be the algorithm used for the adaptation of the taps values.

Recursive Least Square Algorithm (RLS)

RLS is an algorithm that used a recursively approach for finds the taps values which minimize a weighted linear least squares cost function. This algorithm has an extremely fast converge but this comes at the cost of a potentially poor tracking when estimated changes and the high computational complexity. The RLS algorithm has a similar procedure as LMS algorithm but has a tracking rate [9].

3 Simulation Model of a Transmitter Driver with FFE Equalization

This chapter describes the development of a Feed-Forward Equalizer (FFE) simulation model in the transmitter side for high-speed channels analysis using Advanced Design System (ADS), which is a commercial tool, and the Signal and Power Integrity Time Domain Simulator (SPITDS), a simulation tool developed by TUHH. In addition, the MATLAB and ADS implementation of the Least means square (LMS) algorithm in order to adjust the equalizer tap values, to get a better signal recovery according to the channel characteristic. The FFE is implemented in these two simulation tools, in order to compare the results. The four tap FFE is implemented based on the design used in [16], using in the same way one precursor, main tap and two post-cursors.

3.1 ADS FFE implementation

The implementation in ADS for a four tap FFE is illustrated in Figure 3.1. For this implementation two kinds of simulations are used simultaneously: ADS Ptolemy which uses a data flow simulation approach, and is controlled using the DF (data flow) simulation controller component for the equalizer circuits (i.e. a behavioral simulator) and a transient simulation for the channel (i.e. convolution solver). This is possible because ADS allows the cosimulation of both domain using data converters [17]. The DF simulation controller is necessary because the delays, taps and adders for the equalizer are a digital component and require this controller for set the configurations of these elements and the Transient controller for simulated and set the channel characteristics. Figure A.3.1 in Appendix A show a detail diagram of the FFE ADS implementation.

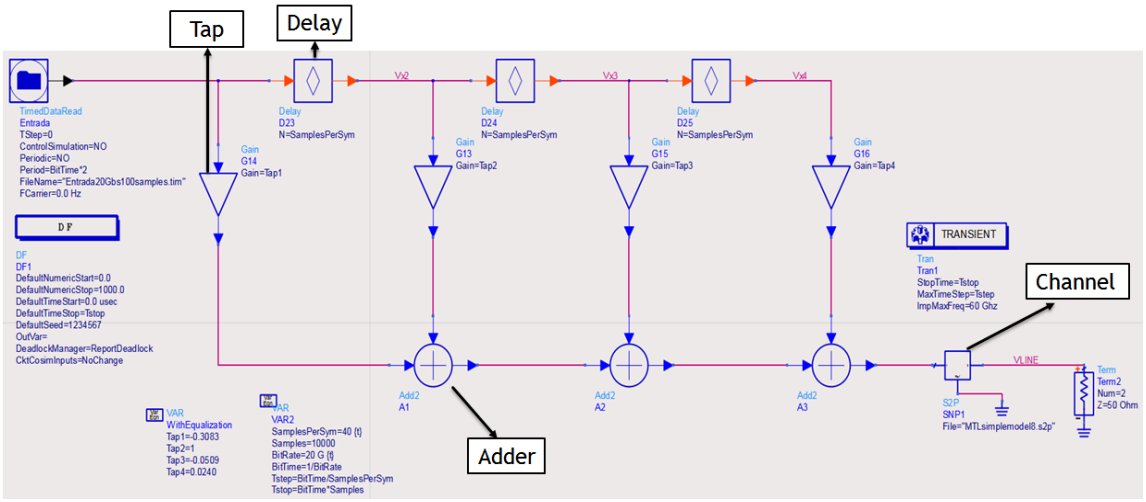


Figure 3.1 Diagram of the implementation for FFE equalizer in ADS with single ended channel.

This FFE can be used for single ended channels (see Figure 3.1) or differential channels (see Figure 3.2). The design for differential channels is implemented because have numerous advantages over a single ended signaling. The differential signals have a reduced electromagnetic interference (EMI) and crosstalk coupling. They have also a lower voltage swings that single ended signals [20] at a cost of more area and power consummation.

The differential implementation uses, like the single-ended implementation, the ADS Ptolemy and transient simulations. In order to simulate a differential channel a balun provides the ideal transformation of single-ended signals into differential signals. The balun between the equalizer output and differential channel is connected. In this way, it is possible simulate the effect of the equalization in a differential channel. The differential implementation with S-parameter block is shown in Figure A.3.2 in Appendix A.

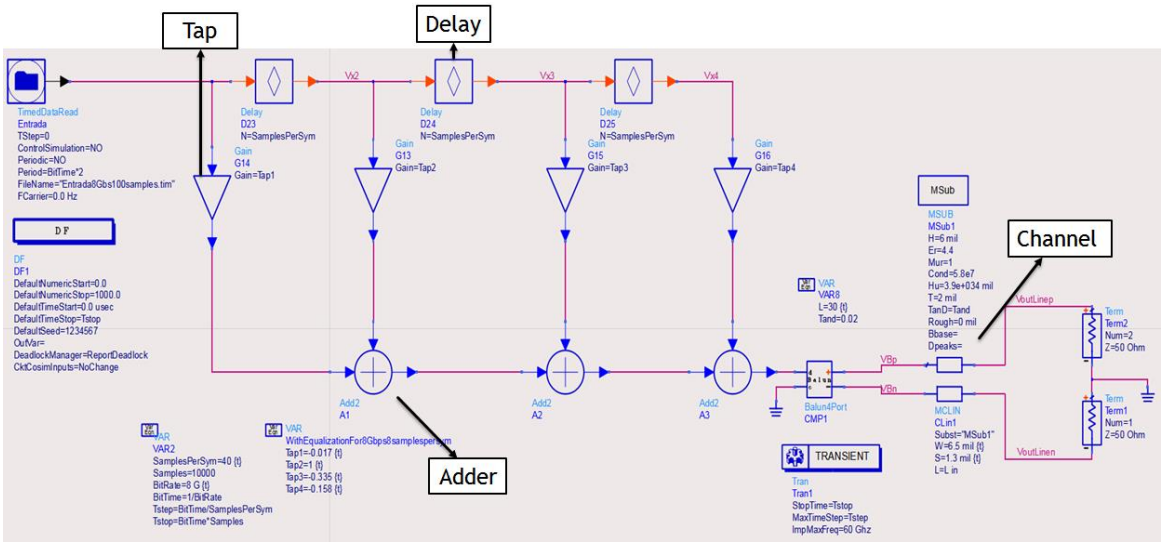


Figure 3.2 Diagram of the implementation for FFE equalizer in ADS for a differential channel.

In both designs the source signal is delayed an unit interval (UI) and is multiplied by the respective pre-tap and post-taps witch outputs are summed. This pre distorted signal is the output of the equalizer and the input for the channel. These implementations can be used with a micro strip lines configured in ADS or a s-parameters block like channel and a term port impedance for the receiver

For obtain a better signal recovery because the amplitude of the equalizer signal to counteract the losses and distortions depends of the number and values of the pre-cursor, post-cursor, and cursor of the equalizer, a LMS algorithm for set the taps values of the FFE in ADS was implemented.

3.2 LMS Adaptation Algorithm ADS Implementation

Figure 3.3 shows the implementation of the LMS algorithm in ADS. This algorithm in general consists of two procedures: the estimation error by comparing this output with a desired signal using the Equation (1) and the adjustment of the tap values of the FFE in accordance with the estimation error using the Equation (2) explained in the section 2.3. These equations are calculated like as shown in the Figure 3.4.

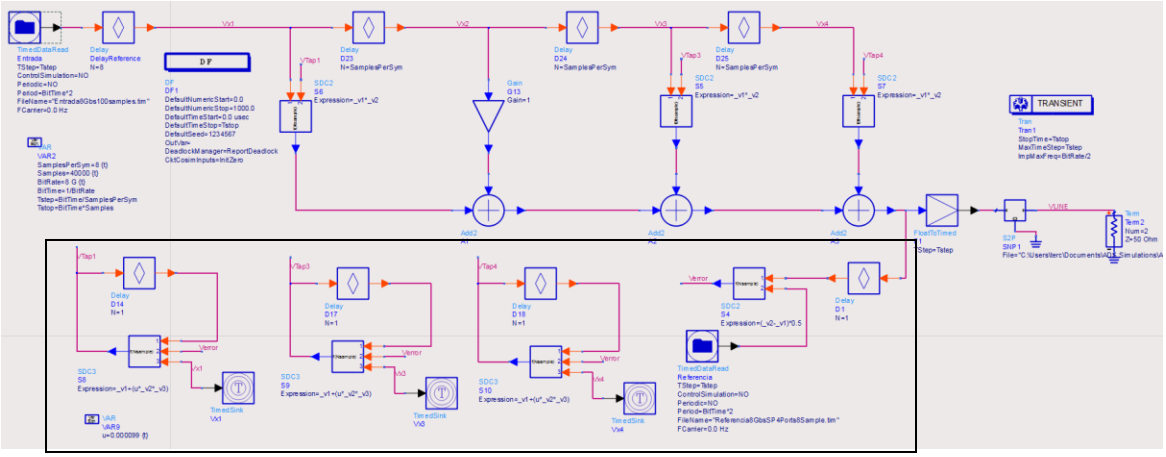


Figure 3.3 Diagram of FFE with LMS algorithm ADS implementation.

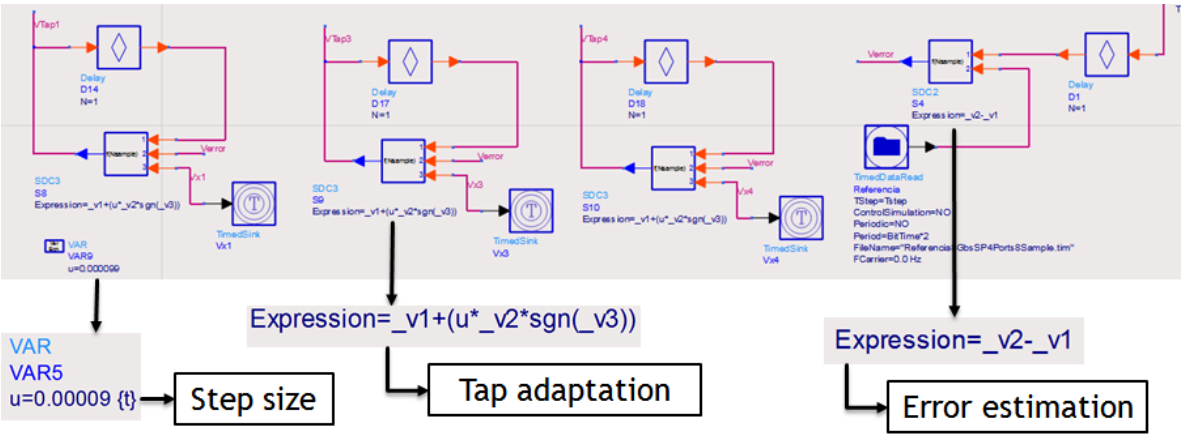


Figure 3.4 Detail view of LMS algorithm implementation in ADS.

For the estimation error the desired signal is required. In order to get this signal, is necessary to characterize the channel. To do that, the channel without equalization is simulated. The signal after channel without equalization is obtained and is compared with the input signal, thereby obtaining a signal which contains the degradation that needs to be compensated. In practical this is done as an initialization step to set the taps when using the equalizer.

An important consideration for used LMS algorithm is that the signals must have the same bit sequence and need to be carefully synchronized.

The LMS algorithm is applied a simple link created in ADS shown in Figure 3.5. It is a microstrip line model whose has a 36 inch of large and the parameters are configured to obtain a simple model to test the equalizer and LMS algorithm implementation.

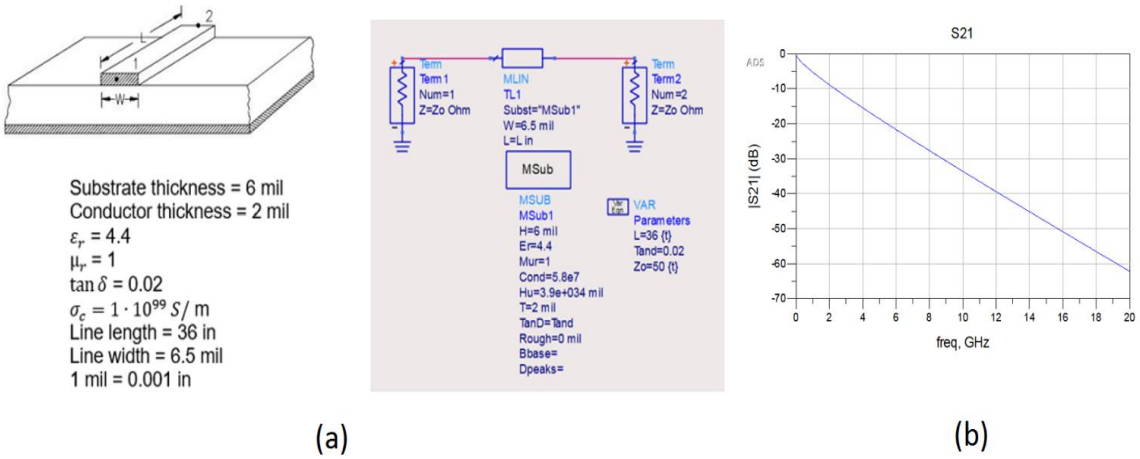


Figure 3.5 ADS transmission line model. (a) Diagram of single ended microstrip line. (b) Transmission parameters of microstrip line.

The LMS algorithm is applied for this link using a PBRS with a level voltage from -1 V to 1 V at 7 Gb/s and a step size (μ) equal to 0.000099. Figure 3.6 shows the calculation of the 3 taps values for the FFE equalizer one precursor (vtap1) and two post-cursors (vtap3 and vtap4). Is showing how the algorithm converges, obtaining the values of the taps for set in the FFE in order to counteract the channel distortion.

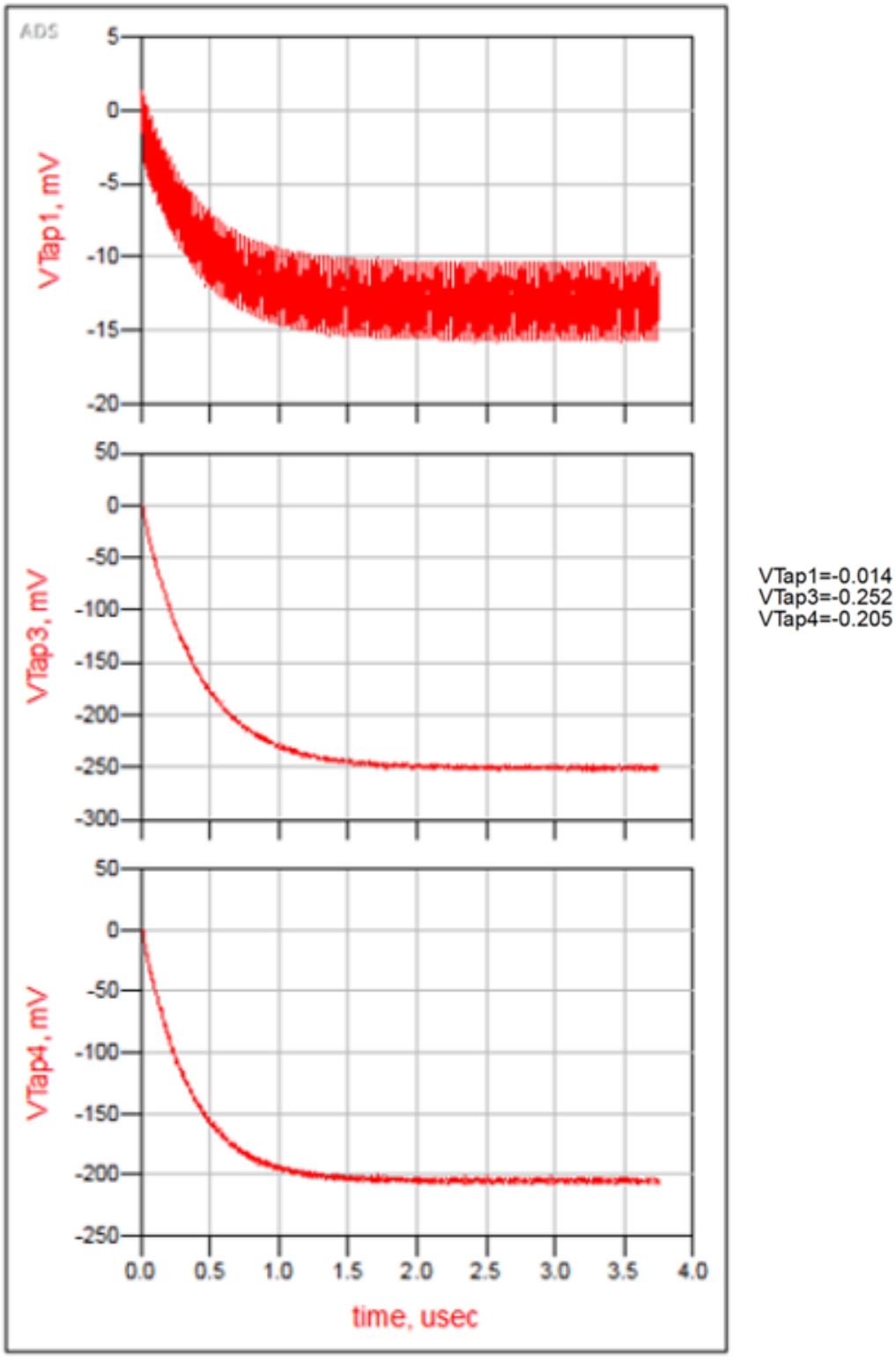


Figure 3.6 Convergence of the LMS algorithm ADS single ended channel implementation.

The FFE ADS implementation for this link without equalization and with equalization setting the taps values calculated from LMS algorithm is simulated, using for both simulations a Pseudo Random Binary Sequence (PRBS) source with a level voltage from 0 V to 1 V at 7 Gb/s using 10000 bits for the simulation. Figure 3.7 shows eye diagrams for these simulations.

When the equalization is not applied the eye is closed and the signal is not recoverable meanwhile when applied equalization the eye is open and has a height of 172.86 mV, which represent a recovered signal (see Figure 3.7).

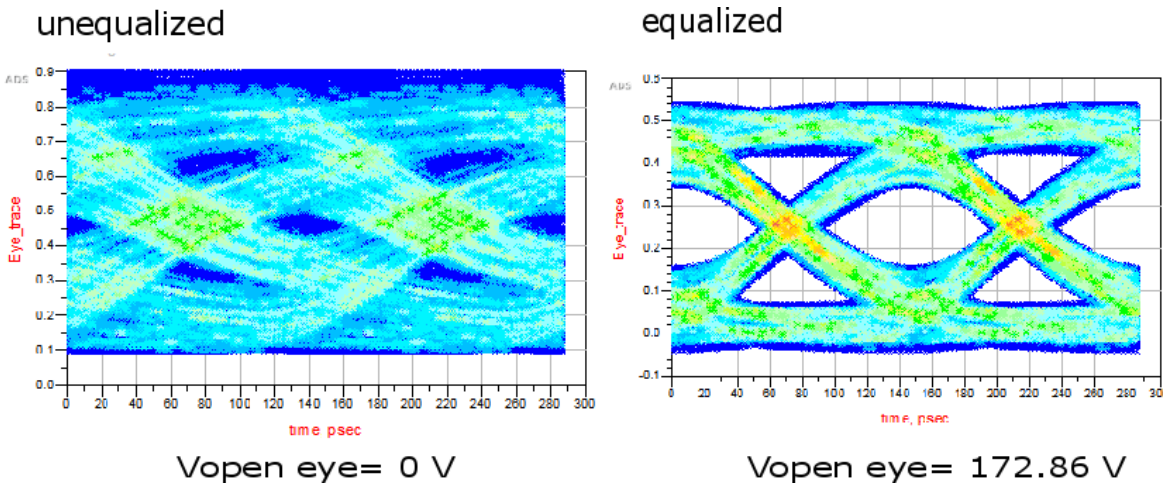


Figure 3.7 Eye diagram comparison for ADS transmission line model at 7 Gb/s with and without equalization using LMS algorithm ADS implementation with a single ended channel model with 36 inches long.

The same LMS algorithm implementation can be used in a differential channel (see Figure 3.8).

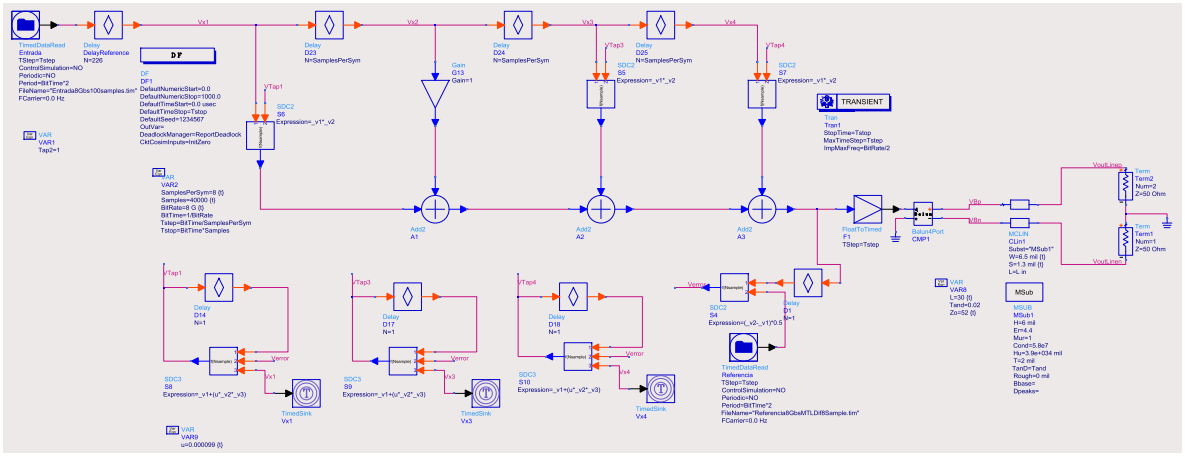
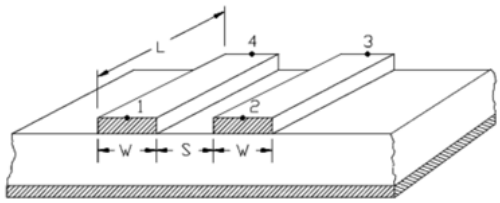


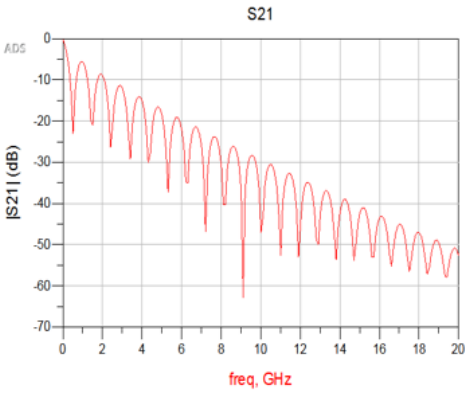
Figure 3.8 Diagram of FFE with LMS algorithm ADS differential channel implementation.

To test this implementation of the algoritm a PRBS source at 7 Gb/s with level voltage from -1 V to 1 V is applied, using a step size (μ) equal to 0.000099. The channel is a line model in ADS like show the Figure 3.9.



Substrate thickness = 6 mil
Conductor thickness = 2 mil
ε_r = 4.4
μ_r = 1
tan δ = 0.02
$\sigma_c = 5.8 \cdot 10^7\ S/$ m
Line length = 36 in
Line width = 6.5 mil
Space between lines= 1.3 mil
1 mil = 0.001 in

(a)



(b)

Figure 3.9 ADS transmission line model. (a) Diagram of microstrip coupled lines. (b) Transmission parameters of microstrip line.

Figure 3.10 shows the values of the taps obtained for this simulation and the convergence of the LMS algorithm.

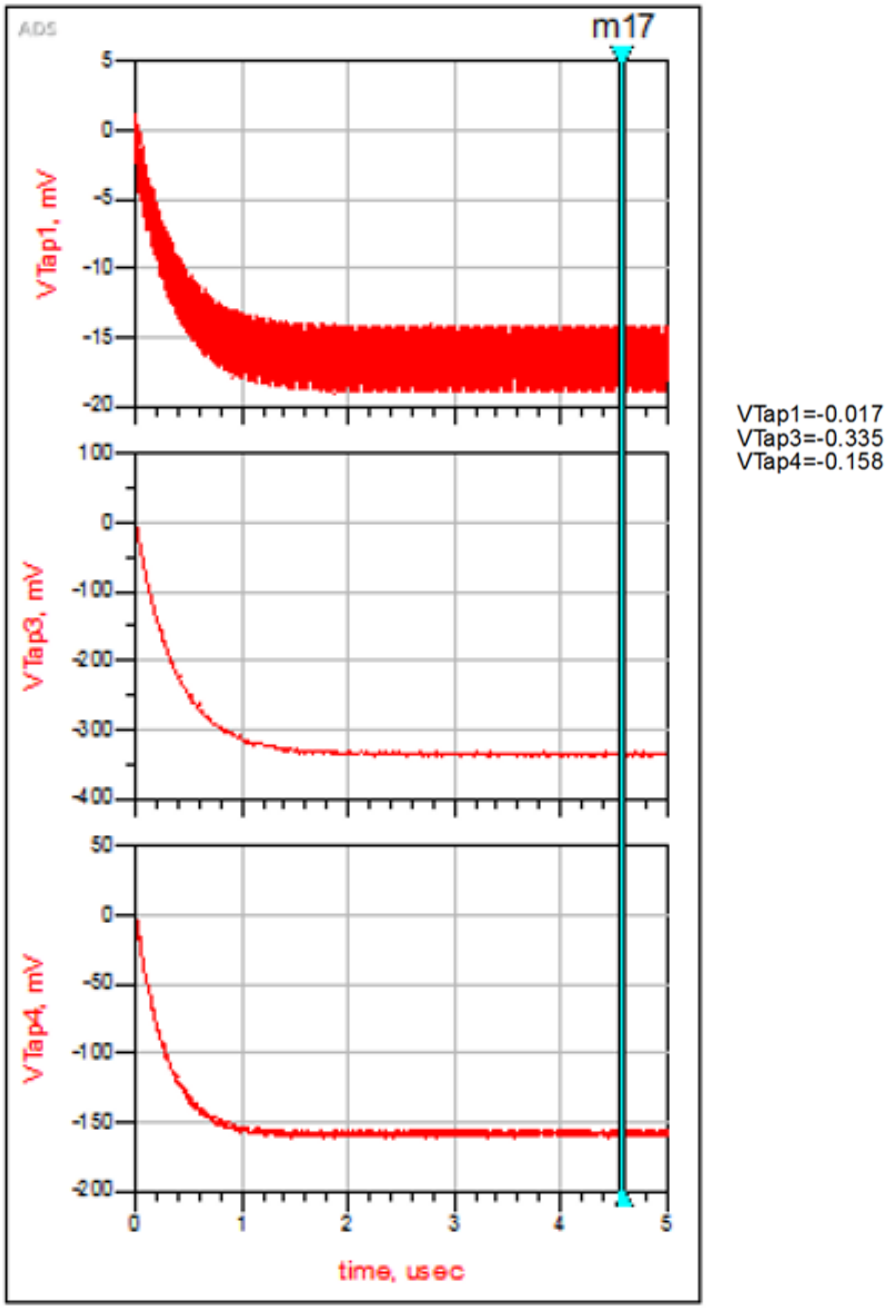


Figure 3.10 Convergence of the LMS algorithm ADS differential channel implementation.

The FFE equalizer with a differential channel implementation (see Figure 3.2) is simulated with a PRBS source at 7 Gb/s with a level voltage from 0V to 1V using for the simulation 10000 bits and setting the tap values obtained by the LMS algorithm. Figure 3.11 shows that without equalization the eye is completely closed but, when the equalization is applied the eye opening is 274.36 mV.

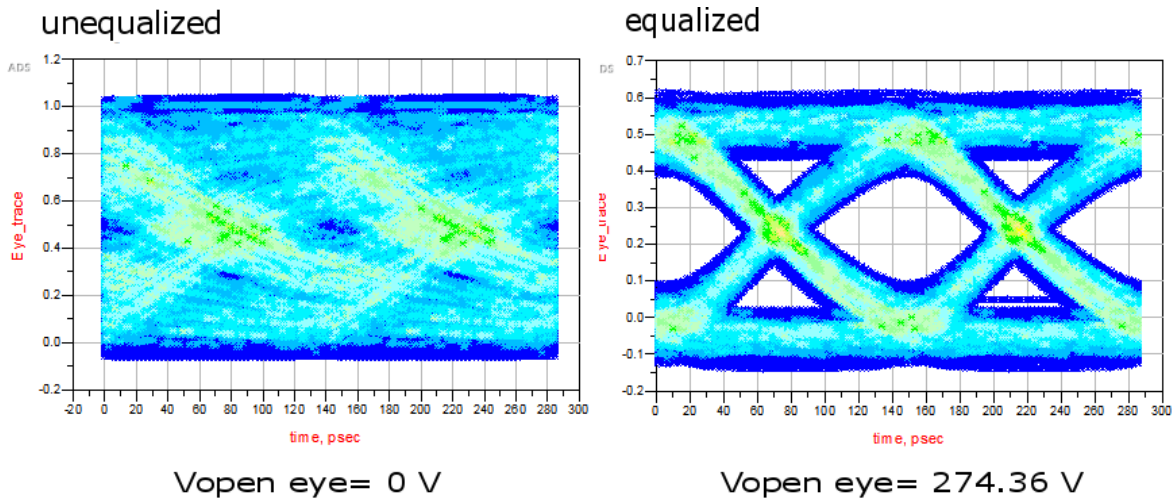


Figure 3.11 Eye diagram comparison for ADS transmission line model at 7 Gb/s with and without equalization using LMS algorithm ADS implementation with a differential channel with 36 inches long.

With these results it is shown that the implementations of FFE and LMS algorithm are working correctly.

3.3 SPITDS FFE implementation

The Signal and Power Integrity Time Domain Simulator (SPITDS) is a simulator developed at the Institute of Electromagnetic Theory, Technical University of Hamburg in Germany. It is capable to simulate different effect in the channel including ISI, crosstalk and SSN. The FFE is implemented in SPITDS with aim to include the feature of applying equalization to a channel in this tool.

Figure 3.12 shows how the FFE in SPITDS is implemented. The inputs for the FFE equalizer are the output waveform of the source, the values of taps and bit numbers from the configuration file. The FFE equalizer use a UI delay, and is implemented for an arbitrary number of taps. The programming language used for this FFE algorithm is Fortran.

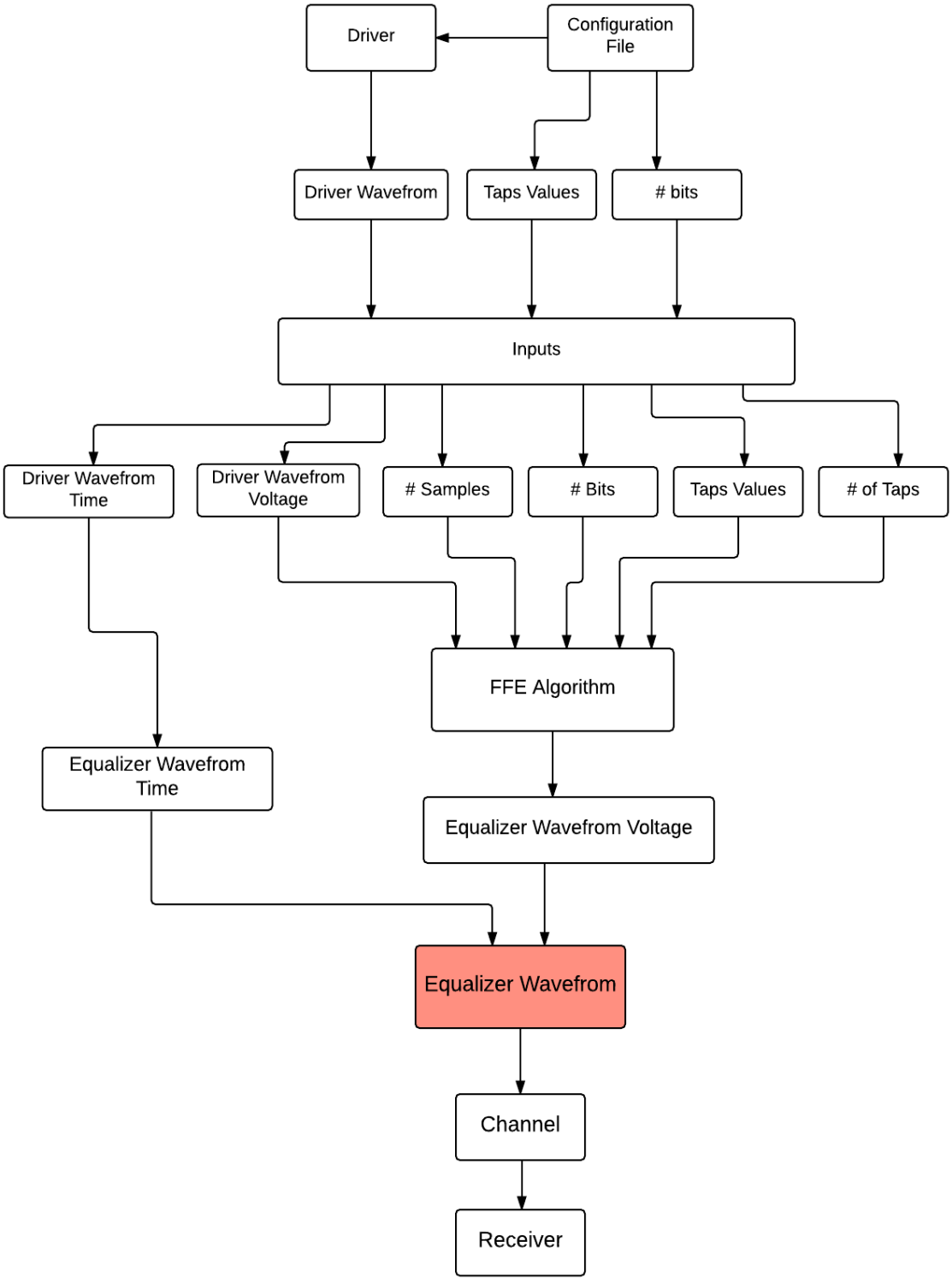


Figure 3.12 Diagram of the implementation for FFE equalizer in SPITDS.

The Equation (3) shows the general expression that the algorithm uses for FFE implementation.

$$y\ (n) = Tap1\ * x(n) + Tap2\ * x(n-1)\ \ldots + Tap\ i * x(n-i-1), \qquad (3)$$

where:
x(n) = Input of the equalizer
y(n) = Output of the equalizer
i = Desire number of taps

3.4 LMS Adaptation Algorithm of the MATLAB Implementation

The LMS algorithm was implemented in MATLAB in order to adjust the tap values for the SPITDS FFE implementation and also this could be useful for ADS FFE implementation.

The diagram of the LMS algorithm implemented in MATLAB is shown in Figure 3.13. It shows the inputs necessary for the calculation of the taps values and how this data is organized. The output of this implementation are only the final tap values.

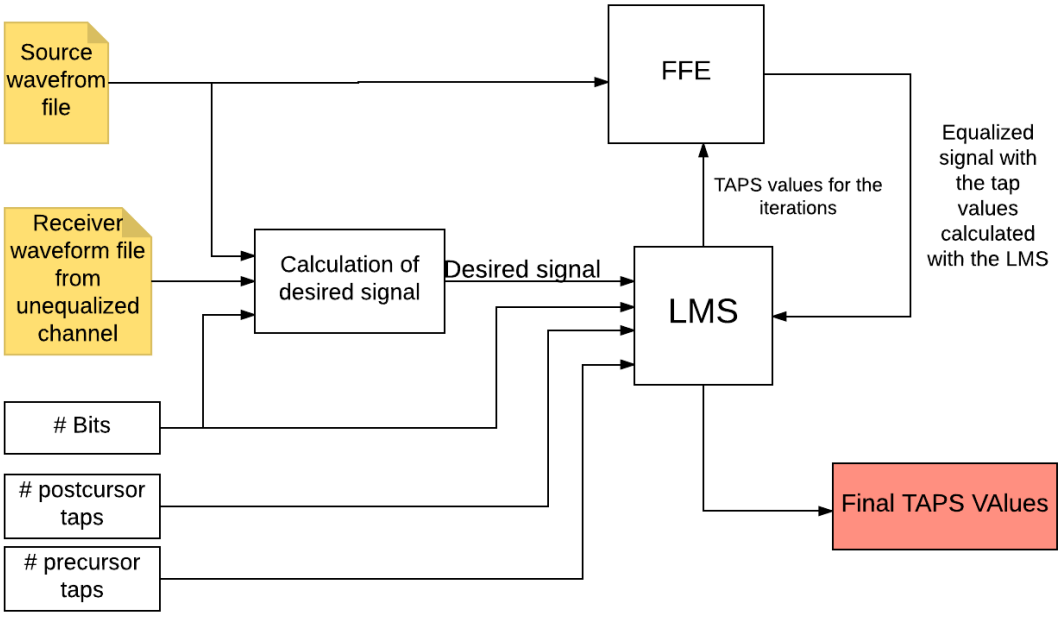


Figure 3.13 Diagram for the implementation of a LSM algorithm adaptation for a FFE.

The algorithm consists of three procedures: calculation of the desired signal, equalization process (FFE), and tap adaptation process (LMS).

For the calculation of the desired signal, it is important to know that the source waveform and receiver waveform from unequalized channel must have the same bit sequence and need to be carefully synchronized.

The equalizer process (FFE) uses the same algorithm for the FFE in SPITDS implementation (see section 3.3) but implemented with MATLAB code.

In the tap adaptation process is where the LMS algorithm is applied. The error signal is calculated like in Equation (1) and after that applied the Equation (2) explained in the section 2.3 to obtain the taps values.

The detail of the LMS algorithm equalizer process (FFE) and adaptive taps process (LMS) can be observed in Figure 3.14, where:

x(n) = Input of the equalizer
y(n) = Output of the equalizer
i = Desire number of taps

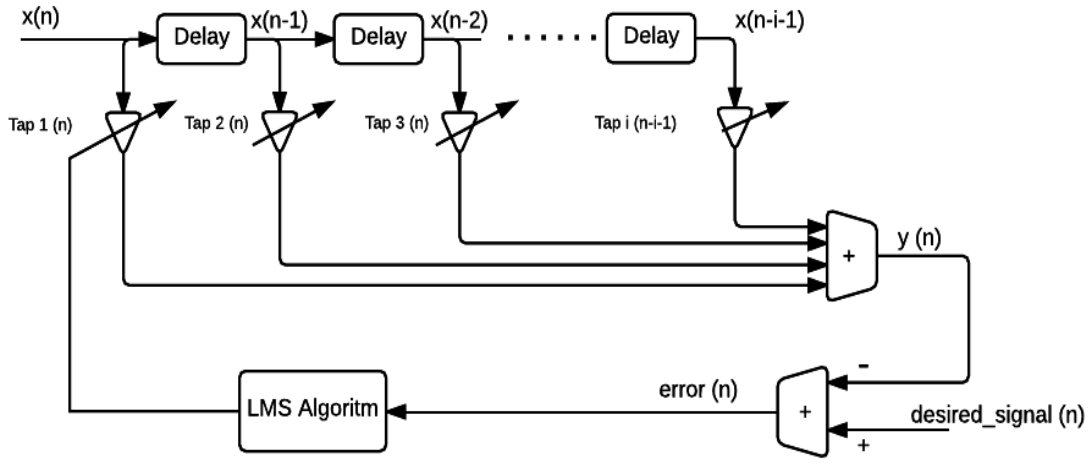
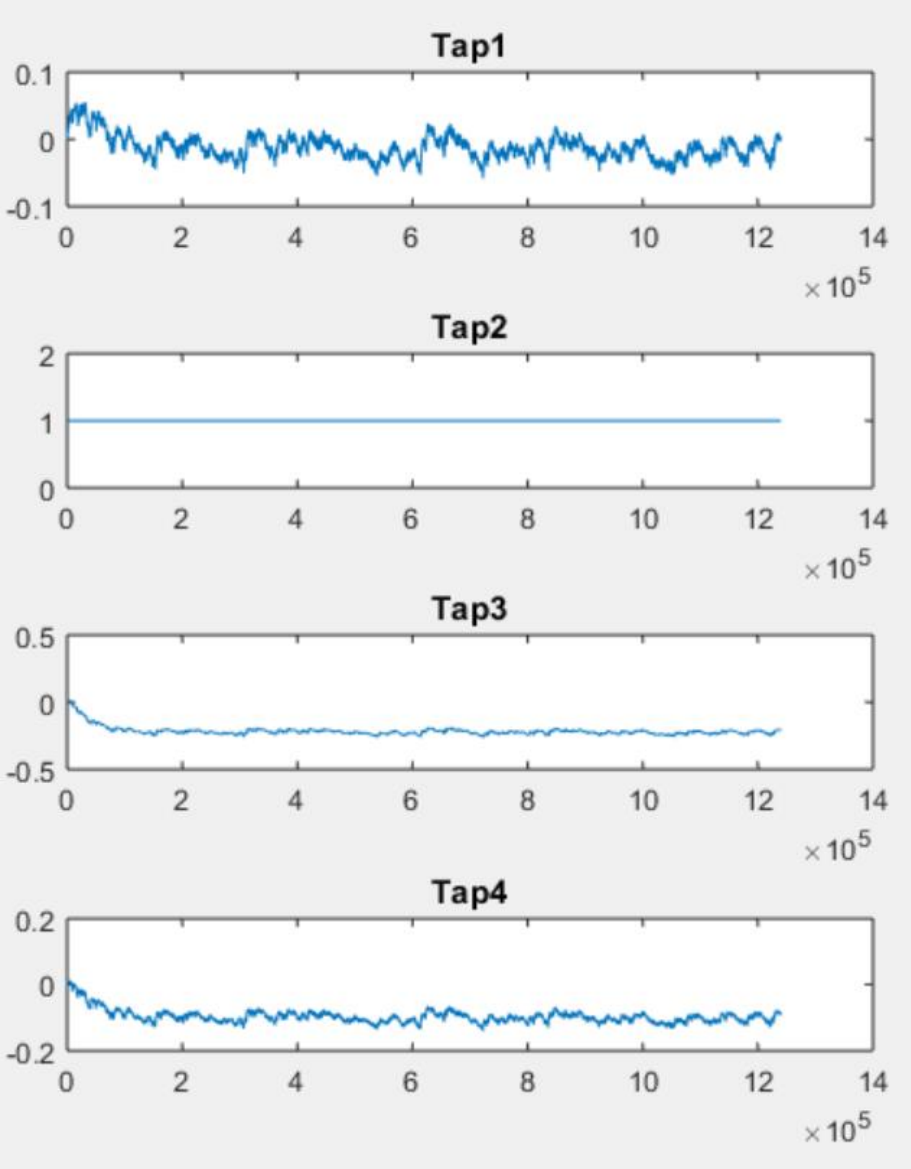


Figure 3.14 Detail of the LMS algorithm equalizer process (FFE) and adaptive taps process (LMS algorithm).

The implemented algorithm has the option to set the main cursor tap value manually. With this we can applied pre-emphasis or emphasis to the signal.

The LMS algorithm implemented in MATLAB is applied to the link explained in section 3.11 using a PBRS with a voltage level from -1 V to 1 V at 7 Gb/s and a step size (μ) equal to 0.000002. Figure 3.15 shown how the LMS algorithm converge and the tap values for the FFE.




```
Tap_values =

   -0.0138    1.0000   -0.2350   -0.1156
```

Figure 3.15 Convergence of the LMS algorithm and taps values applied at SPITDS data.

In order to make the algorithm to converge faster, it is better to use sources with amplitudes of -1 V to 1 V. This is due to how the algorithm calculates the values of the taps for the FFE (Equation (2)).

Figure 3.16 shows eye diagrams for the simulation of the FFE SPITDS implementation without and with equalization using the taps values obtain with the LMS algorithm MATLAB implementation. PRBS source with a level voltage from 0 V to 1 V at 7 Gb/s is used for both simulations.

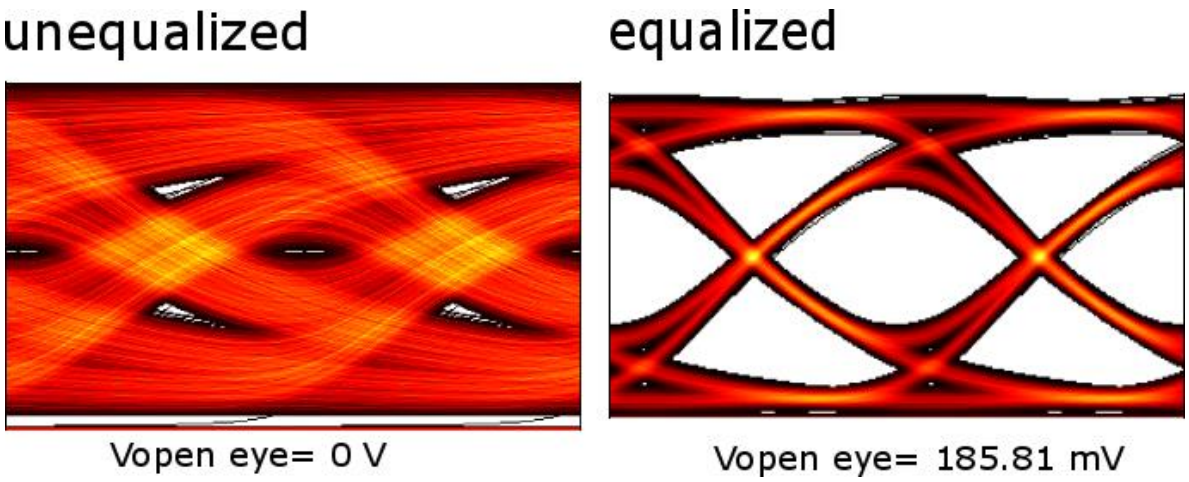


Figure 3.16 Eye diagram comparison for ADS transmission line model at 7 Gb/s with and without equalization using LMS algorithm SPITDS implementation.

In the same way that in Figure 3.7 when the equalization is applied the eye is open. The height if the eye is 185.81mV, and this makes the signal can be recovered.

4 Result Validation

In this chapter, simulations for different links are presented in order compare the FFE ADS and SPIDTS implementation. Both, to assess the effect of equalization on different channels and test the correct operation with the LMS algorithm implemented in MATLAB will be discussed for both FFE implementations. The LMS algorithm realized in MATLAB is used since the same tap values are used for both FFE implementations.

4.1 Channel Models for Link Simulations

This section presents backplane link and a semianalytical model with stub effect used for the evaluation of both FFE and LMS implementations. Also the ADS transmission line model explained in section 3.2 is used.

4.1.1 Backplane Simulated Links

Figure 4.1 an example of a semianalytical link model formed with two cards connected by means of a backplane board is shown. This link is taken from [1]. Two different examples presented in this paper were used as simulation models for testing the equalizer design.

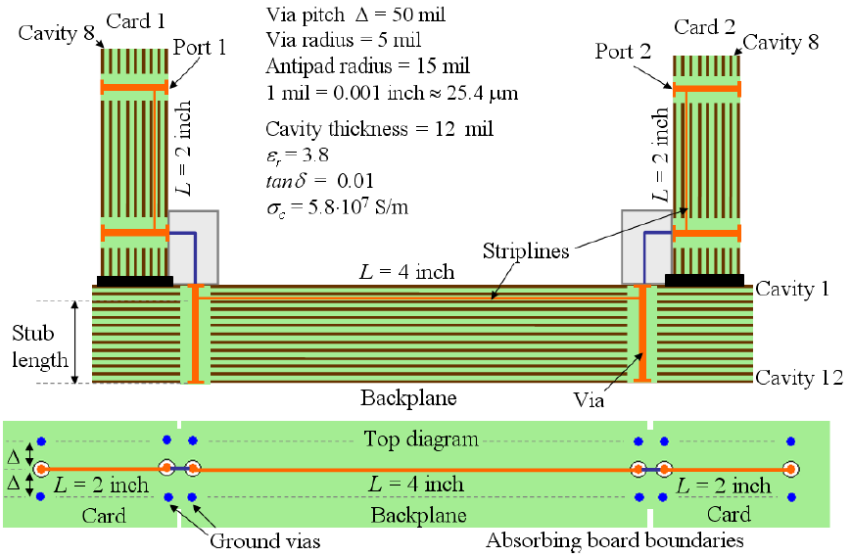


Figure 4.1 Diagram of the link and model parameters taken from [1].

This is an example where the traces are routed at different levels. The transmission parameters for the two examples selected are shown in Figure 4.2. In the curve A, the trace was routed with any cavity below for the first card, with two below for the backplane and two cavities below for the second card. The curve B, has two cavities below the trace for the first card and the backplane and six below the trace for the second card.

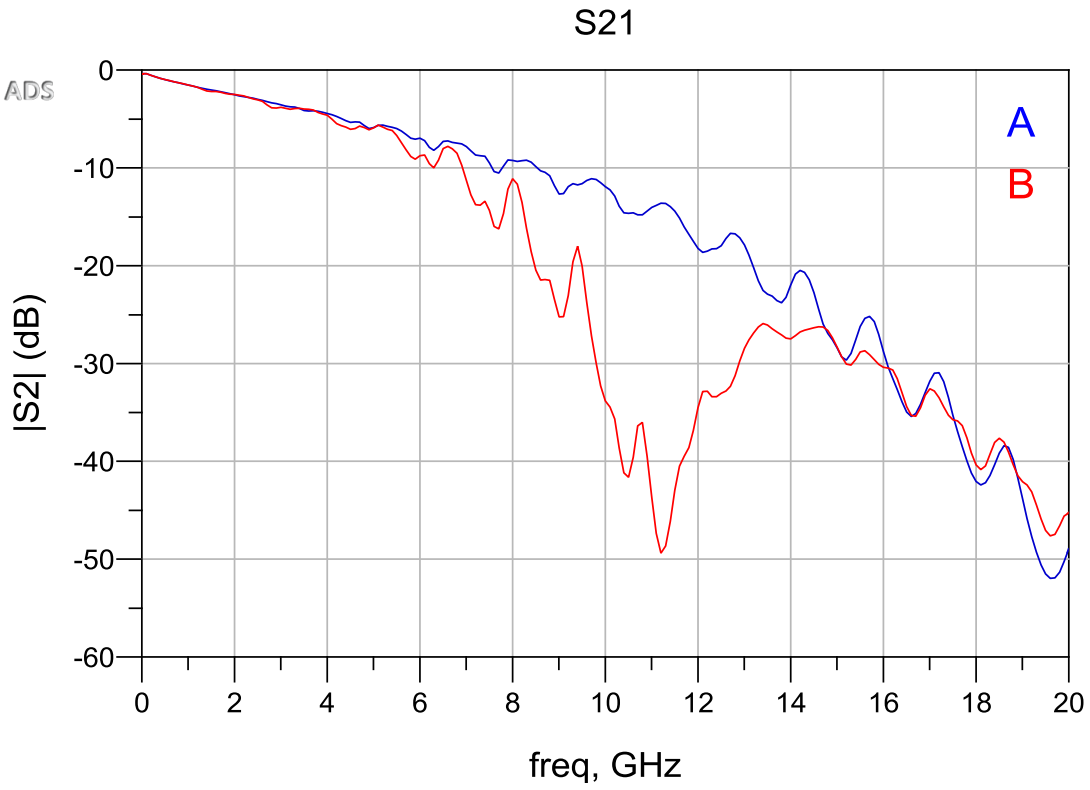


Figure 4.2 Transmission parameters for a link where the traces are routed at different levels.

4.1.2 Semianalytical Models with Stub Effect

The tool used for the creation of this model was Multilayer Substrate Simulator (MLSS) an in house tool of TUHH. It is used to simulate multilayer substrates with semianalytical models. This tool is useful for rapid design prototyping, different links because permit with a fast modification in the configuration file the creation of a new and different link. Figure 4.3 shows the structure for a single ended link design in MLSS. The geometry diagram and model parameters are shown in Figure 4.3, where L represent the length of the line.

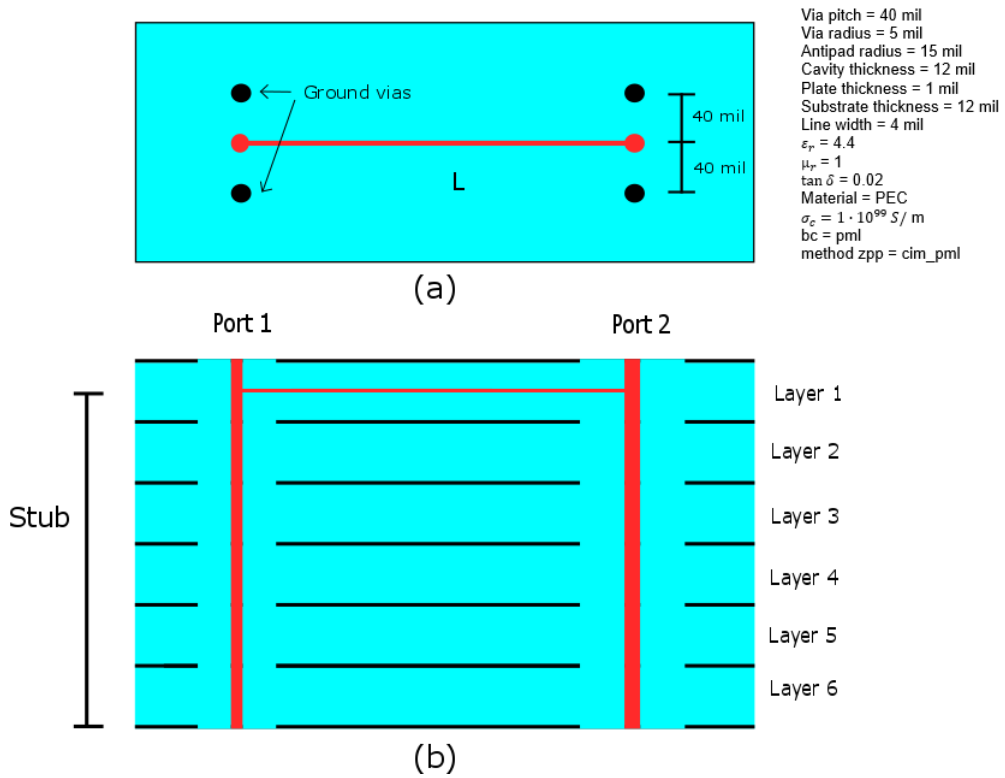


Figure 4.3 Diagram of a link model in MLSS and its main parameters. (a) top view, (b) cross-section. The materials are chosen as a perfect electric conductor and FR4 with the given specifications.

The transmission parameters with the stub effect for this model can be observed in Figure 4.4.

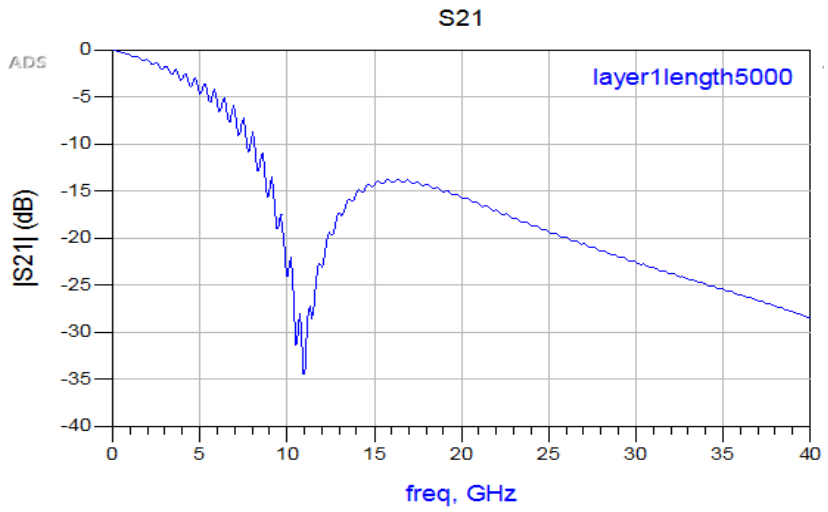


Figure 4.4 Transmission parameters for semianlytical link with stub effect.

4.2 Considerations

In order to make sure that the eye diagrams in ADS and SPITDS are similar, two kinds of plotter are applied in ADS for the comparison. One way to plot the eye diagram is using the Eye Probe plotter, which works only with the Transient and Convolution simulations [18]. Due to that the Eye Probe is only used for comparing the results of ADS and SPITDS without equalization. Since it does no support DF analysis the Eye Diagram FrontPanel, which allows for transient simulation and cosimulation is used.

To understand the differences between ADS and SPITDS obtained in the simulations, first some comparison with the different plotters were done. For this comparison the example A, from section 4.1.1 without equalization is used, because eye probe cannot be used with the equalizer designed in ADS. The diagram used for the simulation is shown in Figure 4.5. A transient simulation was executed.

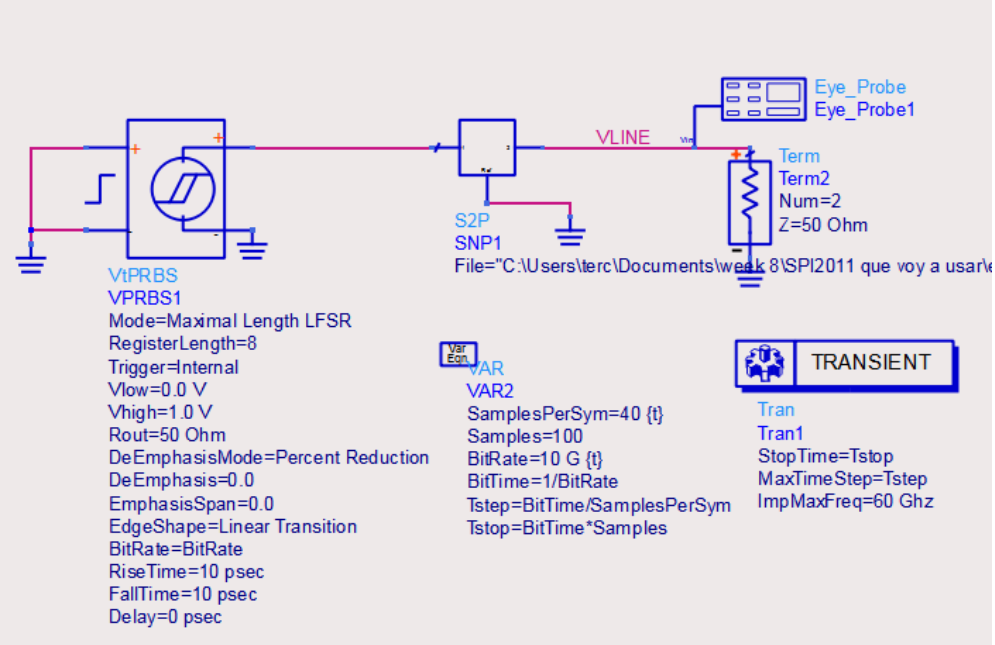


Figure 4.5 Circuit in ADS for eye diagrams from Eye Probe and Eye Diagram FrontPanel plotters comparisons.

Figure 4.6 shows the result of the simulations of this channel at 10 Gb/s with a few bits (256 bits) in order to compare the results. In Figure 4.6 (c) the differences between these two plots can be observed in the same simulation. The most visible difference is the way to plot the density, because the blue lines (arrowed in Figure 4.6 (c)) are plotted only with Eye Diagram FrontPanel. This effect can be observed too in Figure 4.6 (d), when the two eye diagrams are superposed.

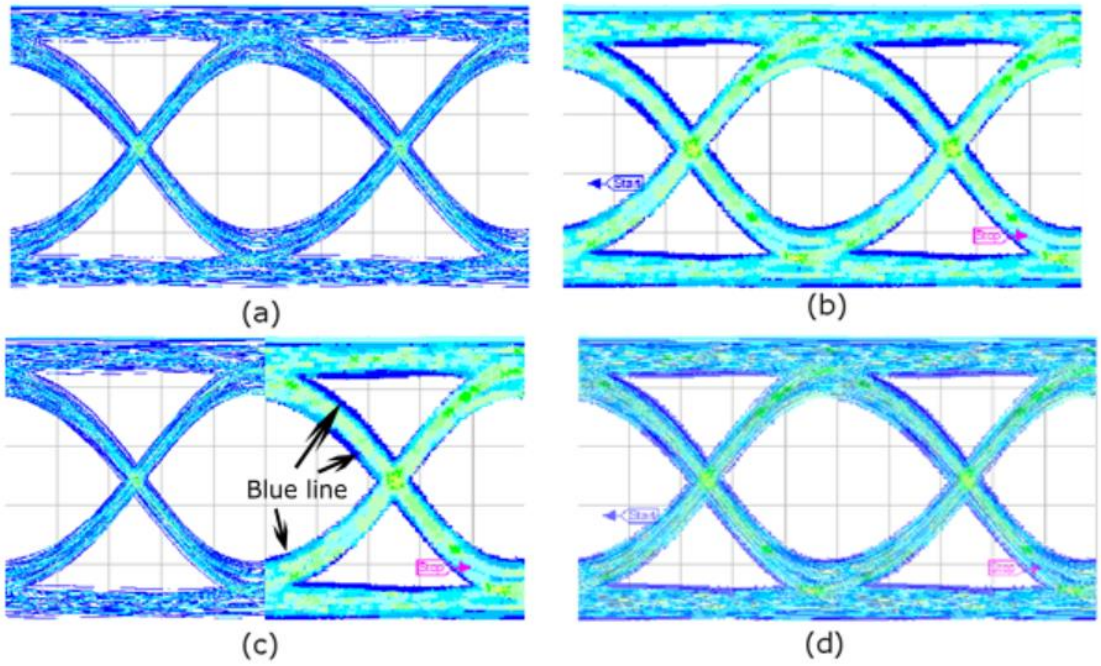


Figure 4.6 Eye diagram of example A (section 4.1.1) at 10 Gb/s with 256 bits. The vertical and horizontal scales are 20 ps per division and 0.1 V per division respectively. (a) eye diagram from Eye Probe plotter. (b) eye diagram from Eye Diagram FrontPanel plotter. (c) comparison between these two plotters. (d) both eye diagrams superposed.

In order to compare the results with SPITDS and see the differences between these plotters, the same channel at 10 Gb/s was simulated in SPITDS. The eye diagram is shown in Figure 4.7.

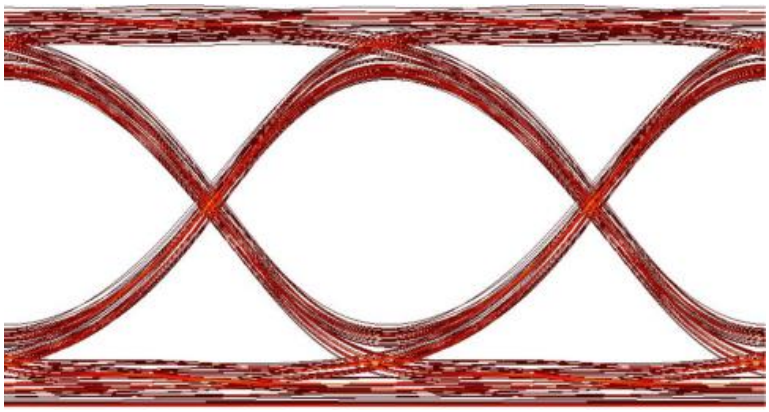


Figure 4.7 SPITDS eye diagram of example A (section 4.1.1) at 10 Gb/s with 256 bits.

As shown in Figure 4.8, the eye diagram from the Eye Probe plotter and SPITDS are very similar, and both plot the density with lines, but the Eye Diagram FrontPanel plot this with stars (*). This is why the eye diagram looks more closed that the others. The principal difference observable in this figure is a blue line (arrowed in Figure 4.8) for the Eye Diagram FrontPanel plotter.

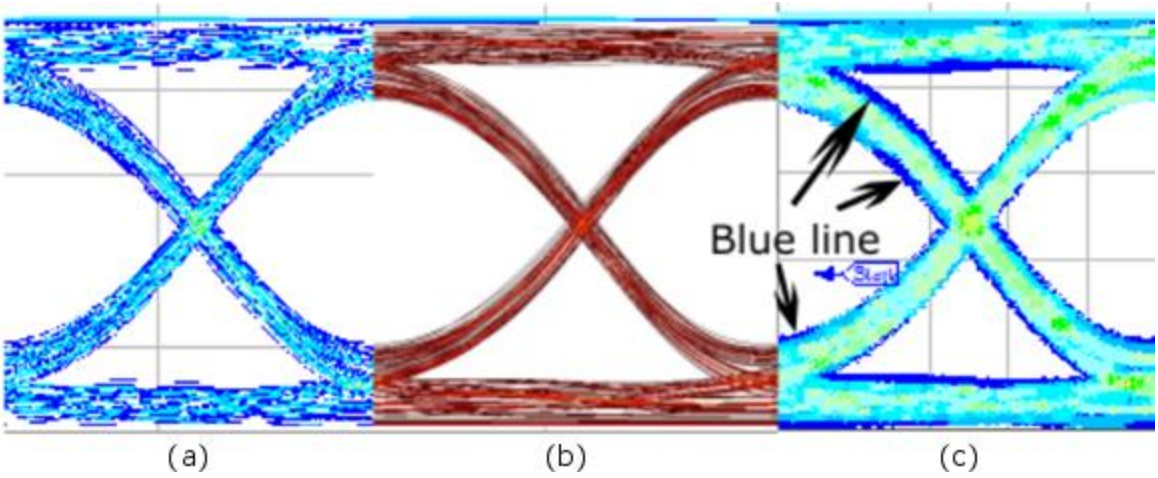


Figure 4.8 Comparison of eyes diagrams from Eye Probe plotter (a), SPITDS (b) and Eye Diagram FrontPanel plotter (c) of example A (section 4.1.1) at 10 Gb/s with 256 bits. The vertical and horizontal scales are 20 ps per division and 0.1 V per division respectively.

The measurements of the eye height are different for both tools. In ADS, like it is shown in Figure 4.9, the eye height is calculated with the distance between the 3-sigma points of the logic-1 and logic-0 histograms level [19]. The measurements of

eye height in SPITDS were made taking the maximum distance. This different way of measuring may cause some differences between the voltage values obtained for the height eye on ADS and SPITDS.

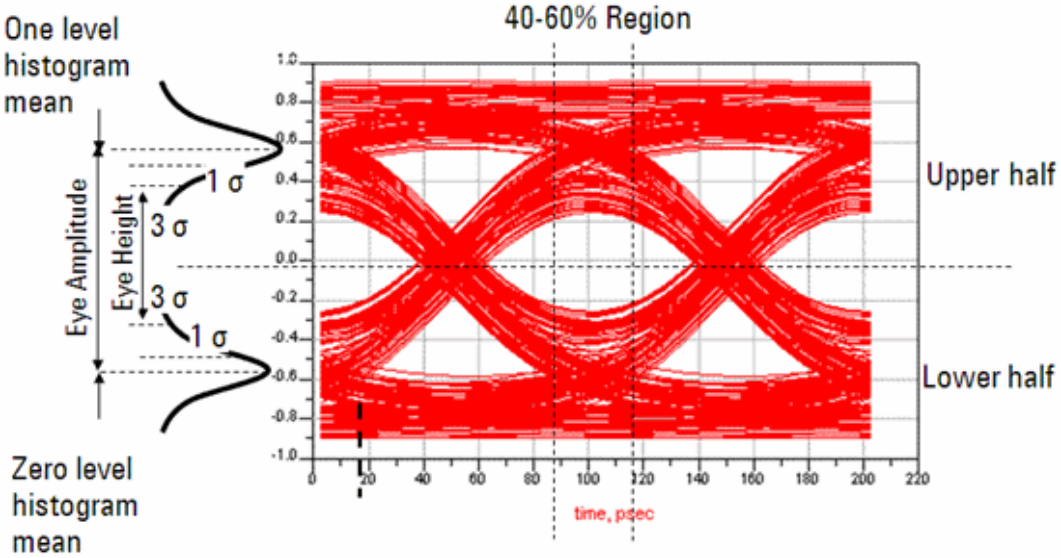


Figure 4.9 ADS eye height measurements, taken from [19].

4.3 Comparison of ADS and SPITDS Simulation Environments

In order to compare both FFE implementations results, simulations for different channel were done with a 256 bits (the minimum possible in SPITDS) to look more detailed into the similarities and with 10000 bits to get more realistic results. Like was explain in section 4.2 the eye diagrams are plotted using Eye Diagram FrontPanel. All the simulations in ADS and SPITDS were done with the same PRBS waveform with a level voltage from 0 V to 1 V.

The eye diagram for a simulation of a link of example A, describe in section 4.1.1, at 15 Gb/s without equalization is shown in Figure 4.10 . The eye diagram of SPITDS simulation and the eye diagram of ADS simulation with a 256 bits are shown in Figures 4.10 (a) and Figure 4.10 (b) respectively. Figure 4.10 (c) shown a visual comparison of these two simulation with few bits (256) and Figure 4.10 (d) with 10000 bits. The diagrams were superposed in order to see the differences between both simulations (see Figures 4.10 (e) and (f)).

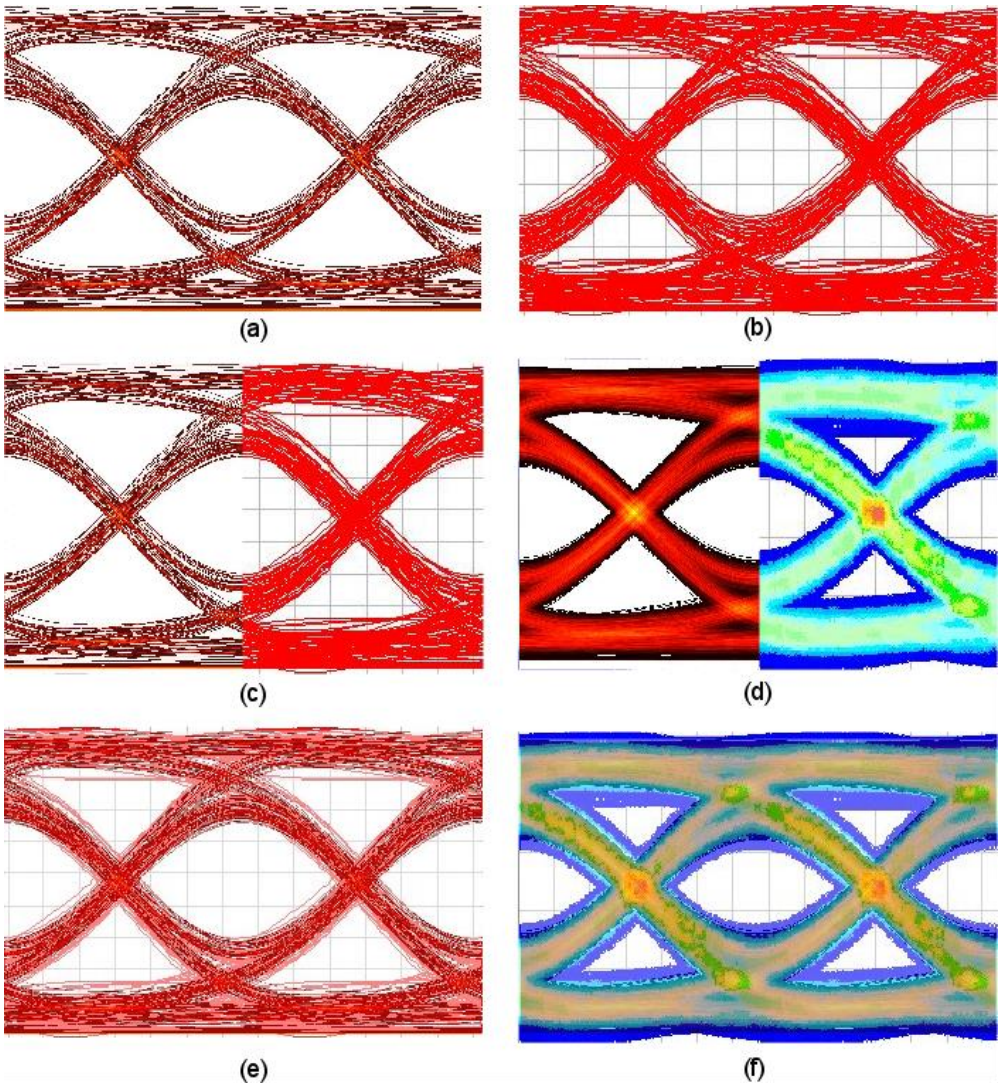


Figure 4.10 Visual comparison between SPITDS and ADS eye diagrams for a link of example A (section 4.1.1) at 15 Gb/s without equalization. (a) eye diagram of SPITDS simulation with 256 bits. (b) eye diagram of ADS FFE simulation with 256 bits. (c) comparison of ADS and SPITDS simulations with 256 bits. (d) comparison of ADS and SPITDS simulation with 10000 bits. (e) eye diagram from ADS and SPITDS with 256 bits eye superposed. (f) eye diagram from ADS and SPITDS with 10000 bits superposed. For (a), (b), (c) and (e) the vertical and horizontal scales are 10 ps per division and 0.1 V per division respectively. (d) and (f) have vertical and horizontal scales of 10 ps per division and 0.2 V per division respectively.

The eye diagram for SPITDS simulation has an eye opening of 297.6 mV meanwhile the eye diagram for ADS simulation has 264.35 mV. The small different between both simulations is because the tools used different way to measure the eye opening and plot the eye diagram like was explain in section 4.2. These results shown that the is easier to see the results when the samples are plotted with a lines like with SPITDS.

In the same way other two different links described in section 4.1 were simulated. The results are compared and shown in Figure A-4.1, Figure A.4.2 and Figure A.4.3 in Appendix A. It can be observed the same results for these simulations, where the main different are because the different way to measure the eye opening.

4.4 Evaluation of FFE Equalization with the LMS Tap Adaptation Algorithm

In this section simulations for different links are present in order to see the effect of the equalization for different channels in both implementations. Also, is proven of the correct operation of both implementations with the same algorithm. The calculation of the values of the taps is performed using the LMS implementation in MATLAB. This because the algorithm work for both FFE implementation and is possible compare the results directly.

For each channel the LMS algorithm was applied separately and different values for the equalization were obtained. All the simulations in ADS and SPITDS were done with the same PRBS waveform with a level voltage from 0V to 1V.

For this simulation was used 4 taps for both FFE implementations, one pre-cursor, main cursor and two post-cursors.

4.4.1 Comparisons Using ADS Transmission Line Model

For this link different data rate (5 Gb/s, 7 Gb/s and 9Gb/s) was used in order to see the effect of the FFE equalization in this channel. The transmission parameters magnitude for the fundamental frequencies of these data rate used in the simulations for ADS transmission line model (section 3.2) are shown in Figure 4.11.

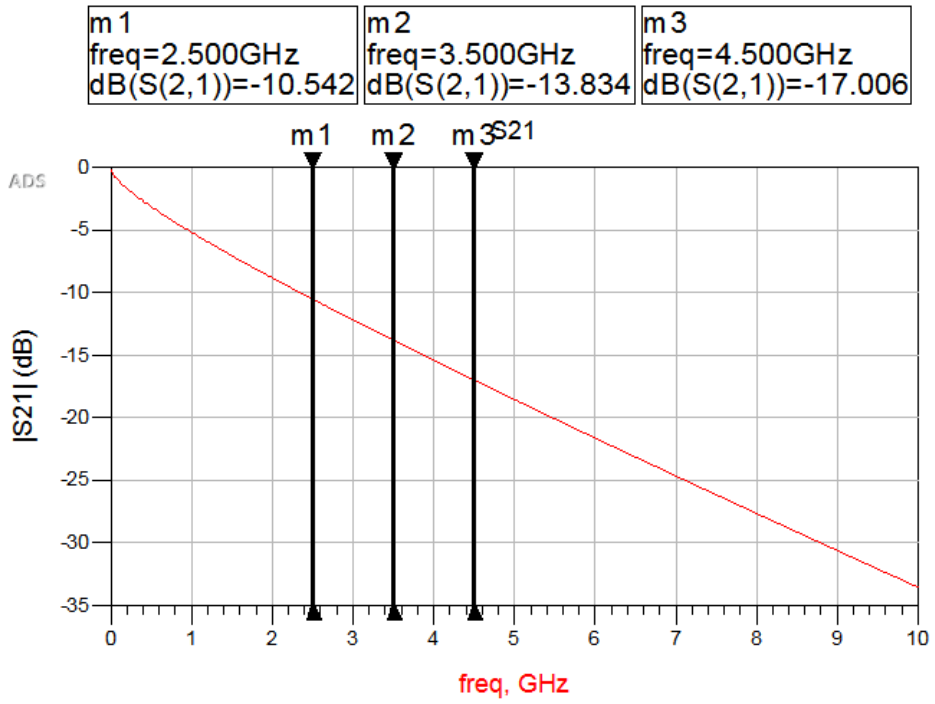


Figure 4.11 Transmission parameter magnitude for the ADS transmission line model (section 3.2) simulations. The three fundamental frequency for 5, 6 and 9 Gb/s are shown.

The taps values obtained with LMS MATLAB algorithm and used for applied the equalization of this link at different data rate are shown in Table 4.1.

Table 4.1 Taps values obtained for the FFE using a ADS transmission line model (section 3.2).

Data rate (Gb/s)	Precursor tap	Main tap	1st Post-cursor tap	2nd Post-cursor tap
5	-0.013	1	-0.211	-0.115
7	-0.0138	1	-0.235	-0.1156
9	-0.0145	1	-0.247	-0.1164

The results from the simulation without and with equalization at 5 Gb/s are shown in Figure 4.12. It can be observed the voltage of the eye height on ADS and SPITDS

eye diagrams increase because the FFE counteracts the losses of the channel. The voltage values for these two tool simulators are different mostly because of the different way to measure the eye height (see section 4.2).

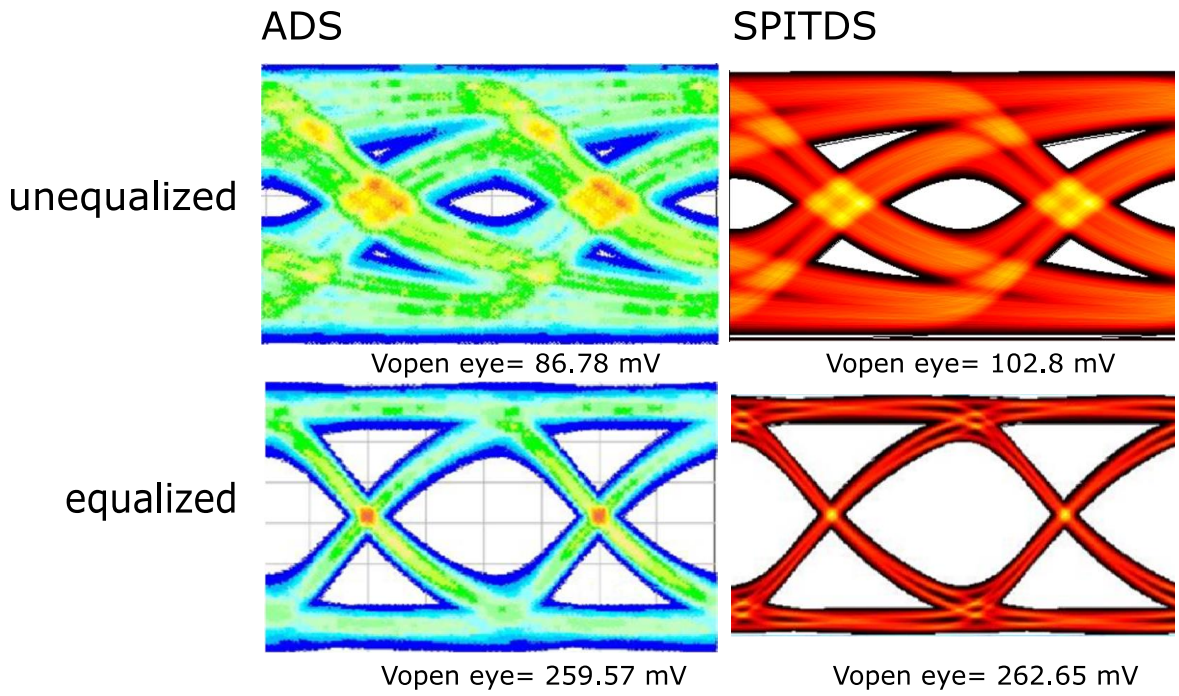


Figure 4.12 Eye diagram comparison of ADS and SPITDS simulations for ADS transmission line model (section 3.2) with equalization at 5 Gb/s with 10000 bits. The vertical and horizontal scales are 50 ps per division and 0.1 V per division respectively.

In Figure 4.13 can be observed how as the channel impairments worsen the eye is closed without equalization when the data rate is increase to 7 Gb/s. When the equalization is applied, the height of the eye increases and the signal can be recovered.

The data rate is increased to 9 Gb/s and the eye diagram without equalization are completely closed (see Figure 4.14). When the FFE equalization with the values obtained from LMS adaptation algorithm is applied, the eye opening for ADS implementation is of 50.59 mV meanwhile for SPITDS implementation is 73.89 mV. In this case even though the effect of the FFE equalization is visible it may not be enough to recover signal.

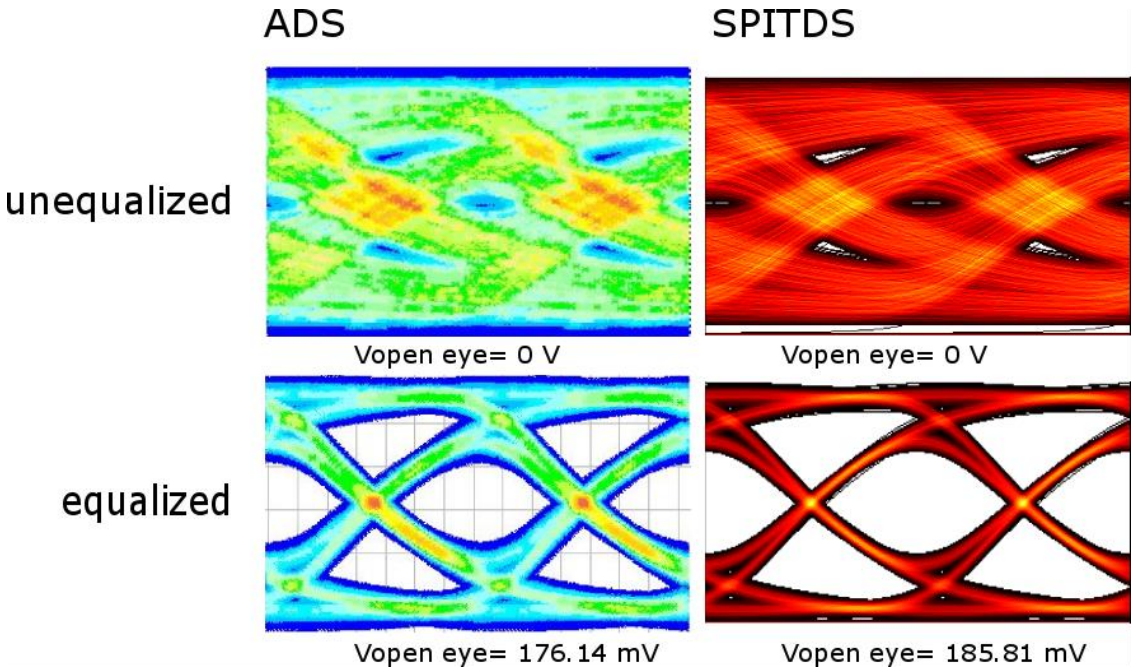


Figure 4.13 Eye diagram comparison of ADS and SPITDS simulations for ADS transmission line model (section 3.2) at 7 Gb/s with 10000 bits. The vertical and horizontal scales are 20 ps per division and 0.1 V per division respectively.

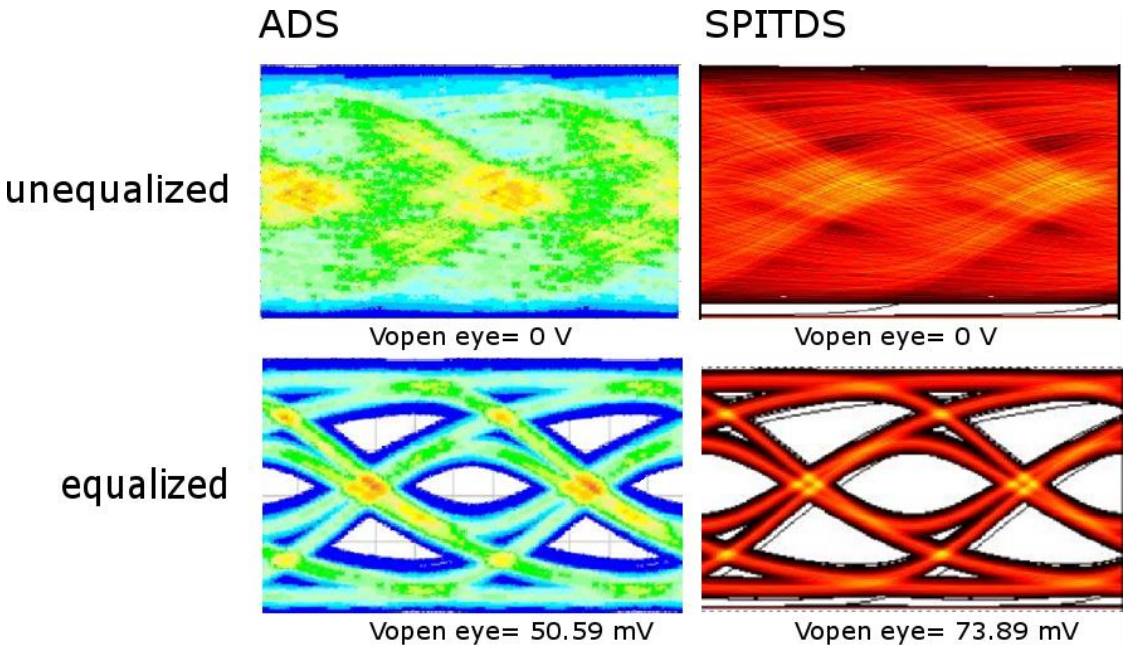


Figure 4.14 Eye diagram comparison of ADS and SPITDS simulations for ADS transmission line model (section 3.2) at 9 Gb/s with 10000 bits. The vertical and horizontal scales are 20 ps per division and 0.1 V per division respectively.

As is expect the signal worsen when the data rate is increased. With the equalization the high frequency losses are counteracted partially, making the eye opening visible.

Also, it is important to look the similarities results between both FFE implementation and the importance of using an adaption algorithm to adjust the taps values in order to obtain a more effective equalization

4.4.2 Comparisons Using Backplane Simulated Links

The link of example A (section 4.1.1) are simulated with three different data rates (10 Gb/s, 15 Gb/s and 20 Gb/s). The fundamental frequency used for the simulation and the transmission parameters are shown in Figure 4.15.

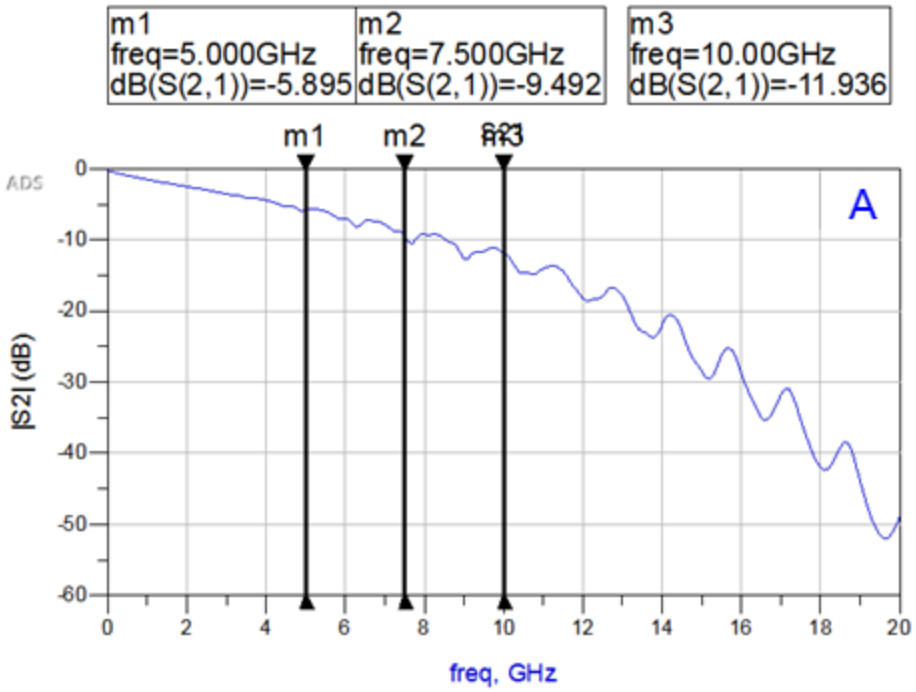


Figure 4.15 Transmission parameter magnitude for the link of example A (section 4.1.1**¡Error! No se encuentra el origen de la referencia.**) simulations. The three fundamental frequency for 10, 15 and 20 Gb/s are shown.

The taps values obtained with LMS algorithm and used for the equalization of this link at different data rate are shown in Table 4.2.

Table 4.2 Taps values obtained by LMS algorithm for the FFE using a link of example A (section 4.1.1).

Data rate (Gb/s)	Precursor tap	Main tap	1st Post-cursor tap	2nd Post-cursor tap
10	-0.12	1	-0.0418	-0.0167
15	-0.2053	1	-0.04389	-0.0172
20	-0.3083	1	-0.0509	0.024

The link with a data rate of 10 Gb/s is simulated. For this data rate, because of the channel characteristic, without equalization the eye is open and the signal can be recovered. When the equalization is applied does not have a bigger effect on the signal (see Figure 4.16). For the ADS FFE simulation the eye opening increase 70.4 mV and in SPITDS FFE simulation 125.8 mV and the signal remains recoverable.

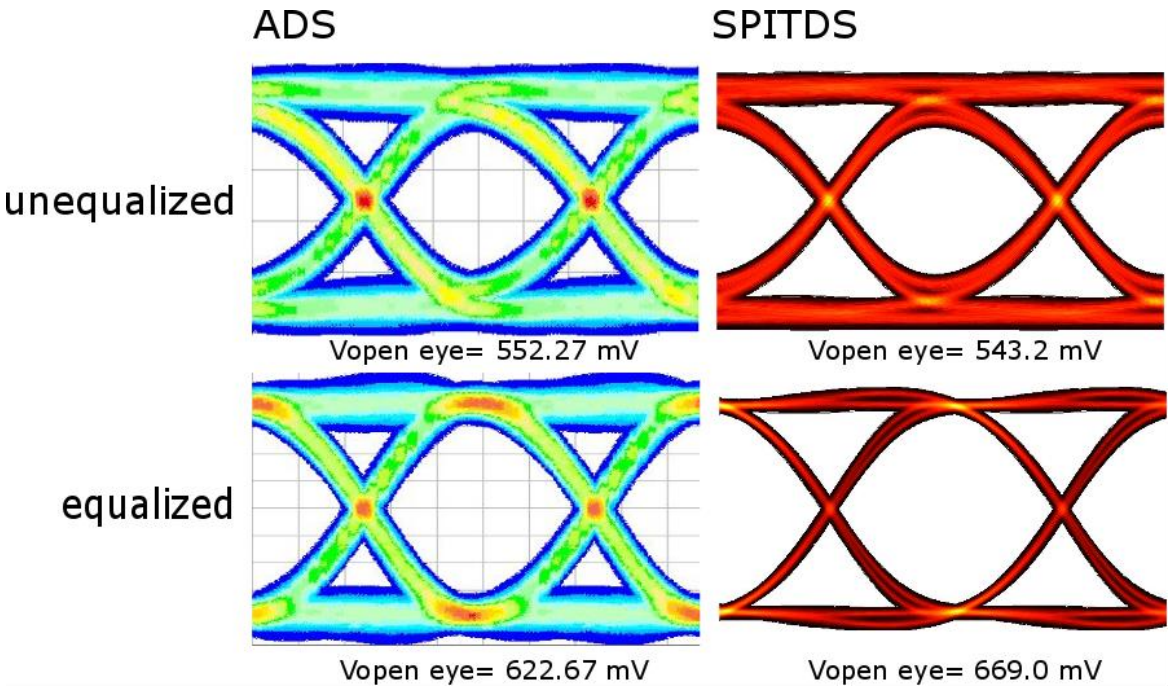


Figure 4.16 Eye diagrams comparison between SPITDS and ADS simulations for a link of example A (section 4.1.1) at 10 Gb/s with 10000 bits. The horizontal scale for all figures is 20 ps per division, the vertical scale is 0.2 V for the unequalized signal and 0.1 V for equalized signal diagrams.

When the data rate is increase to 15 Gb/s the eye diagram without equalization is more closed than at 10 Gb/s. However, when the equalization is applied the eye height is increased, like is shown in Figure 4.17.

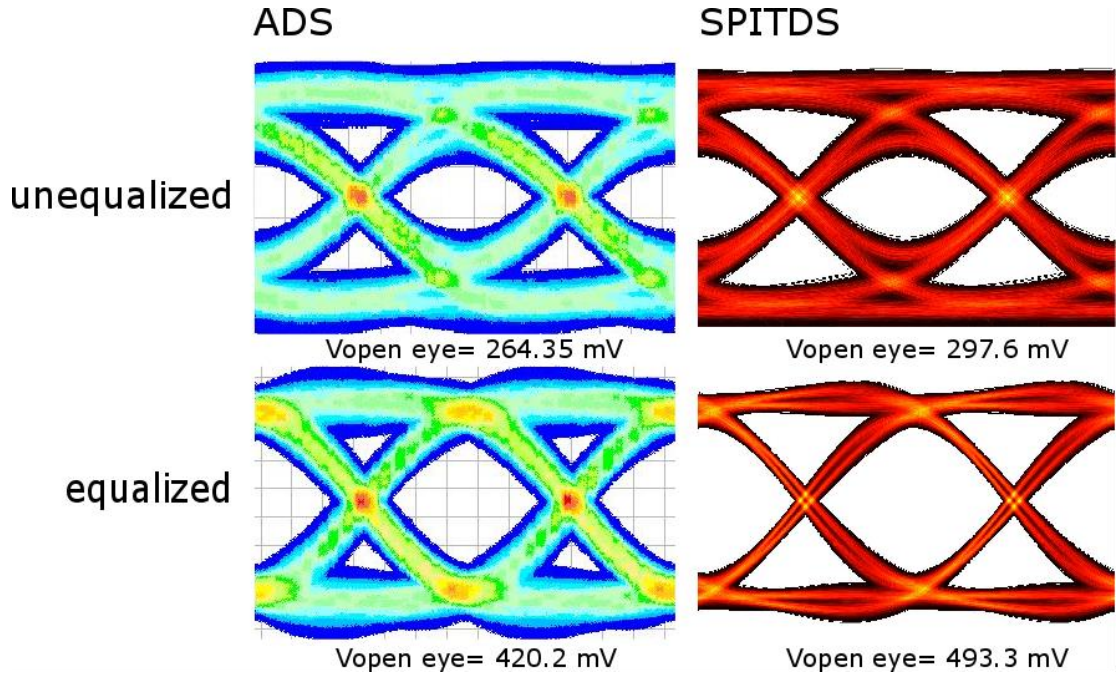


Figure 4.17 Eye diagrams comparison between SPITDS and ADS simulations for a link of example A (section 4.1.1) at 15 Gb/s with 10000 bits. The horizontal scale for all figures is 20 ps per division but the vertical scale is 0.2 V for the unequalized signal and 0.1 V for equalized signal diagrams.

The data rate is increased to 20 Gb/s. With this data rate there are more losses, and, like it is shown in Figure 4.18, without equalization it is not possible to recover the signal. When the equalization is applied the eye height increases and it may be possible to recover the signal but this depend of the receiver capability.

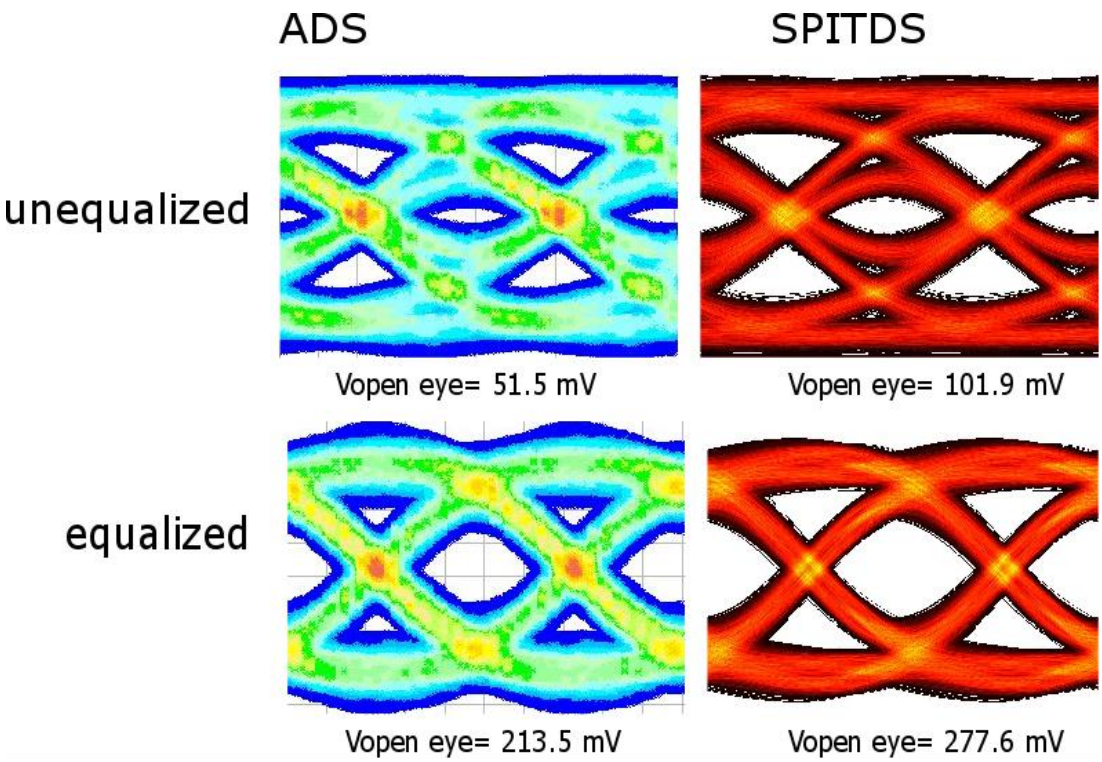


Figure 4.18 Eye diagrams comparison between SPITDS and ADS simulations for a link of example A (section 4.1.1) at 20 Gb/s with 10000 bits. The horizontal scale for all figures is 10 ps per division but the vertical scale is 0.2 V for the unequalized signal and 0.1 for equalized signal diagrams.

The link of example B (section 4.1.1) is selected in order to test the equalizer with a link with more loses. Two different data rate for the simulations were used, one where the fundamental frequency is located in a first little oscillation in the transmission parameters magnitude and another located near of the notch like is shown in the Figure 4.19. This in order to test the equalizer in extreme cases where do not recover the signal.

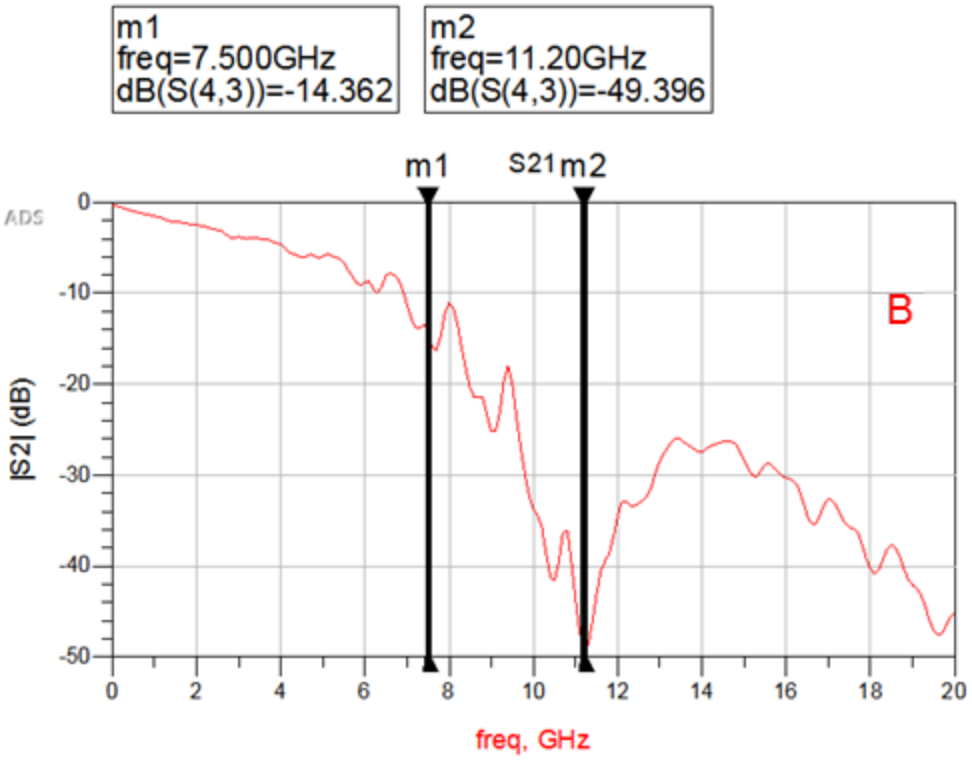


Figure 4.19 Transmission parameters magnitude for thee link of example B (4.1.1) simulations. The two fundamental frequency for 15 and 22.4 Gb/s are shown.

The taps values with LMS adaptation algorithm were obtained and used for the equalization of this link at different data rate are shown in Table 4.3.

Table 4.3 Taps values obtained for the FFE using LMS algorithm for a link of example A (section 4.1.1) at different data rates.

Data rate (Gb/s)	Precursor tap	Main tap	1st Post-cursor tap	2nd Post-cursor tap
15	-0.3302	1	-0.02624	-0.2104
22.4	-0.3198	1	-0.0652	0.0085

First simulations are done with a 15 Gb/s data rate and in this case like Figure 4.20 shows, with the equalizer the eye height increases.

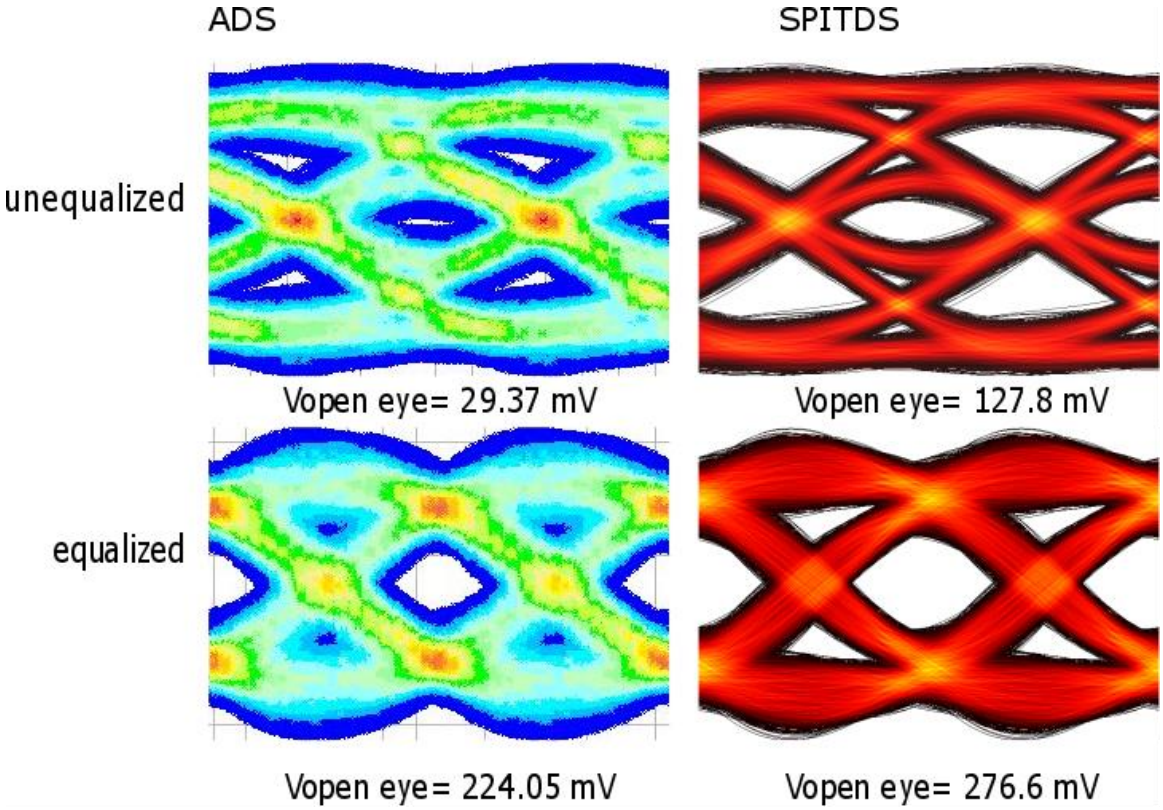


Figure 4.20 Eye diagrams comparison between SPITDS and ADS simulations for a link of example B (section 4.1.1) at 15 Gb/s. The vertical and horizontal scales are 10 ps per division and 0.2 V per division respectively.

When the data rate is increased to 22.4 Gb/s the fundamental frequency is located near of the notch (see Figure 5.15) where do not receive transmission and in this case the equalizer cannot recover the channel (compare with Figure 4.21).

In order to find a way to recover the channel, the numbers of taps are increased to 8, using different combination of number of pre cursor taps and post-cursor, adjusted with the LMS algorithm. However, the height of the cannel did not increase noticeably.

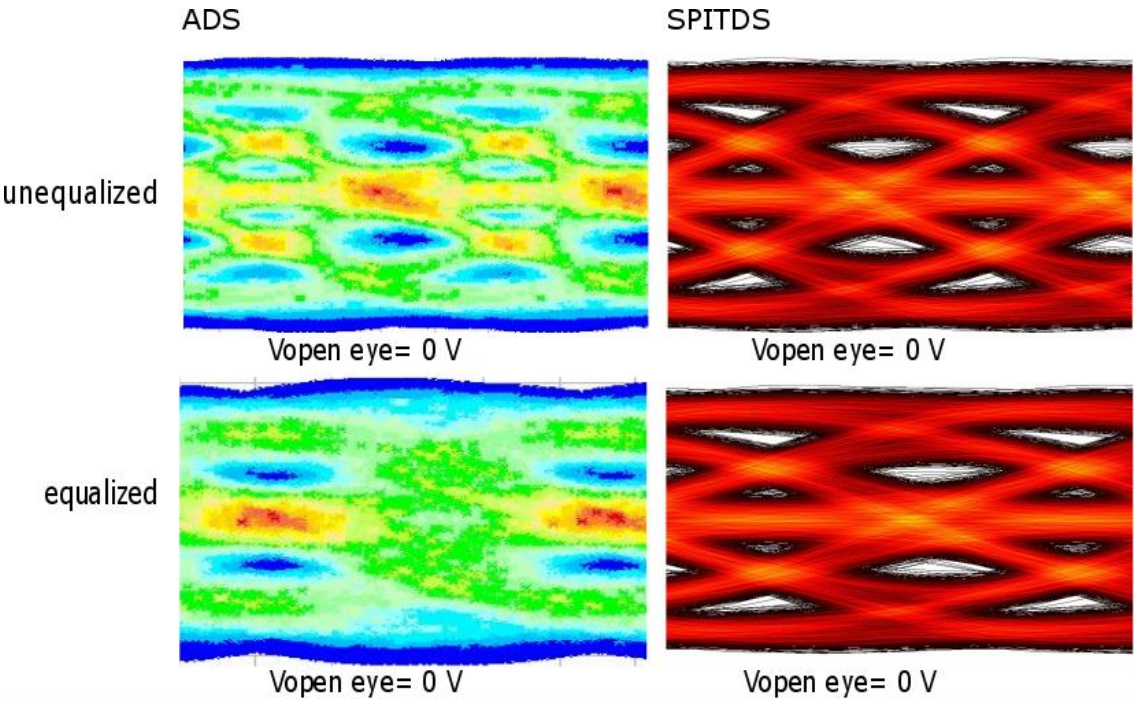


Figure 4.21 Eye diagrams comparison between SPITDS and ADS for a link of example B (section 4.1.1) at 22.4 Gb/s, near of the notch. The vertical and horizontal scales are 10 ps per division and 0.1 V per division respectively.

4.4.3 Comparisons Using Semianalytical Models with Stub Effect

For the simulation the model described in section 4.1.2 was used, with a 5000 mil of the length (L).

The taps values for the FFE calculated by LMS algorithm for a semianalytical model is shown in Table 4.4.

Table 4.4 Taps values obtained for the FFE using a Semianalytical Model with Stub Effect (section 4.1.2).

Data rate (Gb/s)	Precursor tap	Main tap	1st Post-cursor tap	2nd Post-cursor tap
18	-0.1819	1	-0.2072	-0.0077

Figure 4.22 shows the eye diagram without and with equalization at 18 Gb/s with 10000 bits using the taps values of Table 5.4. It can be observable the equalization increases the height of the eye in both simulations. But, if the results from ADS simulation with SPITDS simulation are compared. There are some lines which have different amplitudes, making the difference between these simulations more noticeably. This can be attributed in part to the different approaches to plot the eye diagrams by different tools and the small transmission value for the case evaluated at the stub resonance. To see the differences in more detail, a link without equalization with 256 bits and 10000 bits was simulated. In this comparison, the differences of the simulations are more evident (see Figure 4.23).

Like can be observed in Figure 4.22 and Figure 4.23 the differences between this simulation increase with the frequency increases.

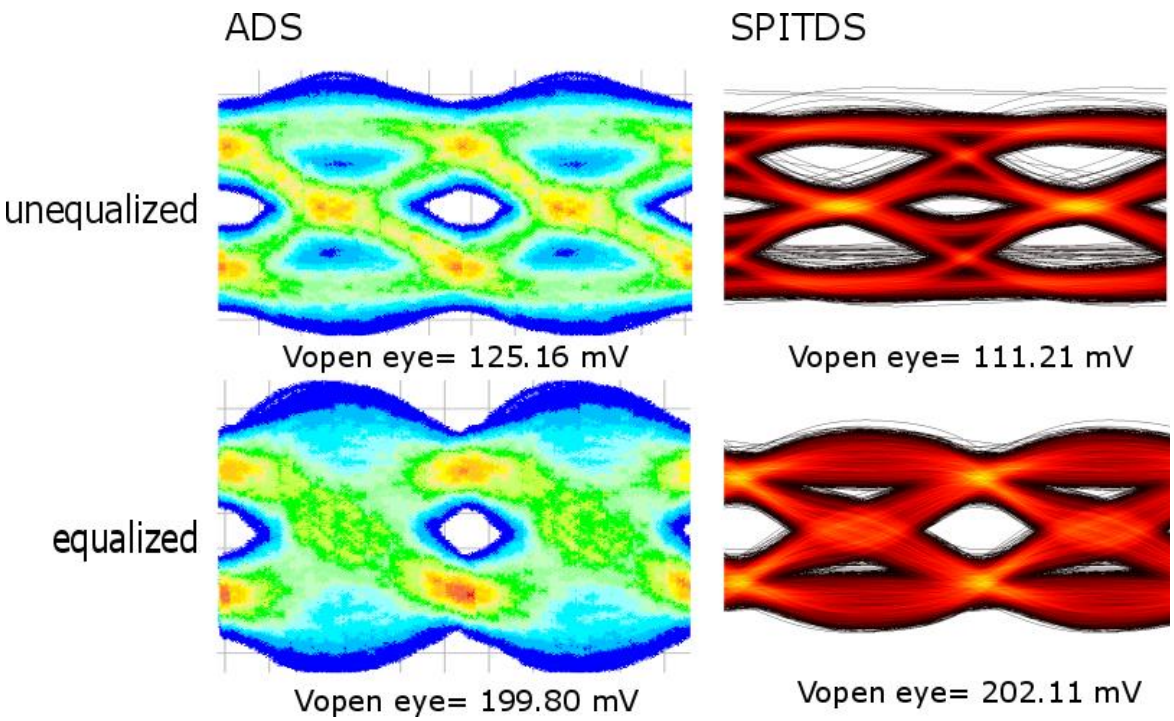


Figure 4.22 Eye diagram comparison for MLSS model with 5000 mil of length (L=5000 mil) for the trace (section 4.1.2) at 18 Gb/s with 1000 bits. The vertical and horizontal scales are 10 ps per division and 0.2 V per division respectively.

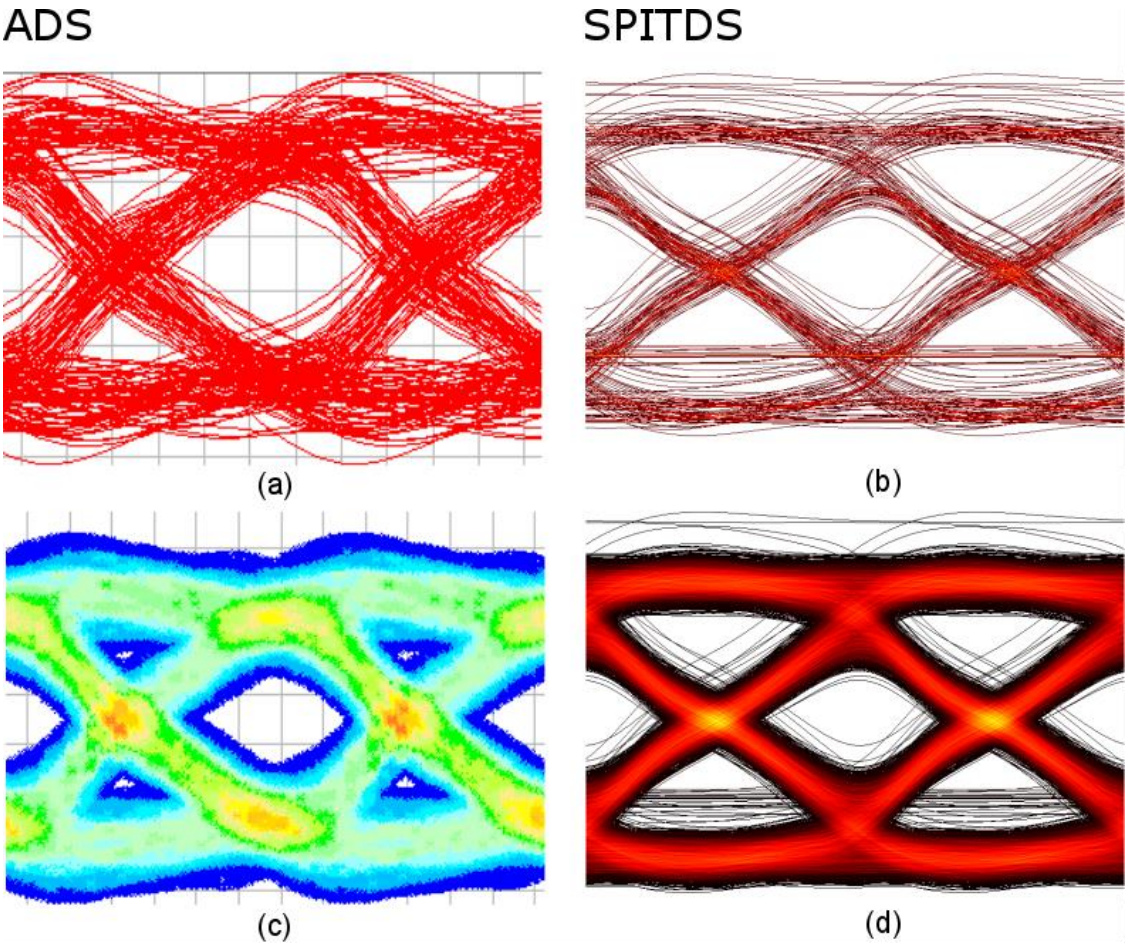


Figure 4.23 Comparison between SPITDS and ADS eye diagrams for a link of example section 4.1.2 at 15 Gb/s without equalization. (a) eye diagram from ADS with 256 bits. (b) eye diagram from SPITDS with 256 bits. (c) eye diagram from ADS with 10000 bits. (b) eye diagram from SPITDS with 10000 bits. (c). The vertical and horizontal scales are 10 ps per division and 0.2 V per division respectively

5 Conclusions and recommendations

5.1 Conclusions

A parameterized FFE equalizer was successfully implemented in ADS and programmed in SPITDS. The LMS algorithm for tap adaptation in ADS and MATLAB was implemented. The implementations were tested and evaluated through several high-speed link simulation scenarios with good results.

The benefits of the FFE equalizations could be observed in several cases where the degradation introduced by the channel is not too large. From the comparisons made, since there are no significant differences between ADS and SPITDS simulations, it can be said that the implementation in SPITDS is reliable for simulated channels. Channels with a maximum loss of -20 dB at the fundamental frequency could be recovered by 4-tap FFE equalization.

The FFE implemented in SPITDS, in conjunction with the LMS adaptation algorithm, permit to try different number and values of pre-cursor and post-cursor taps for equalization in an easy and quick manner compared with ADS FFE implementation, which facilitates to observe and analyze the effect of the FFE equalization at simulation level. The main contribution of this work are the creation of these FFE parameterized models that can be used to the fast evaluation of channels and assess the effect of the FFE equalization as a function of channel characteristics and equalization settings (numbers of taps, ranges, etc.).

5.2 Recommendations

From the results obtained, the following aspects can be addressed in the future:

The LMS algorithm implemented in MATLAB could be developed with a vectorized approach or using another lower-level programming language in order to improve its numerical efficiency, because the MATLAB implementation is relatively slow, in particular when executing loops.

The configuration file in SPITDS could be modified to allow the definition an arbitrary number of taps for the FFE implementation in order to set the number of equalizer taps easily. Further examples with different channels, where the crosstalk is included could be analyzed to observe, for instance, the effect of equalization in these cases.

The differences between ADS and SPITDS to plot and measure eye diagram metrics should be considered in the comparisons, because it can induce erroneous conclusions. The eye diagrams from the example in the section 4.4.3 did not result very similar. This difference could come from the way the eye diagrams are generated. However, this issue requires further investigation.

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Appendix A: Figures

The details of the components used for the FFE equalizer implementation is shown in Figure A.3.1.

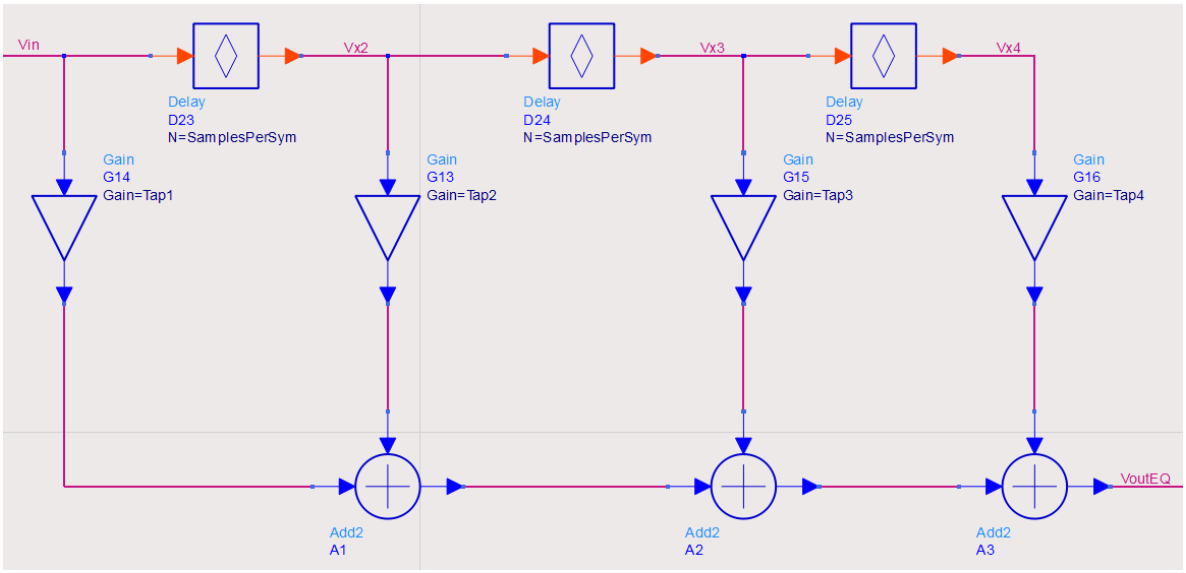

Figure A.3.1 Detail diagram of the implementation for FFE equalizer in ADS.

The FFE implemented in ADS for a different channel using a s-parameters block is shown in Figure A.3.2.

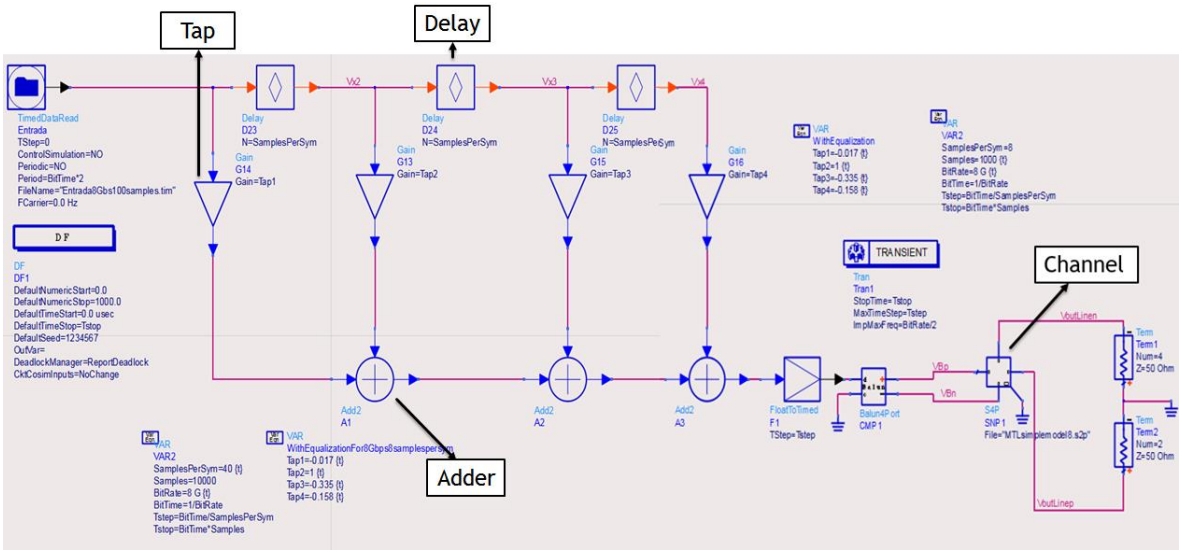

Figure A.3.2 Diagram of the implementation for FFE equalizer in ADS for a differential channel using a s-parameters block.

Figure A.3.3 shows the LMS implementation in MATLAB using a s-parameters block.

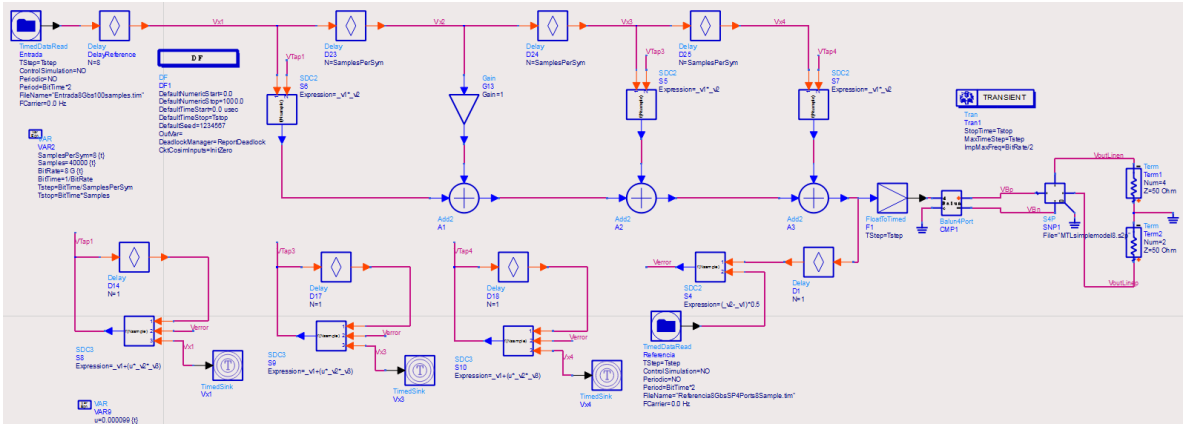

Figure A.3.3 Diagram of FFE with LMS algorithm ADS differential channel implementation using a s-parameters block.

Figures A.4.1, A.4.2 and A.4.3 show the simulations for different channel done with a 256 and 10000 bits in order to compare the ADS and SPITDS FFE implementation. Like was explain in section 4.2 the eye diagrams are plotted using Eye Diagram FrontPanel. All the simulations in ADS and SPITDS were done with the same PRBS waveform with a level voltage from 0 V to 1 V.

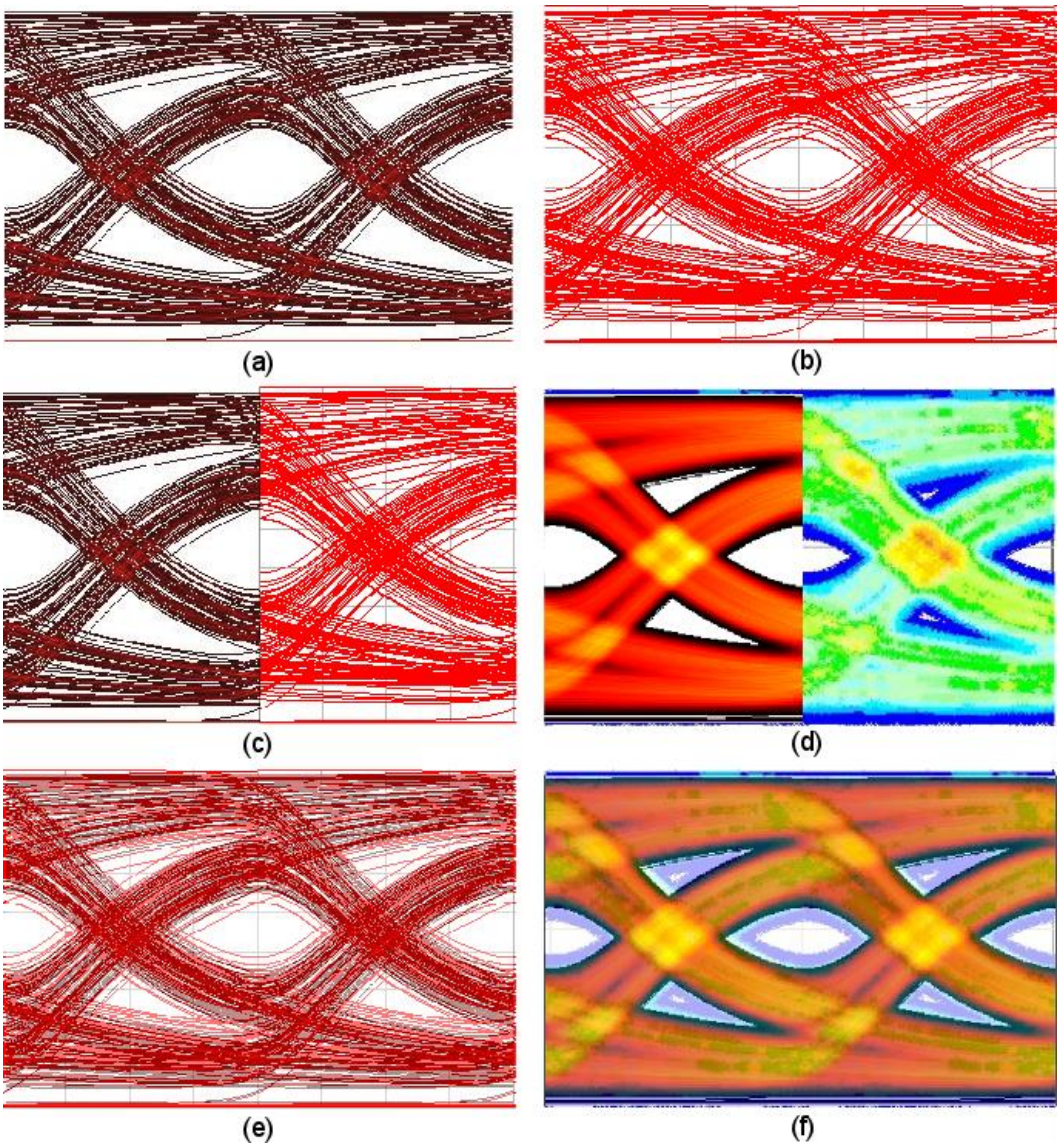

Figure A.4.1 Comparison between SPITDS and ADS eye diagrams for ADS transmission line explained in the section 3.2 at 5 Gb/s without equalization. (a) eye diagram of SPITDS simulation with 256 bits. (b) eye diagram of ADS FFE simulation with 256 bits. (c) comparison of ADS and SPITDS simulations with 256 bits. (d) comparison of ADS and SPITDS simulation with 10000 bits. (e) eye diagram from ADS and SPITDS with 256 bits eye superposed. (f) eye diagram from ADS and SPITDS with 10000 bits superposed.

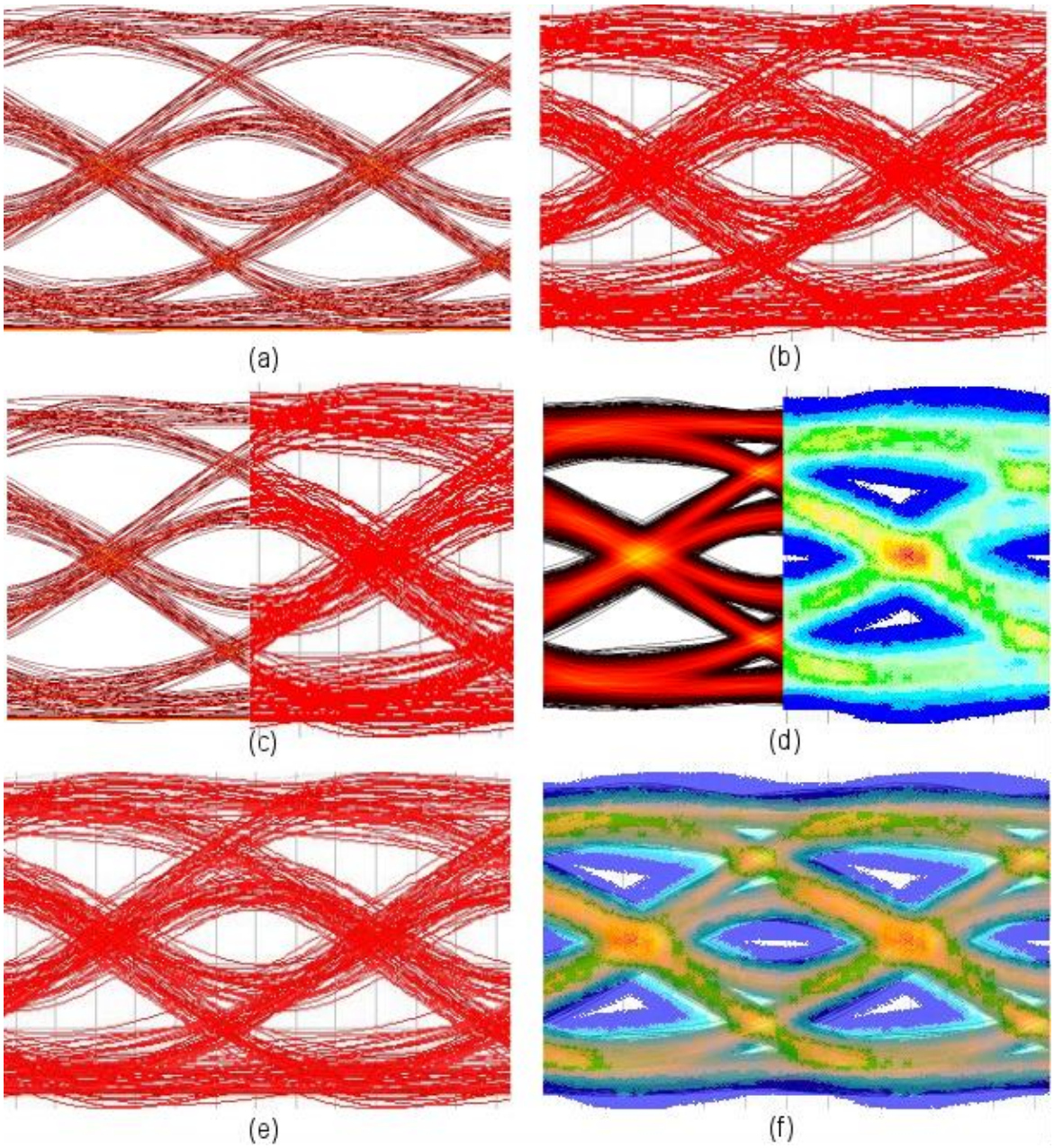

Figure A.4.2 Comparison between SPITDS and ADS eye diagrams for a link of example B (section 4.1.1) at 15 Gb/s without equalization. (a) Eye diagram from SPITDS with 256 bits. (b) eye diagram from ADS with 256 bits. (c) comparison of ADS and SPITDS with a 256 bits. (d) comparison of ADS and SPITDS with 10000 bits. (e) eye diagram from ADS and SPITDS with 256 bits eye superposed. (f) eye diagram from ADS and SPITDS with 10000 bits eye superposed.

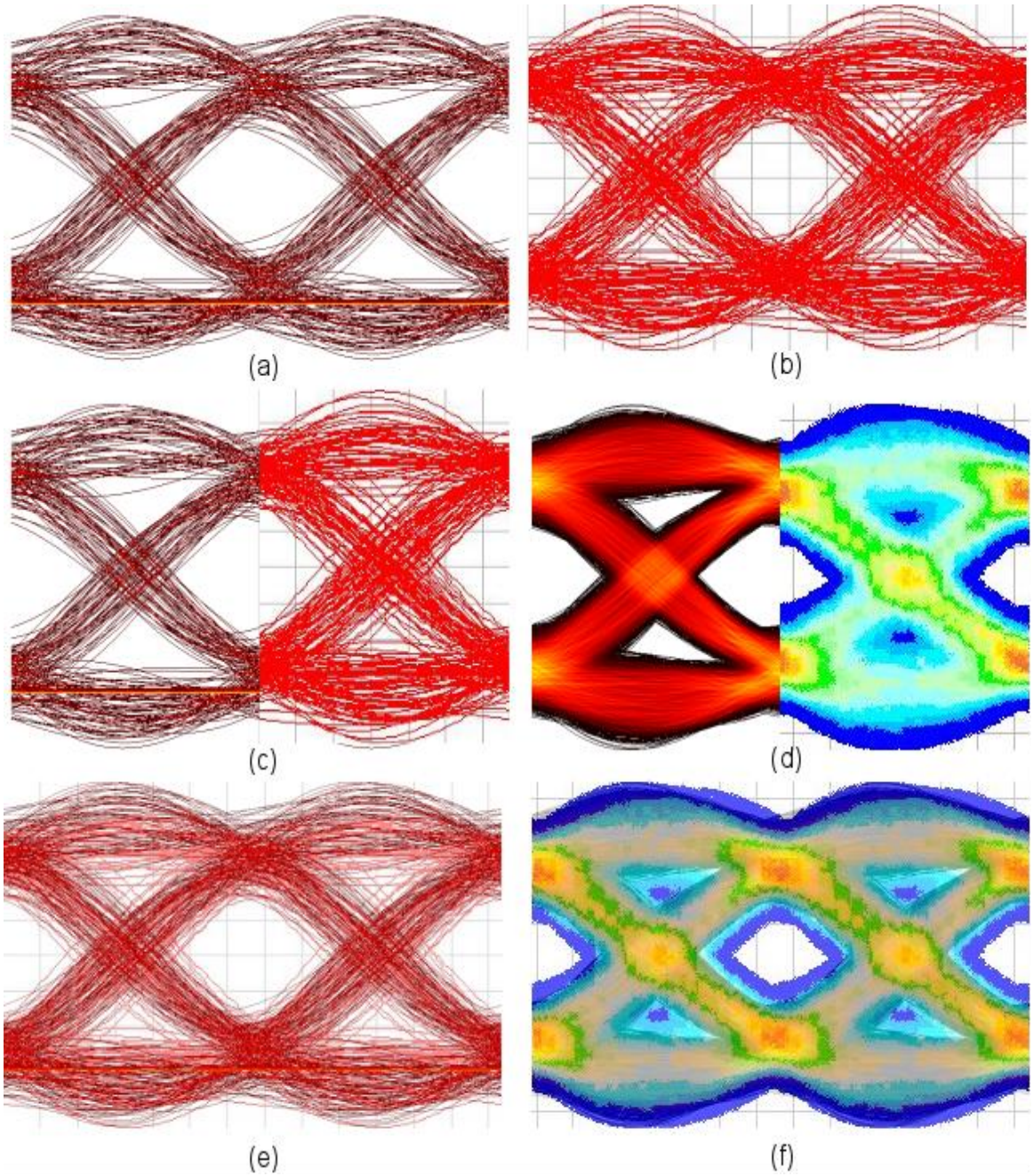

Figure A.4.3 Comparison between SPITDS and ADS eye diagrams for a link of example B (section 4.1.1) at 15 Gb/s with equalization. (a) Eye diagram from SPITDS with 256 bits. (b) eye diagram from ADS with 256 bits. (c) comparison of ADS and SPITDS with a 256 bits. (d) comparison of ADS and SPITDS with 10000 bits. (e) eye diagram from ADS and SPITDS with a 256 bits eye superposed. (f) eye diagram from ADS and SPITDS with 10000 bits eye superposed.