

# An ECG-on-Chip with QRS Detection & Lossless Compression for Low Power Wireless Sensors

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**Abstract**— This paper presents the design of a low power 3-lead ECG-on-Chip with integrated real-time QRS detection and lossless data compression for wearable wireless ECG sensors. Data compression and QRS detection can reduce the sensor power by up to 2 to 5 times. A joint QRS detection and lossless data compression circuit allows computational resources to be shared among multiple functions, thus lowering the overall system power. The proposed technique achieves an average compression ratio (CR) of 2.15 times on standard test data. The QRS detector achieves a sensitivity (Se) of 99.58% and positive productivity (+P) of 99.57% @ 256Hz when tested with the MIT/BIH database. Implemented in 0.35 $\mu$ m process, the circuit consumes 0.96 $\mu$ W @2.4V with a core area of 1.56mm<sup>2</sup> for 2-channel ECG compression and QRS detection. Small size and ultra-low power consumption makes the chip suitable for usage in wearable/ambulatory ECG sensors.

## I. INTRODUCTION<sup>1</sup>

Cardiovascular disease (CVD) causes 31% of all global deaths[1] and is one of the leading causes of death worldwide. The management of CVDs requires significant healthcare resources, especially with a fast aging population and universally increasing life expectancies. An effective way to address this problem is to use low cost wireless wearable sensors for vital signs monitoring such that proactive measures can be taken as needed, which leads to prevention-oriented health and wellness management. Wearable sensors, such as one shown in Fig. 1, are essential to acquire, process and wirelessly transmit vital signs to a personal gateway/cloud server for remote monitoring. The main challenges involved in the development of a wearable sensor is to make it low profile, unobtrusive, user friendly, and with long battery life for continuous usage. A high level of integration with signal acquisition and data conversion can minimize the size, cost and power consumption of these sensors [2], [3].

The major source of power consumption in a wearable sensor is the wireless transceiver. An effective way of lowering the power consumption is to minimize the use of the transceiver, i.e. to transmit information rather than raw data. For an ECG (electrocardiogram) sensor, it is desirable to perform preliminary ECG signal analysis like QRS detection and R-R interval estimation locally. This allows the transmission to be triggered only when it is deemed necessary based on cardiac analysis, and thus reduce the system power [4]. Furthermore, the large quantity of ECG data obtained by round the clock monitoring may need to be either stored locally in a flash memory or transmitted wirelessly to a gateway for further analysis. The transmission of data and/or local storage incurs high power consumption, and increases the device cost.

Data compression is effective in reducing the data rate for either transmission or storage and thus reduce the system power. Lossy data compression techniques provide

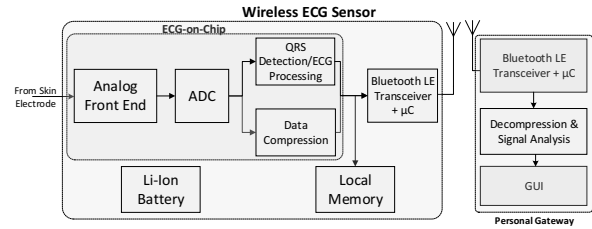


Fig.1 Wireless ECG Monitoring System Block diagram

higher CR, but they are not well suited for ECG signal due to potential loss of diagnostic value and thereby lacking regulatory approvals. Thus, lossless data compression is preferred for ECG. In the context of wearable sensors, ultra-low power operation and low complexity in implementation are critical. There is a need to find a balance between CR and complexity.

In recent years, several QRS detection algorithms with low power features were reported [4], [5]. At the same time, discrete/integrated lossy, lossless data compression techniques were developed for wearables/bio-devices [6]–[8]. Local data compression and QRS detection can reduce the sensor power by up to 2-5 times [4], [9]. It is worth noting that using two separate hardware blocks for QRS detection and compression will result in higher overall system complexity and power. Thus a joint QRS detection and lossless data compression algorithm, which shares processing engine between the two tasks is desirable [10].

In this paper, a novel ECG-on-Chip featuring a joint QRS detector and lossless data compressor (JQDC) is presented [11]. A low power architecture for JQDC along with its implementation is presented together with an ECG front-end. This joint approach lowers system power compared to using independent QRS detection and compression hardware. To the best of our knowledge, this is the first reported device, which jointly performs lossless compression and QRS detection with shared hardware. Implemented in 0.35 $\mu$ m process, the circuit consumes 0.96 $\mu$ W@2.4V with a core area of 1.56mm<sup>2</sup> for 2-channel ECG compression and QRS detection. The chip achieves an average CR of 2.15x at 256Hz and a QRS detection sensitivity (Se) of 99.58% and positive productivity (+P) of 99.57%.

The paper is organized as follows. In Section II, the system architecture of the ECG-on-Chip is discussed. Section III and IV details the analog front-end and ADC. A short discussion of the Joint QRS detection compression scheme is given in Section V. Section VI presents the low power hardware architecture of the JQDC processor. Performance evaluation and measurement results are given in Sections VII and VIII, respectively.

## II. SYSTEM ARCHITECTURE OF ECG ON CHIP

The entire system is illustrated in Fig. 2. It includes an AFE (analog front-end) for 3-lead ECG acquisition (2 measured & 1 derived lead for standard 3-lead ECG), a 12-

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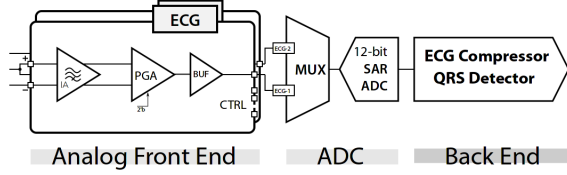


Fig. 2 System architecture of the proposed ECG-on-Chip

bit SAR ADC, a lossless data compressor, and a QRS detector. The ECG signals are first amplified through an AC-coupled low-noise instrumentation amplifier (IA) and band-pass filtered. The programmable gain amplifier (PGA) provides variable gains from 49-67dB to maximize the dynamic range. An output buffer (BUF) is used to improve the analog output settling for the sample-and-hold in the multiplexer (MUX). After digitized by the ADC, the signal is further processed by the backend processor that consists of the joint QRS detector and lossless compressor.

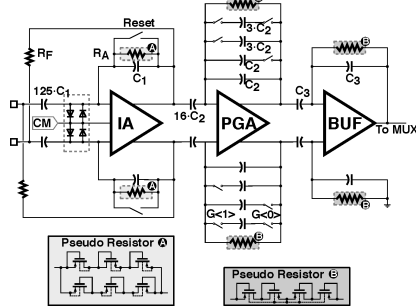


Fig. 3 Architecture of a single amplifier channel for ECG acquisition

### III. ANALOG FRONT-END

Fig. 3 shows the architecture of a single-channel ECG AFE. All three stages-the IA [12], the PGA, and the BUF-are AC-coupled using capacitors to block the DC offsets. The high-pass cut-off frequency is determined by the first stage negative RC feedback through  $R_A$  and  $C_1$ . The output buffer is AC-coupled to support rail-to-rail output, without designing rail-to-rail input range at the cost of extra power.

Two pseudo resistors are used to meet the needs at different stage [13]. As the input voltage is limited, the A-type pseudo resistor is used for the first stage, where three diode-connected PMOS transistors are connected in series. To make the resistor symmetrical a mirrored copy is added in parallel. The resistance of the resistor is large enough to create a sub-0.1 Hz high-pass cut-off. For the 2<sup>nd</sup> and 3<sup>rd</sup> stages, the inputs are higher than that of the first stage, the A-type resistor does not provide high enough resistance to meet sub-0.1 Hz high-pass cut-off. Thus, a different pseudo resistor (marked B in Fig. 3) is used for the PGA and the BUF. The B-type resistor has much larger resistance across the full voltage range.

### IV. ANALOG TO DIGITAL CONVERTER

The data from the AFE is multiplexed using an analog multiplexer and fed into an ADC for conversion. A dual-capacitive-array structure is adopted to implement the rail-to-rail ADC [14]. The structure uses 2 capacitive arrays for quantization. Here resetting the large DAC array after every conversion is not required and only relatively smaller capacitors are switched, resulting in lower power consumption [10].

### V. JOINT QRS DETECTION-COMPRESSION

The block diagram of the proposed joint QRS detection and data compression scheme is illustrated in Fig. 4.

In this scheme, an adaptive linear predictor is used to estimate the current sample  $x(n)$  from the past  $m$  ECG samples. The predictor can closely estimate the future samples, including the P, T wave segments and the baseline variations in the ECG signal using (1) [10]. Here  $\hat{x}(n)$  is the estimate of  $x(n)$  and  $h^k$  are the predictor coefficients.

$$\hat{x}(n) = \sum_{k=1}^m h^k x(n-k) \quad (1)$$

$$e(n) = x(n) - \hat{x}(n) \quad (2)$$

The instantaneous prediction error,  $e(n)$  in (2), will be minimal, except for the QRS period, as shown in Fig. 5. In QRS segment, the predictor statistics are considerably different compared to other regions and hence will result in a higher prediction error. Therefore the prediction error is used as a marker to locate the QRS complex in the ECG.

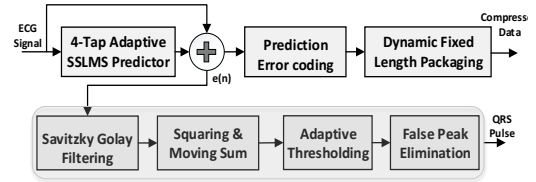


Fig. 4 Proposed joint QRS detection & data compression hardware

Linear prediction is widely used in redundancy reduction in data compression [7]. Since the prediction error contains QRS information, it implies that QRS detection and data compression can be jointly performed to share the computational load. This leads to an efficient, joint QRS detection and data compression implementation scheme.

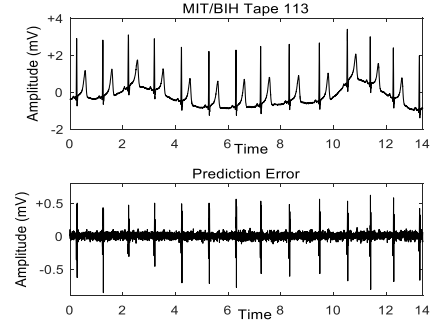


Fig. 5 ECG signal (top) and instantaneous prediction error,  $e(n)$  (bottom)

### VI. HARDWARE ARCHITECTURE OF JQDC PROCESSOR

For the proposed ECG-on-Chip, data from both ECG channels are compressed and data from a single lead is used for QRS detection. The data from the ECG front-end is serially multiplexed, as shown in Fig. 6, and hence has to be demultiplexed before further processing. The ECG is sampled at 256 Hz with 12-bit resolution. The chip uses a 512Hz clock for the processing because there are 2 channels. After each block, data bit widths are limited to a manageable number using truncation, saturation and round off techniques, so as to limit hardware complexity.

A detailed block diagram of the JQDC processor is shown in Fig. 6. The data from each channel is identified with a *channel select* (CS) header appended to the ECG sample by the ADC. Based on this, the incoming data is demultiplexed to form two ECG data streams for channels 1 and 2. Each of the data stream is fed into a separate adaptive predictor for computing the prediction error. The individual predictor is clock gated with the CS signal, which alternates the incoming 512Hz data into 2 separate streams running at an effective 256Hz clock.

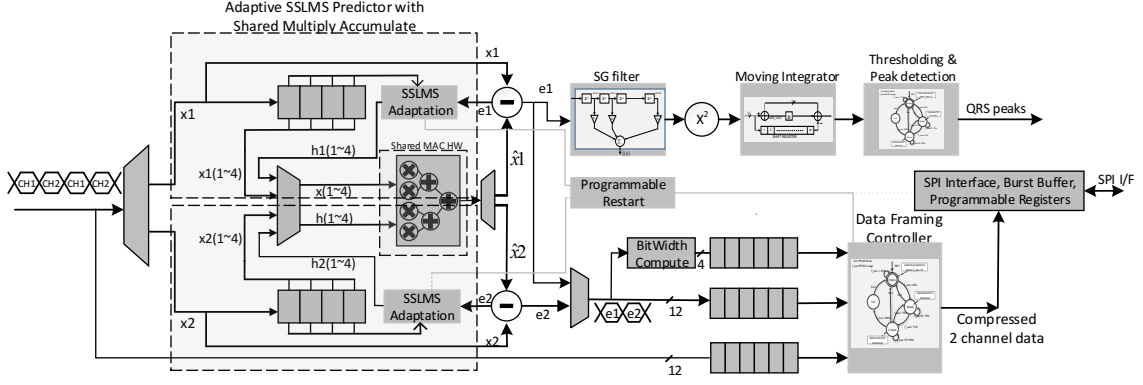


Fig. 6. Overall hardware Architecture of Joint QRS detector & Compression block. The multiply and accumulate block is shared across 2 ECG channels.

### A. SSLMS Adaptive Linear Predictor

The 4-tap adaptive predictor structure used to predict future samples based on past signal statistics is shown in Fig 7. Since the incoming data is serially multiplexed between 2 channels, the multiply-accumulate logic in the predictor is shared by multiplexing the inputs to save the hardware costs as shown in Fig 6.

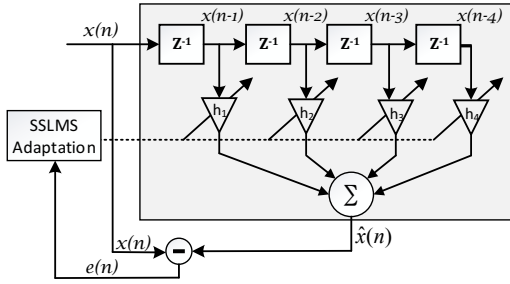


Fig. 7 Four-Tap Adaptive SSLMS Predictor used for linear prediction.

Predictor weights are updated using Sign-Sign Least Mean Square (SSLMS) adaptation (3).

$$h(n+1) = h(n) + \mu \cdot \text{sign}(e(n)) \cdot \text{sign}(x(n)) \quad (3)$$

Here  $\mu$  is the step size and  $h(n+1), h(n)$  are the updated and current predictor coefficients, respectively. The predictor coefficients are updated based on the instantaneous prediction error for every sample. In order to speed up the adaptation, the SSLMS predictor is initialized with pre-computed values  $h_{1i}, h_{2i}, h_{3i}, h_{4i}$  obtained from a training process during the design. A variable step  $\mu_{\text{eff}}$  is used to further speed up the adaptation process (4). Here  $N$  is the number of iterations and  $N_L$  is chosen as 1024.

$$\mu_{\text{eff}} = \begin{cases} \mu_{\text{init}}, & N < N_L \\ \mu_{\text{final}}, & N \geq N_L \end{cases} \quad (4)$$

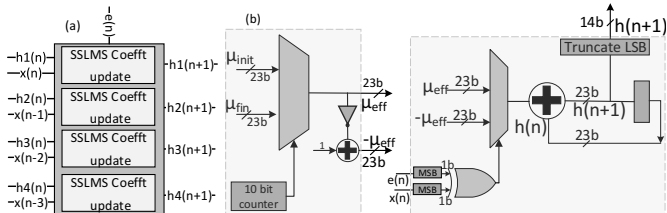


Fig. 8. (a) Weight adaptation block showing the 4 SSLMS taps (b) Coefficient update architecture for each SSLMS block

The SSLMS weight adaptation block is shown in Fig 8(a) and the architecture of each weight update finger and variable step selection is shown in Fig 8(b). Note that there are no actual multipliers required for weight update and a total of only 5 adders are required (including the one for computing  $\mu_{\text{eff}}$ )

in SSLMS adaptation. After initialization,  $\mu_{\text{init}}$  is used as the effective step size for  $N_L$  cycles for fast adaptation, after which it is changed to  $\mu_{\text{fin}}$  which is a smaller value. The internal computation of the adaptation unit is done using 23-bit arithmetic and is truncated to 14 bits while send to the output.

### B. Savitzky Golay Filter

The instantaneous prediction error,  $e(n)$ , from the adaptive SSLMS predictor used for locating the QRS complex has high frequency impulse noise (Fig 5). This noise is filtered out without smoothening or distorting the shape and the height of the error peaks corresponding to QRS complex using a Savitzky Golay (SG) filter. SG filter smoothenes the incoming signal by approximating the signal within a specified window of size  $L$ , to a polynomial of order  $K$ , which best matches the given signal in a least-squares sense. The filter is implemented using a discrete convolution (5), as shown in Fig.9,

$$e_{\text{sg}}(n) = \sum_{m=-M}^M h[m]e(n-m) \quad (5)$$

where  $e(n)$  is the prediction error and  $e_{\text{sg}}(n)$  is the filtered output. For ECG sampled at 256 Hz, an SG filter with  $K, L=3, 11$  yielded the optimum results. The (3,11) SG filter coefficients were computed as described in [10].

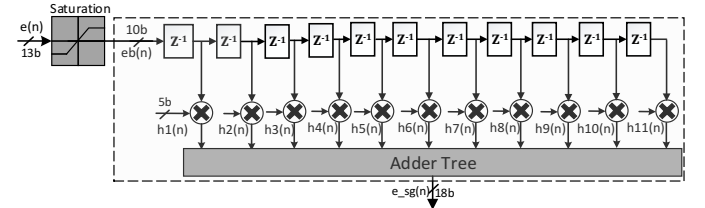


Fig. 9. Savitzky Golay Filter for removing high frequency impulse noise.

### C. Squaring & Moving integration

After SG filtering, the signal is smoothened by squaring and moving integration operation before thresholding (6).

$$e_{\text{no}}(n) = \sum_{m=-M/2}^{M/2} |e_{\text{sg}}(n)|^2 \quad (6)$$

The squaring provides a nonlinear amplification to the prediction error, which helps to further magnify the QRS component in the signal relative to the other segments.

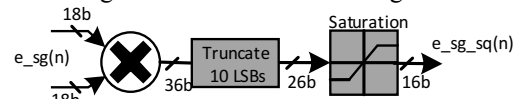


Fig. 10. Bit Limited Squaring operation with Truncation and Saturation.

After the squaring operation, the data is further truncated and saturated to 16 bits, as shown in Fig 10, to reduce the overall hardware complexity, and compensate for the scaling introduced by SG filter. The moving integrator implemented using a simple serial structure with a single adder, subtractor and shift register as shown in Fig.11.

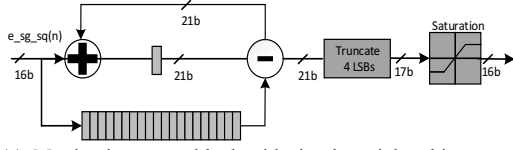


Fig 11. Moving integrator block with simple serial architecture and truncated /clipped outputs for bit limiting.

#### D. Thresholding and Peak Detection.

The enhanced signal in (6) is continuously scanned for QRS peaks. An adaptive threshold is used as a decision function for detection. The adaptive threshold is initialized with a default value and is updated based on the signal amplitude when a new detection is made. When the signal, exceeds the adaptive threshold, the peak detection algorithm starts operation. The detection starts with finding a continually rising edge and then a continually falling edge within a specific period of time, as identified by increasing or decreasing signal amplitudes for several consecutive points (7)(8).

$$\Lambda_{j=0}^2 \text{ eno}(i-j) - \text{eno}(i-j-1) > 0 \quad (7)$$

$$\Lambda_{j=0}^2 \text{ eno}(i+j+1) - \text{eno}(i+j) < 0 \quad (8)$$

The adaptive thresholding and peak detection from the smoothened signal is implemented as a two interacting FSM controllers as in Fig.12. The thresholding block initializes with a default threshold and updates its thresholds, when new peaks are detected. The peak detection block continuously monitors the filtered signal and detects the presence of QRS peaks while the signal is above the adaptive threshold.

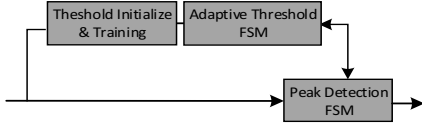


Fig 12. Adaptive Thresholding and Peak Detection blocks interacting with each other simultaneously for QRS peak identification.

#### E. Lossless Data Compressor

For compressing the prediction error, we previously proposed a simple joint coding-packaging scheme which produces a fixed length 16-bit output with low implementation complexity [15]. The dynamic range of the prediction error is low and centers around zero. Therefore only the LSB's which contain any signal value is extracted and packaged into a 16-bit fixed length format [15]. The dynamic data packaging uses a simple priority encoding technique to frame fixed length data from samples of multiple bit widths. As and when

the error data is received, the algorithm packs the maximum number of error samples into a single 16b frame in the order of packaging density. The overall implementation complexity is lower than other comparable methods and compressed data will always have fixed data-width. This avoids the need for further data repackaging that is essential for interfacing with other devices or I/O devices.

### VII. PERFORMANCE EVALUATION

#### A. QRS Detection

The proposed algorithm is evaluated using the MIT/BIH Arrhythmia Database which is a benchmark database with 48 thirty-minute ECG ambulatory recordings.

The MIT/BIH recordings are originally sampled at 360Hz. However, since the hardware is running at 256Hz sampling rate, we have resampled the MIT/BIH data to 256Hz for tuning the algorithm and testing the performance.

QRS detection performance is evaluated using false positive (FP) and false negative (FN) detections. Using FP and FN, the sensitivity (Se), positive predictivity (+P) are computed[10]. The proposed JQDC implementation achieved an average sensitivity and positive predictivity of 99.58% and 99.57% for the fixed point hardware implementation. Table I shows the summary of average QRS detection performance for 48 records from the MIT database.

TABLE I: AVERAGE PERFORMANCE FOR 48 RECORDS IN THE MIT/BIH DATABASE AT 256Hz

	FP	FN	Se (%)	+P (%)
Total/Average	461	465	99.58	99.57

#### B. Compression Performance.

The data compression performance is also tested using 256Hz resampled MIT/BIH Database. Bit compression ratio (BCR) is computed as a ratio of number of uncompressed bits to compressed bits. An average BCR of 2.15 times and a maximum BCR of up to 2.49 times are achieved using 48 thirty-minute ECG records from the MIT-BIH database.

### VIII. CHIP MEASUREMENT RESULTS AND COMPARISON

TABLE II CHIP SUMMARY

Supply Voltage	2.4~ 3.0 V
Technology	0.35 $\mu$ m CMOS
High-Pass Corner	<0. 07 Hz
Low-Pass Frequency	35 ~ 175 Hz
Gain Settings	49 ~ 67 dB
Input-Referred Noise (0. 5 ~ 250 Hz)	1.95 $\mu$ Vrms
Common-Mode Rejection Ratio (CMRR)	82 dB
Power Supply Rejection Ratio (PSRR)	70 dB
Total Harmonic Distortion @Full Scale (THD)	<0.71%
Sampling Frequency	256/512 Hz
Total Front-End Current	5.66 $\mu$ A
Total Back-End Current	0.4 $\mu$ A

TABLE-III: PERFORMANCE COMPARISON.

	TBCAS [4], 2012	TBCAS [16], 2013	TCAS II[9], 2015	TCE [7], 2011	This design
Functions	QRS Detection	QRS Detection	QRS Detection, Lossy Compression	Data Compression	QRS Detection, 2 Channel Data Compression
Method	Quadratic Spline WT	Wavelet Transform	Wavelet Transform	Delta Coding, Golomb Coding	SSLMS, Joint Coding Packaging
Sampling Frequency	300Hz	1KHz	360Hz	256Hz	256Hz
CMOS Process	0.35 $\mu$ m	0.35 $\mu$ m	65 nm	65nm	0.35 $\mu$ m
Supply Voltage(V)	1.8	3V	0.7V	1.0V	2.4V
Se(%)	99.31	99.90	99.7	-	99.58
+P(%)	99.70	99.91	99.49	-	99.57
Compression Ratio	-	-	13.6(Lossy)	2.38	2.15
Power	0.83 $\mu$ W	13.6 $\mu$ W	49/33 $\mu$ W	170 $\mu$ W	0.96 $\mu$ W
Area(mm <sup>2</sup> )	1.11	1.2	0.41	0.058	1.56

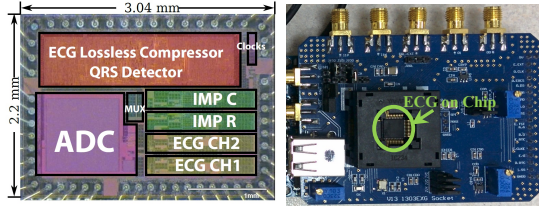


Fig. 13 Chip micro photo and prototype device.

The design is implemented in a 0.35 $\mu$ m process and the front-end measurement results are shown in Table II. The input referred noise from 0.05 Hz to 250 Hz is 1.95  $\mu$ Vrms. The high-pass corner is at 0.07 Hz, and the full-scale 3 V THD is 0.71 %. The total front-end current, including two channels, ADC, DRL, bandgap, and crystal oscillator circuit, is only 5.66  $\mu$ A. The JQDC processor consumes 0.4  $\mu$ A and has a core area of  $0.78 \times 2.0 \text{ mm}^2$ . Fig. 13 shows the die photo and the prototype evaluation board developed for testing the chip. The evaluation board was programmed using an Arduino board to update the SPI registers and read the ECG data. The data from ADC output and the JQDC block output is recorded for several use cases. The ADC output from the chip is passed to a bit accurate JQDC Matlab model and the outputs from the chip and model were compared for verification purposes. The total chip area is  $3.04 \times 2.2 \text{ mm}^2$ .

Performance comparison of the proposed design with others is given in Table III. QRS detection performance is measured in terms of sensitivity (Se), positive predictivity (+P) and compression performance in terms of bit CR. Since data is sampled at 256Hz instead of the original MIT/BIH data sampled at 360Hz, a slight degradation in performance is observed. QRS detection outputs from the test chip when significant ST-Elevation and powerline noise is present, are shown in Fig 14(a),(b). It can be seen that the detector output is accurate even in these noisy conditions. It is noted that detection performance and compression ratio varies according to the sampling frequency and only two reported designs make it explicit that the performance of the chip is related to sampling frequency. While all of the prior arts use 360 Hz MIT/BIH data for simulation, the hardware implementation is at a different sampling frequency. [16] has the best detection performance, but consumes much higher power. [4] consumes only 0.83 $\mu$ W, but is uni-functional. [7] has better compression ratio, but a much higher gate count and power at a smaller node and supply voltage. [9] is the only reported chip which implements both QRS detection and data compression, but the chip can do only one of the function at a time. Also the power consumed is much higher at a much smaller process node and lower power supply. Overall the proposed design has one of the lowest power for QRS detection and achieves a lossless data CR of 2.15.

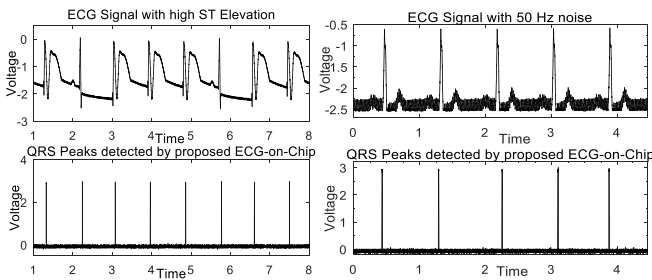


Fig. 14. QRS detection o/p from the ECG-SoC when (a) ST Elevation present (b) 50 Hz noise present

## IX. CONCLUSION

This paper presents a low power ECG-on-Chip with a novel joint QRS detection and lossless data compression circuit for wearable devices. The proposed JQDC processor shares hardware resources between QRS detection and lossless data compression, which leads to the lower power consumption compared to dedicated independent hardware. The QRS detection performance of the proposed chip is at the same level compared to the published QRS detectors, i.e. a detection sensitivity of 99.57% and a positive predictivity of 99.58% and lossless CR of 2.15x @ 256 Hz. The proposed ECG-on-Chip can reduce the sensor power by 2-5 times and therefore is well suited for wearable wireless ECG sensors.

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