# A 900 MHz, 0.9 V Low-Power CMOS Downconversion Mixer

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## Abstract

A low-voltage, low-power mixer operating at a supply voltage of 0.9 V while consuming 4.7 mW is presented. The circuit achieves the multiplication using current mode processing. Moreover, non-conventional differential pairs that don't require current tail generators are utilized. The circuit has been fabricated in a standard double-poly, triple-metal 0.35 $\mu$m CMOS process having a threshold voltage of 0.6 V. Measurement results for 900 MHz and 800 MHz input signals indicate that the circuit has an IIP3 of 3.5 dBm, a 1-dB compression point of -8 dBm and a noise figure of 13.5 dB.

## I. INTRODUCTION

Growth in the demand of wireless communication systems has driven recent efforts to increase integration levels in RF transceivers. The integrability and power consumption of the digital part of the transceiver will further improve with the downscaling of technologies. The bottleneck for further advancement is the analog front-end. One low-cost approach is to implement all the RF functions on a single chip using CMOS technology (1-2). This has given rise to research on designs that include lower cost, longer battery life, smaller size and lower weight systems. In order to achieve these goals low-voltage, low-power analog front-end blocks are required.

The downconversion mixer is one of the indispensable analog blocks in communications receivers, where its main function is to translate the incoming RF signal to an intermediate frequency signal for further processing. A lot of effort has been spent in developing low-voltage CMOS RF mixers in the 0.9 - 2 GHz range (3-5).

A low-voltage, low-power circuit capable of performing the analog multiplication of two differential input signals with low-signal distortion is presented. The circuit exploits the quadratic relation between the current and voltage of the MOS transistor in saturation. The proposed structure operates from a 0.9 V supply while dissipating 4.7 mW. This mixer can sustain high linearity even at this low supply voltage making it suitable for battery operated applications. The circuit has been designed for a 900 MHz application in a standard double-poly, triple-metal 0.35 $\mu$m CMOS process having a threshold voltage of 0.6 V. The architecture used to implement the circuit is described in section II. The measurement results are in good agreement with the theoretical results as shown in section III, while the final conclusion and the references are given in section IV and section V, respectively.

## II. CIRCUIT DESCRIPTION

In most mixer designs a tail current source is stacked below the local oscillator (LO) input pair, as shown in Fig. 1, to provide a stable biasing point and to provide the RF modulation current. This current source is normally made up of a common-source stage which has the RF input signal connected to its gate input to produce the modulating RF current. This stacking of transistors imposes a limit on the lowest supply voltage required by the circuit to function correctly.

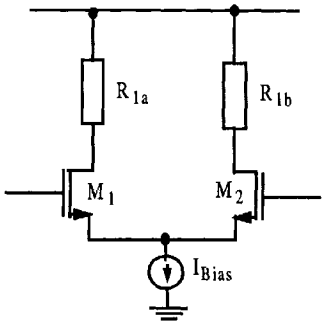


Figure 1: - Mixer with current source

For the circuit shown in Fig. 1 the minimum supply voltage is determined by the saturation voltage of $I_{bias}$, $V_{DS1}$ and some margin. For low-voltage operation the saturation limit of $I_{Bias}$ is not negligible.

To eliminate this contribution we propose a structure, illustrated in Fig. 2, where the control of the total current $I_{M1} + I_{M2}$ comes from resistors $R_{2a}$, $R_{2b}$ and resistors $R_{3a}$, $R_{3b}$. The function of these resistors is to keep the gate-to-



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source voltages of transistors $M_1$ and $M_2$ constant at their common mode drain-to-source voltages. Thus, by removing the stacking current source, operation at a minimum supply voltage of 0.9 V is required with devices having a threshold voltage of 0.6 V.

In order to achieve the required frequency translation an RF modulating current must be introduced in the circuit. This RF current signal is injected, as depicted in Fig. 3, between resistors $R_{2a}$ and $R_{2b}$ using a common-source stage. Two of these structures are required to provide a fully differential operation.

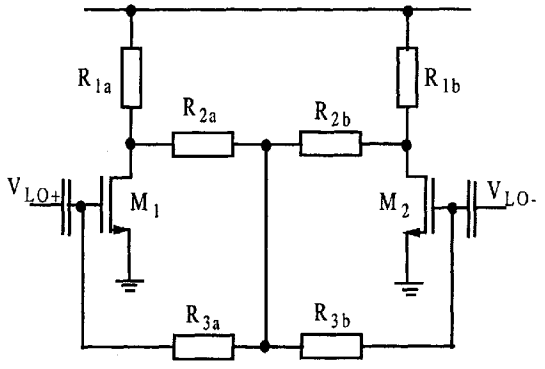


Figure 2: - Proposed biasing structure

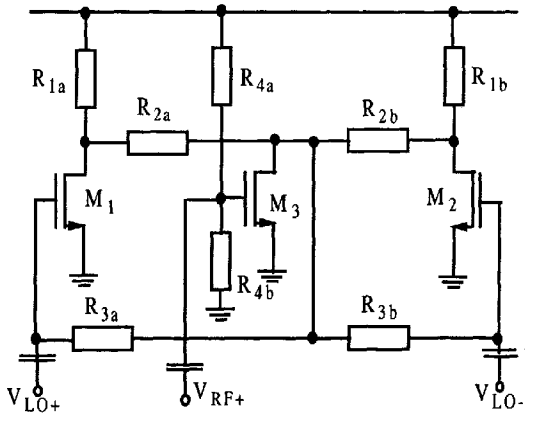


Figure 3: - Proposed mixer building block

The complete schematic diagram of the proposed circuit is shown in Fig. 4. The capacitors shown in the schematic are decoupling capacitors. $R_{4a}$-$R_{4d}$ are the biasing resistors of the RF input pair $M_3$ and $M_6$, and resistors $R_{2a}$-$R_{2d}$ and $R_{3a}$-$R_{3d}$ provide the biasing to the LO input transistors $M_1$, $M_2$, $M_4$ and $M_5$. The output stage consists of common source stages $M_{0a}$-$M_{0d}$, and resistors $R_{0a}$ and $R_{0b}$.The currents produced by transistors $M_{0a}$, $M_{0b}$ and $M_{0c}$, $M_{0d}$ are added in resistors $R_{0a}$ and $R_{0b}$, respectively, to give a differential output voltage proportional to the multiplication of the two input signals.

The circuit exploits the square law characteristics of the MOS transistor in saturation to produce the required output. The current equation for the MOS transistor in saturation is approximately given by:

$$I_D = \frac{KW}{2L}(V_{GS} - V_{th})^2 \tag{1}$$

where K is the transconductance parameter given by $\mu C_{ox}$, W and L are the width and length of the transistor respectively, $V_{GS}$ is the gate-to-source voltage, and $V_{th}$ is the threshold voltage.

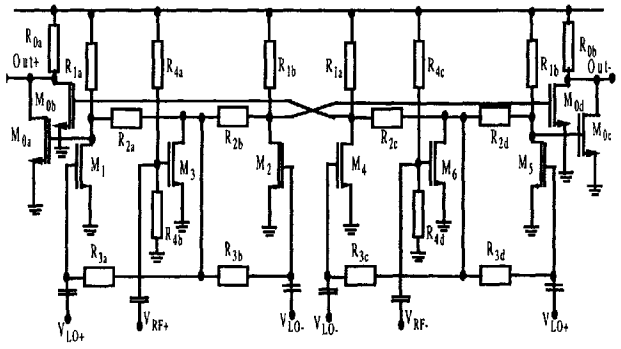


Figure 4: - Schematic diagram of complete mixer

The function of the mixer shown in Fig. 4 can be explained mathematically using the following equations. The current passing through resistor $R_{1a}$, $I_1$, is given by the current passing in $M_1$ plus half the current in $M_3$. Using (1) this gives:

$$I_1 = \frac{K_1 W_1}{2L_1}(v_{LO+} - V_{th})^2 + \frac{K_3 W_3}{4L_3}(v_{RF+} - V_{th})^2 \tag{2}$$

Similarly, the current equations for the current passing through $R_{1b}$, $R_{1c}$ and $R_{1d}$ is given by:

$$I_2 = \frac{K_1 W_1}{2L_1}(v_{LO-} - V_{th})^2 + \frac{K_3 W_3}{4L_3}(v_{RF+} - V_{th})^2 \tag{3}$$

$$I_3 = \frac{K_1 W_1}{2L_1}(v_{LO-} - V_{th})^2 + \frac{K_3 W_3}{4L_3}(v_{RF-} - V_{th})^2 \tag{4}$$

$$I_4 = \frac{K_1 W_1}{2L_1}(v_{LO+} - V_{th})^2 + \frac{K_3 W_3}{4L_3}(v_{RF-} - V_{th})^2 \tag{5}$$

where $W_1 = W_2 = W_4 = W_5$, $L_1 = L_2 = L_4 = L_5$, $W_3 = W_6$ and $L_3 = L_6$.

Now considering the common-source output stage, the current passing through transistor $M_{0a}$ is given by:

$$I_{M0a} = \frac{K_{M0a} W_{M0a}}{2L_{M0a}}(V_{DD} - I_1 R_{1a} - V_{th})^2 \tag{6}$$

Similarly, designing the widths $W_{0a} = W_{0b} = W_{0c} = W_{0d}$ and the lengths $L_{0a} = L_{0b} = L_{0c} = L_{0d}$, the currents in transistors $M_{0b}$, $M_{0c}$ and $M_{0d}$ are given by:

$$I_{M0b} = \frac{K_{M0a}W_{M0a}}{2L_{M0a}}(V_{DD} - I_3R_{1c} - V_{th})^2 \quad (7)$$

$$I_{M0c} = \frac{K_{M0a}W_{M0a}}{2L_{M0a}}(V_{DD} - I_4R_{1d} - V_{th})^2 \quad (8)$$

$$I_{M0d} = \frac{K_{M0a}W_{M0a}}{2L_{M0a}}(V_{DD} - I_2R_{1b} - V_{th})^2 \quad (9)$$

These currents are added in the respective resistors $R_{0a}$ and $R_{0b}$, giving a differential output voltage equal to:

$$V_{out} = R_{0a}(I_{M0a} + I_{M0b}) - R_{0b}(I_{M0c} + I_{M0d}) \quad (10)$$

Assuming perfect matching, $R_{1a} = R_{1b} = R_{1c} = R_{1d}$, and $R_{0a} = R_{0b}$, this results in:

$$V_{out} = \alpha(v_{LO+} - v_{LO-})(v_{RF+} - v_{RF-}) \quad (11)$$

where $\alpha$ is a constant. Therefore, the output represents a constant multiplied by the differential input signals. Thus, the mixing function is proved mathematically.

The accuracy of the multiplication function depends on the cancellation of the higher order terms. This cancellation is related to the matching of the transistors. Special care was taken during the layout of the circuit to reduce mismatch through symmetrically placing the components. The accuracy of the transconductance parameter K is approximately 0.2 % and that of W/L is also approximately 0.2 % in this technology. This leads to a matching accuracy of approximately 0.3 %. Therefore, the accuracy of this circuit is expected to be better than 50 dB. Also the pseudo differential structure attenuates all the even order harmonics improving the spectral purity of the output spectrum of the signal.

The gain of the circuit depends on the parameters of the NMOS transistors, the value of the resistors and the threshold voltage. The value of the output resistors determine the matching of the mixer's output port, hence the value that can be used to implement them is limited by the optimum matching condition. Since the value of these resistors has to be small in order to satisfy this condition they also increase the power dissipation of the circuit. Also the gain depends on the technology being used since it depends on the transistors' parameters and the threshold voltage. Thus a technology that improves these parameters would lead to a better conversion gain and as a direct consequence improve the noise figure of the circuit.

## III. MEASUREMENT RESULTS

The circuit was fabricated in a standard double-poly, triple-metal 0.35 $\mu$m CMOS process and the chip micrograph is shown in Fig. 5. The chip was bonded directly on the test board using aluminium bondwires to avoid the parasitics introduced by the package. The only external components used during the testing of the prototype were transformers at each port of the mixer. These high frequency transformers were required at the input ports to transform the single-ended generator signals into differential signals required by the IC. Also another transformer was required at the output to change the differential output signal from the IC to a single-ended signal for the spectrum analyzer. The input and output 50 Ω matching was provided by an on-chip input matching network and the on-chip output common-source stages, respectively.

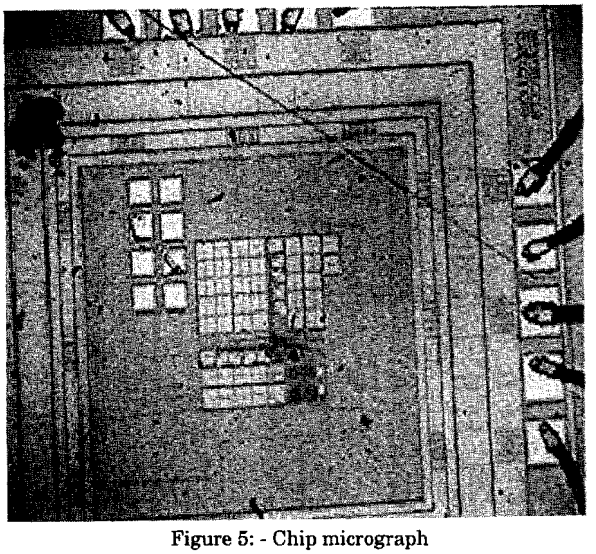

Figure 5: - Chip micrograph

The implemented width/length ratio of transistors $M_1$-$M_6$ is 60/0.35 while that of $M_{0a}$-$M_{0d}$ is 200/0.35. The values of the resistors implemented using the poly2 layer are 1 kΩ, 5 kΩ, 10 kΩ, and 100 Ω, for $R_{1a}$-$R_{1d}$, $R_{2a}$-$R_{2d}$, $R_{3a}$-$R_{3d}$ and $R_{0a}$-$R_{0d}$, respectively. The capacitors were implemented using the oxide layer between the poly1 and poly 2 layers.

The measurements were performed using a 0.9 V supply and an 800 MHz, -12 dBm local oscillator signal supplied by a Hewlett Packard HP 8648C. The RF signal was generated by using a Rhode & Schwarz SMIQ signal generator and the output IF signal was measured using a Rhode and Schwarz FSEB spectrum analyzer having the FSE-K4 option.

The circuit consumes 4.7 mW when operated under these conditions. The measured output spectrum for a -20 dBm, 900 MHz RF input is illustrated in Fig. 6. It shows that the third harmonic signal, at 300 MHz, is more than 50 dB below the fundamental output signal, at 100 MHz.

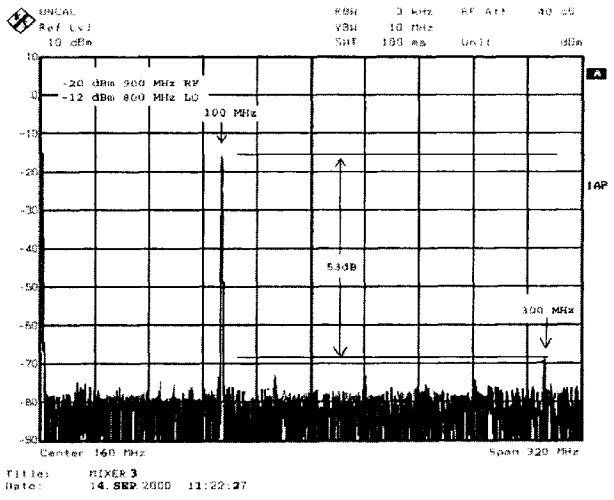


Figure 6: - Output spectrum

Fig. 7 shows that the measured input referred IP3 is approximately at 3.5 dBm, while Fig. 8 shows that the 1-dB compression point is at -8 dBm.

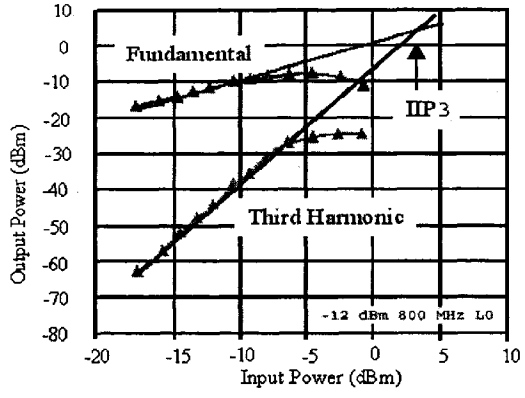


Figure 7: - Measured IIP3

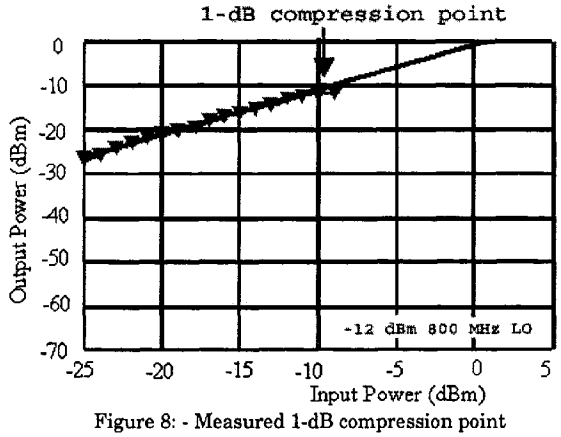


Figure 8: - Measured 1-dB compression point

The measured conversion gain and the noise figure of the mixer at 100 MHz, measured using the FSEB spectrum analyzer with the FSE-K4 option together with a noise source, are depicted in Fig. 9. This shows that the mixer has a conversion gain of 2 dB and a noise figure of 13.5 dB.

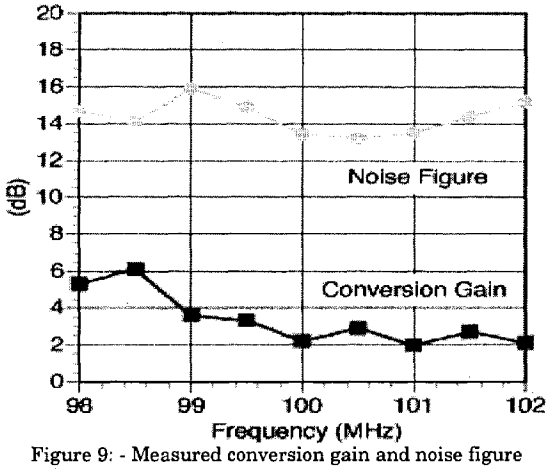


Figure 9: - Measured conversion gain and noise figure

## IV. Conclusion

A 0.9 V supply voltage, 900 MHz mixer has been presented. The threshold voltage of the technology used limits the supply voltage of this circuit and it can operate at lower voltages given a technology that permits lower threshold voltages. The circuit operates satisfactly at a supply voltage down to 0.8 V while dissipating 4.7 mW. Measurement results have shown that the third harmonic component lies more than 50 dB below the fundamental component, and that the circuit has an input referred IP3 of 3.5 dBm. The main advantage of this architecture is that it can operate at such a low-voltage while maintaining a good linearity. The proposed structure is symmetric and occupies a small chip area (active area 240 $\mu$m X 220 $\mu$m) making it a very feasible analog multiplier in the various portable communications systems.

## V. References


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