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A Low Voltage Wide-Input-Range Bulk-Input CMOS OTA

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Abstract. The G_m-C technique is extensively used for continuous-time filtering applications because it results in tunable, wideband and compact designs. In this paper, an OTA architecture using a novel bulk-input differential pair without the use of a tail current source is proposed. Good CMRR is still achieved by using the gate terminal to control the total current in the differential pair, via the use of a dummy pair. The OTA also exhibits a wide differential input range and good G_m-tunability. For this design, two standard double-poly double-metal CMOS processes were investigated: a 0.8 μm process having a nominal threshold voltage of around 0.7 V and a 0.35 μm process having a nominal threshold voltage of 0.5 V. Simulation results are presented for both designs while test results are presented, for the OTA, implemented using the 0.8 μm process, used in a second order cochlea low-pass filter.

Key Words: low voltage, bulk-input, OTA, CMOS design

1. Introduction

OTAs are a fundamental building block in analog signal processing applications and in particular in G_m-C filters. Low voltage operation is an important issue due to low power consumption requirements in battery operated applications and also for compatibility with today's low supply voltages used for digital applications [1]. A low voltage OTA is thus proposed here, with particular application to G_m-C filters, although other applications could include op amps and automatic gain control circuits. The concept of using the bulk terminal of an MOS device as input in a differential pair has already been explored [2–4]; however, these schemes still utilize a tail current source. A further reduction in the supply voltage requirement is achieved here via the elimination of the tail current source, thus reducing the supply voltage requirement by around 0.2 V, without compromising the common mode rejection ratio (CMRR).

2. Implementation

Figure 1(a) shows a conventional differential input stage, where the common mode input range is $(V_{\mathrm{DSsat4}} - |V_{\mathrm{TP}}|)$ to $(V_{\mathrm{DD}} - |V_{\mathrm{DSsat3}}| - |V_{\mathrm{GS1}}|)$, where V_{DSsat4} is the saturation voltage for I_{B2}. Taking a supply voltage of 0.9 V, $V_T = 0.7$ V and $V_{\mathrm{DSsat}} = 0.1$ V, the input range would be -0.6 to 0 V. This means that the OTA is not suitable for G_m-C filters, since it is not possible to provide the required voltage shift between one stage and another.

The circuit shown in Fig. 1(b) provides a solution to this problem since the input is applied to the bulk and therefore the common mode input range is only limited by the leakage current through the drain-bulk and source-bulk diodes, which effectively amounts to a common mode input range of 0.3 to 0.9 V. The minimum supply voltage for this input stage is $V_{\mathrm{DSsat5}} + V_{\mathrm{GS1}}$, where V_{DSsat5} is the saturation voltage of I_{B1}, thus allowing operation down to a supply voltage of 0.9 V. In Fig. 1(b), M_1-M_4 are matched. M_1-M_2 form a dummy pair which mirrors the operation of M_3-M_4. In this configuration, $I_1 + I_2$ is kept constant and equal to I_{B1}, by controlling the gate voltage: in this way, the current $I_3 + I_4$ is also kept equal to I_{B1}, which ensures an adequate CMRR. Considering a single-ended output, with a differential input signal, the voltage gain of the circuit shown in Fig. 1(b) is given by:

$$A_{vd} = \frac{g_{mb}}{2(g_{ds3} + g_{b2} + g_L)} \tag{1}$$

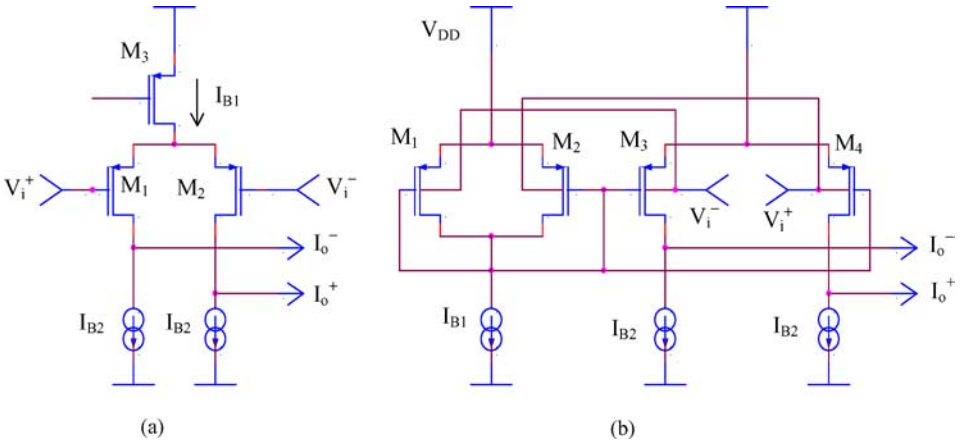


Fig. 1. (a) Conventional and (b) low voltage bulk-driven differential input stage.

where g_{b2}, g_L are the output conductance of the current source I_{B2} and load, respectively. For a common mode input signal, the corresponding single-ended output voltage gain is given by:

$$A_{vc} = \frac{g_{mb}(g_{ds1} + g_{b1}/2)}{g_m(g_L + g_{ds3})} \tag{2}$$

where g_{b1} is the output conductance of current source I_{B1}. The single-ended output CMRR of the differential input stage is therefore given by:

$$\text{CMRR} = \frac{A_{vd}}{A_{vc}} = \frac{g_m(g_L + g_{ds3})}{2(g_{ds3} + g_{b2} + g_L)(g_{ds1} + g_{b1}/2)} \tag{3}$$

Thus a high CMRR value, comparable to that of a conventional differential pair can be obtained provided g_{ds1} and g_{b1} are kept sufficiently small. In order to achieve a high CMRR, it is important that the dummy differential pair M_1, M_2 and the functional differential pair M_3, M_4 are accurately matched: common centroid layout techniques have to be used for this purpose.

Figure 2 shows the complete OTA with the necessary current mirrors in order to transform the differential outputs into a single-ended output. A cascode output stage is used in order to enhance the output resistance of the OTA. In this OTA, $(W/L)_{11} = (W/L)_{13}$, $(W/L)_{12} = (W/L)_{14}$, $(W/L)_9 = (W/L)_{10}$. Thus the effective transconductance of the OTA is given by:

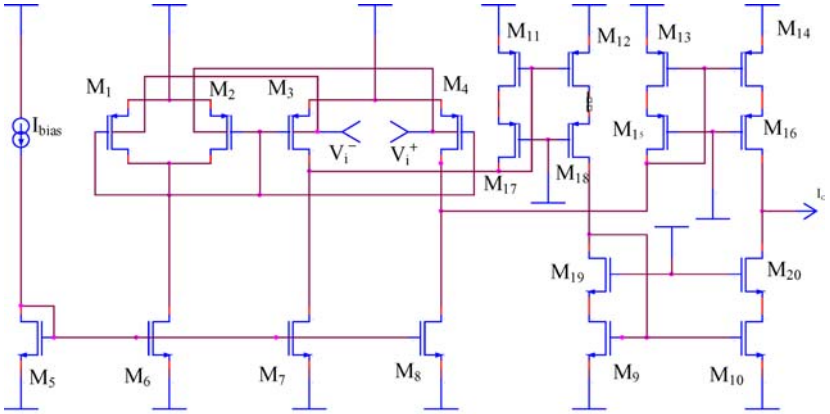
$$G_m = g_{mb3,4} \cdot \frac{(W/L)_{12}}{(W/L)_{11}} \tag{4}$$

3. Simulation Results

3.1. *OTA Simulation Results for the 0.8 μm CMOS Process Implementation*

Figure 3 shows the DC transfer characteristic of the OTA of Fig. 1(b) for differential bias currents I_{B1} ranging from 100 nA to 1 μA. The common mode input voltage was kept at 450 mV, resulting in an input linear range of around $\pm$ 600 mV which is significantly higher than the value of 60 mV that is typically achievable using a standard differential pair [5]. This is due to the fact that the bulk transconductance is lower than the gate transconductance. Figure 4 shows the corresponding G_m-value versus frequency plot. Since the differential pair operates in weak inversion, it can be seen that G_m is proportional to the bias current, although at high bias currents some compression is noticed due to the transistors starting to operate in moderate inversion.

Figure 5 shows the input referred noise plot with frequency for an I_B range from 0.1 to 1 μA. The corresponding thermal noise density range is 2.2 μV/$\sqrt{}$ Hz to 820 nV/$\sqrt{}$Hz. The higher noise value is expected at low bias currents. When compared to gate-driven MOS transistors, bulk-driven MOS transistors exhibit the same channel noise current; however, the input referred noise for bulk-driven MOS transistors is higher



Transistor sizes: $M_{1\text{-}4}$, $M_{11\text{-}18}$: W = 80 µm; L = 2 µm.
$M_{5\text{-}10}$, $M_{19\text{-}20}$: W = 50 µm; L = 2 µm.

Fig. 2. Complete bulk-input OTA.

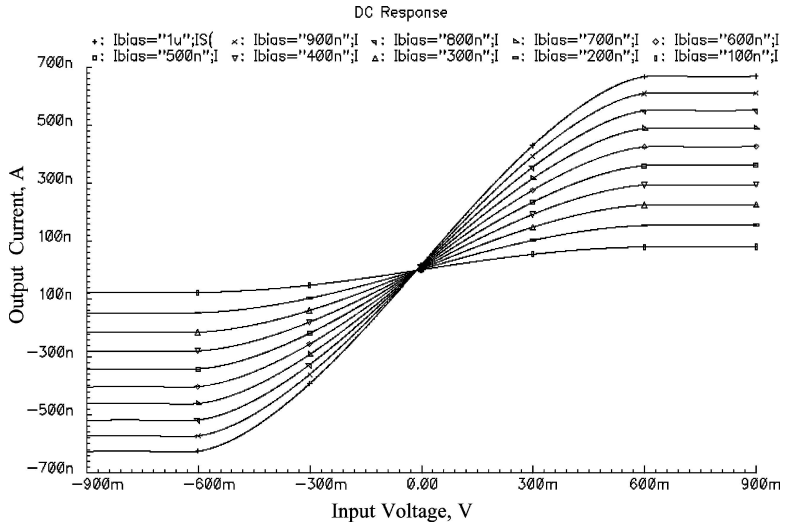


Fig. 3. DC Transfer characteristics of the OTA for $I_B = 0.1$ to 1 μA.

since the bulk transconductance is lower than the gate transconductance.

3.2. *Second Order LPF Simulation Results*

The second order cochlea LPF [5] shown in Fig. 6, using the proposed OTA was simulated. For this section, the transfer function is given by:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{\left(\frac{g_{m\tau}}{C}\right)^2}{s^2 + s\frac{\frac{g_{m\tau}}{C}}{2g_{m\tau} - g_{mq}} + \left(\frac{g_{m\tau}}{C}\right)^2} = \frac{\omega_n^2}{s^2 + \frac{\omega_n}{Q}s + \omega_n^2} \tag{5}$$

where $g_{m\tau}$ is the transconductance of OTA_1, OTA_2 and g_{mq} is the transconductance of OTA_3. In the standard second order LPF expression, $\omega_n = g_{m\tau}/C$ and $Q = g_{m\tau}/(2g_{m\tau} - g_{mq})$. Since the input transistors operate in weak inversion, their transconductance is proportional to the bias current.

Figure 7 shows the frequency response of the second order filter for the ω-tuning current (I_ω) in the range 5 nA to 1 μA. Using $C = 10$ pF, the peaking frequency ranges from 186 Hz to 23 kHz. The Q-tuning current I_Q was kept equal to 1.5 I_ω in all cases, resulting in a theoretical Q-factor of 2. In practice, the Q-factor obtained is 1.6: this value is lower than the theoretical value due

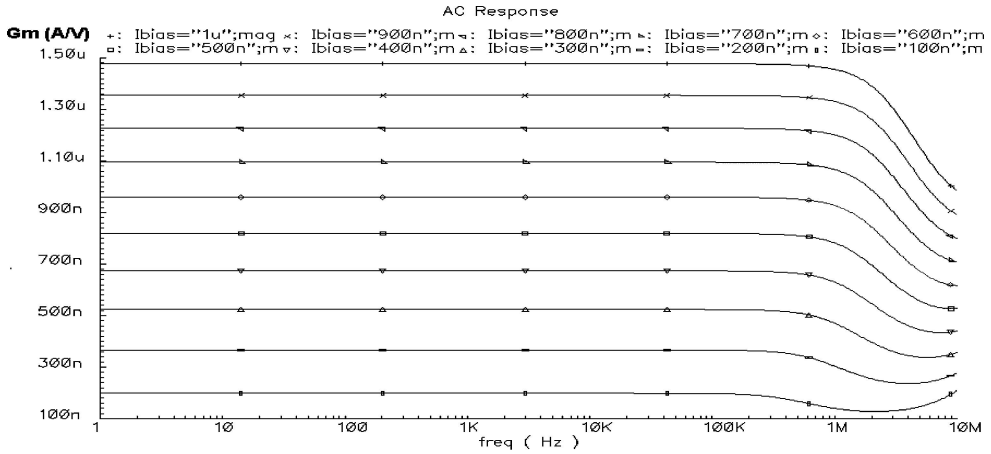


Fig. 4. AC response of the OTA for $I_B = 0.1$ to 1 μA, measured using a load resistor of 1 Ω.

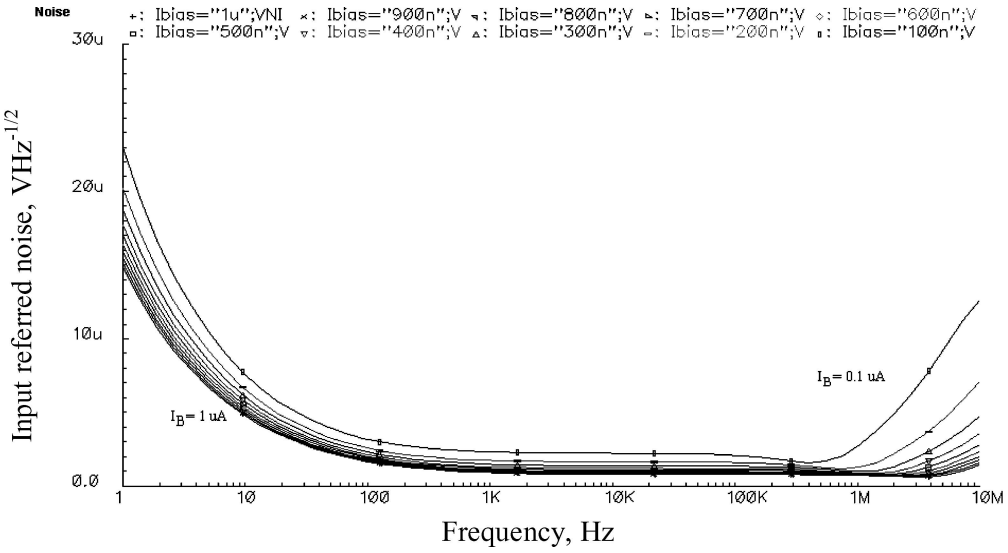


Fig. 5. Noise performance of the open circuit OTA for $I_B = 0.1$ to 1 μA.

to the finite input resistance of the driven bulk-input OTA and also due to the finite output resistance of the driver OTA itself.

3.3. OTA Simulation Results for the 0.35 μm CMOS Process Implementation

In order to investigate the possibility of further lowering the supply voltage, the same OTA architecture was also characterized using a 0.35 μm CMOS process having a threshold voltage of around 0.5 V: the transistor gate widths were kept the same as for the 0.8 μm process, but the gate lengths were decreased to 1 μm. The DC transfer characteristics of the OTA, implemented in the 0.35 μm process and operated at a supply voltage of 0.7 V, for the differential pair bias current I_{B1} ranging from 100 nA to 1 μA, are shown in Fig. 8. The common mode input voltage is kept at 350 mV, resulting in an input linear range of around $\pm$350 mV; this value is lower than that obtained for the 0.8 μm implementation, mainly because of the higher W/L ratio used in this case and the higher intrinsic transconductance (K) of the 0.35 μm process. Figure 9 shows the corresponding G_m-value versus frequency plot; this plot is very

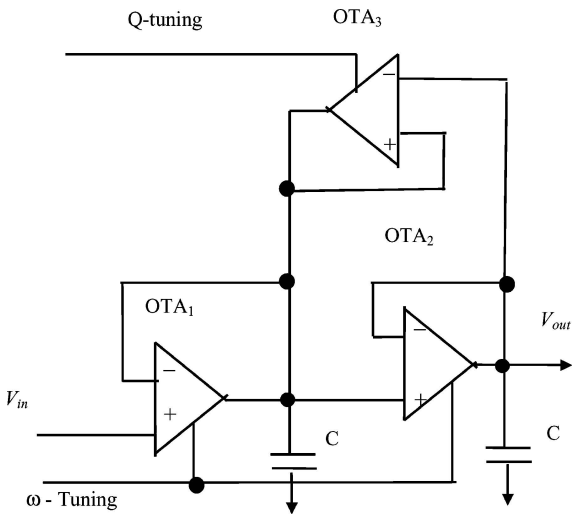


Fig. 6. Second order LPF with separate cut-off frequency and Q-factor tuning.

similar to that obtained for the 0.8 μm process; however, a higher G_m-value can be observed again because of the higher values of W/L and K parameter.

Table 1 summarizes the performance of the OTA implemented in the 0.35 μm process, at different supply voltages with a load capacitance of 0.5 pF, $I_{\text{bias}} = 1\ \mu$A and an input common mode voltage set at $V_{\text{DD}}/2$. A high CMRR is achieved at 0.7 V and 0.8 V even though a tail current source is not used. At $V_{\text{DD}} \geq 0.9$ V, bulk leakage in the input transistors becomes more appreciable and this results in some degradation of the OTA parameters mainly the CMRR, together with an increase in the input offset voltage. Figure 10 shows the variation of (a) the AC response and (b) the common mode gain, of the OTA, with different common mode input voltages with the OTA operated at $I_{\text{bias}} = 1\ \mu$A and $V_{\text{dd}} = 0.7$ V. Results show that for $V_{\text{DD}} = 0.7$ V the OTA exhibits very little parameter dependence on the input common mode voltage as regards to its AC performance; however, a 15 dB degradation in the CMRR can be noticed as the common mode voltage is increased from 0 to 700 mV.

3.4. Third Order Butterworth LPF Simulation Results

A third order Butterworth filter, based on the second order cochlea LPF, discussed in Section 3.2, followed by a first order section, and using the OTA implemented in 0.35 μm technology, has been simulated. Figure 11(a) shows the frequency response of the third order filter for

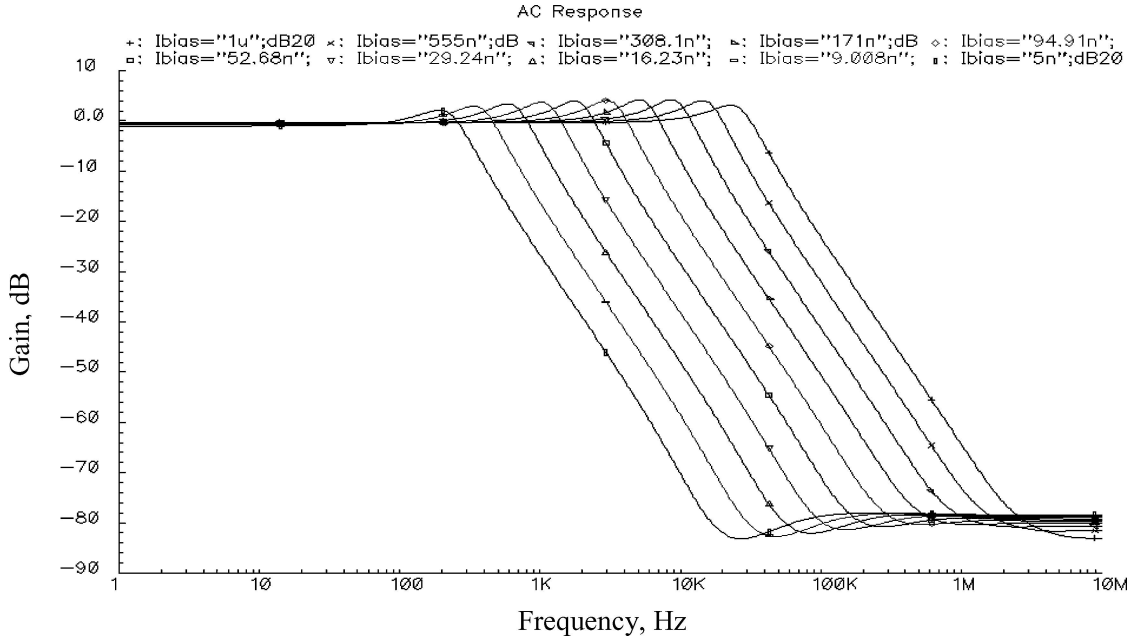


Fig. 7. Frequency response of the 2nd order LPF for $I_\omega = 5$ nA (left curve) to 1 μA (right curve) with $I_Q = 1.5\ I_\omega$.

Table 1. Simulation results for the 0.35 μm process OTA.

Supply voltage (V)	GBW (kHz)	DC gain (dB)	Phase margin (°)	Slew rate (V/μs)	Power (μW)	CMRR (dB)
0.7	446	63	67	1	3.5	123
0.8	450	70	65	1.1	4	131
0.9	398	69	66	0.84	4.5	91
1.0	371	63	68	0.83	5	66

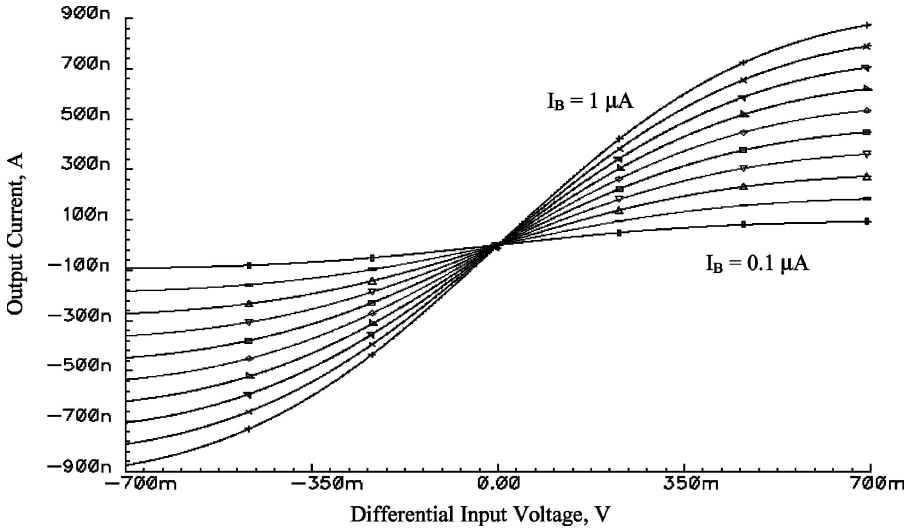


Fig. 8. DC Transfer characteristics of the OTA operated at V_{DD} = 0.7 V for $I_B = 0.1$ to 1 μA in steps of 100 μA.

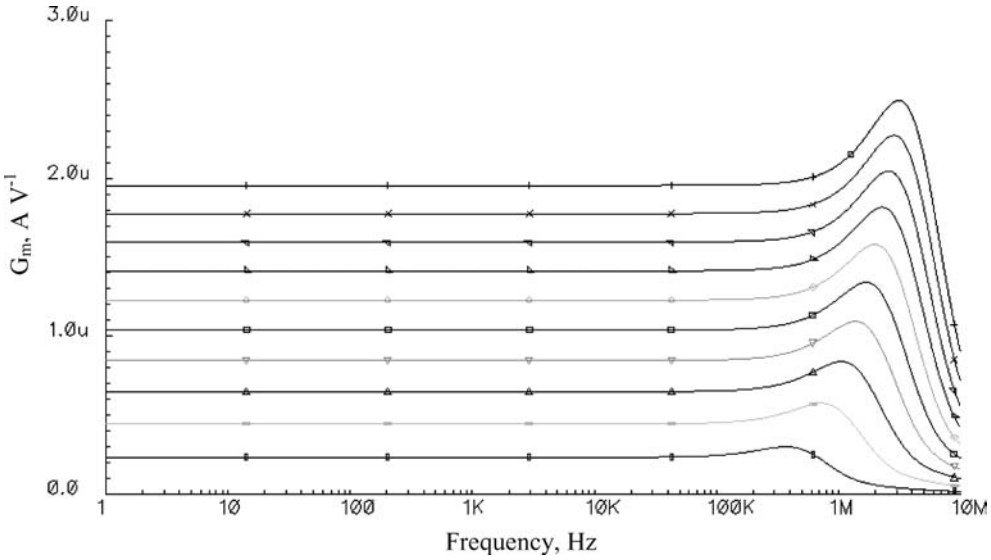
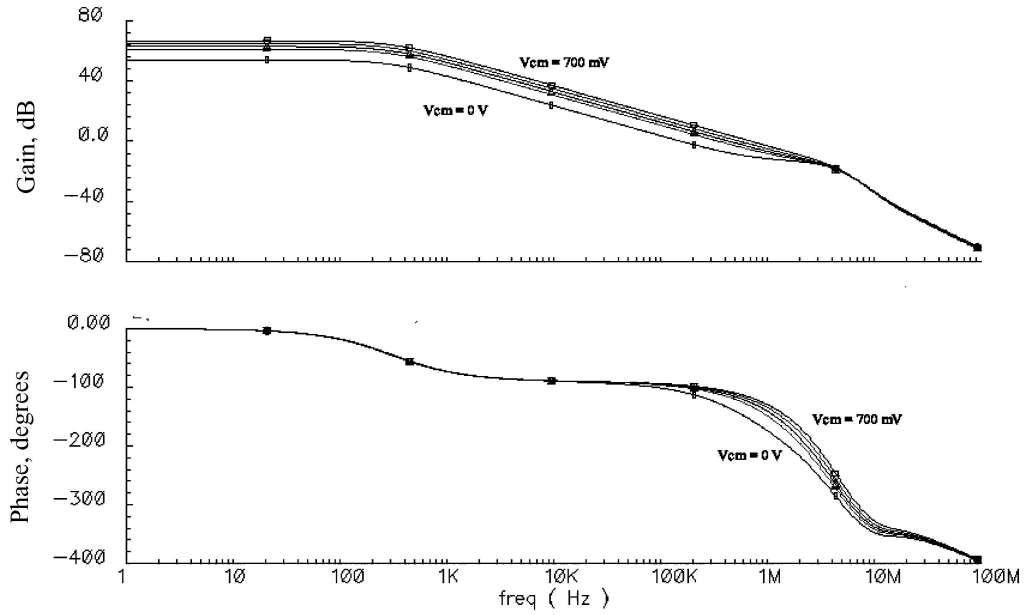
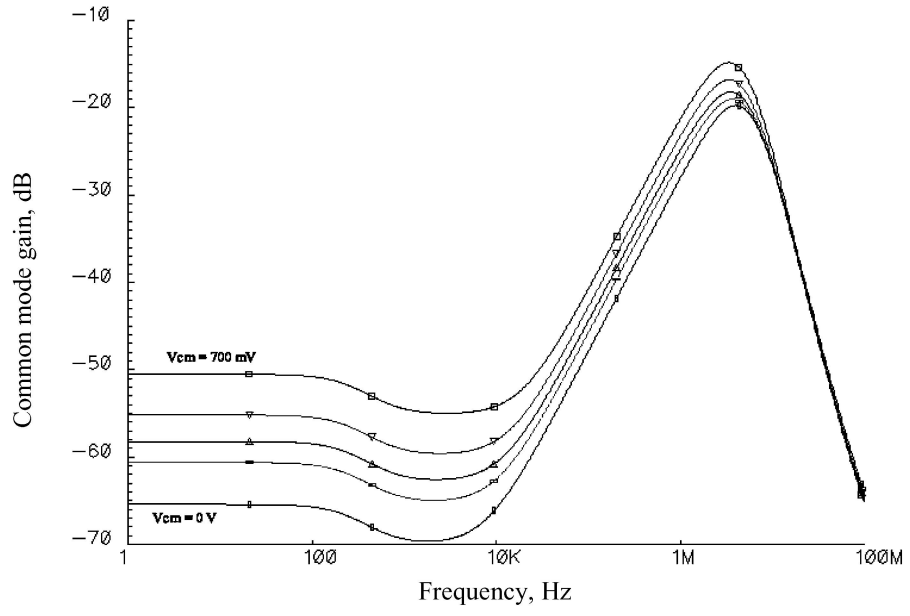


Fig. 9. AC response of the OTA at $V_{DD} = 0.7$ V for $I_B = 0.1$ μA (lower curve) to 1 μA (upper curve) in steps of 100 nA, measured using a load resistor of 1 Ω.



(a)



(b)

Fig. 10. Variation of the (a) differential gain and phase response and (b) common mode gain with common mode input voltage ranging from 0 to 700 mV.

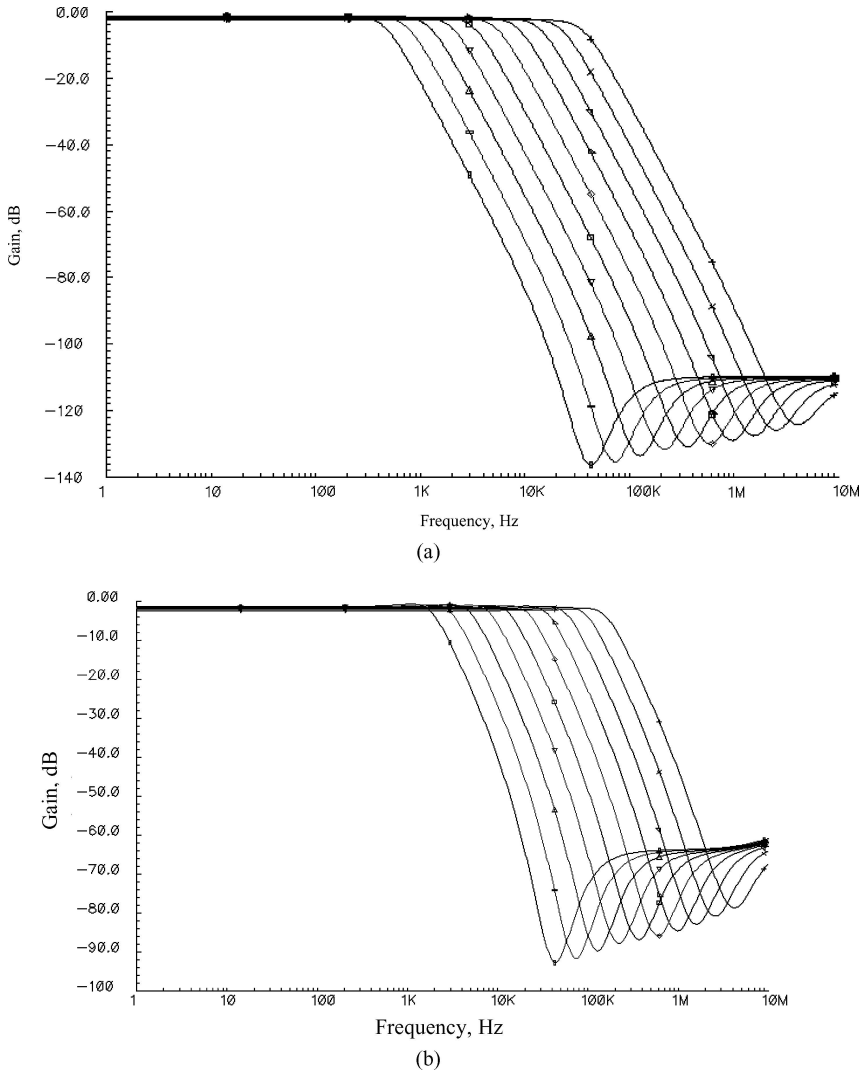


Fig. 11. Butterworth LPF implemented using a second order stage followed by a first order stage, for tuning currents swept logarithmically from 10 nA (left curve) to 1 μA (right curve) for (a) filter capacitors set to 10 pF and (b) parasitic capacitors only.

the ω-tuning current in the range 10 nA to 1 μA. With the filter capacitors set to 10 pF, the cut-off frequency ranges from 500 Hz to 38 kHz, with a stop band attenuation of -110 dB. It is evident that the cut-off frequency is linearly related to the tuning current—this is expected since the cut-off frequency is proportional to the G_m of the OTA, which in turn is proportional to the tuning current if the MOS transistors operate in weak inversion. The same simulation carried out without using any capacitors, but relying on the bulk input parasitic and the corresponding results, are shown in Fig. 11(b). In this case, the cut-off frequency ranges from 1.82 to 200 kHz for the same bias current range; however, the stop band attenuation is limited to -62 dB, since the filtering capacitors are of the same order of magnitude as the other parasitic capacitors in the circuit.

4. Measurement Results for the 0.8 μm Implementation

The OTA designed using the 0.8 μm process was fabricated and tested. The microphotograph of the test chip consisting of a single OTA is shown in Fig. 12. Three

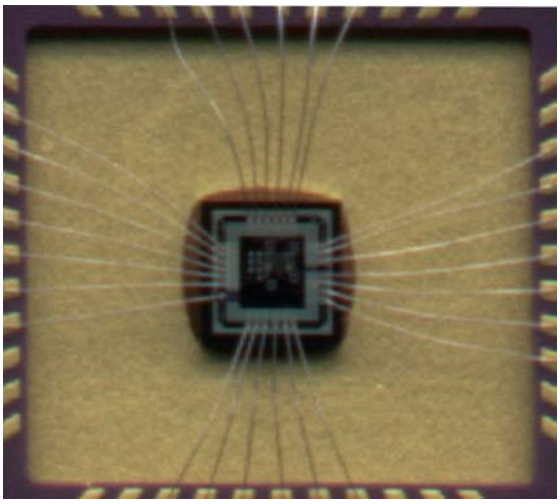


Fig. 12. Microphotograph of the OTA test chip.

test chips were then wired as a cochlea second order LPF, with two external 10 pF capacitors, and the corresponding measured frequency responses for $I_B = 5$ nA to 1 μA are shown in Fig. 13 for (a) feedback OTA disabled, (b) feedback OTA current enabled with $I_Q = 1.5\ I_\omega$. For the case when the feedback OTA is disabled, the Q-factor is equal to 0.5, resulting in a critically damped second order filter: in this case the measured results are very close to the theoretical response. For the second case, the measured Q-factor of 1.4 is lower than the theoretical value and is probably influenced by the leakage current to the bulk inputs of the OTAs.

5. Conclusion

Simulation and test results, for both the 0.8 and 0.35 μm CMOS processes, indicate that the differential pair

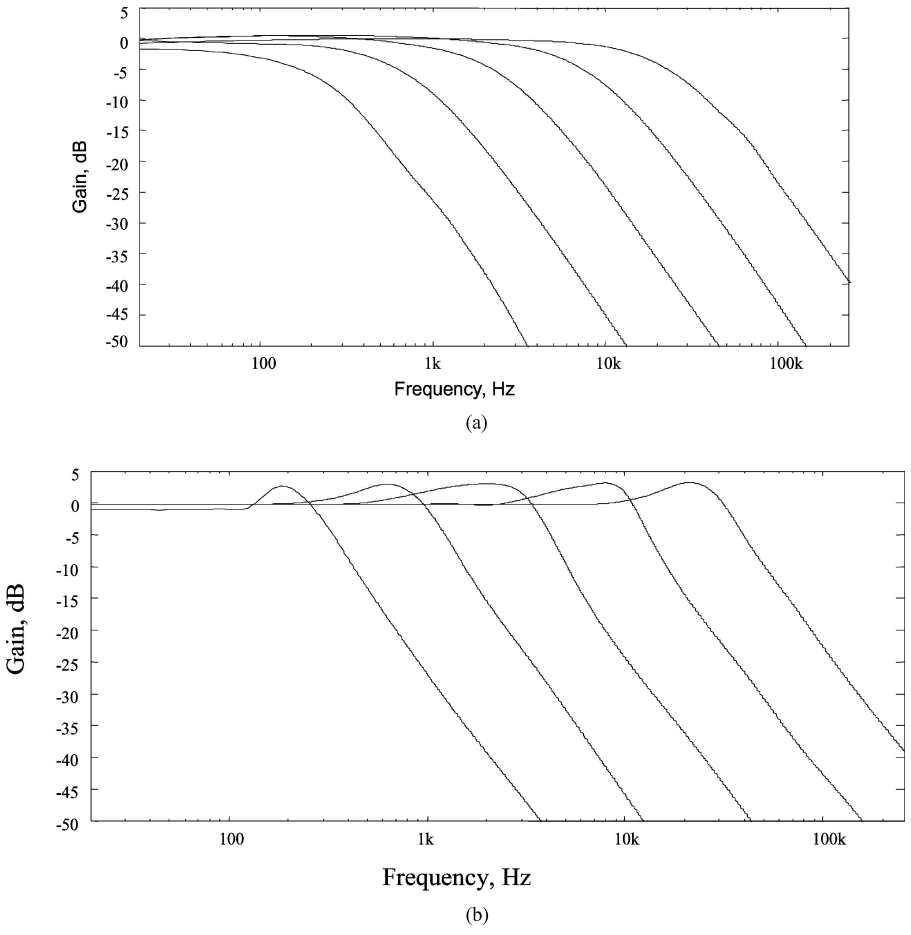


Fig. 13. Frequency response (starting from left curve) for $I_B = 5$, 18, 71, 260, 1000 nA, for (a) feedback OTA disabled and (b) feedback OTA enabled with $I_Q = 1.5\ I_\omega$.

using the bulk terminal as input and the gate terminal for CMRR control is a feasible solution in the area of very low voltage applications—operation supply voltages down to 0.7 V is achievable using a process having a threshold voltage of 0.5 V. When used as the input stage of an OTA, the differential pair exhibits a wide linear input range due to its intrinsically low transconductance value, and is thus applicable to a wide range of current mode analog signal processing techniques, where a slight input bias current can be tolerated as for example in most filtering applications. A second order G_m-C filter has been implemented using three bulk-input OTAs and test chip results presented.

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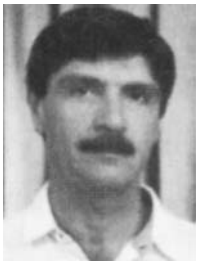

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