An overview of CMOS activities for the ATLAS upgrade

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Introduction

Why HV-CMOS, HV-MAPS, HV/HR-MAPS, DMAPS… in the ATLAS upgrade?

- Motivated for the need of low-cost large area detectors
- With less material (avoid bump bonding)

With the requirements of

- Being able to cope with the radiation level (> 10^{15} n_{eq}/cm^2)
- and the high rate (~MHz/mm^2)

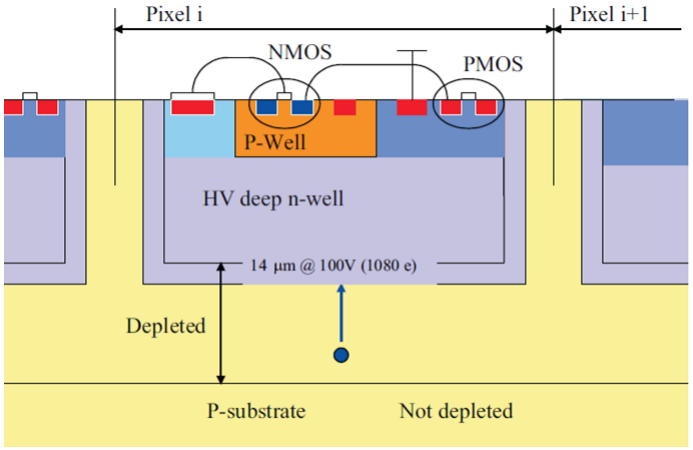
What can HV-CMOS detectors offer?

- Produced in commercially available technologies → reliable, mature, low-cost
- HV → fast charge collection by drift and high radiation tolerance
- HR → to widen the depletion region of the sensor and improve signal, now available in most foundries
- R/O electronics embedded inside the sensor area
- Possibility of monolithic sensors with standalone R/O

ams 0.35 µm/180 nm

Key features:

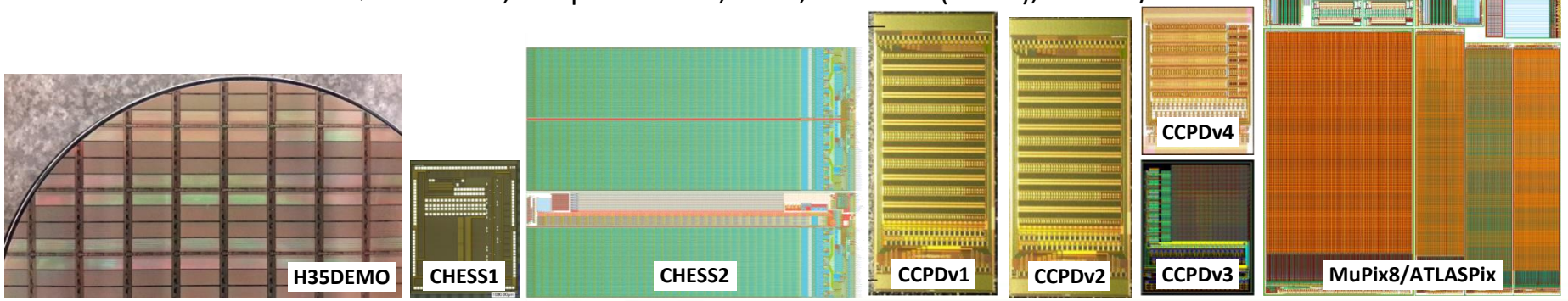
- **Technology node** 0.35 µm/180 nm
- **Wells** No possibility of isolating n-wells from the collecting deep n-well. No CMOS electronics in the sensor area. Can induce cross-talk.
- **Metal layers** 4/6
- **HR** 20 (standard value) – 1k Ω·cm (since 2015/6)
- **HV** -150 V < HV < 0 V
- **Depletion region** 140 µm thick
- **Backside biasing** Not possible
- **Stitching** Not possible



I. Peric, NIMA 650 pp. 158-162, 2011

Prototypes:

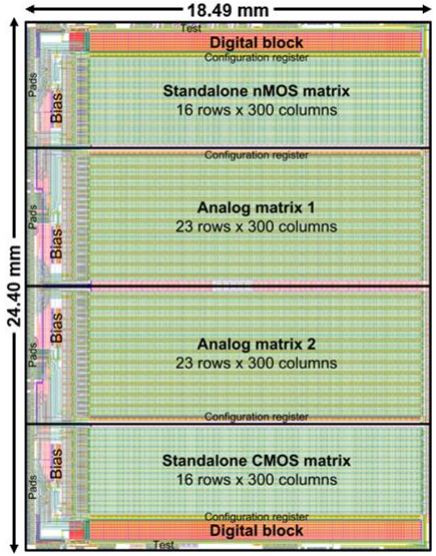
- ams 0.35 µm → Initial R&D developments, H35CCPDv1-2, H35DEMO, HVStrip, CHESS1-2 (strips)
- ams 180 nm → CCPDv1-8, CLICpix=CCPDv3, C3PD, MuPix1-8 (Mu3e), MuPix8/ATLASPix



ams 0.35 µm – H35DEMO

Summary:

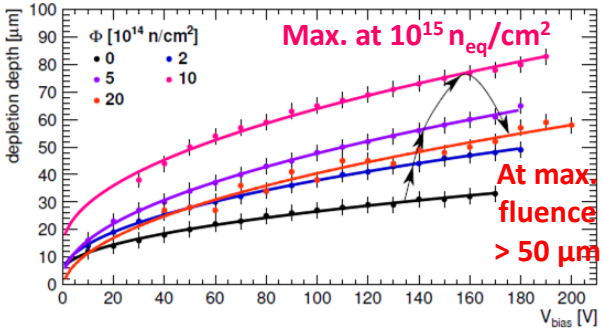
- Submitted in October 2015 (eng. run)
- It includes:
  - 2 matrices of pixels with R/O coupled to FEI4. Pixels without comparators.
  - 2 monolithic matrices of pixels with standalone R/O. Pixels with nMOS/CMOS comparators. Digital blocks (FE-I3 style) are in the periphery of the matrices.
  - Different pixel flavours
  - Test structures for TCT/e-TCT and sensor capacitance measurement
- Pixel size: 50 µm x 250 µm for 1-to-1 connection to FEI4
- Timing resolution: 25 ns
- Readout speed: 320 MHz
- Rad-hard design
- Resistivity: 20 Ω·cm, 80 Ω·cm, 200 Ω·cm, 1k Ω·cm
- Detection efficiency > 99% in test beams



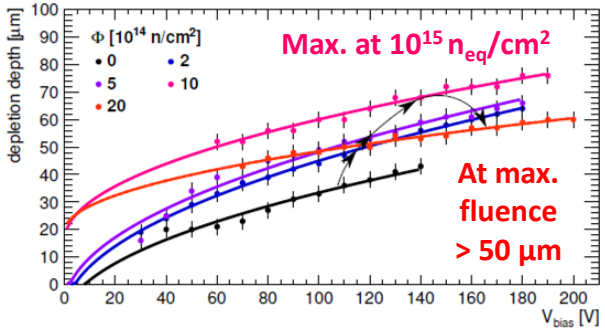
E. Vilella, JINST 11 C01012, 2016

Neutron irradiation at Ljubljana + e-TCT

80 Ω·cm

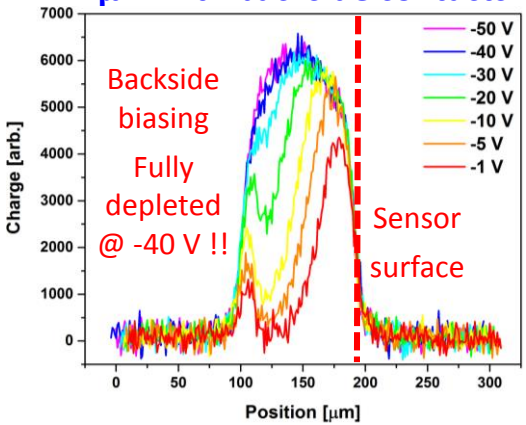


200 Ω·cm



E. Cavallaro, JINST 11 C01012 2016

1k Ω·cm chip thinned to 100 µm with backside contacts

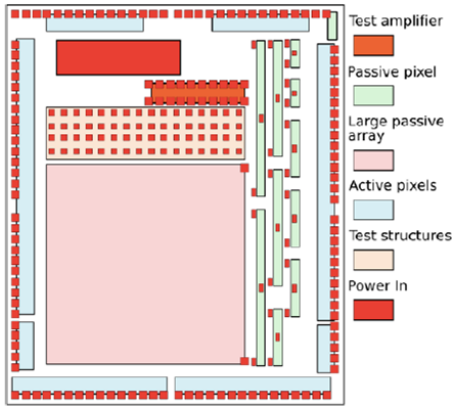


E. Vilella, PIXEL Workshop, 2016

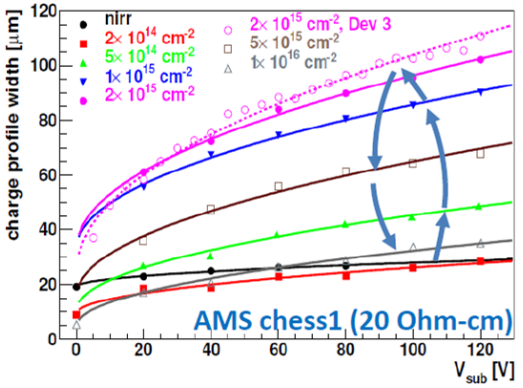
ams 0.35 µm – CHESS strip development

CHESS1 is a test chip:

- Submitted in August 2014
- It includes:
  - Test transistors
  - Passive pixels of different length (45 µm x 100-800 µm)
  - Standalone amplifiers
  - Active pixels with embedded amplifiers
  - Passive arrays for charge collection studies
- Resistivity: 20 Ω·cm (standard value)



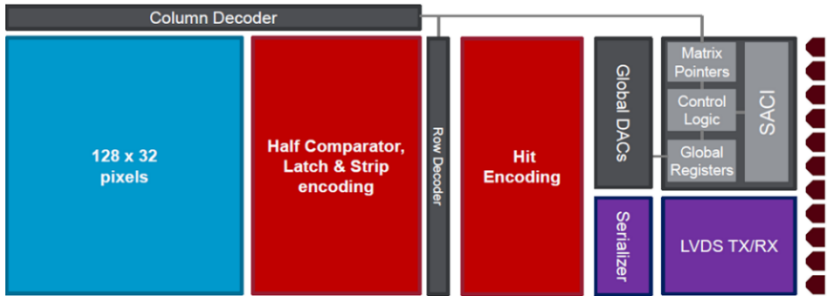
V. Fadeyev, NIMA 831 pp. 189-186, 2016



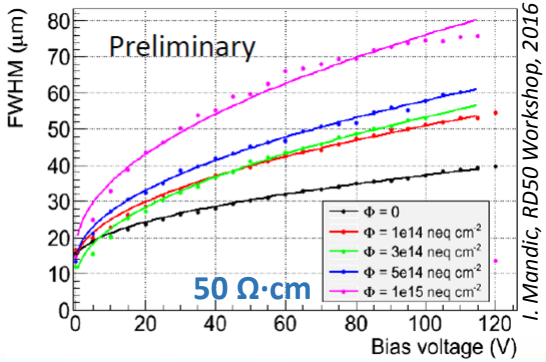
I. Mandic, RD50 Workshop, 2016

CHESS2 is full reticle demonstrator:

- Submitted in 2016
- Design by SLAC and UCSC, support from KIT
- It includes:
  - Array of 128 by 32 striplets with full digital encoding and readout
  - Array of 16 by 32 pixels with multiplexing
  - Test structure for LVDS/CMOS and CMOS/LVDS transmission + pixels arrays for e-TCT and capacitance measurements
- Cell size and timing resolution: 40 µm x 630 µm, 25 ns
- Readout speed: 320 MHz
- Rad-hard design
- Resistivity: 20 Ω·cm, 50-100 Ω·cm, 200-300 Ω·cm, 600-2k Ω·cm



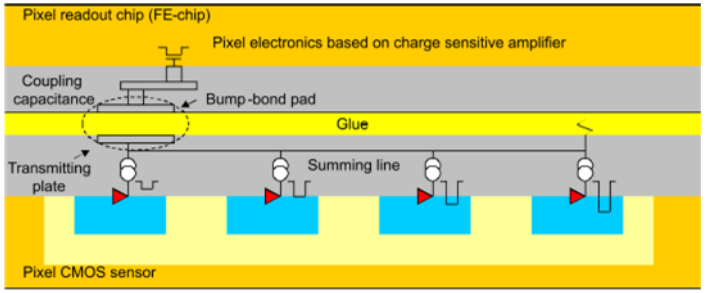
P. Caragiulo, Trento Workshop, 2016



I. Mandic, RD50 Workshop, 2016

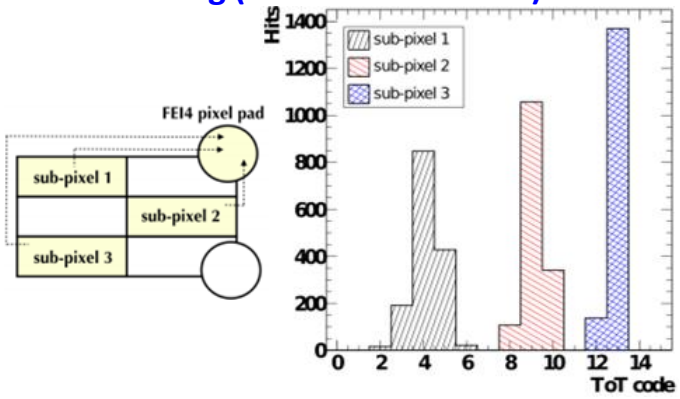
ams 180 nm – Prototypes

- **CCPDv1 (2011)** Basic design. Pixel size 33 µm x 125 µm, readout with FEI4 pixel readout ASIC.
- **CCPDv2 (2012)** Improved radiation tolerance (850 Mrad), linear transistors replaced with enclosed ones.
- **CCPDv3 (2013)** Large matrix with 25 µm x 25 µm implemented, readout with CLICpix pixel readout ASIC.
- **CCPDv4 (2014)** Pixel position encoded as pulse length.
- **CCPDv5 (2015)** Comparator with time walk compensation.
- **CCPDv6** Chip version in AMS aH18 process, a new version of H18 process that offers more flexibility such as the use of HR substrates.
- **CCPDv7** Chip version with a new guard ring geometry that allows higher bias voltage of up to -150 V.



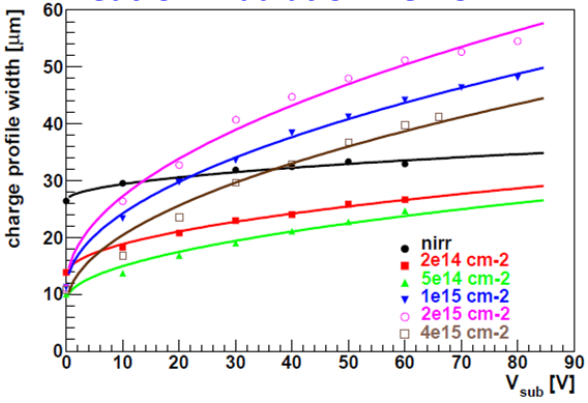
I. Peric, NIMA 731 pp. 131–136, 2013

Pixel encoding (connection to FEI4)



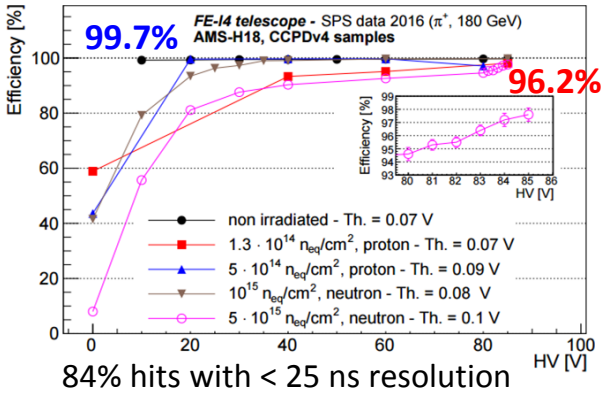
A. Miucci, JINST 9 C05064, 2014

Neutron irradiation + e-TCT



A. Affolder, JINST 11 P04007, 2016

Efficiency in test beam



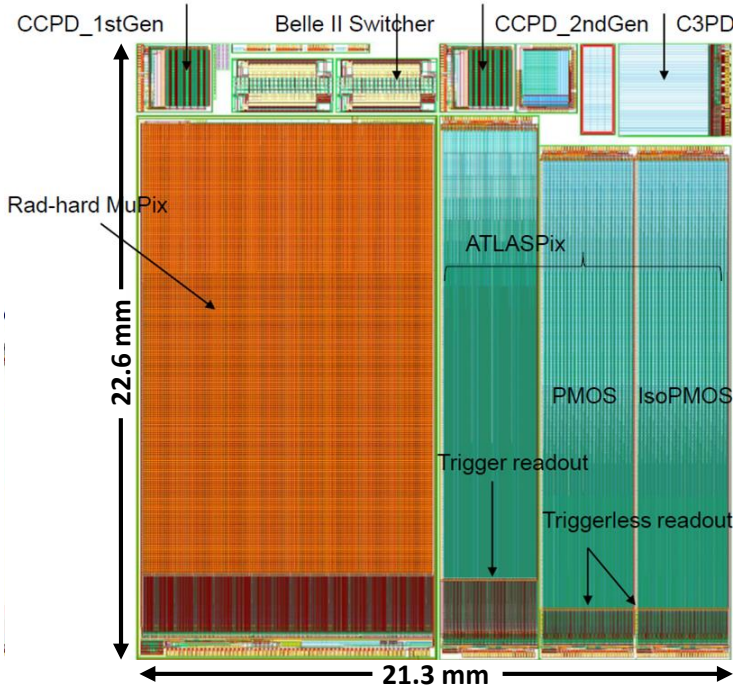
84% hits with < 25 ns resolution

M. Benoit, arXiv:1611.02669v1, 2016

ams 180 nm – MuPix8/ATLASPix and new design

MuPix8/ATLASPix:

- Submitted in January 2017 (eng. run)
- It includes:
  - Matrices of pixels for ATLAS
    - Pixel size: 25 µm x 25 µm, 25 µm x 50 µm, 33 µm x 125 µm, 50 µm x 60 µm, 40 µm x 125 µm
  - MuPix8
    - Pixel size: 80 µm x 81 µm
    - Matrix with 200 x 128 pixels
    - Pixels with CSA and output driver only
    - Hit info: x-address, y-address, 10-bit TS, 6-bit amplitude
    - Time resolution: 6.25 ns
    - Nominal power consumption: 300 mW per matrix
  - Hit driven, triggerless R/O (MuPix8, Simple ATLASPix)
  - Triggered R/O (M ATLASPix)
  - Resistivity: 20 Ω·cm, 50-100 Ω·cm, 100-400 Ω·cm, 600-1.1k Ω·cm



I. Peric, 12th Trento Workshop, 2017

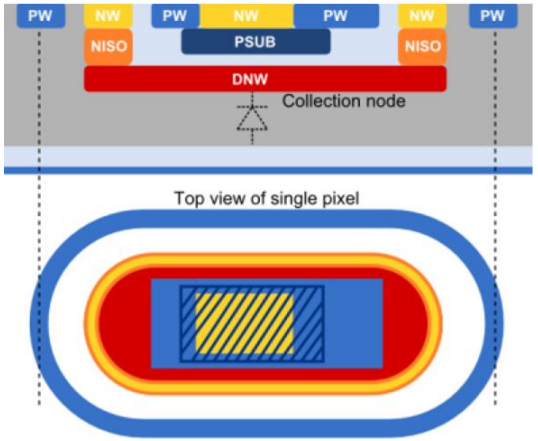
New design:

- Studies considering the integration of RD53-like periphery logic

LFoundry 150 nm

Key features:

- **Technology node** 150 nm
- **Wells** Deep p-well (PSUB) to isolate n-wells from deep n-well (collecting electrode). Full CMOS electronics are possible in the sensor area.
- **Metal layers** 6
- **HR** 10 Ω·cm – ~4k Ω·cm
- **HV** -120 V < HV < 0 V
- **Depletion region** ~170 µm thick @ -110 V
- **Backside biasing** Possible
- **Stitching** Possible

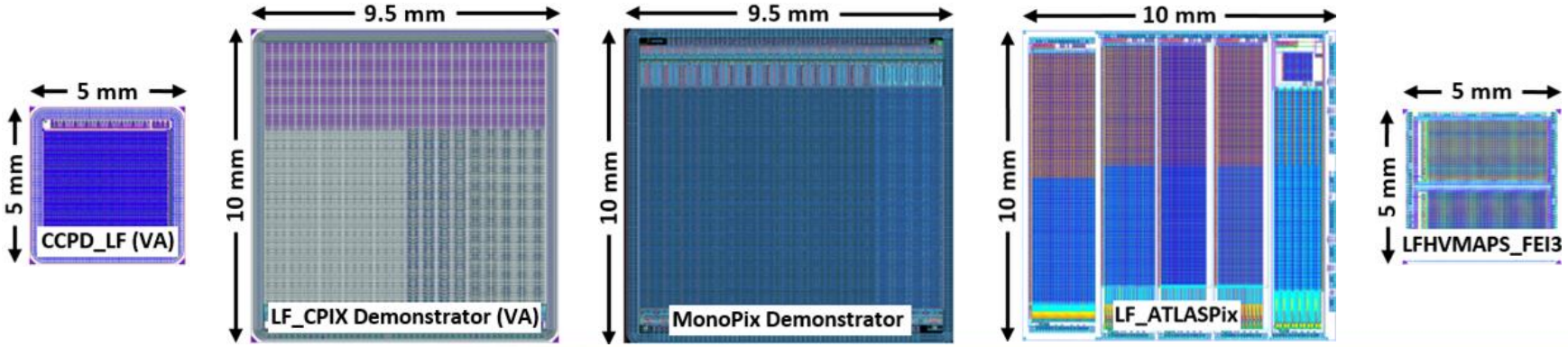


C_{PSUB_DNWELL} non-negligible

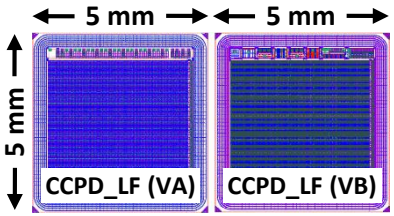
P. Rymaszewski, JINST 11 C02045, 2016

Prototypes:

- CCPD_LF (VA/VB), LF-CPIX Demo. (VA/VB), MonoPix Demo., COOL, LF_ATLASPix, LFHVMAPS_FEI3

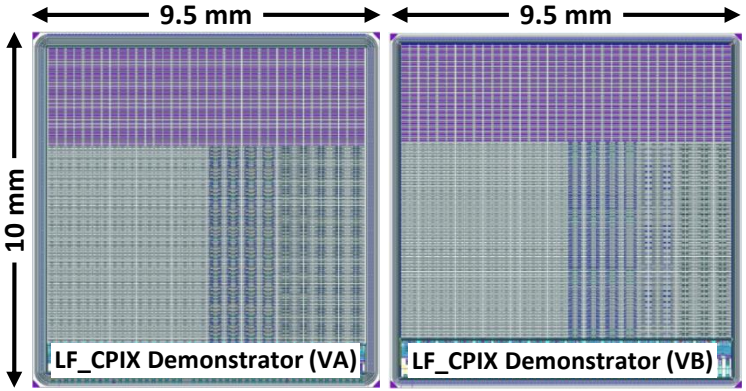


LFoundry 150 nm – Prototypes



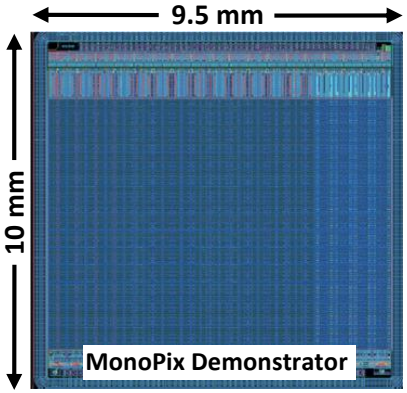
Features:

- Submitted in August 2014
- Design by Bonn, CPPM, KIT
- 33 µm x 125 µm pixels
- R/O coupled to FE-I4
- Sub-pixel encoding, res: 2k Ω·cm



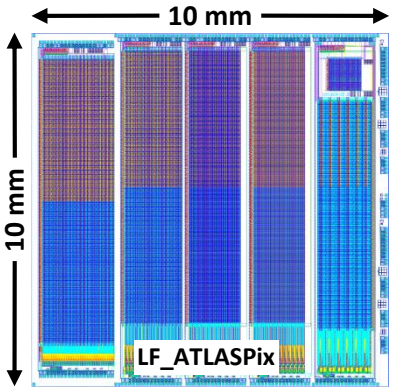
Features:

- Submitted in April 2016
- Design by Bonn, CPPM, IRFU
- 50 µm x 250 µm pixels
- R/O coupled to FE-I4
- No sub-pixel encoding
- Improved version of CCPD_LF chip



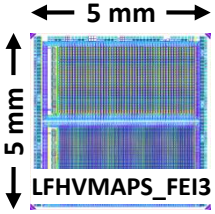
Features:

- Submitted in August 2016
- Design by Bonn, CPPM, IRFU
- 50 µm x 250 µm pixels
- Standalone R/O
- Resistivity: 2k Ω·cm



Features:

- Submitted in August 2016
- Design by IFAE, KIT, Uni. Geneva and Uni. Liverpool
- Different pixel sizes
- Different matrices (1 CCPD and 5 monolithic) and test structures
- Resistivities: 100 Ω·cm, 500-1k Ω·cm, 1.9k Ω·cm and 3.8k Ω·cm



Features: **New prototype within RD50**

- Submitted in November 2016
- 50 µm x 50 µm pixels
- Design by IFAE and Uni. Liverpool
- 2 monolithic matrices and test structures
- Resistivities: 500 Ω·cm and 1.9k Ω·cm

COOL chip:

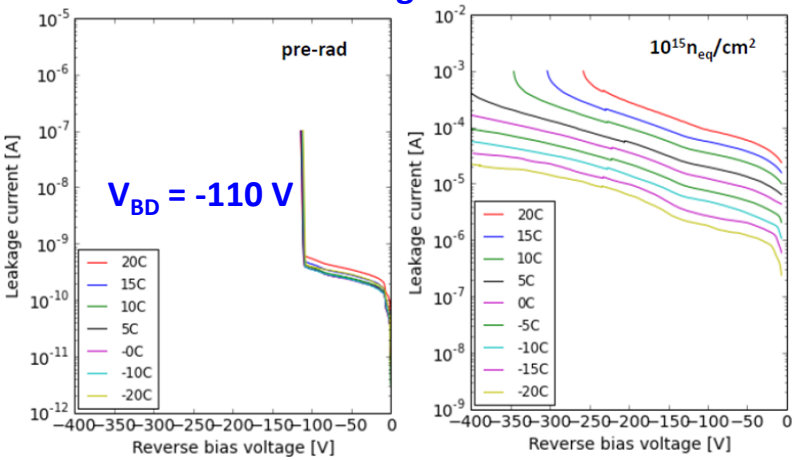
- Designed by SLAC, submitted in August 2016
- 50 µm x 250 µm pixels

LFoundry 150 nm – Results from CCPD_LF

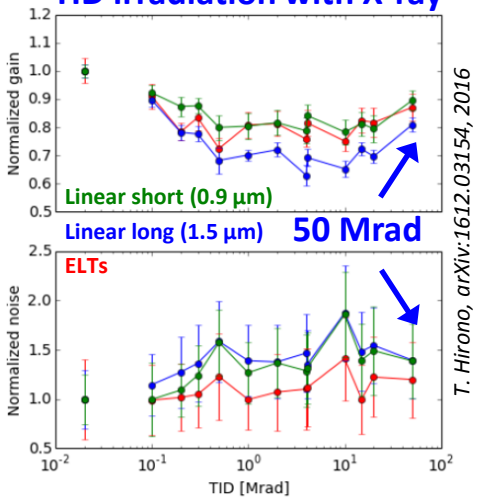
Summary:

- 2k Ω·cm
- Thinned to 100 µm - 300 µm
- Backside contact for HV
- 33 µm x 125 µm pixels, 3 x 2 pixels = 2 FE-I4 cells
- Sensor R/O includes: pulse input, CSA, comparator with 4-bit trim DAC and output stage for voltage amplitude encoding
- Sensor chip attached to R/O chip

Leakage current



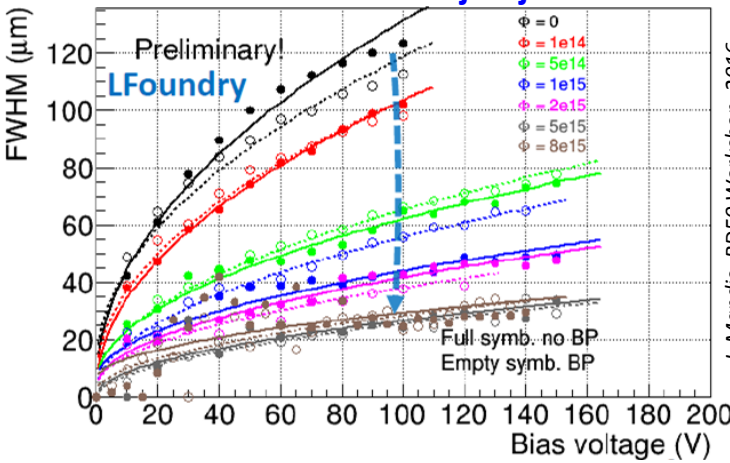
TID irradiation with X-ray



T. Hirono, arXiv:1612.03154, 2016

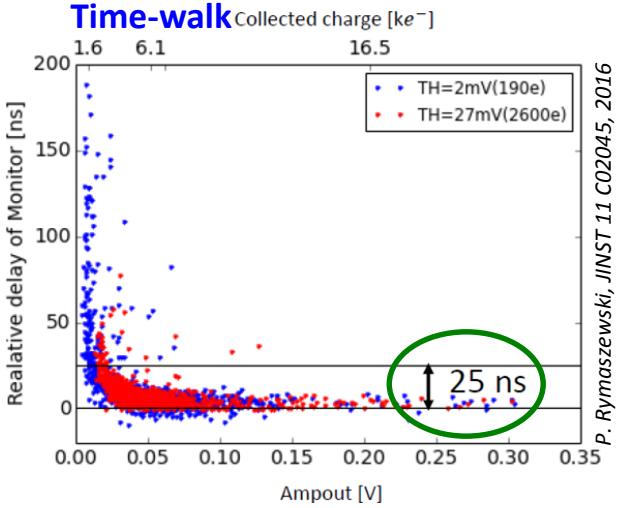
Chips functional after irradiation, but with 20-30% less gain

Neutron irradiation at Ljubljana + e-TCT



I. Mandic, RD50 Workshop, 2016

Time-walk

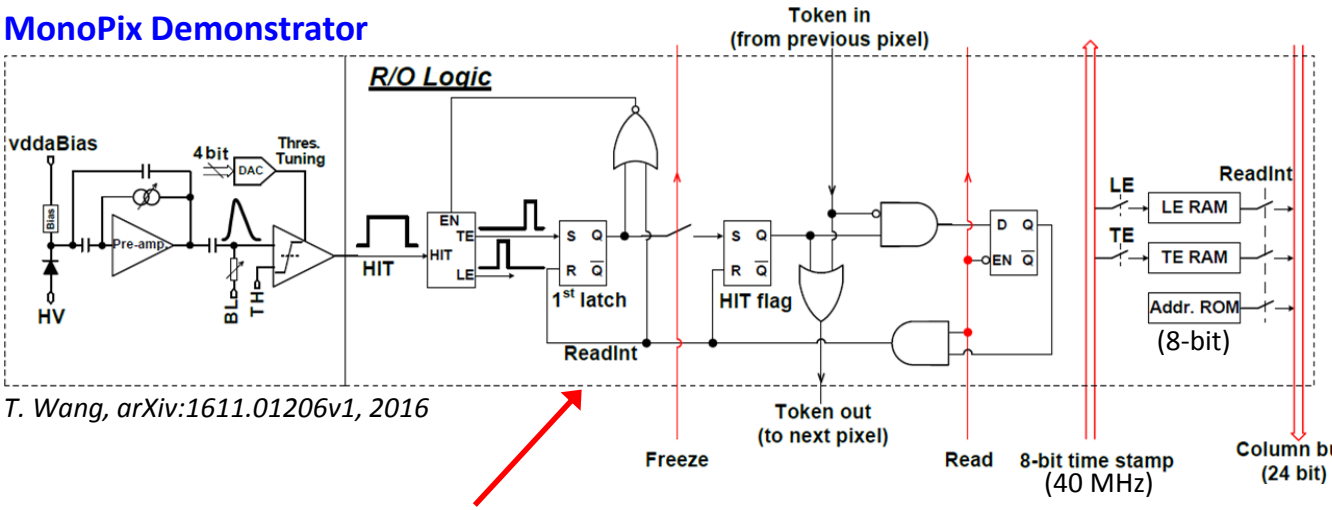


P. Rymaszewski, JINST 11 C02045, 2016

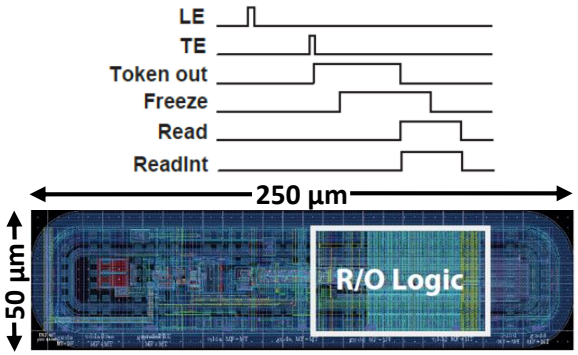
High threshold (2600 e⁻) → 79% hits in-time
Low threshold (190 e⁻) → 91 % hits in-time

LFoundry 150 nm – Fully monolithic designs FEI3-style

MonoPix Demonstrator

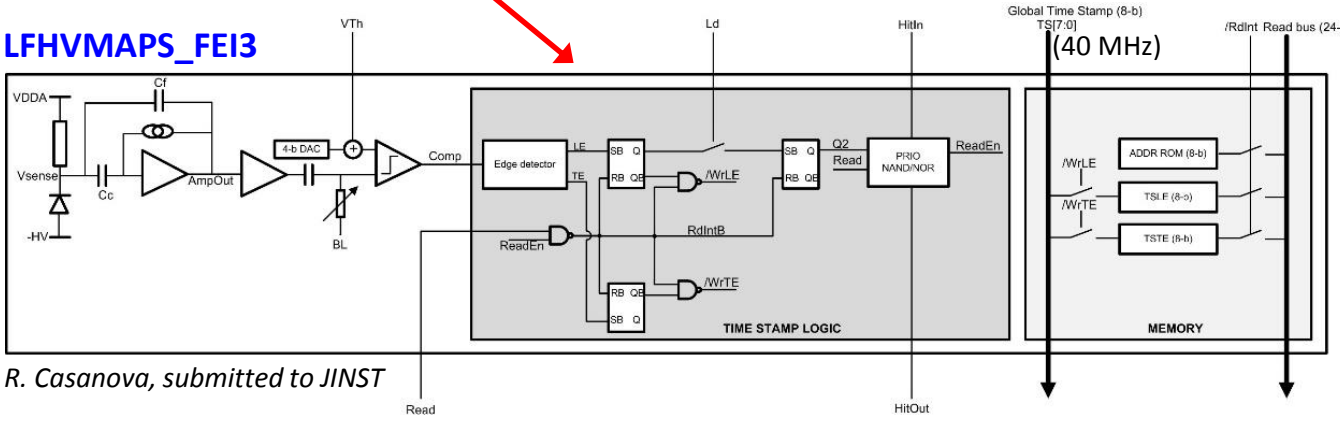


T. Wang, arXiv:1611.01206v1, 2016

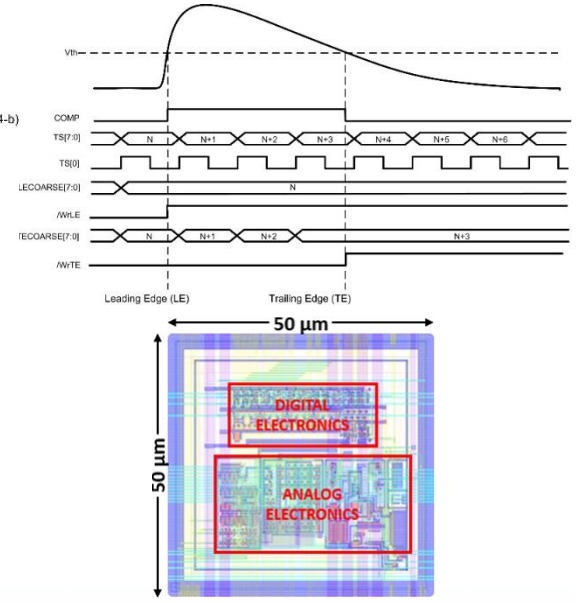


It is possible to embed all these electronics inside the sensor area (PSUB)

LFHVMAPS_FEI3



R. Casanova, submitted to JINST

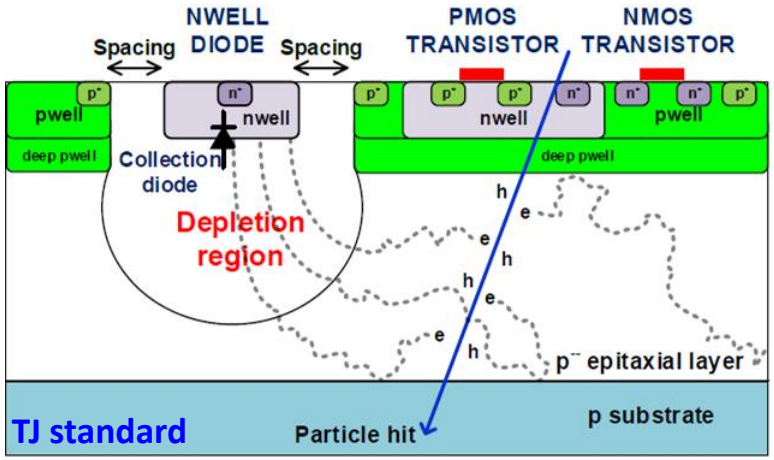


Fully monolithic sensors with standalone R/O

TowerJazz 180 nm

Key features:

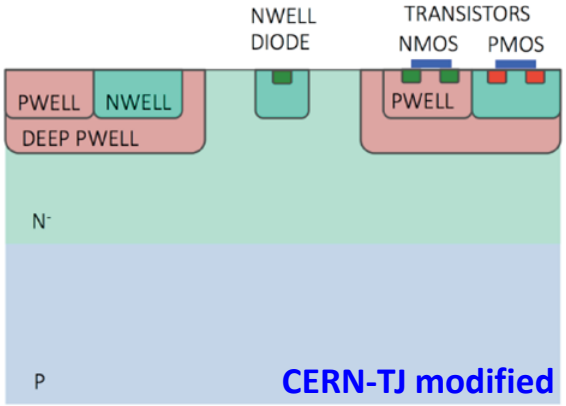
- **Technology node** 180 nm
- **Wells** Deep p-well to isolate n-wells from p-epi layer. Full CMOS electronics are possible in the sensor area.
- **Metal layers** 6
- **Gate oxide** 3 nm (good for radiation tolerance)
- **HR** 1k – 8k Ω·cm
- **HV** -6 V < HV < 0 V
- **Epi-layer** 18 – 40 µm thick
- **Backside biasing** Possible
- Small n-well diode → low sensor capacitance (~5 fF) → higher gain, better SNR, faster signal and potentially lower power consumption



D. Kim et al., JINST 11 C02042, 2016

CERN-TJ modified process:

- Normally, small electrodes produce weak fields under deep p-wells and signal collection after irradiation becomes difficult on edges (efficiency drop towards pixel edges)
- CERN-TJ → Add planar n-type layer to significantly improve lateral depletion and charge collection after irradiation. Implemented in Investigator test chip.



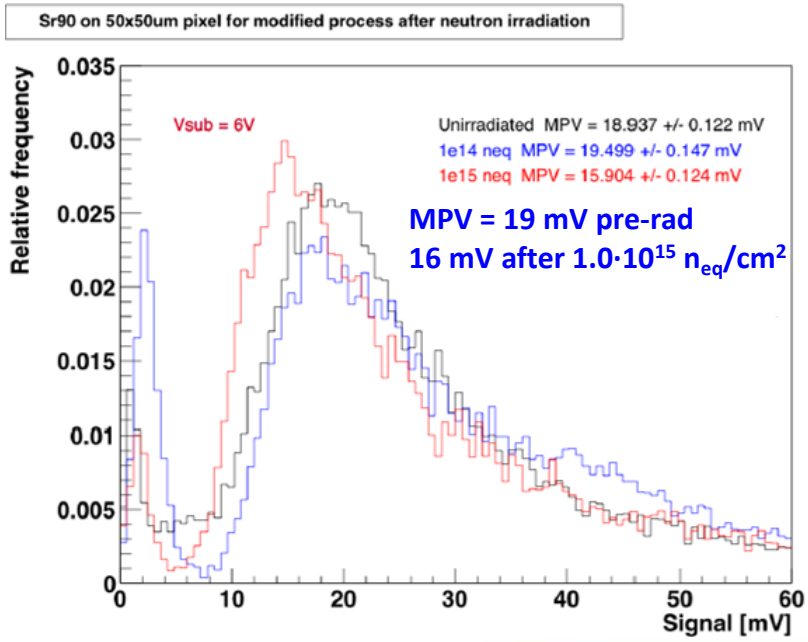
H. Pernegger, Trento Workshop, 2017

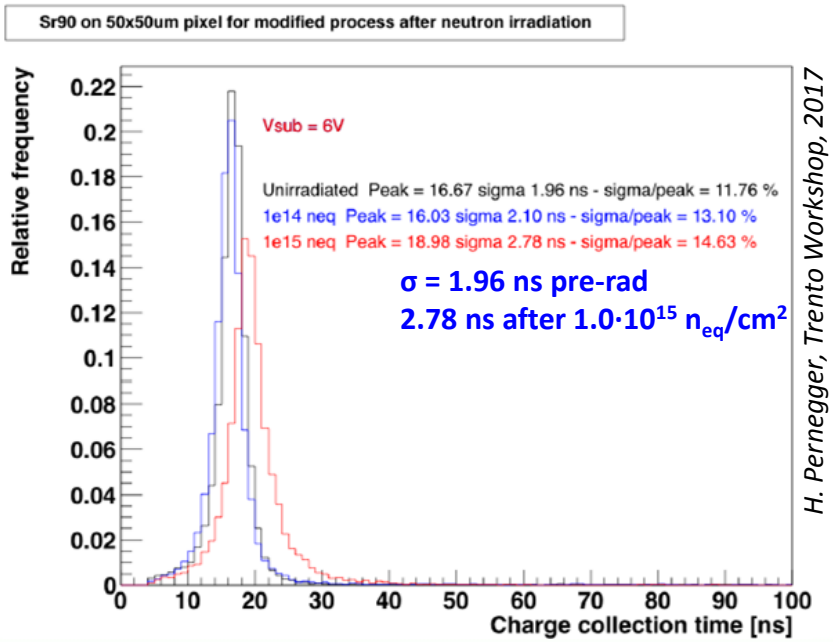
Prototypes:

- ALPIDE (ALICE upgrade chip), MISTRAL, ASTRAL, CHERWELL, Explorer, Investigator, MALTA, MonoPix

TowerJazz 180 nm – Results from Investigator

- **Investigator chip** has pixels with → 50 µm pitch, 3 µm size collection electrode and 20 µm spacing
  25 µm p-epi layer
- Investigator irradiated in IJS Ljubljana (TRIGA) in several steps up to $1.0 \cdot 10^{15}$ n_{eq}/cm^2 (NIEL $1.0 \cdot 10^{15}$ n_{eq}/cm^2, 1 Mrad TID)
- Measurements up to 10^{16} n_{eq}/cm^2 are ongoing
- Little change to signal after irradiation
- First test beam measurements indicate no efficiency loss on pixel boundaries after $1.0 \cdot 10^{15}$ n_{eq}/cm^2 (standard process not working after this fluence)





H. Pernegger, Trento Workshop, 2017

TowerJazz 180 nm – New prototypes

New developments towards a dedicated CMOS chip that matches ATLAS specifications:

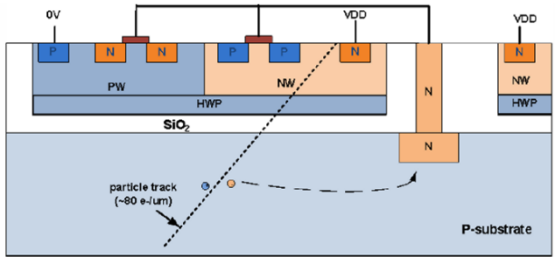
- Analog front-end with CSA + discriminator optimized for 25 ns in-time efficiency and low threshold operation
- 2 cm x 2 cm chip size with < 50 µm x 50 µm pixels
- Monolithic design includes readout architecture which copes with ATLAS outer layer hit rate requirement

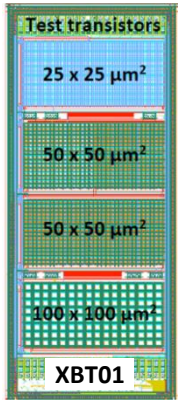
	TJ MALTA chip	TJ MonoPix chip
Pixels	512 x 512	512 x 526
Active area	18 mm x 18 mm	18 mm x 10 mm
Features	Hit memory in active matrix All hits are asynchronously transmitted over high speed bus to EoC logic No clock distribution over active matrix to minimize power and digital-analog crosstalk	Hit memory in active matrix (2 FF per pixel) Synchronous column drain architecture Hit address asserted to bus with 40 MHz 6-bit ToT encoding at end of column
Design	CERN	Bonn

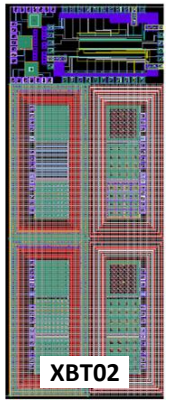
Other technologies

XFAB:

- **Technology node** 180 nm (SOI)
- **Wells** Deep pw, full CMOS
- **Metal layers** 7
- **HR** 100 Ω·cm
- **HV** > -200 V
- **Backside biasing** Not possible
- **Design/Testing** Bonn, CERN, CPPM



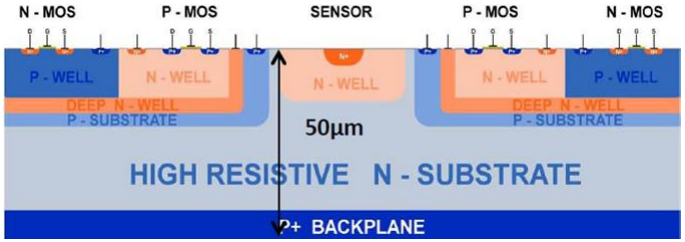


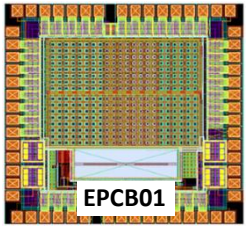


700 Mrad
$5 \cdot 10^{14}$ n_{eq}/cm^2
N. Wermes, 2016

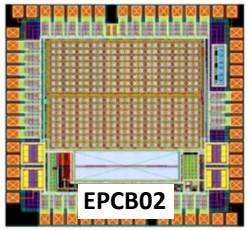
ESPROS:

- **Technology node** 150 nm
- **Wells** Deep pw, full CMOS
- **Metal layers** 6
- **HR (n-type bulk)** 2k Ω·cm
- **HV** > -20 V
- **Depletion region** ~50 µm
- **Backside biasing** 50 µm + p-implant
- **Design** Bonn, Prague





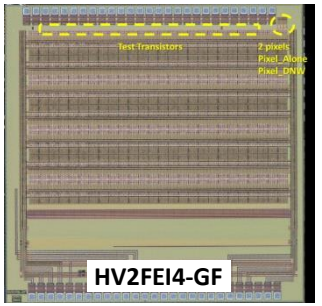
Techno. exploration
40 µm x 40 µm pixels
50 Mrad
$5 \cdot 10^{14}$ n_{eq}/cm^2 *M. Havranek, JINST 10 P02013, 2015*



Improvement of first version

Global Foundries:

- **Technology node** 130 nm
- **Metal layers** 8
- **HR** 10 Ω·cm – 3k Ω·cm
- **HV** > -30 V



33 µm x 125 µm pixels
26 cols x 14 rows
Irradiated to 600 Mrad
Glued to FEI4

P. Pangaud, , 2014

Summary

- At present time, lots of R&D dedicated to the development of HV/HR-CMOS/MAPS detectors:
  - In different commercially available HV-CMOS technologies
    - ams 0.35 µm, ams 180 nm, LFoundry 150 nm, TowerJazz 180 nm, XFAB 180 nm, ESPROS 150 nm, Global Foundries 130 nm…
  - A large number of prototypes and a few demonstrators have been produced
  - Encouraging results
  - Good radiation tolerance

- Option to readout HV-CMOS sensors with existing R/O ASICs:
  - FEI4
  - CLICpix

- Recent alternative of monolithic HV-MAPS with standalone R/O:
  - With digital circuits in the periphery or in the sensor area depending on the technology

- Steps towards the integration of periphery circuits in prototypes