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SINBAD ELECTRONIC MODELS OF THE INTERFACE AND CONTROL SYSTEM FOR THE NOMAD SPECTROMETER ON BOARD OF ESA EXOMARS TRACE GAS ORBITER MISSION

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ABSTRACT

NOMAD is a spectrometer suite: UV-visible-IR spectral ranges. NOMAD is part of the payload of ESA ExoMars Trace Gas Orbiter Mission. SINBAD boards are in charge of the communication and management of the power and control between the spacecraft and the instrument channels. SINBAD development took four years, while the entire development and test required five years, a very short time to develop an instrument devoted to a space mission. The hardware of SINBAD is shown in the attached poster: developed boards, prototype boards and final models. The models were delivered to the ESA in order to testing and integration with the spacecraft.

Keywords: ExoMars, NOMAD, FPGA, breadboard, prototype, flight models.

1. INTRODUCTION

NOMAD (Nadir and Occultation for Mars Discovery [1]) is an instrument led by the Belgian Institute for Space Aeronomy (BIRA) and designed together with the Instituto de Astrofísica de Andalucía, Spain (IAA) and The Open University (OU), United Kingdom. NOMAD is composed by three spectrometers: Solar Occultation (SO [2],[3]), Limb and Nadir Observation (LNO[2],[3]) and Ultraviolet and Visible Spectrometer (UVIS[4]). The instrument has been designed to measure over two infrared channels, SO & LNO, and one ultraviolet-visible channel, UVIS. The instrument can perform observations almost constantly, by taking nadir measurements at day and night side, and during sunset/sunrise in solar occultation. NOMAD is part of the payload on board of ESA ExoMars Trace Gas Orbiter (TGO) Mission on 2016. Figure 1 shows the block diagram of NOMAD Instrument.

SINBAD (Spacecraft Interface and coNtrol Boards for NOMAD) is the NOMAD subsystem in charge of the communication between the spacecraft and instrument's channels and the management of power distribution, as can be seen in Figure 2. Two boards have been designed for these tasks, one board for the power conditioning and distribution

and Housekeeping acquisition, called POW board , which includes also the DC/DC module, and the second board for the communication with the spacecraft and the channels and control of the whole instrument, called COM board.

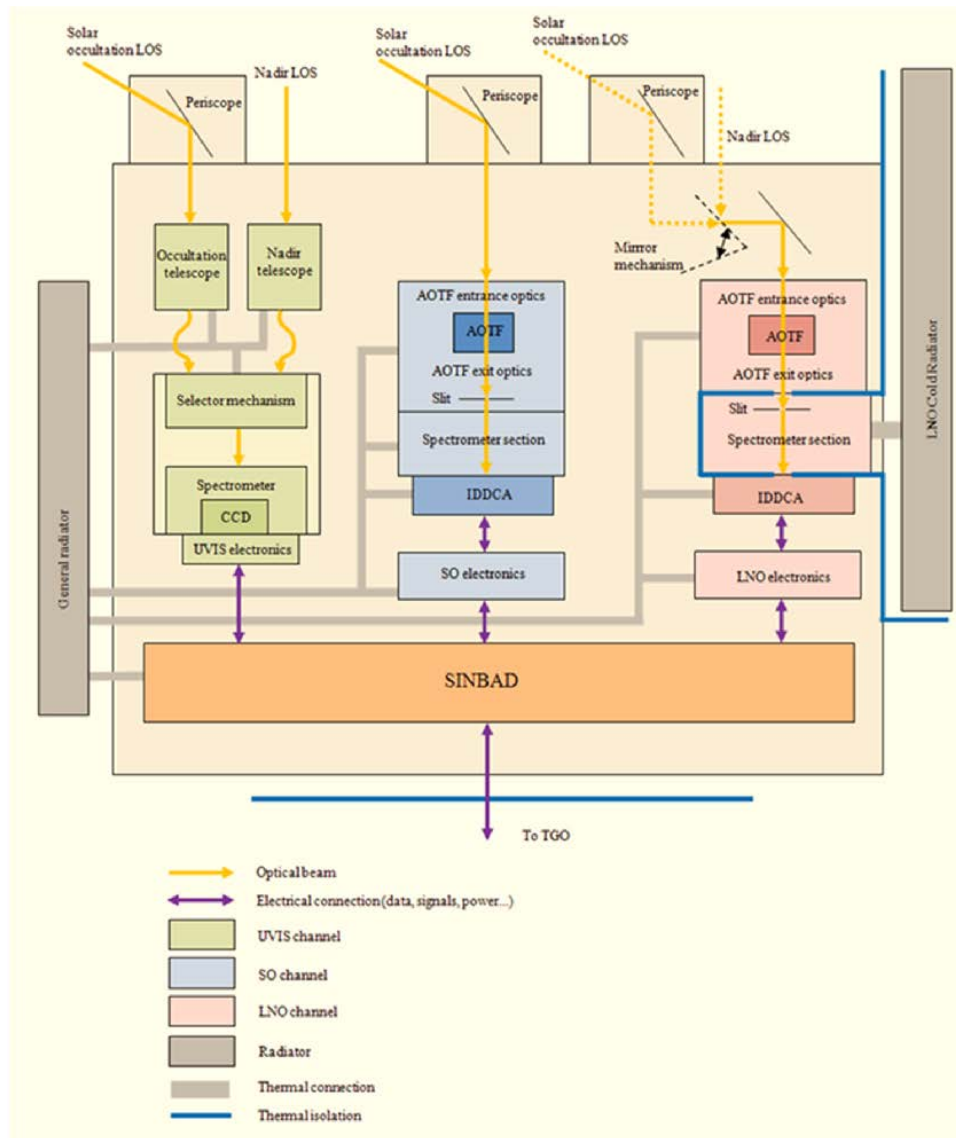


Figure 1 NOMAD Block Diagram

SINBAD system [5] uses a System on Chip (SoC) with a LEON3FT processor and a FPGA to manage communication with channels and Housekeeping acquisition. The telecommands and housekeeping are managed via a dedicated 1MHz MIL-STD-1553B bus. An external connector configures the Remote Address for NOMAD. The science data telemetry is transmitted through a 20Mbit per second SpaceWire (SpW) bus. Both buses are duplicated to achieve redundancy. The communications with the channels are implemented through a 1MHz RS-422 interface for UVIS and through two 100MHz LVDS serial buses for SO and LNO channels. SINBAD system also controls the other internal subsystems: voltage and current acquisition, temperature sensors, actuators (flip mirror and pin-puller), heaters, and ADC conversion system. Finally it also includes a RS-422 test port for debugging.

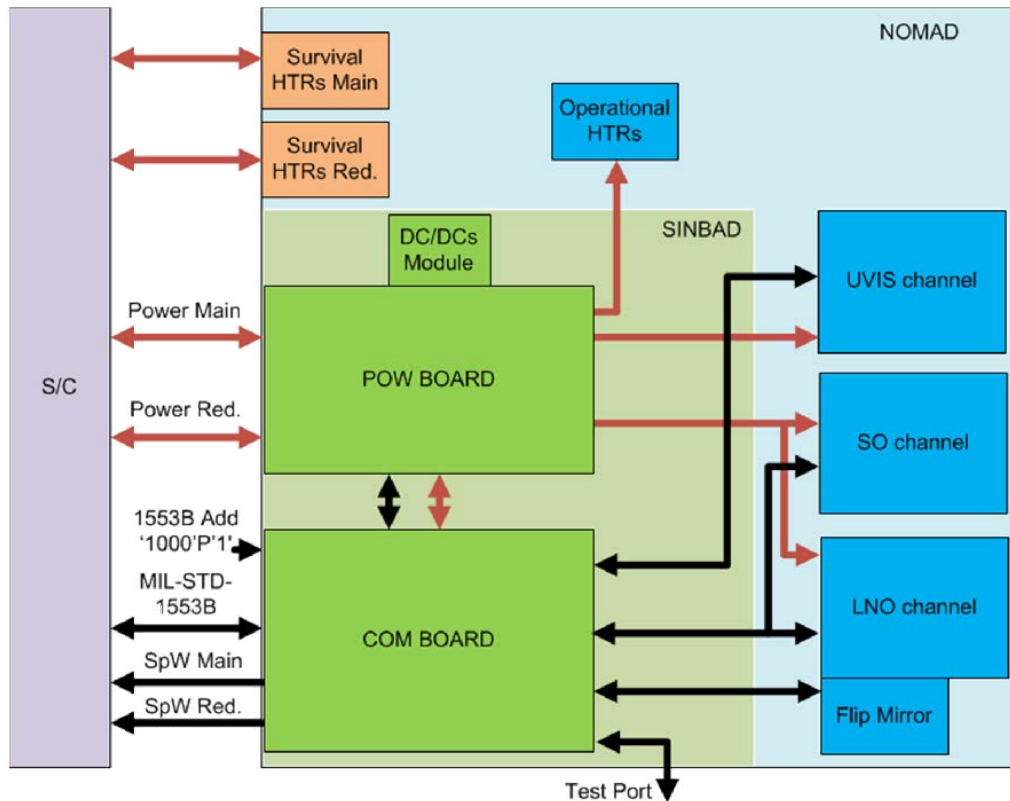


Figure 2 SINBAD Block Diagram with the interfaces.

1.1 POW Board

The power board receives the primary power from the Spacecraft through a main and redundant input. The active power channel is automatically selected by High Power Command (HPC), routed through a soft-start circuit, filtered and taken to the DC/DC converters.

These converters provide isolation between primary and secondary power bus and generate the secondary voltages required by the system.

The POW board also includes the switching system to power independently each of the three scientific channels. It also implements the temperatures, voltage and current acquisition and the analogue to digital conversion, as well as an Auto-power off system controlled by the SINBAD Flight software (SFS), which is used in case of emergency.

1.2 COM Board

The communication and control board is based on two interconnected Actel-RTAX2000-SL FPGA devices. The first FPGA (named "Shireen") implements a SoC which includes a fault tolerant Leon3 processor (32bits SPARC-V8 based), running at 25MHz and a collection of interfaces implemented as peripherals of the processor. The processor controls the interfaces with the spacecraft (SpaceWire and MIL-STD-1553B links), with the UVIS channel and transmits status information through the test and debugging ports. The second FPGA (named "Chimera") manages all other internal subsystems, including stepper motor and pin puller mechanism, and it also contains a processing module designed by BIRA for the image accumulation and the I/F with the SO and LNO channels.

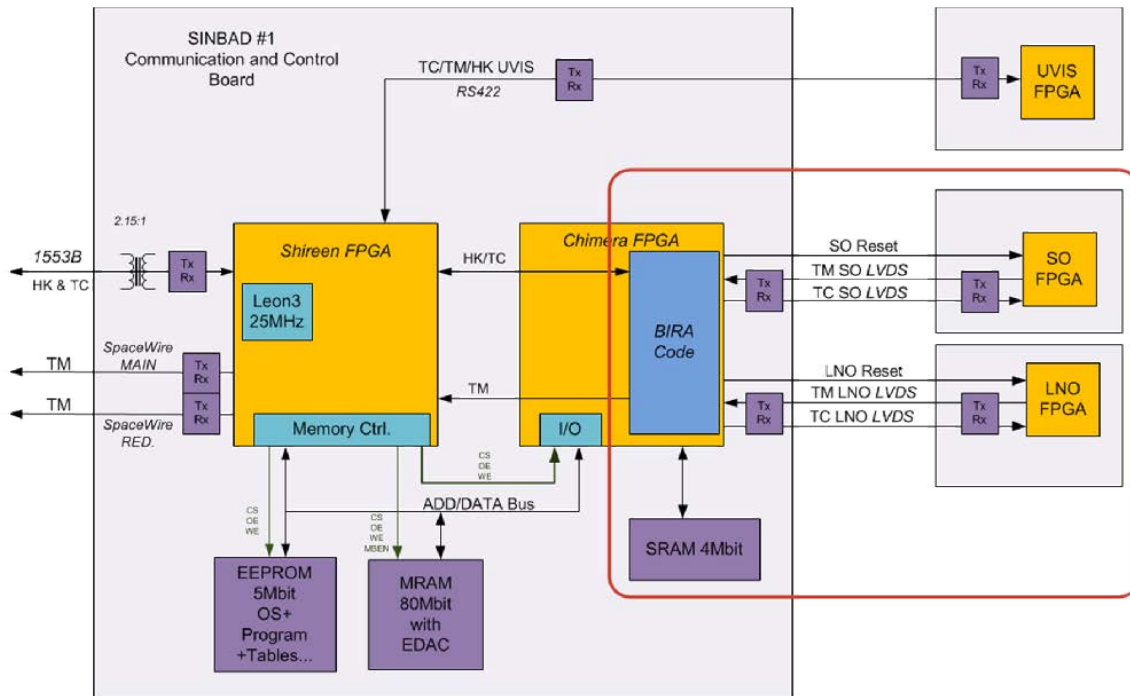


Figure 3 SINBAD Communications Block Diagram

The external memories of the SoC design are:

An EEPROM (Electrically Erasable Programmable Read Only Memory) stores the Application Program (SFS), the context table with the system configuration parameters and the observing parameters tables.

Five Magnetoresistive RAM memories (MRAM) implemented with novel devices, first time used in European space mission. These devices provide a way to data interchange RAM and at the same time, as massive storage with the SFS.

Both memories, MRAM and EEPROM, are protected with EDAC (Error Detection And Correction system) implemented inside Shireen within the Memory Controller IP Core. This function is in addition to the one already implemented inside the MRAM itself. The implemented EDAC detects up to two bit errors in a 16 bits word and can correct one bit error.

The enclosed blocks in the red line (Figure 3) are responsibility of BIRA. These blocks are dedicated to receive and send the telecommands, telemetries and Housekeeping from SO and LNO channels, besides to process the scientific data. For this reason, the Chimera Code has been shared between IAA and BIRA.

1.3 FPGAs

The selected FPGAs are Actel RTAx2000SL devices because of their radiation tolerance characteristics and low power consumption. This FPGA family has Triple Modular Redundancy (TMR) due to the use of the built-in flip-flops and so they are SEU-hardened.

Shireen must manage the communications with the external interfaces. The architecture uses IP cores to manage each interface. The arbitration between all these cores and the internal communication is done using a standard bus already tested for space designs, the AMBA (Advanced Microcontroller Bus Architecture) bus. Figure 4 shows the block detailed design inside Shireen.

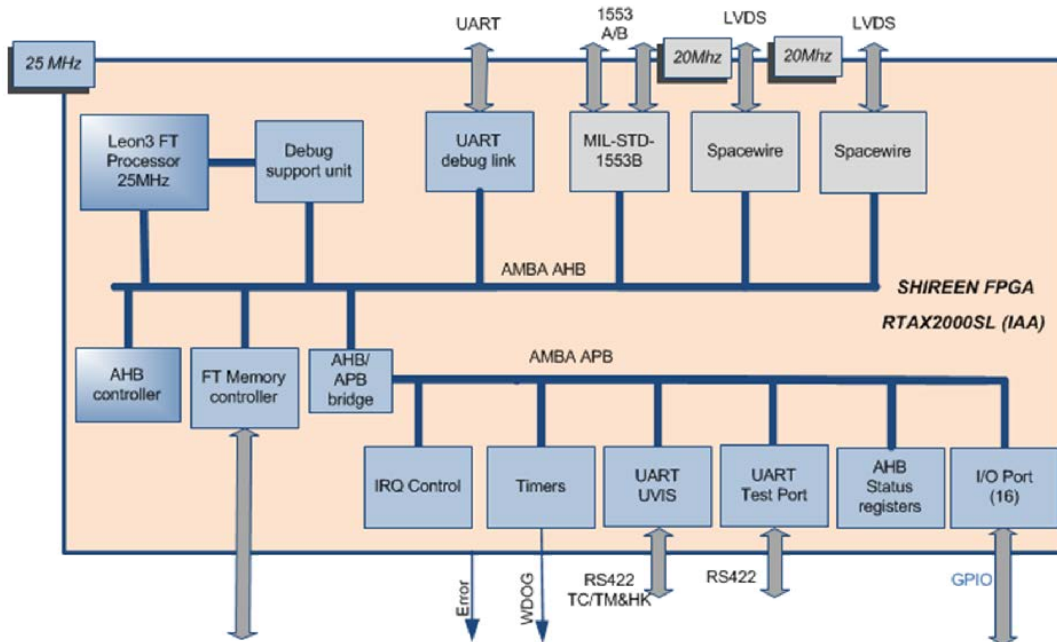


Figure 4 Shireen block detailed design

As it can be seen, this FPGA is based in a Gaisler embedded system, which has been configured to fit with the requirements. The final design incorporates a Leon3-FT, a memory controller, 3xUART ports, and 2xSpaceWire and MIL-STD-1553B cores. The system clock runs at 25MHz.

Chimera firmware is divided in two parts: the first part is in charge of SO and LNO channels control and image acquisition. The second part is in charge of peripheral management: stepper motor control, ADC reading, after watchdog register and heaters control.

Chimera connects with an external SRAM used to store the spectrum accumulation and after it is moved to the internal RAM of Chimera. Detailed design can be seen on figure 5.

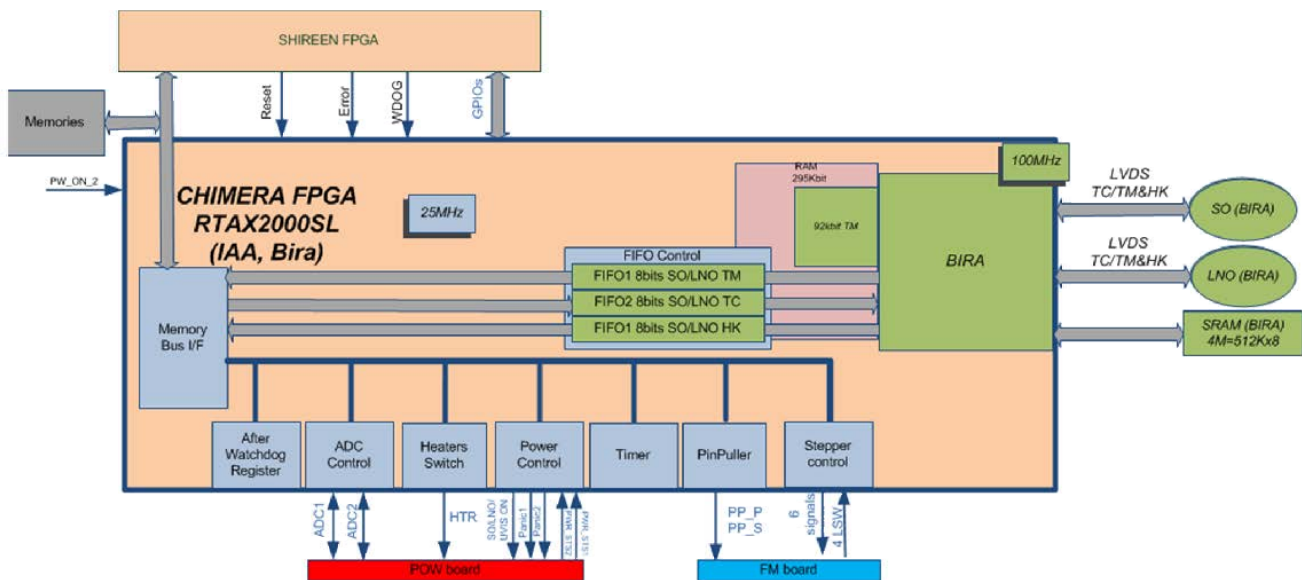


Figure 5 Chimera Block detailed design

Both devices (Chimera and Shireen) communicate between themselves using the memory bus in the I/O map of the processor. Chimera provides a set of registers that are mapped in the memory of the SoC. It has been necessary to include in Chimera an address decoder and a controller to arbitrate communications needed between the different blocks. Each block shown in the figure 5 has one or several registers associated that can be read/written by Shireen, creating an interface used to command the FPGA and to show the state of the subsystem. Despite being controlled by Shireen, Chimera is capable to operate autonomously the operational heater once the sensed temperatures exceed the programmed limits. Finally, all the subsystems in Chimera can be activated or deactivated via software.

2. SINBAD: COM Board Prototypes and Models

In order to ease and check the development of the instrument, a set of models has been produced. Each model is closer to the final instrument, and the development of these models is useful to test different functionalities. The number of delivered models was agreed between ESA and different partners of the instrument.

2.1. Bread-Boards

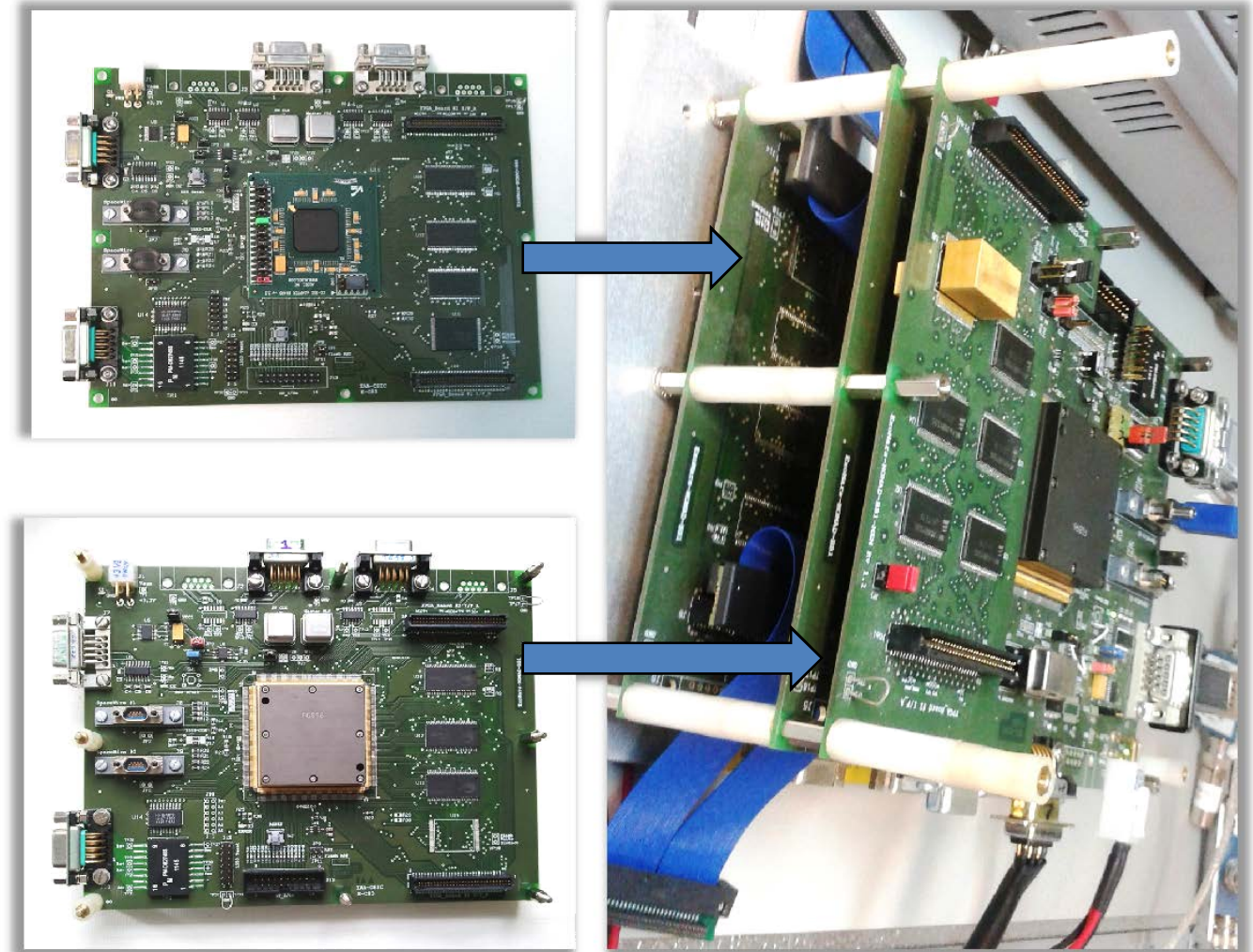


Figure 6 SINBAD Bread Boards

A set of boards has been developed in order to test the functionality of the SINBAD COM board. This system is based in stackable boards: a motherboard with two board to board connectors disposed in order to extend the different modules through the common busses. The motherboard contains an ALDEC prototype adaptor with a ProASIC3 device. This adaptor is used to prototype the RTAx device that contains Chimera, as the ALDEC netlist to netlist converter allows to program for a RTAx device and burn a ProASIC reprogrammable device (via JTAG). RAM and flash system memories, a GPIO (General Purpose Input/output) system and all the data communications ports are also included in the motherboard. The board can be connected to a twin board or to other boards, like memory boards, through the mentioned stackable connectors. The twin board of the Figure 6, has got a FBGA896 to FP352FPGA socket to allocate an AX2000 FPGA and contains Shireen. Both boards can be connected also via the shielded blue cable of the Figure 6.

The Figure 6 (right) shows a memory expansion containing a set of MRAMs and the EEPROM. The MRAM memories have the ability to hold on the information when the system is powered off. These devices allowed the removal of the flash and RAM memories from the final design.

2.2. Prototype Board (1:1 scale)

The developed prototype board has the two interconnected FPGAs and the final configuration of the memory system. This board integrates all the SINBAD system functionalities, except the stepper motor driver.

The board incorporates the communications with the Spacecraft, via MIL-STD-1553B and SpaceWire, the communications LVDS and RS422 with the channels and the communications via RS232 and RS422 with the debugging and Test and Ports, respectively (see Figure 7).

The memories included are EEPROM and MRAMs to the Boot and application SW and a shared SRAM for the channels data. In this model a SRAM has been included to test the data processing of the SO and LNO channels.

It also includes management of the mechanism, stepper motor and Pin-puller control inside the FPGA, which has been tested with an external dedicated board connected to this prototype board.

This model has been tested with the Channel SO of SOIR (Solar Occultation in the Infrared) spare model. SOIR is the IR channel built by Belgian Institute for Space Aeronomy for SPICAV instrument on board of ESA Venus Express Mission.

This prototype board has been also used and is in BIRA-IASB facilities to test the NOMAD EGSE (Electrical Ground Support Equipment) system.

A 1:1 prototype of the POW board has been also manufactured. It includes the whole system to be implemented on the flight model and it has been used to validate the design.

Test of the DC/DC converter system forced to change the converter model used because the peak current at the start-up of the cryocooler motor of the flight units. Due to space limitation, the converters were separated by the POW board and allocated in an external module.

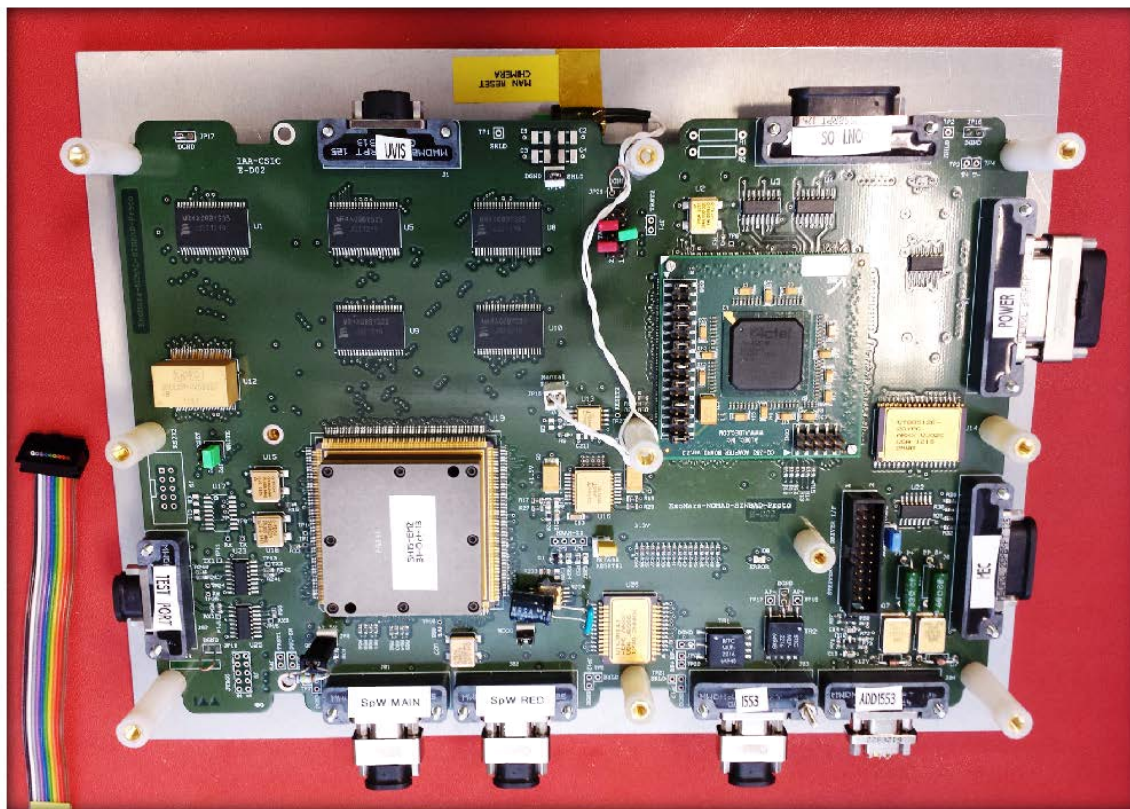


Figure 7 SINBAD Prototype Board

2.3. Engineering models: SINBAD EIM, NOMAD EIM and SINBAD EM

2.3.1 NOMAD EIM (1:1 scale)

The NOMAD Electrical Interface Model (EIM) is the model delivered to ESA as an engineering fully representative model of the flight Interface with the spacecraft. This model has resistive loads to simulate the electrical load of the scientific channels and the data and telemetry output is internal generated by software. Since in this model the science channels are simulated, the telemetry has been also simulated to emulate all the functionalities, with the delivered Application Software, booting Software (SFS) and Firmware.

Shireen was programmed into a proto FPGA device with the final flight Firmware. Chimera FPGA, allocated in a socket-adaptor has been tested with the SFS V0.1.0 in EEPROM and SFS V0.1.1 in MRAM. The procedure and reports have been generated according to ESA standards. Most of the components used in this model as well as the PCBs (Printed circuit board) are flight qualified. This model can be connected to the spacecraft and can receive telecommands and generate the instrument telemetry.

The NOMAD EIM is shown in Figure 8 and Figure 9. The elements of this model are SINBAD EIM , the resistive loads to simulate channels power consumption and heaters. Within SINBAD EIM the upper board is the COM (Figure 10) and the lower is the POW one with the DCDC module (Figure 9).



Figure 8 NOMAD EIM Front Panel

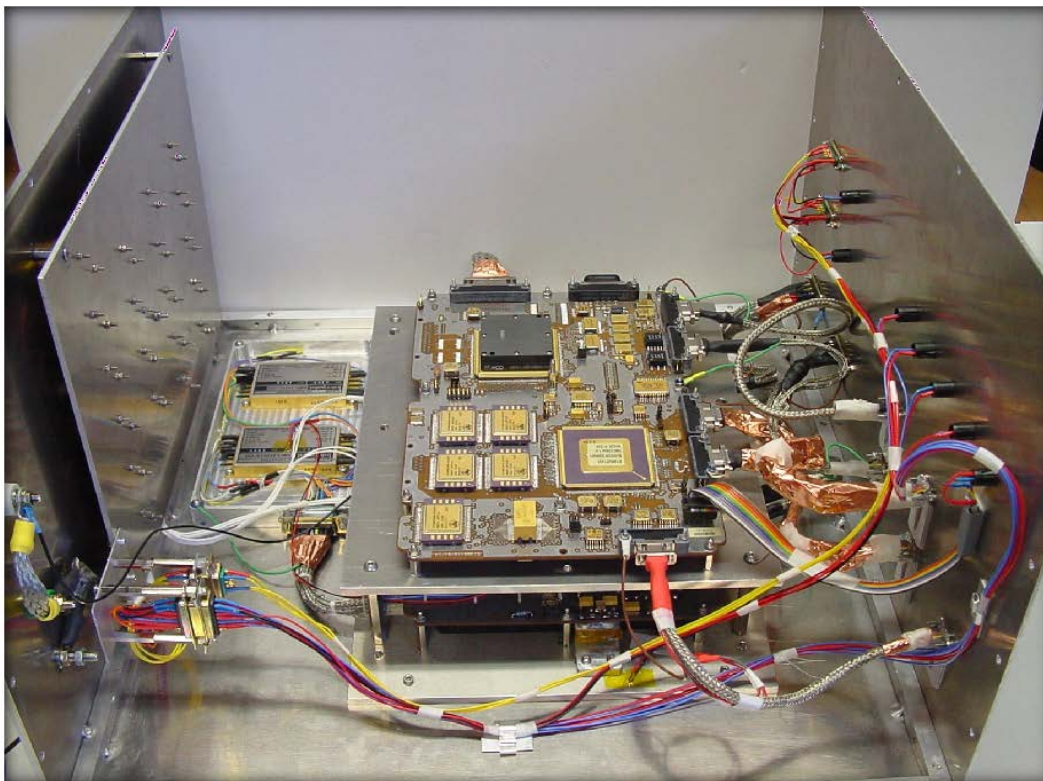


Figure 9 Inside NOMAD EIM

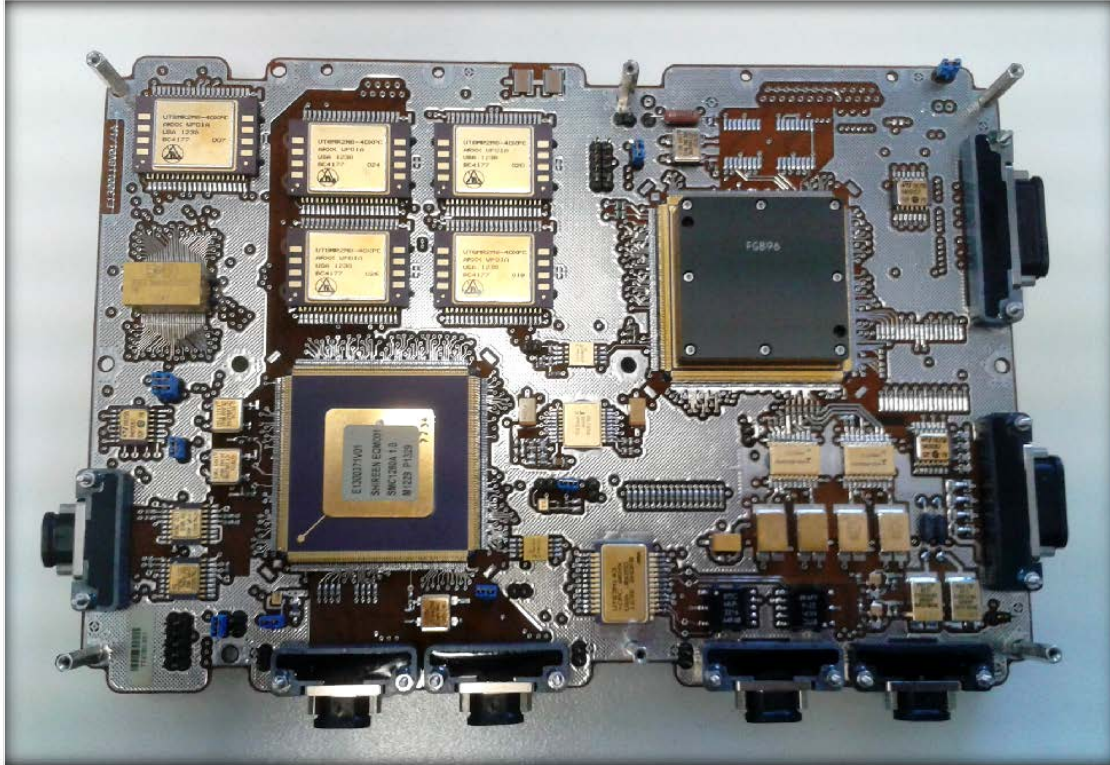


Figure 10 SINBAD EIM COM Board

2.3.2 SINBAD EM

The SINBAD Engineering Model (EM) is similar to the EIM and 1 to 1 scale at the flight models. In this model the Board (Figure 11) is fully populated. The channels have been tested with simulators: one of the UVIS prototype lent by Open University (OU) and one Chimera development board programmed with the BIRA's code to simulate the SO and LNO channels (Figure 12). The Chimera FPGA was deeply tested with this environment. The model has been used in order to update the HW and the SW. This model, dedicated to the development and validation of the different versions of the SFS, will be used also during flight for this purpose and also to check any variation of the normal behavior of the flight unit.

SINBAD EM is the model ready to test any changes in the SFS when the instrument is already in flight. So, the software patch or updating is validated on this model before being transmitted by telecommands from ground to TGO. This model (Figure 13) is allocated in the Instituto de Astrofísica de Andalucía facilities for the entire mission.

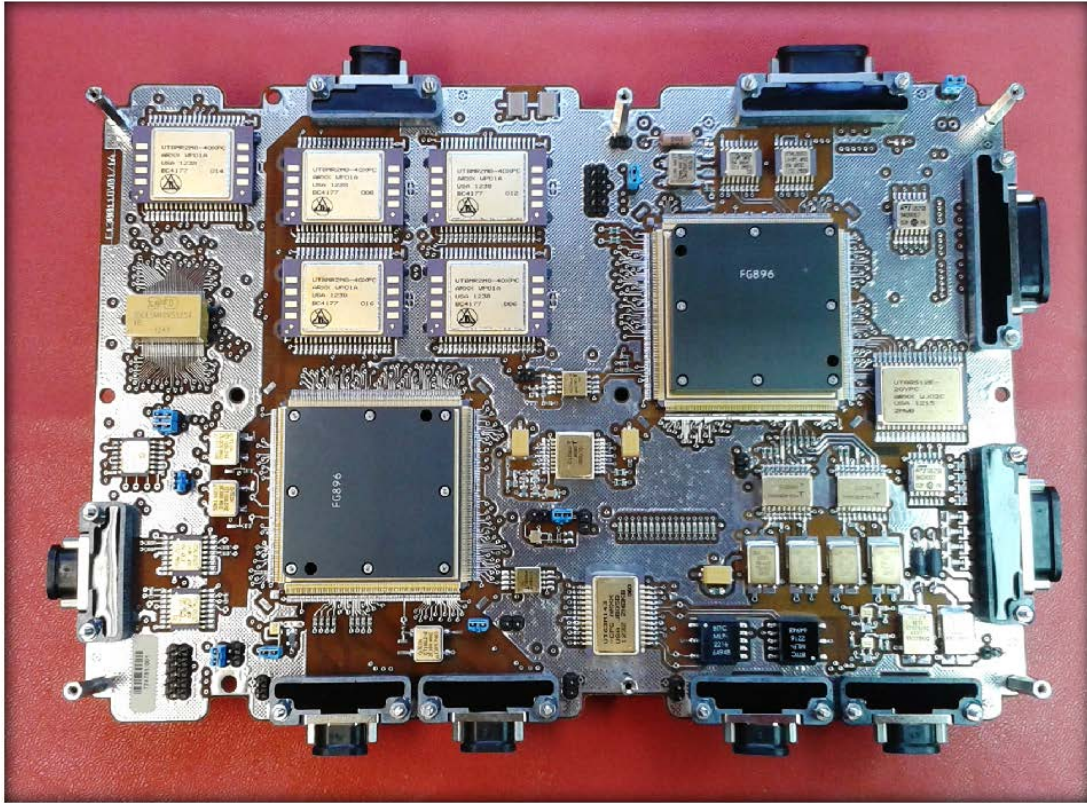


Figure 11 SINBAD EM COM

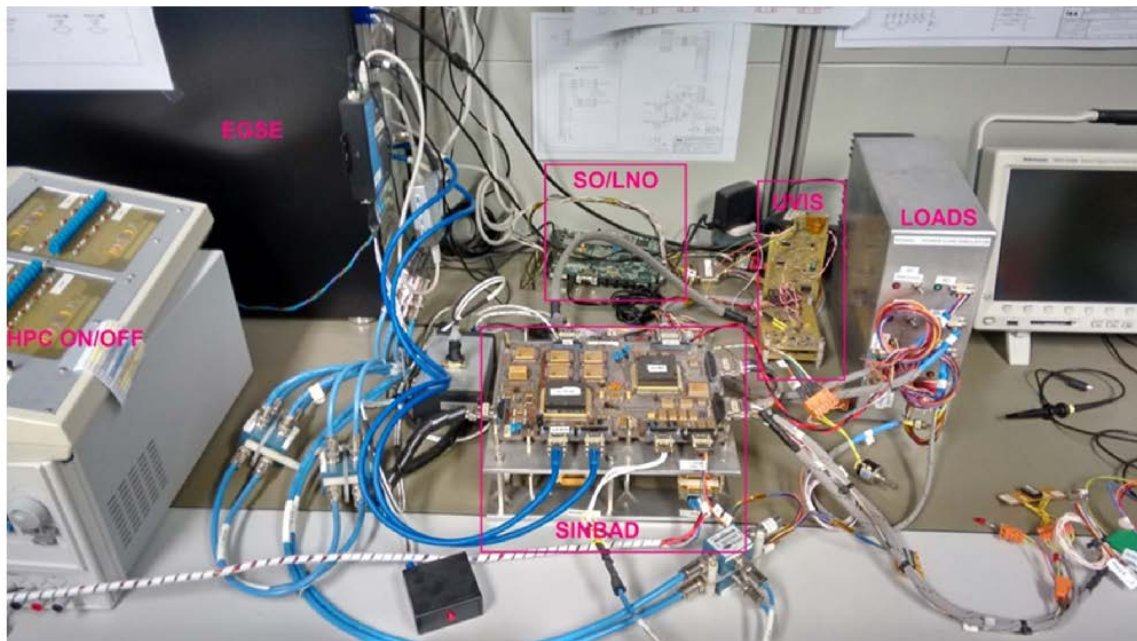


Figure 12 SINBAD EM under testing

Laboratory EGSE in the Figure 12 has been developed in the IAA to simulate the Spacecraft in their telecommands and telemetries functions.



Figure 13 Enclosed EM ready to develop SW

2.4. SINBAD PFM and SINBAD FS

SINBAD Proto Flight Model (PFM) is the model assembled with all the flight components. It has been assembled in an ISO 5 clean room. SINBAD PFM was initially tested at IAA with a prototype version of UVIS, resistive loads and simulator for SO/LNO channels and a QM (Qualification Model) version of flip mirror and Pin-puller mechanisms. SINBAD PFM has been tested completely twice, without and with conformance coating (Figure 14 Top layer and Figure 15 bottom layer).

Several small HW changes, for better performances, were made before coating: change of the UVIS transceivers, inclusion of some pull-up resistor on the channels' control lines and some low ESR (Equivalent Series Resistance) decoupling capacitor.

SINBAD PFM was integrated with the SO+LNO+UVIS channels and tested in NOMAD Proto Flight Model. After the electrical and functional tests, this model was tested for shock, vibration and thermal-vacuum.

During the Thermal cycling, the MRAMs did not work properly below 0°C. The malfunction was solved changing the Wait States number in the readout of the memories. As a side effect, this change affected the UVIS channel behavior because of the new slower data transfer rate, generating errors. Finally the problem could be successfully fixed through software patches.

SINBAD PFM had to be updated to include these changes at SFS 3.1.0 in MRAM. This update was done by telecommands when ESA let us a window in its test campaign with all the instruments.

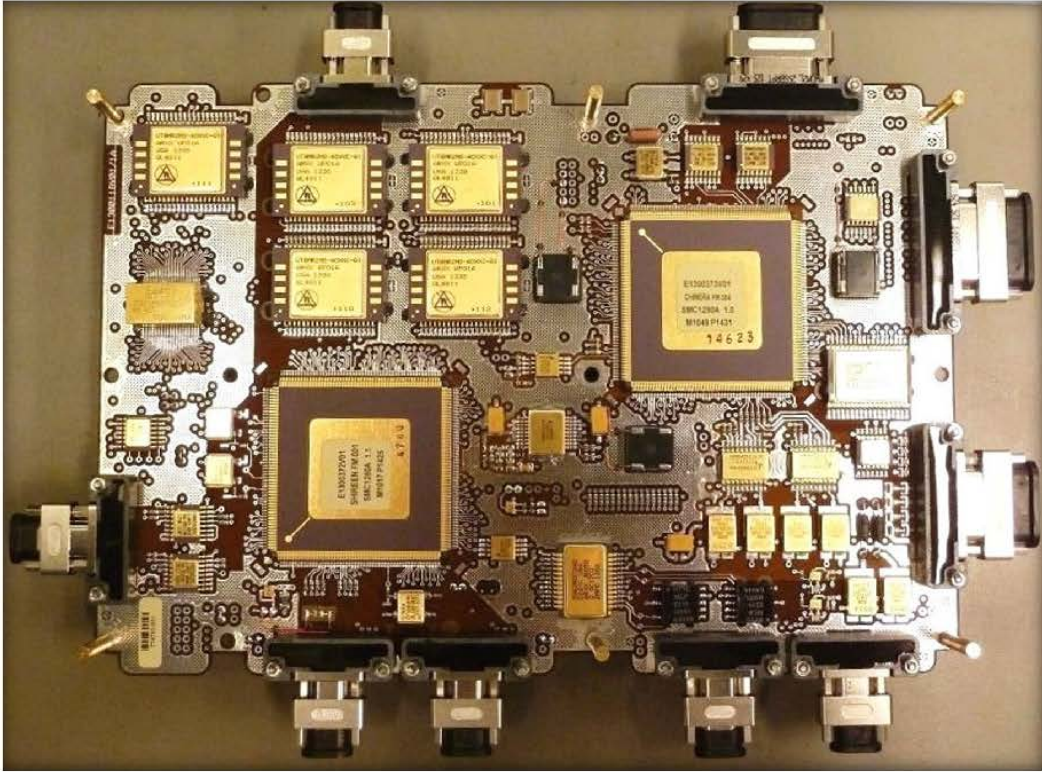


Figure 14 SINBAD PFM COM Top layer

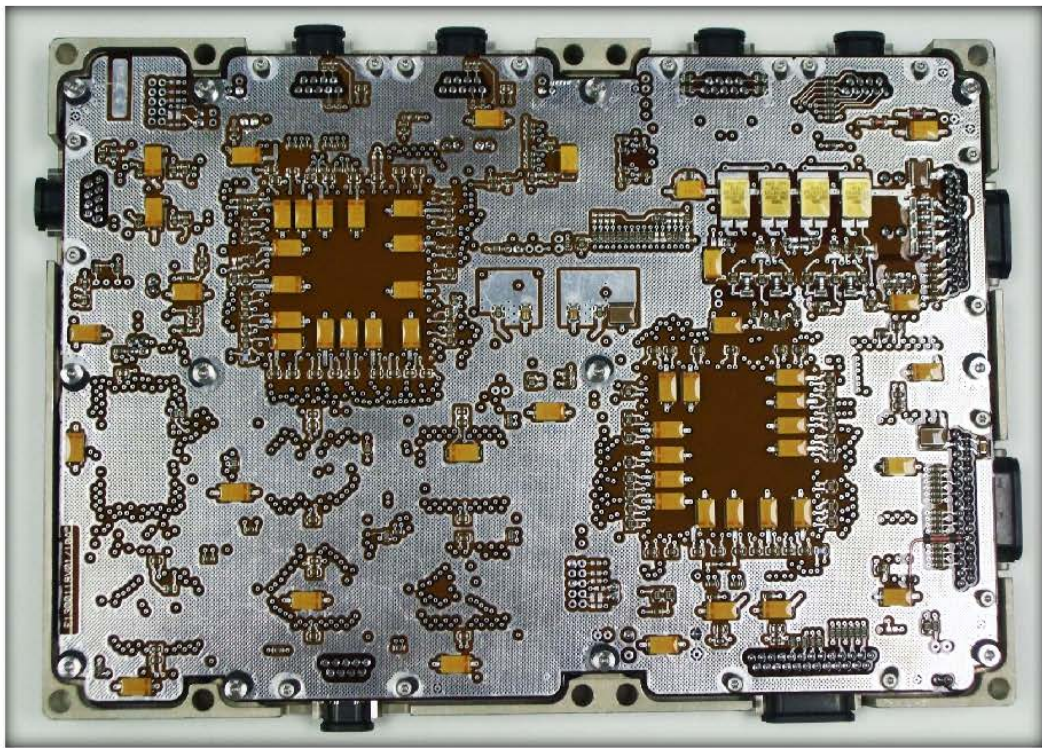


Figure 15 SINBAD PFM COM Bottom layer

SINBAD Flight Spare (FS) is the spare model and completely equal to SINBAD PFM. Both models have been validated to fly. The Test procedure and test report have been delivered with the SINBAD FS model to BIRA for the integration with Channels Spare and to ESA with the entire test of the NOMAD.

NOMAD was launched the 14th of March 2016 and the instrument was powered at the first time at 4th April 2016- The communications worked properly and the Housekeeping was received-. All telemetry values have been checked and reported nominal. The Science Data is under study of BIRA. In October TGO will reach its orbit on Mars.

ACKNOWLEDGMENTS

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The NOMAD Team: Science Team: Vandaele A.C.; Lopez-Moreno J.J.; Bellucci G.; Patel M.; Allen M.; Altieri F.; Aoki S.; Bolsée D.; Clancy T.; Cloutis E.; Daerden, F.; Depiesse C.; Fedorova A.; Formisano V.; Funke B.; Fussen D. r.; García-Comas M.; Geminale A.; Gérard J.C.; Gillotay D.; Giuranna M.; Gonzalez-Galindo F.; Ignatiev N.; Kaminski J.; Karatekin O.; Lefvre F.; López-Puertas M.; López-Valverde M.; Mahieux A.; Mason J.; Mumma M.; Neary L.; Neefs E.; Renotte E.; Robert S.; Sindoni G.; Smith M.; Thomas I.R.; Trokhimovsky S.; Vander Auwera J.; Villanueva G.; Whiteway J.; Willame Y.; Wilquet V.; Wolff M. - **Tech Team:** Alonso-Rodrigo G.; Aparicio-del Moral B.; Barzin P.; BenMoussa A.; Berkenbosch S.; Biondi D.; Bonnewijn S.; Candini G.; Clairquin R.; Cubas-Cano J.; Delanoye S.; Giordanengo B.; Gissot S.; Gómez-López J.M.; Jerónimo-Zafra J.M.; Leese M.; Maes J.; Mazy E.; Mazzoli A.; Meseguer J.; Morales-Muñoz R.; Orban A.; Pastor-Morales M.C.; Perez-Grande I.; Ristic B.; Robles-Muñoz N.; Rodríguez-Gómez J.; Saggin B.; Samain V.; Sanz-Andres A.; Sanz-Mesa R.; Simar J.-F.; Thibert T.

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