Simulations of charge transfer in Electron Multiplying Charge Coupled Devices

Journal Item

Preprint typeset in JINST style - HYPER VERSION

Simulations of Charge Transfer in Electron Multiplying Charge Coupled Devices

Nathan Bush[a]*, **Konstantin Stefanov**[a], **David Hall**[a], **Douglas Jordan**[b], **Andrew Holland**[a]

[a] *Centre for Electronic Imaging,*
The Open University, Walton Hall, Milton Keynes, MK7 6AA, UK
[b] *e2v Technologies plc,*
Waterhouse Lane, Chelmsford, Essex CM1 2QU, UK

E-mail: n.bush@open.ac.uk

ABSTRACT:
Electron Multiplying Charge Coupled Devices (EMCCDs) are a variant of traditional CCD technology well suited to applications that demand high speed operation in low light conditions. On-chip signal amplification allows the sensor to effectively suppress the noise introduced by readout electronics, permitting sub-electron read noise at MHz pixel rates. The devices have been the subject of many detailed studies concerning their operation, however there has not been a study into the transfer and multiplication process within the EMCCD gain register. Such an investigation has the potential to explain certain observed performance characteristics, as well as inform further optimisations to their operation. In this study, the results from simulation of charge transfer within an EMCCD gain register element are discussed with a specific focus on the implications for serial charge transfer efficiency (CTE). The effects of operating voltage and readout speed are explored in context with typical operating conditions. It is shown that during transfer, a small portion of signal charge may become trapped at the semiconductor-insulator interface that could act to degrade the serial CTE in certain operating conditions.

KEYWORDS: EM-CCD; Electron Multiplication; Charge Transfer Efficiency; Interface Defects; Photon-Counting.

*Corresponding author.

Contents

1. EMCCD Technology

Modern scientific imaging applications continue to demand the detection of smaller signals at faster readout speeds. With the suppression of reset noise and dark current, the dominant noise source within a CCD is due to the readout circuit, which can achieve noise of a few electrons RMS at very low readout rates rising to 10s of electrons at MHz rates [1]. The detection of very small signals can therefore only occur at slower readout speeds, and single photon detection would be impossible without the use of an external intensifier.

The Electron Multiplying Charge Coupled Device (EMCCD) is a variant of traditional CCD technology that circumvents the limitation of readout noise through utilisation of on-chip multiplication gain to increase the signal size prior to readout. An image area, serial register and output node are all present that are of conventional design (Figure 1). The main modification is the inclusion of a multiplication register; an array of elements that are each designed to allow signal carriers to experience high electric fields. The high electric fields accelerate the carriers to energies sufficient for the generation of additional electron-hole pairs from the silicon lattice in a process known as impact ionisation.

In practise this is often achieved with a 4-gate structure where two of the electrodes are customised to generate a region of high field. The barrier phase, ϕDC, is held at a low fixed voltage during operation. It acts to prevent the movement of charge when the high field is established. The high-voltage phase (ϕ2HV) can have a timed, high voltage pulse applied to establish the region of high field. The remaining two electrodes (ϕ1, ϕ3) operate at standard device potentials and act to transfer charge from one multiplication element to the next. Appropriate clocking of the gates allows the signal to be transferred from the previous element, experience multiplication, and then be passed to the following element where the process repeats (Figure 2).

The multiplication per element-to-element transfer is typically quite small (1-1.5%), however the effect of multiple consecutive elements mean that high multiplication gains can be achieved at relatively modest operating voltages. Typically there are over 500 multiplication elements on a device, and gains of $\times$1000 can be achieved with voltages for ϕ2HV in the range 40-50V.

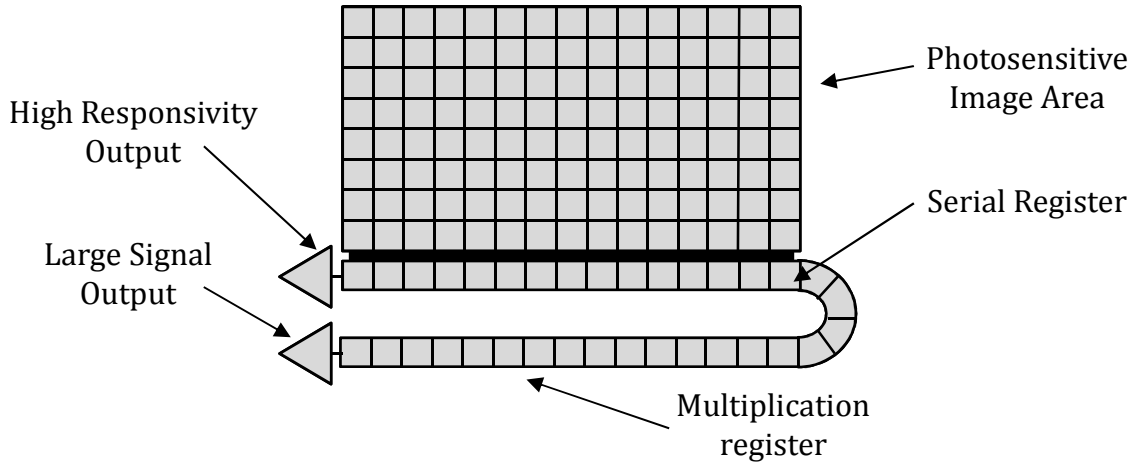

Figure 1. Schematic of an EMCCD. Commercial devices can allow two modes of operation where the device can be used as a conventional CCD or EMCCD depending on the usage scenario. Such a feature is accommodated through the use of two output gates (one for each register) and a serial register that allows "backward clocking".

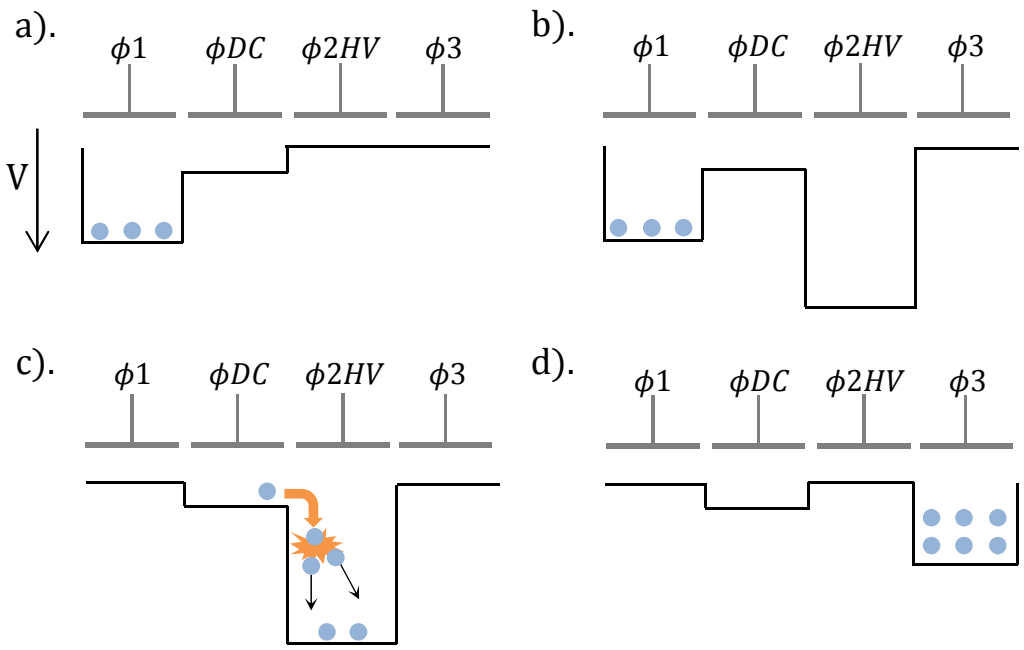

Figure 2. Example EMCCD clocking sequence. The ϕDC phase prevents the motion of charge while the high field is established (b). Impact ionisation occurs as the charge is transferred between ϕDC and ϕ2HV (c). The signal can then be transferred to the following multiplication element.

The multiplication register therefore allows a previously small signal of a few electrons to be amplified so that it is no longer lost beneath the read-noise floor of the device; improving the Signal to Noise (S/N) ratio of the camera system in low light conditions. An additional noise component is introduced, termed the Excess Noise Factor (ENF), which originates from the stochastic nature of the multiplication process. Detailed theoretical treatment in the literature [17] [25], including Monte Carlo simulations and experimental work, has shown that the ENF tends to $\sqrt{2}$ for high gain and a large number of multiplication elements. Statistical processing techniques are available that claim to successfully reduce the ENF below this value for low photon fluxes (lower than 20 photons per pixel per second) [3]. Operation in "binary mode", described in detail by Basden et al. has the ability to reduce the ENF to unity, with a corresponding reduction in Quantum Efficiency, allowing the devices to count single photons under certain conditions.

Since its introduction the technology has found a wide range of applications, including use in the military [4], biomedical imaging [5] and astronomy [6]. Many studies have also been performed concerning their operation [7] [26], radiation hardness [8] and applicability to future space instrumentation [9]. However there has not been a detailed detailed study into the process of charge transfer within the multiplication register. Such as a study has the potential to provide more information on performance characteristics, including the Charge Transfer Efficiency (CTE) of the multiplication register.

2. Simulation of an EMCCD Register Element

Device simulation gives the opportunity for the direct observation of physical processes within the device which may be the underlying cause of performance figures measured in the laboratory. To investigate the process of charge transfer within an EMCCD, a register element was constructed within commercial TCAD software [18]. All device features were chosen to be as representative of an actual device as practically possible. The aim was to accurately simulate the transfer of charge through the multiplication register in order to observe the preferred motion of charge carriers, and the regions where impact ionisation takes place. Appropriate physical models were chosen to handle the device physics, including a mobility model that has shown a wide range of applicability to MOS devices [10]. The impact ionisation process was empirically modelled through modification of a method originally proposed by Lackner [11], whereby parameters were tailored specifically for the case of EMCCDs through comparison to measured values [19]. The transfer was performed with a signal of $\approx 300e^{-}$, and the timings used for clock pulses were consistent with a device operated at 11MHz [19]. At each time-step of the simulation, device parameters were output in a format that allowed the visualisation of carrier concentration (Figure 3), current density and the regions of impact ionisation (Figure 4).

As the $\phi 1$ clock is lowered, the signal packet moves beneath the ϕDC phase and is accelerated towards the interface region before settling beneath the ϕHV phase. The region of highest field is located between ϕDC and ϕHV and is where the majority of the multiplication takes place (Figure 4). Within this region the energy gained by the carriers from the electric field between successive collisions is higher than that lost from scattering processes (which for low electric fields is dominated by acoustic phonon scattering). Beyond this point, the carriers are described as "hot" [12], since they are no longer in thermal equilibrium with the silicon lattice. Instead, their energy

is described by an effective temperature T_e, which can be modelled through a skewed Maxwell Boltzmann distribution with a high energy tail [13]. For carriers with sufficient energy, optical phonon scattering becomes the dominant energy loss mechanism and acts to saturate the velocity of the carriers, with an average speed for electrons within silicon of $\approx 10^7 cms^{-1}$. A small fraction gain energy sufficient for impact ionisation (3.6 eV), and generate additional signal through liberation of an additional electron-hole pairs from the silicon lattice [14].

The primary impact ionisation region is shown to extend close to the interface of the device, indicating that some of the carriers within this region are still of high energy ($\geq$ 3.6 eV). This, coupled with the fact the peak field is located directly at the surface, means it is likely some carriers come into contact with the interface or are even injected into the gate stack, where they may possibly become trapped.

A second region of impact ionisation is also seen directly beneath the ϕDC phase; it does not extend deep within the device. The region of primary impact ionisation is a source of holes as well as electrons, which experience a field similar in magnitude to the electrons yet are accelerated in the opposite direction. The ϕDC phase is the region of least positive potential in the near vicinity, and so the holes are accelerated towards the interface beneath ϕDC where they also become ”hot”, forming a second region of impact ionisation. The threshold energy for impact ionisation due to holes in higher than that of electrons (5.0 eV compared to 3.6 eV), meaning this is another region where carriers may have sufficient energy to interact with interface states.

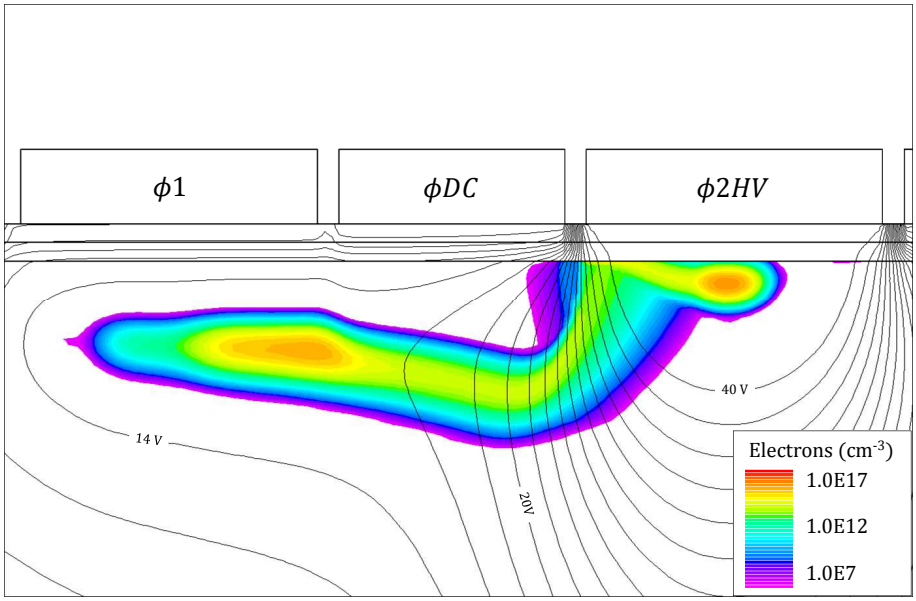

Figure 3. Electron concentration at a point during transfer with $\phi 2HV = 40$ V. Potential contour lines are illustrated at 2V/contour.

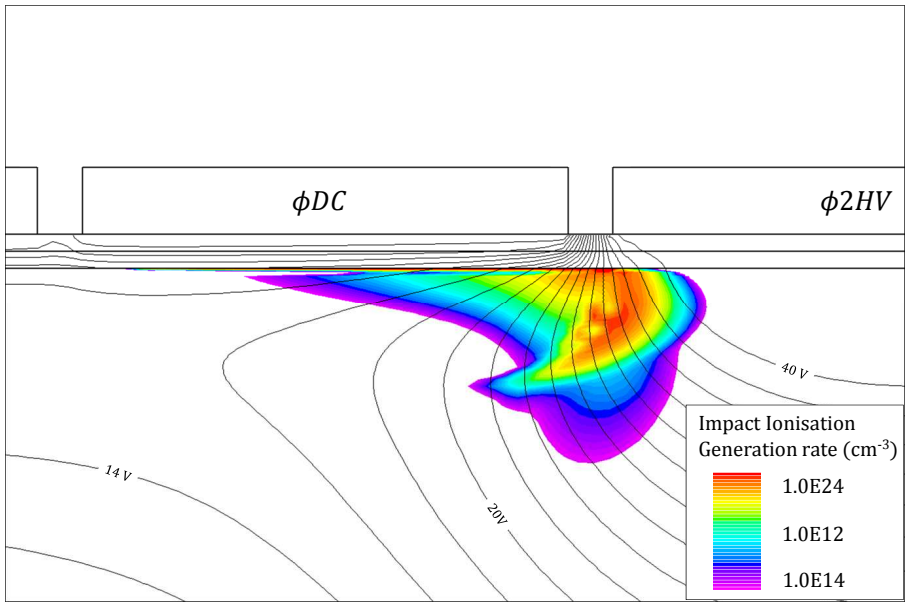

Figure 4. Regions of impact ionisation at the same point during transfer as Figure 3. Two regions of Impact ionisation are present, one between ϕDC and ϕ2HV, and another thin region directly beneath the ϕ DC phase.

3. Carrier Trapping at the Si-SiO$_2$ Interface

The atomic mismatch between silicon and its oxide means that the interface between the two materials contains defects which can act as trapping centres for charge carriers. In CCD technology these sites are avoided through the inclusion of the buried channel structure, which means the sig-

nal charge does not encounter surface states during transfer. However the path of the charge within the EMCCD gain register shows that these sites may be encountered by a small fraction of the signal. Whether this observation could be considered problematic depends on the exact amount of charge that becomes trapped and the time-scales during which it is released. If any signal charge is released when the original charge packet has moved on this would manifest as a decrease in the CTE of the serial register. Simulation of charge transfer with accurate representation of the most common defects present at the interface will help highlight the relative importance of the effect if it exists.

The dominant trapping centres for MOS devices fabricated on <100> silicon using processes for CCD manufacture are P_{b0} and P_{b1} centres [15]. Each trapping centre is amphoteric, meaning each defect has both a donor and acceptor state within the silicon band gap. The P_{b0} centre is well understood, and is believed to consist of a silicon dangling bond defect back bonded onto three other silicon atoms [20]. Many sources claim that the donor and acceptor peaks have correlation energy of approximately 0.6-0.7 eV, and agree that the donor and acceptor energy levels are placed $\approx$0.2 eV and $\approx$0.8 eV from the valence band respectively [15] [23] . The Density of States (DOS) has been shown in many sources to be approximately Gaussian [22] [23]. Grasser et al. [24] report values for a standard deviation of the P_{b0} distribution of a sample which are used for the DOS in this study. The acceptor peak is slightly narrower than the donor peak and has a higher peak DOS.

The exact nature and behaviour of the P_{b1} center has been the subject of much discussion in the literature[21]. Gerardi et al concluded that the P_{b1} center has smaller correlation energy than previously thought, which is estimated to be approximately 0.3-0.4 eV. Lenahon et al state that the mean energy is shifted below the silicon band gap by approximately 0.2 eV. The donor and acceptor energies for the P_{b1} center used for this investigation were 0.26 and 0.56 eV from the valence band respectively, based on the donor energy from the literature [15] and the correlation energy estimated by Gerardi et al. Capture cross sections for the traps were taken from the literature [15], the most notable are the acceptor state cross sections which are $\sigma_{Pb0} = 5 \times 10^{-15} cm^{-2}$ and $\sigma_{Pb1} = 5 \times 10^{-16} cm^{-2}$ for the P_{b0} and P_{b1} states respectively.

The total number of interface defects depends upon many factors including manufacture conditions and device history. The peak DOS was chosen to be $D_{it} = 1 \times 10^{10} cm^{-2} eV^{-1}$ for both P_{b0} and P_{b1} centres. This is believed to be an appropriate value for this type of device to within an order of magnitude. The ratios of acceptor and donor states for P_{b0} centres was chosen to be ≈ 0.6, based on the semi-quantitative approximation shown by Lenahon et al, and experimental results from Grasser et al. It should be noted that the DOS and cross sections for each trapping center are subject to large uncertainty, as literature values can commonly differ by at least an order of magnitude, however the values chosen are believed to be appropriate based on current knowledge.

To investigate whether the existence of defects could have any effect on the CTE of the multiplication register, transfers were performed at various ϕ2HV voltages and the amount of signal charge that became trapped in the acceptor states was measured. Transfers were also performed at different operating temperatures, since EMCCDs are typically cooled during operation which would have implications for behaviour of the trapping centres and hence the total amount of trapped charge.

After a single transfer it can be seen that there are two distinct regions where charge becomes trapped at the interface (Figure 6.0). Between the ϕDC and ϕ2HV phases, a small region exists

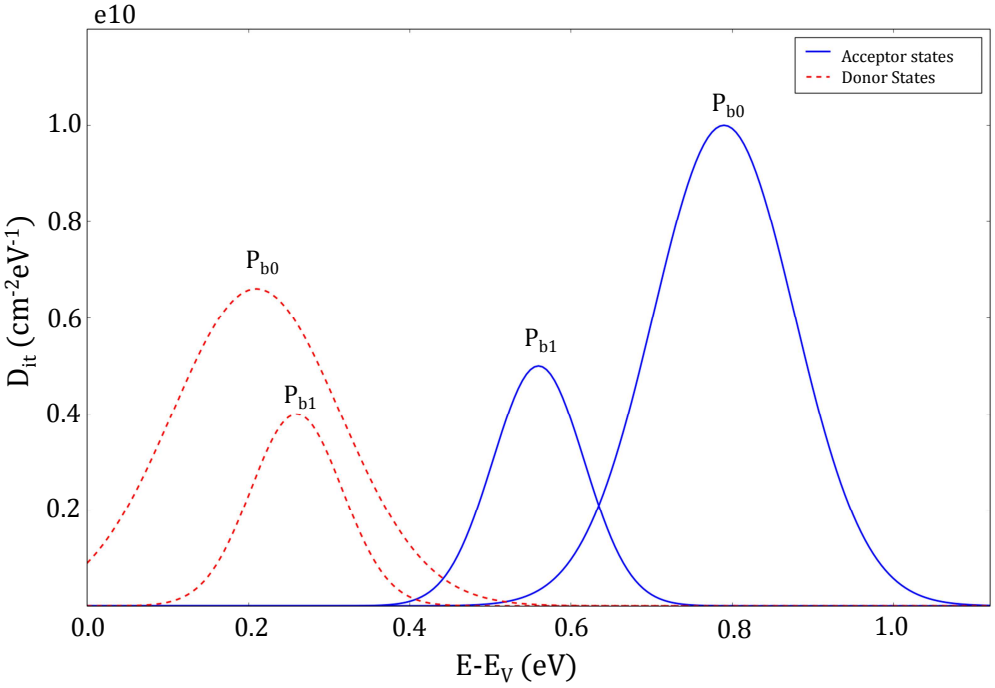

Figure 5. DOS used for the P_{b0} and P_{b1} centres.

where charge has become trapped due to contact with the interface during transfer (region 1). Beneath the ϕ2HV phase, another region of trapped charge exists due to the charge storage location of ϕ2HV being close to the interface (region 2).

The relative importance of each trapping region appears to change with respect to ϕ2HV voltage and temperature. Figures 7 a) shows an example of the measured charge within in region for various ϕ2HV voltages at 293K. In this example, the trapped charge in region 1 forms the majority until approximately ϕ2HV $\geq$ 46 V, at which point the trapped charge increases abruptly due to the signal storage location becoming close to the interface. As the operating temperature is decreased, the total trapped charge (region 1 + 2) is shown to decrease with operating temperature (Figure 7b) for allϕ2HV voltages. Although as the temperature is decreased, the charge trapped in region 2 becomes dominant at increasingly large voltages.

A decrease in temperature acts to reduce the charge storage packet volume for a given signal level, with the degree of reduction dependant on the magnitude of the signal. This is attributed to a reduction in the component of motion due to thermal diffusion. A decrease in temperature would also act to increase the mean free path of the carriers as they are transferred from ϕ1 to ϕ2HV, potentially increasing the charge trapped within region 1 as the temperature decreases. This was observed to be the case for sufficiently high ϕ2HV voltages, however beyond a certain point the trapped charge began to decrease one again (Figure 7c shows an example for ϕ2HV=46V). The exact reason for this is unclear and investigations into the preferred motion of charge at lower temperatures and the trapped charge as a function of acceptor trap energy may shed more light on the observation. Since the majority of trapped charge occurs within region 2 at these ϕ2HV

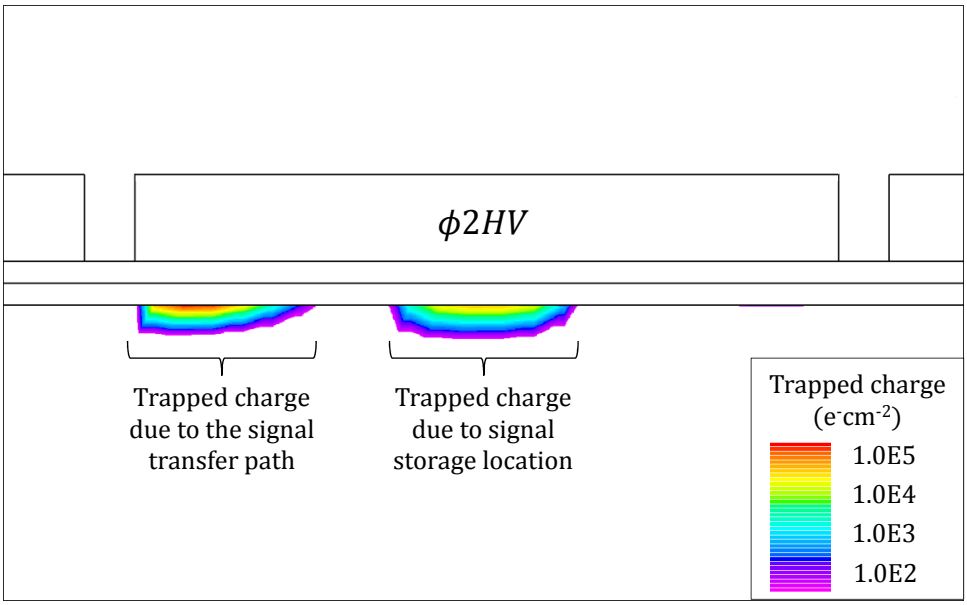

Figure 6. Illustration of the two distinct regions of trapped charge following a transfer at ϕ2HV=40 V. Some charge becomes trapped due to the transfer path of the signal, referred to as region 1. Region 2 is the trapped charge due to the storage location of the signal beneath ϕ2HV.

voltages, the increase does not contribute significantly to the total trapped charge.

The results shown used clock timings consistent with 11MHz operation, if the readout speed is increased then the time the signal packet spends beneath ϕ2HV will also decrease proportionally, reducing the trapped charge within region 2. It is conceivable that at suitably high pixel rates, the total trapped signal can therefore be reduced, and region 1 will become the dominant trapping location. Simulations with timings consistent with operating at higher frame rates could possibly confirm this.

The clear trends are that the fraction of trapped charge can be minimised through operation at lower temperatures and at as low a ϕ2HV voltage as possible while still achieving the desired multiplication gain. Operation at faster pixel rates may also reduce the trapped charge further, however it should be noted that these variables also affect other noise sources (such as clock induced charge) which may also need to be considered.

4. Implications for Charge Transfer Efficiency

Operation at high $\phi 2HV$ voltages and higher temperatures has been shown to give rise to a larger portion of trapped charge following a single transfer, however the link to CTE has yet to be established. If the majority of the trapped charge is released before the signal packet is transferred onwards, the implications for CTE would be small, however if it is released at later times it will also travel through the multiplication register and be registered as signal.

To establish the possible effect of the trapped charge on CTE, simulations were performed with the aim of estimating the time when the trapped charge is most likely to be released. This

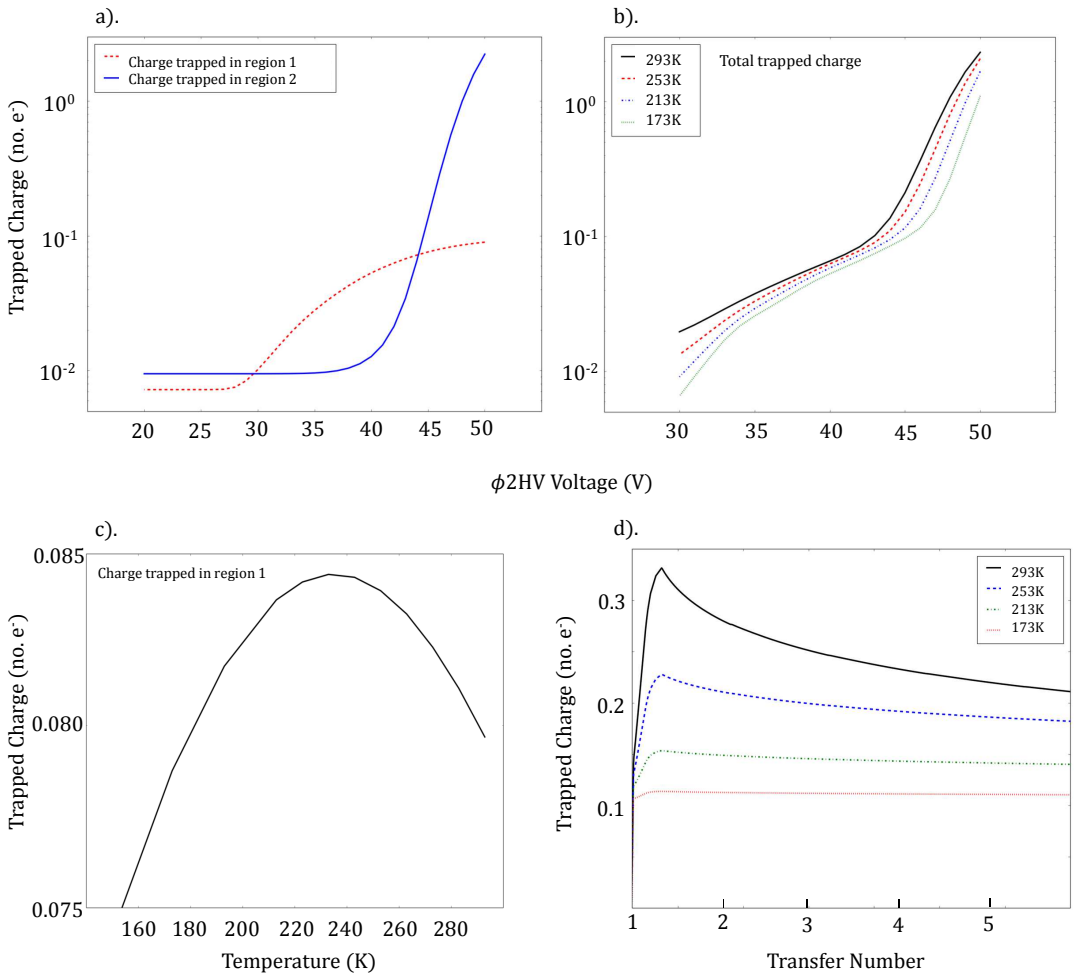

Figure 7. a). Measured trapped charge within each region in figure 7 as a function of ϕ2HV voltages at T=293 K. b). Total trapped charge (region 1 + 2) as a function of ϕ2HV voltage and operating temperature. c). trapped charge in region 1 as a function of temperature for ϕ2HV = 46 V. d). The total population of traps (region 1 + 2) over multiple transfers at different temperatures for ϕ2HV=46 V.

was achieved through populating the traps through simulation of charge transfer in the register, transferring the signal packet onwards out of the register and then repeatedly clocking the device with no signal present while observing how the population of traps changed. This method was designed to replicate the process of single photon detection, where a large signal which has already undergone some degree of multiplication will be passed through the register, followed by many transfers with no signal. The process was repeated for a variety of temperatures (Figure 7 d).

As the operating temperature decreases there are a larger fraction of traps that remain populated when the original signal packet has been transferred onwards, however the total number is

still seen to decrease with temperature, implying that a decrease in temperature could correspond to an increase in the serial CTE of the gain register.

5. Conclusion

Simulation of an EMCCD register element has showed the motion of charge and primary regions of impact ionisation within the device. When operated at high gain, the potential distribution within the device is such that a fraction of the signal charge comes into contact with the gate dielectric, populating acceptor-like traps. The total trapped charge remains small; however it has the possibility to degrade the CTE of the device if operated at high gain in low flux conditions. The fraction of trapped charge can be minimised through operation at lower temperatures and by operating the device at as low a ϕ2HV voltage as possible while still achieving the desired multiplication gain.

References

[1] Paul Jerram ; Peter J. Pool ; Ray Bell ; David J. Burt ; Steve Bowring ; Simon Spencer ; Mike Hazelwood ; Ian Moody ; Neil Catlett ; Philip S. Heyes; *The LLCCD: low-light imaging without the need for an intensifier. Proc. SPIE 4306, Sensors and Camera Systems for Scientific, Industrial, and Digital Photography Applications II*, **178** (May 15, 2001); *doi:10.1117/12.426953*

[2] Craig D. Mackay ; Robert N. Tubbs ; Ray Bell ; David J. Burt ; Paul Jerram ; Ian Moody; *Subelectron read noise at MHz pixel rates. Proc. SPIE 4306, Sensors and Camera Systems for Scientific, Industrial, and Digital Photography Applications II*, **289** (May 15, 2001); *doi:10.1117/12.426988*

[3] Basden, A. G; Haniff, C. A. and Mackay, C. D., *Photon counting strategies with low-light-level CCDs*, *Monthly Notices of the Royal Astronomical Society* **345**, *p985–991*, 2001, *doi: 10.1046/j.1365-8711.2003.07020.x*

[4] G.B. Heim, J. Burkepile and W.W. Frame, *Low-light-level EMCCD color camera*, *Proc SPIE 6209, Airborne Intelligence, Surveillance, Reconnaissance (ISR) Systems and Applications III*, 2010, *eid: 774202*

[5] Teo, B.K.; Shestakova, I; Sun, M.; Barber, W.C.; Hasegawa, B.H.; Nagarkar, V.V., *Evaluation of a EMCCD detector for emission-transmission computed tomography*, *IEEE Nuclear Science Symposium Conference Record*, vol.5, pp.3050,3054, 23-29, 2005, *doi: 10.1109/NSSMIC.2005.1596973*

[6] Mackay, C.; Staley T. D; King, D.;Suess, F. and Weller, K., *High-speed, photon-counting CCD cameras for astronomy*, *Society of Photo-Optical Instrumentation Engineers (SPIE) Conference Series*, **7742**, 774202 *doi: 10.1117/12.855282*

[7] Donal J. Denvir ; Emer Conroy; *Electron-multiplying CCD: the new ICCD. Proc. SPIE 4796, Low-Light-Level and Real-Time Imaging Systems, Components, and Applications*, **164** (February 6, 2003); *doi:10.1117/12.457779*

[8] Smith, D.R.; Ingley, R,; Holland, A.D; *Proton irradiation of EMCCDs IEEE transactions on Electron Devices* **53** (February 2006) *doi: 11.1109/TED.2005.861730*

[9] Djazovski, O.; Diagle, O.; Laurin, D.; Bedirian, M.; Ducharme, M.; Artigau, E.; Doyon R; *Electron Multiplying CCDs for future space instruments SPIE Proceedings on Photons North 2013* **8915** October 2013, *doi: 10.1117/12.2036206*

[10] Lombardi, C.; Manzini, S.; Saporito, A; Vanzi, M., *A physically based mobility model for numerical simulation of nonplanar devices*, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **7** pp.1164,1171, Nov 1988 *doi: 10.1109/43.9186*

[11] T. Lackner; *Avalanche Multiplication in semiconductors: A modification of Chynoweth's Law*, /emphSolid State Electronics, **34** pp. 33-42, 1991. *doi: 10.1016/0038-1101(91)90197-7*

[12] H. FrÃűhlich and B V Paranjape; *Dielectric Breakdown in Solids*, *Proceedings of the Physical Society. Section B*, **69**, pp 21, 1956 *doi:10.1088/0370-1301/69/1/304*

[13] A. Concannon; F. Piccinini; A. Mathewson; C. Lombardi; *The numerical simulation of substrate and gate currents in MOS and EPROMs*, *IEEE Electron Devices Meeting*, pp. 289-292, December 1995, *doi: 10.1109/IEDM.1995.499198*

[14] S. Sze; *Semiconductor Devices: Physics and Terminology*, John Wiley & Sons, 1985, *ISBN 10: 0470873671*

[15] H. S. Nalwa; *Handbook of surfaces and interfaces of materials*, Acaemic Press, 2001.

[16] Daigle, O.; Carignan, C.; Gach, J.-L.; Guillaume, C.; Lessard, S; Fortin, C.-A;Blais-Ouellette, S.; *Extreme Faint Flux Imaging with an EMCCD*, *Publications of the Astronomical Society of the Pacific*, August 2009, **121**, pp. 866-884, *doi:10.1086/605449*

[17] M., S. Robbins and B., J., Hadwen, *The Noise Performance of Electron Multiplying Charge-Coupled Devices*, *IEEE Transactions On Electron Devices* **50** 5 (2003) 1227-1232

[18] SILVACO Inc., *ATLAS User's Manual (2012)*

[19] e2v CCD97 data-sheet, A1A-CCD97BI_2P_IMO, Issue 3 e2v CCD97 data-sheet, A1A-CCD97BI_2P_IMO, Issue 3

[20] C., R. Helms; E., H. Poindexter, *The silicon-silicon dioxide system: Its microstructure and imperfections*, *Reports on Progress in Physics* **57** 8 (1994) *doi:10.1088/0034-4885/57/8/002*

[21] Campbell, J. P. and Lenahan, P. M. *Density of states of Pb_1Si/SiO_2 interface trap centers*, *Applied Physics Letters*, **80** pp1945-1947, *doi: 10.1063/1.1461053*

[22] P., M. Lenahan; T., D. Mishima; J., Jumper; T., N. Fogarty; R., T. Wilkins *Direct Experimental evidence for atomic scale structural changes involved in the interface-trap transformation process*, *IEEE Transactions on Nuclear Science*, **48** (2001) *doi: 10.1109/23.983184*

[23] Campbell, J.P. ; Lenahan, P.M. ; Krishnan, A.T. ; Krishnan, S. *Observations of NBTI-induced atomic scale defects IEEE international integrated reliability workshop final report* (2005) *doi: 10.1109/IRWS.2005.1609551*

[24] Grasser, T.; Kaczer, B.; *Negative bias temperature instability:Recoverable versus permanent degradation IEEE Solid State Research Conference* (2007) pp.127-130, *doi: 10.1109/ESSDERC.2007.4430895*

[25] J. H. Tutt, D. J. Hall, R. D. Harriss, A. D. Holland, N. J. Murray, *The Noise Performance of Electron Multiplying Charge-Coupled Devices at X-rays energies*, *IEEE Transactions on Electron Devices* **59** pp. 167-175 (2012) *doi: 10.1109/TED.2011.2172611*

[26] J. H. Tutt ; D. J. Hall ; A.D. Holland ; N. J. Murray ; J. Endicott; *Developing a high-resolution x-ray imager using electron-multiplying (EM) CCDs*; *Proc. SPIE 8852, Hard X-Ray, Gamma-Ray, and Neutron Detector Physics XV*, **885217** (September 26, 2013); *doi:10.1117/12.2023317*.