Performance of buried channel n-type MOSFETs in 0.18-m CMOS image sensor process

Conference or Workshop Item

Performance of buried channel *n*-type MOSFETs in 0.18-µm CMOS image sensor process

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ABSTRACT

Buried channel (BC) MOSFETs are known to have better noise performance than surface channel (SC) MOSFETs when used as source followers in modern Charge Coupled Devices (CCD). CMOS image sensors find increasing range of applications and compete with CCDs in high performance imaging, however BC transistors are rarely used in CMOS. As a part of the development of charge storage using BC CCDs in CMOS, we designed and manufactured deep depletion BC *n*-type MOSFETs in 0.18 µm CMOS image sensor process. The transistors are designed in a way similar to the source followers in a typical BC CCD. In this paper we report the results from their characterization and compare with enhancement mode and "zero-threshold" SC devices. In addition to the detailed current-voltage and noise measurements, semiconductor device simulation results are presented to illustrate and understand the different conditions affecting the channel conduction and the noise performance of the BC transistors at low operating voltages. We show that the biasing of the BC transistors has to be carefully adjusted for optimal operation, and that their noise performance at the right operating conditions can be superior to SC devices, despite their lower gain as in-pixel source followers.

Keywords: Buried Channel MOSFET, CMOS image sensors, Semiconductor Device Noise

1. INTRODUCTION

Buried Channel (BC) MOSFETs are routinely used as source followers in high performance Charge Coupled Devices (CCDs)[1] due to the reduced *1/f* noise compared to surface channel (SC) MOSFETs to help achieve noise levels measured in single electrons equivalent noise charge (ENC). In contrast, in the vast majority of CMOS Image Sensors (CIS) the source follower transistors are surface channel type, with only a few examples of buried channel MOSFET development. CIS are increasingly competing with CCDs in high performance scientific applications where low readout noise is of primary importance, and particular attention is being paid to the first transistor stage – the in-pixel source follower.

It is widely accepted that the noise performance of CIS is fundamentally limited by Random Telegraph Signal (RTS) and *1/f* transistor noise and significant advances have been made worldwide in reducing both noise components. In surface channel transistors the current flows in a thin layer in direct contact with the Si-SiO_2 interface and charge carriers can interact with the interface and generate RTS and *1/f* noise. In contrast, in BC transistors the drain current can flow at significant depth below the interface and can in principle completely avoid any interaction with it. This is achieved in the BC source followers in modern CCDs, where the potential barrier between the channel and the Si-SiO_2 interface can reach many volts. The transistors are categorized as "deep depletion" type and the large potential barrier is made possible by the high supply voltages available in CCDs, where the drain bias can easily exceed 25V.

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Although the noise performance of state-of-the-art SC transistors in CIS is considered satisfactory for many applications, a question remains whether further improvements in the RTS and *1/f* noise could be achieved by using BC devices, in particular for high performance scientific sensors. Recent efforts to develop BC MOSFETs[2] suggest that this is indeed possible, and a dedicated development for CIS[3] appears promising.

In this work we report the results from the fabrication and the evaluation of deep-depleted *n*-type BC MOSFETs for application in CIS. The transistors were designed as a part of the development of the second generation In-situ Storage Image Sensor (ISIS2)[4], which used linear BC CCD registers per pixel to achieve local charge storage and high burst rate readout. The experimental data is compared to two different SC devices manufactured on the same process and complemented by semiconductor device simulations.

2. OPERATION OF THE BC MOSFET

The BC transistor, also known as depletion mode MOSFET, is typically a normally-on device finding applications in analog circuits. The BC MOSFET is created by defining a conductive channel under the gate of a SC device by ion implantation of the same type of impurities used for the definition of the source and the drain, as shown in Figure 1. In the BC MOSFET the drain current is controlled by modulation of the cross section of the conducting channel, achieved by varying the depletion depth between the gate and the channel, and between the channel and the substrate[5]. The operation of the BC MOSFET is somewhat more complex than the SC equivalent due to the possibility of three distinct conditions at the Si-SiO_2 interface affecting the drain current and the noise performance – depletion, accumulation and inversion[6]. For simplicity, the following description refers to *n*-channel devices only.

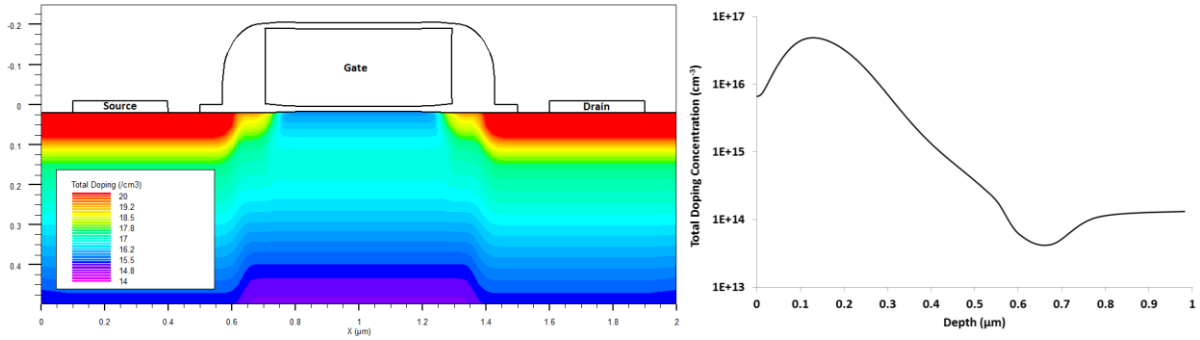

Figure 1. A cross section of the BC transistor showing the doping concentration in 2D (left), and doping profile in depth under the gate center (right). All dimensions are in micrometers.

In BC transistors the drain current flow is separated from the Si-SiO_2 interface by a potential barrier, created by the difference between the peak channel potential and the interface potential. In general, lower *1/f* noise can be achieved due to the much reduced carrier interaction with the Si-SiO_2 interface. Another advantage is the increased carrier mobility, because carriers flow through semiconductor with nearly bulk properties. Typically bulk mobility is a factor of two higher than the surface mobility[7,8], which is favorable for achieving higher gate transconductance g_m and lower thermal noise than SC devices. However, the additional separation between the gate and the channel reduces the effective gate capacitance C_{ox}, which goes against the effects from the increased carrier mobility. The performance of a given BC transistor will depend on the channel doping profile, oxide thickness and bias conditions, and can be predicted by modern semiconductor device simulation tools.

The normal operating mode is in depletion – this occurs when the conducting channel is contained from both sides between two space-charge regions: one created by the MOS capacitor including the gate, and the other formed by the reverse-biased *p-n* junction created by the channel implant and the substrate. The potential barrier between the channel and the gate can be many times the thermal potential and can substantially reduce the interactions of the charge carriers with the interface.

As the gate voltage is increased, the channel is brought towards the Si-SiO_2 interface until the potential barrier disappears, majority carriers begin to accumulate at the surface and the channel conductivity starts to increase. In this mode a part or the whole of the channel could be in accumulation, resulting in current flow at the Si-SiO_2 interface and increased *1/f* noise[7].

If the gate is biased sufficiently negative with respect to the substrate, an inversion layer under the gate begins to appear. As the gate bias becomes more negative, the expanding inversion layer begins to shield the channel from further changes of the gate potential, leading to a marked decrease in the gate transconductance g_m and increased generation-recombination noise[7-10]. For optimal noise performance BC transistors should be operated with the interface in depletion, avoiding either accumulation or inversion under the gate. In this study the operating mode of the BC transistors was monitored by measurements of the gate transconductance and the circuit gain in a source follower configuration.

3. TEST DEVICES

A number of BC CCD test devices were manufactured by TowerJazz Semiconductor (Newport Beach, CA, USA) using customized 0.18 μm dual gate (1.8V/5V) CMOS process on 100 Ω.cm epitaxial wafers. In order to increase the available voltage and the signal dynamic range, the CCDs and the transistors were made using the thicker gate oxide (approximately 12 nm) and rated at 5V. An *n*-type BC implant was designed to achieve peak CCD channel potential of approximately 3V at zero gate voltage. To ensure good charge transfer with non-overlapping polysilicon gates, the BC implant was positioned relatively deep into the epitaxial layer with doping profile shown in Figure 1. Two variants of the CCD structures were included on each chip: one with BC reset transistor, physically part of the CCD channel, and another one with SC reset transistor, placed outside the CCD channel. The CCD and BC transistors were built directly into the epitaxial layer, without the use of a *p*-well. The performance of the BC CCD is described elsewhere[4].

The same BC implant was used to make a number of test transistors for detailed evaluation of their parameters. Typically in CCDs the BC source followers are made with the same implant used for the main buried channel in order to reduce the number of manufacturing steps, and the same approach was followed here. Each test structure consists of three transistors connected in a pixel source follower configuration, as shown in Figure 2. In this way, the test structure allows the evaluation of three distinct transistor types with markedly different conditions for interaction of the current carriers with the Si-SiO_2 interface. This arrangement gives full access to M0, and allows M1A to be evaluated when the transistor M1B is switched on by connecting RSEL to OD. In each test structure the transistor M0 is either a deep depletion BC type made using the implant profile in Figure 1, or a "zero threshold" (Zero V_t) type, offered by TowerJazz Semiconductor as a *n*-type SC MOSFET with large threshold adjustment. The Zero V_t transistor requires a small negative gate-source voltage to be turned off completely, and in terms of device characteristics should be somewhere in between the deep depletion and the enhancement mode transistors. The transistors M1A and M1B are normal enhancement mode *n*-type SC MOSFETs with threshold of 0.65V.

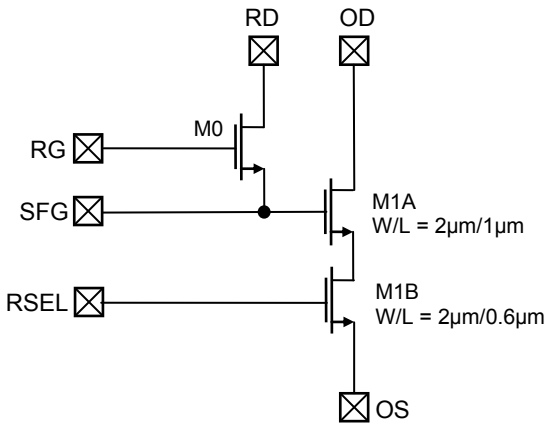

Figure 2. Schematic of the transistor test structure. The device M0 is either (a) BC transistor with W/L = 1.6μm/0.6μm; or (b) Zero V_t type with W/L = 0.6μm/1.2μm. The transistor M1A is SC type with W/L = 2μm/1μm and threshold V_t = 0.65V. The gate protection circuitry between each pad and the substrate is not shown.

Using the ATHENA and the ATLAS software from Silvaco Inc. the behavior of the BC transistor was simulated in 2D in order to establish several critical parameters, including the depth profile of the drain current and the bias range for

optimal operation. The implant profile used in the simulation, shown in Figure 1, was derived from the doses and energies for the ion implantation and from the annealing schedule.

Figure 3 shows the distribution of the drain current in the transistor channel, simulated by ATLAS, for the normal operation mode of the transistor when there is no inversion or accumulation under the gate. For most of their path the electrons travel approximately 150 nm below the Si-SiO_2 interface, only coming in close contact with the surface near the source and the drain regions. From this the expectation is that in the *n*-type BC transistor there should be less interaction between the electron current and the interface, leading to improved noise performance. In the following section we test the validity of this statement by presenting, comparing and discussing the current-voltage and noise measurements of the three types of transistors.

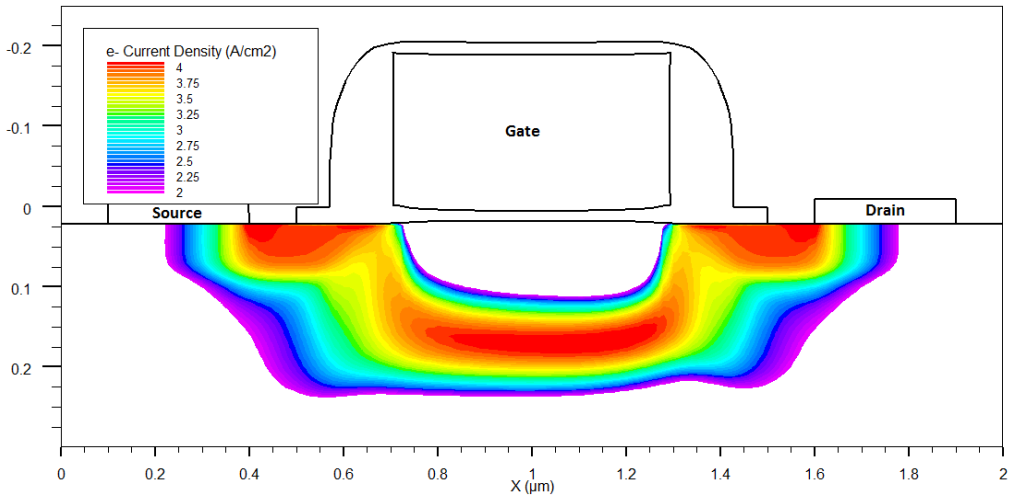

Figure 3. Simulated electron current density in a BC MOSFET at drain current I_D = 11.5 µA, gate-source voltage V_{GS} = -1.25 V, drain voltage V_D = 5 V and substrate V_{SUB} = 0 V. The density levels are on logarithmic scale, with the highest level 10^4 A/cm^2 and the lowest 10^2 A/cm^2. All dimensions are in micrometers.

4. RESULTS AND DISCUSSION

4.1 Experimental setup

For all transistors the input and the output current-voltage (I-V) characteristics were obtained using a pair of Keithley model 2400 source meters. Transistor noise was measured in a source follower configuration with adjustable gate voltage for control of the drain current, as shown in Figure 4. Particular attention was paid to minimizing the parasitic capacitance applied to the source of the device under test (DUT) in order to increase the measurement bandwidth. The low noise amplifier (LNA) was selected to have both low input-referred noise and low input capacitance and placed in the same shielded enclosure as the DUT, thus avoiding the use of a coaxial cable for the connection and minimizing the load capacitance. The LNA was built using the JFET-input ADA4817-1 operational amplifier with datasheet input capacitance of 1.3 pF and input-referred voltage noise density of 4 $nV/\sqrt{Hz}$ above 50 kHz.

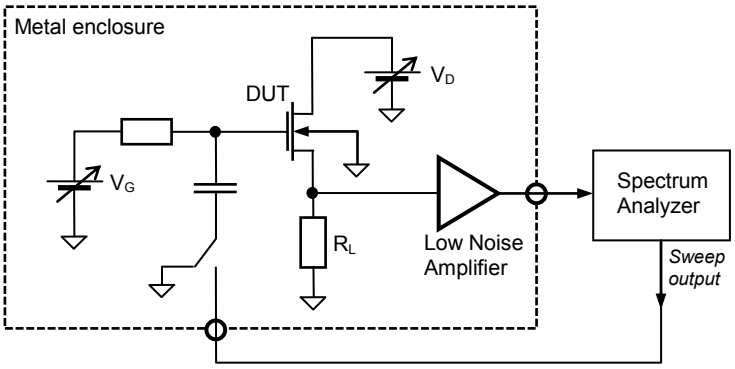

Figure 4. Experimental setup for the noise measurements. The drain current is measured in the V_D supply line.

The noise density spectrum was measured in the range from 100 Hz to 5 MHz for different drain currents using a HP3585A spectrum analyzer. The experimental setup was calibrated by measurements of the white noise of known metal film resistors. The system bandwidth of the source follower circuit was measured for each operating condition using the sweep frequency output from the spectrum analyzer as an AC component added to the gate voltage V_G, and the noise spectrum was corrected accordingly to obtain the input-referred value.

4.2 Output I-V characteristics

Figure 5 shows the measured output I-V characteristics of a BC transistor together with the simulated values using ATLAS, demonstrating good agreement. The deep depleted BC transistor is a normally-on device and requires that the gate is biased negative with respect to the source in order to turn it off. When the source is at substrate potential the gate protection structures do not allow the gate voltage to be lowered below the source voltage, so instead the source was biased positive with respect to the substrate and the gate voltage was varied between the substrate and the drain potentials.

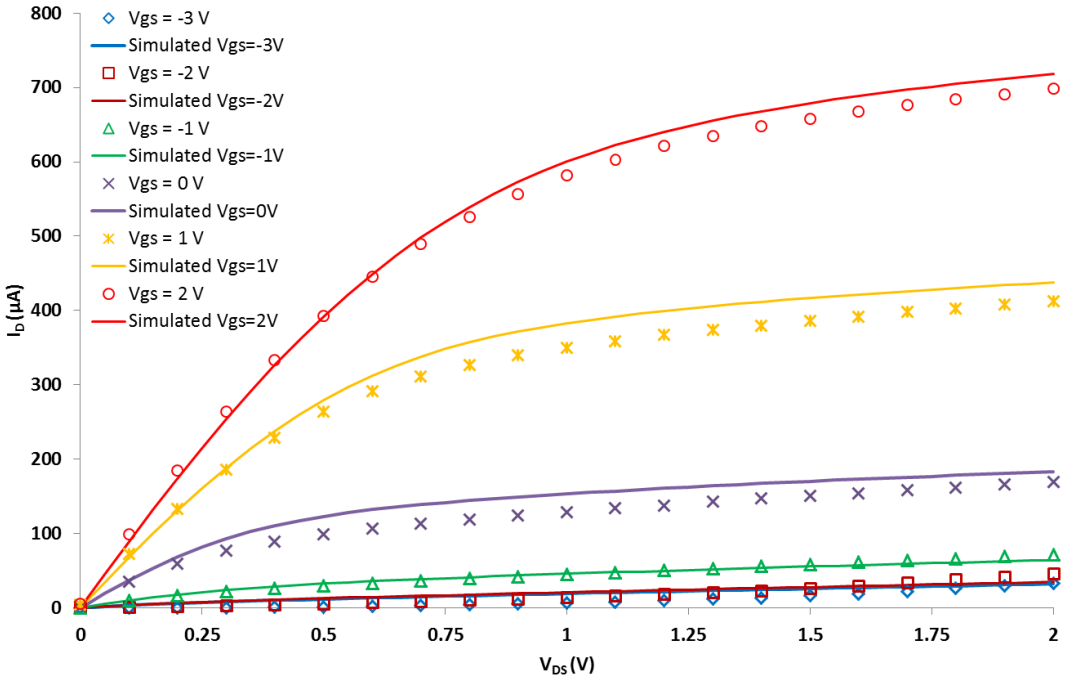

Figure 5. Measured (symbols) and simulated using ATLAS (lines) output I-V characteristics of a BC transistor with the source biased at $V_S = 3V$.

4.3 Input I-V characteristics

The measured DC gate transconductance g_m as a function of the gate-source voltage V_{GS} of the three transistors is shown in Figure 6 and clearly illustrates the differences between the device types. From the low g_m at $V_{GS} < -2V$ we can conclude that an inversion layer starts to form under the gate of the BC transistor. It screens the buried channel from further changes in the gate voltage and leads to a decrease of the gate transconductance. For $V_{GS} > -1$ V the channel approaches accumulation mode and the electron current begins to flow at or near the Si-SiO_2 interface, accompanied with an increase of g_m similar to SC devices. For $-2V < V_{GS} < -1V$ the region between the gate and the buried channel is depleted and the transistor operates in normal depleted mode. The corresponding potential profiles for the BC transistor at different gate-source voltages, simulated using ATLAS, are shown in Figure 7.

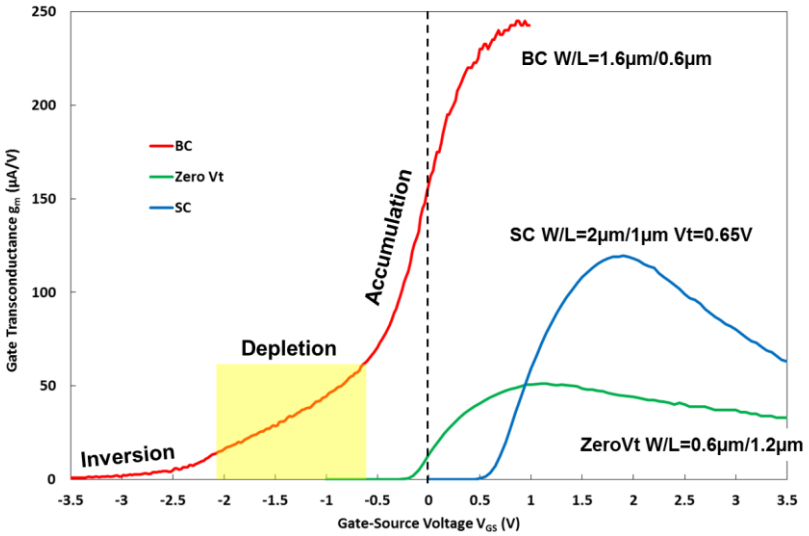

Figure 6. DC gate transconductance for the three transistors, measured at drain-source voltage V_{DS} = 1 V. The sources of the transistors were biased at V_S = 4 V for the BC, V_S = 1 V for the Zero Vt, and V_S = 0 V for the SC, respectively.

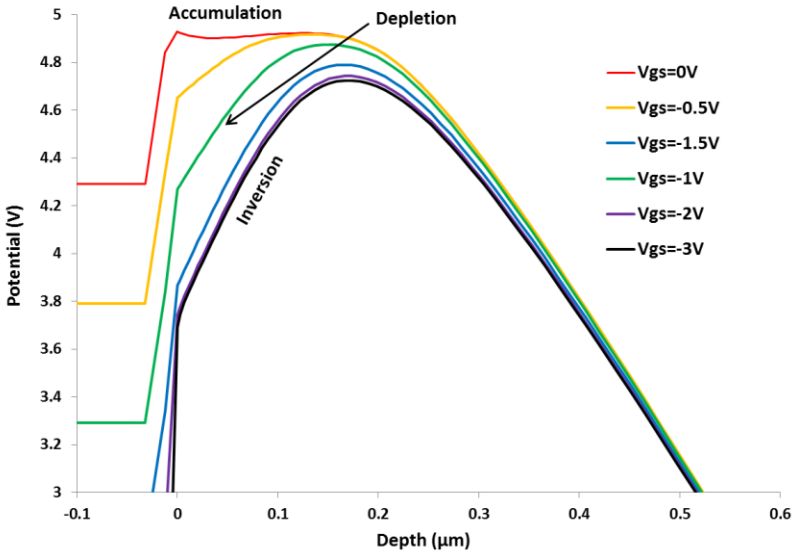

Figure 7. Simulated potential profiles for the BC transistor under the center of the gate for V_{DS}=1V.

4.4 Gain and bandwidth

The frequency response of the three types of transistors in a source follower configuration is shown in Figure 8. The measurements were carried out using the same drain current I_D = 10µA for all transistors. This value was chosen to be representative for the typical currents used in the source followers in CIS. It can be seen that the gain of the BC transistor is markedly lower that the SC devices despite all three having similar gate transconductance, and this can be explained by the stronger body effect. The circuit bandwidth is in the 300-400 kHz range, limited by the parasitic and the input capacitance of the LNA.

4.5 Input-referred noise

The input-referred voltage noise density of a deep-depleted BC transistor as a function of the drain current is shown in Figure 9. For the typical gate transconductance of the DUT (g_m = 20-50 µA/V) the input-referred noise density arising from the load resistor $e_n^2 = 4kT/g_m^2 R_L$, where k is the Boltzmann's constant and T is the absolute temperature, was calculated to be much lower than the dominant low frequency noise and could be ignored. The thermal noise density of the BC transistor, calculated using the formula[8]

$$e_n^2 = 8kT/3g_m \tag{1}$$

is in the range between 14.5 $nV/\sqrt{Hz}$ and 23 $nV/\sqrt{Hz}$.

Figure 9 shows that there is an optimum operating point for achieving the lowest noise, corresponding to the buried channel operating in depletion with minimal interaction of the current carriers with the Si-SiO_2 interface and reduced contribution of other noise sources.

The lowest drain currents correspond to conditions where inversion takes place under the gate, the source follower circuit gain is low and there is an additional generation-recombination noise component from the inversion layer, resulting in high input-referred noise. As the gate-source voltage V_{GS} and the drain current increase, the inversion layer largely disappears and the noise at low frequencies drops significantly. Increasing V_{GS} further brings about the optimal channel conditions at drain current I_D around 11.5µA, with the low frequency noise exhibiting a characteristic decrease typical of BC devices. It is also worth noting that the low frequency noise spectrum appears to deviate from the *1/f* dependence and is closer to $(1/f)^2$, an indication of generation-recombination noise[11]. Based on the simulated drain current and hole concentration profiles, this is supporting our conclusions that the interaction between the electrons in the conducting channel and the Si-SiO_2 interface in this transistor type can be greatly suppressed.

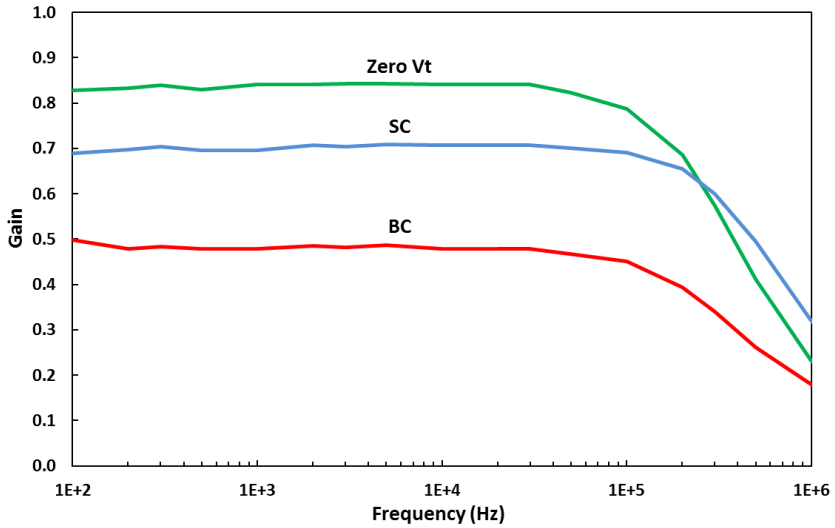

Figure 8. Gain and bandwidth of the three transistor types in a source follower circuit at drain current I_D = 10µA and drain voltage V_D = 5V. The load resistor R_L is 390 KΩ for the BC and Zero Vt types, and 330 KΩ for the SC type.

As the drain current increases further, the voltage drop across the load resistor increases to a point where the drain-source voltage is not sufficient to keep the MOSFET in saturation, thus decreasing the gain of the source follower circuit and superficially increasing the input-referred noise. Device simulations were performed for the bias conditions of the source follower test circuit, where the gate voltage spans between substrate and drain potentials. The results show that the transistor begins operating in linear regime *before* the channel enters accumulation, when current would be flowing near the surface.

Our analysis indicates that the most important condition for achieving the lowest noise in a BC source follower is to select the bias conditions such that inversion under the gate does not occur. In CIS the source follower buffers the sense node, which collects the photo-generated signal and is periodically reset to a fixed voltage by a reset transistor. The potential on the sense node and the gate voltage of the BC source follower will decrease as the signal is collected, and at large signals will approach or reach the conditions for surface inversion. Even if partial inversion does occur, this usually happens when the signal is at its largest, and it is likely that in those conditions the total noise is dominated by the signal shot noise.

The second condition is to make sure that the BC transistor is always saturated by maintaining sufficient drain-source voltage to avoid signal-dependent source follower gain. This could be accomplished by choosing an appropriate reset voltage for the sense node. If this condition is not satisfied the source follower gain could change significantly at small photo-generated signals, until more signal is collected and the gate voltage decreases accordingly.

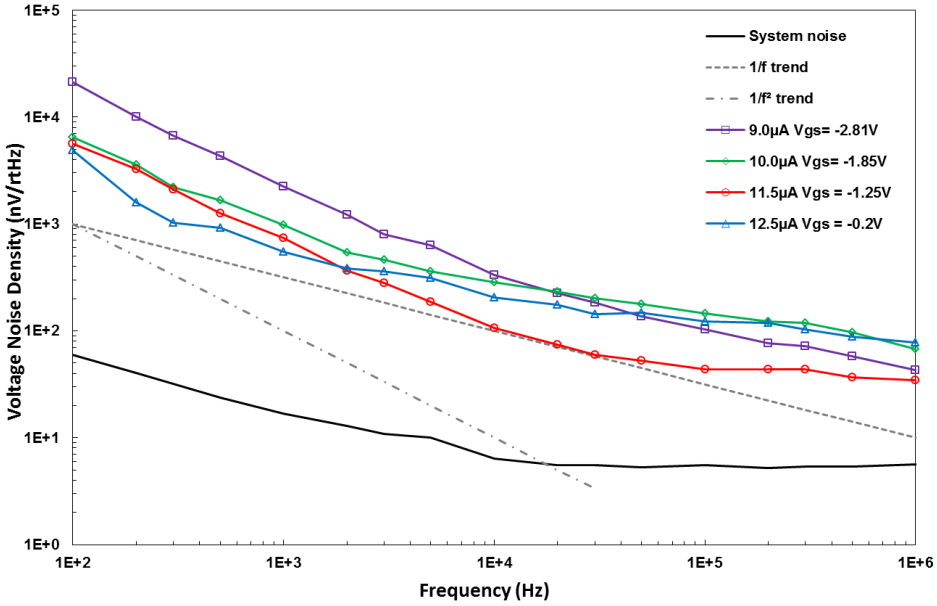

Figure 9. Input-referred voltage noise density spectra for a BC transistor (W/L = 1.6µm/0.6µm) at different drain currents.

The input-referred voltage noise density spectrum of a Zero Vt transistor is shown in Figure 10. In comparison with the deep depletion BC device, the noise does not have strong drain current dependence and exhibits little deviation from the *1/f* trend. In particular, the low frequency noise stays almost constant, unlike in the BC transistor. Very similar behavior was observed in the standard enhancement mode SC transistors too.

It is reasonable to expect the *1/f* noise from the two smaller transistors to be nearly identical due to their similar area – 0.96 μm^2 and 0.72 μm^2 for the BC and Zero Vt transistors, respectively, as the *1/f* noise power density is inversely proportional to the device area[12,13]. The three transistors types have different W/L ratio and an exact comparison between them is not attempted here. However, their thermal noise calculated using (1) is comparable because at the measurement conditions their transconductance is similar.

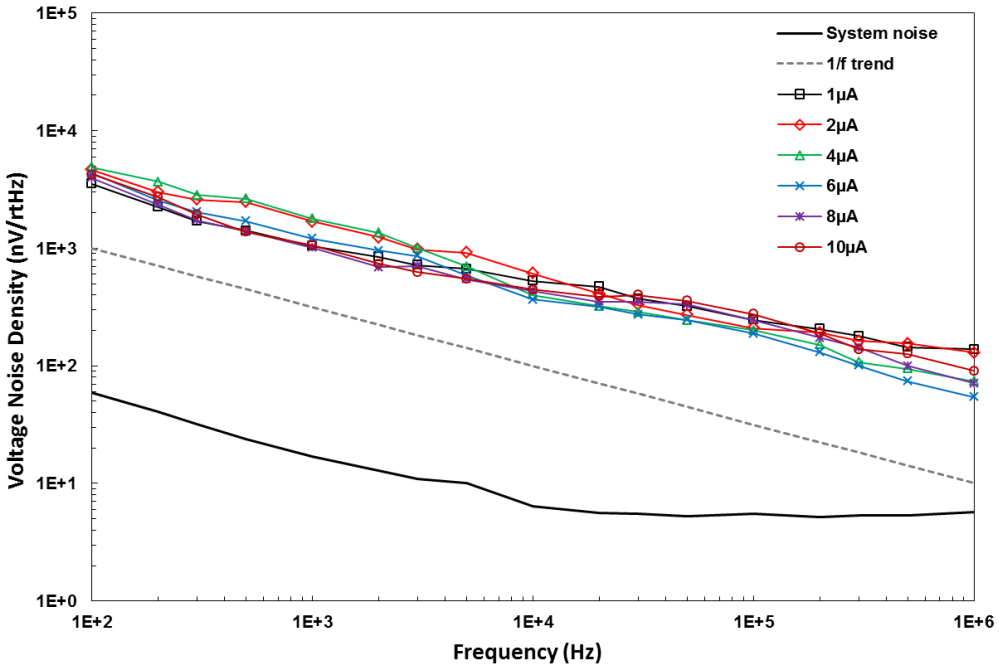

Figure 10. Input-referred voltage noise density spectra for a Zero Vt transistor (W/L = 0.6µm/1.2µm) at different drain currents.

A plot of the input-referred voltage noise density spectra of the three transistor types is shown in Figure 11. For the BC device the spectrum was measured at the optimal current for achieving the lowest noise, within the bias constraints.

For the two SC transistors the noise was measured at I_D=10 µA, considering that the noise dependence on the drain current is small. It can be seen that at frequencies between 10 kHz and 100 kHz the voltage noise density of the BC MOSFET can be up to 5 times lower than in SC devices. At frequencies approaching 1 MHz this advantage diminishes as the thermal noise becomes dominant, but the noise reduction can still be useful.

The trend in high performance CIS is towards column parallel readout with row settling and readout times of the order of few microseconds, corresponding to signal bandwidths below 100 kHz[14]. This is in the range of frequencies where the deep depleted BC MOSFET exhibits lower noise density, and the total readout noise of the image sensor could benefit. Successfully using this type of transistor requires good understanding of its operation and careful consideration of the signal-dependent bias conditions. Its manufacture requires an additional implantation step to create the buried channel, and further optimization of the doping profile could be required to match the parameters to particular operating voltages and currents.

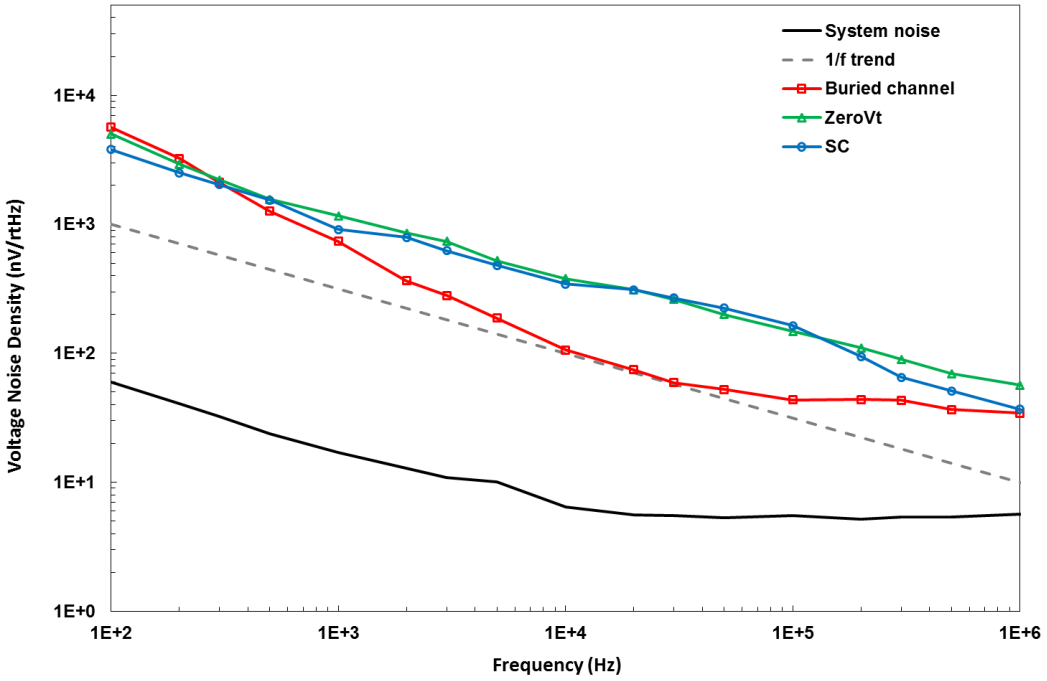

Figure 11. Input-referred voltage noise density spectra of the three transistor types.

5. CONCLUSION

We have presented I-V and noise characteristics of three distinctly different *n*-type MOSFET types and have evaluated their performance for application as source followers in CIS. The devices are deep depletion BC transistor, a normal enhancement mode SC transistor and a "zero threshold" transistor.

The results from the noise measurements indicate that under optimal bias conditions the *1/f* noise component in the deep depletion BC transistors can be significantly suppressed due to the drain current flowing at depth below the Si-SiO_2 gate interface and the reduced interaction of the current carriers with the interface. Detailed semiconductor device simulations have been used to understand the behavior of the BC device and the agreement with the experimental data is good. The Zero V_t transistor requires slightly negative gate-source voltage for turn-off and is somewhere in the middle between the BC and SC types, but its noise behaves in a way similar to an enhancement SC MOSFET and does not show the characteristic noise reduction of the BC device.

Unlike the SC transistors, the BC devices require careful selection of the biasing point to achieve optimal noise at a given drain current. Avoiding either inversion or accumulation at the interface is required to minimize the noise. The input-referred voltage noise density of a correctly biased deep depleted BC transistor is shown to be a factor of 5 lower at frequencies above 10 kHz than in a similar SC device, despite the lower gain of the BC transistor in a source follower circuit.

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