Enhanced Independent Pole Control of Hybrid MMC-HVDC System

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Abstract—This paper presents an enhanced independent pole control scheme for hybrid modular multilevel converter (MMC) based on full bridge sub-module (FBSM) and half bridge sub-module (HBSM). A detailed analysis of power distribution between upper and lower arms under asymmetrical DC pole voltages is presented. It is found that the fundamental AC currents in the upper and lower arms are asymmetrical. To enable operation under asymmetrical DC pole voltages, an enhanced independent pole control scheme is proposed. The controller is composed of two DC control loops, two AC control loops and circulating current suppression control based on current injection. Six modulation indices are presented to independently control the upper and lower arms. With this controller, the DC voltage operating region is significantly extended. To ride through pole to ground DC fault without bringing DC bias at the neutral point of interface transformer, a pole to ground DC fault ride through strategy is proposed. Feasibility and effectiveness of the proposed control scheme are verified by simulation results using PSCAD/EMTDC.

Index Terms— Asymmetrical DC pole voltage, DC pole to ground fault, DC pole to pole fault, energy balance, hybrid MMC, overhead line.

I. Introduction

Increasing demand for integrating bulk onshore renewable energy over long distance has promoted researches on MMC-HVDC (modular multilevel converter based HVDC) transmission using overhead lines [1][2]. To deal with the frequent DC faults on overhead lines, several DC fault tolerant topologies have been proposed [2]-[5]. Although these topologies can isolate the fault current by blocking the IGBTs of the MMC, it prolongs the shutdown of the entire HVDC system and loses the ability to continuously support the AC system during DC faults [6].

To ride through DC faults without blocking the IGBTs, the hybrid MMC based on full bridge sub-module (FBSM) and half bridge sub-module (HBSM) has drawn significant attention in the last few years [7]. The hybrid MMC utilizes the negative voltage output ability and has the merits of fast DC fault current clearance, flexible DC voltage manipulation, and quick system recovery. The design, operation and improved PWM modulation of hybrid MMC have been discussed in [7]-[9]. Its pre-charging and pole-to-pole DC fault ride through strategy were studied in [10], and in [11] an optimal design method to determine the number of FBSM and HBSM was presented and a DC modulation index and elementary control were also introduced.

However, most of the existing literatures have mainly focused on the design, operation and control of hybrid MMC under symmetrical DC pole conditions. Limited attention has been paid to asymmetrical conditions which are common in practical applications. For the HB MMC, reference [12] analysed the behaviour of HB MMC under asymmetrical arm impedance and a differential mode controller, a common mode controller and power balance controller for each phase whereas were designed. An asymmetric control mode for HB MMC to suppress capacitor voltage ripples in low frequency low voltage motor drive applications was proposed in [13]. References [14] and [15] studied the general performance of HB MMC under asymmetrical DC pole voltages and it was reported that there would be DC bias voltage and current at the secondary side of the interface transformer, which increase the cost of insulation and manufacturing of the transformers. To enable operation under DC pole imbalance, [15] proposed a method of controlling the current injected into the star-point reactor of the interface transformer though this method interferes the third harmonic voltage injection of HB MMC leading to reduced MMC voltage margins.

Compared with the HB MMC, hybrid MMC has more control freedoms and can have better performance under asymmetrical conditions. Reference [16] studied the operation of MMC with asymmetrical arm configurations. Double-loop controllers are re-designed for the upper and lower arms separately to decouple the AC/DC voltage offset. However, the DC faults handing ability of the proposed controller was not validated. An enhanced fault ride through control for hybrid MMC was presented in [17] where an additional phase angle was introduced to balance the power between the upper and lower arms during a pole-to-ground (PTG) DC fault.

The main contribution of this paper is to presents a novel independent pole control scheme for hybrid MMC-HVDC system to enable continuous operation under asymmetrical DC pole voltages and DC faults. With the independent control scheme, the hybrid MMC is able to continuously operate under asymmetrical DC pole voltages and ride through PTG DC fault without bringing DC bias at the neutral point of the interface transformer. Thus, a symmetrical monopole MMC-HVDC system can be operated as a bi-pole HVDC

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system.

This paper is organised as follows. Section II depicts the operating principle of hybrid MMC under asymmetrical DC pole voltages. Based on the analysis, section III proposes an independent pole control scheme to independently control the upper and lower arms. To ride through the PTG DC fault, a fault ride through strategy is proposed in section IV. The effectiveness of the proposed control is verified by simulations in section V, and finally, conclusions are drawn in section VI.

II. Analysis of Hybrid MMC Under Asymmetrical DC Pole Voltages

The circuit configuration of a three-phase hybrid MMC is depicted in Fig. 1. Each converter arm has N sub-modules that are consisted of N_{fb} FBSM and N_{hb} HBSM. Topologies of the FBSM and HBSM are shown in Fig. 1.

In Fig. 1, V_{dc}^{p} and V_{dc}^{n} are the respective potentials of positive and negative DC poles. I_{dc}^{p} and I_{dc}^{n} are the DC pole currents. v_{gi} and i_{gi} are the respective output AC phase voltage and current; v_{cpi} and v_{cni} are the arm voltages generated by the N SMs; i_{pi} and i_{ni} are the upper and lower arm currents, where the subscript i refers to phase a, b, c. C is the SM capacitance. L and R are the arm inductance and resistance. S_n, V_{dcn}, I_{dcn}, V_{cn} are the rated transmitting power, rated DC pole to pole voltage, rated DC pole current and rated SM capacitor voltage, respectively.

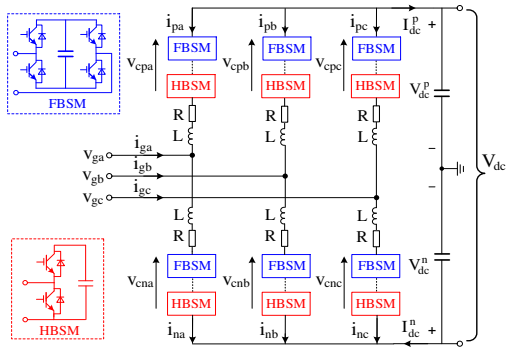


Fig. 1. Topology of hybrid MMC based on FBSM and HBSM.

Taking phase a as an example, the phase voltage and current can be expressed as:

$$\begin{cases} v_{ga} = V_m \cos \omega t \\ i_{ga} = I_m \cos(\omega t + \varphi_a) \end{cases} \tag{1}$$

where V_m and I_m are the amplitude of the phase voltage and current. φ_a is the angle difference between the phase voltage and current. According to [18], each arm current mainly contains a DC component, a fundamental frequency component and a second order harmonic component. Thus, the arm currents can be denoted as

$$\begin{cases} i_{pa} = I_{pa0} - I_{pa1m}\cos(\omega t + \varphi_a) + I_{pa2m}\cos(2\omega t + \varphi_{2a}) \\ i_{na} = I_{na0} + I_{na1m}\cos(\omega t + \varphi_a) + I_{na2m}\cos(2\omega t + \varphi_{2a}) \end{cases} \tag{2}$$

where I_{ja0}, I_{ja1m}, I_{ja2m} (j=p, n) are the amplitudes of the DC component, the fundamental frequency component and the second order harmonic component in arm currents, respectively. φ_{2a} is the phase angle of the second order harmonic component in the arm current. Neglecting the high order components and the resistive voltage drops on arm inductors, the instantaneous power absorbed by the SM capacitors on the upper arm can be obtained

$$\begin{aligned} p_{pa} &= v_{cpa}\cdot i_{pa} = (V_{dc}^{p} - v_{ga})\cdot i_{pa} \\ &= V_{dc}^{p}I_{pa0} + \frac{V_m I_{pa1m}\cos\varphi_a}{2} - V_m I_{pa0}\cos\omega t - V_{dc}^{p}I_{pa1m}\cos(\omega t + \varphi_a) \\ &\quad - \frac{V_m I_{pa2m}\cos(\omega t + \varphi_{2a})}{2} + \frac{V_m I_{pa1m}\cos(2\omega t + \varphi_a)}{2} \\ &\quad + V_{dc}^{p}I_{pa2m}\cos(2\omega t + \varphi_{2a}) \end{aligned} \tag{3}$$

Similarly, the instantaneous power absorbed by the SM capacitors on the lower arm is

$$\begin{aligned} p_{na} &= v_{cna}\cdot i_{na} = (v_{ga} - V_{dc}^{n})\cdot i_{na} \\ &= -V_{dc}^{n}I_{na0} + \frac{V_m I_{na1m}\cos\varphi_a}{2} + V_m I_{na0}\cos\omega t - V_{dc}^{n}I_{na1m}\cos(\omega t + \varphi_a) \\ &\quad + \frac{V_m I_{na2m}\cos(\omega t + \varphi_{2a})}{2} + \frac{V_m I_{na1m}\cos(2\omega t + \varphi_a)}{2} \\ &\quad - V_{dc}^{n}I_{na2m}\cos(2\omega t + \varphi_{2a}) \end{aligned} \tag{4}$$

To balance the transferred power between the AC and DC systems, the integral of (3) and (4) in one fundamental cycle should be zero. Therefore, there are

$$\begin{cases} V_{dc}^{p}I_{pa0} + \dfrac{V_m I_{pa1m}\cos\varphi_a}{2} = 0 \\ -V_{dc}^{n}I_{na0} + \dfrac{V_m I_{na1m}\cos\varphi_a}{2} = 0 \end{cases} \tag{5}$$

Since the sum of three-phase arm currents is equal to the DC pole current, I_{pa0} and I_{na0} can be calculated as

$$I_{pa0} = -\frac{I_{dc}^{p}}{3}, I_{na0} = -\frac{I_{dc}^{n}}{3} \tag{6}$$

Substituting (6) into (5) and considering that I_{dc}^{p} equals I_{dc}^{n} during steady state, there is

$$-\frac{V_{dc}^{p}}{V_{dc}^{n}} = \frac{I_{pa1m}}{I_{na1m}} \tag{7}$$

Considering i_{na}-i_{pa}=i_{ga}, the fundamental frequency components in the upper and lower arm currents can be calculated as

$$\begin{cases} i_{pa1} = \dfrac{V_{dc}^{p}}{V_{dc}^{p} - V_{dc}^{n}} i_{ga} \\ i_{na1} = \dfrac{-V_{dc}^{n}}{V_{dc}^{p} - V_{dc}^{n}} i_{ga} \end{cases} \tag{8}$$

The circulating current i_{diffa} on phase a can be therefore calculated as

$$i_{diffa} = \frac{i_{pa} + i_{na}}{2} = -\frac{I_{dcn}}{3} - \frac{V_{dc}^{p} + V_{dc}^{n}}{2(V_{dc}^{p} - V_{dc}^{n})} i_{ga} + i_{diff2} \tag{9}$$

where i_{dfiff2} denotes the second order frequency component.

Comparing with operation under symmetrical condition, it can be concluded from the above analysis that: 1) the peak value of the fundamental frequency components in the upper and lower arm currents are proportional to the potential of the DC pole voltages as shown in (7); 2) there is a fundamental frequency component existing in the circulating current as

shown in (9); 3) the positive and negative poles can be separately controlled if the AC and DC components in the upper and lower arm currents are independently controlled.

III. Independent Pole Control of Hybrid MMC

A. DC Pole Voltage/Power Control

As reported in [11] and [19], the AC output voltage of phase a can be controlled by

$$v_{ga} = m_a \frac{V_{armdcn}}{2}\cos\omega t \tag{10}$$

where m_a is the AC modulation index of phase a ($0<m_a\leq 1$). V_{armdcn} is the DC component in arm voltage which is the same as nominal DC voltage under steady state conditions ($V_{armdcn}=V_{dcn}$).

To regulate the DC pole voltages independently, two DC modulation indices M_{dc}^p and M_{dc}^n are introduced

$$V_{cp\_dc} = M_{dc}^p \frac{V_{armdcn}}{2}, V_{cn\_dc} = M_{dc}^n \frac{V_{armdcn}}{2} \tag{11}$$

where V_{cp_dc}, V_{cn_dc} are the DC components in arm voltages. The arm voltages can be re-written as

$$v_{cpa} = \frac{V_{armdcn}}{2}(M_{dc}^p - m_a\cos\omega t), v_{cna} = \frac{V_{armdcn}}{2}(m_a\cos\omega t - M_{dc}^n) \tag{12}$$

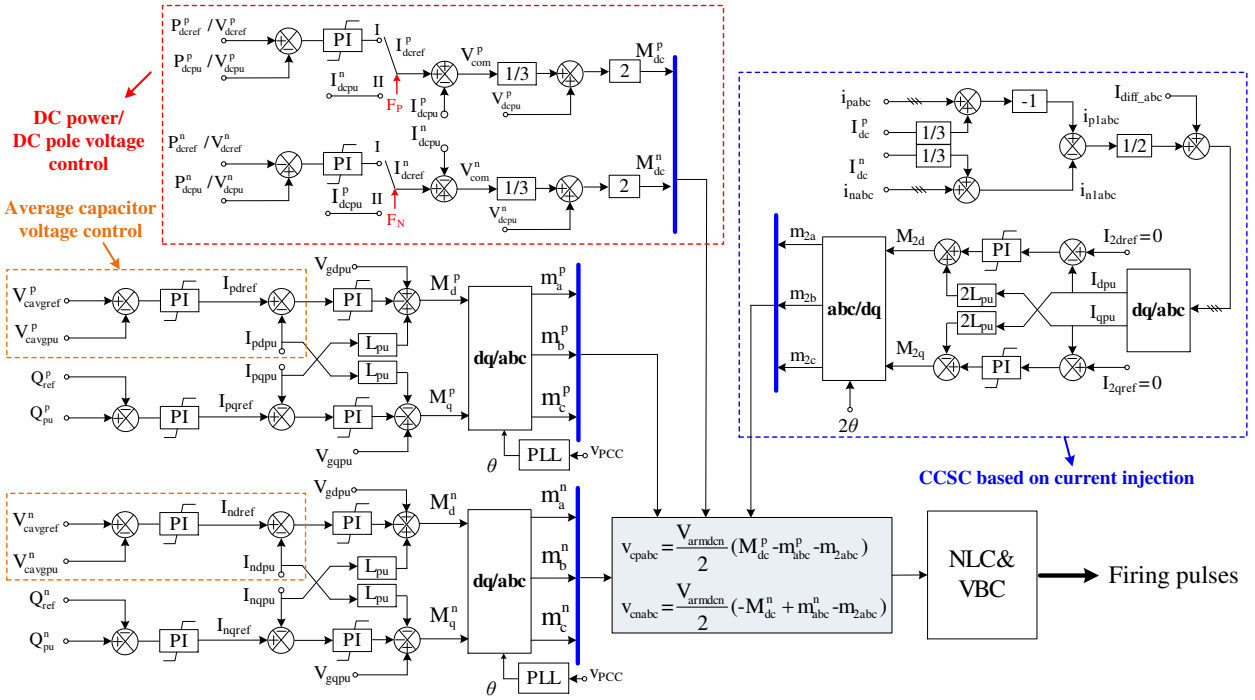


Fig. 2. Control diagram of independent pole control.

B. Capacitor Energy Control

For the upper arms, the active power injected into the hybrid MMC from the AC system can be expressed as:

$$P_{ac}^p = \frac{3}{2} v_{gd} i_{pd} \tag{17}$$

where i_{pd} is the d-axis component of i_{pa1}, i_{pb1} and i_{pc1} in dq rotating frame. The instantaneous power transmitted to the DC system satisfies:

The dynamic of the upper arm current of phase a is obtained

$$L\frac{di_{pa}}{dt} + Ri_{pa} = V_{dc}^p - \frac{1}{2}M_{dc}^p V_{armdcn} \tag{13}$$

Adding up the three upper arms of the three-phase and considering $i_{pa}+i_{pb}+i_{pc}=-I_{dc}^p$ result

$$L\frac{dI_{dc}^p}{dt} + RI_{dc}^p = \frac{3}{2}M_{dc}^p V_{armdcn} - 3V_{dc}^p \tag{14}$$

Let $V_{com}^p=3M_{dc}^p V_{armdcn}/2-3V_{dc}^p$ then it can be obtained from the PI controller as

$$V_{com}^p = K_p(I_{dcref}^p - I_{dcpu}^p) + K_i\int(I_{dcref}^p - I_{dcpu}^p)dt \tag{15}$$

Based on (15), an inner DC current control can be designed for the positive pole as shown in Fig. 2. Taking into account the active power transmitted to the DC positive pole, it satisfies:

$$P_{dc}^p = V_{dc}^p \cdot I_{dc}^p \tag{16}$$

Combining (16) with (15), the DC power/ pole voltage control can be implemented as an outer DC control loop, shown in Fig. 2. Similarly, the DC power/ voltage control and inner DC current control can be designed for the negative pole. It can be concluded that, by controlling M_{dc}^p and M_{dc}^n, the independent DC pole power/ voltage control can be achieved.

$$\frac{3}{2}v_{gd}i_{pd} = P_{dc} + P_{csm}^p \tag{18}$$

where P_{csm}^p is the power absorbed by the SMs on the upper arms and can be expressed as:

$$P_{csm}^p = 3Nd(\frac{1}{2}CV_{cavg}^{p2})/dt = 3NCV_{cavg}^p dV_{cavg}^p/dt \tag{19}$$

where V_{cavg}^p is the average capacitor voltage of the 3N SMs on the upper arms.

To balance the instantaneous power between the DC and

AC systems at any instant, the power absorbed by the SMs should be controlled to zero. By combining (18) and (19), an average capacitor voltage control can be designed as the outer AC control loop which controls the average capacitor voltage to be the set value and generates the d-axis current order [11].

Similarly, an average capacitor voltage control can be designed for the lower arms.

In Fig. 2, V_{gdpu} and V_{gqpu} are the dq components of the phase voltage in per unit form. v_{PCC} is the AC voltage at the PCC (Point of common coupling). (M_d^p, M_q^p, M_d^n, M_q^n) are the modulation indices in the dq rotating frame generated by the inner AC current control loop.

C. Circulating Current Suppression Control Based on Current Injection

To suppress the second order fundamental frequency component in the circulating currents, the circulating current suppression control (CCSC) proposed in [20] can be used. However, referring to (9), there is also an AC fundamental frequency components in the circulating current i_{diffi} (i=a, b, c) under asymmetrical DC pole voltages. As a result, high order harmonics will be deduced using dq transformation in the double fundamental frequency, negative sequence rotational reference frame.

To extract the second order frequency component, as seen in (9), the fundamental frequency component should be compensated. Therefore, the current injection method is re-designed for the CCSC as:

$$i_{inject\_i} = \frac{i_{pi1} - i_{ni1}}{2} \tag{20}$$

As shown in Fig. 2, the compensated current is injected as the input of CCSC.

Since the detailed design of nearest level control (NLC) and capacitor voltage balancing control (VBC) has been reported in [1] and [11], they will not be described further in this paper.

D. Operating Region of DC Pole Voltage

According to (5), (10) and (11), for the upper arm of phase a, there is

$$I_{pa1m} = 2M_{dc}^p I_{dc}^p / (3m_a \cos\varphi_a) \tag{21}$$

To ensure successful voltage balancing of the HBSMs, (22) should be satisfied.

$$I_{pa1m} \geq \left|I_{pa0}\right| = \left|I_{dc}^p / 3\right| \tag{22}$$

Therefore, M_{dc}^p should satisfy:

$$M_{dc}^p \geq m_a \cos\varphi_a / 2 \tag{23}$$

It can be seen from (23) that the minimum DC pole voltage is 0.5 (in pu term relative to $V_{dcn}/2$) under unit power factor. To enable operation under lower DC pole voltage, a feasible approach is to insert all N_{fb} FBSMs on each arm. Referring to (12), the output voltage of the upper arm meets

$$-N_{fb}V_{cn} \leq v_{cpi} = \frac{V_{armdcn}}{2}(M_{dc}^p - m_a \cos\omega t) \leq N_{fb}V_{cn} \tag{24}$$

Since $V_{cn}=V_{dcn}/N$, there is

$$-2N_{fb}/N + m_a \cos\omega t \leq M_{dc}^p \leq 2N_{fb}/N + m_a \cos\omega t \tag{25}$$

To always meet(25), M_{dc}^p should satisfy

$$m_a - 2N_{fb}/N \leq M_{dc}^p \leq 2N_{fb}/N - m_a \tag{26}$$

Equation (26) shows that the minimum value of M_{dc}^p can be equal to (m_a-2N_{fb}/N). Similar relationship can be derived for the lower arms as

$$m_a - 2N_{fb}/N \leq M_{dc}^n \leq 2N_{fb}/N - m_a \tag{27}$$

Equation (27) shows that the maximum value of M_{dc}^n can be equal to (2N_{fb}/N-m_a). Taking N_{fb}=N_{hb}=N/2 and m=0.9 as an example, (26) and (27) become

$$-0.1 \leq M_{dc}^p,\ M_{dc}^n \leq 0.1 \tag{28}$$

It shows that the minimum and maximum values of M_{dc}^p are -0.1 and 0.1 (in pu term relative to $V_{dcn}/2$) respectively. Therefore, with all the FBSMs inserted, the hybrid MMC is able to operate under the DC pole to pole voltage in the range of -0.1~0.1V_{dcn}.

As for M_{dc}^p, within the range of (0.1~0.5), HBSMs should be inserted to provide sufficient positive voltage, contributing to the total arm voltage in (12). However, to avoid HBSM voltage balancing problem and meet(23), the power factor $\cos\varphi_a$ shown in (23) should be decreased.

Using the dynamic phasor model proposed in [21], Fig. 3 depicts the PQ operating zone of the upper arms versus several constraints under V_{dc}^p=0.2pu. The DC base voltage, current, and apparent power are defined respectively as $V_{base}=V_{dcn}/2$, $I_{base}=I_{dcn}$, $S_{base}=S_n/2$. It can be seen from Fig. 3 that at 0.2 pu DC voltage, the upper arms of hybrid MMC is able to operate under 1pu DC pole current (namely, 0.2pu active power) unless 0.5~1pu capacitive or 0.4~1pu inductive reactive power is provided.

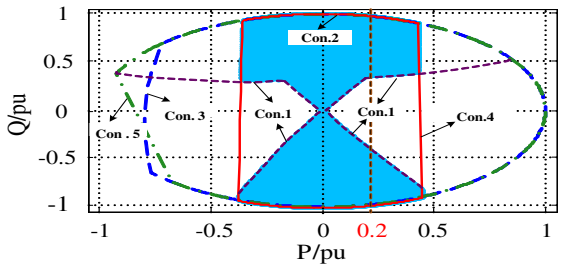


Fig. 3. PQ operating zone of positive pole when V_{dc}^p=0.2pu.
Con.1, voltage balancing constraint. Con.2, converter capacity constraint. Con.3, maximum arm current constraint (2pu). Con.4, maximum DC current constraint (2pu). Con.5, capacitor voltage fluctuation constraint (±10%).

In conclusion, for hybrid MMC with half FBSM and half HBSM, the operating region of DC pole voltage can be extended to -0.1~1pu.

IV. Fault Ride Through of PTG DC Fault

As for the most severe asymmetrical condition, the dynamics of the hybrid MMC during PTG DC fault is analysed. Fig. 4 shows the circuit diagram of a two-terminal HVDC system based on the hybrid MMC. The grounding configuration of the interface transformer adopts the high resistance grounding method implemented in the Yunnan Luxi MMC-HVDC asynchronous interconnection project [22].

Assuming the positive pole is subjected to a PTG DC fault, by using Kirchhoff's Voltage Law (KVL) and Kirchhoff's

Current Law (KCL), the following equations can be derived for the upper arms of the three-phase of MMC1.

$$\begin{cases} v_{ga1} - R_{g1} i_{f1} = -R_1 i_{pa1} - L_1 \dfrac{di_{pa1}}{dt} - v_{pa1} + R_{dc1} I^p_{dc1} + R_f i_f \\ v_{gb1} - R_{g1} i_{f1} = -R_1 i_{pb1} - L_1 \dfrac{di_{pb1}}{dt} - v_{pb1} + R_{dc1} I^p_{dc1} + R_f i_f \\ v_{gc1} - R_{g1} i_{f1} = -R_1 i_{pc1} - L_1 \dfrac{di_{pc1}}{dt} - v_{pc1} + R_{dc1} I^p_{dc1} + R_f i_f \end{cases} \quad (29)$$

where R_{dc1}, R_{dc2} and R_{dc} are the resistances of the overhead lines. R_{g1} and R_{g2} are the respective grounding resistances at MMC1 and MMC2 sides. R_f is the fault resistance. i_f is the fault current at the fault point. i_{f1} and i_{f2} are the currents flowing into the neutral point of the interface transformers at MMC1 and MMC2 sides, respectively. The subscript "1" refers to the variables at MMC1 side and the subscript "2" refers to the variables at MMC2 side. Adding up the three equations in (29) results:

$$\sum_{i=a,b,c} v_{pi1} = (3R_{dc1} + R_1) I^p_{dc1} + L_1 \frac{dI^p_{dc1}}{dt} + 3R_{g1} i_{f1} + 3R_f i_f \quad (30)$$

For the lower arms of MMC1 and MMC2, the following equations can be derived:

$$\begin{aligned} v_{ga1} - R_{g1} i_{f1} &= R_1 i_{na1} + L_1 \frac{di_{na1}}{dt} + v_{na1} - R_{dc} I^n_{dc} \\ &\quad - v_{na2} - R_2 i_{na2} - L_2 \frac{di_{na2}}{dt} + v_{ga2} - R_{g2} i_{f2} \end{aligned} \quad (31)$$

$$\begin{aligned} v_{gb1} - R_{g1} i_{f1} &= R_1 i_{nb1} + L_1 \frac{di_{nb1}}{dt} + v_{nb1} - R_{dc} I^n_{dc} \\ &\quad - v_{nb2} - R_2 i_{nb2} - L_2 \frac{di_{nb2}}{dt} + v_{gb2} - R_{g2} i_{f2} \end{aligned} \quad (32)$$

$$\begin{aligned} v_{gc1} - R_{g1} i_{f1} &= R_1 i_{nc1} + L_1 \frac{di_{nc1}}{dt} + v_{nc1} - R_{dc} I^n_{dc} \\ &\quad - v_{nc2} - R_2 i_{nc2} - L_2 \frac{di_{nc2}}{dt} + v_{gc2} - R_{g2} i_{f2} \end{aligned} \quad (33)$$

Adding up (31)-(33) results,

$$\begin{aligned} &\sum_{i=a,b,c} v_{ni1} - \sum_{i=a,b,c} v_{ni2} \\ &= (L_1 + L_2) \frac{dI^n_{dc}}{dt} + (3R_{dc} + R_1 + R_2) I^n_{dc} + 3R_{g2} i_{f2} - 3R_{g1} i_{f1} \end{aligned} \quad (34)$$

Recalling (12) and neglecting the line resistance, (30) and (34) can be re-written as

$$\frac{3V_{armdcn}}{2} M^p_{dc1} - R_1 I^p_{dc1} - L_1 \frac{dI^p_{dc1}}{dt} = 3R_{g1} i_{f1} + 3R_f i_f \quad (35)$$

$$\begin{aligned} \frac{3V_{armdcn}}{2} \left(M^n_{dc2} - M^n_{dc1} \right) &= (L_1 + L_2) \frac{dI^n_{dc}}{dt} + (R_1 + R_2) I^n_{dc} \\ &\quad + 3R_{g2} i_{f2} - 3R_{g1} i_{f1} \end{aligned} \quad (36)$$

Combining (35)-(36) and (14), it can be seen that the grounding resistance provides the path for fault current and affects the dynamic response of the DC current control loop.

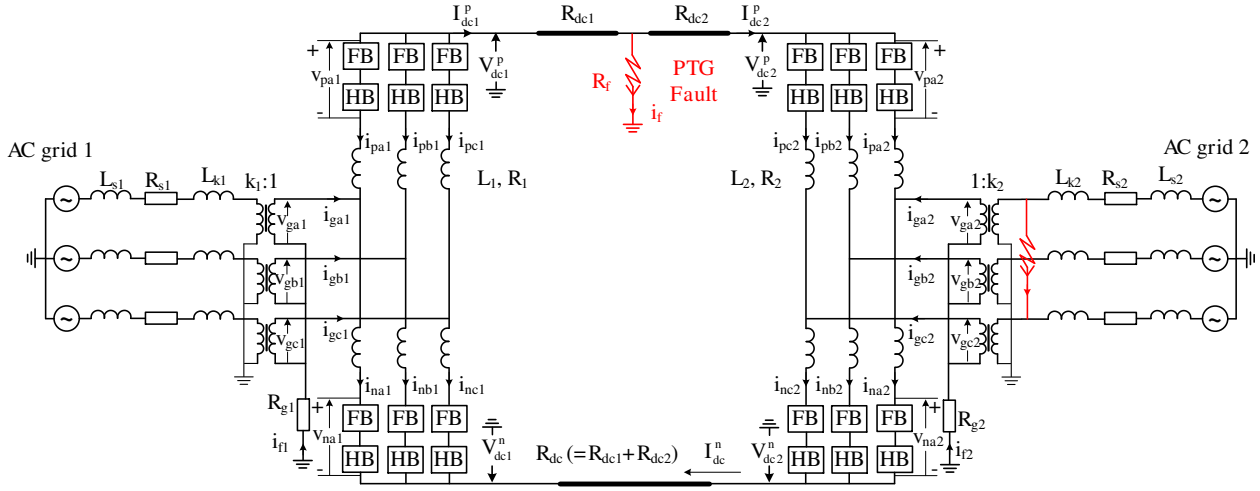


Fig. 4. Circuit diagram of a two-terminal VSC-HVDC based on hybrid MMC.

If the fault currents i_{f1} and i_{f2} are not controlled, there will be DC current flowing through the grounding devices of the interface transformers, which could bring magnetic saturation at the transformer windings and continuous heat of the grounding resistance. Thus, such current path needs to be avoided. To eliminate the fault current path for the fault currents, according to KCL, the DC current of the faulted pole (I^p_{dc1}, I^p_{dc2}) needs to be controlled to be the same as the current I^n_{dc} at the un-faulted pole. For the un-faulted pole, since it is desirable to transmit half of the rated power, I^n_{dc} should be controlled at the pre-fault value.

Referring to Fig. 2, the flags F_P (F_N) are used to configure the outer of the DC control loops. F_P=I corresponds to DC power control or DC voltage control whereas F_P=II corresponds to PTG DC fault ride through control. During a pole-to-ground DC fault, the DC current order of the faulted pole is set to be the same as the measured current of the un-faulted pole so that no steady-state fault current will flow through the fault point and the grounding resistance at the interface transformer.

V. Simulation Validations

A. The Test System

In order to verify the efficacy of the proposed controller, a

201-level two-terminal hybrid MMC-HVDC system shown in Fig. 4 is simulated in PSCAD/EMTDC. The number of FBSM per arm is 100 while the number of HBSM per arm is also 100. The simulation parameters are listed in Table 1.

The 120km overhead line is modelled using the frequency dependent model provided by PSCAD. MMC1 controls the DC pole voltages and MMC2 controls the transferred active power. To test the performance of the proposed controller, a relatively small DC limiting inductance of 50mH is used [23]. This independent pole control method is also applicable to HVDC using star reactor with resistance grounding configuration.

Table 1 Parameters of the simulated system

Parameters	Nominal value
MMC nominal power S_n	1000MW
Rated DC pole voltage	±320 kV
Rated DC arm voltage V_{armdcn} (V_{dcn})	640kV
AC system nominal voltage	400 kV
Short circuit ratio (SCR)	4.0
X/R ratio	10.0
Interface Transformer	400kV/352kV
Grounding Resistance R_g	5000Ω [22]
Capacitance of each SM	10mF
Arm inductance L	0.07H
Arm resistance R	3Ω
Rated capacitor voltage of each SM	3.2 kV

B. Verification of Monopole Reduced DC Voltage Operation

To verify the independent pole control, the DC voltage order of the positive pole is set to be 0.5pu (160kV) during 1.3-2.4s and 0.8pu (256kV) during 2.5-3.2s (the pu unit is relative to V_{dcn}/2 of 320kV). The simulation results are shown in Fig. 5.

Fig. 5(a) shows the DC pole voltages of MMC1. As can be seen, the DC voltage of positive pole is well controlled at 160 kV during 1.3-2.4s and 256 kV during 2.5-3.2s. Whereas the negative pole voltage is controlled at the rated -320 kV during the entire process.

Fig. 5(b) shows the DC modulation indices generated by the upper and lower DC current control loops. M_{dc}^{p} is controlled at 0.5 under steady state during 1.3-2.4s and at 0.8 during 2.5-3.2s, whereas M_{dc}^{n} is controlled at -1 under steady state. Figs. 5(a)-(b) validates the effectiveness of the two DC control loops.

Fig. 5 (c) shows the average capacitor voltages. At 1.2s and 2.4s, the active power is not equally split among the upper and lower arms due to the sudden change of DC pole voltages. As a result, there is divergence between the average capacitor voltages in the upper and lower arms. However, they are well controlled at 1 pu under steady state.

Fig. 5(d) shows the AC modulation indices generated by the upper and lower AC current control loops. Despite some transients at 1.2s, they are well controlled by the two AC control loops. Fig. 5(e)-(f) shows the output AC current and current flowing through R_{g1} at MMC1 side. Although the DC voltages of the positive and negative pole are asymmetrical, no DC bias current is observed.

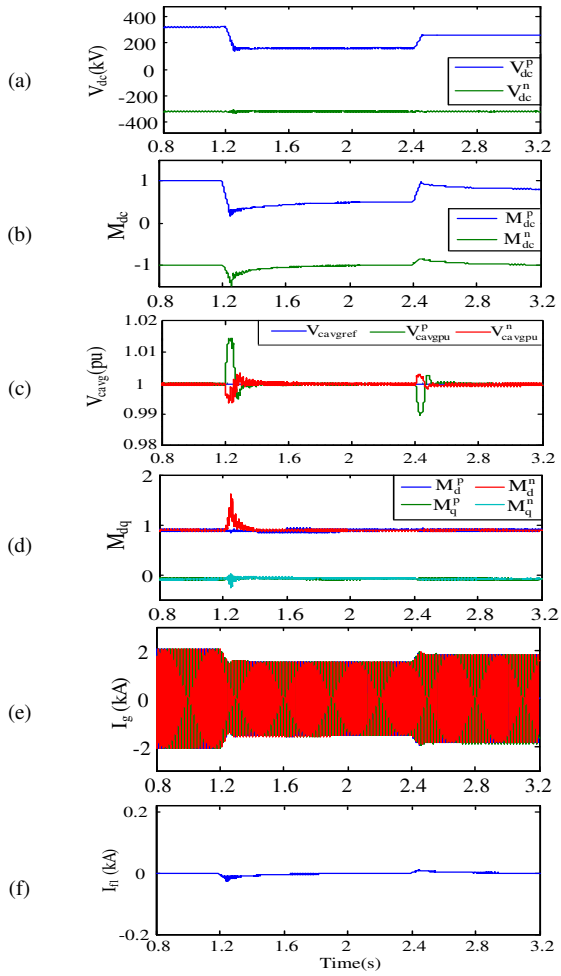


Fig. 5. Test of reduced DC voltage operation at the positive pole. (a) DC pole voltages. (b) DC modulation indices. (c) Average capacitor voltages of upper and lower arms. (d) AC modulation indices. (e) Output AC current. (f) Current flowing through R_{g1}.

To verify the efficacy of the proposed CCSC, the zoomed waveforms of the arm and circulating currents during 2.3-2.4s (V_{dc}^{p}=160kV, V_{dc}^{n}=-320kV) are shown in Fig. 6.

Fig. 6(a) shows that the peak-to-peak value of the fundamental frequency component in the lower arm current (2.35kA) is almost 2 times larger than the one in the upper arm current (1.16kA), which verifies the analysis in (7). The circulating current I_{diff} shown in Fig. 6(b) is calculated as the common mode current of the upper and lower arm currents. It can be seen that there are a DC component and a fundamental frequency component existing in I_{diff}. After adopting the current injection method as outlined in (23), the circulating current (I_{diff_inject}) has a pure DC component.

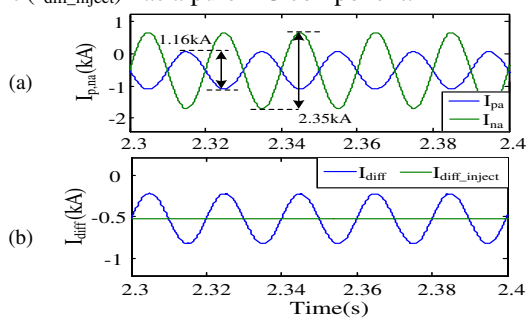


Fig. 6. Verification of CCSC based on current injection method. (a) Upper and lower arm currents of phase a. (b) Circulating currents.

C. Verification of Operating Region of DC Voltage

To verify the operating region of the DC pole voltage, the DC voltage order of the positive pole is ramped down from 1pu to 0.2pu during 1.2-1.5s. At the same time, the reactive power order of the positive pole is gradually decreased from 0 to -0.25 pu (relative to S_n). The simulations results are shown in Fig. 7.

Fig. 7(a) shows that the DC positive and negative pole voltages can be operated stably at 64 kV and -320 kV respectively, while providing reactive power as shown in Fig. 7(b). The upper and lower arm currents shown in Fig. 7(c) have both positive and negative values to ensure successful SM capacitor voltage balancing. This can be further noticed in Fig. 7(d) where the average capacitor voltages of the upper and lower arms are all well controlled at 1pu, and the well balanced average capacitor voltages of the FBSMs and HBSMs on the upper arm of phase a are shown in Fig. 7(e). V_{cFB} and V_{cHB} are the average capacitor voltages of the N/2 FBSMs and the N/2 HBSMs on the upper arm of phase a, respectively.

Fig. 7 validates the analysis in section III.D and Fig. 3, where 0.5 (in pu relative to $0.5S_n$) reactive power should be provided to enable operation under 0.2pu DC positive pole voltage.

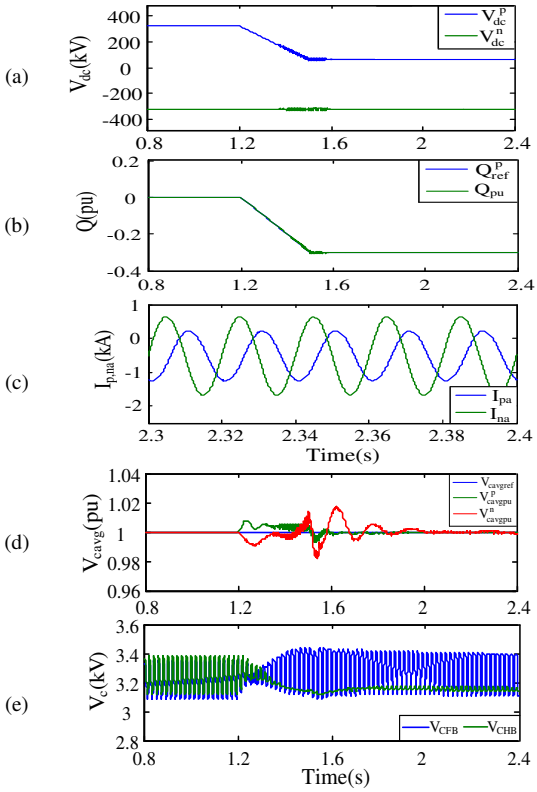


Fig. 7. Verification of operating region of DC pole voltages. (a) DC pole voltages. (b) Order and measured value of reactive power. (c) Upper and lower arm currents of phase a. (d) Average capacitor voltages of upper and lower arms. (e) Average capacitor voltages of FBSMs and HBSMs on the upper arm of phase a.

To verify the performance under minimum DC pole voltage, the DC voltage is ramped down from 640kV to -64kV ($-0.1V_{dcn}$) during 1.5-1.7s, and the simulations results are shown in Fig. 8.

Fig. 8(a) shows that the DC positive and negative pole voltages can remain stable at -32kV and 32kV respectively. Figs. 8(b)-(c) show the DC and AC modulation indices respectively, and they are well controlled by the DC and AC control loops. Both the upper and lower arm currents have negative value only as shown in Fig. 8(d). Since the HBSMs cannot be balanced with unipolar arm current, all HBSMs should be bypassed.

Fig. 8(e) shows the inserted SM number calculated by NLM (nearest level modulation). It can be seen that the minimum number is -100, i.e. all the FBSMs on each arm are negatively inserted. Fig. 8(f) shows the average capacitor voltages of the HBSMs and FBSMs on the upper arm of phase a. Since the HBSMs are bypassed, their average capacitor voltage on the upper arm of phase a (V_{cHB}) stays unchanged.

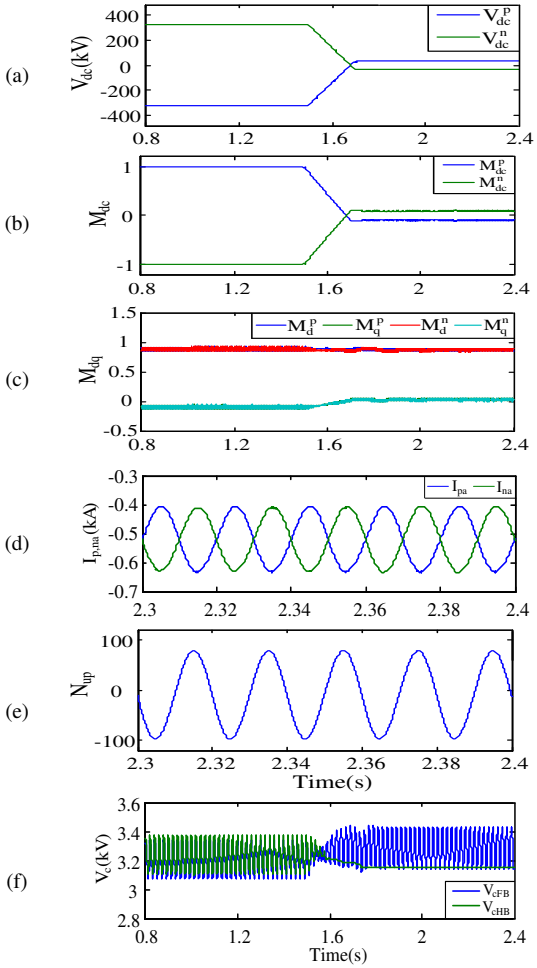


Fig. 8. Test of the hybrid MMC under DC voltage of $-0.1V_{dcn}$. (a) DC pole voltages. (b) DC modulation indices. (c) AC modulation indices. (d) Upper and lower arm currents of phase a. (e) Number of inserted SM on upper arm of phase a. (f) Average capacitor voltages of FBSMs and HBSMs on the upper arm of phase a.

To further verify the performance, the DC voltage is reduced from 640kV to -128kV ($-0.2V_{dcn}$) at 1.5s. The simulations results are shown in Fig. 9. From Figs. 9(a) and (b), it can be seen that the DC voltage and AC current controllers

become saturated. This is further evidenced from the inserted SM number shown in Fig. 9(c), as the output of NLM is saturated at -100.

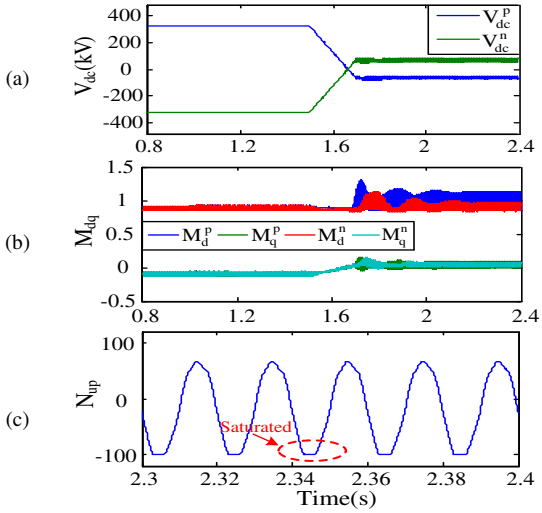


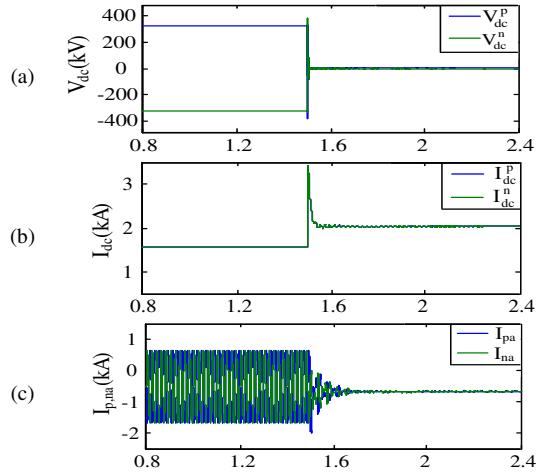
Fig. 9. Test of the hybrid MMC under DC voltage of -0.2V_{dcn}. (a) DC pole voltages. (b) AC modulation indices. (c) Number of inserted SM on upper arm of phase a.

D. Response to Pole to Pole DC Fault

To test the natural response of the proposed controller during pole to pole DC faults, a permanent pole to pole fault is applied at 1.5s. The fault point is 20km away from the DC terminal of MMC1.

Figs. 10(a) and (b) show the DC voltages and currents of both poles. Since the inner DC current reference is saturated at the upper limit I_{dclim} (1.3pu in this paper), the DC pole currents are controlled at 2.02kA. Figs. 10(c) and (d) show the arm currents and the fault current, and it can be seen that the arm currents are well limited with no over-current during the fault.

Fig. 10(e) shows the average capacitor voltages of the HBSMs and FBSMs on the upper arm of phase a. They largely remain balanced around the rated value except the initial over-voltage for the FBSMs during the fault due to the sudden loss of transmission power. Fig. 10(f) shows that the output AC voltage at MMC1 side has no DC bias.



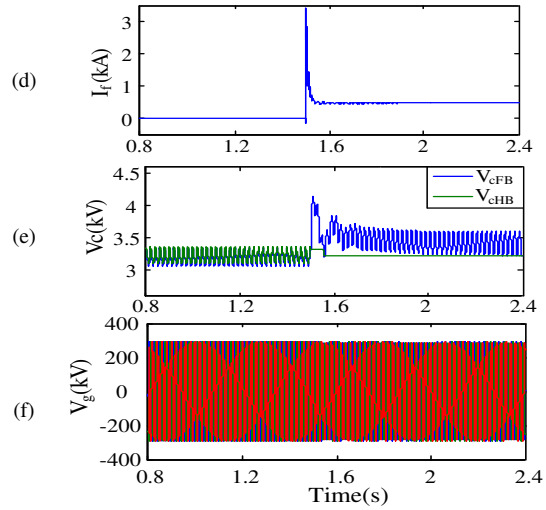
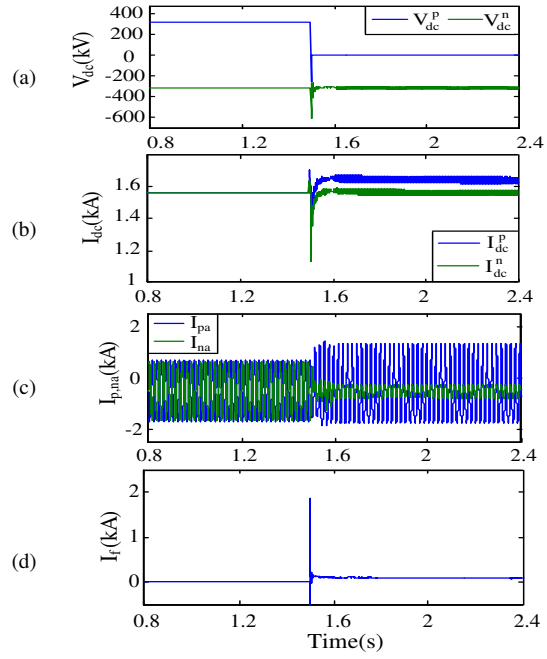


Fig. 10. Test of the hybrid MMC under pole to pole DC fault. (a) DC pole voltages. (b) DC pole currents. (c) Arm currents. (d) Fault current. (e) Average capacitor voltages of FBSMs and HBSMs. (f) Output AC voltage.

E. Response to Pole to Ground DC Fault without Fault Ride Through Control

Figs. 11(a)-(f) show the natural response to pole to ground DC fault where a permanent PTG DC fault is applied at the positive pole at 1.5s. Figs. 11(a) and (b) show the DC voltages and currents of both poles. As can be seen, at the instant of DC fault, the DC voltage of negative pole is decreased to be nearly -620kV due to the discharge of transmission line capacitors.

The arm currents and fault current shown in Figs. 11(c) and (d) indicate that they are still within the safe range during transients. Fig. 11(e) shows the average capacitor voltages of the HBSMs and FBSMs on the upper arm of phase a, and they are well balanced. Fig. 11(f) shows the output AC voltage at MMC1 side. Since the fault current flows through the grounding resistance of the interface transformer, a DC bias of -380kV is observed which increases the cost of insulation of the interface transformers.



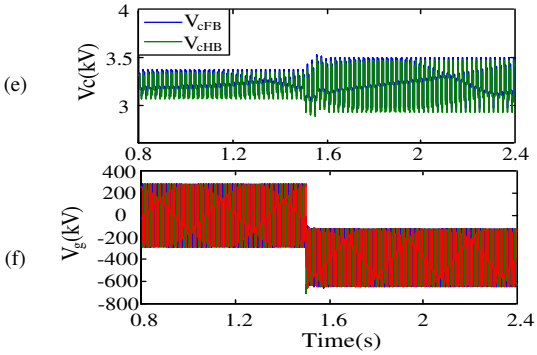
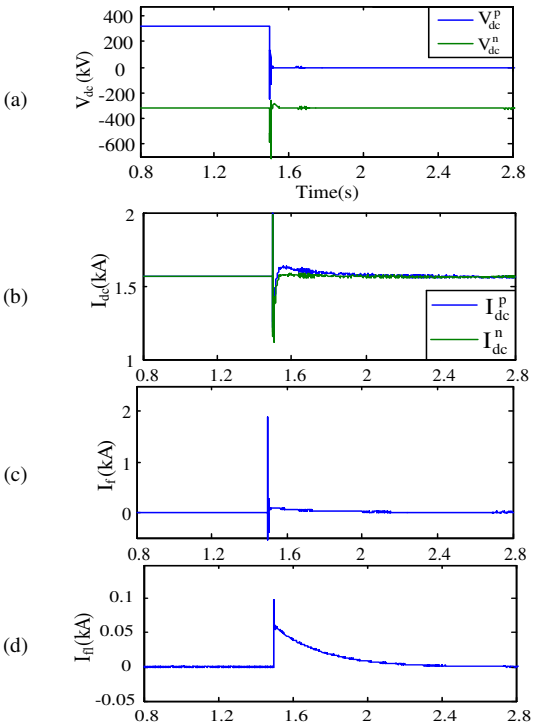


Fig. 11. Test of the hybrid MMC under pole to ground DC fault without fault ride through control. (a) DC pole voltages. (b) DC pole currents. (c) Arm currents. (d) Fault current. (e) Average capacitor voltages of FBSMs and HBSMs. (f) Output AC voltage.

F. Response to Pole to Ground DC Fault with Fault Ride Through Control

Figs. 12s (a)-(f) show the response to a permanent PTG DC fault applied at 1.5s using the proposed fault ride through control.

Figs. 12(a) and (b) show the DC voltages and currents of both poles. As can be seen, the DC current of the positive pole is controlled to be the same as the un-faulted pole. Therefore, the fault currents i_f and i_{fl} can be effectively eliminated, as shown in Figs. 12(c) and (d). Fig. 12(e) shows that the arm currents are still within the safe range during transients. Fig. 12(f) shows the average capacitor voltages of the HBSMs and FBSMs on the upper arm of phase a, and they are well balanced. Fig. 12 (g) shows the output AC voltage at MMC1 side. Since the fault current flowing through the grounding resistance of the interface transformer is eliminated, the DC bias voltage decreases to zero quickly.



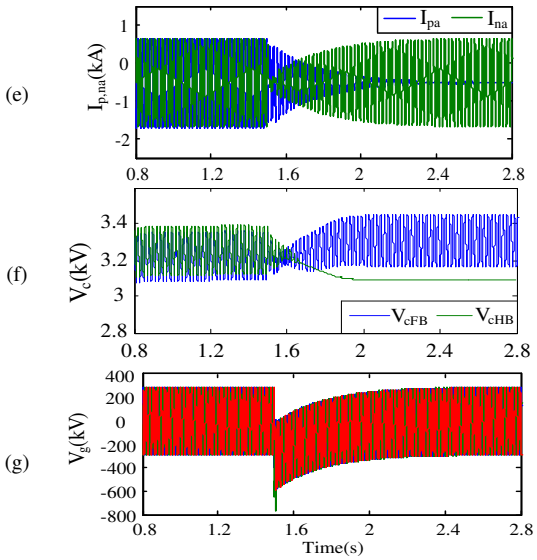
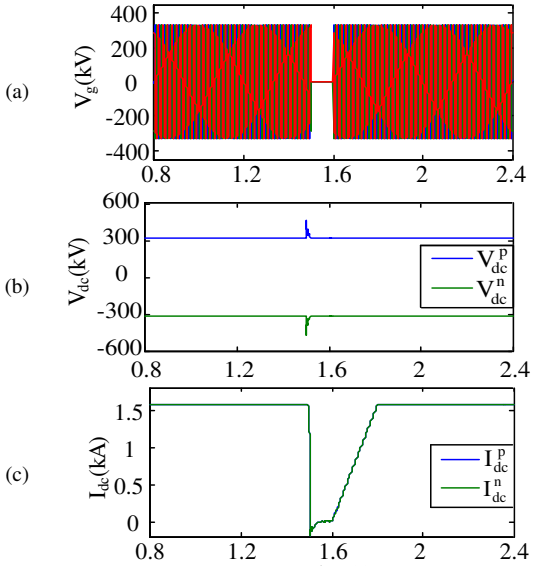


Fig. 12. Test of the hybrid MMC under pole to ground DC fault with fault ride through control. (a) DC pole voltages. (b) DC pole currents. (c) Fault current. (d) Current flowing through R_{g1}. (e) Arm currents. (f) Average capacitor voltages of FBSMs and HBSMs. (g) Output AC voltage.

G. Response to Three-phase AC Fault

Figs. 13(a)-(f) show the response to a three-phase AC short circuit fault. The temporary AC fault is applied at 1.5s at MMC2 side and lasts for 0.1s. On detecting the AC fault, the order of the active power reference is decreased to zero.

Fig. 13 (a) shows the AC voltage of AC grid 2, and Fig. 13 (b) shows the DC voltages of both poles. Because of the AC fault, the surplus power temporarily increases the DC pole voltages. The DC pole currents and arm currents shown in Figs. 13 (c)-(d) indicate that there is no over-current during the AC fault. The average capacitor voltages of the upper and lower arms as shown in Fig. 13 (e), are all well controlled at 1pu, and the well balanced average capacitor voltages of the FBSMs and HBSMs on the upper arm of phase a are shown in Fig. 13 (f).



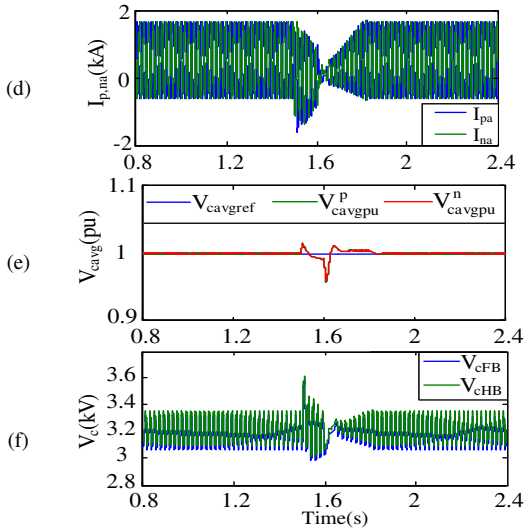


Fig. 13. Test of the hybrid MMC under AC fault. (a) AC voltage of AC grid 2. (b) DC pole voltages. (c) DC pole currents. (d) Arm currents. (e) Average capacitor voltages of upper and lower arms. (f) Average capacitor voltages of FBSMs and HBSMs on the upper arm of phase a.

VI. Conclusion

In this paper, an enhanced independent pole control is proposed for hybrid MMC operating under asymmetric DC pole voltages. Six modulation indices including DC modulation indices (M^{p}_{dc}, M^{n}_{dc}) and AC modulation indices (M^{p}_{d}, M^{p}_{q}, M^{n}_{d}, M^{n}_{q}) are generated to separately control the upper and lower arms.

With this enhanced independent pole control, the following attributes can be achieved. 1) The hybrid MMC is able to continuously operate under asymmetrical DC pole voltages without bringing DC bias at the neutral point of the interface transformer. 2) the DC voltage region of the hybrid MMC can be significantly extended, where a hybrid MMC based on half FBSM and half HBSM is able to operate within -0.1~1pu DC voltage range. Thus, the hybrid MMC has the ability to actively extinguish the fault arc like the LCC-HVDC system. 3) In case of PTG DC faults, the fault ride through control can effectively eliminate the fault current and the hybrid MMC is able to continuously operate at half of the rated power capacity. No DC bias voltage or current is present at the neutral point of the interface transformers during post-fault steady state.

The proposed control scheme enables a monopole symmetrical hybrid MMC-HVDC system to behave like a bi-pole system, thus provides an attractive approach with high robustness and system availability for applications in future HVDC systems.

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