Improving the Yield and Lifetime of Microfabricated Sensors for Harsh Environments

E.O. Blair, D.K. Corrigan, H.J. Levene, I. Schmueser, J.G. Terry *Senior Member IEEE*, S. Smith *Senior Member IEEE*, A.R. Mount, A.J. Walton *Senior Member IEEE*

Abstract – This paper details improvements in the design and fabrication of electrodes intended to function in the high temperature, corrosive environment of a molten salt. Previously reported devices have displayed low yield and lifetimes and this paper presents two strategies to improve these aspects of their performance. The first one involves reducing the critical area, which increased both the electrode yield and lifetimes. The second element utilised test structures, targeted at identifying failure mechanisms, which helped facilitate the materials/design modifications required to make the devices more robust.

***Index Terms* — Test Structures, Microelectrodes, Molten Salt, LKE, Yield, Lifetime, Microfabrication.**

I. Introduction

Molten salt (MS) is an important medium for metal manufacture, nuclear waste reprocessing, and renewable energy; in particular, the LiCl-KCl eutectic (LKE) has received significant attention [1]–[3]. However, operating temperatures in LKE are typically between 450 and 500°C and dissolved reactive species often produce a highly corrosive medium [4]. Hence, the development of microfabricated systems capable of survival in this environment is a challenge [5], [6]. However, being able to provide quantitative analysis of the chemical species present in the salt is important for process control in nuclear fuel reprocessing, where the concentration of U, Pu, and other fission products must be known. Also important for any MS industrial process is the monitoring of pipework corrosion by detecting elements such as Fe, Cr, and Ni. Microelectrodes offer a means to achieve this [7]–[9].

Previous work has delivered microelectrodes capable of successfully operating in the LKE environment [7]–[9]. However, the initial yield (percentage of devices which function for any length of time) of these devices has only been around 46% and they typically only survived for around 90 minutes of operation. These devices consist of a patterned electrode metal sandwiched between two insulating films with holes in the top insulation layer providing access to the electrode and contact pad. For these electrodes, the overlying dielectric forms the protective coating, insulating the microelectrode interconnect from the electrolyte. This covering is a key element in the operational survival of the structure, because for quantitative measurements the microelectrodes must retain a stable, known area during their lifetime [10], [11]. Failure of the top insulator during operation is normally indicated by an increase in current resulting from the exposure of additional electrode metal to the LKE. This changes the electrode area, which usually then becomes too large for the device to be considered a microelectrode. Clearly, being able to identify the causes of failure provides the information required to address these types of process challenges. Most importantly, the integrity of the overlying dielectric needs to be targeted to enable the development of microelectrodes that exhibit superior yield and lifetimes. There was also the aspiration to identify what, if any, simple measurements could be undertaken to help predict the likely yield and potential lifetime of batches of electrodes.

The presence of Li ions in the melt poses a severe challenge to the integrity of the dielectric, which is required to act as a barrier to the salt [12]. Electrode characterisation within an MS environment is also a time-consuming operation, requiring electrical connections that survive high temperatures (450 - 500°C) and corrosive environments. These two aspects of the operation of electrodes in MS make it only possible to characterise small numbers of structures each day. Therefore, for efficient and cost-effective fabrication it is imperative to deliver a high yield process.

The low yield and lifetime of the sensors presented a challenge and several methods were employed to improve these aspects of the devices' performance. Test structures have previously been employed to investigate device failures and were reported in the 2016 International Conference of Microelectronic Test Structures [13]. This paper presents an expanded version of this research. First described are the yield and lifetime of the initial microelectrode design. A commonly used method of improving yield and lifetime, reduction of critical area (CA), is then presented. This offered improved lifetimes but a significant number of devices still failed to function. Hence, test structures were then designed to investigate these continued microelectrode failures. They are employed to provide more quantitative information on the device design and quality of the fabrication process. The information gained from these test structures is then

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E.O. Blair, J.G. Terry, and A.J. Walton are with the Institute for Integrated Micro and Nano Systems, School of Engineering, SMC, The University of Edinburgh, King's Buildings, Edinburgh, EH9 3FF, UK.

S. Smith is with the Institute for Bioengineering, School of Engineering, SMC, The University of Edinburgh, King's Buildings, Edinburgh, EH9 3FF, UK.

H.J. Levene, I. Schmueser, and A.R. Mount are with the School of Chemistry, The University of Edinburgh, Joseph Black Building, Kings Buildings, Edinburgh, EH9 3JJ, UK.

D.K. Corrigan was with the School of Chemistry at The University of Edinburgh and is now with Department of Biomedical Engineering, Wolfson Building, University of Strathclyde, Glasgow, G4 0NW, UK.

Corresponding author: e.blair@ed.ac.uk.

incorporated into a new device design, which demonstrates a higher yield than previous designs.

II. Methodology

Experiments in MS were carried out using a standard three-electrode cell. An Ag/Ag^+ reference electrode was used in the measurements, the construction of which involved sealing a silver wire in a mullite tube which contained 1 g of LKE + 1% wt AgCl. All potentials quoted in this paper are with respect to this electrode. A 1.8 mm diameter tungsten rod was employed as the counter electrode. The microfabricated microelectrodes were used as the working electrode. Once fabricated, the devices were connected to crocodile clips that were crimped to a tungsten wire for the electrical connection to a potentiostat. The MS was contained in a vitreous carbon crucible in a quartz cell, located in a vertical tube furnace. Ports in the lid enabled the introduction of electrodes and gas lines, which were used to maintain the MS under an Ar atmosphere. The fabrication of the microelectrode is detailed in [7].

Microelectrode lifetimes were assessed by continuous plating and stripping of Ag from AgCl using cyclic voltammetry at 450°C and in a potential window of 0 V to -0.65 V. The devices were considered to have failed when they no longer displayed a microelectrode-type response. This is typically characterised by a steady state current in the nano-ampere range, associated with the reduction of solvated Ag^+ to solid Ag on the surface of the microelectrode [14]–[16]. Yield values were calculated from all experiments performed using the microelectrodes, and are reported as the percentage of electrodes which initially functioned as microelectrodes (even if this was for a very short time).

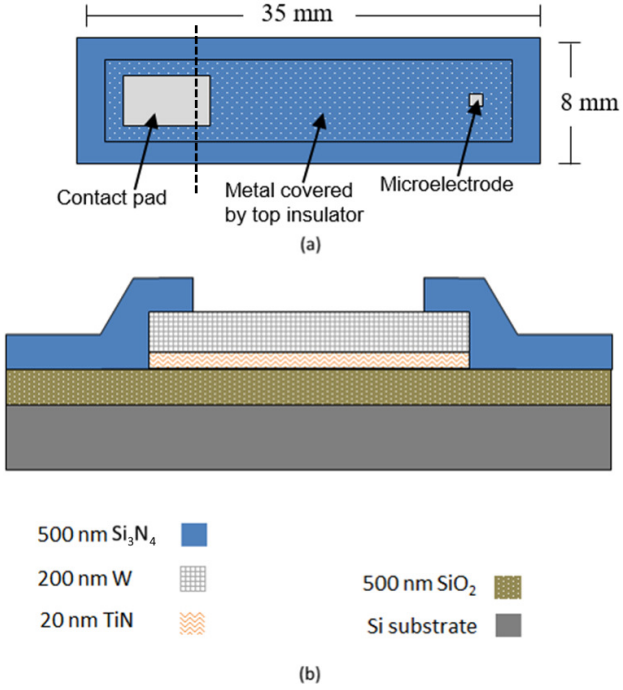

Figure 1: (a) Schematic of the microelectrode layout and (b) a transverse cross section of the microelectrode architecture through the dashed line in (a). Both the size of the microelectrode and the layer thickness has been exaggerated

III. Initial Microelectrode Layout

A. Yield

The initial microelectrode layout (IML) and a cross-section of the architecture is presented in figure 1 (a) and (b) respectively. These microelectrodes had a yield of only 45.8% (n = 84) when operated in the LKE. Functioning microelectrodes demonstrated quantifiable steady-state currents of around 50 – 500 nA depending on the microelectrode size [7], [9]. The majority of failed IMLs exhibited high currents of the order of 1 – 10 µA and no steady-state current. These were key indicators that additional electrode metal was exposed to the LKE. Despite this, inspection of the microelectrode insulation after operation found no obvious pinholes in most cases, although the presence of salt encrusted on the surface of the insulator made optical investigation difficult. A small number of devices suffered dielectric failure along the edge of the metal steps. Figure 2 (a) shows an example of when there is no failure at the step edge with (b) showing dielectric failure after use in MS.

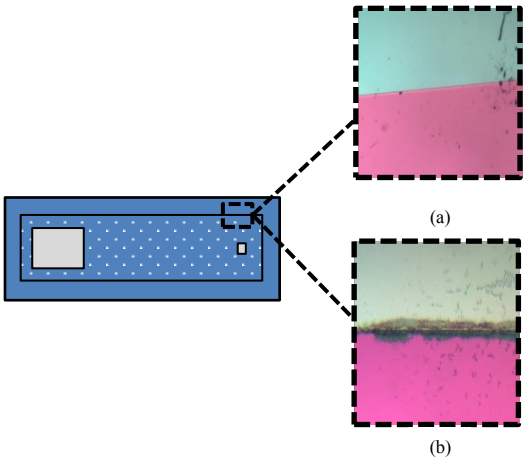

Figure 2: (a) A clean metal step with no dielectric damage. (b) An example of damage to the overlying dielectric along the perimeter of the metal step after use in the LKE.

B. Lifetime

Figure 3 shows the results from six lifetime experiments with the lifetimes of the IMLs ranging between 51 and 123

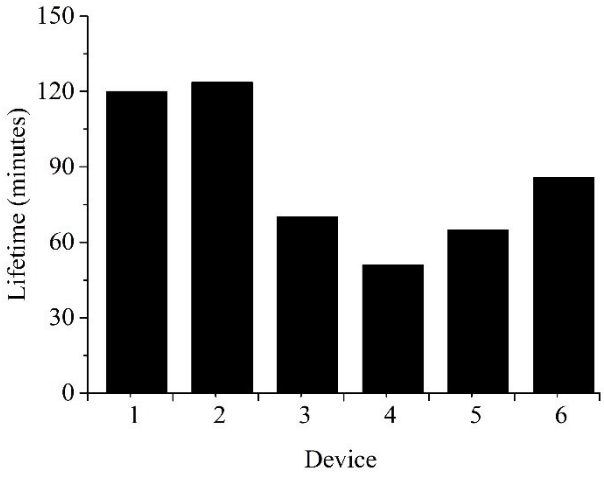

Figure 3: Lifetimes of the IMLs

minutes, with the average lifetime being 84 minutes. The low yield of this layout (figure 1) implies that weak points, or latent defects, exist in the dielectric (most likely the top insulator). When the electrode failed it displayed no steady-state response and high currents similar to those observed with electrodes which never functioned in the first place.

IV. Reduced Critical Area Layout

A. Yield

The CA of a microelectronic structure is the area, in which the presence of a defect would lead to device failure [17]–[20]. Therefore, reduction of the CA is an effective way of improving device yield [17]–[20]. In the case of the electrodes presented, the CA of the top dielectric is the area of metal underlying the top insulator. If a defect were to be located in this area, additional metal would be exposed to the environment, resulting in higher than expected currents. This corresponds with the observed behaviour of the failed IMLs described above. As a consequence, the layout was modified to the form shown in figure 4. The electrode metal layer now consists of a 150 µm wide interconnect between the contact pad and microelectrode. This equates to a 97.3% decrease in critical area of the top dielectric.

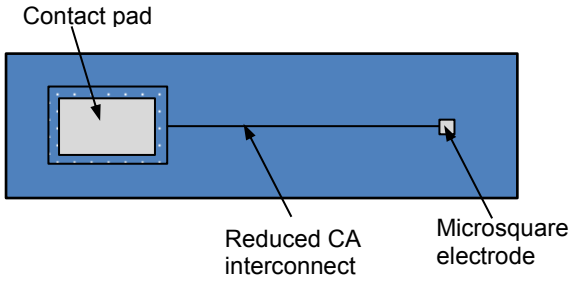

Figure 4: A schematic top-down layout of reduced CA device. The size of the microsquare electrode has been exaggerated for clarity.

The microelectrode design with Reduced CA (RCA) layout demonstrated an increased yield of 60% (n = 41). However, this still leaves a significant number of non-functional electrodes. Again, visual inspection of the microelectrode insulation showed no obvious difference between those that did and did not function, and hence revealed no indication of the failure mechanism. This motivated the design of test structures to help determine the cause of these failures.

B. Lifetime

In order to assess the effect of CA reduction on lifetime, the RCAs were subjected to the same lifetime tests as the IMLs. Figure 5 compares the measured lifetimes of the RCAs against the IMLs. It can be observed that the average lifetime increased from the 1.4 hours to 16.5 hours. The spread of results was very large, with lifetimes either being upwards of 25 hours or grouping around 3 hours. This suggests that microelectrode lifetime is still controlled by latent defects rather than intrinsic material failure. Another cause for device failure could be the variability in, or contamination of, the LKE environment. This is unlikely as the salt was only changed once during the experiments presented in figure 5. The seal of the cell was also checked daily (failure of which could lead to oxygen and/or water ingress) and did not show any appreciable change. However, all the RCAs showed higher lifetimes than the IMLs, indicating that reducing the CA has had a positive impact on microelectrode lifetime as well as yield.

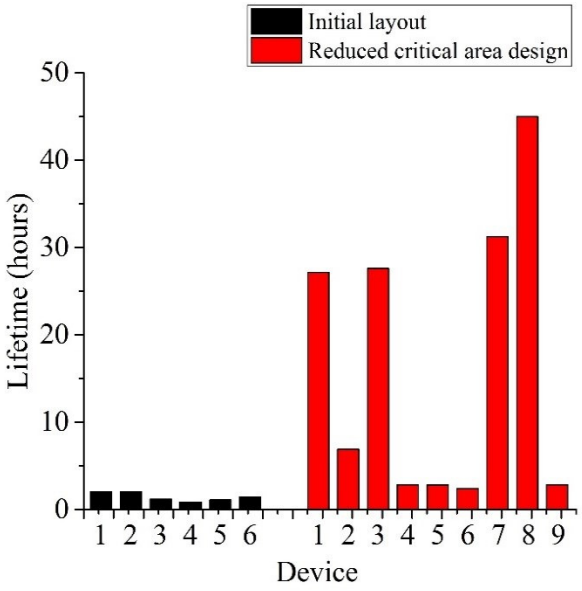

Figure 5: Lifetimes of the reduced critical area design compared against those of the initial layout.

V. Design of Test Structures

Despite the improved yield of the RCA design, a high number of non-functional devices remained. Therefore, test structures were designed to investigate the causes of device failure and to quantify defectivity in the top insulator. These structures are shown schematically in figure 6 (a) and consist of metal electrode plates with a range of areas, covered by an overlying dielectric. This set of structures enables the quality/defectivity of the dielectric on a fixed, largely planar surface to be monitored. Clearly, quantifying the contribution of the protective coating to the electrode's yield and lifetime is of considerable interest.

As defects had been observed at the point where the dielectric covered the step of the electrode metal layer, a comb test structure, shown schematically in figure 6 (b), was designed to quantify the problem and thereby provide the data required to optimise the process.

Electrical connections to the Si substrate were also made to detect defects in the underlying SiO_2 layer which insulates the electrode metal from the underlying Si substrate. In addition to these application-specific structures, standard test structures to measure stress, sheet resistance and linewidth were included in the mask design and figure 7 shows the full mask layout.

VI. Fabrication of Test Structures

The test structures were fabricated by first growing a 500 nm thick thermal SiO_2 layer on 4" (100) p-type Si wafers. A 20 nm TiN adhesion layer was sputter deposited, followed by the 200 nm W layer. Both layers were patterned and dry etched to form the metal plates, interconnects, and contact pads.

A 500 nm top insulator of LPCVD Si_3N_4 was then deposited to provide the top insulation layer that protects the metal from the MS. Openings in the Si_3N_4 were patterned and etched to create contact pads and the structures were then diced, ready for testing.

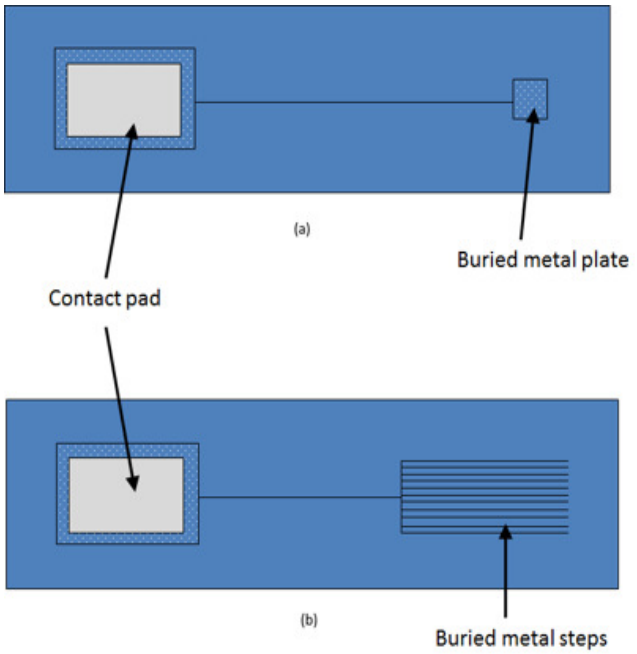

Figure 6: (a) Layout of the test structures to provide information on electrode size and yield. The structures consist of a bond pad connected via narrow thin metal interconnect to metal plates of areas: 0.25 mm², 1 mm², 4 mm², and 16 mm². (b) Test structures for monitoring dielectric step coverage integrity. A contact pad is connected to a series of 10 µm wide metal strips set 25 µm apart.

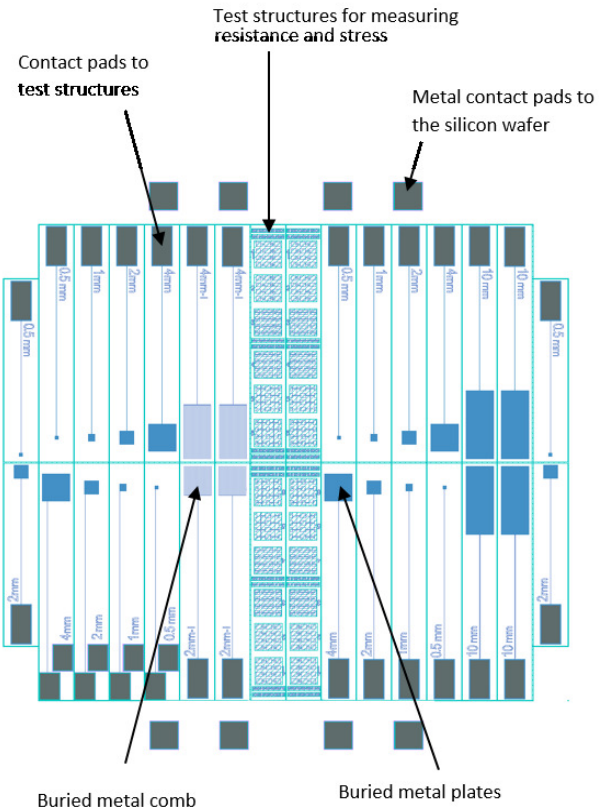

Figure 7: Layout of the test structure photomask. Exposed metal is in grey while metal covered by insulator is in blue.

VII. Test Structure Results

The test structures have been designed to be dipped in the MS at 450°C until the metal plate or comb is fully submerged. A potential was applied and the currents were recorded on structures with metal plates of areas: 0.25 mm², 1 mm², 4 mm², and 16 mm². It should be noted that these areas are only valid for determining the effectiveness of the top Si_3N_4 insulator and assume no other conduction paths.

All the different variants of the test structure were characterised in the experimental set up described in section II. To locate the sites of dielectric defects 18 mg (5 mM) of AgCl was added to the MS and the applied potential set to -0.46 V, the potential at which silver plates according to the reaction:.

$$Ag^{+}_{(solv)} + e^{-} \rightarrow Ag_{(s)} \qquad (1)$$

This approach identifies the location of dielectric failure as the silver will electroplate on the surface of any electrode metal exposed on the test structure. The measurement involves applying a potential for 15 minutes, and given that all the underlying metal should be completely passivated, any current passed that is not associated with capacitive charging, indicates exposed metal, and hence a defect (or defects) in the dielectric.

A. Test structure performance

The average current (of three structures) for the four metal plate sizes is shown in figure 8. What can be immediately seen from these results is that the average currents are non-zero, implying Ag^{+} ions are reaching the buried metal in at least some of the three structures. It can also be noted that the currents do not scale with area, indicating they are most likely due to randomly occurring defects rather than a fundamental

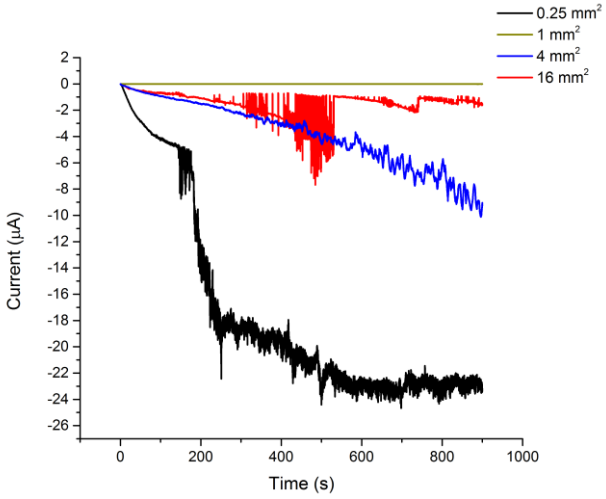

Figure 8: Average current vs time plots over 15 minutes for each area of metal plate studied. N = 3 for each size of test structure.

intrinsic property of the Si_3N_4 dielectric, which was the initial suspect. This conclusion is also supported by a large variation

in currents between these nominally identical samples. Figure 9 shows current responses from three individual 4 mm^2 buried metal plate test structures; these give currents varying across four orders of magnitude, ranging from 10^{-9} to 10^{-5} A. This suggests the presence of random defects. Although it would be expected that, with a high enough sample size, random defects would begin to scale with area. Only four out of the 18 test structures tested showed zero leakage current.

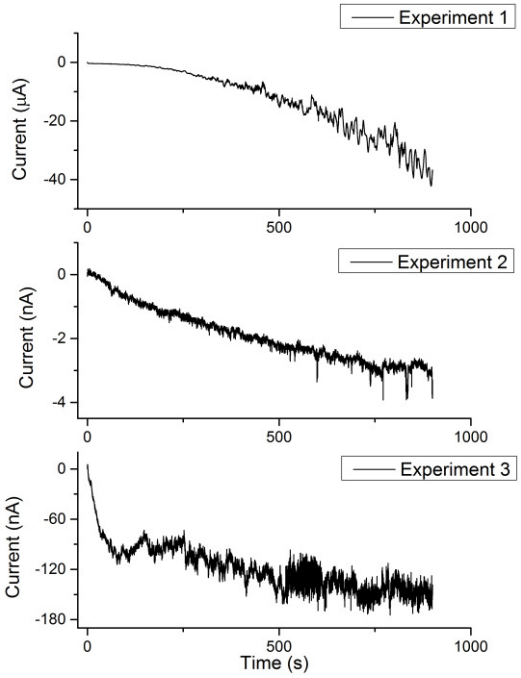

Figure 9: Current vs time plot of three individual experiments using 4 mm^2 edge length devices over 15 minutes.

B. Defect location

When the test structures were examined after removal from the MS, no silver was observed on the surface of the top insulator overlying the metal electrode. Figure 10 (a) shows this top insulator over the metal electrode before silver plating and (b) and (c) after the plating test. Although deposits of salt can be seen, there is clearly no evidence of any silver plated on the exposed Si_3N_4. This suggests the observed current is not flowing via this route.

Following further examination of the device, metallic deposits were observed on the edge of the exposed Si, around the perimeter of the chip. Figure 11 (a) shows the edge of the Si after dicing and (b) after the silver plating experiment, with (c) showing a more magnified image of this edge. To confirm that these deposits were the plated silver, a SEM with EDX (Energy-Dispersive X-ray) spectroscopy was used to image and measure the elemental composition of the deposits. A SEM image of such a deposit is presented in figure 12 along with its elemental breakdown in the inset, which confirms that the metallic deposits observed on the Si edge are silver.

It should be noted that at 450°C, Si behaves as a conductor, owing to the thermal excitation of intrinsic charge carriers into the conduction band. The silver plating observed on the Si suggests that defects are connecting the electrode metal to the underlying Si. Hence, the observed insulator failure is associated with the underlying thermal SiO_2 layer rather than

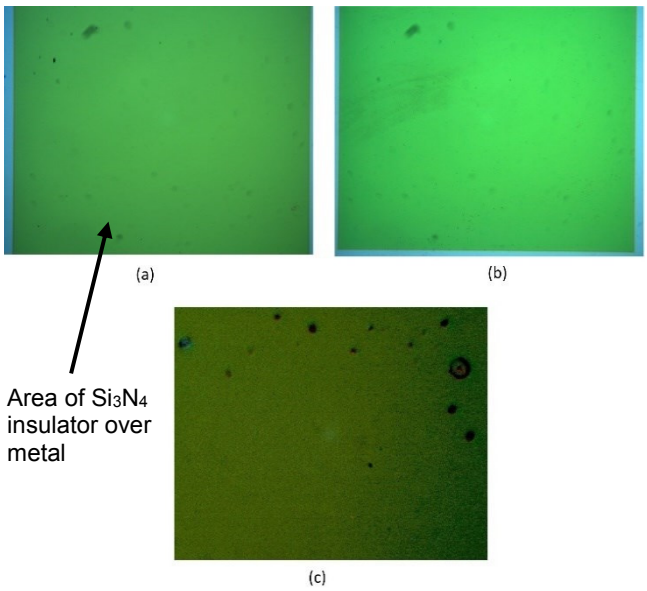

Figure 10: Optical images (Reichert-Jung Polyvar Optical Microscope) of the surface of the Si_3N_4 insulator over buried metal plates (a) before silver plating (× 10), (b) after silver plating (× 10) and, (c) after silver plating (x 100).

the exposed Si_3N_4 layer. At this point, it is important to remember that the defined plate areas described above (0.25 mm^2, 1 mm^2, 4 mm^2, and 16 mm^2) are only valid CAs if the top insulator is the source of the defects. Given the defects actually arise in the underlying SiO_2 layer, the CAs under examination increase to ~ 18.9 mm^2, 19.6 mm^2, 21.6 mm^2, and 34.7 mm^2 respectively. The reason for this is that the CA now includes the contact pad and interconnect as well as the

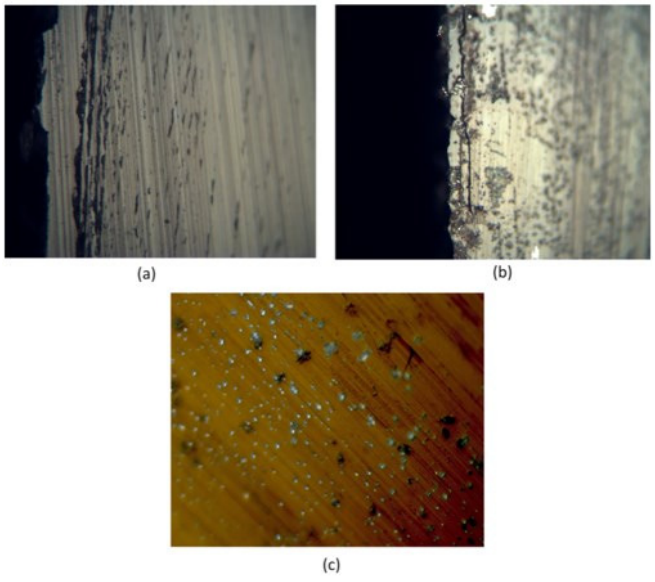

Figure 11: Optical images (Reichert-Jung Polyvar Optical Microscope) of the surface of the Si perimeter around the test structure chip (a) before silver plating (× 40), (b) after silver plating (× 40), and (c) after silver plating (× 100).

metal electrode plate.

Another possible mechanism for the observed silver plating on Si, is the SiO_2 exposed at the perimeter of the test structures after dicing is being chemically attacked/removed. This would enable the MS to compromise the insulation between the electrode metal and Si. To investigate this possibility, the perimeter of the test structure was examined using a focused ion beam to section and image the structure.

The image is shown in figure 13 and no deterioration of the SiO_2 layer was observed suggesting that this is not the mechanism responsible for shorting between metal and Si.

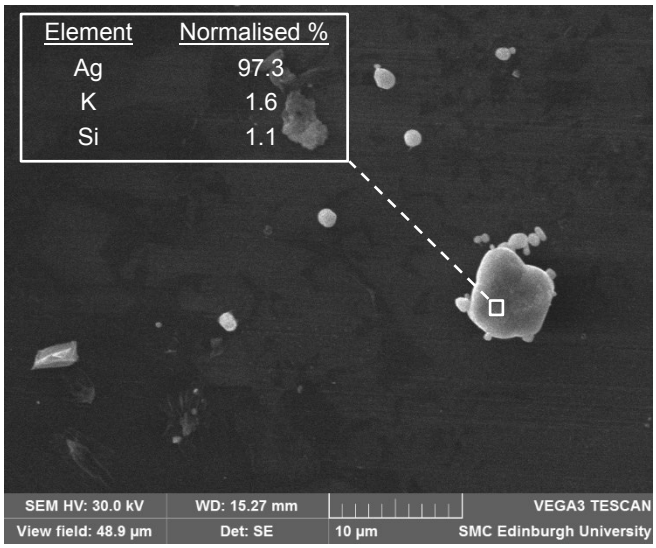

Figure 12: SEM image of silver deposits on the exposed Si perimeter of a test structure. Elemental composition of the highlighted area is presented in the inset, determined using EDX spectroscopy.

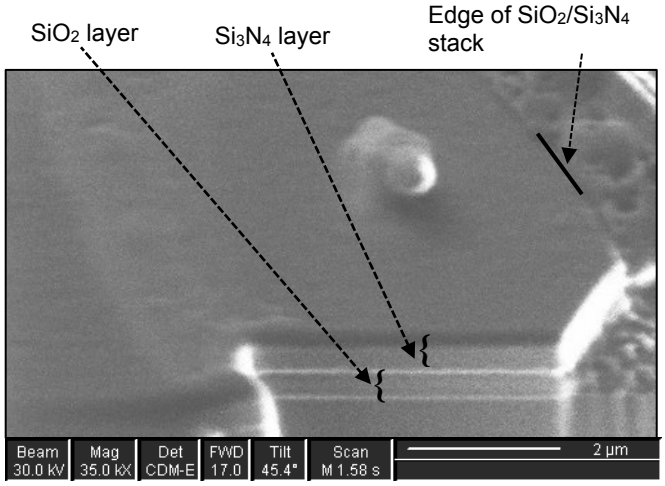

Figure 13: The edge of a test structure sectioned using a focused ion beam.

C. Buried metal step test structures

The test structures for dielectric integrity at step edges, shown in figure 6 (b), were also subject to the same silver plating test. These test structures also gave a non-zero current response with large current differences between devices of the same electrode area. Figure 14 shows a set of these steps (a) before and (b) after silver plating and it can be observed there is no silver plating along the edge of the metal step. However, silver deposits were identified on the exposed Si edge of the chip in a similar fashion to those observed on the buried metal plate structures suggesting a similar mechanism to the planar test structures.

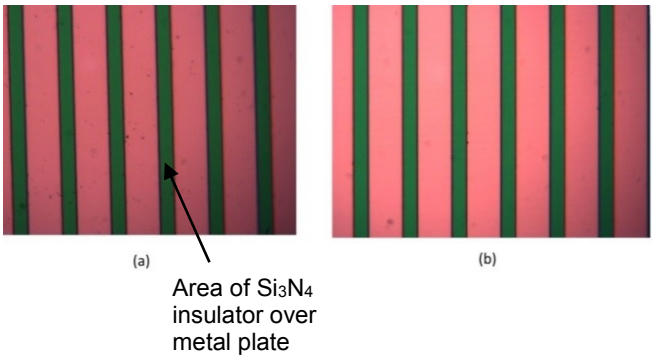

Figure 14: Test structure with top insulator covering metal tracks to monitor defects along step edges. (a) before silver plating (b) after 15 minutes of silver plating.

VIII. DISCUSSION

The test structures have identified the SiO_2 layer as a major source of device failures. Interestingly, this type of failure is not observed in aqueous room temperature studies, where the yield of microelectrode sensors was greater than 99% (thermally grown SiO_2 is an excellent dielectric with low defectivity). It should be noted that at MS operating temperatures, the Si is much more conductive than it is at room temperature [21] and it is the presence of mobile Li ions in the MS that presents a likely explanation for device failures [22]. Reference [23] identifies that Li ions diffuse very fast in both SiO_2 and Si (2.5×10^{-3} *exp* (0.656 *e/kT* cm^2s^{-1} [24]). In addition Li ions are known to insert itself into Si [25] and under an electric field Li ions are mobile in SiO_2. Their drift mobilities at low concentrations obey the Arrhenius relationship ($\mu_o=2.5\times10^{-3}$ cm^2s^{-1}, $E_A=0.104$ eV) in a similar manner to K ($\mu_o=4.\ .5\times10^{-4}$ cm^2s^{-1}, $E_A=0.47$ eV) and Na ($\mu_o=3.52\times10^{-4}$ cm^2s^{-1}, $E_A=0.44$ eV) ions, which were historically a major cause of problems in the gate oxide of MOS devices [26]. This strongly suggests that the SiO_2 does not provide a barrier to Li ions, and this contributes to electrode failures.

As mentioned above, metal contacts to the Si were included on the mask layout to test for any electrical connection between the Si and the W electrode metal. A value of 49.6 ± 1.2 MΩ was measured at room temperature between three pairs of Si contacts 5 mm apart. Before immersion in MS, the resistance between the contact pad and exposed Si edge at the top of the test structure chip (a distance of ~0.5 mm) was measured, and 5% of test structures gave values between 1.5 MΩ and 10 MΩ. Due to the high resistivity of Si at room temperature, only a small number of compromised test structures were identified before their immersion in MS.

The increase in current observed over time in the electrochemical measurements, implies that the resistance of the conduction paths decrease during their immersion in the salt, either by enlarging or becoming more numerous. It may also be the case that the increase in current was due to Ag plating on the Si, effectively increasing the electroactive area. However, this seems unlikely as the shape of the plots differ greatly, which would not be expected if the mechanism controlling them had been consistent. It was hoped that any change in the conduction paths could be measured after use

in the MS. However, the large increase in the resistance of the silicon when returned to room temperature masked the detection of any conduction paths formed in the SiO_2.

Figure 15 models the buried metal plate test structures as a series of resistors. The resistance associated with the SiO_2 defects can be determined by estimating the approximate values of the other components. The resistivity of Si at 450°C is ~1 Ωcm [21] with the metal track having a maximum resistance of 1,100 Ω. The solution resistance has been reported elsewhere as 2.5 Ω [27]. This estimate identified that 75% of the current leakages were in a range of 10 µA to 1 nA. These current levels are in the range of the currents recorded in electrochemical measurements with microelectrodes [7]–[9]. This means identifying small leakage currents when using microelectrodes is difficult in the majority of cases. In contrast, the test structures presented identify any current flow as being a failure in the insulation layers.

Figure 15: Resistors model for the buried metal plate test structure.

VIII. Incorporating Test Structure Findings Into Device Design

Despite defects in the SiO_2 layer being a major source of device failures, the stress relief it provides is necessary for robust device operation, as detailed in [7]. Hence it was not desirable to replace this layer. It was therefore decided to include an additional insulation/barrier layer between the electrode metal and SiO_2. The results presented above have indicated that the Si_3N_4 is effective in such a role and as a consequence, subsequent devices fabricated included a 100 nm thick layer of Si_3N_4 between the electrode metal and underlying SiO_2 as shown in figure 16.

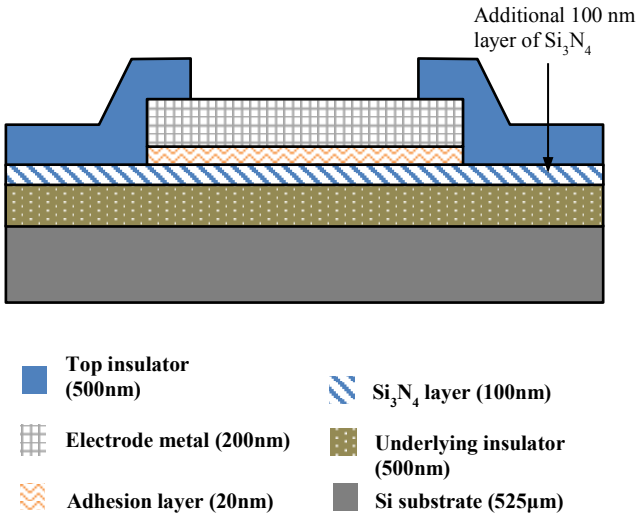

Figure 16: A transverse cross-section of the new device architecture through the contact pad showing the layers of the device, including the additional 100 nm layer of Si_3N_4 above the SiO_2 insulation layer. The thickness of the layers has been exaggerated for clarity.

The yield of 26 sensors with this structure characterised in MS, as previously described, was determined to be 77%. The improvement in yield is gratifying, and further confirms the SiO_2 insulation layer as the most likely source of failures. Additionally, only one out of the six failed electrodes demonstrated the higher than anticipated currents, symptomatic of shorting to the Si.

IX. Conclusion

This paper has described two methods of improving yield and lifetime of microfabricated sensors for the harsh environment of MS. Reduction of the metal area underlying the top insulator resulted in an increase in yield of ~15% and a significant improvement in lifetime, from 84 minutes to 16.5 hours. Despite this, the mechanisms controlling the remaining device failures were still unknown. A set of test structures were then presented, targeted at characterising microelectrode failures. This includes structures designed to assess the performance parameters of both dielectric layers (the underlying SiO_2 and covering Si_3N_4). These test structures have been used to help identify conductive paths through the underlying SiO_2 layer connecting the electrode metal to the conducting Si substrate at 450°C. The large variation in currents recorded suggests that this is most likely caused by a number of random failure sites. Interestingly these defect or weaknesses in the dielectric did not cause device failures under ambient aqueous measurement conditions, highlighting the challenge of working the MS environment. The test structures have indicated that the top insulation layer of Si_3N_4 insulated effectively, even over metal steps up to 200 nm.

The results from the test structures were used to implement a secondary Si_3N_4 insulation layer, between the electrode metal and the underlying SiO_2. The yield of these devices was determined to be 77%, demonstrating the test structures had successfully identified the main cause of microelectrode failure and allowing the development of an effective solution.

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