Control Design of a Neutral Point Clamped Converter Based Active Power Filter for the Selective Harmonic Compensation

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***Abstract*—This paper presents the control of an active power filter (APF) based on a 3-phase, 3-level neutral point clamped (NPC) converter with selective harmonic compensation. To achieve the selective harmonic compensation, the APF use several synchronous rotatory frames, which are rotating at the angular frequency and sequence of their respective harmonics, to detect and control the magnitude and angle of each individual harmonic using d and q variables. A three dimensional space vector modulator (3D-SVPWM) is used to generate the compensation currents. Due to its multilevel topology, the proposed active power filter can be used in high voltage power quality applications, such as sub-transmission and distribution levels. Simulation results are shown to validate the proposed solution and corroborate the proper function of the multilevel active power filter.**

Keywords: Active Power Filters, Neutral Point Clamped, Selective Harmonic Compensation, Overall Harmonic Compensation.

I. Introduction

Energy quality issues are an important aspect in the electrical energy consumption. That way, the harmonics in power systems results in several problems due to the wide application of power electronic equipment and nonlinear loads. Harmonic distortion causes several problems such as increased power losses, excessive heating in rotating machinery, electromagnetic interference in communication systems and operation failures of protection devices and electronic equipments [1]. Additionally, non-sinusoidal currents produce low power factor and high total harmonic distortion. Because of this, the modernization on transmission and distribution grids require new systems based on power electronic converters, with favorable characteristics such as, high efficiency, high power density, and low harmonic distortion, to suitable into the distributed generation and smart-grids concepts. A multilevel NPC converter topology can be used at higher power applications as APF. Thus, it can be applied in transmission, sub transmission, wind, photo-voltaic and mining system.

The APF performance depends on its controller which is divided in two parts. The first part determines the fundamental and harmonic reference current of the APF and maintains a stable DC bus voltage. Due to, several harmonic current detection methods, such as instantaneous reactive power theory, synchronous reference frame method, and supplying current regulation can be used [2–5]. These methods measure the harmonic currents either from the load or from the mains current to generate a reference harmonic current that will cancel out the grid currents at the point of common coupling. The second part is related to generate the compensating current into the AC mains. Therefore, several modulation techniques are implemented for driving the inverter. Among these methods, the pulse width modulation (PWM) techniques have been employed in APFs for harmonics elimination [6]. With the development of high speed microprocessors, space vector modulation (SVM) has become one of the most important PWM methods for three phase converters. The SVM based PWM methods have several advantages over carrier based ones such as lower total harmonic distortion (THD) and higher efficiency and higher available DC-link [7, 8].

The 3D-SVPWM is an useful algorithm used in multilevel level converters. This modulation technique optimizes the number of commutations and the number of calculations to get the switching sequence and the duty cycles [9–11].

This paper presents the control of an active power filter (APF) based on a 3-phase, 3-level neutral point clamped (NPC) converter with selective harmonic compensation. Figure 1 shows the APF with three level converter topology. To achieve the selective harmonic compensation, the APF use several synchronous rotatory frames, which are rotating at the angular frequency and sequence of their respective harmonics, to detect and control the magnitude and angle of each individual harmonic using d and q variables. A 3D-SVPWM is used to generate the compensation currents. The multi level

topology has the advantages to be used in high voltage power quality applications, such as sub-transmission and distribution levels. Simulation results are shown to validate the proposed solution and corroborate the proper function of the multilevel active power filter.

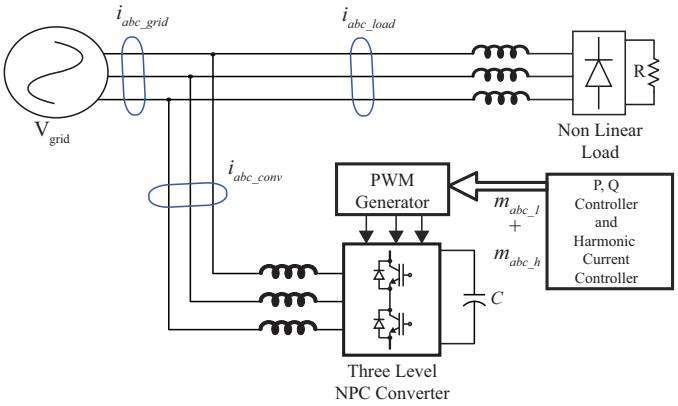

Fig. 1. Active power filter with three level inverter topology.

II. Three Level Converter

In a multilevel NPC converter topology, the voltages stress across the switches are lower and there are more available control vectors. Thus, the harmonic content of the converter is reduced if appropriate switching vectors are selected [12].

A three-phase three-level NPC converter is shown in Figure 2. The three phases have a common DC bus, divided by two capacitors into three levels. The voltage across each capacitor is $V_{DC}/2$; and the voltage stress across each switching device is limited to $V_{DC}/2$ through the clamping diodes. A three-level NPC converter is able to produce five levels of line to line voltage and three levels of phase voltage. This NPC converter reduces harmonics in both voltage and current output.

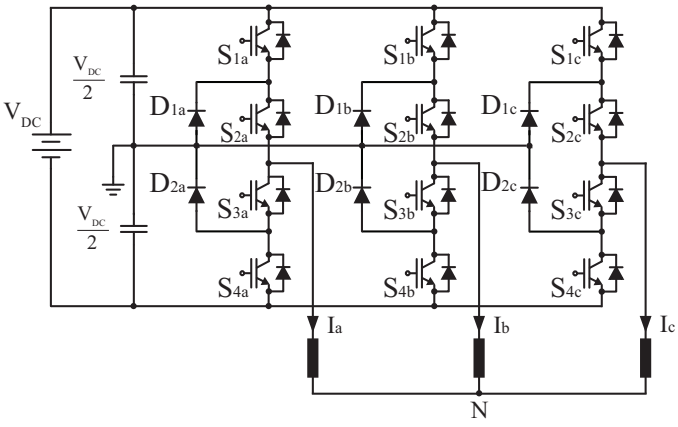

Fig. 2. Three-level NPC inverter topology.

Table I gives the switch states for phase *a*. Similar switching sequence will be derived for other phases by according the phase angle displacement. Here, S_{1a} and S_{3a} are complement of each other and S_{2a} and S_{4a} are complement of each other.

TABLE I
SWITCHING STATES OF THREE-LEVEL NPC CONVERTER

States of switches				Voltage Level
S_{1a}	S_{2a}	S_{3a}	S_{4a}	V_{aN}
1	1	0	0	+Vdc/2
0	1	1	0	0
0	0	1	1	-Vdc/2

State condition 1 means switch ON and 0 means switch OFF. Now, it is clear that an *m*-level diode clamped converter consists of *(m-1)* capacitors on dc bus, output phase voltage has *m*-levels and output line voltage has (2*m*-1)-levels. Each active switching device has to withstand a blocking voltage of Vdc/(*m*-1), even then clamping diode must have different voltage ratings for reverse voltage blocking. The number of diodes required will be 2(*m*-2) and the number of switching required will be 2(*m*-1) for each phase. Where *m* is the number of levels of the converter [8].

III. Harmonic Detection dq using synchronous reference frame

In the synchronous reference frame (SRF) algorithm, synchronous harmonic $d-q$ frame rotates at a frequency and sequence equal to the selected harmonic. Thus, in the harmonic $d-q$ frame, only the respective harmonic will be a dc-signal and all other frequencies including the fundamental will be ac-components. The detection of the respective harmonic results in removing the ac-signals with low pass filters (LPF). As seen in Fig. 3, the load current i_{abc_load} is measured and fed to the multiple synchronous reference frames. Each frame provides the $d-q$ components of each harmonic plus an ac signal. The ac signal of the harmonic $d-q$ components is filtered by a low pass filter based on the moving average architecture. The current of the inverter i_{abc_inv} is also fed to the multiple synchronous frames and the resulting $d-q$ signals are also filtered by a low pass filter with the same characteristics and delay as the $d-q$ load harmonic currents. The filtered $d-q$ harmonic currents from the load and the inverter are then fed to a PI controller. The PI controller generates, as a control action, a modulator signal that would produce harmonic currents of magnitudes that match those of the load, but in opposite polarity. In consequence, the load harmonic currents would cancel out with the inverter harmonic currents at the point of common coupling [5, 13].

In addition, a limiter is added after every PI regulator in order to ensure that the harmonic currents never increase beyond their allowed range. Otherwise, inverter voltage references may become greater than the maximum voltage allowed by the DC capacitor. This produce saturation in the modulator

signal which in turn produces unwanted harmonic content. The main advantage of a selective harmonic compensation (SHC) mode over an overall harmonic compensation (OHC) mode is the ability to select individual harmonics to compensate. Therefore, SHC systems can be installed in parallel to cancel individual harmonics from separate units.

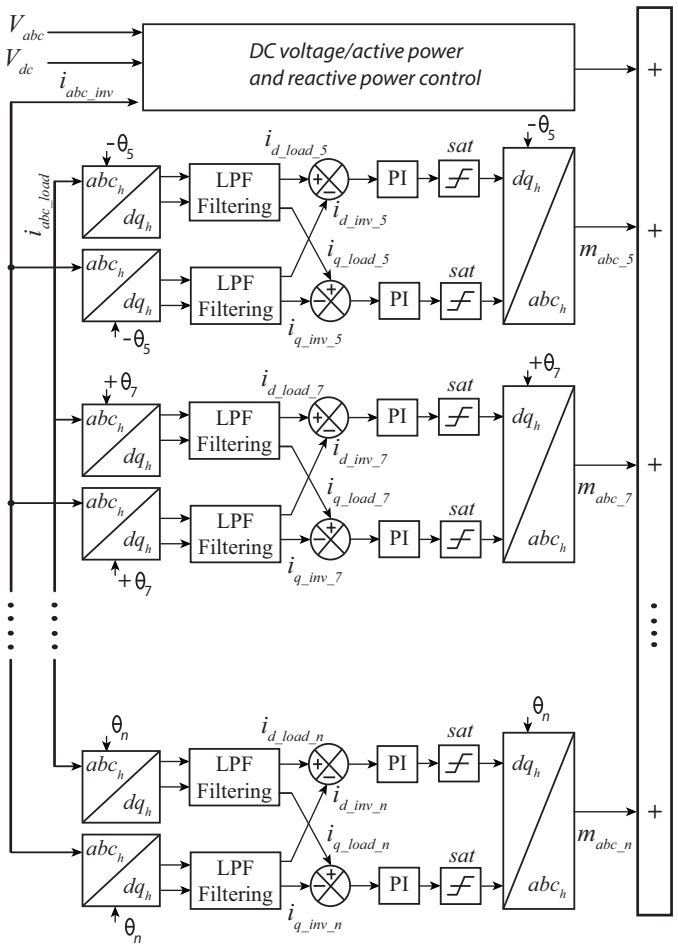

Fig. 3. Selective harmonic compensation based synchronous reference frame.

IV. Active Power Filter Controller

The overall APF selective harmonic controller is shown in Figure 4. A vectorial control is carried out to achieve the selective APF controller, three phase currents and voltages are described as vectors in a complex reference frame, called α-β frame. A rotating reference frame synchronized with the ac-grid is also introduced. As the $d-q$ frame, is synchronized to the grid, the voltages and currents occur as constant vectors in the $d-q$ reference frame in steady state. The value of the angle θ is calculated by using a synchronization technique phase locked loop (PLL). The PLL information is used to synchronize the turning on/off of the power devices, calculate and control the active/reactive power flow by transforming the feedback variables to a reference frame suitable for control purposes [14].

As the vector control technique offers decoupled control of

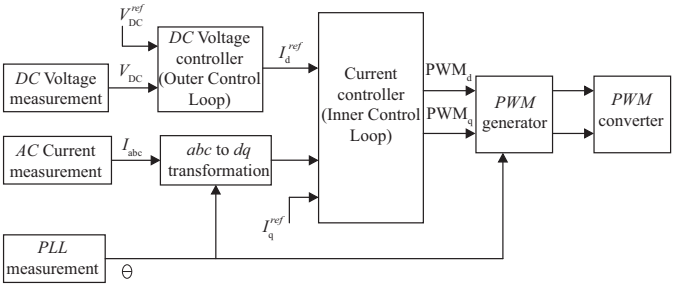

Fig. 4. Overall Scheme of Vectorial Control

active and reactive power and a fast dynamics, it makes the realization of system control in form of cascade structure possible, with two PI control loops in cascade. Meaning this, an outer control loop and inner current control. The control system is based on a fast inner current control loop controlling the ac current. The ac current references are supplied by outer controllers. The inner and outer controller are described below.

A. Inner and Outer Controller

The inner current control loop can be implemented in the $d-q$ frame, based on the basic relationship of the system model. A general inner current control block is represented in Figure 5.

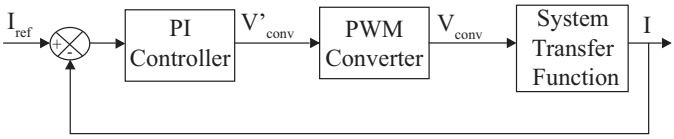

Fig. 5. General block diagram of inner current control.

Inside the current control block, there are two PI regulators, respectively for d and q axis current control. They transform the error between the comparison of d and q components of current into voltage value. In order to have a detail overview of the control system, each block of the control system is discussed as below.

The representative equation of the PI regulator is:

$$R(s) = K_p + \frac{K_i}{s} = K_p.\left(\frac{1+T_i.s}{T_i.s}\right) \tag{1}$$

considering the $I(s)$ and $I_{ref}(s)$ and PI controller block,

$$\{I_{ref}(s) - I(s)\}\left(K_p + \frac{K_i}{s}\right) = V'_{conv}(s). \tag{2}$$

The PWM converter block is considered as an ideal power transformer with a time delay. Thus the PWM block is given as,

$$V'_{conv}(s).\frac{1}{1+T_a.s} = V_{conv}(s) \tag{3}$$

where $T_a = T_{switch}/2$.

Considering the converter system connected to grid, as seen in Figure 1, the phase voltages and currents are given by the equation,

$$V_{abc} = R.i_{abc} + L\frac{di_{abc}}{dt} + V_{abc,conv} \tag{4}$$

where V_{abc} and i_{abc}, are ac voltages and currents respectively, and $v_{abc,conv}$ is the voltage converter. R and L are the resistance and filter inductance between the converter and the ac system. Using the abc to $d-q$ transformations, the 3-phase currents and voltages converter are expressed in 2-axis $d-q$ reference frame, synchronously rotating at given ac frequency w as

$$V_d = R.i_d + L\frac{di_d}{dt} - \omega L i_q + V_{dconv} \tag{5}$$

$$V_q = R.i_q + L\frac{di_q}{dt} + \omega L i_d + V_{qconv} \tag{6}$$

Similarly on the output side,

$$I_{dc} = C.\frac{dV_{dc}}{dt} + I_L \tag{7}$$

As seen from equations (5) and (6) the equations in d and q axis have a similar form, for this reason only the d-axis equations is used for further analysis and control rule derivation. The inner loop current controllers for i_d, gives the output of V_d voltage reference signals, which fed to the converter. Using Equation (5),

$$V_{dconv} = (i_{dref} - i_d).\left(K_p + \frac{K_i}{s}\right).\frac{1}{1+sT_a} \tag{8}$$

The transformed $d-q$ voltage equations have the frequency induced terms, wLi_d and wLi_q, that produces a cross coupling between the d and q currents. This cross coupling term can be cancelled out algebraically in the control loops, enabling an independent control in d and q axis, respectively. With the compensation terms used for decoupling, the system input from converter is defined as

$$V'_{dconv} = -(i_{dref} - i_d).\left(K_p + \frac{K_i}{s}\right) + wLi_q + V_d \tag{9}$$

Equation (9) when substituted in Eqn. (3) and equated to equation (5), it gives,

$$L\frac{di_d}{dt} + Ri_d = V_{dconv} \tag{10}$$

by Laplace transformation the equation becomes:

$$s.I_d(s) = -\frac{R}{L}.I_d(s) + \frac{1}{L}.V_{dconv}(s). \tag{11}$$

Thus,

$$I_d(s) = \frac{1}{s.L+R}.V_{dconv}(s) \tag{12}$$

Hence the system transfer function is:

$$G(s) = \frac{1}{R}.\frac{1}{1+s.\tau} \tag{13}$$

Where the time constant is defined as $\tau = L/R$.

Since the control of the inverter fundamental currents and harmonic is carried out by dc signals, the modulus optimum tuning criteria can be used to select the constants of the PI controllers. If considering the cross coupling terms the $d-q$ current equations and the grid voltage components are disturbances, not present during the calculation of the $d-q$ current control, but instead being numerically compensated by a feed-forward loop in the main harmonic current control loop, then, the plant for $d-q$ fundamental and harmonic currents is:

$$G(s) = \frac{i_{d\_h}(s)}{V_{dconv\_h}(s)} = \frac{i_{q\_h}(s)}{V_{qconv\_h}(s)} = \frac{i_h(s)}{V_{conv_h}(s)} \tag{14}$$

where V_{dconv_h} and V_{qconv_h} are the $d-q$ components of the average voltages generated by the inverter for the harmonic h, i_{d_h} and i_{q_h} are the $d-q$ components of the current between the inverter and the grid for the harmonic h.

From (13) it can be seen that the system has a stable pole at $-R/L$. This pole can be cancelled with the zero provided by the PI controller, where Kp_{conv_h} and Ki_{conv_h} are the proportional and integral constants of the h harmonic PI current controller. Thus, choosing $Ki_{conv\_h}/Kp_{conv\_h} = R/L$ and $Kp_{conv\_h}/L = 1/\tau_{conv\_h}$, where τ_{conv_h} is the time constant of the closed-loop system.

The power balance in the system is achieved through the dc voltage controller. The general diagram for the outer controller is shown in Figure 6. The diagram consists of a PI controller, the inner controller and the power transfer function of the capacitor.

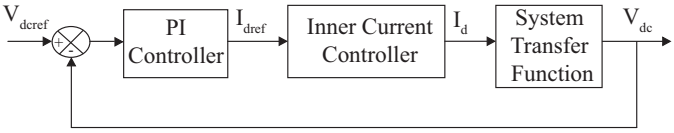

Fig. 6. General block diagram of outer dc voltage control.

The representative equation of the PI voltage regulator is:

$$R(s) = K_{pv} + \frac{K_{iv}}{s} = K_{pv}.\left(\frac{1+T_{iv}.s}{T_{iv}.s}\right) \tag{15}$$

where the subscript v denotes the voltage regulator. For the PI controller block for outer voltage control,

$$\{V_{dcref}(s) - V_{dc}(s)\}\left(K_{pv} + \frac{K_{iv}}{s}\right) = i_{dref}(s) \tag{16}$$

The power balance relationship between the ac input and dc output is given as,

$$P = \frac{3}{2}(V_d.i_d + V_q.i_q) = V_{dc}.I_{dc} \tag{17}$$

where V_{dc} and I_{dc} are dc output voltage and current respectively. Using the condition $V_q = 0$, the relation between i_d and I_{dc} can be written as,

$$I_{dc} = \frac{3}{2}.\frac{V_d}{V_{dc}}.i_d \tag{18}$$

This defines the value of the current gain to be used from dc current to input current or viceversa. Substituting this value in (7), we get,

$$C\frac{dV_{dc}}{dt} = \frac{3}{2}.\frac{V_d}{V_{dc}}.i_d - I_L \tag{19}$$

It is possible to observe that the dc link current equation is a nonlinear equation. For analyzing the stability of a nonlinear system in the neighbourhood of a steady state operating point, it is necessary to linearize the system model around the operating point and perform linear stability analysis. The reference point for linearization is found by specifying reference input, $V_{dc,ref}$ for the nonlinear model.Consequently the linear expression becomes,

$$C\frac{d\Delta V_{dc}}{dt} = \frac{3}{2}.\frac{V_{d,0}}{V_{dc,ref}}.\Delta i_d \tag{20}$$

By Laplace transformation it is:

$$\frac{\Delta V_{dc}(s)}{\Delta i_d(s)} = \frac{3}{2}.\frac{V_{d,0}}{V_{dc,ref}}.\frac{1}{s.C} \tag{21}$$

The dc link voltage controller controls the capacitor current so as to maintain the power balance. Hence under balanced conditions, $Ic = 0$. That is, $I_{dc} = I_L$. Thus, the reference value of i_d should be,

$$i_d = \frac{2}{3}.\frac{V_{dc}}{V_d}.I_{dc} \tag{22}$$

The overall control block diagram of the dc voltage controller based on equations (16)-(22) is as shown in Fig. 7. The inner

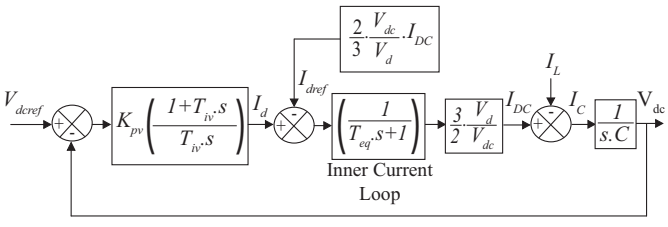

Fig. 7. Closed loop control diagram of dc voltage controller

control time response is selected in $1ms$, hence, the outer control is selected 10 times this value in order to get a good performance of the controller.

B. 3D-Space Vector Modulator

The 3D-SVPWM algorithm optimizes the commutation sequence using four state vectors, which are adjacent to the reference vector, and determine the respective commutation times of the three-level converter switching devices. The reference vector is represented by means of four vertices of a tetrahedron which are the state vectors of the sequence switching. Figure 8 shows a tetrahedron in a sub-cube with corresponding state vectors.

The computational load is independent of the number of levels of the converter. In addition, the algorithm provides the switching sequence that minimizes the total harmonic distortion (THD) and the number of switchings of the semiconductor devices.

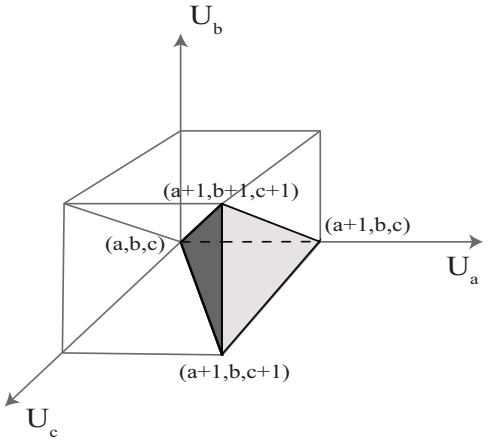

Fig. 8. Tetrahedrons in a sub-cube with corresponding state vectors.

Figure 9 shows the complete block diagram of the algorithm. This algorithm is well suited due to the good performance

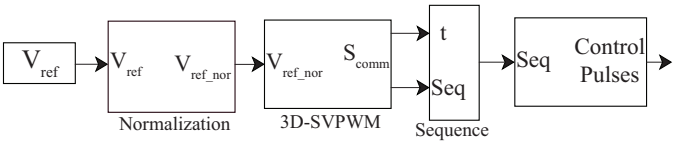

Fig. 9. Block diagram of 3D-SVPWM algorithm.

for multilevel converters and it can be used for converters with more levels applying a minimum of changes in its programming. The matrix with four commutation vectors and the corresponding switching times are defined by:

$$Sec = \begin{pmatrix} S_a^1 & S_a^2 & S_a^3 & S_a^4 \\ S_b^1 & S_b^2 & S_b^3 & S_b^4 \\ S_c^1 & S_c^2 & S_c^3 & S_c^4 \end{pmatrix} \tag{23}$$

$$t = \begin{pmatrix} S_1 \\ S_2 \\ S_3 \\ S_4 \end{pmatrix} \tag{24}$$

V. Simulation Results

The simulations results of the proposed APF are described in this section. A three-phase rectifier as nonlinear load has been connected to a 100 V, 60 Hz grid through filtering inductors. The APF operates at a switching frequency of 10 kHz and regulates its internal DC voltage to 250 V. Figure 10 shows the grid current effect in phase a when the compensator is enable in 0.5s. Applying this selective harmonic compensator the total harmonic distortion (THD) has been reduced from 22.5% to 4.3%.

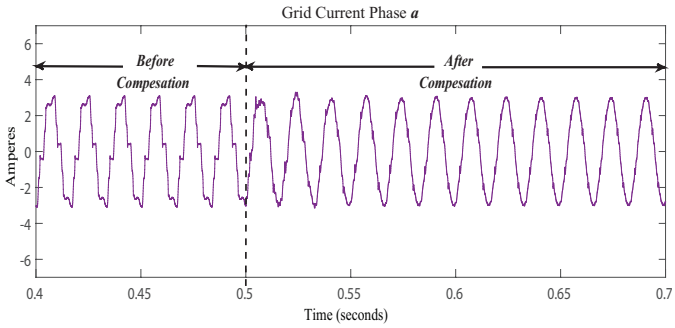

Fig. 10. Grid current in phase a before and after compensation.

In Figure 11 is shown the three phase currents, before and after the compensation.

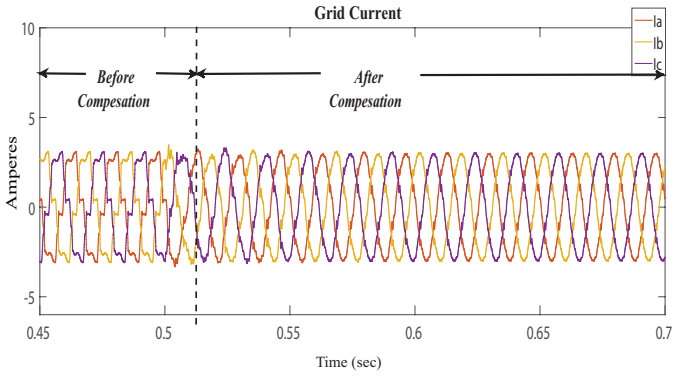

Fig. 11. Grid three phases currents before and after compensation.

In order to see the result of the individual harmonic control capability of the APF, Figure 12, show the effect of each harmonic compensated and the corresponding THD when this is activated.

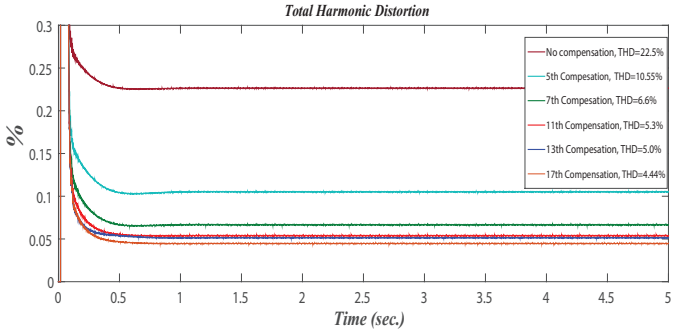

Fig. 12. Total harmonic distortion for each harmonic selected.

VI. Conclusion

This paper presents the design and control of an active power filter based on 3-level NPC converter for selective harmonic compensation using synchronous reference frames. The controller for the selective harmonic compensation uses synchronous reference frames and a low pass filter in order to enables the control of individual harmonics using $d-q$ signals. Therefore, the derive control rules can be selected and applied, and the harmonic compensation is carried out without steady state error.

The use of three level converters and 3D-SVPWM provide an accurate generation of the harmonic currents with a lower harmonic content. Thanks to this, the active power filter based on the three level converter is an attractive application for power quality improvement application in distribution and sub transmission systems.

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