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Exploitation of Digital Filters to Advance the Single-Phase *T*/4 Delay PLL System

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***Abstract*—With the development of digital signal processing technologies, control and monitoring of power electronics conversion systems have been evolving to become fully digital. As the basic element in the design and analysis phases of digital controllers or filters, a number of unit delays (z^{-1}) have been employed, e.g., in a cascaded structure. Practically, the number of unit delays is designed as an integer, which is related to the sampling frequency as well as the ac signal fundamental frequency (e.g., 50 Hz). More common, the sampling frequency is fixed during operation for simplicity and design. Hence, any disturbance in the ac signal will violate this design rule and it can become a major challenge for digital controllers. To deal with the above issue, this paper first exploits a virtual unit delay (z_v^{-1}) to emulate the variable sampling behavior in practical digital signal processors with a fixed sampling rate. This exploitation is demonstrated on a *T*/4 Delay Phase Locked Loop (PLL) system for a single-phase grid-connected inverter. The *T*/4 Delay PLL requires to cascade 50 unit delays when implemented (for a 50-Hz system with 10 kHz sampling frequency). Furthermore, digital frequency adaptive comb filters are adopted to enhance the performance of the *T*/4 Delay PLL when the grid suffers from harmonics. Experimental results have confirmed the effectiveness of the digital filters for advanced control systems.**

I. Introduction

In grid-connected applications, the injected grid current should be synchronized with the grid voltage [1], [2]. For three-phase systems, synchronization is typically achieved in the stationary reference frame, while unbalances and faults in the grid voltage presenting positive- and negative-components challenge the synchronization [3], [4]. Due to the limited number of variables in single-phase systems (i.e., only grid voltage), synchronization becomes even more challenging in single-phase systems. Many attempts have thus been made to synchronize the injected grid current with the grid voltage for single-phase systems [4]–[6]. Among the prior-art solutions, Phase Locked Loop (PLL) techniques have attracted more attention in recent years, where a virtual voltage in quadrature with the real grid voltage is created in order to achieve the synchronization.

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For instance, a Second Order Generalized Integrator (SOGI) has been widely studied and recognized as a promising solution to single-phase PLL systems [7], due to its high immunity to harmonics and fast dynamics. However, in the case of severe low-order harmonic distortions, the performance of SOGI-based PLL systems will be degraded [8], [9]. Hence, multiple harmonic cancellation cells are introduced in [8] in order to improve the harmonic attenuation capability at the cost of complexity. This is the reason - more focus has been put on structural simplification in [8]. Nevertheless, the major task of synchronization in single-phase systems is to "filter" the measured grid voltage, and introduce a phase-shift of 90° to create the virtual voltage. Following, a Park transformation is applied to extract the phase error used for synchronization.

Along with the development of digital micro-controllers, e.g., Digital Signal Processors (DSPs), and the digital signal processing technology, many other PLL systems have been proposed and implemented in digital controllers [10]–[14]. In terms of simplicity, a zero crossing detector and/or a *T*/4 Delay unit can be used to create the virtual voltage, where *T* is the nominal period of the grid voltage [8], [13]–[15]. However, measurement noise makes it difficult to achieve exact zero crossing detection, where advanced digital filters can be employed. The *T*/4 Delay unit is easy to implement in a digital controller with a fixed sampling period T_s. Specifically, by cascading an integer number of unit delays (i.e., z^{-N}), the measured voltage can be shifted by 90° in theory. Notably, the number N is related to the fundamental period of the grid voltage (denoted as T_n), i.e., $N = \frac{T_\mathrm{n}}{4T_\mathrm{s}}$. It is thus clear that if there are variations in the grid voltage frequency (T_n is varying), the delay z^{-N} can not ensure an exact phase-shift of 90°. As a consequence, the frequency and phase estimated by the PLL will be affected. In addition, all the harmonics in the grid voltage will also be shifted but not eliminated, which will give errors in the output.

In order to tackle the above issues, this paper exploits the digital filters implemented with unit delays to advance the *T*/4 Delay PLL, where a Virtual Unit Delay (VUD) is introduced in § III. In contrast to the conventional variable sampling frequency solutions, the introduced VUD based on first-order linear interpolation polynomial is simple but effective, and it enables frequency-adaptive single-phase *T*/4 Delay PLL

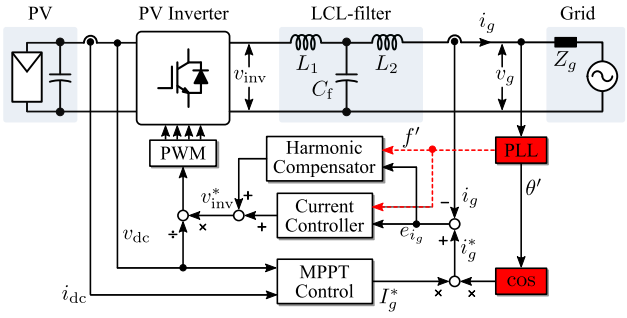

Fig. 1. General control structure of a single-phase grid-connected PV inverter system with an LCL filter (PWM - Pulse Width Modulation; MPPT - Maximum Power Point Tracking), where f' is the output frequency of the PLL and $\theta' = 2\pi f' t$ is the grid voltage phase.

system. In addition, to better eliminate the impact of grid voltage distortions on the PLL performance, a frequency-adaptive comb filter has also been incorporated into the *T*/4 Delay PLL. Experiments have been carried out to verify the theoretical analysis, and the results are provided in § IV. Finally, concluding remarks are given.

II. Control of Single-Phase Inverters

Fig. 1 gives an example of a single-phase grid-connected PV inverter system, where the "role" of synchronization in control is highlighted. It can also be seen in Fig. 1 that the control system contains two cascaded loops. Namely, the outer loop achieves the Maximum Power Point Tracking of the PV panels, and gives also the amplitude reference of the grid current [16]. Then, the reference grid current is generated by multiplying the amplitude reference and $\cos\theta'$ calculated from the PLL output estimated phase θ', as shown in Fig. 1. Herein, the synchronization between the reference grid current i_g^* and the grid voltage v_g is accomplished. Finally, the grid current i_g will be shaped as closely as possible to the synchronized reference grid current i_g^* by the inner control loop.

Note that a harmonic compensator is also plugged in parallel with the current controller. This is to improve the quality of the feed-in grid current and maintain the distortion level below the limits in relevant grid-connection standards [17]. A proportional resonant controller is employed as the current controller [16]. Multiple resonant controllers and a repetitive controller can be adopted to compensate the harmonics [1], [2], [4], but these controllers are frequency-dependent. Hence, as it is shown in Fig. 1, in order to enhance the frequency adaptability [2], the PLL output frequency f' is fed to these controllers that are usually implemented in digital signal processors. Additionally, the use of an LCL filter can also improve the current quality to some extent.

III. Advanced *T*/4 Delay PLL with Digital Filters

As indicated in Fig. 1, synchronization is an important task in grid-connected applications. Considering the implementation complexity in digital signal controllers, this section discusses the single-phase digital *T*/4 Delay PLL and different schemes exploiting digital filters are introduced in order to advance the PLL.

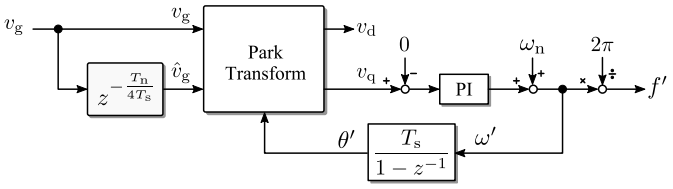

Fig. 2. Digital implementation of the conventional single-phase *T*/4 Delay PLL system (PI - Proportional Integral controller).

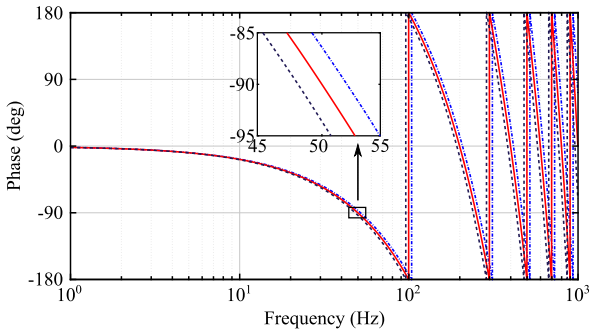

Fig. 3. Phase response of the *T*/4 Delay unit with $f_{\rm s}$ = 10 kHz, where the grid fundamental frequency has been changed by ±2 Hz and the nominal grid frequency is 50 Hz (red solid line).

A. Conventional Digital T/4 Delay PLL

Fig. 2 shows the digital implementation of the conventional *T*/4 Delay PLL, where " ′ " denotes the estimated variables by the PLL. As stated previously, the *T*/4 Delay unit will introduce a phase-shift of 90° to the grid voltage v_g only when the grid voltage is harmonic-free and $N_{\rm n} = \frac{T_{\rm n}}{4T_{\rm s}}$ is an integer. In that case, the transfer function from the virtual voltage $\hat{v}_g$ to the real grid voltage v_g can be given as

$$\frac{\hat{v}_g}{v_g} = z^{-N_{\rm n}} = z^{-T_{\rm n} f_{\rm s}/4} \tag{1}$$

where $f_{\rm s} = 1/T_{\rm s}$ is the sampling frequency. Considering a fixed sampling frequency, the phase response of (1) is shown in Fig. 3. It can be observed that the phase-shift will be slightly deviated from 90°, meaning that the virtual voltage will not be in quadrature with the grid voltage. Consequently, the output of the Park transformation will contain errors. This impact can be quantified in the time domain as following.

Considering a grid voltage as $v_g(t) = V_m \cos(\omega t + \phi_0)$ with V_m being the grid voltage amplitude, ω being the grid voltage angular frequency and ϕ_0 is the initial phase ($\phi_0 = 0$ for simplicity), the virtual voltage $\hat{v}_g(t)$ can be expressed as

$$\hat{v}_g(t) = v_g(t - \frac{T_{\rm n}}{4}) = V_m \cos(\omega t - \omega \frac{T_{\rm n}}{4}) \tag{2}$$

According to Fig. 2, the outputs of the Park transformation can be obtained as

$$\begin{bmatrix} v_{\rm d}(t) \\ v_{\rm q}(t) \end{bmatrix} = \overbrace{\begin{bmatrix} \cos\theta' & \sin\theta' \\ -\sin\theta' & \cos\theta' \end{bmatrix}}^{T_{\rm p}} \begin{bmatrix} v_g(t) \\ \hat{v}_g(t) \end{bmatrix} \tag{3}$$

with $T_{\rm p}$ being the Park transformation matrix and $\theta' = \omega' t$ being the PLL estimated phase of the grid voltage.

Hence, the q-axis voltage $v_{\mathrm{q}}(t)$ used for synchronization is obtained as

$$\begin{aligned} v_{\mathrm{q}}(t) &= -\sin\theta' v_g(t) + \cos\theta' \hat{v}_g(t) \\ &= -V_m \sin\theta' \cos\theta + V_m \cos\theta' \cos(\theta - \tfrac{\omega T_{\mathrm{n}}}{4}) \end{aligned} \tag{4}$$

where $\theta = \omega t$ is the instantaneous grid phase angle. In the case of a nominal grid frequency (i.e., $\omega = \omega_{\mathrm{n}} = 2\pi/T_{\mathrm{n}}$),

$$\cos(\theta - \frac{\omega T_{\mathrm{n}}}{4}) = \sin\theta \tag{5}$$

Substituting (5) into (4) yields

$$v_{\mathrm{q}}(t) = V_m \sin\Delta\theta \approx V_m \Delta\theta \tag{6}$$

with $\Delta\theta = \int \Delta\omega dt$ being the phase error and $\Delta\omega = \omega - \omega'$. Since a Proportional Integral (PI) controller has been employed to regulate the phase error to zero, the output frequency and phase of the conventional *T*/4 Delay PLL are "locked" to those of the grid voltage, meaning that synchronization is achieved in normal grid conditions. In that case, the PI controller $G_{\mathrm{pi}}(s)$ can be designed based on the small signal model [4] as

$$G_{\mathrm{pi}}(s) = 0.28 + 7.36/s \tag{7}$$

which roughly results in the settling time being 100 ms for the closed-loop system.

However, the practical grid frequency may vary. In the case of a small deviation $\Delta\omega_g = \omega - \omega_{\mathrm{n}}$, the condition in (5) will not hold any more. When considering small frequency variations $\Delta\omega_g$ and according to (4), the q-axis voltage $v_{\mathrm{q}}(t)$ can be approximated as

$$v_{\mathrm{q}}(t) \approx \underbrace{V_m \Delta\theta - V_m \cdot \frac{\pi\Delta\omega_g}{4\omega_n}}_{\text{dc term}} \underbrace{- V_m \cdot \frac{\pi\Delta\omega_g}{4\omega_n} \cos(\theta' + \theta)}_{\text{ac term}} \tag{8}$$

which contains an ac component of twice the grid fundamental frequency (i.e., $\cos(\theta'+\theta)$). The ac term can not be completely mitigated due to the limited bandwidth of the closed-loop PLL system shown in Fig. 2, when the PI controller is adopted. Fig. 4 shows the steady-state performance of the conventional *T*/4 Delay PLL, where the nominal amplitude and frequency of the grid voltage are 325 V and 50 Hz, respectively. It can be observed that the output frequency f' contains harmonics of twice the grid fundamental frequency in the case of an abnormal grid frequency (i.e., f = 51 Hz). Furthermore, the q-axis voltage v_{q} will in that case also vary. The variation has a frequency of twice the fundamental grid frequency, and the amplitude is 5.1 V, which is in a close agreement with the theoretical calculations according to (6).

Additionally, in practice, the grid voltage v_g contains harmonics (typically, low-order odd harmonics). However, according to (1) and (3), both the *T*/4 Delay unit and the Park transformation unit has no filtering capability. Instead, the grid voltage harmonics after the Park transformation become high-order (even) harmonics that will pass to the PI controller. As a consequence, the output frequency f' will also be affected (i.e., it will contain harmonics). Fig. 5 exemplifies the impact of the grid voltage harmonics on the conventional *T*/4 Delay PLL. Clearly, efforts should be devoted to advance the *T*/4 Delay PLL with the above two considerations.

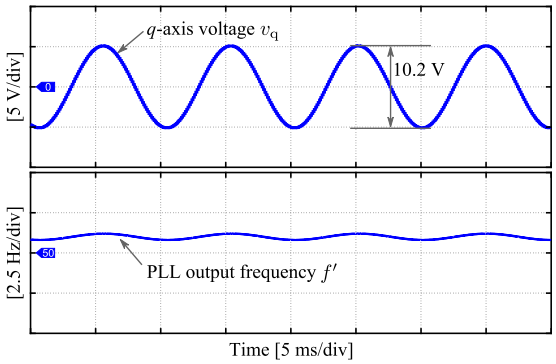

Fig. 4. Steady-state performance (simulation) of the conventional *T*/4 Delay PLL, where the sampling frequency is 10 kHz and the grid frequency is 51 Hz. The PI controller in (7) has been employed.

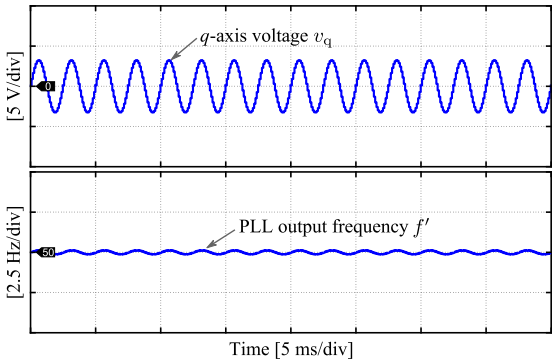

Fig. 5. Steady-state performance (simulation) of the conventional *T*/4 Delay PLL, where the sampling frequency is 10 kHz and the grid frequency is 51 Hz. The grid voltage contains low-order harmonics (i.e., 3rd-order: 2%, 5th-order: 2%, 7th-order: 0.5%, and 9th-order: 1.5%, leading to the total harmonic distortion: 3.2%). The PI controller in (7) has been employed.

B. Advanced T/4 Delay PLL Using A Virtual Unit Delay Filter

Considering a practical grid voltage with the fundamental period being denoted as T, the desired number of delays is calculated as $N = Tf_{\mathrm{s}}/4$, which can be fractional. It is thus common to round the number of delays N in the implementation. However, doing so will lead to inaccuracies in the PLL outputs as demonstrated in Fig. 4. Let $T = T_{\mathrm{n}} + \Delta T$, the corresponding number of delays can be calculated as

$$N = \frac{Tf_{\mathrm{s}}}{4} = N_{\mathrm{n}}(1 + \frac{\Delta T}{T_{\mathrm{n}}}) = N_{\mathrm{n}}(1 + F_{\mathrm{n}}) \tag{9}$$

where ΔT is the difference between the fundamental period of the measured voltage and the nominal fundamental period and $F_{\mathrm{n}} = \Delta T/T_{\mathrm{n}}$ is the fractional number with $|F_{\mathrm{n}}| \ll 1$.

Similarly, the *T*/4 Delay unit can be obtained as

$$z^{-N} = \left[z^{-(1+F_{\mathrm{n}})}\right]^{N_{\mathrm{n}}} = \left[z_v^{-1}\right]^{N_{\mathrm{n}}} \tag{10}$$

in which $z_v^{-1} = z^{-(1+F_{\mathrm{n}})}$ is defined as a Virtual Unit Delay (VUD). However, it is still difficult to implement the VUD. Fortunately, the VUD z_v^{-1} can be effectively approximated by first-order Lagrange interpolation polynomials [2], which in returns can be implemented in practice using conventional unit

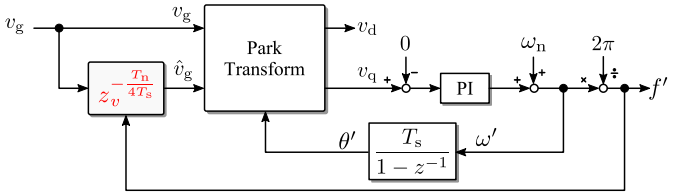

Fig. 6. Digital implementation of the advanced single-phase *T*/4 Delay PLL system with virtual unit delays (i.e., z_v^{-1}).

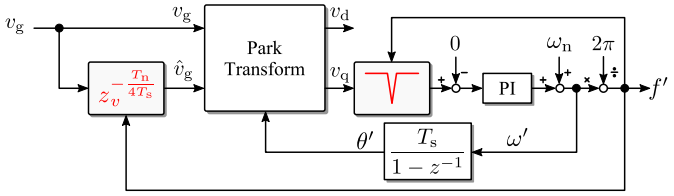

Fig. 7. Block diagram of the advanced single-phase *T*/4 Delay PLL system with digital filters.

delays z^{-1}. Specifically, the Lagrange-based approximation can be expressed as

$$z_v^{-1} \approx \begin{cases} |F_\mathrm{n}|\, z^0 + (1-|F_\mathrm{n}|)z^{-1} & -1 < F_\mathrm{n} < 0 \\ (1-|F_\mathrm{n}|)z^{-1} + |F_\mathrm{n}|\, z^{-2} & 0 \le F_\mathrm{n} < 1 \end{cases} \tag{11}$$

Substituting (11) into (10) gives the VUD-based *T*/4 Delay unit that can be implemented in digital controllers with a fixed sampling rate. Fig. 6 shows the entire structure of the digital VUD-based *T*/4 Delay PLL, where it can be seen that the output frequency f' is fed into the *T*/4 Delay unit to calculate the fractional number F_n. The use of VUDs makes the *T*/4 Delay PLL frequency-adaptive and being an advanced digital PLL system. It should be pointed out that the VUD with a fixed sampling rate can virtually be taken as a conventional unit delay with a variable sampling frequency. However, its effectiveness is sustained within a limited range [2], [18].

C. Advanced T/4 Delay PLL Using Generalized Comb Filters

It has been demonstrated in Fig. 5 that poor harmonic immunity is another shortcoming for the conventional digital *T*/4 Delay PLL. As also mentioned previously, even-order harmonics will appear in the q-axis voltage v_q, which will pass to the output estimated frequency. When considering an input voltage with background distortions as

$$v_g(t) = V_m \cos(\omega t + \phi_0) + V_m^h \cos(h\omega t + \phi_0^h) \tag{12}$$

with h being the harmonic order and V_m^h, ϕ_0^h being the amplitude and initial phase of the harmonic, the q-axis voltage v_q can be obtained as

$$\begin{aligned} v_\mathrm{q}(t) \quad &= V_m \Delta\theta - V_m^h \sin\theta' \cos(h\theta) \\ &\quad + V_m^h \cos\theta' \cos(h\theta - \tfrac{h\omega T_\mathrm{n}}{4}) \end{aligned} \tag{13}$$

where the initial phases $\phi_0 = \phi_0^h$ for simplicity.

In addition, for single-phase systems, the harmonics are mainly concentrated at specific frequencies (i.e., $h = 2k+1$ times of the fundamental with k = 1, 2, 3, $\cdots$). Assuming $\omega = \omega_\mathrm{n}$, and then (13) can be simplified as

$$v_\mathrm{q}(t) \approx \begin{cases} V_m \Delta\theta - V_m^h \sin(h\theta + \theta') & k = 1, 3, 5, \cdots \\ V_m \Delta\theta + V_m^h \sin(h\theta - \theta') & k = 2, 4, 6, \cdots \end{cases} \tag{14}$$

indicating that even-order harmonics are produced by the Park transform. However, those harmonics can not be eliminated by the PI controller, which is effective for dc components. Hence, a straightforward way to alleviate the grid voltage harmonic impact is to incorporate a filter before the PI controller. Fig. 7 shows the block diagram of the *T*/4 Delay PLL with an incorporated filter, which should be able to mitigate major even-order harmonics.

Clearly, to remove these ac harmonic components, the filters should approach zero gains at the harmonics of interest (e.g., the even-order harmonics). For an individual harmonic (e.g., 200 Hz), a notch filter with its central frequency being the target harmonic frequency can be adopted. Thus, it is straightforward to mitigate the major even-order harmonics by paralleling a number of notch filters with different central frequencies. However, this will result in much more efforts for tuning the parameters of each notch filter.

Actually, the frequency response of a notch filter is opposite to that of a proportional (i.e., 1) resonant controller [19]. Therefore, the frequency response of multiple parallel notch filters is expected to be opposite to that of a proportional multi-resonant controllers. In that case, the design can be done like the case for a proportional multi-resonant controller. Furthermore, it is known that the repetitive controller can be expanded into a combination of a dc gain, an integrator, and infinite parallel resonant controllers [2]. Thus, by taking the "reciprocal" of a proportional controller (i.e., 1) with a repetitive controller, the resultant digital filter will behave like parallel notch filters at all harmonic frequencies [2], and its design is simpler. However, the q-axis voltage of the Park transformation contains even-order harmonics. Hence, a repetitive controller for selective harmonics should be employed, which results in

$$G_\mathrm{shf}(z) = \frac{z^{-2P/n} - 2\cos(2\pi m/n)z^{-P/n} + 1}{-\cos(2\pi m/n)z^{-P/n} + 1} \tag{15}$$

being a general selective harmonic filter (i.e., parallel notch filters for selective harmonics at frequencies of $nk \pm m$), and $P = T_\mathrm{n}/T_\mathrm{s}$. The filter in (15) is also called a comb filter due to its comb-like magnitude response.

When $n = 1$ and $m = 0$, the comb filter in (15) can filter out all harmonics in theory; when $n = 2$ and $m = 0$, it becomes a selective harmonic filter only effective at the even-order harmonics (i.e., $2k$ order harmonics). Hence, the even-order comb filter can improve the harmonic immunity of the *T*/4 Delay PLL. For convenience, the comb filter (i.e., when $n = 2$ and $m = 0$) is given as

$$G_\mathrm{comb}(z) = 1 - z^{-P/2} \tag{16}$$

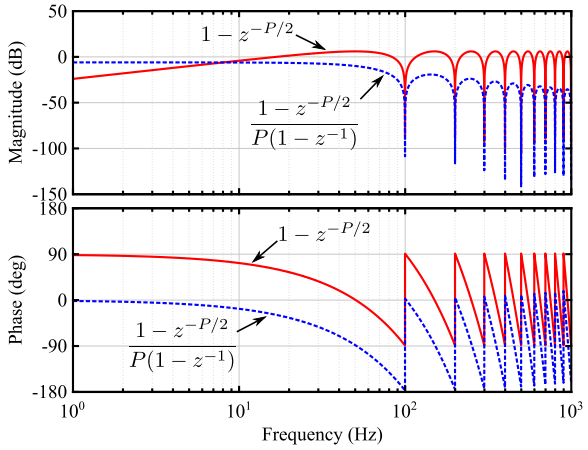

Fig. 8. Frequency responses of the generalized comb filter with T_n = 0.02 s and f_s = 10 kHz (and thus P = 200).

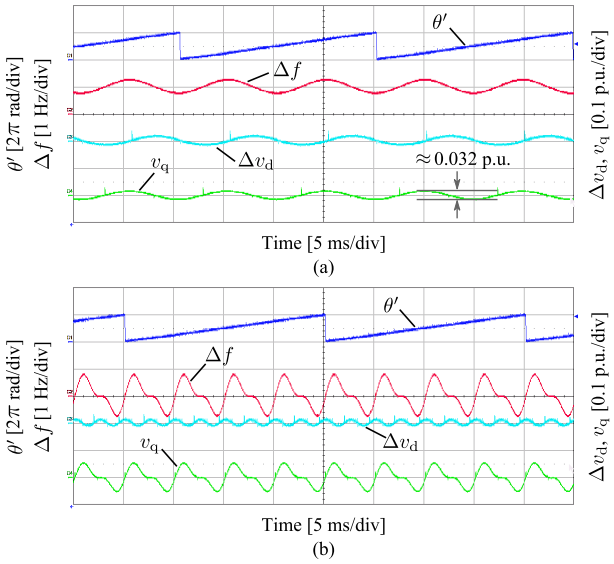

Fig. 9. Performance of the conventional $T/4$ Delay PLL under abnormal grid conditions: (a) grid frequency f = 51 Hz and (b) low-order voltage distortions (3rd-order: 2.2%, 5th-order: 1.7%, 7th-order: 0.4%, 9th-order: 1.4%, and 11th-order: 0.5%, leading to the total harmonic distortion: 3.3%).

whose frequency response is shown in Fig. 8. It can be found that the comb filter approaches to zero gains only at the selected harmonic frequencies as discussed previously. However, it is also shown in Fig. 8 that for dc components, the comb filter in (16) also has attenuation capability, which is not desired. Hence, the notch filter in (16) is modified by adding an integrator in order to allow dc signals to pass through the filter. The modified comb filter is given as

$$G'_{\text{comb}}(z) = \frac{T_s}{T_n(1-z^{-1})} \cdot (1-z^{-P/2}) = \frac{1-z^{-P/2}}{P(1-z^{-1})} \quad (17)$$

From the Bode plots in Fig. 8, it can be found that the modified comb filter in (17) will allow the dc signal to pass but block the selected harmonics (i.e., the even-order harmonics).

Note that the digital comb filters in (16) and (17) can be implemented by cascading a number of unit delays. Thus, grid frequency deviations will also lead to filtering performance degradation. To alleviate this impact, the VUD should be employed in the implementation of the comb filters. In that case, the comb filter in (17) can be expressed as

$$G'_{\text{comb}}(z) = \frac{1}{P(1-z^{-1})} \cdot (1-z_v^{-P/2}) \quad (18)$$

Hence, when the filter in Fig. 7 is replaced by a generalized comb filter in (18), the single-phase $T/4$ Delay PLL system will become frequency-adaptive and harmonic-immune.

IV. Experimental Results

In order to verify the above discussions, experiments have been carried out. The conventional and advanced $T/4$ Delay PLL systems have been discretized and implemented in a dSPACE DS 1103 system. The sampling frequency f_s is 10 kHz. The nominal grid voltage amplitude V_m and period T_n are 325 V and 20 ms, respectively. Accordingly, it can be obtained that N_n = 50 and P = 200. Since frequency deviations and harmonics are major challengers to the conventional $T/4$ Delay PLL, tests were performed only considering an abnormal grid frequency and low-order voltage harmonics.

Fig. 9 presents the steady-state performance of the conventional $T/4$ Delay PLL (see Fig. 2), where $\Delta f = f' - 50$, $\Delta v_d = (v_d - 325)/325$, $v_q = v_q/325$. It can be observed in Fig. 9 that the conventional $T/4$ Delay PLL is sensitive to grid frequency variations, and it is also non-immune to low-order harmonics in the grid voltage. Those results agree with the theoretical discussions in § III.A. Furthermore, in the case of an abnormal grid frequency being 51 Hz, the PLL system can not estimate the frequency accurately but it has double-line frequency variations, as shown in Fig. 9(a). The variation amplitude of the q-axis voltage can be approximated according to (8) as 10.2 V, which is 10.4 V (i.e., 0.032 p.u.) in the experiments. In addition, observations in Fig. 9(b) confirm that the low-order odd harmonics in the grid voltage will result in high-order even harmonics in the q-axis voltage, as it is also discussed in § III.C. Unfortunately, both the double-line frequency components and the high-order even harmonics can not be fully eliminated by the PI controller.

To address those shortcomings, the VUD has been adopted according to Fig. 6. Experiments have been conducted under the same conditions, and the results are shown in Fig. 10. It can be seen in Fig. 10(a) that employing the VUD can improve the frequency adaptability of the $T/4$ Delay PLL. The experiments verified that the VUD system can introduce a phase-shift of 90° to the grid voltage with an abnormal frequency (e.g., 51 Hz). As a consequence, the fundamental of the virtual voltage $\hat{v}_g$ will be in quadrature with the fundamental of the real grid voltage v_g. However, all harmonics in the grid voltage will also be phase shifted and passed to the Park transform system. In that case, high-order even harmonics will appear in the q-axis voltage, as demonstrated in Fig. 10(b). This means that the poor harmonic immunity remains even when the VUD system is adopted.

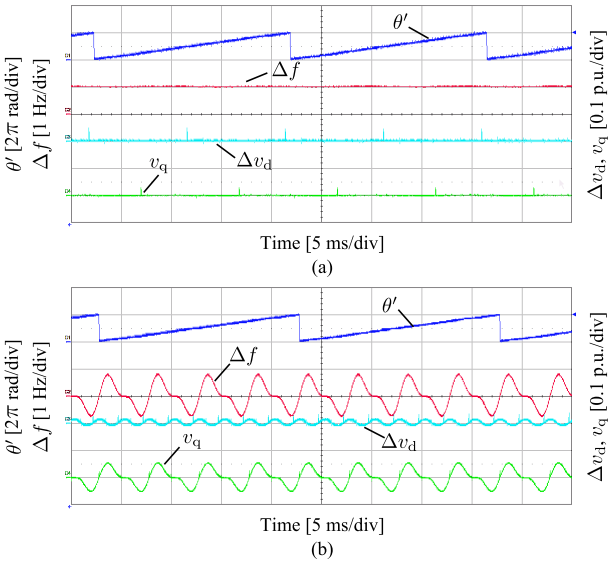

Fig. 10. Performance of the $T/4$ Delay PLL with virtual unit delays (see Fig. 6) under abnormal grid conditions: (a) grid frequency f = 51 Hz and (b) low-order voltage distortions (total harmonic distortion: 3.3%).

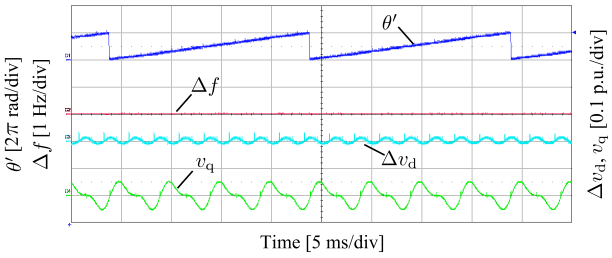

Fig. 11. Performance of the $T/4$ Delay PLL with virtual unit delays and a comb filter (see Fig. 7), where the grid voltage contains low-order harmonics (total harmonic distortion: 3.3%).

Considering the harmonic characteristics of the q-axis voltage, an even-order selective harmonic filter of (17) is incorporated in the PLL system according to Fig. 7. The system performance under the distorted grid voltage is shown in Fig. 11, where it can be seen that the VUD-based PLL system with the comb filter can accurately estimate the grid frequency. In fact, when the comb filter is employed, the VUD system can be replaced by the conventional $T/4$ Delay unit. This is due to that the double-line frequency components induced by grid frequency variations can also be mitigated by the even-order comb filter. Nevertheless, employing digital filters can advance the single-phase $T/4$ Delay PLL system, as shown in the above.

V. Conclusion

In this paper, digital filters have been explored to advance the $T/4$ Delay PLL. Firstly, a Virtual Unit Delay (VUD) has been introduced to improve the frequency adaptability of the PLL system. The VUD system ensures a 90° phase-shift of the grid voltage, so that the resultant system can tolerate the impact of varying grid frequency in practice. However, the VUD-based $T/4$ Delay PLL is also not harmonic-immune. In order to enhance the harmonic rejection capability, a generalized comb filter for even-order harmonics has been employed in the $T/4$ Delay PLL, which makes the PLL system frequency-adaptive and harmonic-immune. Experiments have confirmed the theoretical analysis and discussion.

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