Arm Balancing Control and Experimental Validation of a Grid Connected MMC with Pulsed DC load

M. Jankovic, *Member, IEEE*, A. Costabeber, *Member, IEEE*,
A. Watson, *Member, IEEE*, and J. C. Clare, *Senior Member, IEEE*

***Abstract*—This paper focuses on the operation of a grid connected Modular Multilevel Converter (MMC) supplying a pulsed DC load. The goal is to achieve minimum AC power fluctuation despite the high power fluctuation present on the DC side. The MMC has been selected for its inherent ability to decouple AC and DC current controllers. However, if no additional provisions are taken, the pulsed load causes imbalance of cell capacitor voltages between upper and lower arm in each phase. The paper presents the theoretical analysis of the imbalance problem, and proposes a simple arm balancing controller to enable the operation of the converter under pulsed DC load. The effectiveness of the controller has been successfully verified on a 7 kW MMC experimental prototype with a 3 kA pulsed DC load.**

***Index Terms*—Arm balancing control, Grid-connected converter, Modular Multilevel Converter, Pulsed power.**

I. Introduction

Modular Multilevel Converters (MMCs) have been increasingly used in medium and high voltage applications, with the most common application being in HVDC transmission [1]. The MMC offers high efficiency, high modularity and good AC waveform quality [2]. A three phase MMC is presented in Fig. 1. Each phase has two arms, comprised of the series connection of an arm inductor and a defined number of half bridge submodules (forming a chainlink). In this paper the MMC is the grid interface for a number of klystron modulators [3], [4] used in the next generation linear accelerator under feasibility studies at CERN [5].

Klystron modulators generate the high-voltage, short-duration pulses required by klystron accelerators, by discharging an input capacitor bank [6]. The simplified diagram of this application is shown in Fig. 2, where the MMC is used as a charger for the capacitor bank. Therefore, a DC link capacitor is present even though one of the benefits of the MMC is the absence of DC link capacitors [2]. This capacitor has not been added to the system but is embedded into the load.

Manuscript received November, 2016; revised March, 2017; accepted May, 2017. This work has been funded and it was a part of a collaboration with the European Organization for Nuclear Research (CERN).

M. Jankovic, A. Costabeber, A. Watson and J. C. Clare are with the Electrical and Electronic Engineering Department, University of Nottingham, Nottingham, UK (e-mail: marija.jankovic@nottingham.ac.uk, alessandro.costabeber@nottingham.ac.uk, alan.watson@nottingham.ac.uk, jon.clare@nottingham.ac.uk).

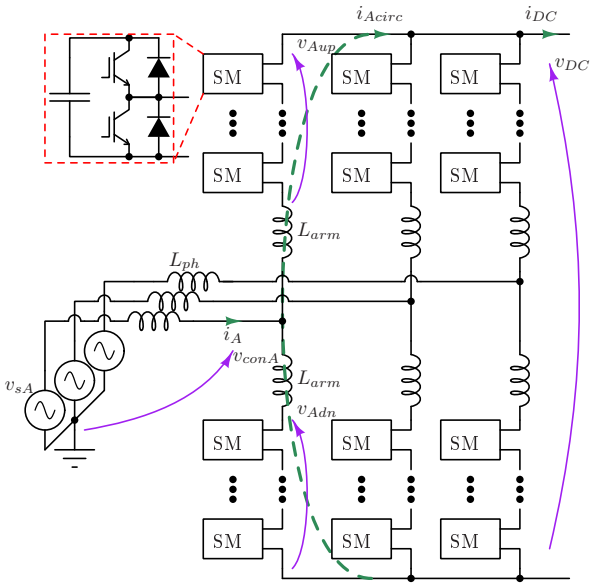

Fig. 1. Modular Multilevel Converter.

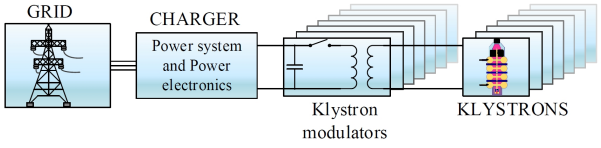

Fig. 2. Grid interface to the klystron modulators.

During operation, the klystron modulators draw from the DC link input capacitor high current 140 μs long pulses at a repetition rate of 50 Hz. As a result, the DC voltage will have a 50 Hz ripple component [7]. Consequently, a defined amount of DC power fluctuation is present [4] and the converter should act as a firewall, limiting the AC power fluctuation below 2 % (for specifications refer to [4]). The current pulses are periodic, with the same period as the grid voltages, with an arbitrary position within the grid voltage period.

Independent control capability of the AC and DC side, based on the decoupled converter model [8], [9] is an important feature of the MMC. However, it can be shown that the presence of 50 Hz ripple in the DC voltage is a constant source of imbalance between converter arms. If not compensated, this causes increased low frequency AC power fluctuation and

AC current distortion [7], [10]. This makes arm balancing controllers necessary to achieve low AC power fluctuation.

In general, multi-cellular converters require cell capacitor voltages balancing, i.e. a mechanisms for keeping the capacitor voltages at the correct levels. This can be achieved with different methods and at different levels of the control architecture. Usually the problem of capacitor voltage balancing relate to balancing capacitor voltages within one arm, which is achieved by exploiting modulation methods and tightly related to the switching frequency [1], [11]–[13]. In addition, balancing controllers are also used to maintain the energy stored in the converter phases or in the entire converter while the modulation methods ensure the correct energy distribution within chainlinks [7], [14], [15]. Arm balancing mechanisms reported in literature are used to compensate for the converter asymmetries and transient imbalance. Often, the modulation signal for each cell is derived to provide balancing within the arm and also amongst arms [9], [16], [17]. In other methods arm balancing is achieved by manipulating the circulating current reference to control the absorbed arm powers [7], [15], [18].

The control algorithm proposed in this paper belongs to the second group and it is based on the DC voltage ripple characteristics. Since the pulsed load is a constant source of imbalance among converter arms, the arm balancing controller has to be capable of achieving zero error in the steady state, which is typically guaranteed by PI based controllers, such as those used in [7], [15], [19].

In the next section the decoupled AC and DC side control is revisited and the overall control strategy is discussed. The third section analyses the pulsed load effects on the average arm powers and suggests an analytical solution for the circulating current reference to achieve balancing. The fourth section presents the simulation results and their comparison with the analytically derived expectations on a 400 kV AC/20 kV DC/16.6 MW converter (full scale rating [3]). The fifth section presents the experimental results from a laboratory scale prototype rated at 7 kW, for 225 V AC voltage and 400 V DC voltage.

II. Control Algorithm

MMC control methodologies with decoupled AC and DC controllers have been proposed in [9], [17], [20]. The decoupled control is based on the converter AC and DC side models, used to control phase current and circulating currents, respectively. In this paper, the term *circulating current* indicates the contribution of each phase to the total DC current. On a per-phase basis, the circulating current is the arithmetic average between upper and lower arm currents. The analysis proposed in this section neglects the impact of submodule capacitor ripple on the operation of the converter. As shown later in the experimental validation, the proposed arm balancing control is not affected. The AC side controller is based on the AC side equation, that can be derived from Fig. 1 (phase A only) as:

$$\frac{v_{Adn} - v_{Aup}}{2} = v_{sA} - L_{eq} \cdot \frac{di_A}{dt} = v_A \tag{1}$$

where $L_{eq} = L_{ph} + \frac{L_{arm}}{2}$ is the equivalent phase inductor and v_A is a control variable corresponding to the differential mode component of the arm voltages in phase A. This control variable has the grid voltage as feed-forward term and another term compensating for the voltage drop across L_{eq}.

Similarly the DC side controller is based on the DC side equation, given by:

$$v_{Adn} + v_{Aup} = v_{DC} + 2 \cdot L_{arm} \frac{di_{Acirc}}{dt} = v_{ADC} \tag{2}$$

where v_{ADC} is a control variable corresponding to twice the common mode component of the arm voltages. This control variable has a DC voltage feed-forward term and a compensation for the voltage drop across two arm impedances. It should be noted that v_{ADC} is purely DC only in the ideal case. The need for suppressing the second harmonic circulating current and the injection of a circulating current reference for arm balancing, adds AC components to this control variable.

Based on previous model, the upper and lower arm voltages are defined by the two control variables as:

$$v_{Aup} = \frac{1}{2} v_{ADC} - v_A \tag{3}$$

$$v_{Adn} = \frac{1}{2} v_{ADC} + v_A \tag{4}$$

If the modulation strategy ensures that arm voltages follow their reference, by neglecting the switching ripple, the arm voltages can be described by the AC and DC side control references:

$$v_{Aup} = {v_{Aup}}^{ref} = \frac{1}{2} {v_{ADC}}^{ref} - {v_A}^{ref} \tag{5}$$

$$v_{Adn} = {v_{Adn}}^{ref} = \frac{1}{2} {v_{ADC}}^{ref} + {v_A}^{ref} \tag{6}$$

In that case the AC and DC side controllers are fully decoupled and the power fluctuation on the DC side does not cause increased power fluctuation on the AC side.

The MMC used as grid interface to klystron modulators requires the control of the AC active and reactive powers and the DC voltage, to recharge the capacitor bank before the next pulse. The proposed concept of the controller is presented in Fig. 3. The AC power references are used to compute the d, q current references for the PI phase current controllers [21] based on (1). The MMC has distributed energy storage, and the overall energy stored in the converter must be actively maintained. In [17] the energy stored in each phase is controlled by varying the circulating current reference and this approach is typical when the MMC is used as an inverter, e.g. drives. In the application analysed in this paper, the DC power is imposed by the load and the energy control loop can only act on the AC active power reference (Fig. 3). Naming P_{ACcorr}, as the active power component used for energy control, the relation between the sum of all cell capacitor voltages v_{tot} (stored energy) and P_{ACcorr} is approximated by:

$$P_{ACcorr} = C_{cell} \frac{V_{DC}}{N} \frac{dv_{tot}}{dt} \tag{7}$$

where N is the number of submodules per arm and V_{DC} is the nominal DC voltage. The previous equation is valid

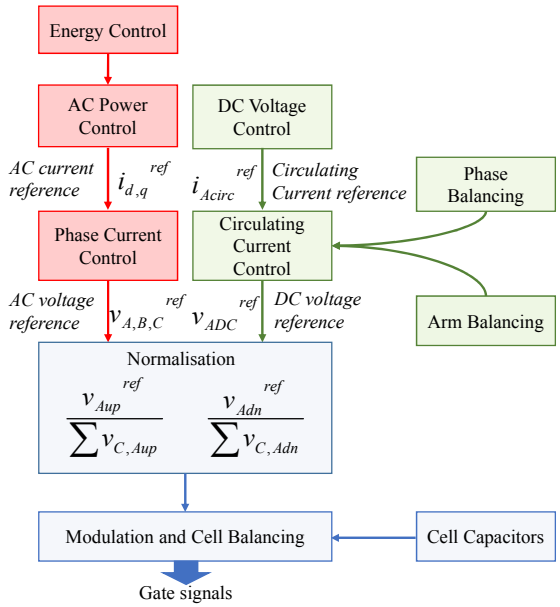

Fig. 3. AC and DC side control strategies for the MMC supplying klystron modulators.

under the assumption that the cells within converter arms are well balanced and the average cell voltages of all arms are close to the nominal cell voltage $\frac{V_{DC}}{N}$. A PI controller can be designed to ensure that v_{tot} follows the reference, equal to $6 \cdot V_{DC}$. The controller is an outer loop to the phase currents controller, and its bandwidth has to be significantly lower. The AC side control diagram is shown in Fig. 4, where reactive power is set to zero for simplicity; AVG indicates a periodical average filter with a period of 20 ms to remove voltage ripple; and signals entering PI controllers indicate errors if from comparison nodes, feed-forward terms otherwise.

The DC side control diagram is presented in Fig. 5, for phase A. The DC voltage controller generates the DC current reference which contributes to circulating current references (one third of the DC current). The controller is a slow PI acting on the average DC voltage, thus providing a constant DC current reference. Each circulating current reference is corrected in order to provide phase and arm balancing. Similarly to [16] where the total phase energy is controlled, a PI controller can be set to ensure that the average of the sum of cell capacitors is the same in all three phases. Each phase balancing loop will output a DC offset for the circulating current reference.

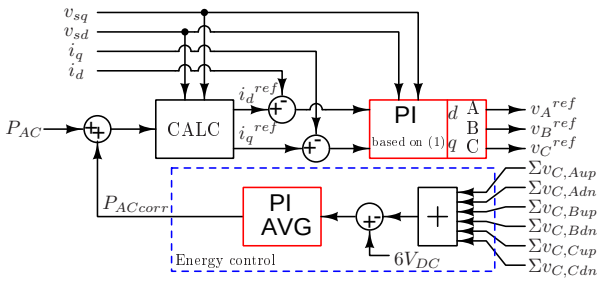

Fig. 4. AC side control diagram.

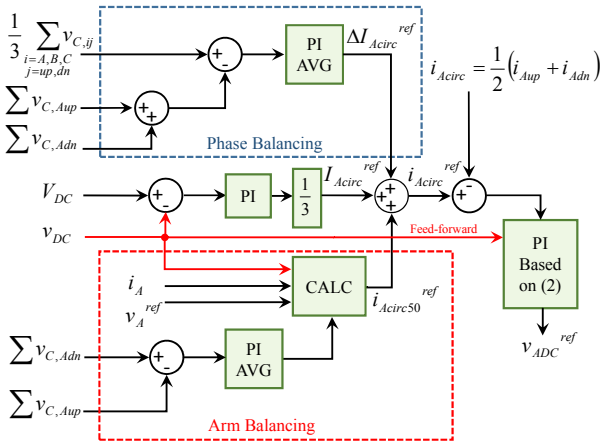

Fig. 5. DC side control diagram - Phase A of the MMC.

Naming ΔI_{Acirc} as the phase A circulating current correction, the relation between the sum of the phase A cell capacitor voltages, v_{Atot}, and the current correction is approximated by:

$$\Delta I_{Acirc} = \frac{C_{cell}}{N} \frac{dv_{Atot}}{dt} \tag{8}$$

The previous approximation is valid under the same assumptions as the one of (7). The sum of the offset components is zero, guaranteeing that there is no DC offset in the DC current. The arm balancing controller requires a 50 Hz component in the circulating current [7], [15], [18] which ensures zero average arm powers, enabling capacitor balancing. A pulsed DC load with a repetition rate of 50 Hz is a source of imbalance for the arms and it will be discussed in the following sections.

The PI controller for DC current regulation, based on equation (2), tracks constant references with zero steady-state error. In this case the reference is not constant because of the 50 Hz components. Also, the controller has to suppress the second harmonic current induced by capacitor ripple. If a high bandwidth controller is used, acceptable tracking errors are possible, as shown later in the simulation results. If perfect tracking is required, a proportional-resonant controller can be designed [22]. In any case, a DC voltage feed-forward is provided to attenuate the impact of the DC voltage ripple on the current control.

The modulation algorithm produces the gate signals for all the cells based on the arm references (5, 6). The modulation adopted in this paper is a level-shifted carrier-based algorithm with sorting of the cell capacitor voltages considering dynamic allocation of the carriers to the specific cells [1], [14], [23] also known as nearest level control with pulsed width modulation (NLC+PWM) [24]. In the given algorithm only one cell in an arm performs PWM at a time and the balancing of the cells is guaranteed by the sorting algorithm.

III. Pulsed Load Effects and the Need for Arm Balancing

The frequency of the klystron modulator pulses is equal to the frequency of the grid (50 Hz) and, intuitively, when the current pulse happens, the modulation signals and arm

currents of all the six converter arms are different, leading to different average arm powers and causing their imbalance. If arm balancing is not applied, i.e. if the circulating current reference is constant, the sum of all capacitor voltages of upper and lower arms (the overall available arm voltage) start diverging. This is illustrated for the case of an MMC rated at 20 kV DC voltage and 16.6 MW power, under pulsed load conditions, by showing the sum of all capacitor voltages of the phase A upper and lower arms together with the corresponding voltage references in Fig. 6. At 0.35 s overmodulation occurs in the lower arm, causing low frequency distortion of the waveforms that leads to an increased AC power fluctuation, manifested with the low frequency region distortion [7], [10].

In order to analyse the imbalance, average upper and lower arm powers have to be computed. In ideal conditions, when the AC waveforms contain only the fundamental component, DC current is constant and the arm balancing is not applied, only the mean value, V_{DC}, and the 50 Hz component v_{DC50} of the DC voltage are relevant for power balance:

$$v_{DC} = V_{DC} + v_{DC50} \tag{9}$$

The average upper arm power during one period of the fundamental $P_{Aup} = \overline{p_{Aup}}$ is given by:

$$\begin{aligned} P_{Aup} &= \overline{-v_{Aup} \cdot i_{Aup}} \\ &= -\frac{V_{DC} \cdot I_{Acirc}}{2} - \frac{\overline{v_{DC50} \cdot i_A}}{4} + \frac{\overline{v_A \cdot i_A}}{2} \end{aligned} \tag{10}$$

where the products of a DC quantities and 50 Hz quantities are neglected since they do not contribute to the average power. Note that due to the constant circulating current reference the DC side control variable was approximated as $v_{ADC} = {v_{ADC}}^{ref} = v_{DC}$. If equal AC and DC powers are assumed, i.e. $P_{AC} = 3 \cdot \overline{v_A \cdot i_A} = P_{DC} = V_{DC} \cdot I_{DC}$, the upper and lower arm powers become:

$$P_{Aup} = -\frac{\overline{v_{DC50} \cdot i_A}}{4} \qquad P_{Adn} = \frac{\overline{v_{DC50} \cdot i_A}}{4} \tag{11}$$

The previous equations imply that with non-zero 50 Hz component in the DC voltage, there will be an imbalance between upper and lower converter arm average powers. This causes capacitor voltage drift, which will stop only when overmodulation is reached. The effect is present in all the phases but

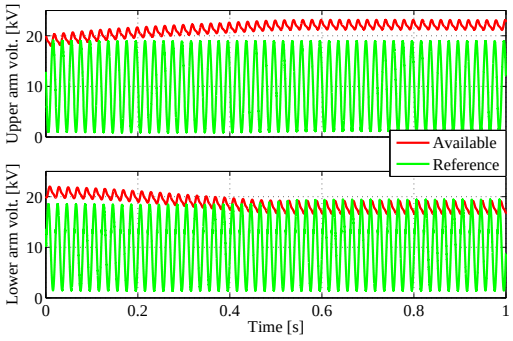

Fig. 6. Phase A upper (top) and lower (bottom) arm modulation signals and total cell capacitor voltages without arm balancing with the converter operating according to the ratings in Table II for the pulse position of 0.534 rad.

varies depending on the phase shift between phase current and the DC voltage 50 Hz ripple.

The only way to balance the arm powers with the proposed control architecture and modulation strategy described by (5 and 6), is to act on the current references. To guarantee low AC power fluctuation, the AC reference should remain unchanged, and therefore the modification of the circulating current references is necessary. As previously discussed, the frequency components of the arm currents and voltages that contribute to the absorbed arm powers are dominated by DC and 50 Hz, and therefore those are assumed to be added to the circulating current. A DC offset in the circulating current affects both arm powers in the same way and therefore it can be used as a tool to maintain the energy stored in the converter phase (phase balancing) [17]. Adding a 50 Hz component to the circulating current affects upper and lower arm powers in an opposite way, and therefore it can be used for the purpose of arm balancing [7], [15], [18]. In this case, the circulating current modification is based on average energy/power evaluation. Assuming that the circulating current has a generic 50 Hz component, used for arm balancing, it can be represented for phase A as:

$$i_{Acirc} = I_{Acirc} + i_{Acirc50} \tag{12}$$

where I_{Acirc} is the DC component and $i_{Acirc50}$ is the 50 Hz component of phase A circulating current reference. In this case, based on (2), the ${v_{ADC}}^{ref}$ can not longer be approximated with v_{DC}, but must be written as:

$${v_{ADC}}^{ref} = v_{DC} + 2L_{arm} \cdot \frac{d}{dt} i_{Acirc50} \tag{13}$$

Average upper and lower arm powers are described by:

$$\begin{aligned} P_{Aup} = &-\frac{\overline{v_{DC50} \cdot i_{Acirc50}}}{2} - \frac{\overline{v_{DC50} \cdot i_A}}{4} \\ &- L_{arm} \cdot \frac{d}{dt} i_{Acirc50} \cdot \frac{i_A}{2} + \overline{v_A \cdot i_{Acirc50}} \end{aligned} \tag{14}$$

and

$$\begin{aligned} P_{Adn} = &-\frac{\overline{v_{DC50} \cdot i_{Acirc50}}}{2} + \frac{\overline{v_{DC50} \cdot i_A}}{4} \\ &+ L_{arm} \cdot \frac{d}{dt} i_{Acirc50} \cdot \frac{i_A}{2} - \overline{v_A \cdot i_{Acirc50}} \end{aligned} \tag{15}$$

From the equations, the only way both upper and lower arm powers can be equal to zero at the same time, is if:

$$\frac{\overline{v_{DC50} \cdot i_{Acirc50}}}{2} = 0 \tag{16}$$

Equation (16) is true only if the 50 Hz DC voltage ripple and the 50 Hz circulating current reference are phase shifted by $\frac{\pi}{2}$. In that case, based on the amplitudes and phase angle of all variables from (14, 15) the amplitude of the 50 Hz component of the circulating current ($I_{Acirc50}$, for phase A) can be computed. The labels for phase angles (with respect to phase A of the grid) and amplitudes of the 50 Hz components of interest are given by Table I.

TABLE I
AMPLITUDE AND PHASE ANGLE OF 50 Hz COMPONENTS.

Signal	Amplitude label	Phase label
i_A	I_m	ϕ_{Ai}
v_A	V_m	ϕ_{Av}
v_{DC50}	V_{DC50}	ϕ_{DC50}
$i_{Acirc50}$	$I_{Acirc50}$	$\phi_{Acirc50}$

When the phase angle of the circulating current is fixed to $\phi_{Acirc50} = \phi_{DC50} - \frac{\pi}{2}$, the amplitude of the 50 Hz component of the circulating current reference is:

$$I_{Acirc50} = \frac{NUM_A}{DEN_A} = \frac{\frac{V_{DC50} \cdot I_m \cos(\phi_{DC50} - \phi_{Ai})}{4}}{V_m \cos(\phi_{DC50} - \frac{\pi}{2} - \phi_{Av}) - \frac{L_{arm}\omega I_m \cos(\phi_{DC50} - \phi_{Ai})}{2}} \quad (17)$$

where ω is the grid frequency. As shown in Fig. 7 for phase A, an arm balancing controller can be designed for each of the three phases to provide the 50 Hz component of the circulating current reference in order to compensate for the arm imbalance induced by the pulsed DC load. The amplitude and phase of the 50 Hz current reference component are provided as feed-forward terms, calculated using (17) and knowing the operating point of the converter. A correction to the amplitude is provided by a PI controller which ensures equal energy stored in the upper and lower arms in each phase. The difference between upper and lower arm average powers ΔP_{Aarm}, based on (14) and (15), is described by:

$$\Delta P_{Aarm}(t) = \frac{C_{cell} \cdot V_{DC}}{N} \frac{d\Delta v_{Aarm}(t)}{dt} \quad (18)$$

where Δv_{Aarm} is the difference between the sums of upper and lower arm cell capacitor voltages and should be controlled to zero for arm balancing. To provide the difference in power needed for arm balancing, a corresponding amplitude of the 50 Hz current $I_{Acirc50}$ is given by:

$$I_{Acirc50} = \frac{C_{cell} \cdot V_{DC}}{N \cdot DEN_A} \cdot \frac{d\Delta v_{Aarm}}{dt} \quad (19)$$

Using (19) as the control plant, a PI controller can be designed to add a closed loop correction term to NUM_A and ensure that the two arms store an equal amount of energy. From (17), the circulating current amplitudes in the different phases depend on the phase shift between the 50 Hz DC link voltage ripple and the corresponding AC voltages and currents. Considering this, a net amount of 50 Hz component will be generally present in the total DC current, even if the DC current reference from the DC voltage controller is constant. This will increase the DC power fluctuation, but the AC power fluctuation will be maintained at a low level.

A similar balancing algorithm with a 50 Hz circulating current component aligned with the AC voltage reference of each phase is suggested in [18], where only a proportional controller is used to cope with transient arm imbalances. In [15] a PI based arm balancing method with a 50 Hz component in the circulating current suggested that either arm balancing can be provided by controlling the amplitude when the angle of the current is fixed or by controlling the angle when the amplitude is fixed. Furthermore, it has been suggested that the arm balancing with the lowest current amplitudes is provided if the 50 Hz circulating current is aligned with the grid voltage of the corresponding phase.

In the method proposed in this paper, the same phase angle ($\frac{\pi}{2}$ rad) is used for all circulating currents and it is defined by the DC voltage ripple phase. This method does not guarantee minimum amplitude of the 50 Hz balancing current, but enables an arm balancing control that is decoupled from the phase energy controller. In fact, forcing (16) in (14, 15) means that a change in the 50 Hz balancing current does not affect the total phase power.

IV. SIMULATION RESULTS

Simulation results from a PLECS model of the converter are proposed to validate the overall controller and the proposed arm balancing method on an MMC rated for 20 kV DC and 16.6 MW. The converter and load parameters used in the simulation are given in Table II. The converter passives are sized according to [25]. The load is emulated with an ideal rectangular pulse current source with given amplitude, duration and repetition rate. The bandwidth and phase margin (PM) of the controllers used in the simulation model are presented in Table III.

Based on (17), DEN and the amount of 50 Hz circulating currents can be computed for a given 50 Hz DC voltage ripple. As shown in Fig. 8, the denominators of all three phases have two zero crossings and in those positions the computation of the circulating current amplitude is not possible, meaning that the arm balancing control cannot be implemented with the

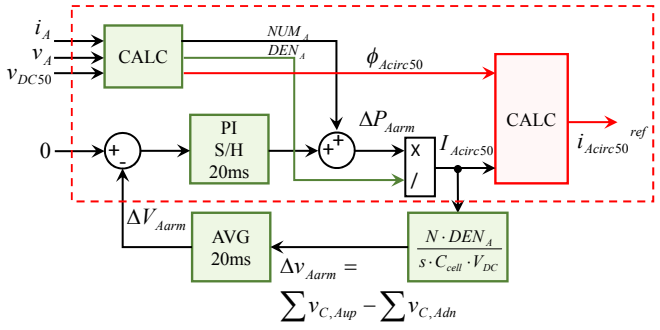

Fig. 7. Proposed arm balancing controller.

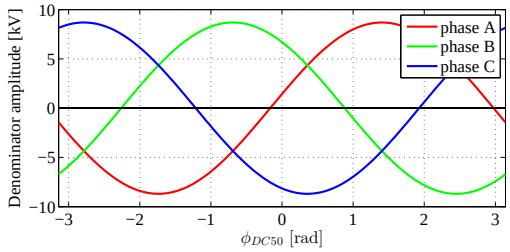

Fig. 8. The denominator values vs. the 50 Hz DC voltage ripple phase angle.

TABLE II
CONVERTER AND LOAD PARAMETERS USED IN THE SIMULATION MODEL AND EXPERIMENTAL RIG.

Description	Simulation	Experiments
Rated power	16.6 MW	7 kW
DC voltage	20 kV	400 V
AC voltage	10.5 kV	225 V
Number of cells per arm	20	4
Nominal cell voltage	1 kV	100 V
Phase inductance	3.5 mH	3 mH
Arm inductance	1.8 mH	1.5 mH
Cell capacitance	13.8 mF	3.3 mF
DC link capacitance	8.3 mH	8.5 mF
DC voltage droop	2 kV	40 V
Pulse frequency	50 Hz	50 Hz
Pulse duration	140 μs	$\approx$150 μs
Peak pulse current	118.57 kA	3.3 kA

TABLE III
CONTROLLER GAINS USED IN SIMULATION AND EXPERIMENTAL IMPLEMENTATION.

Controller	Simulation		Experiments	
	Bandwidth	PM	Bandwidth	PM
Phase Current	2000 rad/s	87 °	2670 rad/s	86 °
Circ. Current	3750 rad/s	89 °	5000 rad/s	89.4 °
Energy	10 rad/s	87 °	8.8 rad/s	71 °
DC voltage	12.7 rad/s	52 °	14.2 rad/s	86 °
Ph. balancing	20 rad/s	88 °	120 rad/s	89.9 °
Arm balancing	8 rad/s	38 °	10.5 rad/s	87.3 °

proposed approach. The phase angle of the DC link voltage ripple depends on the position of the load pulse with respect to the phase A grid voltage positive gradient zero crossing. Assuming the converter phases are symmetric, it is enough to analyse the pulse positions between grid voltage phase A and phase B zero crossings (i.e. from 0 to $\frac{2\cdot\pi}{3}$ rad). The converter has been simulated for 21 equally spaced pulse positions. Amplitude and duration of the pulse are constant.

Fig. 9 presents the AC and DC power fluctuations as a function of pulse position. In two out of 21 observed pulse positions, balancing is not possible because one of denominators is close to zero. In those positions, AC power fluctuation is beyond 2 % specification. In the other 19 pulse positions, the achieved AC power fluctuation is about 0.2 % even in the cases when the DC power fluctuation is 80 %. It is worth mentioning that DC power fluctuation increases when approaching the zero crossings of one of the DEN, because the amplitude of the 50 Hz circulating current needed for balancing increases rapidly.

The amplitudes of the three circulating current references in the different pulse positions are presented in Fig. 10. The first critical point (pulse position of 0.105 rad close to grid voltage phase A zero crossing) corresponds to the DEN_A zero crossing, while the second critical position (1.152 rad) corresponds to the DEN_C zero crossing.

From the theoretical analysis and from simulation results

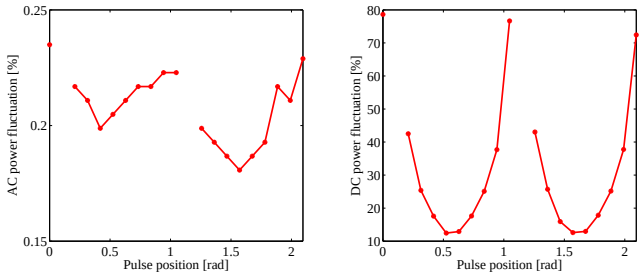

Fig. 9. AC and DC power fluctuation for different pulse positions.

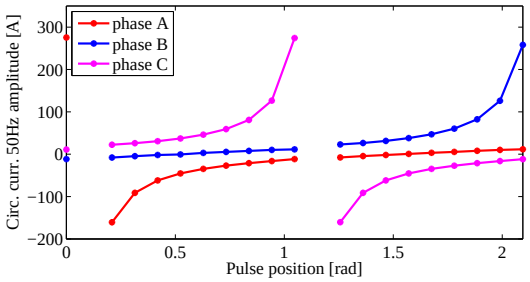

Fig. 10. Amplitudes of the 50 Hz circulating currents for different pulse positions.

it can be seen that the sum of the three 50 Hz circulating current components will generally result in a non-zero DC current ripple at 50 Hz, with an amplitude dependent on the pulse position.

Based on (17), the expression for the resulting 50 Hz DC current ripple component can be found as a function of the DC voltage ripple angle and amplitude. Knowing the expression for the DC current, the load current (50 Hz component) and the DC link capacitance, the DC voltage ripple amplitude can be computed for an arbitrary DC voltage angle. In addition, the voltage ripple phase angle is $\frac{\pi}{2}$ rad shifted from the load and DC current, and if ideal pulse is assumed, the relation between pulse position in radians and the DC voltage ripple 50 Hz component angle can be derived:

$$\phi_{DC50} = \pi - PP - \omega\frac{T_{pulse}}{2} \tag{20}$$

where PP stands for pulse position in radians and T_{pulse} for pulse duration. The obtained amplitude of the DC current ripple using the analytical model and by simulation is presented in Fig. 11.

In the considered application, the pulse can be synchronised to the grid voltages and therefore a pulse position where all the denominators are far from their zero crossings can be

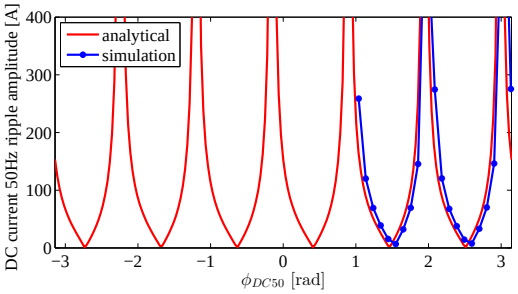

Fig. 11. Amplitudes the DC current for different pulse positions.

selected. The following simulation results relate to a fixed pulse position of 0.534 rad. Fig. 12 presents the AC and DC side currents and voltages. The obtained AC currents are sinusoidal with a THD of 0.19 %. The selected pulse position corresponds to a relatively low 50 Hz component in the DC current ripple (0.6 %). In the AC converter phase voltages (v_{conA} in Fig. 1) there are no visible signs of distortion since the overmodulation is not present. The DC voltage has a 2 kV voltage droop occurring approximately 1.7 ms after phase A current zero crossing. The obtained AC power fluctuation is 0.22 % while the obtained DC power fluctuation is 12.1 %.

Fig. 13 shows the action of the arm balancing controller on the 50 Hz circulating current references. Fig. 14 presents phase A upper and lower arm reference and available voltage (the sum of all cell capacitor voltages of an arm). Arm balancing is successful and the reference voltage is always lower than the available arm voltage, avoiding the overmodulation that was present in Fig. 6.

Fig. 15 (top) shows the energy controller dynamics, by observing the average sum of all cell capacitor voltages in two cases, when arm balancing is applied and when it is not. At $t = 1.5$ s the load peak current is reduced by 20 % and the energy controller dynamics are not affected by the presence

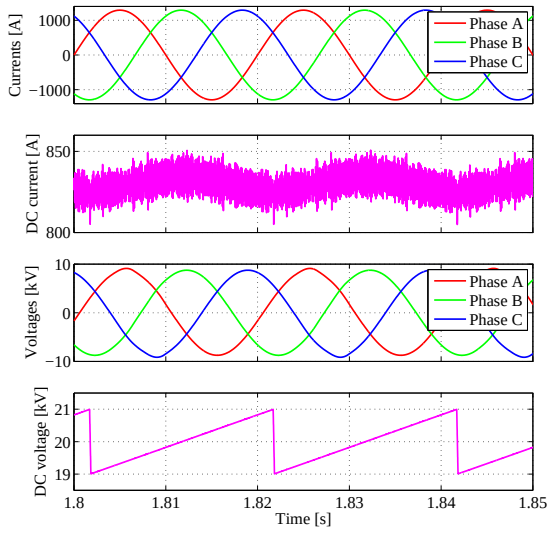

Fig. 12. From top to bottom: Phase currents, DC currents, Phase voltages and DC voltage.

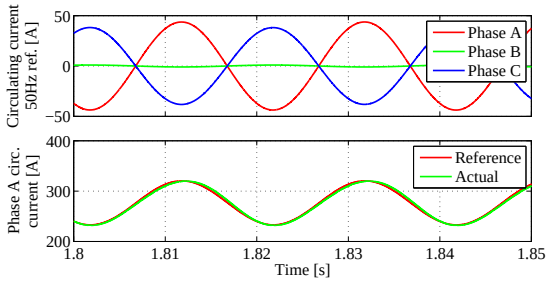

Fig. 13. Phase A, B and C 50 Hz circulating current references generated by the arm balancing controller (top plot) and phase A circulating current and its reference (bottom plot).

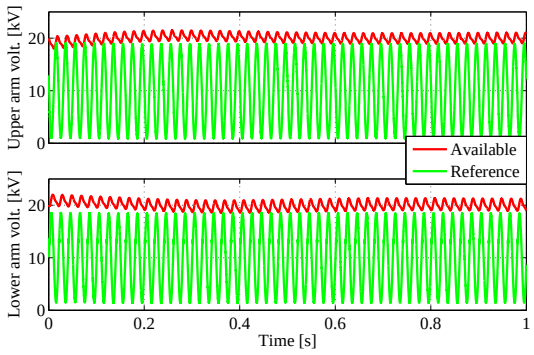

Fig. 14. Phase A upper (top) and lower (bottom) arm modulation signals and total cell capacitor voltages with arm balancing with the converter operating according to the ratings in Table II for the pulse position of 0.534 rad.

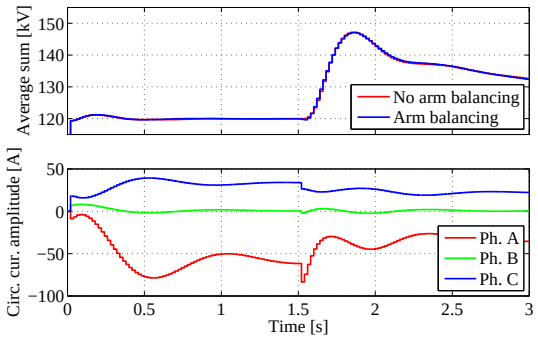

Fig. 15. The average of the sum of all cell capacitor voltages (top) and amplitude of the circulating currents used for arm balancing (bottom) during load power transient.

of the arm balancing controller whose dynamics are presented in the bottom of Fig. 15.

V. Experimental Results

A small scale prototype has been built to validate the behaviour of the grid connected MMC under pulsed DC load conditions with the proposed arm balancing controller. A 4 cell per arm, 7 kW converter has been designed by scaling both voltages and currents with the same scaling factor. A picture of the experimental converter is shown in Fig. 16. A thyristor controlled resonant circuit has been designed to emulate the pulsed DC load, which generates a 3.3 kA current pulse in a shape of half a sinusoid (Fig. 17). Table II lists the converter and the load parameters. The resonant load parameters are designed to provide the same average current (16.5 A) as the ideal rectangular pulse. Table III lists the bandwidth and PM of all controlled used in the experimental implementation.

The control algorithm is implemented in a DSP-FPGA platform, including a Texas instruments 225MHz TMS320C6713 DSP and FPGA cards used for data acquisition and PWM signal generation. The DSP board is equipped with an HPI daughter card for data logging, sampled at 10 kHz. The pulse load current and the DC voltage droop captured by the oscilloscope are presented in Fig. 18. In the experimental converter, a certain amount of imbalance is present between the converter arms even when the pulsed load is not present.

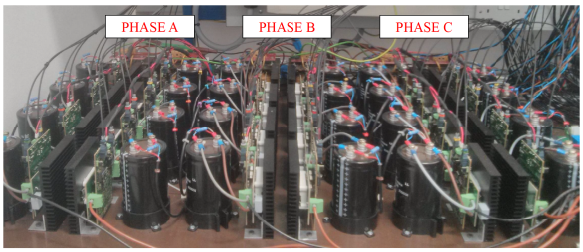

Fig. 16. Three phase MMC with 4 cells per arm.

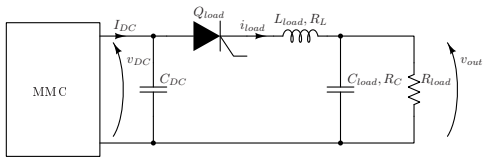

Fig. 17. Resonant load circuit.

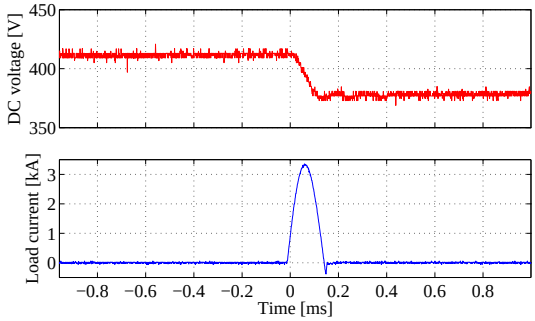

Fig. 18. DC voltage and load current during the pulse.

This is due to the non fully symmetrical converter arms and to the errors in the acquisition system. Therefore some arm balancing is necessary even with no-load or resistive DC load conditions.

Experimental results consider the same pulse position range discussed in simulation. Fig. 19 presents the AC and DC power fluctuation measured through the HPI on the experimental prototype for various pulse positions. The AC power fluctuation is not significantly affected by the pulse position, being always between 1.4 and 1.7 %, while the DC power fluctuation increases with the increase of the DC current ripple in a similar way as in simulation results. Here the critical regions are extended only beacuse the maximum circulating current 50 Hz component amplitude is limited to 3 A in order to avoid tripping the converter due to the high arm currents. Fig. 20 presents obtained amplitudes of the circulating current 50 Hz component references captured though the HPI for various pulse positions. The obtained dependence is in agreement with the one seen in simulation.

The converter phase currents measured with the oscilloscope in steady state conditions for the pulse position of 0.534 rad are presented in Fig. 21. The currents are well balanced with the low harmonic spectrum not exceeding 0.4 % of the fundamental and the THD of approximately 2 %.

Captured converter AC and DC side waveforms under

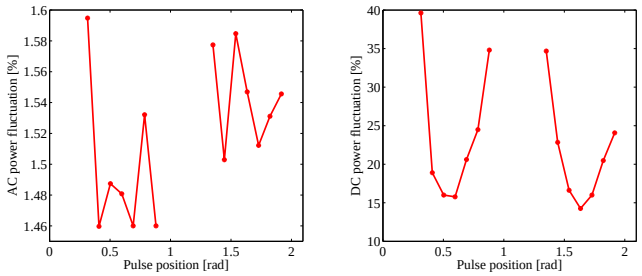

Fig. 19. AC and DC power fluctuation for different pulse positions obtained by experiment.

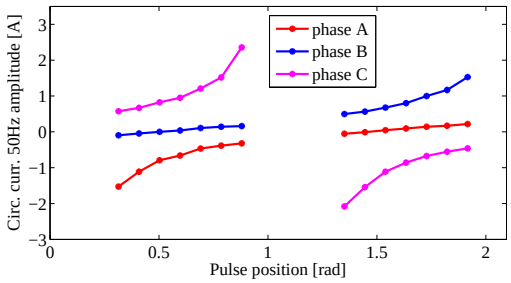

Fig. 20. Amplitudes of the circulating currents for different pulse positions obtained experimentally.

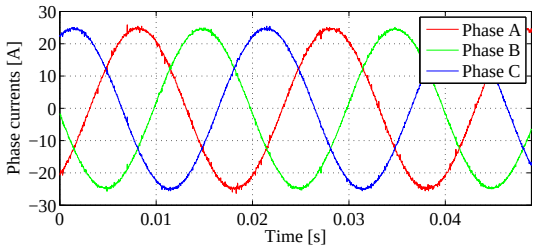

Fig. 21. Converter/grid phase currents under steady-state conditions.

steady state conditions for the position of 0.534 rad are shown in Fig. 22. The droop in the DC voltage occurs approximately 1.7 ms after phase A current zero crossing. The amplitude of 50 Hz component in the DC current ripple is similar as in the case of simulation - 0.6 % of the nominal DC current. Fig. 23 presents the sum of cell capacitor voltages of upper and lower arms obtained through the HPI. Initially the arms are perfectly balanced and the arm balancing controllers are operational. At $t = 0$ s the arm balancing controllers are disabled and the cell capacitor voltages of the upper and lower arms start diverging. At $t = 0.4$ s the arm balancing controllers are re-enabled, and the sum of capacitor voltages of the upper and lower arms start converging. The selected pulse position has a more significant effect to phases A and C, while they almost do not cause any imbalance in phase B.

The circulating current 50 Hz component references obtained through the HPI corresponding to the transient are presented in Fig. 24. For this pulse position, in the steady state, the sum of the three references is close to zero.

VI. Conclusion

This paper proposed a new arm balancing method suitable for the operation of an MMC under pulsed DC load. The

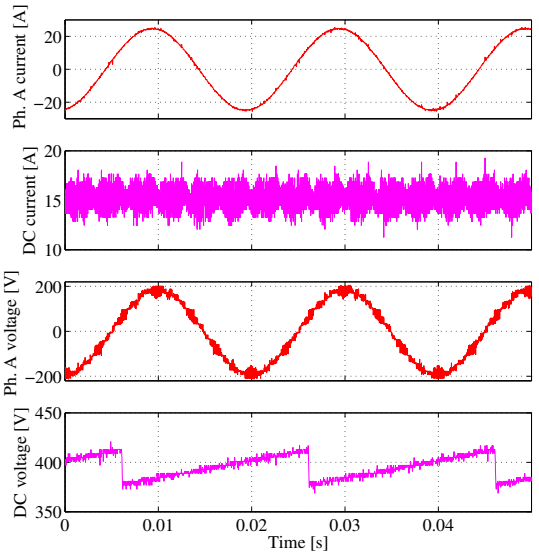

Fig. 22. From top to bottom: Phase A current, DC current, phase A voltage and DC voltage.

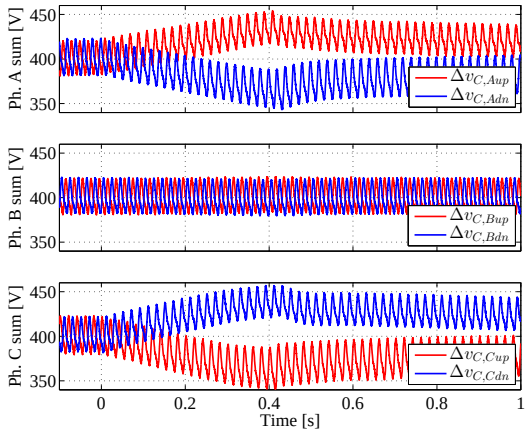

Fig. 23. Sum of the phase upper arm and lower arm cell capacitor voltages under steady state conditions, when arm balancing controller is disabled and re-enabled.

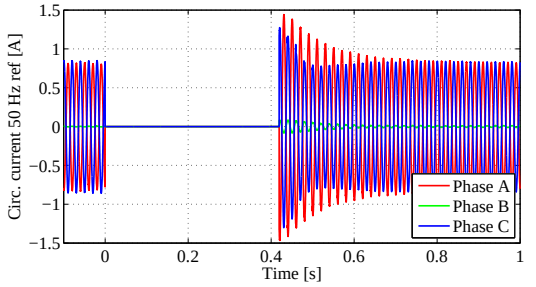

Fig. 24. Circulating current reference 50 Hz component used for arm balancing under steady state conditions, when arm balancing controller is disabled and re-enabled.

pulsed load is representative of the klystron modulators used in the next generation linear particles accelerator under study at CERN. The MMC has been selected for its decoupled AC and DC control capability, allowing the suppression of the DC power fluctuation from the AC side.

The repetition rate of the pulsed load is 50 Hz, causing imbalance of the cell capacitor voltages between upper and lower arms in each phase. Without suitable provisions, over-modulation occurs in one arm of each phase, leading to distorted AC waveforms and large AC power fluctuation. The proposed arm balancing method is based on the addition of 50 Hz components in the circulating current references, orthogonal to the 50 Hz DC voltage ripple. Detailed analysis of the proposed method has been developed and the balancing controller has been design accordingly. The proposed method is sensitive to pulse position, and balancing is not possible for 6 pulse positions within the grid voltage period. However, if the klystron modulators are synchronised with the grid, the pulse position within the grid period can be controlled, avoiding the critical regions.

Simulation results provide a first validation of the behaviour predicted by the analytical model. In addition, the proposed controller has been validated on a 400 V DC/7 kW experimental prototype. The obtained AC power fluctuation for pulse positions outside the critical regions is approximately 1.6 %. The success of the arm balancing method is proven and the required circulating current references are in agreement to those obtained by simulation.

REFERENCES

[1] M. Saeedifard and R. Iravani, "Dynamic performance of a modular multilevel back-to-back HVDC system," *IEEE Transactions on Power Delivery*, vol. 25, no. 4, pp. 2903–2912, Oct. 2010.

[2] R. Marquardt, "A new modular voltage source inverter topology," in *European Power Electronics Conference (EPE)*, Sep. 2003.

[3] M. Jankovic, A. Watson, J. Clare, P. Wheeler, and D. Aguglia, "Optimal power system and grid interface design considerations for the CLICs klystron modulators," in *2014 IEEE International Power Modulator and High Voltage Conference (IPMHVC)*, pp. 83–88, Jun. 2014.

[4] D. Aguglia and E. Sklavounou, "Klystron modulators capacitor chargers design compromises for ac power quality increase of the compact linear collider (CLIC)," in *International Symposium on Power Electronics Power Electronics, Electrical Drives, Automation and Motion*, pp. 1535–1541, Jun. 2012.

[5] D. Dannheim, P. Lebrun, L. Linssen, D. Schulte, and S. Stapnes, "Clic e+e- linear collider studies - input to the snowmass process 2013," in *Snowmass on the Mississippi CSS*, Aug. 2013.

[6] F. C. Magallanes, D. Aguglia, P. Viarouge, C. de Almeida Martins, and J. Cros, "A novel active bouncer system for klystron modulators with constant ac power consumption," in *2013 19th IEEE Pulsed Power Conference (PPC)*, pp. 1–6, Jun. 2013.

[7] M. Jankovic, A. Costabeber, A. Watson, and J. Clare, "Control of a grid connected modular multilevel converter under pulsed dc load," in *IECON 2015 - 41st Annual Conference of the IEEE Industrial Electronics Society*, pp. 002 526–002 531, Nov. 2015.

[8] S. Norrga, L. Ängquist, K. Ilves, L. Harnefors, and H. P. Nee, "Decoupled steady-state model of the modular multilevel converter with half-bridge cells," in *6th IET International Conference on Power Electronics, Machines and Drives (PEMD 2012)*, pp. 1–6, Mar. 2012.

[9] M. A. Pérez, R. L. F., and J. Rodríguez, "Decoupled current control of modular multilevel converter for HVDC applications," in *2012 IEEE International Symposium on Industrial Electronics*, pp. 1979–1984, May. 2012.

[10] A. Lachichi and L. Harnefors, "Comparative analysis of control strategies for modular multilevel converters," in *2011 IEEE Ninth International Conference on Power Electronics and Drive Systems*, pp. 538–542, Dec. 2011.

[11] F. Deng and Z. Chen, "Voltage-balancing method for modular multilevel converters under phase-shifted carrier-based pulsewidth modulation," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 7, pp. 4158–4169, Jul. 2015.

[12] W. van der Merwe, P. Hokayem, and L. Stepanova, "Analysis of the n -cell single phase mmc natural balancing mechanism," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 2, no. 4, pp. 1149–1158, Dec. 2014.

[13] A. Hassanpoor, L. Ängquist, S. Norrga, K. Ilves, and H. P. Nee, "Tolerance band modulation methods for modular multilevel converters," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 311–326, Jan. 2015.

[14] M. A. Perez, S. Bernet, J. Rodriguez, S. Kouro, and R. Lizana, "Circuit topologies, modeling, control schemes, and applications of modular multilevel converters," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 4–17, Jan. 2015.

[15] S. Fan, K. Zhang, J. Xiong, and Y. Xue, "An improved control system for modular multilevel converters with new modulation strategy and voltage balancing control," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 358–371, Jan. 2015.

[16] M. Hagiwara, R. Maeda, and H. Akagi, "Control and analysis of the modular multilevel cascade converter based on double-star chopper-cells (MMCC-DSCC)," *IEEE Transactions on Power Electronics*, vol. 26, no. 6, pp. 1649–1658, Jun. 2011.

[17] M. Hagiwara and H. Akagi, "Control and experiment of pulsewidth-modulated modular multilevel converters," *IEEE Transactions on Power Electronics*, vol. 24, no. 7, pp. 1737–1746, Jul. 2009.

[18] J. Pou, S. Ceballos, G. Konstantinou, V. G. Agelidis, R. Picas, and J. Zaragoza, "Circulating current injection methods based on instantaneous information for the modular multilevel converter," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 2, pp. 777–788, Feb. 2015.

[19] M. Jankovic, A. Watson, A. Costabeber, and J. Clare, "Control of a modular multilevel converter with pulsed dc load," in *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, pp. 1–8, Sep. 2016.

[20] W. Yang, Q. Song, and W. Liu, "Decoupled control of modular multilevel converter based on intermediate controllable voltages," *IEEE Transactions on Industrial Electronics*, vol. 63, no. 8, pp. 4695–4706, Aug. 2016.

[21] A. Yazdani and R. Iravani, *Grid-Imposed Frequency VSC System: Control in dq-Frame*, pp. 541–. Wiley-IEEE Press, 2010. [Online]. Available: http://ieeexplore.ieee.org/xpl/articleDetails.jsp?arnumber=6739414

[22] R. Teodorescu, F. Blaabjerg, M. Liserre, and P. C. Loh, "Proportional-resonant controllers and filters for grid-connected voltage-source converters," *IEE Proceedings - Electric Power Applications*, vol. 153, no. 5, pp. 750–762, Sep. 2006.

[23] E. K. Amankwah, J. C. Clare, P. W. Wheeler, and A. J. Watson, "Multi carrier PWM of the modular multilevel vsc for medium voltage applications," in *2012 Twenty-Seventh Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, pp. 2398–2406, Feb. 2012.

[24] M. Rejas, L. Mathe, P. D. Burlacu, H. Pereira, A. Sangwongwanich, M. Bongiorno, and R. Teodorescu, "Performance comparison of phase shifted PWM and sorting method for modular multilevel converters," in *2015 17th European Conference on Power Electronics and Applications (EPE'15 ECCE-Europe)*, pp. 1–10, Sep. 2015.

[25] M. Zygmanowski, B. Grzesik, and R. Nalepa, "Capacitance and inductance selection of the modular multilevel converter," in *2013 15th European Conference on Power Electronics and Applications (EPE)*, pp. 1–10, Sep. 2013.

Marija Jankovic (S'10-M'17) was born in Valjevo, Serbia in 1988. She received the B.Sc. and M.Sc. in electrical engineering and computer science at the University of Belgrade, Serbia in 2010 and 2011, respectively; and the Ph.D. degree in electrical and electronic engineering at the University of Nottingham, UK in 2017.

From 2016 she has been working as a Research Fellow with the Power Electronics, Machines and Control Group, at the University of Nottingham. Her research interests include high power multilevel topologies, converter modelling and control.

Alessandro Costabeber (S'09-M'13) received the Degree with honours in Electronic Engineering from the University of Padova, Padova, Italy, in 2008 and the Ph.D. in Information Engineering from the same university in 2012, on energy efficient architectures and control techniques for the development of future residential microgrids.

In the same year he started a two-year research fellowship with the same university. In 2014 he joined the PEMC group, Department of Electrical and Electronic Engineering, University of Nottingham, Nottingham, UK as Lecturer in Power Electronics. His current research interests include HVDC converters topologies, high power density converters for aerospace applications, control solutions and stability analysis of AC and DC microgrids, control and modelling of power converters, power electronics and control for distributed and renewable energy sources.

Dr. Costabeber received the IEEE Joseph John Suozzi INTELEC Fellowship Award in Power Electronics in 2011.

Alan Watson (S'03-M'08) received his MEng (Hons) degree in Electronic Engineering from the University of Nottingham in 2004 before pursuing a PhD in Power Electronics, also at Nottingham.

In 2008, he became a Research Fellow in the Power Electronics Machines and Control Group, working on the UNIFLEX project (http://www.eee.nott.ac.uk/uniflex/). Since 2008, he has worked on several projects in the area of high power electronics including high power resonant converters, high voltage power supplies, and multilevel converters for grid connected applications such as HVDC and FACTS. In 2012 he was promoted to Senior Research Fellow before becoming a Lecturer in High Power Electronics in 2013. His research interests include the development and control of advanced high power conversion topologies for industrial applications, future energy networks, and VSC-HVDC.

Jon C. Clare (M'90-SM'04) was born in Bristol, U.K., in 1957. He received the B.Sc. and Ph.D. degrees in electrical engineering from the University of Bristol, Bristol.

From 1984 to 1990, he was a Research Assistant and Lecturer with the University of Bristol, where he was involved in teaching and research on power electronic systems. Since 1990, he has been with the Power Electronics, Machines and Control Group, University of Nottingham, Nottingham, U.K., where he is currently a Professor of power electronics. His research interests include power-electronic converters and modulation strategies, variable-speed-drive systems, and electromagnetic compatibility.