Measuring Structure Functions of Power Devices in Inverters

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Abstract

This paper proposes the extraction of structure function from power devices on-board induction motor drives and multilevel converters. It puts forward the issues and methodology related to on-board measurement of the cooling curve and derivation of the structure function during idle times in induction motor drives for maintenance purposes. The structure function uses the thermal resistances and capacitances in the Cauer form to identify changes in the device structure. The advantage of the structure function is that it does not only reveal the value but also the location of the thermal resistance and capacitance in the heat flow path. The novelty in this work is the methodology used to achieve the measurement of the cooling curve and the derivation of the structure function despite issues related to freewheeling current due to energy stored as a result of motor inductance. A detailed description of the measurement circuit is presented. The possibility of applying this technique to multilevel converters in different application is also elaborated.

1   Introduction

Power Semiconductors are central to a number of key societal infrastructures. They are the basic building blocks of power (electrical) conversion applications. From Figure 1, the various silicon based semiconductor devices can be observed to be used for a wide range of power levels. Also the various possible applications for the semiconductor devices have been illustrated. Most of these applications are integral to daily life. In fact, according to [1], electric motors and the systems they drive are the single largest electrical end-use, consuming more than twice as much as lighting, the next largest end-use. It is estimated that electric motor driven systems account for between 43% and 46% of all global electricity consumption. Over 90 % of this is represented by induction motors. About 25-30% of induction motor drives are driven by power switched converters. This number is growing in motor drive applications, automotive, renewable and other applications.
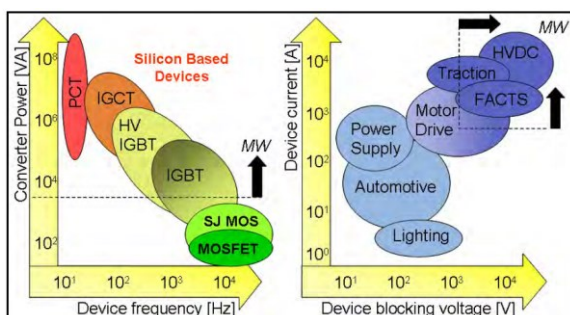

Figure 1: Power Semiconductor Devices and Applications[2]

Power converters that use insulated gate bipolar transistors (IGBT) modules are becoming more common in automotive, rail-traction, aerospace, renewable energy and several other applications where the combination of environmental and load-derived thermal cycling can result

in large and unpredictable fluctuations in junction temperature [3]. The power module is made up of different layers and several materials. This is designed to provide mechanical stability, electrical insulation and thermal conductivity[4]. The conventional power module is usually made up of eight layers as seen in Figure 2. The numbers indicate the different layers and the colors are indicative of the materials used. Table 1 enumerates some of the different materials used and the coefficients (CTE) of thermal expansion. The CTE indicates change of a component's size with a change in temperature.
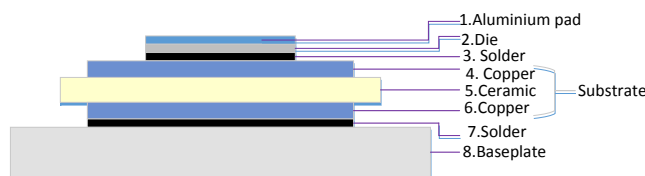

Figure 2: Conventional Power Module Cross Section

Table 1: Power Module Materials and CTE

Material	CTE ppm/°C
Aluminium	~22
Silicon (Die)	~3
Ceramic (Al_2O_3)	~7
Copper (Cu)	~17

The different values of CTE will make the different materials expand and contract at different rates which will lead to mechanical stresses resulting in various failure mechanisms, such as wire-bond lift off and cracking, solder delamination and aluminium reconstruction [4]. Wire-bond lift off and solder delamination are shown in Figure 3. The failure mechanisms need to be detected in order to prevent

abrupt destruction of the devices. Therefore to detect the impending failure, cursor/cursors of detecting the failure mechanisms need to be defined. Some parameters related the device or device structure will be related to the failure mechanisms. The thermal response function (cooling or heating curve) as a result of power step excitation contains information of structure of the device. Hence by measuring the thermal response function a change in the structure can be detected. The junction temperature then is an important parameter to monitor degradation; the power modules are enclosed and provide no opportunity for a direct measurement of the junction temperature.
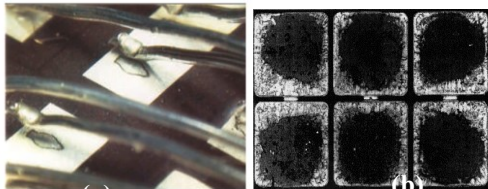

Figure 3: Failure mechanisms (a) wire-bond lift-off (b) solder delamination[5]

A common method to detect the temperature in enclosed devices with no direct contact is with temperature sensitive electric parameter (TSEP). TSEPs are electrical parameters like collector-emitter voltage (V_{ce}) [6-9] which have a mathematical relationship to temperature. V_{ce} is chosen in this work based on the fact that the aim is to measure the dynamic temperature of the device. Therefore a continuous measurement of the temperature is needed. This eliminates the use of the threshold voltage, turn-off time as regular switching is needed in order to obtain the temperature. The V_{ce} as presented in [10], exhibits the favourable characteristics such as a high repeatability, linearity.

1.1 Measuring Thermal Transients

The basic concept for measuring the cooling temperature curve by using temperature sensitive electrical parameters is shown in Figure 4(a). A high current (red) is passed through the device under test to heat up the device using a high current source; the temperature profile (blue) of the device heating and cooling can be observed. A basic set-up to obtain the aforementioned temperature profile can be seen in Figure 4 (b). A control switch is placed in the high current path to turn on and off the high current during heating and measurement respectively. The device under test (DUT) is left on, so during the measurement the low current passes through the DUT to create a voltage drop proportional to temperature. The relationship between the voltage and temperature is obtained from the device calibration. The calibration process is carried out by heating the device to a certain temperature and applying the low current (measurement current) and measuring the corresponding voltage. By measuring at different temperatures a relationship between the temperature and the voltage can be established.

The aim of this paper is to present the challenges and methodology used to extract the cooling curve and derive the structure function (from cooling curve) of the power devices in a 2-level 3-phase inverter as seen in Figure 5 without dismounting or changing the connections [8]. As seen from the basic measurement in Figure 4(b) a current source is provided in order to heat up the DUT. However in the inverter setup, the current (constant) has to be taken from the DC voltage supply without exceeding the current ratings of the devices.
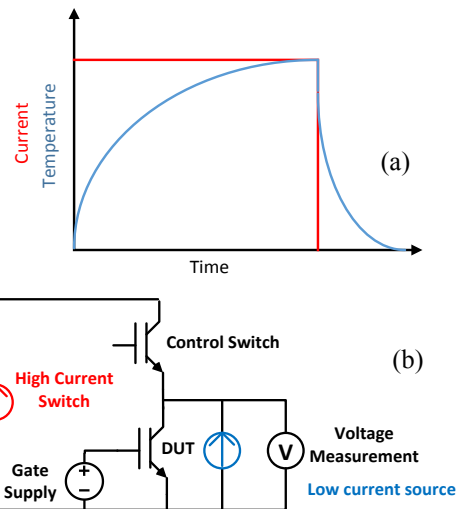

Figure 4: (a) Junction Temperature & Heating Current Pulse (b) Basic Concept of Junction Temperature Measurement Using vce
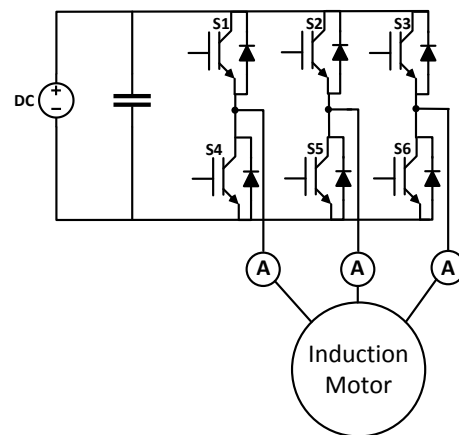

Figure 5: 2- Level 3-Phase Inverter with an Induction Motor Load

As opposed to the real-time monitoring solutions, which take measurements of the TSEP of the device during operation of the inverter, in the methodology proposed here, measurements are taken when the system is not operation in order to measure the cooling curve. In [11, 12] real-time monitoring is presented, which compares physical measurement with a model estimate to accurately track the

junction temperature of the device under consideration. The limitations of this method are that the collector emitter voltage is noisy and intermittent due to the non-linearity of the I-V characteristic of the IGBT, low temperature sensitivity and the variable phase current in an inverter. A quasi real-time method was also proposed in [13] which uses the RMS collector emitter voltage and current to detect fault just before start in vehicles.

The in-situ method in [14] works by injecting external currents into the power unit during idle times. Both high currents (heating) and low currents (measuring) are injected externally. Moreover, in [14] a set of relays need to be inserted to select which device undergoes test, with severe limitation of the applicability of such solution and considerable complication of the testing methodology. The method [15], mainly made reference to in this work introduces the use of vector control to heat up the power devices making use of the DC voltage supply as opposed to [14] which uses external high current source. An original approach in this paper is extraction of structure function (on-board) which can be carried out between operational phases of the equipment, such as in trains once a week/month in the depot for maintenance routines.

2 Structure Function

The structure function uses the thermal resistances and capacitances in the cauer form (because Cauer networks have a link with the physical structure) to identify changes in the devices structure. The structure functions are obtained by direct mathematical transformations from the heating or cooling curves [16]. These curves may be obtained either from measurements or from the simulations of the detailed structural model of the heat flow path. In both cases a unit step function powering has be applied on the structure, and the resulting increase (or decrease, in case of switching off) in the temperature at the same location has to be measured in time, following the switching on[17].

The advantage of the structure function is that it does not only reveal the value but also the location of the thermal resistance and capacitance in the heat flow path. There are two types of structure function, differential and cumulative. The cumulative structure function is also known as the Protonotarios-Wing function[18]. This is a function that presents a graphical representation of the structure of the device by using the thermal capacitance and thermal resistance. The cumulative structure function is sum of the thermal capacitances $C\Sigma$ (cumulative thermal capacitance) in the function of the sum of the thermal resistances $R\Sigma$ (cumulative thermal resistance) of the thermal system, measured from the point of excitation towards the ambient. In [17], the differential structure function is defined as the derivative of the cumulative thermal capacitance with respect to the cumulative thermal resistance, by

$$K(R_\Sigma) = \frac{d\,C_\Sigma}{d\,R_\Sigma} \qquad (1)$$

From Figure 6, considering a dx wide slice of a single matter of cross section A, we can calculate this value. Since for this case $dC\Sigma=cAdx$, and the resistance is $dR\Sigma=dx/\lambda A$, where c is the volumetric heat capacitance, λ is the thermal conductivity and A is the cross sectional area of the heat flow, the K value of the differential structure function is
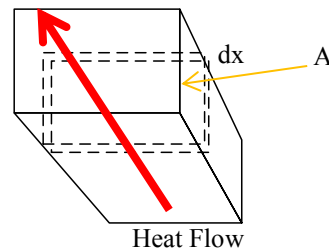

Figure 6: One Dimensional Heat Flow Model

$$K(R_\Sigma) = \frac{cAdx}{\frac{dx}{\lambda A}} = c\lambda\,A^2 \qquad (2)$$

This value is proportional to the c and λ material parameters, and to the square of the cross sectional area of the heat flow, consequently it is related to the structure of the system. In other words: this function provides a map of the square of the heat-flow cross section area as a function of the cumulative resistance. The differential function is shown in Figure 7, the local peaks indicate reaching new surfaces (materials) in the heat flow path, and their distance on the horizontal axis gives the partial thermal resistances between these surfaces. More precisely the peaks point usually to the middle of any new region where both the areas, perpendicular to the heat flow and the material are uniform
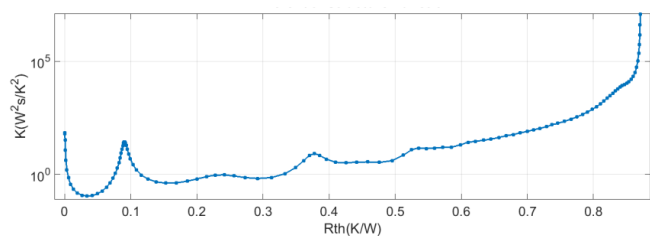

Figure 7: Differential Structure Function

3 Extracting Structure Function On-Board

One of the challenges of extracting the structure function from the inverter is heating the devices with constant current. A control technique called vector control is introduced to heat up the devices and at the same time keeps the induction motor stationary, as test is to be carried out during maintenance routines. Vector control is used because it provides the opportunity to control the torque current (I_{sq})

and field current I_{sd} which analogous to the armature current and the field current in DC motors respectively. By making the torque current (I_{sq}) 0 and giving the required current as the field (I_{sd}) reference, current flows in the devices hence heating the devices up without moving the rotor. These conditions make it suitable for maintenance routine. The details of this process are presented in [15]. The resulting phase currents during heating can be seen in Figure 8. From the phase currents it is evident that the motor will be stationary due to absence of rotating fields.
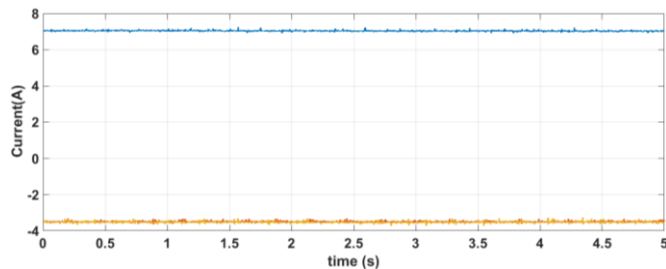
Figure 8: Three Phase Currents During Heating

The next step after heating is measuring the V_{ce}, which has to be carried out on the inverter in the presence of high voltages.

3.1 Measurement Circuit

The measurement circuitry is based on the work in [6]. Two diodes D1 and D2 shown in Figure 9 are connected in series and a current source forward-biases them during the IGBT on time. When the IGBT is off, the D1 diode is blocking the V_{ce} voltage, protecting the measurement circuitry from damage. Assuming the two diodes are identical ($V_{D1} = V_{D2}$), the V_{ce} voltage may be measured by subtracting the voltage drop on diode D2 from the V_b potential. This mathematical function can be realized using the circuit shown in Figure 9.

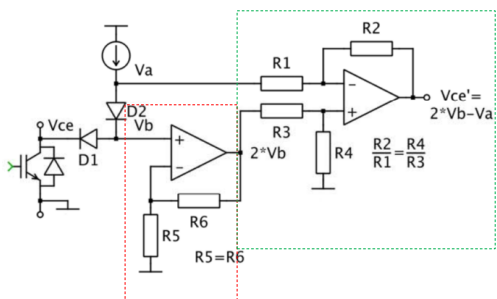$$V_{ce} = V_b - V_{D2} = V_b - (V_a - V_b) = 2V_b - V_a$$
(3)

Figure 9:Schematic of measurement circuit [6]

The circuit in Figure 9 makes it possible to implement the equation above. The first op-amp (highlighted in red) does the mathematical function of producing $2V_b$ in (3). The second part (highlighted in green) of the circuit completes the mathematic function using a differential amplifier to obtain V_{ce} ($2V_b$-V_a). Extra stages have been added to the

measurement circuit, such as conditioning the signal to utilize the full range of the FPGA and increase resolution. An isolation stage has also been added to protect the control board.

The measurement circuit was designed with the resolution of the temperature measurement using collector-emitter voltage in mind. The resolution of the collector-emitter voltage with respect to temperature is ~2mV/°C, thus a direct measurement of the collector-emitter voltage inevitably yields to noisy data. The voltage range of the collector-emitter voltage in relation with the temperature is 0.14612V-0.56612V for the range of temperature 0°C-200°C. The range used in this work for the sake of convenience is 0.1V-0.6V. The A/D converter chosen in order to achieve high resolution is a 12 bit chip LTC1407. For a 12 bit A/D the number of discretization levels is

$$N = 2^{12} = 4096$$
(4)

The limits for the input of the A/D converter is ±5V. Hence :

A/D full range=10V= 4096 levels

Collector-emitter voltage range=0.5≈205 levels

This means that the minimum voltage that can be recorded in the host PC is 0.0024 V. As mentioned earlier the relationship between the voltage and the temperature is 2mV/°C. Therefore with a direct measurement into the FPGA the minimum temperature that can be measured is just above 1°C. To improve this, the full range of the FPGA has to be utilised by applying a gain and an offset to the measured signal. This is implemented by making the value of the highest voltage measured (0.6) correspond to the upper limit of the FPGA voltage input (+5V) and the lowest voltage measured (0.1) correspond to the lower limit of the FPGA voltage input (-5V). The gain and the offset needed to achieve this is calculated by solving the simultaneous equations

$$5 = 0.6 gain + offset$$
(5)

$$-5 = 0.1 gain + offset$$
(6)

Yielding: gain 20; offset 7V. This can be implemented using electronics. In the practical implementation the values of gain and offset need to be incorporated into the circuit design. A practical simulation of the measurement circuit was carried on LT spice using real components. The schematic of the practical measurement circuit is shown in Figure 10. The op-amps 1 & 2 result in the Vce voltage as explained in Figure 9. The differential amplifier (op-amp1) can be used to partly implement the gain derived from equations (5) & (6). The differential amplifier (op-amp 1) is used to produce a gain of 10 although a gain of 20 is needed. The gain of 20 is obtained in 2 stages due to the configuration used to achieve the offset as will be seen.
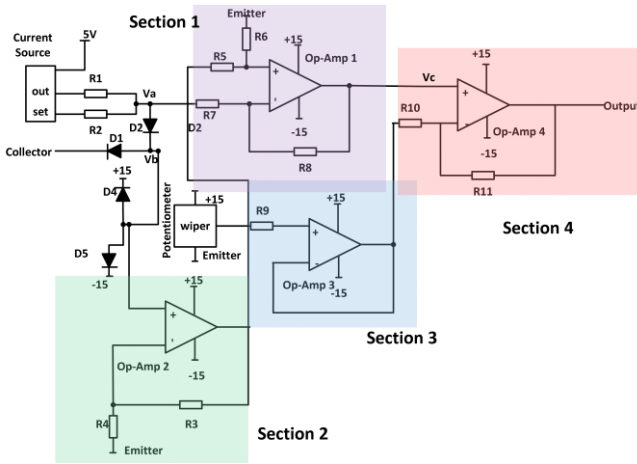
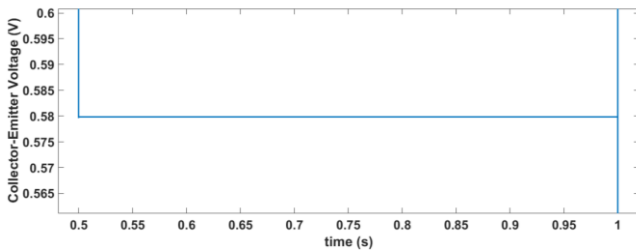Figure 10:Schematic of the for the top device measurement circuit

Figure 11:Simulation of collector emitter voltage

In the simulation, for the IGBT, an FGA180N33ATD Fairchild 330V IGBT was used. Its V_{cesat} is given in Figure 11 as 0.579834 V. Equation (3) is used to derive Vce using the op-amps in section 1(purple) and section 2 (green) shown in Figure 10. Op-amp 2 (green) is a non-inverting amplifier with a gain of 2 and V_b as an input. The output (2Vb=3.25693V) of the op-amp 2 (green) and the node Va (2.67709) is shown in Figure 12. By using equation (3) the inferred Vce is derived to be 0.57984V, which is the same value as the value measured across the collector emitter.
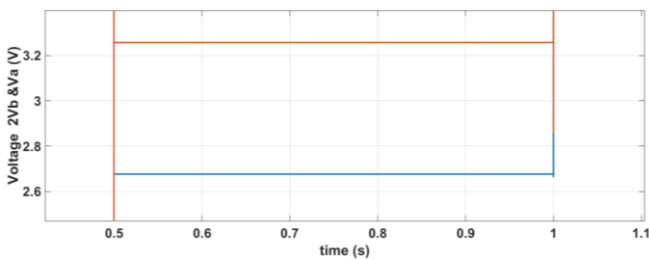

Figure 12: Voltages at the output of op-amp2 and node Va

The op-amps in section 1, 3 and 4 are used to achieve a gain 20 & offset of -7. The differential Op-amp in section 1 (purple) is used to subtract V_a from $2V_b$ (V_{ce}) and apply a gain of 10 by choosing R_5 and R_7 to be 10,000Ω and R_6 and R_8 to be 100,000Ω. This means, considering equation (7) the output of op-amp 1(purple) will gain by 10.

$$V_{out} = V_{ce} = 2V_b\left(\frac{R6}{R5+R6}\right)\left(\frac{R7+R8}{R7}\right) - V_a\left(\frac{R8}{R7}\right)$$

(7)

Only a gain of 10 is applied in section 1 because a non-inverting amplifier in section 4 is used to apply the offset of -7. Since the gain of a non-inverting amplifier will always be greater than 1, a gain of 2 is applied to get a gain of 20 in total. The equation for the output of op-amp 4 (red) can be written as:

$$V_{out} = Gain * V_c + (1 - Gain)V_{offset} \qquad (8)$$

From equation (8) the part (Gain*V_c) of the equation contains the product of collector-emitter voltage, the gain of the differential amplifier (op-amp1-purple) which is 10 and the gain (Gain) of op-amp 4 (red) which is 2; the second part ((1-Gain)* V_{bias}) gives -7. The bias is applied by the use of a potentiometer using a voltage follower (op-amp 3-blue) to apply the reference voltage on the inverting input of op-amp 4. This is done so that the gain of the op-amp 4 (red) is not affected. Hence a gain of 20 and an offset of – 7 are achieved. The two diodes D5 and D4 are used as protection in case of any voltage spikes to protect the op-amp 2. The simulation output of the measurement circuit can be seen in Figure13. This gives an accurate result of 4.596V which is the same as (Vce*20)-7, where Vce is 0.579834V.
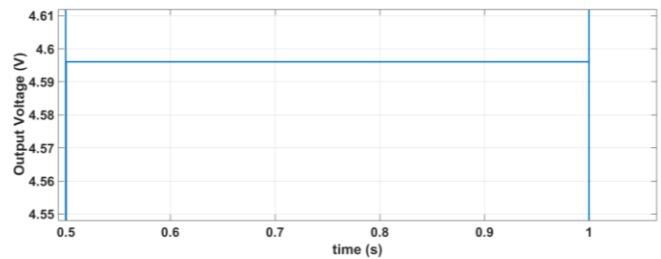

Figure13: Output of the measurement circuit

3.1.1   Protection Board

The reference point of the measurement circuit is the IGBT emitter. Since this is floating, there is a need for galvanic isolation between the measurement circuit and the FPGA board. A high speed isolation amplifier is used to isolate the emitter of the power device from a direct connection to the FPGA. The isolation amplifier used here is the Analog devices AD215BY 120 kHz bandwidth, low distortion, isolation amplifier. One of the applications the isolation amplifier is designed for is high speed data acquisition which is important in this work in order not to lose valuable data. The unity gain configuration of the op-amp for signals within the range ±10 is used (measurements range between ±5V) and can be seen in Figure14. On the output of the isolation amplifier a voltage follower is used with a ±5V supply to limit the output voltage so as to match the limits of the input of the A/D converter.
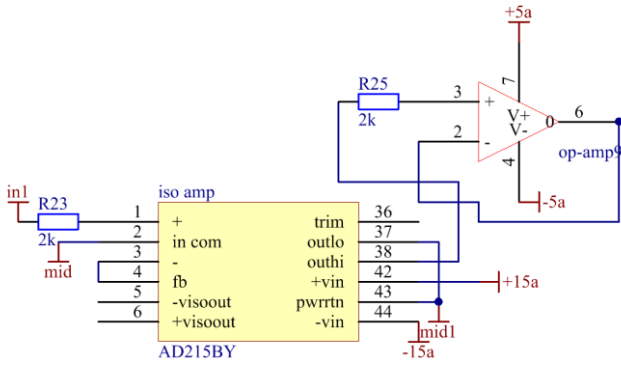
Figure14: Schematic of the isolation board

An image of the measurement board and the isolation board can be seen in Figure15. The diodes used to extract Vce D1 and D2 is the BY203 diodes which have a blocking capability of 2kV. A DC-DC converter is used to supply the op-amps and isolation amplifier with a ±15V. The buffer op-amp the output is supplied by a DC-DC converter of ±5V. Capacitors are also applied to the supply for each op-amp to ensure a smooth DC supply.
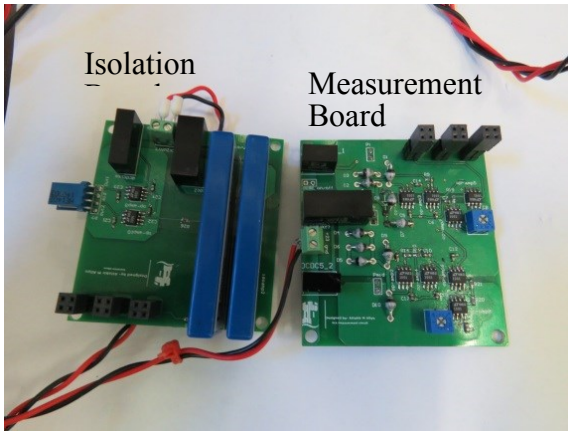

Figure15: Image of measurement circuit and isolation board

A test was carried out using the measurement circuit to determine the accuracy. At room temperature the voltage of the power device was measured using both the measurement circuit and an accurate digital multi-meter. The measurement circuit is read by the host PC as seen in Figure 16. The mean value of the measured signal is derived to be 5.238V which matches the value on the digital multi-meter. The device was then heated by supplying a current pulse of a few seconds to test the capability to measure temperature change. The voltage after the heating pulse is removed can be seen in Figure 17. The voltage is then converted to temperature using equation (9) as can be seen in Figure 18. Equation (9) has been derived from the experimental calibration involving a hot plate and accurate temperature measurement. The results indicate that the measurement circuit is functioning well.
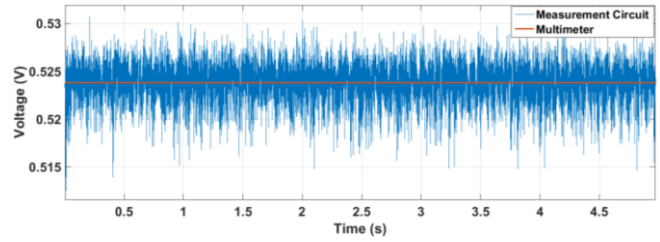

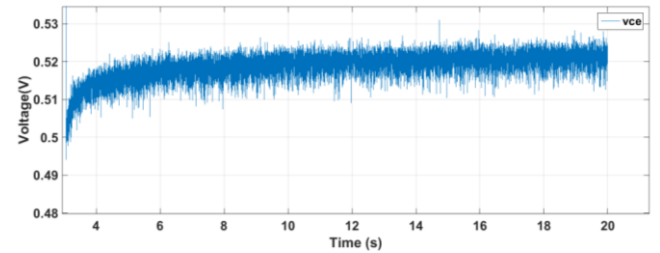Figure 16: Constant voltage measurement using digital multimeter and measurement circuit

Figure 17: Voltage measurement after the heating pulse

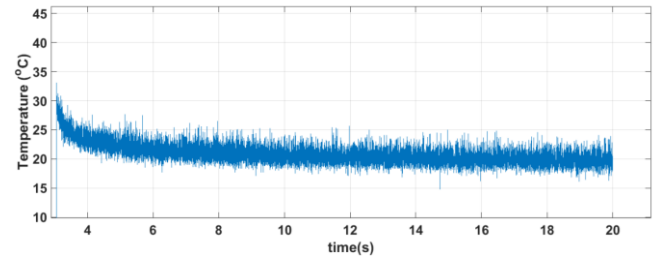$$Temperature = (voltage*(-496.88)) + 278.64 \tag{9}$$

Figure 18: Temperature change after heating pulse

3.2 Measurement On-Board

The measurement is carried out by passing the low current used to calibrate the device. This is carried out by switching on only S1 in Figure 5 and switching off S2-S6, in order to prevent high current paths. Due to the energy stored in the motor inductance current free wheels through the device switched on for measurement and the top 2 diodes in the 2 other phases as shown in Figure 19.This means that the low current measurement cannot be carried out during the free-wheeling period due to high current flowing in the device. A voltage (collector-emitter) and current measurement of the device was carried out at this stage and it can be seen in Figure 20 that the current decays slowly.
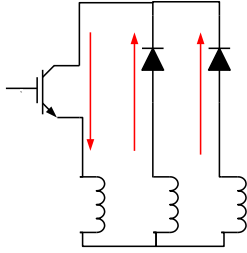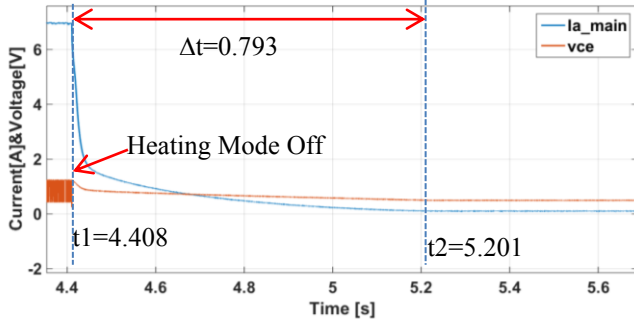
Figure 19: Inverter during Measurement Phase

Figure 20:Current and Voltage (collector-emitter) of DUT

The magnetising inductance of the motor is considerable; it takes time for the current to decay to the measurement current used for calibration. This means that by this time, a lot of information is lost in the cooling curve which means information on the structure of the device is lost. From Figure 20, it can be observed that it takes 0.793s for the current to reach the level of the measurement current. If the measurement is to start at 0.793s most information of the structure of the device will be lost; as the die, solder and substrate faster time constants. The data sheet gives information about the junction to case thermal resistance of the device (Magna Chip MPMB75B120RH) which is typically 0.2 °C/W. By matching this information to the derived normalized temperature (divided by the power dissipation) shown in Figure 21. The approximate time constant from the junction to the case can be obtained. In this case the obtained time constant from the graph is 0.2512s. This means that any measurement that starts past this time constant is measuring the heat sink. Therefore any degradation present in the device will not be recorded
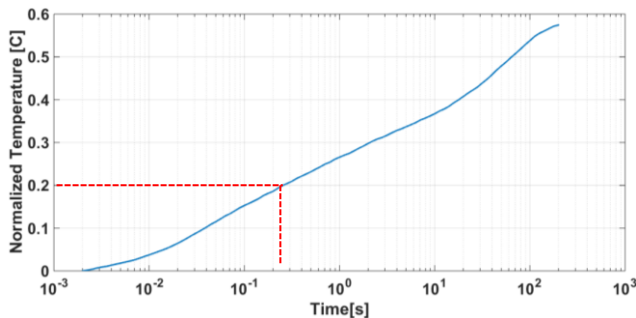

Figure 21: Normalized Temperature Curve

To solve this problem, the methodology will be outlined. Since the current stored in the inductor flows through the device and the voltage is always measured. The collector current against the collector emitter voltage (I-V curves) at different temperatures can be used to measure the temperature by creating a look-up table. In Figure 22, the maroon line is the measured voltage and current passing through the device. However this curve passes through a point on the IV curves where there is no difference in voltage and current for all the temperatures. This means that it is impossible to measure at this point (Inflexion Point). But above the and below this point the sensitivity (to noise) gradually decreases. The highlighted area in Figure 22 below the Inflexion point has a lower sensitivity (to noise) of about 2mV/°C and the highlighted area above this region has a higher sensitivity(to noise) of 0.9mV/°C This methodology exploits the point below the inflexion point. One of the reasons for this is that the region has a lower sensitivity (to noise) and also it is known that there is negligible self-heating in this region as the current is low.
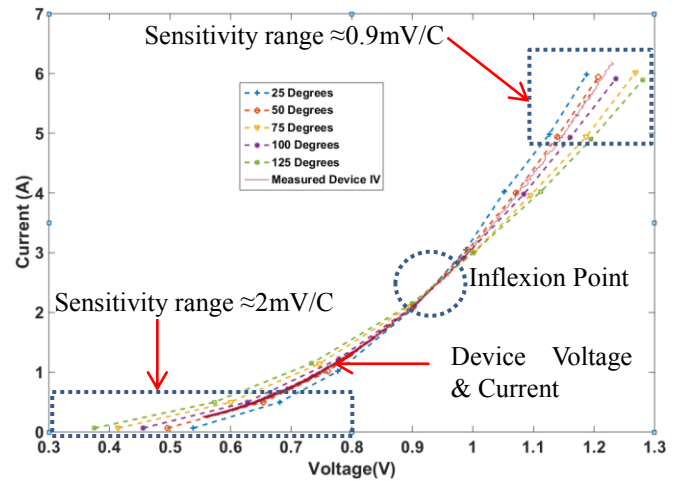

Figure 22: I-V Curves and Measured Device current and Voltage

4   Results

The methodology is to use the controller (vector control) used to heat the devices to force the current to a low value so that the region in the IV curves will be of a low sensitivity. It can be seen in Figure 23 that the reference changes from 7A to a low value (0.2 amps in this case). The current changes faster (from 7Amps to 0.2 A in 2ms) than in the previous case. This means that the self-heating is negligible, faster time constants will be recorded. In this case the measurement starts when the current falls below 1A. As it can be seen from Figure 22, the sensitivity(to noise) of the IV curves reduces as the current approaches zero therefore less error in the measurement.
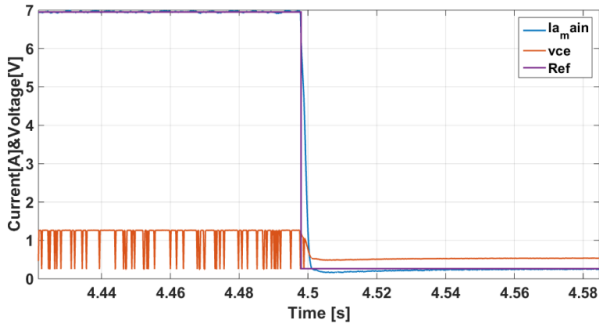
Figure 23: Current and Voltage During Measurement Using Vector Control.

The Junction Temperature measurements taken in this case are shown in Figure 24. An averaging technique was used to derive the two averaged curves (Blue and Orange). The two curves are presented here to show that this process is repeatable. This is important because the process is carried out to check for degradation in power modules; making sure changes are due to degradation not measurement. The differential structure function of the temperature curves can be seen Figure 25 also showing repeatability.
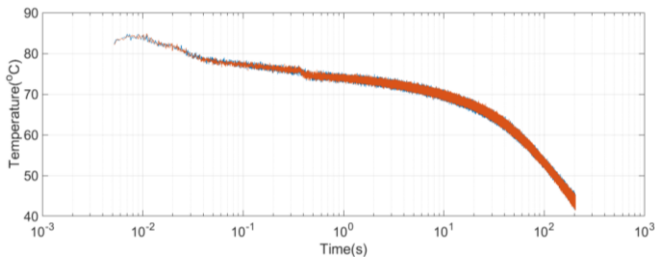

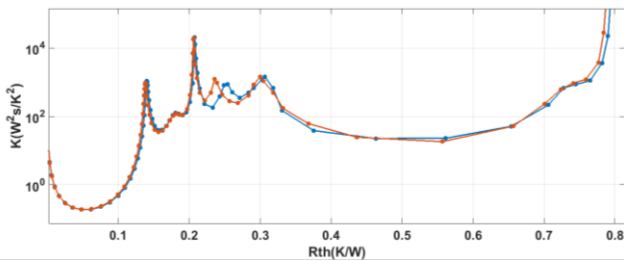*Figure 24: Junction Temperature Curves*

Figure 25: Differential Structure Function

5   Measuring Structure Functions in Multilevel-Inverters

Multi-level converters are widely used in medium-voltage drives (MVDs) for industry (e.g., rolling mills, fans, pumps, and conveyors), marine appliances, mining, and traction [19]. The use of multi-level converters in critical applications makes degradation monitoring in these topologies very important. Recently wide-band gap devices in dc/dc converters and dc/ac inverters have been widely introduced. Various converters with different application conditions show the potential of achieving very high efficiencies with WBG devices under a wide operating range [20]. This makes WBG devices favourable for most

applications, consequently making monitoring the health of the devices a very important aspect of operation. Simulations to implement the methodology in this work using a multi-level converter topology are carried out using an active neutral point clamped (ANPC) as a case study.

As mentioned in Section 3, the freewheeling current disrupts the measurement of temperature after the heating current is switched off as shown in Figure 20. The control scheme implemented in this work to ensure that measurement starts early enough only measures the solder between the substrate and the baseplate. The application of this methodology in multi-level converters provides the potential to enhance measurements and capture small time constants such as the solder layer (die-attach). For example the use of ANPC will enable measurement that captures faster time constants due to opportunity to isolate the DUT from freewheeling current.

The ANPC inverter has 6 switches in a single phase as shown in Figure 26 which are used to obtain a 3-level output phase voltage with respect to the neutral point. Different modulation strategies exist for the ANPC. One of these modulation strategies based on the reverse conduction capability of SiC MOSFETs is shown Fig 7.3.
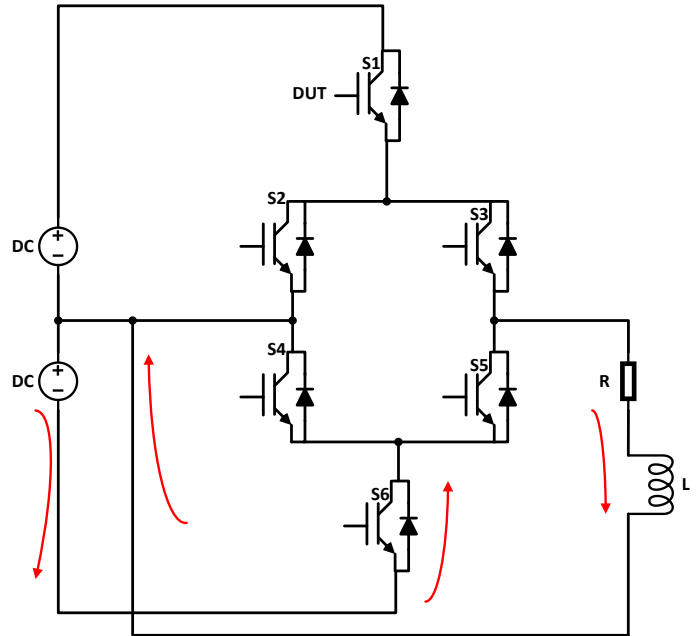

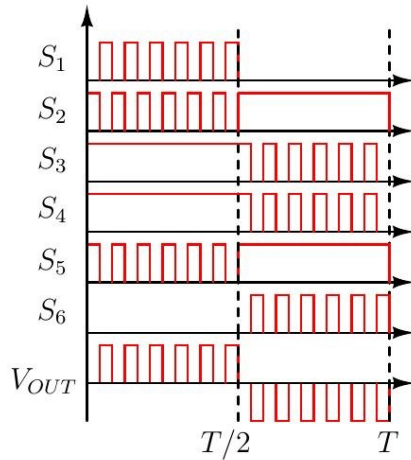*Figure 26: Single phase ANPC inverter*

Figure27: Switching Sequence and output voltage of a single phase of ANPC [21]

For the maintenance routine, the circuit is simulated in the same way the single phase converter in this work is operated and with the same control technique. The two switches S1, S3 are driven by the same control signal and S5, S6 are driven with the opposite signal while S2 and S4 remain completely off. Hence the ANPC operates as a single phase of a 2 level converter.

A heating current reference of 20 A is applied for 5s. After the 5s heating period all the switches were turned off with the exception of the DUT (S1). The output current is shown in Figure28, with the freewheeling current flowing through the phase, after all the devices except S1 have been switched off. The freewheeling current path is illustrated in Figure 26 with the current flowing through the load, then the lower DC link, then the anti-parallel diodes of S6 and S5. This means that during measurement no load current flows through the DUT (S1). The current that flows through the DUT is shown in Figure29. It can be seen that in the simulation the current goes to 0 instantaneously. In experiment the initiation of measurement is only limited to the device transient as opposed to the freewheeling current.
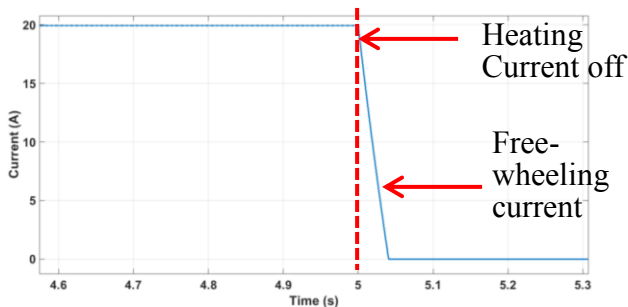

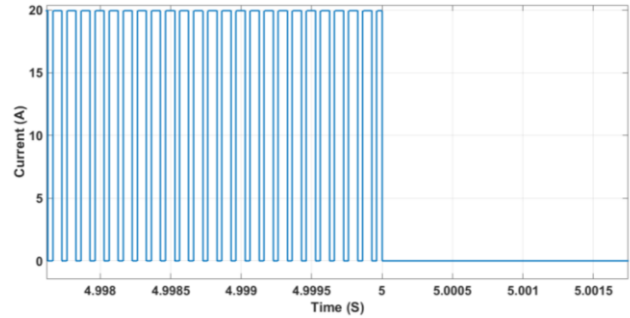*Figure28: Simulation output current ANPC inverter during maintenance routine*

Figure29: Simulation of current through DUT during maintenance routine

Application of this technique provides an opportunity to make accurate thermal characterisation of the devices used in various multilevel converters. There is also a possibility of including bond wire measurements. These can be carried out by obtaining the voltage when the high current is passed through the device as was presented in [22]. The voltage measurement is already implemented in this system; hence no added complexity is needed. If the voltage measurement at both high current and low current are utilised measuring both the wire bond lift off and the degradation in the structure becomes a possibility. This gives rise to the potential of on-board monitoring of power devices in different multilevel applications using WBG devices such as automotive, traction and aerospace.

6 Conclusion

This work has shown a method of extracting the junction temperature and structure function of power modules for health monitoring purposes. It introduces the use current controller to measure junction temperature. It also shows how to avoid the stored energy in the induction motor that disrupts temperature measurement. Experimental results of junction temperature and the structure function have been provided. The system is carried without additional components or changes to the inverter system except the analog measurement circuitry. A detailed explanation of the measurement circuit has been presented. Simulations applying this technique to an ANPC multilevel converter have also been elaborated. Future work will entail the implementation of this technique in multilevel converters.

7 Literature

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