A Survey of Carbon Nanotube Interconnects for Energy Efficient Integrated Circuits

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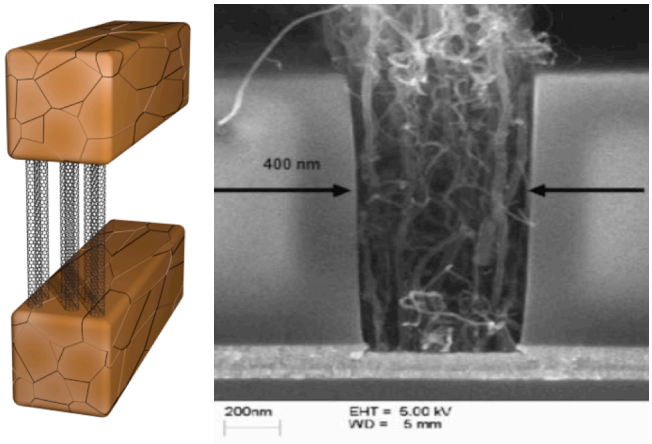
***Abstract*—This article is a review of the state-of-art carbon nanotube interconnects for Silicon application with respect to the recent literature. Amongst all the research on carbon nanotube interconnects, those discussed here cover 1) challenges with current copper interconnects, 2) process & growth of carbon nanotube interconnects compatible with back-end-of-line integration, and 3) modeling and simulation for circuit-level benchmarking and performance prediction. The focus is on the evolution of carbon nanotube interconnects from the process, theoretical modeling, and experimental characterization to on-chip interconnect applications. We provide an overview of the current advancements on carbon nanotube interconnects and also regarding the prospects for designing energy efficient integrated circuits. Each selected category is presented in an accessible manner aiming to serve as a survey and informative cornerstone on carbon nanotube interconnects relevant to students and scientists belonging to a range of fields from physics, processing to circuit design.**

***Index Terms*—carbon nanotubes, interconnects, energy efficiency.**

I. Introduction

IT was in early 2000 that the team lead by F. Kreupl filed the very first patent on the use of carbon nanotubes (CNTs) as vertical interconnects for nanoelectronic components on semiconductor chips [1] (see Fig. 1). The team emphasized that CNTs would be particularly beneficial for interconnect application due to quasi-ballistic current transport in CNTs that would allow very low resistance interconnects. They also explored how CNTs could be processed to be compatible with the on-chip interconnect fabrication. Since then, CNTs for interconnect application have attracted a lot of research interest.



(a) (b)

Figure 1. a) Illustration of carbon nanotube as the vertical connection between two copper wires, and b) SEM image of a cross-section of a carbon nanotube via [Kreupl, IEDM2004].

Before we delve deeper into CNTs properties and advancements, it is important to understand the flaws of current interconnect technologies and the imminent interconnect problems that the industry is currently facing.

Continued aggressive scaling into the deep nanometer regime has been an essential strategy to improve transistor performance—however, the reverse is happening for interconnects. Such scaling continually forces the semiconductor industry to search for new material combinations and innovative technological solutions to meet the demands set for future generations. The fabrication of interconnects is no exception to this trend. It was this driving force that forced the transition from Aluminium (Al) interconnects to dual Damascene Copper (Cu) interconnects a few decades ago, that proved to be a groundbreaking accomplishment in the field deep nanometer scale VLSI (Very Large Scale Integration) technology. Copper interconnects were introduced in 1998 and since 2001, the International Technology Roadmap for Semiconductors (ITRS [2]) highlighted problems with the resistivity increase as line widths approached electron mean free path. For example, Cu interconnects with dimensions in the order of the mean free

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path of electrons (~40 nm in Cu at room temperature) undergo resistance increase rapidly. This is due to the combined effects of enhanced grain boundary scattering, surface scattering and the presence of a highly resistive diffusion barrier layer surrounding the copper line [3,4]. Moreover, at nano-scale dimensions, the increase of Cu interconnect resistivity, in addition to the increasing current density (J), results in higher self-heating of interconnects.

By 2003, low-K insulator dielectrics were introduced to slow this pace. However, Cu resistivity continued to rise due to electron scattering. Additionally, yield issues associated with the integration of low-K materials with copper proved to be more challenging than expected. Also, low-K dielectrics with inherently lower thermal conductivity (i.e. $K_{th,\ ILD}$<0.4 W/mK) hinder heat conduction from interconnect layers to the heat sink. Vias and interconnects have a thermal conductivity in the range of $K_{th,\ Cu}$=385 W/mK. Nevertheless, thermal conductivity worsens when the back-end metal temperature (T_m) rises above the junction temperature [3]. Elevated temperatures along with scaling introduce reliability concerns on Cu lines with low-K dielectric also known as time dependent dielectric breakdown (TDDB). All these factors adversely affect electromigration (EM) lifetime of Cu interconnects which depends quadratically on J and exponentially on T_m [3]. ITRS [2] reports that current density limits for copper will be exceeded by 2017.

While some solutions have been found for the logic and memory applications up to 14nm node, there is an on-going race on contenders for replacing copper interconnects. Thinner barrier and adhesion layers, doping of metals to enhance the grain boundary conductance, and selective capping are some of the adopted solutions improving copper interconnects. Other short-term solutions to address the scaling challenges faced by Cu include load-aware redundant double vias to avoid EM issues [6], via prefill with alternate materials (like Cobalt) with higher current migration resistance and better fill [7], ultra-thin self-forming barriers (metal oxide barriers like MnO_x) to optimize the utilizable cross-section for Cu, alternative materials for better EM [8], reflow seed layers for defect reduction [9], etc. Nevertheless, these short-term steps aim to solve one or few of the Cu-foreseen issues at once and to combine them might prove to be impractical or just economically unfeasible. As we go beyond 10nm and 7nm nodes, novel interconnect materials and integration approaches are needed and are under investigation.

In digital logic design, local interconnects (interconnects closer to the device level, see Fig. 2) and intermediate interconnects tend to shrink with scaling. Thus, the impact of their delay is minor. Global interconnects (usually used for power/ground and clock) have the greatest wire lengths and widths, and are the most impacted by scaling. The problem is even more severe for memories. Metal bit lines (local metal layer) in memory cells have the most aggressive metal pitch, and their contact layer has the highest aspect ratio in all semiconductor devices. Therefore, they face the largest delay due to electron scattering. To date, potential solutions have been identified to solve these problems. Hence, the

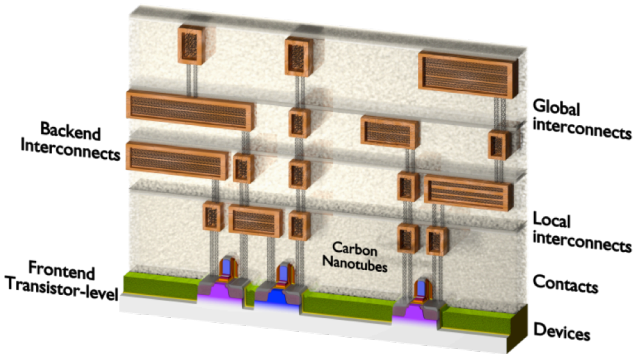

Figure 2. Illustration of an integrated circuit cross-section depicting devices and interconnects made with carbon nanotubes.

interconnect problem is acute, and the limits of copper interconnects are approaching fast.

Comparable to the paradigm shifting transition from Al to Cu dual damascene process in the late 1990s, new potential pathways of advanced metallization in the back end of line, addressing the aforementioned issues, need to be explored for future technology nodes. This very necessity has yielded a great number of ambitious concepts involving graphene-based interconnects [10], optical interconnects [11], organic interconnects, spintronic switches [12], alternative metals as well as alloys and composites.

Carbon nanotubes (CNTs) have aroused a lot of interest in their applicability as VLSI interconnects of the future because of their extremely desirable properties of high mechanical and thermal stability, high thermal conductivity and large current carrying capacity [13,14,15,16]. Due to strong sp2 bonding between carbon atoms, CNTs are much less susceptible to EM problems than copper interconnects and can carry high current densities [13]. Ballistic electronic transport can go over long nanotube lengths, 1 μm, enabling CNTs to carry very high currents with virtually no heating due to nearly 1D electronic structure. Metallic single-walled CNT bundles have been shown to be able to carry extremely high current densities of the order of 10^9 A/cm^2 [17]. In contrast, EM limits the current carrying capacity of Cu interconnects to ~10^6 A/cm^2 [18]. Copper interconnect with cross-section 100 nm x 50 nm can carry currents up to 50 μA, whereas a 1 nm diameter CNT can carry up to 20-25 μA current [19]. Hence, from a reliability perspective, a few CNTs are enough to match the current carrying capacity of a typical Cu interconnect. Although it should be noted, that the need to reduce interconnect resistance (and hence delay) makes it necessary to have CNTs with a minimum density of 0.096 per nm^2 [2], if pure CNT interconnects are used. Additionally, estimations based on measured thermal conductivity (K_{th}) on films of SWCNT bundles, combined with observations from electrical conductivity experiments, predict K_{th} in the range 3000-10000 W/mK [20] at room temperature, while $K_{th,\ Cu}$=385 W/mK. Hence, heat diffuses more efficiently through CNT vias than Cu vias and can reduce the on-chip temperature. Such properties also make CNTs desirable as vertical through-silicon via for three-dimensional (3D) integration. There is also progress on the commercial wafer-level scaling of CNTs.

Current state-of-the-art on CNT deposition is developed using equipment such as AIXTRON BM300T [116]. CNT growth occurs in a vertical flow reactor where gasses (ammonia, argon, acetylene, hydrogen, methane) can be injected to control the CNT growth and alignment. The growth chambers can be assembled into a cluster for high-volume production capacities.

In this paper, we overview the recent advancements of carbon nanotubes as interconnect material for nanoelectronics. The rest of the paper is organized as follows. CNT transport properties and modeling are described in Section II. Section III presents some of the research work related to CNT on-chip interconnects covering aspects on doping and composite CNTs for enhancing current density and lowering resistance. Section IV provides an overview on CNT-based through-silicon vias. Section V includes some of the on-going efforts on the chip design with CNT devices and interconnects for energy efficiency. Section VI provides an overview of the CNT characterization methods. Section VII describes the prospective research problems related to CNT interconnects and Section VIII concludes the paper.

II. Transport Properties of CNTs

In this section, we provide a brief description of CNT modeling. CNT properties such as band structure, electronic transport, and tunneling currents are now well understood and predicted by atomistic-level modeling. The modeling of CNT structures consists of two closely interlinked models: physical 'microscopic' modeling and compact/analytical 'macroscopic' modeling for circuit-level simulations. The modeling cycle starts from the development of an efficient physical simulation framework, based on first-principle methods such as density functional theory (DFT) combined with transport simulation models such as non-equilibrium Green's functions (NEGF) or Monte Carlo methods. Robust physics-based models allow a comprehensive theoretical study of CNTs and facilitate the design of high-performance systems. Physical models need continuous calibration with measured data to increase model accuracy and the predictive capabilities of simulation tools. Compact models are the interface between physical simulations and measurements. Compact models are based on extensive physical simulations and suitable for circuit simulations using standard SPICE-like circuit simulators [22]. Below is a brief survey of available macroscopic and microscopic models.

Macroscopic level modeling – compact models: From a circuit-simulation perspective, a generalized compact RLC model for CNT interconnects can be depicted as in Fig. 3 [23]. The model is also applicable to SWCNTs with a single shell. The model represents conductance, inductance, and capacitance. Each shell has a lumped ballistic resistance (R_i) and lumped contact resistance (R_c) due to imperfect metal nanotube contacts. These contacts are typically constructed of Gold, Palladium, or Rhodium [23]. The nanotubes also have a distributed ohmic resistance (R_o), which is dependent on length, l_b, and mean free path of acoustic phonon scattering (λ_{ap}). CNT resistance also depends on the applied bias voltage, $R_{hb} = V_{bias}/I_o$, where I_o is the maximum saturation current (I_o values 15 to 30 μA [24]). Between shells in MWCNTs, there

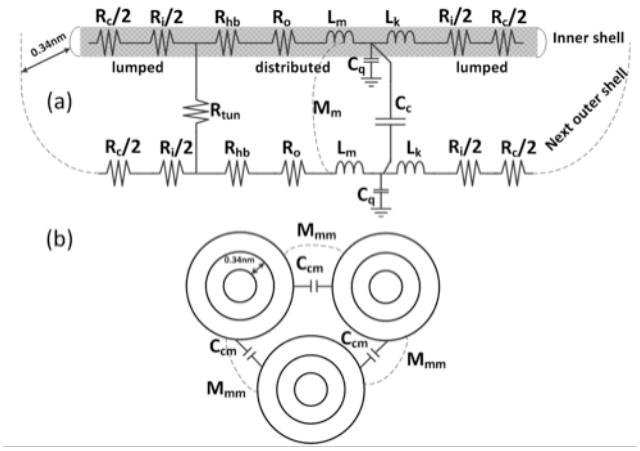

Figure 3. Illustration of compact RLC model for CNT interconnect.

is also an intershell tunneling resistance (R_{tun}). As the applied bias voltage to each shell is the same, the impact of R_{tun} is relatively small. All the aforementioned ballistic, ohmic and contact resistance depend on the number of 1-D conducting channels, N_c. For metallic SWCNTs, the number of conducting channels is always $N_c=2$ due to lattice degeneracy [25]. Carbon nanotubes have quantum, C_q (i.e. 193 aF/μm per conducting channel) and electrostatic capacitance, C_e. Additionally, there is coupling capacitance between 1) conducting shells inside MWCNTs, C_c and 2) one nanotube to another depending on their distance, C_{cm}. As for inductance, CNTs have kinetic L_k (i.e. 8 nH/μm per conducting shell) and magnetic inductance, L_m. There is also mutual inductance between shells and among CNT bundles.

The macroscopic circuit simulation addresses just the interconnect performance neglecting other important aspects like reliability and variability of CNTs, which can be adequately treated only at the mesoscopic level by employing fully three-dimensional (3D) Technology Computer Aided Design (TCAD) modeling approaches. Recently, industrial and scientific communities are investing considerable efforts to investigate the modeling of CNT variability and reliability utilizing 3D TCAD approaches for advanced technologies.

Microscopic level modeling: Besides macroscopic (circuit-level) and mesoscopic (TCAD level) modeling of CNT interconnects, it is also important to consider microscopic (Ab Initio level) modeling to understand the underlying physics. Significant work has been carried out on the electrical, [24-27] and thermal [28], [29] modeling of CNTs. Simulation tools on band structure and molecular level simulation tools can be found in [30]. For the modeling of the electronic and thermal properties of CNT structures, several methods have been successfully applied—models based DFT, the extended Hückel [31] or Slater-Koster [32] formalisms. Classical models have also been incorporated into commercial tools such as ATK-QuantumWise [33] allowing in-depth insight into the physical behavior of CNTs. Transport models such as NEGF and molecular dynamics are also widely available as part of commercial and open-source software packages such as LAMMPS [34] and GPAW [35].

Table I: Comparison of properties of Cu, SWCNT, MWCNT and Cu-CNT composites.

	Cu	SWCNT	MWCNT	Cu-CNT
Maximum current density (A/cm^2)	**< 1 x 10^7**	**> 1 x 10^9 [55]**	**> 1 x 10^9 [56]**	**6 x 10^8 [53]**
Thermal conductivity @ 300 K (W/mK)	**385**	**3000-10000 [52]**	**3000 [52]**	**~800 [54]**
Electron mean free path @ 300 K (nm)	**40**	**> 1000 [58]**	**> 25000 [57]**	
Conductivity (S/cm)	**5.8 x 10^5**	**7 x 10^5 [59]**	**2.7 x 10^5 [60]**	**2.3 - 4.7 x 10^5 [53]**

III. CNTs for On-Chip Interconnects

CNTs can be either single-wall (SWCNT) or multi-wall (MWCNT). Research papers on CNT interconnect date as early as 2002 [36]. It has been reported that SWCNT bundles with same dimensions as Cu/low-K interconnects can provide significant improvements [37], [38]. An arrangement of several SWCNTs has shown to reduce the resistance by as much as 50% and to help reduce the delay and power consumption, which can be particularly interesting for local interconnects [39]. As for MWCNTs, it was proven both theoretically and experimentally that all inner shells can conduct if properly connected [40], [41], [42], [43] and can potentially outperform Cu and SWCNTs. MWCNTs interconnects operating in the gigahertz frequency range, have been demonstrated. However their conductivity is considerably lower than the theoretical models predict, due to large defect density [44], [45]. More recently, researchers have designed and fabricated the first carbon nanotube computer [46], which operates on only 1-bit of information and uses a single instruction. Additionally, [47] and [48] have demonstrated 1GHz operation of carbon nanotube interconnects with silicon transistors. While these resemble a rudimentary computer design, they are significant advances to fabricate a circuit using only CNT field effect transistors and interconnects.

Thus, the enhanced properties of CNTs address most of the challenges faced by the current Cu-interconnect technology, especially the issues that rise due to its parasitic resistance and insufficient current carrying capacity. Table 1 shows the comparison between Cu, single-walled (SWCNT) and multi-walled CNTs (MWCNT). Specifically, Fig. 4 shows the theoretical resistivity comparison among Cu wire and MWCNTs for different lengths and diameters up to 32nm [49]. For a larger diameter of MWCNTs, resistivity values are shown in Fig. 5. They show that for long lengths (>10um), the theoretical resistivity of MWCNTs is several times lower that Cu wires and become comparable to that of SWCNTs. These characteristics highlight the potential of CNTs for interconnects that drive the enormous technological efforts realized in the past 15 years to integrate CNTs in back-end-of-line semiconductor device fabrication.

From a processing point of view, the most widespread and most studied approach to integrating CNTs in interconnects is to directly grow CNTs in the desired structures by catalytic chemical vapor deposition (CCVD). Most efforts so far were devoted to the fabrication of vertical *via* interconnects, and a number of integration process flows were developed to selectively grow densely packed bundles of CNTs on the metallic bottom electrode and to contact the other end of the CNTs with a top metal [61]. Recently, an original integration approach relying on the report of CNT plugs in via holes was also introduced [62]. As for horizontal interconnects, fewer reports exist and mostly rely either on the direct horizontal growth of CNTs on dedicated vertical structures [63]; or on

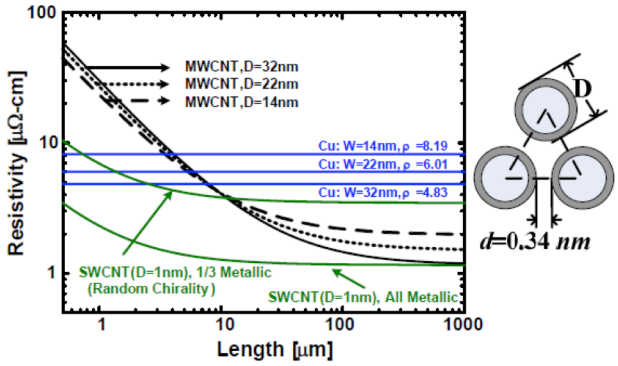

Figure 4. Comparison of resistivity of MWCNT bundles with Cu wires. The dimension of Cu wires are adopted from ITRS [49].

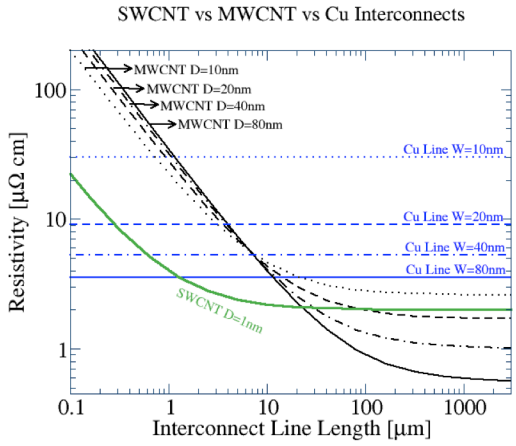

Figure 5. Comparison of resistivity of MWCNTs with Cu wires using analytical models for Cu and CNT materials [50-51].

the vertical growth of CNTs followed by subsequent horizontal alignment [64, 65]. It should be noted that alternative processes based on the assembly of CNTs from solutions were also considered [66]. Despite the significant improvements realized regarding CNT integration, there are still several processes and reliability related challenges that need to be addressed before CNTs can enter as mainstream VLSI interconnects. Presently, the realization of good electrical contacts with metallic electrodes remains a challenge. This is particularly problematic for vertical interconnects where the bottom electrode acts both as a support for the catalytic growth of CNTs and as an electrical contact [67,119]. Another major roadblock comes from the fact than one ideally desires to inject current alongside the axis of the CNT to create a so-called *end-bonded* contact to the CNTs, which requires a perfect control over the quality of the interface between open-ended CNTs and metal [68].

In addition to contact issues, the electrical performances of CNTs integrated as interconnects are systematically lower than those of copper or the prediction of theoretical models, regardless of the process flow for vertical or horizontal alignment. Regarding resistivity, the lowest values reported fall in the range of 0.5 to 1 mΩ.cm, i.e. at least two orders of magnitude higher than the resistivity of aggressively scaled Cu interconnects [65, 67, 69-71]. These reduced performances can be explained by two main factors: (1) the quality of the CNTs produced by CCVD, which is a relatively low-temperature process compared to arc-based processes; and (2) the non-ideal packing density of CNTs in integrated interconnects. The latter was much improved by increasing the CNT growth density in the 10^{13} cm^{-2} range [67, 119], but it is however inherently limited by the tortuosity of the CNTs produced by CCVD. Even after liquid-induced compaction of the CNT bundles, the packing density of CNTs in interconnect structures is still rather low. Due to current technological challenges, CNT interconnects are unlikely to replace all copper interconnects at once but rather gradually—introducing hybrid structures such as doped and metal composite CNTs.

A. Doped CNTs

As already mentioned above, over the recent years there have been many advancements in process and growth of CNTs interconnects and more specifically for vertical lines. Currently, several growth techniques have been established to synthesize carbon nanotubes at workable temperature levels for microelectronics process (i.e. below 450°C) with the ability to control nanotube dimensions, density (i.e. up to 10^{13} CNTs cm^{-2}) and patterning at specific locations [72], [73], [74], [75], [67], [119]. However, the design of catalyst to control nanotube chirality and especially for metallic nanotubes is very challenging [75], [76]. It is one of the main challenges for CNT interconnects to design catalyst and process conditions that simultaneously give ultra-high area densities, chiral selectivity, and growth on conductive support layers [77].

However, doping carbon nanotubes is an alternative to reducing resistivity without the need for chirality control since all doped tubes behave as metals irrespective of their semiconducting or metallic character in the neutral state [118]. Indeed, whichever approach is used to dope the CNTs, i.e. substitutional doping, internal (endohedral) doping, or external doping, the transport properties are affected by shifting the Fermi level and thus changing the number of conduction channels per CNT. Two- to four-fold improvement in the conductivity of horizontal CNT interconnects was already demonstrated using external doping by platinum salts [66] or iodine vapor [78, 79]. The temporal and thermal stability of such charge transfer based doping process, however, needs to be carefully studied. In this respect, substitutional or internal doping may be more robust.

Recently, an interesting alternative relying on the coating of CNTs by a thin film of evaporated MoO_3 was reported [77]. Significant decreases in resistivity were obtained up to 50 μΩcm, which is the lowest resistivity value measured to date on nanotube bundles while maintaining a highly ordered alignment [77]. The improved electrical resistivity was attributed both to the shift of the Fermi energy of semiconducting nanotubes (i.e. doping by charge transfer) and to the conversion of the MoO_3 oxide into a layer of metallic character [77].

Doped CNTs might be potential candidates for replacing on-chip local interconnects due to lower resistivity for short interconnect lengths typically used for local interconnects. For small dimension interconnects (< 10 nm diameter), which would be made of only a few carbon shells in parallel and would thus exhibit large performance variability due to the random distribution of semiconducting and metallic shells, one can also expect doping to reduce this variability by causing all shells to conduct.

B. Composite CNTs

Cu-CNT composite interconnects can be potential replacements of global copper interconnects. Global interconnects for supply voltage delivery are susceptible to electromigration issues due to a large amount of unidirectional current flowing for an extended period of times, which ultimately cause atoms to migrate by creating voids and hillocks. To circumvent this issue, combinations of CNTs with copper were envisioned soon after the pioneering studies about CNT interconnects [80]. In [81,82,83], initial experiments were conducted on "bulk" approach where a mixture of CNTs and Cu is deposited from a solution to target substrate. This approach demonstrated a mitigated performance for interconnects such that the focus now is exclusively on composite materials where CNT alignment is controlled by current flow (referred to as aligned CNT-Cu composite).

Chai et al. [85-87] first demonstrated the fabrication of vertical interconnects using aligned CNT-Cu composite materials in 2007 where vertically aligned CNTs were grown before electroplating was used to fill the voids between CNTs with Cu. They demonstrated that the composite material could reach low, Cu-like, resistivity, however, more resistant to electromigration than copper. More recently, a renewed interest for composite CNTs was generated by [84] claiming a

100 fold increase in current carrying capacity of aligned CNT-Cu material compared to pure Cu while maintaining Cu-like conductivity (see Fig. 6). The integration of aligned CNT-Cu composite materials in interconnect structures is now actively studied [88-92] and can lead to significant performance gain and reliability enhancement of integrated circuits.

The benefits such as robustness, fabrication and economic feasibility of introducing aligned CNT-Cu composites in the semiconductor interconnects technology are immense. This might prove to be one of the most promising short-term solutions to pave the way for a paradigm shift of on-chip interconnects.

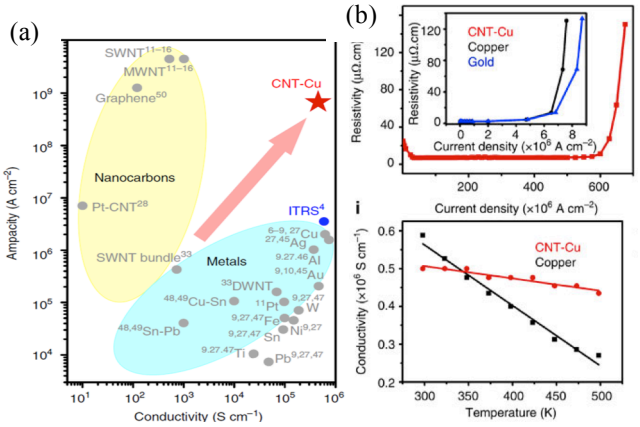

Figure 6. Properties of Cu-CNT composite. a) improvement of current density vs. conductivity. b) Cu-CNT resistivity comparison with copper [84].

IV. CNTs Through-Silicon Vias

An important application of CNTs is also their use as vertical via interconnect. As future high-performance systems will demand large memory bandwidth, the state of the art of off-chip interconnects (i.e. 25pJ/bit) needs to be further improved to allow for low power, fast and high bandwidth interconnects. Three-Dimensional (3D) integration is one of the most promising technologies for System-on-Chip (SoC) developments and a viable solution for heterogeneous integration (i.e. processors, memory, digital, analog, mems, sensors, harvesters, etc.). Through-Silicon-Vias (TSVs) are the key enablers of 3D integration by providing continuous connections between different stacked dies. TSVs are etched in the silicon substrate and filled either with copper or Tungsten (W). However, these materials have limitations due to the highly demanding fabrication process, reliability, manufacturability, and performance. In the recent years, a lot of research efforts have been dedicated to the development of carbon nanotube-based TSVs for 3D integration. CNT TSVs present an opportunity to further progress packaging technology and enable high-density interconnects.

CNT TSVs are extensively investigated, and several research groups have successfully implemented growth and realized functional integration of multi-wall CNT bundles as high aspect ratio TSVs. In [93], CNT TSV bundles were grown in sub-5μm diameter on top of metal lines in a bottom-up approach, which is compatible with CMOS process temperatures (see Fig. 7). In [95], integration scheme for CNT-based TSVs are demonstrated for two scenarios 1) connecting two TSVs and 2) connecting a TSV to a metal pad. Authors reported on integration scheme for vias 100 μm in diameter and 132 μm deep and resistance values of 46 Ω and 9.8 Ω were obtained for via and contact, respectively. In [94], CNT TSV bundles with 50 μm length and aspect ratio 5 or 10 were demonstrated. CNT bundle resistance of 69.7 Ω was reported. Further improvement on integration scheme and

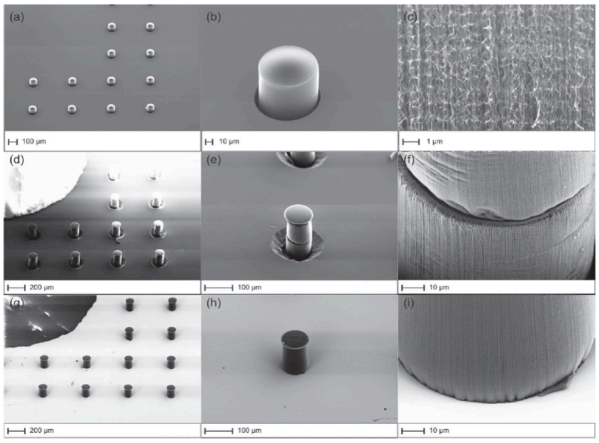

Figure 7. Scanning electron microscopy images of through-silicon vias filled with carbon nanotubes for 3D stacking of logic with memory [95].

lowering contact resistance of vias are required for enabling seamless integration of CNT TSVs as off-chip interconnects.

V. CNT-Aware VLSI Design Methods

To overcome the challenges of processing highly aligned CNTs (i.e. either for devices or interconnect), there is a lot of on-going research on circuit design methods that take into account misalignment and mispositioned CNTs to design functionally correct and reliable circuits. Thus, circuit designers are looking into efficient methods to design reliable, energy efficient and high-performance circuits despite the fact that CNTs might have defects. One effective method that has been applied by [96] is that after transferring CNT-based field effect transistors (CNTFETs) or CNT interconnects, regions of misalignments are identified and are etched away by using lithography. These techniques are known as CNT removal after CNT growth by electrical burning [97] or selective etching [98].

A strong motivation for this work is that disregarding defective chips (i.e. misaligned, mispositioned CNTs) or reconfiguring around defective devices and interconnects may be very expensive and simply not feasible due to complexity in processing methods. Moreover, traditional fault-tolerance techniques (i.e. redundancy) might not be applicable due to a large area and power overhead. Hence, many research efforts are focused on defective CNT-immune design techniques while having a minimal impact on existing design flows.

Additionally, considerable progress has been made towards full wafer-level CNT-based digital systems. Recently, researchers [46] have demonstrated the first processor design with CNT field effect transistors and developed VLSI-compatible design techniques to overcome the challenges of CNT imperfections [99].

To explore energy efficiency of carbon nanotube-based circuits and recent advancements on nano-engineering, researchers have presented a design approach that capitalizes on several recent nanotechnology breakthroughs called N3XT [99]. The main thrust of N3XT is to include high performance and energy efficient devices based on CNTs, combined with large amount of nonvolatile memory (such as low-voltage resistive RAM and magnetoresistive memories as spin-transfer torque magnetic RAM, STT-MRAM) and new microarchitectures for scalable computing that are all implemented in fine-grained (monolithic) 3D integration with ultra dense CNT interconnects between logic and memory layers. Exploiting the progress on each technology enables new system integration that promises high energy-efficiency and high-performance.

VI. CNT Characterization

Suitable characterization techniques are essential for the successful integration of CNT interconnects and evaluation of development prototypes.

For a CNT-based interconnect technology, electrical measurements are necessary for verifying the expected high conductivities and are required for optimization of doping and contact technology. The main challenge of electrical characterization is the formation of suitable contacts. The first successful attempts at defining metal contacts on single CNTs have already been reported in the late 1990s, along with the first experimental studies of their electrical properties [100-102]. Today, even though the contacting of single CNTs was demonstrated and nanoscale devices based on CNTs can be built and characterized [103] – the realization of transparent ohmic electrical contacts is still challenging [68].

CNT interconnect technology promises improved thermal properties with reduced self-heating and improved thermal coupling to the heat sink. To maximize the potential benefits, thermal characterization techniques are crucial. One approach to studying the thermal properties of single, metallic CNTs is deriving them from their current-voltage (I-V) characteristics under bias conditions where Joule heating leads to non-ohmic behavior [104]. This approach can yield the global thermal conductivity of a single CNT line, but a valid electro-thermal model is needed to extract the data. Moreover, the approach cannot resolve non-homogeneous thermal conductivity distributions or the formation of hot spots.

Optical approaches are fast and contact-less, but diffraction limits their spatial resolution. The temperature-induced shift of the **G** bands in CNTs can be measured using Raman spectroscopy [105-107]. This way, the local temperature and thermal conductivity along the axis of self-heated CNT lines can be obtained with sub-micron lateral resolution. A second laser source can be used for rapid local heating of the CNT [108]. Infrared thermometry was also successfully applied to image local heat dissipation in carbon nanotube network (CNN) transistors. The technology might be applicable for interconnect structures made from bundled CNTs.

Scanning probe-based thermometry techniques are not diffraction-limited and therefore achieve the highest reported spatial resolutions. Scanning Joule Expansion Microscopy (SJEM) has been applied to study the thermal properties of an array of parallel, single CNT lines embedded in PMMA [109]. By measuring the thermal expansion of the CNTs and the surrounding PMMA - metallic and semiconducting CNTs could be distinguished, the local temperature could be obtained with a lateral resolution of 100 nm and local hot-spot formation could be observed. Moreover, the point where the thermal breakdown would occur can be accurately predicted. To reach even higher performances, specialized tips can be used in so-called scanning thermal microscopy (SThM).

One such approach, in which the passive atomic force microscope (AFM) tip is replaced with a nanoscale thermocouple [110], has been applied to single CNTs [109]. Self-heating of a single CNT could be resolved with a lateral resolution of 50 nm. A novel SThM approach, relying on a cantilevered tip with integrated heater, recently demonstrated a lateral resolution of 10 nm [111]. This approach has also been used to study the thermal transport into graphene [112] and is a promising candidate for high-resolution thermometry of single CNTs. Thermal and electrical properties of CNTs strongly depend on their morphology and structure. The properties of SWCNTs are to a large extent determined by their chirality. Defects in the honeycomb lattice can affect the properties of both SWCNTs and MWCNTs. Impurities in the lattice—such as doping atoms—can have a strong impact as well. It is thus important to characterize morphology and structure of CNT interconnects alongside their thermal and electrical properties.

For morphological and structural characterization of CNTs on an individual level, only a few technologies are suitable. Among them are scanning tunneling microscopy (STM) and transmission electron microscopy (TEM) [113]. While STM can also yield information on the electronic density of states, a conductive substrate is necessary, which makes the approach rather suited for primary CNT research. TEM, on the other hand, can be applied to suspended CNTs, to allow in-situ investigations with atomic resolution imaging. Today, using low-voltage aberration corrected TEM technologies, dopant atoms and nanostructures that have been filled inside CNTs can be visualized [114] while imaging morphology and potential defects at the atomic scale simultaneously. It is possible to identify in a precise manner the location and type of defects and contaminations on a CNTs surface. Damage introduced by electron irradiation may nowadays be kept at a minimum. Moreover, the position and atomic structure of dopant atoms can be characterized [115] The information gained from *in-situ* TEM measurements can be expected to enable a more direct comparison of theory and experimental data and might provide insights into the mechanisms that shape the electrical and thermal properties of CNT interconnects.

VII. Research Prospects

Carbon nanotubes present viable solutions to overcome the current challenges with copper interconnect technology. The challenge of introducing CNTs in integrated circuits is not just in the processing technology. The scientific community still lacks the know-how to exploit CNTs both as devices and interconnects. Understandings such as to what extent CNTs can be exploited for reliable and efficient interconnect architectures; are certain device technologies more suitable to be integrated with CNTs and give best performance; and how to design optimal circuits despite of having non-perfect CNTs are significant challenges to be addressed if we are to truly find a replacement material for copper.

Research efforts related to physical modeling, physical design, design space exploration, CNT processing and characterization are gaining momentum and will provide a clearer picture of the costs and benefits of integrating CNTs as on-chip interconnects [117]. With respect to modeling, electro-thermal modeling and simulation tools are needed to evaluate the performance, reliability and variability of CNTs and composite Cu-CNT interconnects. It can also help to assess the impact of CNT-metal contacts. In this context, a multi-scale physics-based simulation platform (from ab-initio material simulation to circuit-level) that considers all aspects of VLSI interconnects (i.e. performance, power, and reliability) is desirable to explore and evaluate the potential of CNT technology. Regarding circuit design, novel VLSI design methods are needed to take into account the peculiarities of CNT process and its variability issues. Such design methods will enable design space exploration of carbon nanotube circuits. On the processing side, continued efforts are needed on the CCVD growth of CNTs both to produce high-quality CNTs at a reasonable temperature, but also to reduce the CNT tortuosity and increase their packing density in interconnects. There is also a large effort, which is necessary, to integrate CNTs into the back-end-of-line fabrication process. Challenges arise from high planarity CMP processes, temperature budget (i.e. 350^{o}C) and contamination management. Stable doping of CNTs at the operating temperature of circuits still needs to be developed and integrated into back-end-of-line processing. The fabrication of aligned CNT-Cu composite material requires specific developments, and the corresponding electrical conduction mechanism needs to be carefully studied. On characterization, there is a need for structural and morphological CNT-level electrical and thermal characterization. In summary, there are a lot of research efforts required into enabling CNTs to be embedded on-chip and become widely deployed in the semiconductor industry.

VIII. Conclusions

In this paper, we provide an overview of the advancements of carbon nanotube based interconnects. There is a lot of on-going research focused on the processing and growth of carbon nanotube interconnects for achieving high density, directional growth, and well-aligned carbon nanotubes. To allow integration of CNT interconnects as on-chip interconnects, there are two short-term solutions being explored by the community. Doped CNTs present interesting properties to be used as local interconnects by reducing their resistance. Metal-CNT composite materials are also being investigated as a potential replacement for global copper interconnects to allow high current densities. To further increase package density and bandwidth, carbon nanotube based through-silicon-vias allow faster, denser and reliable off-chip interconnects and can thus be expected to lead to advancements in other fields of nanoelectronics, such as CNT-based-devices, non-volatile memories, and 3D integration. CNTs present new opportunities for designing energy efficient, high-bandwidth and high-performance circuits and systems.

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