A Multiphysics Modeling and Experimental Analysis of Pressure Contacts in Power Electronics Applications

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Abstract—This paper details a modeling and experimental assessment of the packaging process for a silicon carbide Schottky diode using pressure contacts. The work detailed in this paper is original, as it applies a combined electrothermomechanical modeling analysis to this packaging method supported by experimental validation. A key design objective for this packaging process is to identify suitable contact pad materials, heatsinks, and process variables such as clamping force to meet electrical, thermal, and reliability specifications. Molybdenum and aluminum graphite (ALG) have been identified as two suitable materials for the contact pads. Clamping forces ranging from 300 to 500 N and electric current ranging from 10 to 30 A have been investigated in terms of the resulting electrical and thermal contact resistances, temperatures, and stresses induced across the package. The performance of two heatsink designs with heat dissipation rates of 12893 and 4991 W/m²k has also been investigated. Both the modeling and initial experimental results detailed in this paper show that ALG provides better performance in terms of generating a lower average chip temperature. Both temperature and stress in the diode are predicted as a function of clamping force and load current. This will aid the packaging engineer to identify suitable process parameters to meet junction temperature requirements at different applied load currents.

Index Terms—Diode, power electronic module (PEM), press pack.

I. INTRODUCTION

I N THIS paper, a multiphysics (electrothermomechanical) modeling and analysis is presented and compared to experimental results for a press-pack diode (PPD) in a power electronic module applications. The thermomechanical characteristics of the pressure contact packaging system offer certain advantages since the majority of the failure mechanisms in power electronics modules are associated with bonded joints such as solder joints and wirebonds [1]. Eliminating both

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Fig. 1. Cross-sectional view of the press-pack structure.

wirebonds and solder joints helps to minimize the risk of fatigue failure, hence providing an enhanced reliability.

In a press-pack module, (also named as flat pack in some of the literature), the power semiconductor is pressed between two conductive copper elements using an intermediate contact material to match the coefficient of thermal expansion (CTE) of the copper and the semiconductor. The press-pack module is assembled and mounted under pressure by a complex mechanical system [2] in order to obtain the necessary pressure contact between the interfaces in the package. Other advantages of press pack assembly in power electronics applications are compact design, double-sided cooling, and reduction in rigid interconnection between materials of different CTE [3].

In contrast to fully bonded interfaces such as solder joint and wirebond, press-pack interfaces introduce additional electrical and thermal contact or constriction resistances due to interface surface nonlinearity and roughness. This results in higher electrical resistance, which together with higher thermal contact resistance results in higher temperatures. However, even with these challenges, press-pack modules have advantages over fully bonded interfaces.

Some of the key design questions that arise when using pressure contacts (as in Fig. 1) are the choice of contact pad material and the determination of the optimal clamping pressure, which will affect both the junction temperature and stress on the SiC Schottky diode. This was the motivation behind this work and the development of a multiphysics modeling and validation with experimental results.

A finite-element analysis (FEA) study on press-pack insulated bipolar transistor (PPIGBT) was reported by Hasmasan *et al.* [4] for the impact of mechanical clamping pressure on the thermal distribution among the chips. That paper concluded that nonuniform clamping pressure condition

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affects the distributions in current, junction temperature, and power loss, which leads to reduction in lifetime. Another FEA study on PPIGBT was reported by Poller *et al.* [5], [6], who investigated the effect of external clamping pressure on the stress, temperature, and current distributions on the IGBT chips for three different clamping kits. The simulation results were validated with experimental results.

A mechanical FEA study was presented by Hasamasan *et al.* [7] for PPIGBT to evaluate the clamping pressure distribution among chips for uniform and nonuniform clamping pressure situations for various friction coefficients (FCs) between interface layers. This paper concluded that FCs between layers have little impact on pressure distribution on the chip.

A similar study on PPIGBT was also reported by Pirondi *et al.* [8], [9]. That paper concluded that for single-chip configuration, the pressure distribution on the chip behaves like a convex shape. In contrast for multichip configuration, pressure distribution in the chips behaves like concave shape. An FEA on PPD by direct coupling of electrothermomechanical analysis is proposed in this paper. Additionally, two different contact pad materials were utilized in this paper in order to identify the impact of the material on the thermomechanical properties of the press-pack assembly.

In order to model the electrothermomechanical characteristics of the PPD structure accurately, the values of the electrical and thermal contact resistances between contacts interfaces need to be known *a priori*. Measuring the pressure-sensitive contact resistances experimentally is very difficult due to placing the measuring probe closer to the contact surface in small press-pack packages.

A number of approaches have been reported in the literature for predicting contact resistances. Poller *et al.* [10] proposed a method to predict the electrical and thermal contact resistances by combining the finite-element results with experiments. The experimental measurements were extracted from the surface of the IGBT chip of the press-pack assembly. The method proposed by Poller *et al.* [10] utilizes an iterative algorithm (genetic search algorithm) to estimate both contact resistances by changing the estimate iteratively to match the results of FEM simulations with the experimental measurements. Busca *et al.* [11] predicted the thermal contact resistance of IGBT press-pack structure by combining experimental data with dynamic component-level thermal models (physical cauer equivalent circuit network).

From a design perspective, the above approaches are resource-consuming and expensive. Hence, in this paper, we have employed an approach that uses analytical models to estimate the contact resistances on the molybdenum (Mo) [or aluminum graphite (ALG)]/ Cu and Mo (or ALG)/SiC interfaces. These models are dependent and are described in Section III.

II. PRESS-PACK MODULE

In this paper, finite-element modeling analysis has been undertaken for a prototype of a PPD structure. The PPD consists of an anode, anode pad, a SiC Schottky diode chip, cathode pad, and cathode layers. The material of anode and



Fig. 2. (a) Press-pack prototype, including the external case. (b) Detail of the assembled clamp with the press-pack diode.

cathode is copper. Two types of contact pad materials have been selected as possible candidates. These are Mo and ALG from Schunk Hoffmann Carbon Technology [12]. ALG is a metal matrix composite produced by pressure infiltration of porous graphite by liquid aluminum. According to manufacturers' specification, this new composite incorporates the advantageous properties of both materials. The type of ALG that was used in this paper is ALG 2208.

A Cree/Wolfspeed manufactured silicon carbide Schottky diode with datasheet reference CPW5-1200-Z050B was used in the module. Enclosing the diode is a polypropylene sulfide (PPS) die carrier, used for positioning the elements of the assembly as shown in Fig. 1. The external clamping force was applied using a commercial clamping kit and heatsinks. The module internal interface layers are pressed by the external force exerted by the clamping kit in order to establish the appropriate electrical and thermal contact at the interfaces of the assembly. An external case made of polyether ether ketone was used for aligning the copper poles. A detailed view of the real prototype and the assembled clamp is shown in Fig. 2.

III. FINITE-ELEMENT MODELING

The finite-element modeling captures direct coupling between the physics involving joule heating, thermal expansion, and subsequent mechanical deformation and hence stresses on the structure. By exploiting symmetry in the module, one-quarter symmetry has been utilized in this paper. The model of the press-pack package was developed in the finite-element code ANSYS [13]. Complexity of the model structure can be further reduced by representing the effect of the heatsink as an equivalent heat transfer coefficient. This is detailed in the following.

The temperature-dependent forward voltage of the SiC Schottky diode was extracted from the forward characteristics given on the datasheet. The material properties used in this paper are detailed in Table I. In ANSYS, surface-to-surface contact elements CONTA174 and TARGE170 were utilized for the contact interfaces in the model. CONTA174 and TARGE170 are surface elements with 3 degrees of freedom at nodes which these surfaces are associated with, and the geometric characteristic of these surface elements is same as the associated solid element (in this paper, SOLID226). Coulomb and shear stress friction exists between contact and target surfaces. The volume of the structure was discretised using SOLID226 element that has electrothermomechanical

 TABLE I

 MATERIAL PROPERTIES OF PRESS-PACK MODELING

Material Property	Мо	AlG2208	Cu	PPS	SiC
Density (Kg/m ³)	10220	2300	8930	1350	3210
Poisson Ratio	0.38	x,y:0.16 z:0.2	0.34 3	0.3	0.14
CTE(µm/m°C)	5.35	x,y:8 z:12	16.4	49	4
Young's Modulus (GPa)	330	33	110	4.34	476
Thermal conductivity (W/m°C)	138	x,y:220 z:140	385	0.25 5	370
Specific Heat (J/Kg/C)	217	800-950	385	-	750
Resistivity (Ω/m)	5.3e-8	x,y : 4e-7 z : 6e-7	1.6e- 8	1e14	Model



Fig. 3. Cross section of the meshed model of the press-pack diode ANSYS.

capabilities. After undertaking a mesh sensitivity analysis, a model consisting of approximately 20000 elements was used for all investigations, as shown in Fig. 3.

A. Thermal Contact Resistance

Contact interfaces are never perfectly flat due to surface roughness. Thermal contact resistance depends on the surface, material hardness, and contact pressure at the interface. Assuming that heat transfer is dominated by conduction at these interfaces, then the following equation can be used for thermal contact resistance [14]:

$$\frac{1}{R_{\text{Thermal}}} = \frac{2.5k_1k_2}{(k_1 + k_2)} \frac{m}{\sigma} \left(\frac{P}{H}\right)^{0.95} \tag{1}$$

where k_1 and k_2 are the thermal conductivities of the contacting materials. The parameters σ , m, P, and H are, respectively, the effective root mean square (rms) of surface roughness, mean absolute slope of the interface as in Fig. 4, contact pressure of the joint, and hardness of the softer material. If the mean absolute slope (m) is not available, then mean absolute asperity slope can be approximated by the correlation equation

$$m = 0.125(\sigma \times 10^6)^{0.402} \tag{2}$$

which is valid for an effective rms of surface roughness (σ) range of 0.216 μ m $\leq \sigma \leq$ 9.6 μ m [15]. The effective rms (σ) values calculated in this paper are within the range



Fig. 4. Rough surface schematic.



Fig. 5. Characterization of the surface of the ALG contact.

of 0.216–9.6 μ m. The average rms surface roughness of the Mo and ALG contacts was characterized obtaining 1.1 μ m for the ALG contacts and 1 μ m for the Mo contacts. The characterized surface of the ALG is shown in Fig. 5.

B. Electrical Contact Resistance

Electrical contact resistance also depends on the contact force and the hardness of the contacting materials. When electrical current passes through the contact interface, the current lines are restricted to pass through the reduced contacting area; this will result in an increase in electrical resistance at the interface. Assuming that the asperities at the SiC and pad surfaces form circular contact areas, then the following equation can be used to predict electrical contact [16], [17]:

$$R_{\text{Elec_Con}} = \frac{(\rho_1 + \rho_2)}{4} \sqrt{\frac{\pi H}{F}}$$
(3)

where ρ_1 , ρ_2 , and *F* are, respectively, electrical resistivity of the materials 1 and 2 and applied force on the contact joint. The above equation is widely used by design engineers to estimate the contact resistance. The equation is valid over a wide range of applied loads and contact materials [17]. Other more complex models (requiring additional materials data) are also available [18]. The Vickers hardness of the ALG was chosen as 441 MPa [19], and Mo was chosen as 1530 MPa [19].

C. Boundary Condition

In the mechanical analysis, the mechanical contact between contacting surfaces is controlled by friction.



Fig. 6. Single-sided heatsink and box clamp assemblies for the press-pack prototype. (a) Large heatsink. (b) Small heatsink.

An FC of 0.75 was assumed between contact layers Cu/Mo (or ALG). Similarly FC of 0.5 is assumed for SiC/Mo (or ALG) interface [10]. Clamping pressure varies for single-diode package, hence a quarter of the original intended pressure was applied on the one-quarter model we simulated. Electric current was applied to anode/heatsink interface by coupling the finite-element mesh nodes and applying the current load to the master node.

D. Single-Sided Cooling

Estimating the impact of the heatsink with a suitable heat transfer coefficient is detailed as follows. Natural free-flow convection coefficient is assigned as 10 W/m²k based on [21, Table 9.1]. From the heatsink manufacturers' specifications, the surface area of the heatsink can be extracted. Hence, the heat transfer coefficient representing the heatsink was approximated as h_{Heatsink} as in the following:

$$h_{\text{Heatsink}} = \frac{A_{\text{Heatsink}}}{A_{\text{Interface}}} \times h_{\text{Natural Convection}}$$
(4)

where A_{Heatsink} is the heatsink surface area exposed to the natural free-flow convection, $A_{\text{Interface}}$ is the model interface area between the anode (cathode), and $h_{\text{Natural Convection}}$ is the standard natural free-flow convection coefficient. Two commercial heatsinks (recommended for press-pack assemblies) have been investigated: a large heatsink model PS260/150B and a small heatsink model PS136/150B, both from GD rectifiers [22]. The rationale for using the large and small heatsinks was to investigate the impact of heatsink size of heat extraction. For the large heatsink and small heatsink, the heat transfer coefficients were approximated as 12893 and 4991 W/m²k, respectively. The complete assembly for both heatsinks is shown in Fig. 6.

IV. SIMULATION AND RESULTS

Using the developed model as detailed above, the combined loading of current, clamping pressure, and two different contact pad materials (Mo or ALG) have been simulated. Electrical and thermal contact resistances were dominated by the clamping pressure; for example, if clamping pressure increases, then the contact resistances decreases, but the stresses on the chip increases. The average von Mises stress on chip and the average temperature on the chip were extracted by volume weighted averaging method, which is widely reported



Fig. 7. For AlG contact pad, 400-N clamping force, 20-A loading and for large heatsink. (a) Temperature ($^{\circ}$ K) distribution on the structure. (b) Electric potential (V) distribution on the structure.



Fig. 8. Temperature ($^{\circ}$ K) distributions on diode for 20-A loading, 400-N clamping force, and with large heatsink. (a) Model with Mo pad. (b) Model with ALG pad.



Fig. 9. Average temperature (°C) plot versus clamping force (N) of diode on model with small heatsink (PS136) for 20- and 25-A loadings.

in the literature. The plots of temperature and electric potential distributions of the structure are given in Fig. 7.

A. Thermal Distribution on the Diode

Fig. 8 illustrates the temperature distribution on the diode chip for 400-N constant clamping force for both Mo and ALG contact pads. Clearly, the use of an ALG pad is resulting in a lower temperature distribution across the diode compared to Mo pad. This trend (as in Figs. 9 and 10) was also observed for other clamping pressure, electrical loadings, and heatsink designs combination.

By considering the temperature distribution on the diode chip as dominant factor, the model with ALG contact pad outperforms the model with Mo contact pad. This observation agrees with our expectation since the hardness value of ALG is low in comparison to the hardness value of Mo, hence small



Fig. 10. Average temperature ($^{\circ}$ C) plot versus clamping force (N) of diode on model with large heatsink (PS260) for 20- and 25-A loadings.



Fig. 11. Average temperature (°C) plot versus loading current (A) of diode on models with 300-N clamping force.

electrical and thermal contact resistances and consequently small average temperature on the model with ALG pad. As expected, increasing the load current value increases the diode temperature distribution (as in Fig. 11) for both models (ALG and Mo contact pads).

- 1) The predicted temperature reduction when using a small heatsink compared to the large heatsink for load currents ranging from 20 and 25 A are, respectively, ~ 13 °C and ~ 24 °C as detailed in Figs. 9 and 10. This trend was observed for the models with both contact pad materials.
- 2) For identical heatsink (either large heatsink or small heatsink) models, the average temperature difference of the chip between the model with Mo contact pad and the model with ALG contact pad for load current of 25 A is in the range of 10 °C−16 °C, and for load current of 20 A, the average temperature difference on the chip is in the range of 6 °C−10 °C.

It should be noted that the predicted difference between maximum and average temperature across the diode is <5 °C in all simulations. Hence, the reported temperatures are representative of the junction temperature in the diode. For silicon carbide, the maximum operating junction temperature based on manufacturers' specification should not exceed 175 °C. Hence, for even small heatsink, the chip temperature at 25-A load current is within the operating temperature regime. This can provide benefits when smaller form factor of the overall assembly is required.

B. Stress Distribution on the Diode

The von Mises stress distributions on the diode for both contact pad material models using 400-N clamping force and



Fig. 12. Von Mises stress (N) distributions of diode for 20-A loading and 400-N clamping force, and with large heatsink. (a) On diode with Mo pad. (b) On diode with ALG pad.



Fig. 13. Average von Mises stress (MPa) on diode plot versus clamping force (N) on models with small heatsink (PS136) for 10- and 15-A loadings.

20-A current loading are illustrated in Fig. 12. Unlike the trends observed for temperature, the average von Mises stress in the diode is higher for ALG contact pad compared to Mo contact pad. This trend (as in Fig. 13) was also observed for various load currents, clamping pressures, and heatsinks model combinations.

The maximum stress on the chip observed in the FEA simulation is 190 MPa. It should be noted that the yield stress of SiC is 21 GPa [23]. According to Sharp *et al.* [24], the fracture strength of smooth SiC of any shaped specimen is in the range of 0.5–1.5 GPa. Additionally in the experiment, we have not observed any crack in the chip for both contact pad materials. Hence, these predicted stresses in the diode are significantly below this value and should not be of concern in terms of mechanical failure of the diode during the assembly process.

From the results, it can be concluded that average von Mises stress on the diode increases from large heatsink model to small heatsink model by less than or equal to 3 MPa. This additional stress increment is due to percentage stress induced by thermal load increment.

V. EXPERIMENTAL RESULTS

In order to verify the numerical results, experimental measurements of junction temperature were performed. The traditional dc power cycling setup [25] shown in Fig. 14(a) has been used for the evaluation of the performance of the press-pack diode as device under test (DUT), with a photograph of the test setup configuration using the large heatsink assembly as DUT shown in Fig. 14(b). In this experimental



Fig. 14. (a) Electrical schematic of the test circuit. (b) Detail of the test circuit, where the auxiliary switch and the DUT can be identified.



Fig. 15. Experimental results of diode temperature (°C) versus time (s) for small heatsink, on ALG pad for 300-N clamping pressure.



Fig. 16. Experimental results of diode temperature (°C) versus time (s) for small heatsink, on Mo pad for 300-N clamping pressure.

configuration, a dc heating current is used for increasing the temperature of the device due to self-heating, and when this heating current is switched OFF, the forward voltage across the device at low current is used as a temperature-sensitive electrical parameter (TSEP) for the estimation of the junction temperature [26]. The calibration of the TSEP was done using a thermal chamber, measuring the forward voltage at low current at different temperatures and clamping forces, leaving enough time to reach the thermal equilibrium, hence assuming that the temperature in the chamber is the temperature of the chip.

The heating tests have been performed for various combinations, and the junction temperature increment from ambient temperature against time is plotted as in Figs. 15 and 16. The trend curves of power equation were fit to the discrete data sets. Assuming the junction temperature stabilizes after a certain amount of time, then we can extract the stabilized junction temperature of the structure for a constant loading current and clamping force. The time period for stabilized temperature was assumed to be 3600 s for obtaining the trend curve equation of junction temperature increment.



Fig. 17. Experimental results of diode temperature (°C) versus time (s) for large heatsink for both contact pad models for 500-N and 10-A loadings.



Fig. 18. Experimental results of diode temperature (°C) versus time (s) for large heatsink for model with Mo pad for 300- and 500-N clamping forces and 10- and 20-A loadings.

Comparing Figs. 15 and 16, it can be clearly observed how the temperature increase is smaller when ALG contacts are used. Fig. 17 presents the stabilized junction temperature increase for both contact materials, using a heating current of 10 A, a clamping force of 500 N, and the large heatsink model PS260. The impact of the clamping force on the junction temperature increase is presented in Fig. 18. Using Mo as intermediate contact, the effect of the clamping force (300 and 500 N) has been measured for two heating currents, namely 10 and 20 A. For the SiC device used in this paper, the forces of 300 and 500 N are based on the recommendations from Lutz *et al.* [3]. These recommndations state that clamping pressure should lie within the range 10–20 N/mm².

VI. COMPARISON OF FINITE-ELEMENT RESULTS TO EXPERIMENTAL RESULTS

Since the FEA modeling does not consist of the timedependent material properties in the modeling, the FEA modeling results were compared to stabilized temperature extracted from the experiments. The clamping force has less impact on the junction temperature rise than the contact material, as it can be observed in Figs. 19–21, where a combination of test assemblies (contact pad material, clamping force, and model of heatsink) has been evaluated to validate the model presented in this paper.

These results follow the trend shown in the simulations and suggest a better thermal performance of the ALG contact. The FEA results slightly under-predict the junction temperature in comparison to the experiments due to the approximated value of certain parameters in the FE modeling. Overall, the experiment and finite-element modeling follow the trends: 1) the reduction in junction temperature for increased clamping



Fig. 19. Junction temperature (°C) on diode versus clamping force (N) for large heatsink, finite element and experimental results for 10- and 20-A loadings on Mo contact pad.



Fig. 20. Junction temperature (°C) on diode versus clamping force (N) for large heatsink, finite element and experimental results for 10- and 20-A loadings on ALG contact pad.



Fig. 21. Junction temperature (°C) on diode versus clamping force (N) for small heatsink, finite element and experimental results for 10-and 20-A loadings on ALG contact pad.

pressure, and 2) ALG contact pad model generated lower junction temperature in comparison to Mo pad model.

The impact of the contact material and the clamping force on the thermal resistance was measured and characterized in [27] using advanced equipment. From the results presented, increasing the force reduces the thermal resistance and the press-pack assembly with ALG contacts has also a lower thermal resistance, corresponding with the modeling results obtained in this paper.

VII. CONCLUSION

A novel combined electrothermomechanical modeling methodology for assessing diode temperature and stress imposed on the diode in the press-pack packaging process is demonstrated. Based on the assumptions made in this paper, for load currents ranging from 20 to 25 A and clamping forces ranging from 300–500 N, the results show the following.

 Both contact pad materials Mo and ALG result in junction temperatures that meet manufacturers' specifications.

- Both contact pad materials result in stresses in the diode that are well below any stress that could cause mechanical failure in the diode.
- Using ALG results in a lower junction temperature compared to Mo (~6 °C-16 °C for process parameters investigated in this paper). Hence, using ALG could result in a significant increase in overall diode reliability.
- Adoption of a smaller heatsink design also meets manufacturers' specifications in terms of junction temperature. This can aid design engineers to meet smaller form factor requirements for the package.
- 5) Model results compare with experimental data both in terms of junction temperatures and temperature trends for both contact pad materials.

Based on the methodology detailed in this paper, a packaging design engineer can use any contact pad material whose thermal and mechanical properties are known. If the surface roughness of the interfaces is also known, these can easily be included into the analysis to provide values of thermal and electrical contact resistances. Hence, the developed methodology provides significant benefits to packaging engineers in identifying clamping forces and packaging materials that meet temperature, form factor, and reliability requirements for specific package designs and applications.

REFERENCES

- F. Wakeman, K. Billett, R. Irons, and M. Evans, "Electromechanical characteristics of bondless pressure contact IGBT," in *Proc. 14th Annu. Conf. Appl. Power Electron. Conf. Expo. (APEC)*, Dallas, TX, USA, Mar. 1999, pp. 312–317.
- [2] M. H. Rashid, *Power Electronics Handbook*, 3rd ed. Oxford, U.K.: Butterworth-Heinemann, 2011.
- [3] J. Lutz, H. Schlangenotto, U. Scheuermann, and R. D. Doncker, Semiconductor Power Devices: Physics, Characteristics, and Reliability. Berlin, Germany: Springer Verlag, 2011.
- [4] A. A. Hasmasan, C. Busca, R. Teodorescu, L. Helle, and F. Blaabjerg, "Electro-thermo-mechanical analysis of high-power press-pack insulated gate bipolar transistors under various mechanical clamping conditions," *Inst. Elect. Eng. Japan J. Ind. Appl.*, vol. 3, no. 3, pp. 192–197, 2014.
- [5] T. Poller, S. D'Arco, M. Hernes, A. R. Ardal, and J. Lutz, "Influence of the clamping pressure on the electrical, thermal and mechanical behaviour of press-pack IGBTs," *Microelectron. Rel.*, vol. 53, nos. 9–11, pp. 1755–1759, 2013.
- [6] T. Poller, T. Basler, M. Hernes, S. D'Arco, and J. Lutz, "Mechanical analysis of press-pack IGBTs," *Microelectron. Rel.*, vol. 52, pp. 2397–2402, Sep. 2012.
- [7] A. Hasamasan, C. Busca, R. Teodorescu, and L. Helle, "Modelling the clamping force distribution among chips in press-pack IGBTs using the finite element method," in *Proc. 3rd IEEE Int. Symp. Power Electron. Distrib. Generat. Syst. (PEDG)*, Aalborg, Denmark, Jun. 2012, pp. 788–793.
- [8] A. Pirondi, G. Nicoletto, P. Cova, M. Pasqualetti, and M. Portesine, "Thermo-mechanical finite element analysis in press-packed IGBT design," *Microelectron. Rel.*, vol. 40, pp. 1163–1172, Jul. 2000.
- [9] A. Pirondi, G. Nicoletto, P. Cova, M. Pasqualetti, M. Portesine, and P. E. Zani, "Thermo-mechanical simulation of a multichip press-packed IGBT," *Solid State Electron.*, vol. 42, no. 12, pp. 2303–2307, 1998.
- [10] T. Poller, J. Lutz, S. D'Arco, and M. Hernes, "Determination of thermal and electrical contact resistance in press-pack IGBTs," in *Proc. 15th Eur. Conf. Power Electron. Appl.*, Lille, France, Sep. 2013, pp. 1–9.
- [11] C. Busca, R. Teodorescu, F. Blaabjerg, L. Helle, and T. Abeyasekera, "Dynamic thermal modelling and analysis of press-pack IGBTs both at component-level and chip-level," in *Proc. 39th IEEE Conf. Ind. Electron. Soc. (IECON)*, Vienna, Austria, Nov. 2013, pp. 677–682.
- [12] Hoffmann & Co Elektrokohle AG. *Aluminum Graphite Composites*. [Online]. Available: http://www.hoffmann.at

- [13] Release 12.0, Help System, Coupled Field Analysis Guide, ANSYS, Inc, Canonsburg, PA, USA, 2009.
- [14] M. M. Yovanovich, "Four decades of research on thermal contact, gap, and joint resistance in microelectronics," *IEEE Trans. Compon. Packag. Technol.*, vol. 28, no. 2, pp. 182–206, Jun. 2005.
- [15] V. W. Antonetti, T. D. Whittle, and R. E. Simons, "An approximate thermal contact conductance correlation," *Exp./Numer. Heat Transf. Combustion Phase Change*, vol. HTD-170, no. 1, pp. 35–42, 1991.
- [16] S. Ganesan and M. G. Pecht, *Lead-Free Electronics*. Hoboken, NJ, USA: Wiley, 2006.
- [17] P. G. Slade, *Electrical Contacts, Principles and Applications*. 2nd ed. Boca Raton, FL, USA: CRC Press, 2014.
- [18] M. Ciavarella, G. Murolo, and G. Demelio, "The electrical/thermal conductance of rough surfaces—The Weierstrass–Archard multiscale model," *Int. J. Solids Struct.*, vol. 41, no. 15, pp. 4107–4120, Jul. 2004.
- [19] P. Sharma, S. Sharma, and D. Khanduja, "A study on microstructure of aluminium matrix composites," *J. Asian Ceram. Soc.*, vol. 3, no. 3, pp. 240–244, Sep. 2015.
- [20] M. Winter. (2010). Web elements. [Online]. Available: http://www. webelements.com/molybdenum/physics.html
- [21] J. Walker, Handbook of RF and Microwave Power Amplifiers. Cambridge, U.K.: Cambridge Univ. Press, 2012.
- [22] GD Rectifiers Ltd, accessed on 2016. [Online]. Available: http://www.gdrectifiers.co.uk/
- [23] T. Kimoto and J. A. Cooper, Fundamentals of Silicon Carbide Technology: Growth, Characterization, Devices, and Applications. Hoboken, NJ, USA: Wiley, 2014.
- [24] W. N. Sharp, G. M. Beheim, L. J. Evans, N. N. Nemeth, and O. M. Jadaan, "Fracture strength of single crystal silicon carbide microspecimens at 24 °C and 1000 °C," *J. Microelectromech. Syst.*, vol. 17, no. 1, pp. 244–254, Feb. 2008.
- [25] L. R. GopiReddy, L. M. Tolbert, and B. Ozpineci, "Power cycle testing of power switches: A literature survey," *IEEE Trans. Power Electron.*, vol. 30, no. 5, pp. 2465–2473, May 2015.
- [26] Y. Avenas, L. Dupont, and Z. Khatir, "Temperature measurement of power semiconductor devices by thermos-sensitive electrical parameters—A review," *IEEE Trans. Power Electron.*, vol. 27, no. 6, pp. 3081–3092, Jun. 2012.
- [27] J. O. Gonzalez, A. M. Aliyu, P. Mawby, O. Alatise, L. Ran, and A. Castellazzi, "Development and characterisation of pressed packaging solutions for high-temperature high-reliability SiC power modules," *Microelectron. Rel.*, vol. 64, pp. 434–439, Sep. 2016.

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