A 10-Bit 4th-Order Quadrature Bandpass Continuous-Time ΣΔ Modulator with 33-MHz Bandwidth for a Dual-Channel GNSS Receiver

Junfeng Zhang, Yang Xu, Zehong Zhang, Yichuang Sun, *Senior Member*, *IEEE*, Zhihua Wang, *Fellow*, *IEEE*, *and* Baoyong Chi, *Member*, *IEEE*

***Abstract*—A 4th-order quadrature bandpass (QBP) continuous-time (CT) sigma-delta (ΣΔ) modulator for a dual-channel global navigation satellite system (GNSS) receiver is presented. With a bandwidth of 33 MHz, the modulator is able to digitalize the down-converted GNSS signals in two adjacent signal bands simultaneously, realizing dual-channel GNSS reception with one receiver channel instead of two independent receiver channels. To maintain the loop-stability of the high-order architecture, any extra loop phase shifting should be minimized. In the system architecture, a feedback and feedforward hybrid architecture is used to implement the 4th-order loop-filter, and a return-to-zero (RZ) feedback after the discrete-time differential operation is introduced into the input of the final integrator to realize the excess loop delay (ELD) compensation, saving a spare summing amplifier. In the circuit implementation, power-efficient amplifiers with high-frequency active feedforward and anti-pole-splitting techniques are employed in the active RC integrators, and self-calibrated comparators are used to implement the low-power 3-bit quantizers. These power saving techniques help achieve superior figure of merit (FoM) for the presented modulator. With a sampling rate of 460 MHz, current-steering digital-analog converters (DACs) are chosen to guarantee high conversion speed. Implemented in only 180 nm CMOS, the modulator achieves 62.1 dB peak Signal to Noise and Distortion Ratio (SNDR), 64 dB dynamic range (DR) and 59.3 dB image rejection ratio (IRR), with a bandwidth of 33 MHz, and consumes 54.4 mW from a 1.8 V power supply.**

***Index Terms*—quadrature bandpass, continuous-time, wide-band, sigma-delta modulator, RZ ELD compensation, power-efficient amplifier.**

I. Introduction

With the rapidly increasing demand of navigation service in mobile electronics in recent years, global navigation satellite systems (GNSS), including Global Positioning System (GPS), Global Navigation Satellite System (GLONASS), Galileo and Compass (Beidou2), are being developed in many countries. The accuracy, speed and reliability of the positioning service would be improved with more available satellites. If the analog-digital converter (ADC) in the GNSS receiver could provide wide enough bandwidth and high enough dynamic range, a simplified architecture as shown in Fig. 1 would be feasible for the dual-channel receiver. Unlike the dual-channel receivers presented in [1] and [2], which are implemented with two independent receiver channels, it could receive dual-channel signals simultaneously with one receiver channel. What's more, with the inherent anti-aliasing filtering characteristics of the sigma-delta (ΣΔ) modulator used as ADC, the pressure on the IF analog filter could be relaxed.

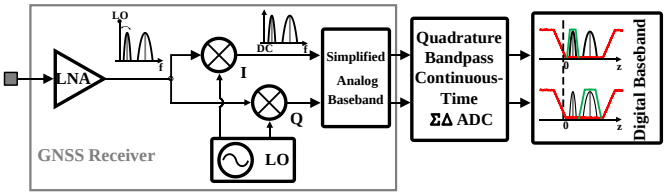


Fig. 1. Simplified block diagram of the dual-channel GNSS receiver.

TABLE I
DUAL-CHANNEL MODES SUPPORTED BY THE RECEIVER

	Mode	Operating Frequency (MHz)	BW (MHz)	Overall BW (MHz)
1	GPS L1(Galileo E1)	1575.42	2.2	32.68
	GLONASS L1	1602	10	
2	GPS L1(Galileo E1)	1575.42	2.2	17.52
	Compass B1	1561.1	4.2	
3	GPS L1(Galileo E1)	1575.42	18	25.42
	Compass B1	1561.1	4.2	
4	GPS L2	1227.6	18	31.4
	GLONASS L2	1246	8	
5	GPS L2	1227.6	18	31.56
	Compass B2 (Galileo E5b)	1207.14	4.2	

TABLE I lists the frequency plan of the dual-channel receiver. Five different dual-channel modes are supported. The modulator bandwidth must cover two signal bands and the frequency gap between them, resulting in a 33 MHz bandwidth (BW) requirement.

As the modulator is implemented in 180 nm CMOS, its sampling rate (F_S) is limited due to the relatively severe

This work was supported in part by the National Natural Science Foundation of China under grants 61331003.

J. Zhang, Z. Zhang, Y. Xu, Z. Wang and B. Chi are with the Institute of Microelectronics, Tsinghua University, Beijing, 100084, China (chibylxc@tsinghua.edu.cn).

Y. Sun is with School of Engineering and Technology, University of Hertfordshire, Hatfield, Herts AL10 9AB, United Kingdom.

parasitics. A 4th-order architecture with multi-bit quantizers is chosen to realize the wide-band high-dynamic-range modulator. To maintain the loop-stability of the high-order architecture, any extra loop phase shifting should be minimized. In the system architecture, a feedback and feedforward hybrid architecture is used to implement the 4th-order loop-filter, and a return-to-zero (RZ) feedback after the discrete-time differential operation is introduced into the input of the final integrator to realize the excess loop delay (ELD) compensation, saving a spare summing amplifier and reducing the power consumption as well as the loop phase shifting.

In the circuit implementation, embedded amplifiers with high gain-bandwidth product (GBW) are needed. As the amplifiers in [3] and [4] could achieve high GBW with low power consumption, their output swings are low due to the feedforward structure at the output. In this paper, a new high-frequency feedforward structure is proposed, which allows large output swing while maintaining good phase margin.

The offset calibration of the comparators in [3] and [5] introduces large parasitic capacitance at the outputs of the preamplifiers and badly lowers down their bandwidth. This work comes up with a new calibration method, which is suitable for high-speed comparators and does not influence the bandwidth of the preamplifier, guaranteeing low phase shifting.

Moreover, an optimized reset-set (RS) latch is presented, which has shorter response time than the conventional RS latch (in [3] and [4]) in extreme conditions to realize a higher sampling rate.

This paper is expanded from a RFIC 2015 conference paper with more details about the system-level and circuit-level design consideration and more measurement results.

The paper is organized as follows. Section II describes the system architecture of the modulator. The circuit-level implementation is discussed thoroughly in Section III, and the measurement results are unveiled in section IV. Finally, Section V concludes the paper.

II. System Architecture

The peak signal-noise ratio (SNR) of a ΣΔ modulator is determined by its over-sampling ratio (OSR), loop-filter order (L) and number of quantizer bits (N) with the following equation:

$$SNR_{peak} = \frac{3(2L+1)}{2\pi^{2L}}(2^N-1)^2 OSR^{2L+1} \quad (1)$$

.

As the modulator is implemented in 180 nm CMOS, its sampling rate is limited due to the relatively severe parasitics. Thus the OSR couldn't be high. In order to get a well-shaped noise transfer function (NTF) with a low OSR, high-order loop-filter and multi-bit quantizers are needed. With a 4th-order architecture, the presented modulator operates at an OSR of 14, resulting in an F_S of 460 MHz. Besides, two 3 bit FLASH ADCs are employed as the quantizers after the trade-off among stability, clock jitter tolerance and linearity.

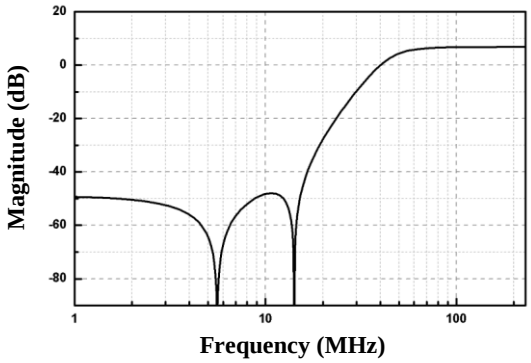


Fig. 2. The low-pass modulator NTF in z-domain.

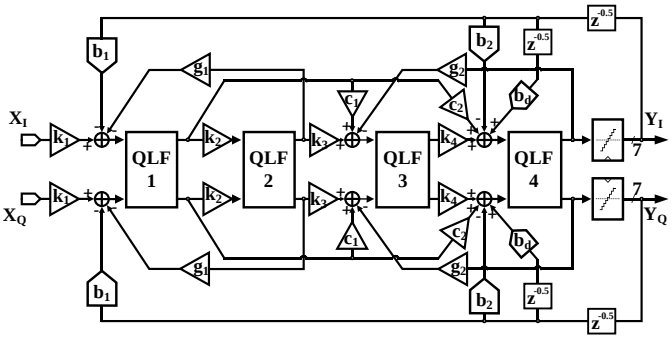


Fig. 3. Block diagram of the proposed modulator.

A. NTF Selection

The NTF of the corresponding low-pass modulator is first generated in the discrete-time domain (z-domain) with the MATLAB toolbox "synthesizeNTF". And the chosen z-domain NTF is plotted in Fig. 2. As the modulator contains a 4th-order loop-filter, the out-of-band gain of the NTF is set to be 2.2, which is 6.8 dB, to maintain its stability. Two zeros exist at low frequency, which are contributed by g_1 and g_2 in Fig. 3, and make the in-band NTF relatively flat. After the NTF is transformed into s-domain, the out-of-band gain of the s-domain NTF is 1 (0 dB). The low-pass modulator is further transformed into the quadrature band-pass architecture, with the center frequency of the NTF shifted from dc to f_c.

B. Modulator Architecture

Feedback and feedforward are two main loop filter structures. The full-feedback structure needs four feedback digital-analog converters (DACs) while the full-feedforward structure needs only one. Once the modulator gets saturated in case of a strong blocker, the feedback structure couldn't recover while the feedforward structure could when the blocker disappears. However, the full-feedback structure shows a 4th-order anti-aliasing filtering characteristics while the full-feedforward structure only shows a 1st-order anti-aliasing filtering characteristics. Furthermore, the signal transfer function (STF) of a full-feedforward structure has a peak at the band-edge, which may amplify the blocker located at the band-edge and saturate the quantizers. So a feedback and feedforward hybrid architecture as depicted in Fig. 3 is

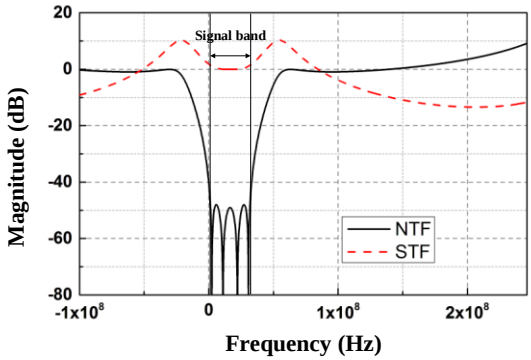


Fig. 4. The NTF and STF magnitude responses of the modulator.

adopted. The complex loop-filter consists of four 1st-order quadrature loop-filters (QLF), whose poles are located at the center frequency f_c. Unlike the full-feedback structure in which there is one feedback at the input of every QLF, local feedforward paths c_1 and c_2 are introduced from the output of the QLF1 to the inputs of the QLF3 and QLF4 in this hybrid architecture, resulting in the absence of two 3-bit feedback DACs at the inputs of the QLF2 and QLF3. Local feedbacks g_1 and g_2 form two complex 2nd-order resonators together with the four QLFs. They split the poles of the QLFs apart, so that they are distributed uniformly in the signal band. This architecture maximizes the in-band noise shaping. Simplify the QLFs into low-pass integrators, the NTF and STF of the modulator are

$$NTF = \frac{(s^2 + g_2k_4)(s^2 + g_1k_2)}{s^4 + b_2s^3 + b_1c_2s^2 + b_1c_1k_4s + b_1k_2k_3k_4} \quad . \tag{2}$$

$$STF = \frac{k_1c_2s^2 + k_1c_1k_4s + k_1k_2k_3k_4}{s^4 + b_2s^3 + b_1c_2s^2 + b_1c_1k_4s + b_1k_2k_3k_4} \quad . \tag{3}$$

This architecture shows a 2nd-order STF and the peak at the band-edge is about 10 dB, which is much lower than the 20 dB peak in the full-feedback structure. The coefficients $k_{1,2,3,4}$ and $c_{1,2}$ are determined by the NTF chosen before, and to make the STF gain at dc equal to 1, b_1 must be equal to k_1.

The NTF and STF magnitude responses of the modulator is shown in Fig. 4.

C. *Excess Loop Delay (ELD) Compensation*

The delay between the clock edge and the quantizer output greatly depends on the input signal. In order to guarantee the settling time of the quantizer outputs before being sampled, the ELD is always inserted between the quantizer clock and the DAC clock. We set the delay as half a sampling period, which is also easy to realize [5]. We choose non-return-to-zero–pulse (NRZ) feedback DACs due to their better clock jitter tolerance, so ELD compensation is needed to guarantee stability [5]. The most commonly used approach to realize the ELD compensation is to insert a direct feedback at the input of the quantizer (as shown in Fig. 5 (a)), in which an extra adder

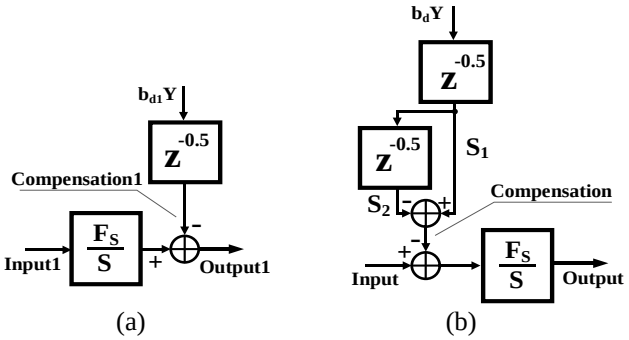


Fig. 5. (a) Block diagram of the direct feedback ELD compensation; (b) Block diagram of the differentiated RZ feedback ELD compensation.

before the quantizer is needed. The adder not only increases the power consumption and die area, but also deteriorates the phase margin due to its additional phase shifting. Suppose that two pole amplifiers with their second poles at their GBWs are adopted in the integrators and the adder, and the GBWs of the amplifiers in the integrators are 1.5 Fs and the GBW of the adder amplifier is 2 Fs, the phase margin of the modulator should be 55° without the adder and 40° with the adder, respectively. To guarantee the phase margin to be above 50° without modifying the amplifiers, the Fs must be lowered down by 40% (shown in Fig. 6). Thus we adopt the differentiated return-to-zero-pulse (RZ) feedback shown in Fig.5 (b) at the input of the final integrator to realize the ELD compensation. According to [5], the loop responses of the two different structures are similar. Thus we can get the value of b_d from the equation (4):

$$\begin{aligned} Compensation1(s) &= b_{d1} \cdot Y(s) z^{-0.5} \\ &= \frac{b_{d1}}{b_d} \cdot s \cdot S_1(s) \cdot \frac{1}{s} \\ &= \frac{b_{d1}}{b_d} \cdot \mathscr{L}\left[dS_1(t)/dt\right] \cdot \frac{1}{s} \\ &\approx \frac{b_{d1}}{b_d} \cdot \mathscr{L}\left\{\left[S_1(t) - S_1(t - 0.5T_S)\right] / \left(0.5T_S\right)\right\} \cdot \frac{1}{s} \\ &= \frac{2b_{d1}}{b_d} \cdot Compensation(s) \cdot \frac{F_S}{s} \quad . \end{aligned} \tag{4}$$

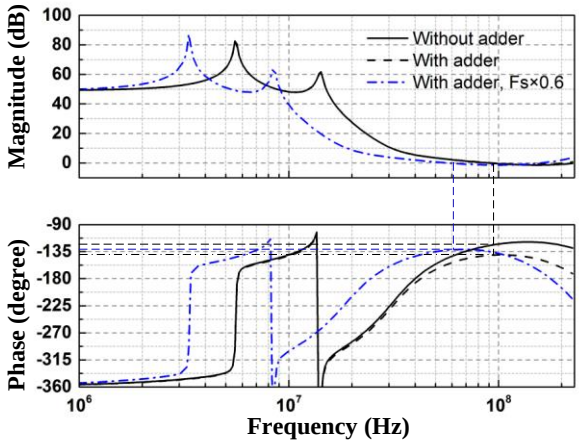


Fig. 6. Plots of the loop-transfer-functions with and without the adder.

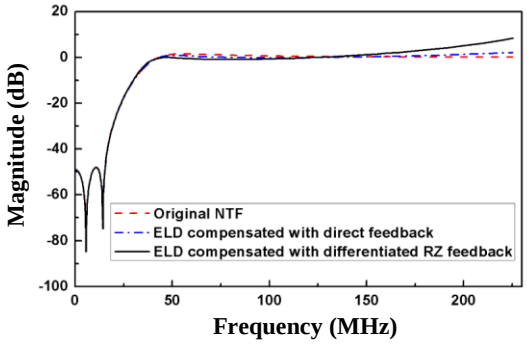


Fig. 7. Plots of the original NTF and its variants after the direct feedback ELD compensation and differentiated RZ feedback ELD compensation.

So we can see that $b_d = 2\,b_{d1}$. In Fig. 3, the half-clock-delay path is merged into the feedback path b_2.

Fig. 7 shows the comparison among the original s-domain high-pass NTF and the NTFs with two ELD compensation approaches. The NTF in the signal band is unchanged, while different tilt degrees happen at high-frequency band, and the adopted RZ feedback ELD compensation approach shows stronger deterioration at high frequency band. So with the proposed ELD compensation approach, the in-band noise suppression is not affected while the dynamic range may be slightly reduced as the high-frequency tilt would raise the out-of-band noise power a little.

III. Circuit Implementation

Fig. 8 illustrates the circuit-level diagram of the presented modulator including the ELD compensation. Active RC integrators are chosen to implement the quadrature loop-filters. The cross-coupling resistors R_{IF} shift the integral poles from dc to the center frequency f_c, which is determined by the RC time constant of R_{IF} and the integral capacitors C_{int}. NRZ DACs are adopted to realize the feedback paths. Thanks to the virtual ground provided by the active RC integrators, the feedforward paths c_1 and c_2 are able to be realized with the resistors R_{c1} and R_{c2}, which introduces little nonlinearity or extra phase-shift. The local feedbacks g_1 and g_2 in Fig. 3 are pretty weak. If they are realized with feedback resistors, the resistances could be high, which suffers from large area occupation and parasitic capacitance. This issue is solved by replacing a small coefficient with the difference between two large coefficients. So g_1 is realized with two resistors R_{g1n} and R_{g1p} which are of opposite phases, and g_2 is implemented in the same way. To simplify the RC time-constant trimming, the capacitors in the four integrators are all set to 988 fF, and the values of the resistors are listed in TABLE II. Two 3-bit FLASH ADCs are employed as the quantizers in the I and Q paths, and their offsets are automatically calibrated during the start-up.

TABLE II
VALUES OF THE RESISTORS IN THE LOOP-FILTERS

Component	R_1	R_2	R_3	R_4	R_{c1}	R_{c2}
Value(kΩ)	2.2	8.8	13.2	0.88	11	1.83
Component	R_{g1p}	R_{g1n}	R_{g2p}	R_{g2n}	R_{IF}	
Value(kΩ)	11	14.67	8.8	9.35	9.35	

A. Active RC Integrator

In order to get high peak signal to noise and distortion ratio (SNDR) and achieve good precision, good linearity in the signal band must be guaranteed. So Gm-C integrators are not suitable here, although they are much more power-efficiency than active RC integrators and more suitable for high-speed operation. On the contrary, active RC integrators are utilized due to their good linearity and high output swing. Besides, the virtual grounds provided by them would strongly relax the requirement on the output resistance of the feedback DACs.

1) RC-Constant Variations

The RC time-constant of the active RC integrator varies with process, voltage and temperature (PVT) variations while the F_s stays the same. The influence of RC-constant variations on the NTF, STF and stability is shown in Fig. 9. When the RC-constant increases, the bandwidth of the NTF and STF is dropped, the peak of the STF is reduced, and the phase margin of the feedback loop is improved. When the RC-constant decreases, everything changes in the opposite direction. To get a correct bandwidth and maintain the stability, the RC time-constant is calibrated by reconfiguring the 5-bit binary-weighted capacitor arrays.

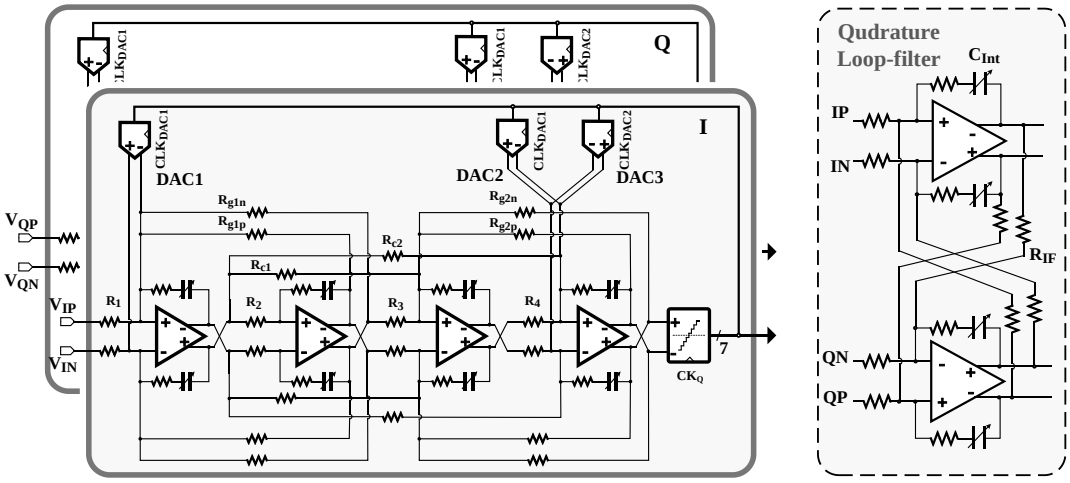


Fig. 8. Left: Circuit-level diagram of the presented modulator. Right: Schematic of the QLF.

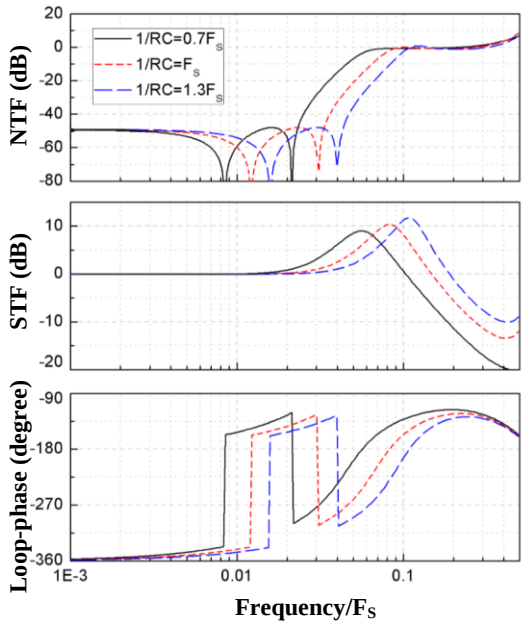


Fig. 9. NTF, STF and the loop-phase shift with different RC time-constants.

2) Finite GBW Compensation

To overcome the quantization delay that may lead to instability of the whole modulator, we introduce the excess loop delay and compensate it in the z-domain. But the additional phase shifting of the loop-filter is not compensated, and it may also reduce the stability margin of the modulator. For this reason, the RZ ELD compensation is used to avoid the spear adder as well as its phase shift. However, the finite GBW of the amplifiers used in the integrators would still impact the stability of the modulator. If we suppose the amplifier in the active RC integrator shown in Fig. 10 (a) is a one-pole system and has infinite gain and finite GBW. The transfer function of the integrator is expressed as the equation (5):

$$In(s) = \frac{F_S}{s(1+\frac{s}{GBW_r})}. \tag{5}$$

in which

$$F_S = \frac{1}{RC}$$
$$GBW_r = 2\pi \cdot GBW. \tag{6}$$

The ideal transfer function of an integrator has only the pole at dc, and the second pole at GBWr is introduced by the finite GBW of the amplifier. This extra pole would introduce considerable phase shifting at the frequency higher than 0.1 GBW, which would greatly harm the stability of the modulator. To reduce the phase shifting caused by the finite GBW, a compensation technique is employed here, in which a resistor R_C is added to the integrator in series with C, as shown in Fig. 10 (b). Still supposing the amplifier is a one-pole system and has infinite gain and finite GBW, the transfer function

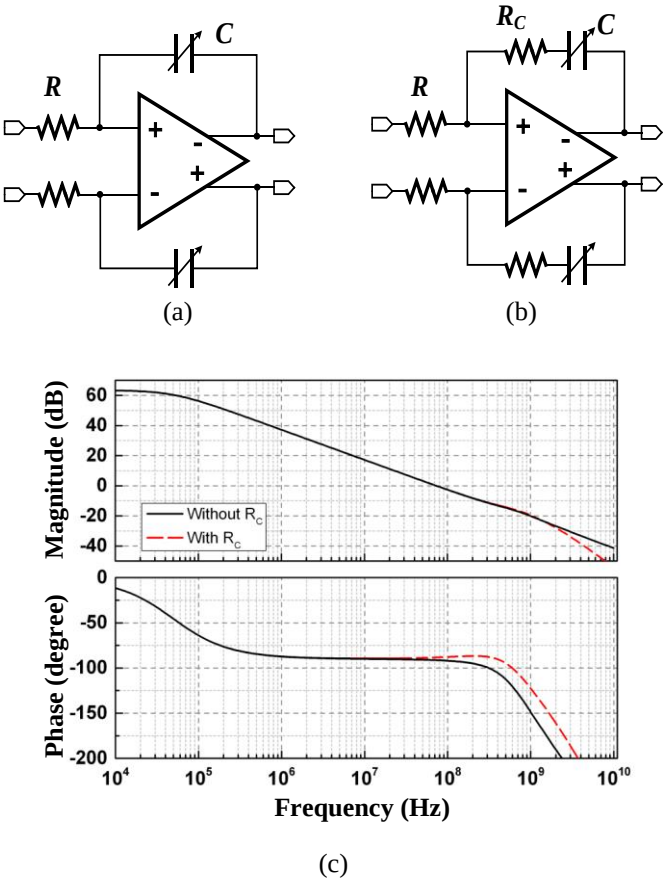


Fig. 10. (a) Schematic of the active RC integrator; (b) Schematic of the active RC integrator with finite GBW compensation; (c) Bodes of the integrator with and without finite GBW compensation.

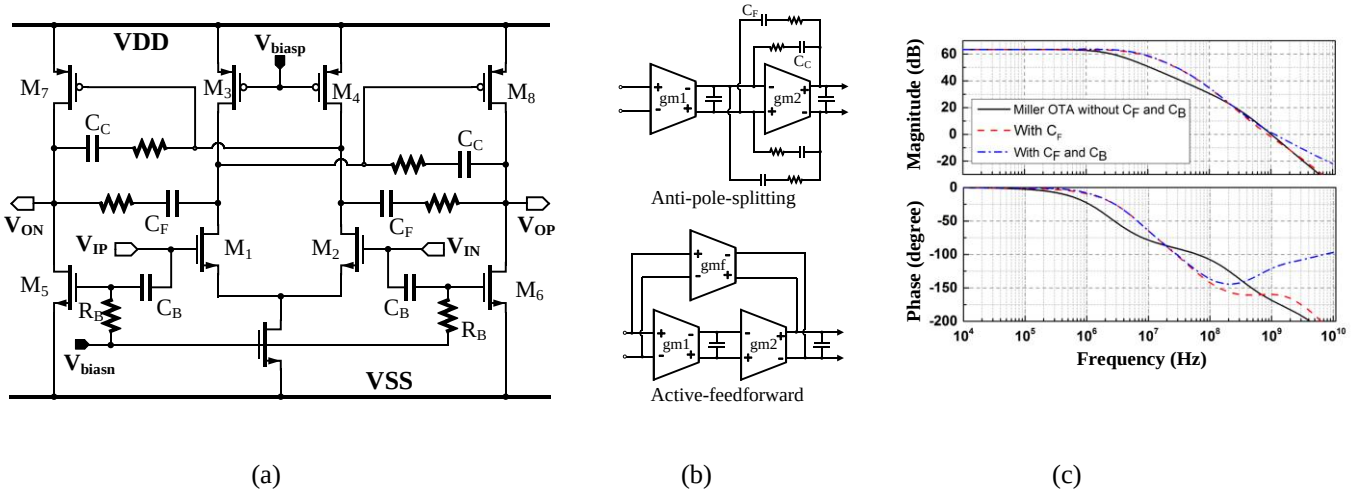
of the integrator would be expressed as the equation (7):

$$In'(s) = \frac{(1+sR_CC)}{sRC(1+\frac{s}{GBW_r})}. \tag{7}$$

So R_C introduces a zero into the transfer function. The integrator would have only the pole at dc and become an ideal integrator if we set

$$\frac{1}{R_CC} = GBW_r = 2\pi \cdot GBW. \tag{8}$$

A real amplifier would have more than one pole and have finite gain as well as finite bandwidth. But the additional phase shift caused by the finite GBW could still be reduced. The magnitudes and phases of a real active RC integrator with and without R_C are plotted in Fig. 10 (c). The high-frequency magnitude is slightly lifted by the zero introduced by R_C, but the phase shift at the middle-frequency zone is clearly compensated. The effect works well even under the process variation of the R_CC constant due to the wide-band phase-lifting feature of the zeros. This technique makes it possible to avoid the high GBW, power-hungry amplifiers while maintaining the phase margin of the modulator.



(a) (b) (c)

Fig. 11. (a) Schematic of the power-efficient amplifier; (b) Equivalent block diagram of the two techniques used in the amplifier; (c) Bodes of the proposed amplifier and the original two-stage Miller-compensated amplifier.

3) Power-Efficient Amplifier

The requirements of the amplifiers used in the integrators are listed in TABLE III, where the noise and non-linearity are not taken into account due to the modelling difficulty. The voltage gain of the four amplifiers need to be higher than 40 dB, which is easy to realize. And the slew rate of the 1st to 3rd amplifiers should be higher than 500 V/μs, while the slew rate of the 4th amplifier should be higher than 1500 V/μs. Since the requirements are simulated with the tool Simulink, the amplifiers are all regarded as one-pole systems. So the actual requirements of the GBW is higher than those in TABLE III. It could be seen that the last amplifier should have a GBW much higher than 1.5 GHz. Thus the 4th amplifier should have a GBW of higher than 1.5 GHz and a slew rate of higher than 1500 V/μs. The most commonly used two-stage Miller-compensated OTAs provide enough dc gain and show good stability, but they would be power-hungry to achieve wide bandwidth since the principle of Miller-compensation is to increase the load of the amplifier and reduce its bandwidth to guarantee the stability. Therefore, a two-stage amplifier with high-frequency active feedforward and anti-pole-splitting techniques is proposed here, as shown in Fig. 11 (a), to achieve high bandwidth with reduced power consumption. The transistors $M_{1\sim4}$ form the first stage and without C_F, C_B and R_B, $M_{5\sim8}$ would be the second stage of a Miller-compensated OTA, in which C_C is a Miller compensation capacitor. C_F can be regarded as a negative Miller capacitor. It introduces negative capacitance between the input and the output of the second stage, which counteracts the effect of the Miller compensation capacitor and pushes the two poles closer to each other. This "anti-pole-splitting" effect greatly expands the bandwidth of the amplifier without increasing its power consumption [3] [4] [6].

TABLE III
REQUIREMENTS OF THE AMPLIFIERS IN THE INTEGRATORS

	AMP1	AMP2	AMP3	AMP4
Gain (dB)	⩾40	⩾40	⩾40	⩾40
GBW(GHz)	⩾0.5	⩾0.5	⩾0.5	⩾1.5
Slew Rate(V/μs)	⩾500	⩾500	⩾500	⩾1500

In [3]-[5] and [7], an active feedforward path realized with a differential pair is used to guarantee the phase margin. The differential pair is connected to the output while its gates are connected to the input. So the output swing could be no higher than twice the threshold voltage of the differential pair transistors. Large output swing could reduce the effect of circuit noise on the output SNR as well as relaxing the requirement of the offsets of the comparators. As the phase margin is meaningful only at high-frequency, here we propose a high-frequency active feedforward structure. With R_B providing the dc bias-voltage, $M_{5,6}$ act as current mirrors at dc. And C_B introduces a direct feedforward from the input to the output. The concept of this technique is shown in Fig. 11 (b). Since the gain and phase of the first-order path drops much slower than those of the second-order path at high-frequency, the feedforward helps significantly achieve a higher unit-gain bandwidth with good phase margin. Meanwhile, its output swing is the same as the two-stage Miller-compensated OTA. It can be seen in Fig.11 (c) that the proposed amplifier with high-frequency active feedforward and anti-pole-splitting techniques achieves much wider bandwidth than the two-stage Miller-compensated OTA with the same power consumption and shows similar phase margin.

B. Self-Calibrated Comparator

Three-stage dynamic comparators are employed in the quantizers to realize high conversion speed. Each comparator is composed of a preamplifier stage, a regeneration latch stage and a RS latch stage. The preamplifier could isolate the kick-back noise and amplify the difference between the input signal and the reference voltage. If its voltage gain is higher than 1, it could reduce the offset of the comparator caused by the process mismatch. Since the higher gain would provide the better offset suppression, the gain of the preamplifier is usually designed to be high. In the presented 4th-order modulator, the loop stability requirement is difficult to meet, and the phase shift of the preamplifier is not compensated. So the bandwidth of the preamplifier must be high enough to avoid affecting the stability. For the presented modulator application, the simulated -3 dB bandwidth should be higher than 2 GHz. The

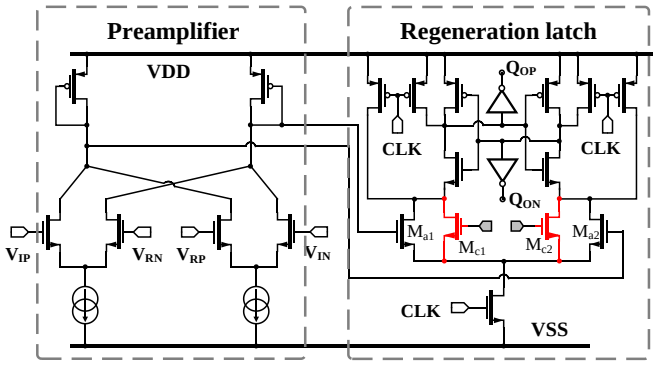


Fig. 12. Schematic of the preamplifier and the regeneration latch.

power consumption would be unacceptably high to achieve that high bandwidth as well as high gain. So a preamplifier with ultra-wide bandwidth and a voltage gain of about 0 dB (see Fig. 12) is adopted. While the offset is not suppressed by the first stage, it is calibrated in the regeneration latch stage. With this strategy, the two quantizers consume less than 15% of the total modulator power consumption, while many other wide-band works spend much more power by the quantizers. The schematic of the regeneration latch is shown in Fig. 12. The two input transistors $M_{a1,2}$ amplifies the output of the preamplifier at the rising edge of the clock, and two cross-coupled inverters amplify the differential drain voltage of $M_{a1,2}$ into the full-swing digital signal. In [3] and [5], offset of the comparator is calibrated with a current-steering DAC which is connected to the output of the preamplifier. This DAC introduces pretty large parasitic capacitance at the output of the preamplifier and reduces its bandwidth badly. Here we come up with a new method of calibration, which is suitable for high-speed comparators and does not influence the bandwidth of the preamplifier. Calibrating transistors $M_{c1,2}$ paralleled with the input transistors $M_{a1, 2}$ play a role of active resistors. With their gate voltages digitally controlled, they introduce an extra offset opposite to the offset caused by the device mismatch and result in a much lower offset. The calibration circuit is shown in Fig. 13 (the comparators are illustrated as single-ended while they are actually differential). The calibration control voltages are generated by a resistor ladder and connected to the gates of the calibration transistors $M_{c1,2}$ of each comparator through two switch arrays which are controlled by a 4-bit counter. At the start-up of the modulator, all the comparators are calibrated at the same time to speed up the calibration procedure. After the reset pulse, all the inputs of the comparators are connected to the common-mode reference voltage and the 4-bit counters start counting. The counters keeps counting up, controlling the differential gate control voltages switched from 1.8 V to -1.8 V step by step, until the outputs of the comparators flip. The calibration achieves the final offsets lower than 10mV while the least significant bit (LSB) is 125 mV.

The RS latch is commonly composed of two cross-coupled NOR gates (see Fig. 14 (a)). Since the outputs of the NOR gates are determined by each other, the response time of the RS latch could be long. When the input voltage is low, the response time of the whole comparator could be much long. As in Fig.14 (c), the simulated response time is 672 ps when the input voltage is 0.1 mV. We notice that the digital output of the regeneration latch Q_{OP} and Q_{ON} could be “00”, “01” and “10”, but could not be “11”. When the outputs of the RS latch flip, the inputs are always “01” or “10”. So four extra transistors $M_{i1\sim4}$ are inserted into the two cross-coupled NOR gates, as shown in Fig. 14 (b). And with these extra transistors, the output would be determined directly by the inputs when they are “01” or “10”, and the response time of the RS latch is reduced to 562 ps. Supposing that there is no delay in the following circuits, the highest F_s that could be achieved is improved from 744 MHz to 890 MHz.

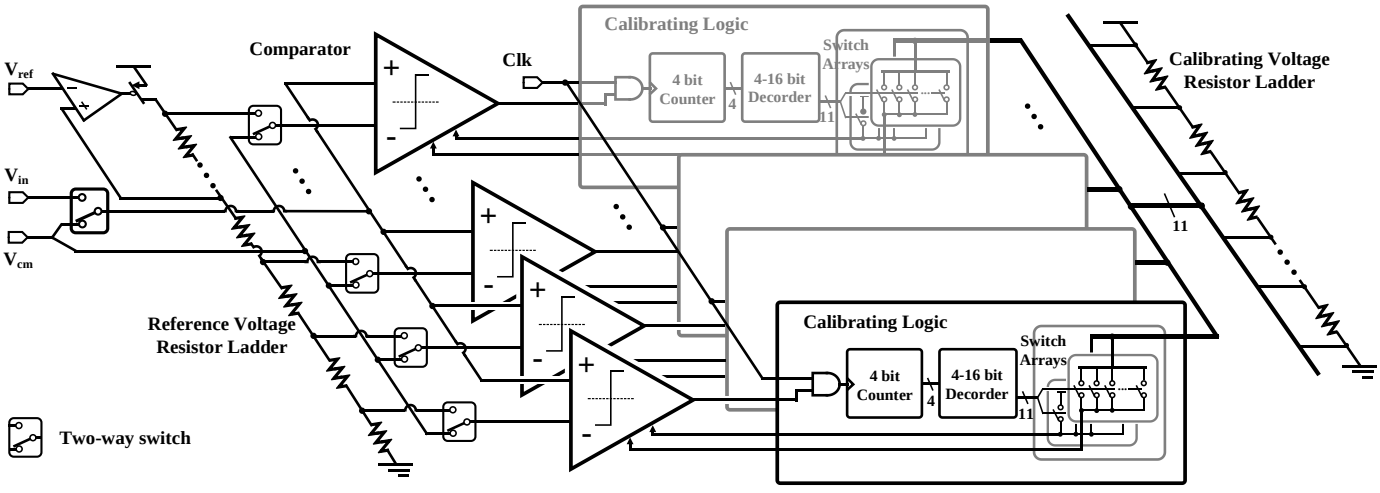


Fig. 13. 3-bit FLASH ADC with offset-calibration logic.

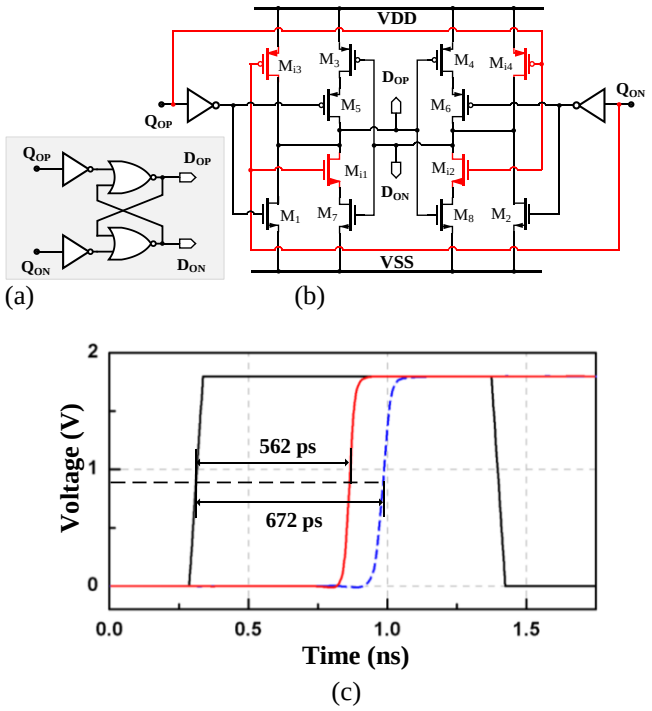


Fig. 14. (a) Conventional RS latch; (b) Optimized RS latch; (c) Response of the comparators with the two kinds of RS latches. (Black: Clock; Blue Dash: With conventional RS latch; Red: With optimized RS latch).

C. Current-Steering DAC

The feedback DACs are driven by 7-bit thermometer codes. Current-steering DAC units are employed due to their high conversion speed. The schematic of the adopted DAC unit of the DAC1 is shown in Fig. 15 (a). The current sources in the DAC unit are all cascoded to realize high output impedance and isolate the parasitic drain capacitance while the current source transistors are large size in order to get good linearity. The currents of the pmos side and the nmos side are 65 μA and 32.5 μA, respectively. As shown in Fig. 15 (b) and (c), when DP is 1 or 0, DN is in the opposite state. So the currents flowing into or out from OutP and OutN are always 32.5 μA. The first DAC (DAC1) is connected directly to the input of the loop-filter, so its noise and harmonics are directly injected into the input together with the input signal, while the noise and nonlinearity of the DAC2 and DAC3 are suppressed by the three integrators in front of them. The supply net always carries much more noise than the ground net. As we can see in Fig. 15 (b) and (c), the noise voltage on the power supply is turned into noise current and injected into the integrator. Since this noise current only exists on one input of the integrator, it would appear in the differential output of the integrator. To suppress the noise from the power supply, the source degeneration resistors R_S are adopted in the DAC1. It weakens the equivalent trans-conductor of the pmos current source transistors and reduces the noise current. Furthermore, it suppresses the thermal noise of the pmos current source transistors as well. On the contrary, the noise voltage from the ground results in a common mode noise which does not affect the output differential signal. Thus there is no source degeneration resistor at the NMOS side. The degeneration resistance is 12 kΩ and the dc current of the DAC1 unit is

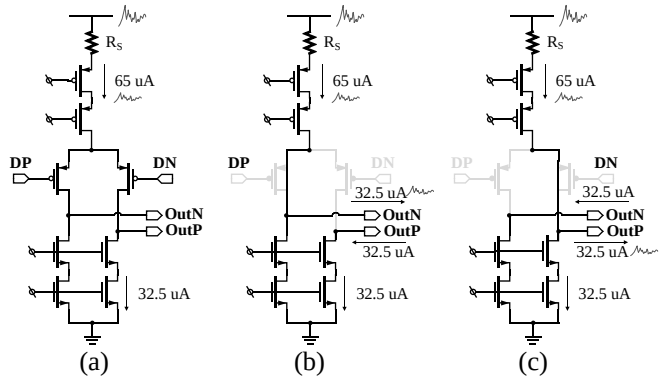


Fig. 15. (a) Schematic of the current-steering DAC unit in the DAC1; (b) Current direction when DP is high; (c) Current direction when DP is low.

about 65 μA, so the voltage drop on the resistor R_S is 0.78 V, which is unacceptable under a 1.8 V power supply. Thus a 3.3 V power supply is employed to provide enough voltage swing for the DAC1 unit. For the DAC2 and DAC3, there is no need for R_S, so they are not source degenerated and the supply voltages are 1.8 V.

The Simulink simulation shows that the standard deviation of the first DAC units should be lower than 1‰ to guarantee the performance of the modulator. The Monte Carlo simulations show that the standard deviation of the presented DAC units is about 1‰. Thus, no DEM is used here to reduce the delay between the quantizers and the DACs and achieve a higher sampling rate.

D. Circuit Simulated Results

The simulated power consumption of each amplifier and quantizer are listed in TABLE IV. The I and Q paths together with digital circuits consume 53.2 mW from a 1.8 V power supply.

Fig. 16 shows the simulated normalized output spectrum with a 5 MHz full-scale input signal. The resolution bandwidth (RBW) is 28.08 kHz. In the interested band from 0.5 MHz to 33.5 MHz, the noise-floor is quite flat and the modulator achieves 66.46 dB SNR, 66.38 dB SNDR and 91.12 dB spurious free dynamic range (SFDR).

TABLE IV
POWER CONSUMPTION OF THE AMPLIFIERS AND QUANTIZER

Component	Amp1	Amp2	Amp3	Amp4	Quantizer
Power(mW)	5.1	5.1	5.3	5.89	3.96

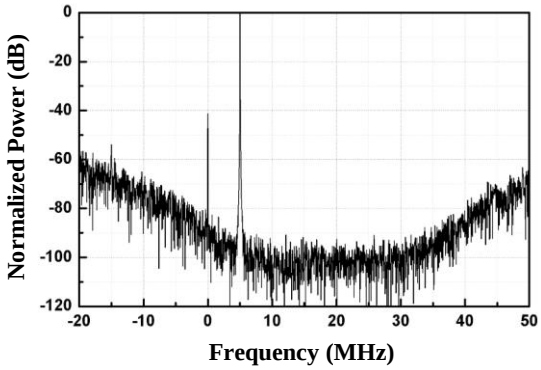


Fig. 16. Simulated output spectrum with a 5 MHz full-scale input signal. RBW=28.08 kHz. SNR=66.46 dB, SNDR=66.38 dB, SFDR=91.12 dB.

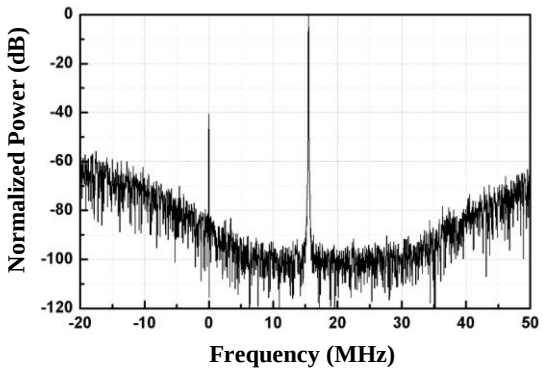


Fig. 17. Simulated output spectrum with a 15.5 MHz full-scale input signal. RBW=28.08 kHz. SNR=66.04 dB, SNDR=66.0 dB, SFDR=89.36 dB.

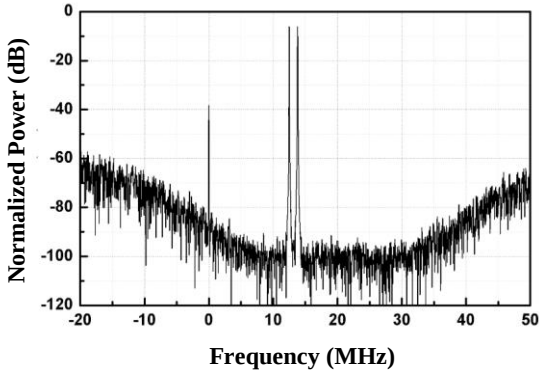


Fig. 18. Intermodulation simulation result with two-tone signal at 12.5 MHz and 13.8 MHz. RBW=28.08 kHz.

The simulated result with a 15.5 MHz input signal is shown in Fig. 17, and 66.04 dB SNR, 66.0 dB SNDR and 89.36 dB SFDR are achieved.

The simulated intermodulation performance with a two-tone signal at 12.5 MHz and 13.8 MHz is shown in Fig. 18. The amplitudes of both the tones are half of the full-swing. The 3rd-order intermodulation product (IM3) and 2nd-order intermodulation product (IM2) are lower than -90 dB.

IV. Measured Results

To lower down the cost, the proposed modulator has been implemented in 180 nm CMOS, together with clock generator and LVDS output drivers. Fig. 19 shows the test board and the chip micro-photograph. The input I/Q signals are injected into the board through two SMA connectors and converted into differential signals by two off-chip baluns. The 460 MHz clock is also injected through a SMA connector.

Fig. 20 shows the measured output spectrum with a 5 MHz full-scale input signal. In the interested band from 0.5 MHz to 33.5 MHz, the noise-floor is quite flat and the modulator achieves 64.5 dB SNR, 62.1 dB SNDR, and 67.2 dB SFDR. Compared with the simulated results, the SNRs of the measured results are about 2 dB lower, and the SNDRs are degraded by 4.2 dB. The deviations are mainly caused by non-ideal clock and higher non-linearity.

The measured result with a 15.5 MHz input signal is shown in Fig. 21, and 63.4 dB SNR, 61.8 dB SNDR and 67.3 dB SFDR are achieved.

The intermodulation performance of the modulator is tested with a two-tone signal at 12.5 MHz and 13.8 MHz (see Fig. 22). The amplitudes of both the tones are half of the full-swing. -63.6 dB IM3 and -69 dB IM2 are achieved. The 5th-order intermodulation product (IM5) is -76.3dB, and it's too small to harm the performance of the modulator.

A wideband quadrature power splitter (I/Q Generator) is used to generate the I/Q input signals, as shown in Fig. 19. Due to the wideband characteristics of the quadrature power

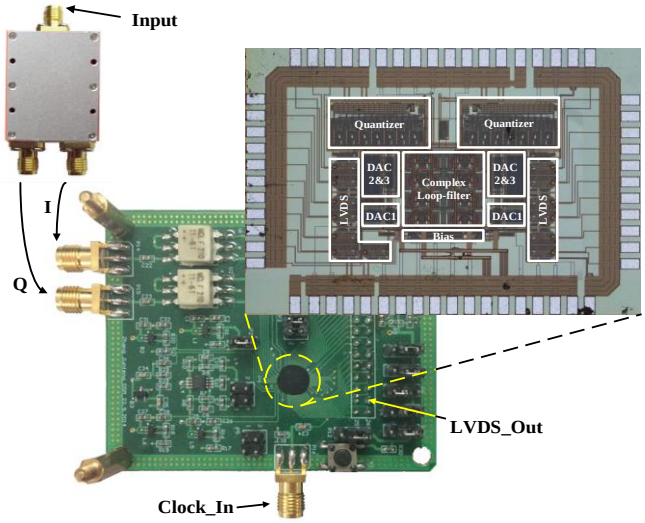


Fig. 19. Test board and chip microphotograph of the modulator.

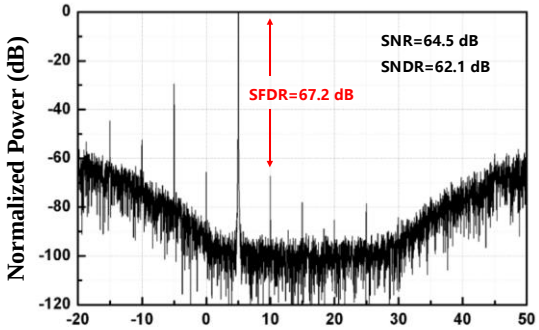


Fig. 20. Measured output spectrum with a 5 MHz full-scale input signal. RBW=14.04 kHz. SNR=64.5 dB, SNDR=62.1 dB, SFDR=67.2 dB.

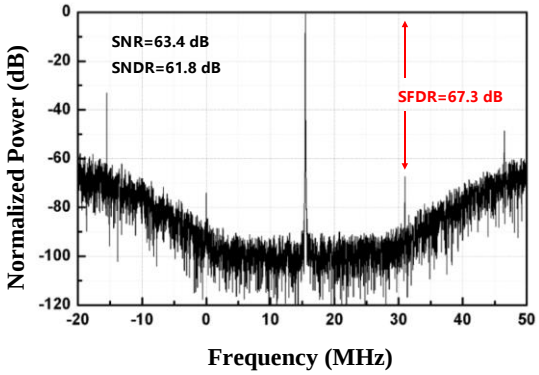


Fig. 21. Measured output spectrum with a 15.5 MHz full-scale input signal. RBW=14.04 kHz. SNR=63.4 dB, SNDR=61.8 dB, SFDR=67.3 dB.

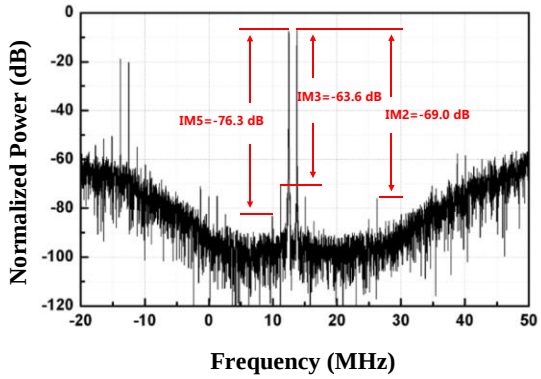


Fig. 22. Intermodulation measurement result with two-tone signal at 12.5 MHz and 13.8 MHz. RBW=14.04 kHz. IM3=-63.6 dB, IM2=-69.0 dB, IM5=-76.3 dB.

splitter, the I/Q matching performance of the generated I/Q input signals is not good. As a proof, the same I/Q Generator was also used to measure another sigma-delta modulator chip, and an IRR of around 30 dB before digital I/Q calibration was achieved [4]. In this work, the IRR measured with this I/Q Generator is also about 30 dB, as shown in Fig. 20. So this low IRR is mainly caused by the poor matching I/Q Generator.

In Fig. 23, the I/Q input signals come from the measurement equipment directly without any filtering and have a better I/Q matching. A much better IRR of 59.3 dB is achieved, which also verifies that the measured low IRR in Fig. 20 isn't caused

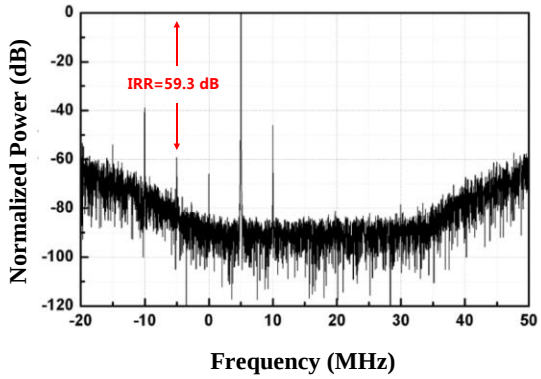


Fig. 23. IRR measured result. RBW=14.04 kHz. IRR=59.3 dB.

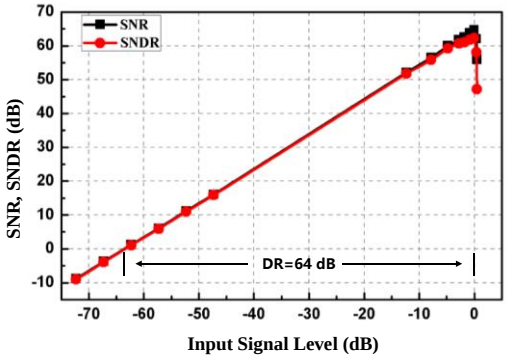


Fig. 24. SNR and SNDR versus input signal level with a 5 MHz signal. SNR_{peak}=64.5 dB, $SNDR_{peak}$=62.1 dB, DR=64 dB.

TABLE V
PERFORMANCE COMPARISON AMONG QBP CT MODULATORS

	This Work	[7]	[8]	[9]	[4]	[10]
Process (nm)	**180**	180	130	90	65	250
Supply (V)	**1.8**	1.8	1.2	1.2	1.2	2.5
BW (MHz)	**33**	8	2	20	20	20
IF (MHz)	**17**	8	3	10.5	12	10
SNDR (dB)	**62.1**	60.9	57.1	69	53.7	53.5
F_S (MHz)	**460**	200	64	340	480	320
IRR (dB)	**59.3**	>55	37	55	60.1	47.2
Power (mW)	**54.4**	12.1	4.2	56	8.1	32
FoM (pJ/conv)	**0.79**	0.84	1.78	0.61	0.52	2.06

by the sigma-delta modulator itself. However, the input I/Q signals have strong second harmonic (limited by the equipment, and the filtering is not possible in this test) and insufficient amplitude (limited by the output power ability of the equipment). Furthermore, its noise floor is higher than the in-band quantization noise.

Fig. 24 presents the plots of the SNR and SNDR versus the input signal level with a 5 MHz input signal. The peak SNR and SNDR are 64.5 dB and 62.1 dB, respectively, and the dynamic range (DR) is 64 dB.

Not including low-voltage differential signaling interface (LVDS), clock generator and pads, the modulator occupies a core area of 0.73 mm^2, and consumes 54.4 mW from a 1.8 V power supply, making a figure of merit (FoM) of 0.79 pJ/conv. Here FoM is defined by Power/(2×BW× $2^{(SNDR-1.76)/6.02}$), and smaller FoM is better. The modulator achieves superior FoM, even only implemented in 180 nm CMOS, by utilizing the following power saving techniques: in the system architecture, a feedback and feedforward hybrid architecture is used to implement the 4^{th}-order loop-filter, and a RZ feedback after the discrete-time differential operation is introduced into the input of the final integrator to realize the ELD compensation, saving a spare summing amplifier. In the circuit implementation, power-efficient amplifiers with high-frequency active feedforward and anti-pole-splitting techniques are employed in the active RC integrators, and self-calibrated comparators are used to implement the low-power 3-bit quantizers.

TABLE V compares the presented quadrature band-pass continuous-time (CT) ΣΔ modulator with the-state-of-the-art QBP CT ΣΔ modulators. [4] and [7] support multi-mode operations and only the maximum bandwidth modes are listed. Besides, the IRR in [4] is the result with the digital-calibration after the output of the modulator. This work achieves an improved performance over a wide signal bandwidth with a relatively low FoM.

V. CONCLUSION

A 4^{th}-order quadrature band-pass continuous-time sigma-delta modulator with a bandwidth of 33 MHz is proposed. Implemented in 180 nm CMOS, it occupies a core area of 0.73 mm^2 and achieves 64 dB DR, 62.1 dB SNDR, and 59.3 dB IRR with a 5 MHz input signal. The IM3 with a two-tone signal is -63.6 dB. Powered by a 1.8 V supply, the modulator consumes

54.4 mW and achieves a FoM of 0.79 pJ/conv. With wide bandwidth and high DR, the modulator makes it possible to achieve dual-channel GNSS reception from two different satellite systems with one receiver channel while simplifying the analog IF-filter and programmable-gain amplifier (PGA) design in the GNSS receiver. Five dual-channel modes covering most channels of four different systems are supported.

REFERENCES

[1] N. Qi, Y. Xu, B. Chi, et al, "A dual-channel GPS/Compass/Galileo /GLONASS reconfigurable GNSS receiver in 65nm CMOS", in IEEE Custom Integrated Circuits Conference (CICC), 2011, pp. 1-4.

[2] N. Qi, B. Chi, Y. Xu, et al. "A 180nm fully-integrated dual-channel reconfigurable receiver for GNSS interoperations", in IEEE European Solid-State Circuits Conference (ESSCIRC), 2013, pp. 177-180.

[3] Y. Xu, Z. Zhang, B. Chi, et al, "Dual-mode 10MHz BW 4.8/6.3 mW reconfigurable lowpass/complex bandpass CT ΣΔ modulator with 65.8/74.2 dB DR for a zero/low-IF SDR receiver", in Radio Frequency Integrated Circuits Symposium (RFIC), 2014, pp 313-316.

[4] Z. Zhang, Y. Xu, N. Qi, et al, "A 5/20MHz-BW 4.2/8.1 mW CT QBP ΣΔ modulator with digital I/Q calibration for GNSS receivers", in IEEE Asian Solid-State Circuits Conference (A-SSCC), 2013, pp. 393-396.

[5] G. Mitteregger, C. Ebner, S. Mechnig, et al, "A 20-mW 640-MHz CMOS continuous-time ADC with 20-MHz signal bandwidth, 80-dB dynamic range and 12-bit ENOB", in IEEE Journal of Solid-State Circuits (JSSC), 2006, 41(12), pp 2641-2649.

[6] A. Vasilopoulos, G. Vitzilaios, G. Theodoratos, et al, "A low-power wideband reconfigurable integrated active-RC filter with 73 dB SFDR", in IEEE Journal of Solid-State Circuits, 2006, 41(9), pp 1997-2008.

[7] C. Y. Ho, W. S. Chan, Y. Y. Lin, et al, "A quadrature bandpass continuous-time delta-sigma modulator for a tri-mode GSM-EDGE /UMTS/DVB-T receiver", in IEEE Journal of Solid-State Circuits (JSSC), 2011, 46(11), pp 2571-2582.

[8] K. W. Cheng, K. Natarajan, D. J. Allstot, "A current reuse quadrature GPS receiver in 0.13 μm CMOS", in IEEE Journal of Solid-State Circuits (JSSC), 2010, 45(3), pp 510-523.

[9] L. J. Breems, R. Rutten, et al, "A 56 mW continuous-time quadrature cascaded ΣΔ modulator with 77 dB DR in a near zero-IF 20 MHz band", in IEEE Journal of Solid-State Circuits (JSSC), 2007, 42(12), pp 2696-2705.

[10] J. Arias, P. Kiss, V. Prodanov, et al, "A 32-mW 320-MHz continuous-time complex delta-sigma ADC for multi-mode wireless-LAN receivers", in IEEE Journal of Solid-State Circuits (JSSC), 2006, 41(2), pp 339-351.

[11] Y. Ke, "Design of reconfigurable A/D converter for 4G radios", Ph.D. dissertation, Faculty of Eng., Leuven Univ., Leuven, Belgium, 2011.

[12] Y. Li, "CMOS Wideband Continuous-Time Sigma-Delta Modulator", M.S. thesis, Institute of Microelectronics, Fudan Univ., Shanghai, 2008.

[13] F. Henkel, U. Langmann, A. Hanke, et al, "A 1-MHz-bandwidth second-order continuous-time quadrature bandpass sigma-delta modulator for low-IF radio receivers", IEEE Journal of Solid-State Circuits (JSSC), 2002, 37(12), pp 1628-1635.

[14] F. Munoz, K. Philips, A. Torralba, "A 4.7 mW 89.5 dB DR CT complex/spl Delta//spl Sigma/ADC with built-in LPF", in IEEE ISSCC International Digest of Technical Papers, 2005.

[15] J. G. Kauffman, P. Witte, J. Becker, et al, "An 8.5 mW continuous-time modulator with 25 MHz bandwidth using digital background DAC linearization to achieve 63.5 dB SNDR and 81 dB SFDR", in IEEE Journal of Solid-State Circuits (JSSC), 2011, 46(12), pp 2869-2881.

[16] M. Ranjbar, O. Oliaei, R. W. Jackson, "A robust STF 6mW CT ΔΣ modulator with 76dB dynamic range and 5MHz bandwidth", in IEEE Custom Integrated Circuits Conference (CICC), 2010.

[17] M. Bolatkale, L. J. Breems, R. Rutten, et al, "A 4GHz CT ΔΣ ADC with 70dB DR and− 74dBFS THD in 125MHz BW", in IEEE ISSCC International Digest of Technical Papers, 2011, pp 470-472.

[18] J. Zhang, Y. Lian, L. Yao, et al, "A 0.6-V 82-dB 28.6-W continuous-time audio delta-sigma modulator", in IEEE Journal of Solid-State Circuits (JSSC), 2011, 46(10), pp 2326-2335.

[19] G. Keskin, J. Proesel, J. O. Plouchart, et al, "Exploiting combinatorial redundancy for offset calibration in flash ADCs" , in IEEE Journal of Solid-State Circuits (JSSC), 2011, 46(8), pp 1904-1918.

[20] P. Shettigar, S. Pavan, "A 15mW 3.6 GS/s CT-ΔΣ ADC with 36MHz bandwidth and 83dB DR in 90nm CMOS", in IEEE ISSCC International Digest of Technical Papers, 2012, pp 156-158.

[21] H. M. Geddada, C. J. Park, H. J. Jeon, et al, "Design Techniques to Improve Blocker Tolerance of Continuous-Time ADCs", in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23(1), pp 54-67.

[22] R. Schoofs, M. S. J. Steyaert, W. Sansen, "A design-optimized continuous-time delta–sigma ADC for WLAN applications", in IEEE Transactions on Circuits and Systems I: Regular Papers, 2007, 54(1), pp 209-217.

[23] T. Song, Z. Cao, S. Yan, "A 2.7-mW 2-MHz Continuous-Time ΣΔ Modulator With a Hybrid Active–Passive Loop Filter", in IEEE Journal of Solid-State Circuits, 2008, 43(2), pp 330-341.

[24] M. Andersson, M. Anderson, L. Sundstrom, et al, "A 7.5 mW 9MHz CT ΔΣ modulator in 65nm CMOS with 69 dB SNDR and reduced sensitivity to loop delay variations", in IEEE Asian Solid State Circuits Conference (A-SSCC), 2012, pp 245-248.

[25] A. Nikoozadeh, B. Murmann, "An analysis of latch comparator offset due to load capacitor mismatch", in IEEE Transactions on Circuits and Systems II: Express Briefs, 2006, 12(53), pp 1398-1402.

[26] P. M. Figueiredo, J. C. Vital, "Kickback noise reduction techniques for CMOS latched comparators", in IEEE Transactions on Circuits and Systems II: Express Briefs, 2006, 53(7), pp 541-545.

Junfeng Zhang was born in Gansu Province of China in 1991. He received his B.S. and M.S. degree from the Department of Microelectronics, Tsinghua University, Beijing, China, in 2013 and 2016 respectively. His research interests mainly focus on the design of low-power analog baseband circuits and high performance continuous-time sigma-delta modulators.

Yang Xu received the B.S. degree from the Department of Electronics Science and Technology, Huazhong University of Science and Technology, Wuhan, China, in 2010 and the M.S. degree from the Institute of Microelectronics, Tsinghua University, Beijing, China, in 2013. He is currently working towards the ph.D. degree at Oregon State University, Corvallis. His research interests mainly focus on the design of low-power analog baseband circuits and multi-mode reconfigurable continuous-time sigma-delta modulator (CTSDM) for multi-standard receivers.

Zehong Zhang was born in Hubei Province of China in 1989. He received his B.S. degree from the Department of Electronics Science and Technology, Huazhong University of Science and Technology, Wuhan, China, in 2011 and the M.S. degree from the Institute of Microelectronics, Tsinghua University, Beijing, China, in 2014. His research interests mainly focus on the design of continuous-time sigma-delta modulators.

Yichuang Sun (M' 90-SM' 99) received the B.Sc. and M.Sc. degrees from Dalian Maritime University, Dalian, China, in 1982 and 1985, respectively, and the Ph.D. degree from the University of York, York, UK, in 1996, all in communications and electronics engineering. He is currently a Professor in the School of Engineering and Technology of the University of Hertfordshire, UK. His research interests fall into two major areas: wireless and mobile communications including MIMO techniques, MIMO-OFDM, MU-MIMO, distributed space-time coding, cooperative and relay communications, cognitive radio communications, and green radio; and microelectronic circuits and systems including RF, analog and mixed-signal circuits, wireless transceiver architectures, continuous-time active filters, impedance matching networks, antenna tuning systems, and mixed-signal circuit tests. Professor Sun has published over 260 technical papers and contributed nine chapters in edited books. He has also published four text and research books including Wireless Communication Circuits and Systems, IEE Press, 2004. He has been a Series Editor of the IEE Circuits, Devices and Systems Book Series . He is an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS-I and Editor of the ETRI Journal. He has been a Guest Editor of six IET (IEE) journal special issues including the issues on MIMO wireless and mobile communications published in IEE Proceedings: communications in 2006, advanced signal processing for wireless and mobile communications in IET Signal Processing in 2009, and cooperative wireless and mobile communications in IET Communications in 2013. Professor Sun has also been widely involved in various IEEE technical committee and international conference activities.

Zhihua Wang (M'99–SM'04-F'17) received the B.S., M.S., and Ph.D. degrees from the Department of Electronic Engineering, Tsinghua University, Beijing, China, in 1983, 1985 and 1990 respectively. In 1983, he joined the faculty at Tsinghua University, where he is a full Professor since 1997 and Deputy Director of Institute of Microelectronics since 2000. From 1992 to 1993, he was a Visiting Scholar at Carnegie-Mellon University. From 1993 to 1994, he was a Visiting Researcher at KU Leuven, Belgium. His current research mainly focuses on CMOS RF IC and biomedical applications. His ongoing work includes RFID, PLL, low-power wireless transceivers, and smart clinic equipment with combination of leading edge CMOS RFIC and digital imaging processing techniques. Prof. Wang has served as Deputy Chairman of Beijing Semiconductor Industries Association and ASIC Society of Chinese Institute of Communication, as well as Deputy Secretary General of Integrated Circuit Society in China Semiconductor Industries Association. He had been one of the chief scientists of the China Ministry of Science and Technology serves on the expert committee of the National High Technology Research and Development Program of China (863 Program) in the area of information science and technologies from 2007 to 2011. He had been an official member of China Committee for the Union Radio-Scientifique Internationale (URSI) during 2000 to 2010. He was the chairman of IEEE Solid-State Circuit Society Beijing Chapter during 1999–2009. He has been a Technologies Program Committee member of ISSCC (International Solid-State Circuit Conference) during 2005 to 2011. He is an Associate Editor for IEEE TRANSACTIONS ON BIOMEDICAL CIRCUITS AND SYSTEMS.

Baoyong Chi (M'08) received the B.S. degree in microelectronics from Peking University, Beijing, China, in 1998, and the Ph.D. degree from Tsinghua University, Beijing, China, in 2003. From 2006 to 2007, he was a Visiting Assistant Professor with Stanford University. He is currently a Professor with the Institute of Microelectronics, Tsinghua University. In his nine years of academic experience, he has authored or coauthored over 90 academic papers and two books. He holds over ten patents. His research interests include RF/millimeter-wave integrated-circuit design, analog integrated circuit design, and monolithic wireless transceiver analog front-ends. Dr. Chi has been a Technical Program Committee (TPC) member of A-SSCC since 2005.