Functional Oxide as an Extreme High-k Dielectric Towards 4H-SiC MOSFET Incorporation

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Abstract. MOS Capacitors are demonstrated on 4H-SiC using an octahedral ABO_3 ferroic thin-film as a dielectric prepared on several buffer layers. Five samples were prepared: ABO_3 on SiC, ABO_3 on SiC with a SiO_2 buffer (10 nm and 40 nm) and ABO_3 on SiC with an Al_2O_3 buffer (10nm and 40 nm). Depending on the buffer material the oxide forms in either the pyrochlore or perovskite phase. A better lattice match with the Al_2O_3 buffer yields a perovskite phase with internal switchable dipoles. Hysteresis polarization-voltage loops show an oxide capacitance of ~ 0.2 μF/cm^2 in the accumulation region indicating a dielectric constant of ~120.

Introduction

Although silicon carbide MOSFETs are today commercially available the SiC/SiO_2 interface still limits performance, particularly at lower voltages, from reaching its full potential. An alternative to this is to incorporate high-*k* dielectric insulators. Previous work has yielded moderate success with HfO_2, Al_2O_3 and TiO_2 amongst other materials. A reduced interface trap density is observed albeit with increased gate leakage due to reduced bandgap (although this may be mitigated by a SiO_2 buffer layer) [1-4].

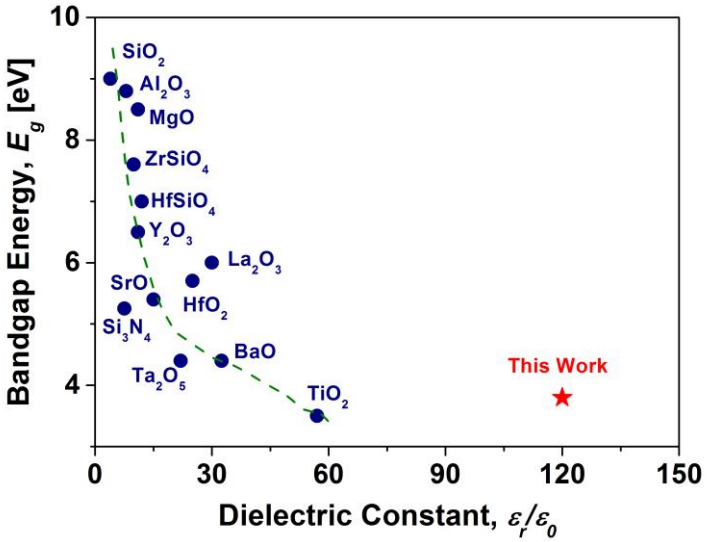

Fig. 1: Comparison of dielectric materials for use on 4H-SiC

Fig. 1 shows the trade-off between bandgap and dielectric constant in typical oxide materials used on 4H-SiC alongside the significantly increased value achieved in this work. The best solution may be an oxide stack to utilise the natural SiO_2 oxide of SiC while getting the high-k from elsewhere, this is a similar idea to the phosphosilicate glass (PSG) method for SiC where a PSG/SiO_2 stack can give the low leakage of the SiO_2 oxide combined with an improved mobility [5]. Complex oxide stacks utilising exotic materials are becoming more common in CMOS technology and even in power electronics e.g. high-k stacks in silicon CMOS [6]. In terms of power electronics materials such as GaN and diamond, these possess no naturally occurring oxide. High-k materials have been demonstrated for GaN [7] and transition metal oxides such as MoO_3 for diamond (as well as MESFET devices) [8-9]. So an oxide / ferroic stack may indeed provide an interesting solution for SiC FETs.

Due to the orientable polarization contribution, the polarizability of some functional oxides unit cells is far stronger than classical high-*k*. The dielectric constant of these materials is naturally very high and may be altered by a phase transition in the material, achieved by the application of an external electric field. This could lead to a new paradigm for scaling transistor technology allowing an 'amplification' of low gate voltage to enable very low switching pulses. In addition, functional oxides are recognised as having other important potential applications [10].

In this pioneering experiment, oxygen octahedral ABO_3 ferroic thin-films (Fig. 2) are deposited chemically at temperatures below 700° C on five samples of 4H-SiC. A Ti/Ni ohmic metallisation is utilised on the highly nitrogen *n*-type doped (> $1x10^{19}$ $cm^{-}3$) backside, a low doped 35 µm epitaxial layer (4 x 10^{15} cm^{-3}) is present on top of the substrate. After standard RCA cleaning the buffer oxides were deposited and ferroic film grown: one bare SiC, two with thermally grown SiO_2 as a buffer and two with Al_2O_3 as a buffer. Silver gate contacts were evaporated on to the samples to create MOS capacitor structures.

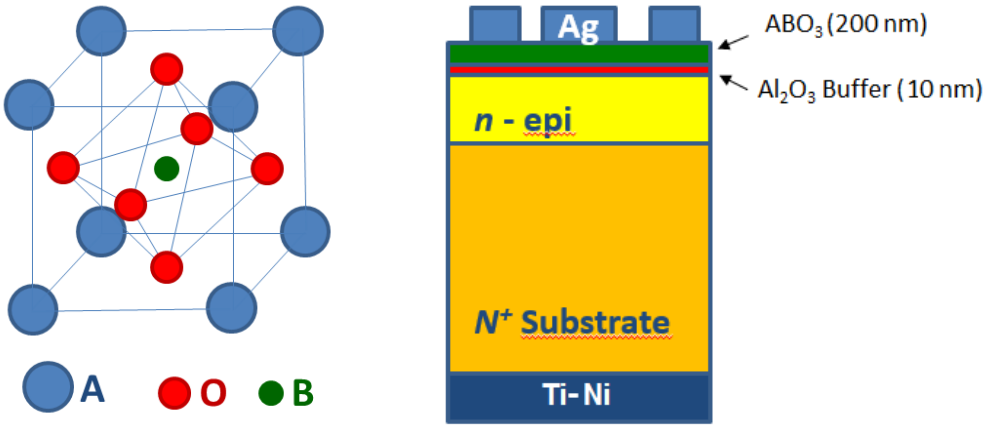

Fig. 2: Orientation of the perovskite structure and structure of typical MOSCAP

Results & Discussion

It is observed the functional oxide may form in either a pyrochlore or perovskite phase depending on deposition conditions. X-Ray Diffraction (XRD) analysis (Fig. 3) has shown the oxide to be in a preferential perovskite form on the Al_2O_3 sample while pyrochlore has the predominant texture on the others, in particular on SiO_2. This is thought to be due to a better lattice match with the Al_2O_3 material. A SiC reference sample with no oxide deposited is also included as a comparison. In principle, the perovskite phase is more interesting as the pyrochlore does not possess switchable internal dipoles.

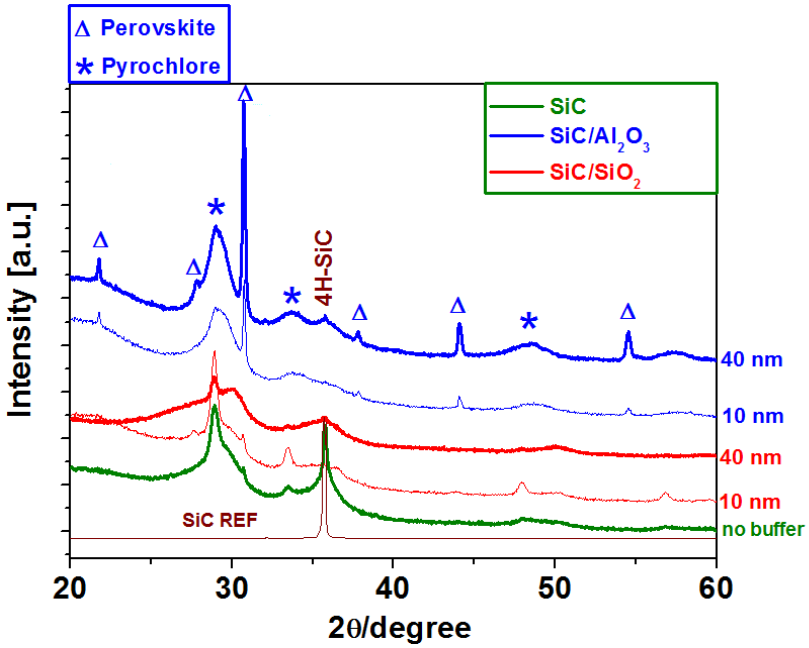

Fig. 3: XRD of the ABO_3 oxide on SiC, SiO_2 and Al_2O_3.

Hysteresis polarization-voltage loops (*P*-*V*) and capacitance-voltage (*C*-*V*) characterisation are displayed in Fig. 4 for the 10nm Al_2O_3 – ferroic oxide stack. *P*-*V* loops were performed in a Radiant *LC* meter where the low frequency - a low enough frequency where the internal antiparallel dipoles are able to respond. It is clear from Fig. 4 that this stack does indeed contain a polarization arising from the switchable dipoles of the perovskite structure. This is further evidenced by the hysteresis observed in the capacitance-voltage characteristic (derived from the derivative *(dP/dV)*) of Fig. 5. Assuming an Al_2O_3 thickness of 10 nm and relative dielectric constant of 8 along with a ferroic oxide thickness of 200 nm it is possible to derive a high density oxide capacitance of $C \sim 0.2$ $\mu F/cm^2$ in the accumulation region which represents a dielectric constant of ~ 120 (Fig. 5) a factor x15 larger than Al_2O_3 and almost and order of magnitude larger than HfO_2.

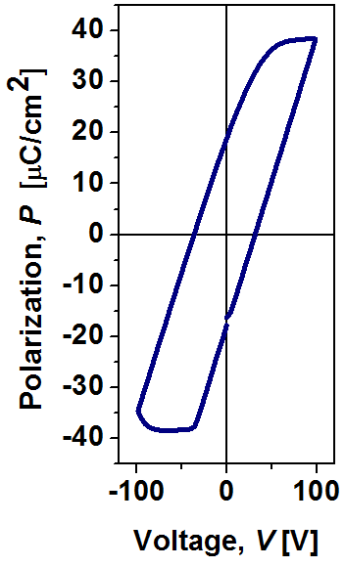

Fig. 4: *P*-*V* hysteresis loop.

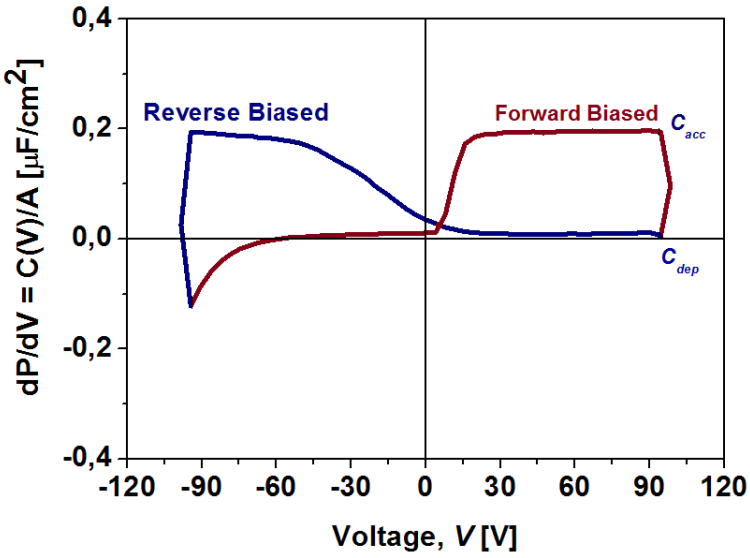

Fig. 5: Capacitance-voltage characteristic measured from the derivative of *P*-*V* at $\tau = 1$ ms (1kHz).

Summary

This experiment demonstrates the promise of ferroic materials for integration in to future SiC MOSFET devices to further advance this technology. The extremely high k-value yielded here potentially allows further scaling of SiC MOSFETs, SiO_2 as a gate oxide as well as having problems with interface traps is plagued by long term instability, a high-k material should be better equipped to deal with high electric fields. Further work needs to be undertaken to perfect the exact stack thickness and find the ideal conditions for deposition of the functional oxide. This will be aided by further MOS capacitor fabrication and analysis of leakage currents and interface traps before integration in to FET devices.

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