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Hardware Design of the Discrete Wavelet Transform: an Analysis of Complexity, Accuracy and Operating Frequency

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Abstract

The purpose of this paper is to present a comparative analysis of hardware design of the Discrete Wavelet Transform (DWT) in terms of three design goals: accuracy, hardware cost and operating frequency. Every design should take into account the following facts: method (non-polyphase, polyphase and lifting), topology (multiplier-based and multiplierless-based), structure (conventional or pipelined), and quantization format (floating-point, fixed-point, CSD or integer). Since DWT is widely used in several applications (e.g. compression, filtering, coding, pattern recognition among others), selection of adequate parameters plays an important role in the performance of these systems.

Key words: Discrete Wavelet Transform; topology; quantization format; accuracy.

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Diseño hardware de la transformada wavelet discreta: un análisis de complejidad, precisión y frecuencia de operación

Resumen

El propósito de este documento es presentar un análisis comparativo de esquemas hardware de la Transformada Wavelet Discreta, DWT, en términos de tres objetivos de diseño: precisión, complejidad y frecuencia de operación. Cada diseño debe considerar los siguientes aspectos: método (no polifásico, polifásico y *lifting*), topología (basados en multiplicadores y sin multiplicadores), estructura (convencional o pipeline) y formato de cuantización (punto flotante, punto fijo, CSD o entero). Dado que la DWT es ampliamente utilizada en diversas aplicaciones (por ejemplo en compresión, filtrado, codificación, reconocimiento de patrones, entre otras), la selección adecuada de parámetros de diseño desempeña un papel importante en el diseño de estos sistemas.

Palabras clave: DWT; topología; formato de cuantización; precisión.

1 Introduction

The Discrete Wavelet Transform is a powerful tool for the multi-resolution analysis of different kind of signals (e.g. biomedical, voice, image and video). Among others, DWT is used in filtering [1],[2],[3], compression [4],[5],[6],[7], [8],[9],[10], pattern recognition [11],[12],[13],[14] coding,[15],[16],[17],[18],[19] applications. Since several systems require real-time operation [20],[21],[22], [23],[24],[25],[26], the design of hardware topologies of the DWT is a current issue.

Design of the hardware implementation of the DWT has several choices. In terms of the method, it is carried out within non-polyphase (convolution-based) [27], polyphase [28],[29],[30],[31] or lifting schemes [32],[33],[34]. In terms of the topology, the schemes are multiplier-based [27],[35],[36],[37],[38], [39] or multiplierless-based [28],[29],[30],[31],[40],[41],[42],[43],[44],[45],[46], [47],[48],[49]. In terms of the quantization of the filters weights, the system can work with floating-point data [35], fixed-point data [27],[36],[37, 41], Canonical Signed Digit (CDS) [30],[31],[40] or integer data [28],[29],[42],[43], [44],[45]. Finally, structure is conventional [27],[28],[29],[30],[31],[40],[42],[43], [44],[45] or pipelined-based [41],[50],[51],[52],[53],[54],[55].

Every choice plays an important role in the performance of the system. For example, non-polyphase schemes have easier design than the others, but lower throughput. Lifting schemes with non-pipelined structures have higher path delay than the non-polyphase schemes. Quantization error decreases with long word-bits, but the hardware cost increases. Therefore, the following design aims must be taken into account: high accuracy, high operating frequency or low hardware cost. None of them is able to simultaneously optimize the above objectives. A good design for one of them cannot be a good design for other aim.

The rest of the paper is organized, as follows. Firstly, the background of the Discrete Wavelet Transform is presented. Secondly, a review of works in terms of complexity is shown. Thirdly, main concepts behind accuracy and some of the most remarkable works in terms of accuracy are illustrated. Then, a discussion about pipelined-based and conventional schemes is presented.

2 Background of the discrete wavelet transform

Discrete Wavelet Transform (DWT) is one of multi-resolution transforms in which both time and frequency of the input signal are analyzed. At the point of view of filter banks, DWT is carried out in two stages: firstly, the input signal is filtered with two half-band filters (i.e. low-pass filter and high-pass filter); secondly, the filtered signals are decimated by a power of two. There are many filters that satisfy the conditions of the wavelet transform and they are grouped in families. In the same family, there are many filters related to the length of the filter.

The easiest representation of the DWT is the convolution (non-polyphase) approach. In this case, the two stages of the DWT are clearly separated (Figure 1). If the DWT is designed as a FSM (Finite State Machine), the first state consists on calculating the filtered signals (it can use several clock cycles), and then in the second state, half of data are eliminated (by the decimation process). Although its hardware implementation is less complex, throughput is not the highest as possible.

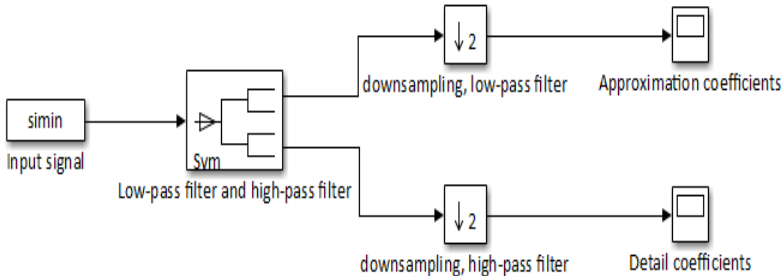

Figure 1: Generic block diagram of the non-polyphase scheme.

The second design method is the polyphase one. In this case, in the same state convolution and decimation process are carried out. The input signal is down-sampled (i.e. split) in data of even clock cycles and data of odd clock cycles. Then, data of the even cycles are filtered with the even weights of the filter (low-pass or high-pass) and data of the odd cycles are filtered with the odd weight of the filter. At the end, a sum (between even filtered data and odd filtered data of the same filter) is applied (Figure 2) [29]. Unlike the convolution approach, half of data are not wasted. Therefore, throughput of this kind of schemes is the double that of the convolution-based schemes.

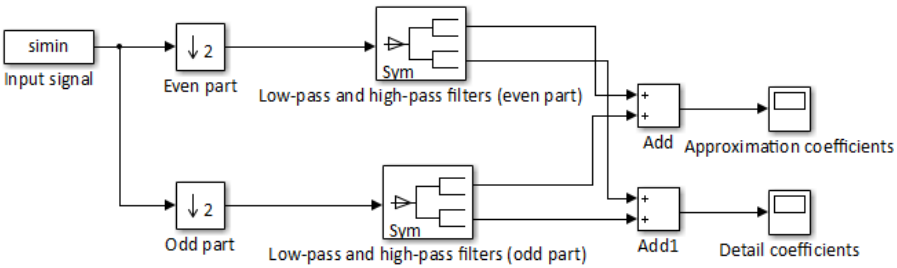

Figure 2: Generic block diagram of the polyphase scheme.

A special case of a polyphase scheme is the lifting approach. In a similar way of the polyphase structure, the input signal is down-sampling before the filtering process. Nevertheless, the approximation and detail coefficients are calculated using P (prediction) unit and U (updating) unit. With data of odd part and the result of the P unit, detail coefficients are obtained.

With the detail coefficients, the result of the U unit and data of the even part, approximation coefficients are found. P and U functions are directly related to the selected wavelet base. Figure 3 shows a generic block diagram in which these functions are not specified.

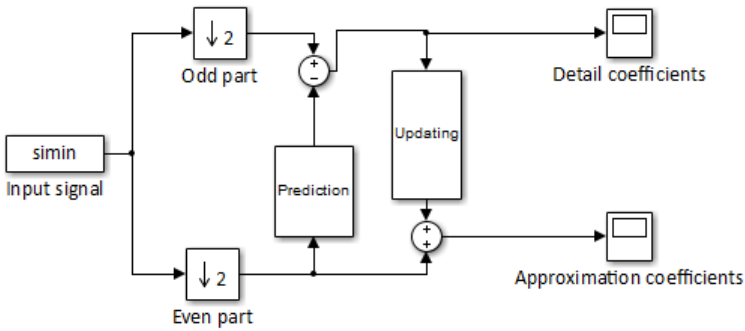

Figure 3: Generic block diagram of the lifting scheme.

In terms of throughput, the result of the lifting scheme is the same than the result of the polyphase scheme. Differences lie on hardware resources and latency, but it depends on the P and U functions (and therefore the selected wavelet base).

3 Design goal: complexity

Since DWT uses mathematical operations (adder, sum, down sampling), one parameter to take into account is the topology, which can be multiplier-based or multiplierless-based. In the first case, convolution process between the input signal and the filters weigths are carried out by multiplier units; in the second case, it is calculated by right-shifts and left-shifts.

In order to illustrate the differences between the topologies with an example, we have selected the wavelet base 5/3 (i.e. CDF 2, 2). The filters weights have the values, as follows:

$$h_0(k) = \frac{\sqrt{2}}{8}[-1 \quad 2 \quad 6 \quad 2 \quad -1] = [-0.167 \quad 0.353 \quad 1.06 \quad 0.353 \quad -0.167] \quad (1)$$

$$h_1(k) = \frac{\sqrt{2}}{4}[1 \quad -2 \quad -1] = [0.353 \quad -0.707 \quad 0.353] \tag{2}$$

Where h_0 is the low-pass filter, h_1 is the high-pass filter, k is in the range $[0 \quad 4]$ for h_0, and k is in the range $[0 \quad 2]$ for h_1.

In the case of multiplier-based schemes, the design uses one multiplier for each weight of the filter (i.e. 5 multipliers for h_0 and 3 multipliers for h_1) and one adder to obtain approximation coefficients and one adder to obtain detail coefficients. These multiplier units must allow multiply data in float-format or fixed-format, with several bits in inputs and outputs. Therefore, hardware resources are directly related to the length of the input signals (word-length). The higher the word-length of the inputs, the higher is the hardware cost. Like the multiplier units, the adder unit must work with several bits and then hardware cost is directly related to the word-length.

Figure 4 shows a generic block diagram for the low-pass filter of the 5/3 wavelet base, for a multiplier-based topology.

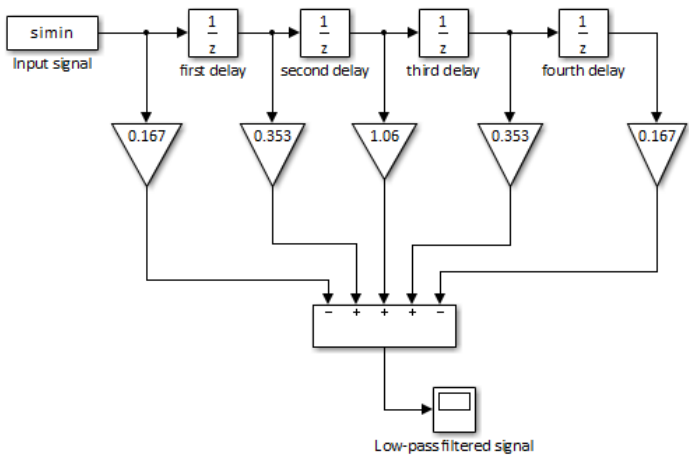

Figure 4: Generic block diagram of the low-pass filter 5/3 wavelet base: multiplier-based topology.

If the input signal is quantized to 16-bits, and the filters weights are quantized to 8-bits (e.g. in fixed-format), multiplier units must work with 23-bits and the adder unit must work with at least 23-bits. The higher the

total number of bits, the higher is the delay of the multiplication process.

On the other hand, in multiplierless-based schemes the multiplier units are eliminated of the design and then mathematical operations are carried out by left-shifts or right-shifts. If the signal is left-shifted, one bit with value of 0_b is added at the right of the signal; otherwise, if the signal is right-shifted, the least significant bit of the signal is discarded. Left-shift operation is equal to multiply by 2 the input; right-shift operation is equal to the integer part of the division by 2 of the input signal. For example, if the input signal is 10111_b, the result of the left-shift is 101110_b and the result of the right-shift is 1011_b. In decimal format, the input signal is 23, the result of the left-shift is 46 and the result of the right-shift is 11. As consequence of the right-shift, a clipping error appears. However, clipping error is enough low and then quantization error is low, too.

In multiplierless-based schemes, if data are quantized with integer format, the length of the internal signals is significantly lower than in the case of multiplier-based topology, even if the later uses integer quantization, too. For example, suppose that the input signal is 5-bits (e.g. $23 = 10111_b$), and the weight of the filter is 2-bits (e.g. $2 = 10_b$). With a multiplier unit the result is 7 bits (e.g. $46 = 0101110_b$). However, as we explain in the above paragraph, the result with one right-shift (that it is equal to multiply by 2) is 6 bits (e.g. 101110_b). Although input data is the same in both topologies, multiplierless-based schemes have lower bits than the multiplier-based schemes.

Figure 5 shows a generic block diagram for the low-pass filter of the 5/3 wavelet base, for a multiplierless-based topology with integer data. Constant $\sqrt{2}$ has been ignored. It is taken into account in a post-amplifier stage.

An example of multiplierless-based topology and integer quantization of the weights of the filter is found in the work of Ballesteros and Moreno [28]. In that case, they use left-shift, right-shift, delay, and split units to compute the wavelet base 5/3. In terms of hardware resources, the wavelet transform use 99 slice registers, 130 slice LUTs, 87 LUT FF-pairs and 51 bounded IOBs. With that design the maximum delay is 3.59 ns with latency equal to 2. This design was used for data hiding purposes [29].

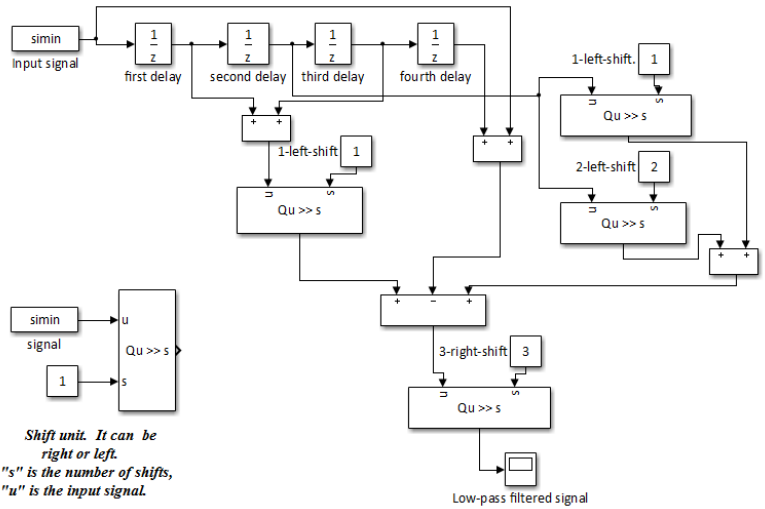

Figure 5: Generic block diagram of the low-pass filter 5/3 wavelet base: multiplierless-based topology.

Summarizing, in terms of complexity is better a design with multiplierless-based topology and integer quantization of the weights of the filter than with multiplier-based topologies, even if quantization of the filters weights is integer, too.

4 Design goal: accuracy

One of the most important requirements in several systems is accuracy. If a system satisfies this requirement, the user knows that the obtained data are highly close to the theoretical data. In the case of hardware wavelet-based systems, it is desirable that the quantization error (q_e) of the filters weights is the lower as possible, and therefore the obtained data are highly similar to the real one. If the system uses the decomposition (DWT) and the reconstruction (IDWT) stages, the total error due to the quantization is known as the reconstruction error (r_e). In some applications, the system tolerates values of r_e 2 %; but in other cases (e.g. data hiding systems) r_e must be lower than 0.1 %. In this section we present some architectures of the DWT-IDWT and they are analyzed in terms of accuracy.

Since accuracy is strongly related with the quantization process of the filters weights, the main point in the design is to select the most appropriate format to represent data. There are four formats, as follows: floating-point, fixed-point, Canonical Signed Digit (CSD) and integer. In floating-point format, the filters weights are represented by several bits related to the integer part and the mantissa. The higher the number of bits, the lower is the quantization error. Nevertheless, higher precision implies higher hardware cost. In the case of fixed-point format, binary representation encompasses two parts: integer part and fractional part. In a similar way of float format, the total number of bits is strongly related to the quantization error. In the third case, in CSD, every bit can be a positive or a negative power of two (i.e. $0.\overline{1} = -0.25$) and then the total number of bits to represent data is lower than in fixed format (because it does not need a sign bit). Finally, integer format is the easiest format in terms of binary representation. It is useful in multiplierless topologies in which data operations (multiplication, division) are performed by right-shifts and left-shifts.

In order to illustrate the quantized error with an example, we have selected the wavelet base 5/3. Their values are shown in Eq. 1 and 2.

In fixed-format, if the weights are represented with six bits, one bit is for the integer part and five bits are for the decimate part (e.g. $|h_0(1)| = 0.00101_b = 0.15625$). In this example, the sign is not included within binary data. The quantized filters for the 5/3 wavelet base are obtained as follows:

$$h_{0quantized}(k) = [-0.15625 \quad 0.34375 \quad 1.0625 \quad 0.34375 \quad -0.15625] \tag{3}$$

$$h_{1quantized}(k) = [0.34375 \quad -0.6875 \quad 0.34375] \tag{4}$$

Since by definition $\sum h_0(k) = \sqrt{2}$ and in the current case:
$\sum h_{0quantized}(k) = 1.4375$, the total quantized error is 1.64 %.

In the case of integer format, the term $\sqrt{2}$ of this wavelet base can be factorized in a similar way of [28, 29], and then the weights are represented by rational terms in which both the numerator as the denominator are integer data. Now, quantization error is only due to the division process which is related to the right-shifts of data (i.e. $1/(2^p)$ needs p right-shifts).

The authors of [28, 29] found that the quantization error is up to 0.0031 %. In the case of data hiding schemes based on LSB (Least Significant Bit) substitution is very useful working with a very low quantization error with the aim of recovering the embedded data.

With a second example of the quantization process with fixed-format, suppose that the wavelet base db2 is selected. The decomposition filters are shown in Equations 5 and 6:

$$h_0(k) = [-0.1294 \quad 0.2241 \quad 0.8365 \quad 0.4830] \tag{5}$$

$$h_1(k) = [0.4830 \quad 0.8365 \quad -0.2241 \quad -0.1294] \tag{6}$$

With nine bits, the binary representation of the weights is, for example, $|h_0(1)| = 0.00100001_b = 0.12890625$. The quantized filters for db2 are obtained as follows:

$$h_{0quantized}(k) = [-0.12890625 \quad 0.2265625 \quad 0.8359375 \quad 0.48046875] \tag{7}$$

$$h_{1quantized}(k) = [-0.48046875 \quad 0.8359375 \quad -0.2265625 \quad -0.12890625] \tag{8}$$

In the current case $\sum h_{0quantized}(k) = 1.4140625$ and then the total quantized error is 0.01 %. This result is better than the obtained in the first example; however, in the current case the quantization process uses nine bits instead of six bits.

Table 1 shows the comparison of some works in the design of wavelet transform. In the first column, the method of the design and the proposal are included (Non-pol.: non-polyphase, pol.: polyphase, lif.: lifting). In the second column, it is presented the topology (M: multiplier, Ml: multiplierless). In the third column, it is presented the type of structure (C: conventional, P: pipelined). In the fourth column, quantization format is defined. In the fifth column, the highest quantization error or/and the total reconstruction error are calculated. Finally, in the sixth column, the strengths and weakness of the proposal are identified.

Table 1: Comparison in terms of accuracy.

Work	**T**	**S**	**Q**	$q_e(max)$, $r_e(total)$	**Strengths and weakness**
[35] Lif.	M	P	Floating-point	Non-fixed	It allows choosing desired data precision. Long word-width.
[36] Lif.	M	P	Fixed-point	$q_e \leq 3\,\%$	High size of internal signals. Middle frequency operation.
[27] Non-pol.	M	C	Fixed-point	$q_e \leq 2\,\%$	Non-external memories. Very low latency.
[37] Lif.	M	P	Fixed-point	$q_e \leq 0.02\,\%$	Very low latency. Long word-width. Middle hardware cost.
[30],[31] Pol.	Ml	C	CSD	$q_e \leq 7\,\%$	Long sum-product terms. Long latency.
[40] Non-pol.	Ml	C	CSD	$q_e \leq 4\,\%$	Long sum-product terms. Long latency.
[41] Lif.	Ml	P	Fixed-point	$q_e \leq 6\,\%$	High frequency operation. Middle hardware cost.
[42]	Ml	C	Integer	$q_e \leq 5\,\%$	It can work for image processing.
[43],[44] Lif.	Ml	C	Integer	$q_e \leq 2.5\,\%$	Non-reconfigurable. Middle hardware cost. Real-time operation.
[45] Pol.	Ml	C	Integer	$q_e \leq 0.0031\,\%$	Non-reconfigurable. Middle hardware cost. Real-time operation.
[28],[29] Pol.	Ml	C	Integer	$q_e \leq 0.0031\,\%$ $r_e \leq 0.0092\,\%$	Non-reconfigurable. Low latency and low hardware cost. Real-time operation.

As it is expected, quantization format is the most important parameter in terms of accuracy. Very low quantization error may be obtained with multiplier or multiplierless topologies. However, designs are less complex with multiplierless topologies because they need only shifts (instead of multiplier units).

If accuracy is the goal of the design, it is suggested multiplierless topologies with integer quantization. Since the throughput of lifting and polyphase schemes is the same, any of them can be selected.

5 Design goal: operating frequency

Another important aspect to take into account in the design of the DWT and the inverse DWT (IDWT) is the operating frequency. Several applications works with signals of high frequency and then it is necessary a scheme fast response. We compare pipelined-based designs and conventional designs.

One disadvantage of the lifting schemes over the non-polyphase schemes is that the latter has a higher value of the delay path and therefore, it is expected that its operating frequency is lower. To overcome this problem pipelined architectures are used. For example, the highest operating frequency of the DWT can increase of 117 MHz to 277 MHz with a pipelined structure [54]. In another work, it has been found that the highest operating frequency depends on the number of pipeline stages. The higher the number of pipeline stages, the higher is the highest operating frequency (i.e. 60 MHz with 3 pipeline stages, 186 MHz with 18 pipeline stages [41]). However, pipelined-based scheme does not always ensure a high value of operating frequency. For example, a design of the 9/7 lifting wavelet with pipeline-based structure, fixed-point quantization of the filters weights and multiplierless-based topology has highest operating frequency up to 100 MHz [55].

Another approach consists on using Distributed Arithmetic. For example, the db4 wavelet base is implemented with a ROM lookup table and a cascade of shift registers, into a parallel structure. In this approach, the highest operating frequency is 134 MHz [56].

On the other hand, in some works with multiplierless-based topologies and conventional structures, the highest operating frequency is 110 MHz [30], 140 MHz [31] or 166 MHz [28]. These values are lower than the obtained in [54] but higher than the results of [55] and [41] (with 3 pipeline stages).

Summarizing, although pipelined-based structures may have lower delay path, choice of this structure does not guarantee the high values of operating frequency. Other facts, like topology and quantization, should be taken into account, too.

6 Conclusion

In this paper we revised several works of hardware implementation of the DWT. Proposals were analyzed in terms of three design aims: complexity, accuracy and highest operating frequency. In any design, the following parameters must be taken into account: method (convolution, polyphase, lifting), topology (multiplier-based or multiplierless-based), structure (conventional, pipelined), and quantization format (floating-point, fixed-point, CSD, integer).

Firstly, if the aim of the design is low complexity (and low hardware cost), it is suggested multiplierless topologies. In addition, integer data uses lower number of equivalent blocks than the other formats. In terms of the method, there is not a meaningful difference between polyphase and lifting schemes.

Secondly, if the aim is accuracy, the most important aspect in the design is the quantization format. It has been found low error values when the system works with integer data (it does not matter about the structure). It is worth noting that multiplierless-based schemes take advantage of integer data, and therefore this choice is also suggested.

Finally, if the aim is operating frequency, the best result was found in a pipelined structure. Nevertheless, some conventional designs obtained better results than some pipelined-based designs, and then it is not asserted than pipelined-based structures always outperform conventional structures.

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