Doubly Self-Aligned DMOSFET in SiC for Microgravity Manufacture

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Abstract

The need exists for power electronics capable of operation at high temperatures in a high radiation environment, such as in deep space. There is a rationale for fabricating such devices from materials already in situ, such as building very large phased array antennas. Device manufacture on human-staffed microgravity platform presents a challenge to the tight lithographic alignment required for traditional fabrication methods. Presented here for the first time is a process sequence to produce high-mobility DMOS FETs with no masking steps requiring critical alignment, yet yielding channel lengths of 0.15 micron. The fabrication process is further designed to utilize and recycle materials expected to be available on certain classes of asteroids and within extinct comets, with minimal need for reagents from earth. One application is manufacture of the tens of millions of MMIC power amplifiers required for wireless power transfer to terrestrial customers from solar power satellites in geostationary earth orbit.

INTRODUCTION

A 950 meter phased array antenna delivering 6 GW to a 10 km diameter receiving antenna on earth at 2.45 GHz and having a 0.8 wavelength spacing between elements (to prevent grating lobes, which waste power and disrupt communication) requires up to 48,413,486 power amplifiers. For tapered beam profiles (e.g. Gaussian, Taylor, Dolph-Chebychev) antenna elements at the periphery of the array require less power, so that several can be served by a single power amplifier (PA). This can reduce the number needed, but based on current MMIC PA performance, a minimum bound is approximately 2,100,000. With a MMIC mass of approximately 0.4 kg, and with available GEO launch costs, the launch expense alone is no less than 3.7 billion USD. In-space manufacture of electronics for PA, power converters, and rad-hard electronics enhances the economic attractiveness of in situ resource utilization (ISRU).

Current fabrication methods for power MOSFETs in SiC require at least one mask step for which alignment is critical. At the very short channel lengths desired, this requires large and complex lithographic operations, and such machines must be stably mounted on solid foundations immune to vibrations from adjacent footfalls, nearby heavy vehicles, and earthquakes. By comparison, a microgravity environment in orbit or in transit through space provides a very poor foundation for critical alignment. Gravity gradients, tides, and fluctuations flex a space vehicle, and if people are present, their natural movements make critical alignment very challenging. In this paper a fabrication sequence is presented for developing short-channel, high-mobility DMOSFET devices in SiC which can all be performed in a not-quite-stable microgravity environment. In addition, the chemicals used in the process are drawn from in situ resources as much as possible, and the recycling of effluents is used to minimize the need for resupply from earth. Of course the method can be used on earth as well, yet a key part of this innovation is the development of a pathway to complete independence from earth for some of the most sophisticated manufacturing challenges faced by a space-faring species. It also has the potential for favorable economics in the development of Space Solar Power (SSP).

FABRICATION SEQUENCE

Drawing from a now-expired patent modified for power devices, this doubly self-aligned device structure brings three benefits which are expected to significantly improve the experimental channel mobility of power DMOSFETs in SiC. As depicted in Fig. 2 a polysilicon sidewall spacer is formed by directional RIE etching of a conformal layer deposited over a previously-RIE etched layer of deposited silicon dioxide. The poly sidewall provides blocking for a N+ source implant. The poly is then is selectively removed to allow the slab of silicon dioxide to block for the P channel implant. The thickness of the poly layer determines the channel length, which can be in the deep submicron range (< 0.15 microns), requires no lithographic alignment, and can be highly uniform within a device and across a wafer. A silicon nitride layer in direct contact with the SiC substrate serves to protect the surface from re-arrangement and step formation during inert high temperature (1700 C) implant anneal/activation. The nitride layer also provides a small amount of surface N-type doping, creating a “retrograde” profile to the implanted P-region (reduces interactions with surface states). Next the nitride layer is partly removed isotropically in such a way that the oxide block is partially undercut, exposing some of the JFET region of the emerging DMOS structure. An

electrochemical etch of the naked SiC surface is used if needed to reduce step heights across a slightly off-axis (0001) surface [Zhuang, Neudeck]. Then, a gate oxide is grown (e.g. 1200 C in dry O_2) followed by a second layer of conformal polysilicon (deposited using recycled etch effluent), directionally etched to leave a sidewall gate directly over the channel. At suitable LPCVD conditions, initially of very low pressure, poly will deposit in the gap between the gate oxide and the oxide block formerly occupied by the nitride. This approach is an improvement over, but contains similarities to a process proposed in 2013 [Sun]. This novel approach will provide channel mobilities at a high fraction of the bulk, and still provides gate overlap of the JFET region in the corners where the current turns vertically downward towards the backside drain contact. All of this is achieved without a single critical mask-to-mask alignment so that devices are closely matched, and production yields are high, benefitting the design performance and production cost of high blocking voltage, low on-resistance, high-temperature power transistors.

Adapting IC fabrication to microgravity is facile for CVD deposition and plasma etch operations, where gases are readily transported to and from the active surface. Applying photoresist on earth begins with dispensing a large droplet onto a wafer held flat on a chuck. This may still be feasible in orbit if the droplet is sufficiently adherent that it remains on the wafer surface. Spray deposition of photoresist is another option. Sprayed-on resist layers will likely have worse thickness uniformity, which places greater demands on etch selectivity. Removal of spent photoresist with oxygen plasma is likewise straightforward.

There is one wet etch step, for removal and undercut of the silicon nitride layer, typically done with hot phosphoric acid mixed with hydrogen peroxide. This wet etch step is possible in microgravity, but will require a complex apparatus for handling the steam and other gaseous vapors generated. This etch must be selective against SiC which is exposed upon its removal, so the options for developing a plasma etch solution for this step (3rd cross section in Fig. 2) are limited.

Supplies of materials for processing are available in space. Lunar soil has a modest amount of phosphorus, abundant aluminum and silicon, but nearly zero carbon or halogens. On the other hand, carbonaceous chondrite asteroids have carbon compounds, silicates, water-bearing compounds, and small amounts of chlorine and fluorine (e.g. 40-61 ppm), mostly bound in minerals [10]. Effluent recycling is highly desired compared to the cost of either bringing or extracting halogens. Most compounds can be thermally decomposed. For example, hydrosilicic acid (HSiF6) decomposes below 200 C leaving Si metal and HF vapor behind.

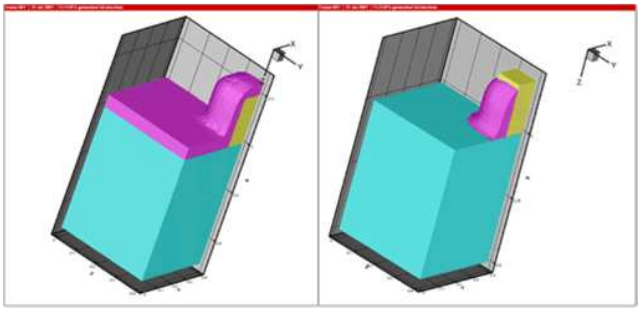

Figure 1. Sample output from FLOOPS/FLOODS for directional etching of conformal layers on pre-existing directionally-etched features.

DEVICE PERFORMANCE

With a 25 micron drift layer at $5x10^{14}/cm^3$ blocking voltage is expected to be at least 1700 V with suitable edge termination structure. With a 20 nm gate oxide (SiO_2) a threshold voltage of 3.0 V is expected [11]. Channel length is set by the polysilicon thickness and is nominally set at 150 nm. With channel mobility at 60 cm^2/Vs [12] switching speeds of 6.8 GHz are expected.

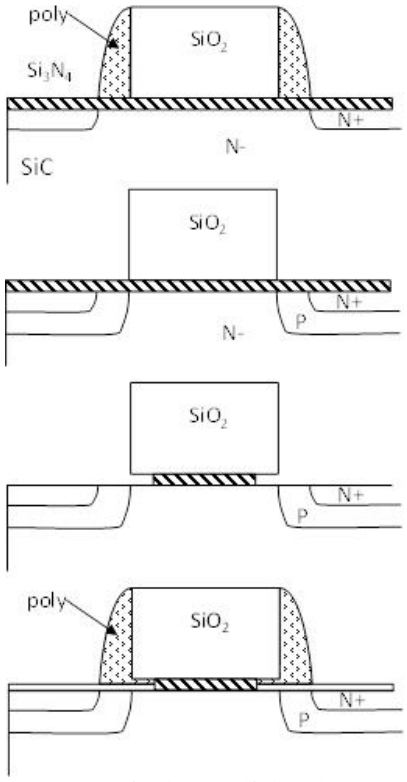

Figure 2. Process sequence for doubly self-aligned LDMOSFET gate and channel fabrication.

CONCLUSIONS

Presented here for the first time is a novel fabrication sequence ideally suited for in-space manufacture of radiation-hard, high temperature, power MOSFETS using mostly

materials already found in orbit. This capability opens up economic and technical capabilities for wireless power transfer for applications including commercial, industrial, and scientific.

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