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Insights into Tunnel FET-based charge-pumps and rectifiers for energy harvesting applications

David Cavalheiro, Francesc Moll and Stanimir Valtchev

***Abstract*— In this work the electrical characteristics of Tunnel FET (TFET) devices are explored for energy harvesting front-end circuits with ultra-low power consumption. Compared to conventional thermionic technologies the improved electrical characteristics of TFET devices are expected to increase the power conversion efficiency (PCE) of front-end charge-pumps and rectifiers powered at sub-µW power levels. Under reverse bias conditions the TFET device presents particular electrical characteristics due to the different carrier injection mechanism. A negative differential resistance (NDR) is observed at low reverse bias and high drift diffusion (DD) current is observed at high reverse bias, thus degrading the efficiency of low-power front-end circuits and limiting their operation range. Therefore, in order to take full advantage of the TFET electrical characteristics in front-end energy harvesting circuits, different circuit approaches are required. In this work we propose and discuss different topologies for TFET-based charge-pumps and rectifiers for energy harvesting applications.**

***Index Terms*—Charge-Pump, Energy Harvesting, Passive Rectifier, Thermogenerator, Tunnel FET, Ultra-Low Power.**

I. INTRODUCTION

THE emerging Tunnel Field-Effect Transistor (TFET) has been considered an attractive alternative to replace conventional CMOS technologies in ultra-low power and energy efficient computing applications [1-7]. In contrast to thermionic devices, the high energy filtering of the band-to-band tunneling (BTBT) carrier injection mechanism characterizes the TFET device with a sub-threshold slope (SS) below 60 mV/dec (at room temperature) and lower leakage current.

Simulation results show that TFET devices present better electrical characteristics than conventional technologies at sub-0.25 V operation [8]. On the other hand, TFETs conduct less current at voltages around 1 V, and thereby their use is envisioned for low voltage, low performance applications.

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As energy harvesting transducers produce low output voltage values from typical ambient conditions with small temperature gradients (case of thermogenerators) and low RF power (antennas powered by electromagnetic radiation), energy conversion circuits are required to increase these values for use by the electronic systems. Under extreme low voltage scenarios, TFETs appear as an interesting device to implement the required power conversion circuits. As an example, the work reported in [9] show improvements in the performance of TFET-based charge-pump converters compared to the application of the FinFET technology at sub-400 mV levels. In [10] we have shown that a gate cross-coupled charge-pump topology with TFETs powered by a thermogenerator presents a peak power conversion efficiency (PCE) of 74% for a temperature variation of 1 K (Vin=80 mV). In another work, the authors have shown similar PCE improvements in RF passive rectifiers based on TFETs for input power levels below -30 dBm (typical far-field ambient RF-power) [11]. These results are highly motivating for several applications where the power requirements of external batteries are still mandatory to ensure a proper circuit operation.

Despite the improvements shown in the circuit performance of the referenced works at low voltage (sub-0.4 V), the operation voltage range is limited by the particular TFET electrical characteristics when the device is reverse biased. In front-end circuits for energy harvesting applications as rectifiers (required by electromagnetic radiation) and up-converters (required by any low-voltage input source), the transistors can be subjected to both forward and reverse bias conditions (on and off-state respectively).

Under reverse bias conditions, the intrinsic *p-i-n* diode of the TFET is forward biased and the reverse current follows the characteristic of an Esaki Tunnel diode. When increasing the reverse bias magnitude of TFETs, a transition between a negative differential resistance (NDR) behavior and drift-diffusion (DD) mechanism characterizes the reverse current. As the magnitude of this reverse current can be controlled by the magnitude of the gate to source voltage, different circuit topologies are required in order to extend the voltage/power range operation of TFET-based circuits.

In this work, we propose changes in conventional charge-pumps and rectifier topologies for the application of TFETs with a focus on energy harvesting applications. These changes are characterized by attenuating the reverse current conducted by the TFETs when subjected to reverse bias conditions, thus increasing the rectification/conversion efficiency at a wider range of voltage/power operation. In section II we make a short review of the TFET structure, carrier injection

mechanisms and the main electrical characteristics of the device. In section III and IV we explore the performance of TFET devices in DC-DC converters and AC-DC passive rectifiers respectively. New topologies are proposed to minimize the reverse losses suffered by conventional circuits when the TFET is under reverse bias conditions. Finally, section V presents the conclusions of the work.

II. The Tunnel FET Device

A. Physical characteristics and BTBT

Unlike conventional MOSFET devices, the TFET is designed as a reverse biased *p-i-n* diode [1-2]. For an n-type TFET, the p-type source presents a higher doping concentration than that of the n-type drain as shown in Fig. 1 (a) top. Under forward bias conditions, the drain is at a higher potential than that of the source. In contrast, the p-type TFET is characterized by an n-type source with a higher doping concentration than that of the p-type drain as shown in Fig. 1 (a) bottom. Under forward bias conditions, the drain of the p-TFET is at a lower potential than that of the source.

In TFET devices, the carrier injection mechanism does not follow the laws of thermionic injection as in conventional MOSFETs. In Fig. 1 (b), the energy band diagram for an n-TFET shows the Fermi level in the source region below the energy valence band, and above the energy conduction band in the drain region. During the off-state condition, i.e. V_{GS} = 0 V both Fermi levels in the source and channel regions are aligned (dashed blue curves).

When V_{GS} = 0 V, electrons below the Fermi level on the source region see a large channel resistance to tunnel through the channel until the drain side. This channel resistance sets the leakage current of the Tunnel FET device.

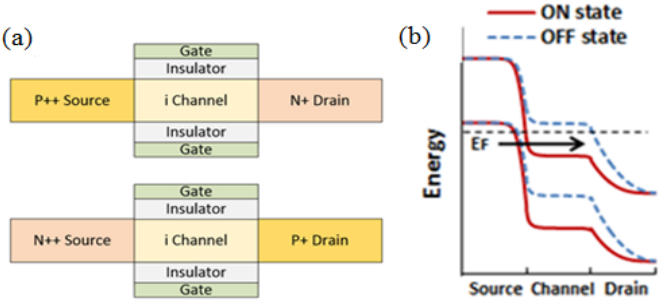

Fig. 1. (a) Double-gate Tunnel FET structure and (b) BTBT mechanism

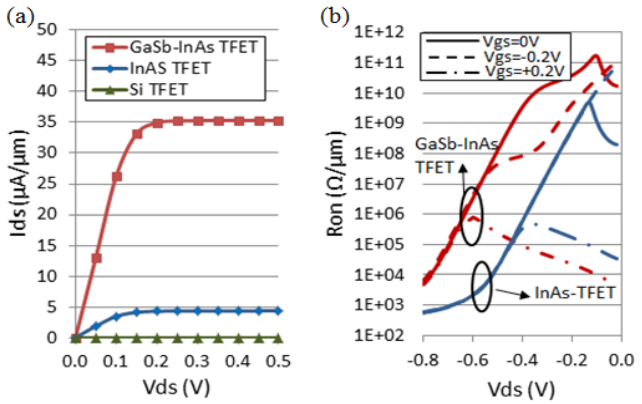

Fig. 2 (a) Current-Voltage characteristic of TFETs for different materials, (b) Internal resistance under reverse biasing

When a positive gate bias is applied, the energy levels in the channel bend down and the Fermi level in the channel region moves below the Fermi level of the source region (solid red curves). In this case, there is an increase of probability of electrons in the source region to tunnel through the channel to the empty states of the drain region.

During the on-state condition of Fig. 1 (b), the decrease of the energy barrier between the source and the channel sets the tunneling mechanism at the source-channel interface. As the band-to-band tunneling (BTBT) carrier mechanism does not follow the thermal laws of conventional transistors, a sub-60 mV/dec of sub-threshold slope (SS) in the I-V characteristics (at ambient temperature) is possible. In a p-type TFET, when a negative bias is applied to both channel and drain regions (respective to the source), the energy levels bend up, increasing the probability of holes in the source region to tunnel to the empty states of the drain region. Similar to the n-type, the BTBT in p-TFETs is set at the source-channel interface (not shown for simplicity).

In TFETs, the magnitude of current is dependent on the device materials. As shown in Fig. 2 (a), TFETs designed with lower energy band gap and mass materials than silicon allow for higher on-current values. In comparison with silicon-based TFETs, the use of III-V materials as InAs and GaSb decrease the tunneling barrier at the source-channel interface allowing for a higher tunneling probability and a consequent reduction of channel-resistance [1]. In comparison with an homojunction InAs TFET, the higher drive current of the heterojunction GaSb-InAs TFET comes from the reduction in the effective tunneling barrier at the source-channel junction without reducing the energy band-gap of the channel material [5].

The homojunction TFET is characterized by InAs material in both drain, channel and source with a gate length of 20 nm. The heterojunction TFET presents a GaSb source and a InAs channel and drain with a gate length of 40 nm. More information about these two devices can be found in [12]. The Silicon TFET is simulated with a gate length of 20 nm.

B. Carrier injection mechanism under reverse bias conditions

Under reverse bias conditions (negative V_{DS} for n-type and positive V_{DS} for p-type TFET), the intrinsic *p-i-n* diode of the TFET is forward biased and the resulting reverse current is characterized by two different carrier injection mechanisms. For an n-type TFET, a low reverse bias condition (V_{DS} < 0 V) results in a reverse current characterized by a reverse BTBT carrier mechanism occurring at the channel-drain interface as shown in Fig. 3 (a). As long as reverse bias increases (V_{DS} << 0 V) the BTBT mechanism is suppressed due to the increase of energy bands in the drain region, and the drift-diffusion (DD) mechanism characterizes the current as shown in Fig. 3 (b).

In Fig. 2 (b), simulations show that when both homojunction and heterojunction n-TFETs are reverse biased (V_{DS} < 0 V) with a positive V_{GS}, a negative differential resistance (NDR) is observed. This behavior is due to the transition between reverse BTBT and DD mechanism with the decrease of V_{DS}.

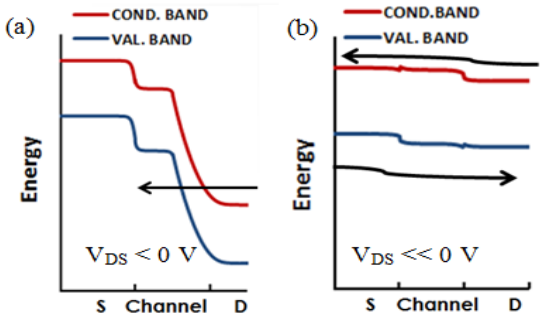

Fig. 3. TFET energy band diagram of an n-TFET under reverse bias conditions: (a) reverse BTBT mechanism, (b) drift-diffusion mechanism.

It is also shown that the heterojunction TFET (source with a higher energy band gap material than that of the channel and drain) presents a reverse current lower than that of the homojunction InAs TFET. This electrical behavior characterizes the heterojunction TFET as a better switching device in comparison with the homojunction InAs due to the respectively lower and higher internal resistance under forward and reverse bias conditions.

When a negative V_{GS} is applied to a reverse biased TFET, the NDR behavior is not observed and the DD mechanism characterizes the current at large reverse V_{DS}. However, it is shown that for a reverse biased heterojunction TFET, a V_{GS}=0 V can reduce the reverse current for a significant range of V_{DS} (-0.1 V to -0.6 V). This behavior is not observed for the homojunction InAs TFET.

The two particular carrier injection mechanisms of TFETs under reverse bias conditions are expected to deteriorate the performance of front-end circuits for energy harvesting applications. As the transistors applied in conventional charge-pumps and rectifier circuits are characterized by both forward (on-state) and reverse (off-state) bias conditions it is of the major importance to mitigate the reverse current conducted by TFETs during their off-state operation. In this work we focus our simulations and results on the application of the heterojunction TFET device due to its better switching performance at low voltage in comparison with the homojunction counterpart.

C. Tunnel FET intrinsic capacitance

In TFET devices, the intrinsic gate-to-source and gate-to-drain capacitances present a different behavior in function of the gate bias compared to conventional MOSFET devices. As shown in Fig. 4 (a), the total gate capacitance of the heterojunction TFET is dominated by C_{GD}. As the TFET current is dependent on the barrier shrinking in the source-channel interface, the resulting C_{GS} is shown much lower than C_{GD} when the transistor is active [13, 14], Fig. 4 (b).

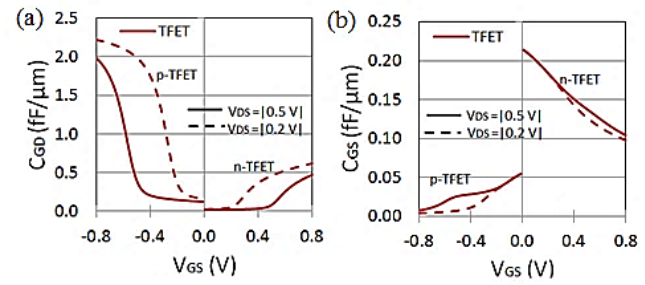

Fig. 4 (a) Gate-to-drain and (b) gate-to-source intrinsic capacitance of TFET.

The lower gate-capacitance of TFETs in comparison with Si MOSFETs can reduce the dynamic power consumption and delays of digital circuits as shown in [15]. In digital logic, the uni-directional conduction of TFET devices and the enhanced Miller capacitance can result in bootstrapped nodes within the circuit, causing potential failures and reliability risks [15, 16]. In conventional MOSFETs, charges can be transferred under both positive and negative V_{DS} bias due to a similar doping structure in the source and drain junctions. In contrast, a reverse biased TFET has low conduction and cannot quickly dissipate the charge. This characteristic can result in switching nodes with transient "spikes", with voltage values above the power supply voltage and below ground. For TFET-based charge-pumps and rectifier, this behavior can induce an increased switching power as referred in [11].

In [13], the authors have shown that in comparison with Si-based TFETs, the design of TFETs with III-V materials (low bandgap and low mass) can mitigate the Miller capacitance effect due to the reduced density of states (DOS) of such materials. Therefore, TFETs designed with III-V materials are advantageous in comparison with Silicon devices for ultra-low power applications focused on energy-harvesting.

In the following sections, the performance of the heterojunction GaSb-InAs TFET in charge-pumps and rectifiers is explored, with circuit solutions that mitigate the reverse losses suffered by the transistors operating during their off-state (reverse-biased).

III. TFET-BASED CHARGE-PUMPS

In this section, the behavior of the TFET at a device-level is simulated with a Verilog-A model using look-up tables describing the main electrical characteristics. Both current-voltage (I-V) and capacitance-voltage (C-V) characteristics were obtained from the TCAD Sentaurus device simulator by the NDCL group at PSU [6-7, 12]. The Verilog-A model describes the behavior of a 40 nm double gate GaSb-InAs TFET device calibrated through full-band atomistic simulations with a dynamic non-local band-to-band tunneling model. The drain doping concentration of the n-TFET is presented as $N_D = 2 \times 10^{17} cm^{-3}$, the source doping concentration as $N_A = 4 \times 10^{19} cm^{-3}$, the thickness of the channel as $T_{CH} = 5\ nm$ and the thickness of the High K oxide as $T_{OX} = 2.5\ nm\ (HfO_2)$. The current-voltage characteristics of the p-TFET are assumed to be the same (in magnitude) as the n-TFET type. The C-V characteristics of both n-TFET and p-TFET devices are different.

A. State-of-the-art TFET-based Charge-pumps

As mentioned in section II B, in TFET devices the increase of the reverse current conduction with the increase of reverse bias is expected to degrade the conversion efficiency of charge-pumps and therefore, solutions are required to increase both the voltage/power operation range. In order to understand the limitations of TFETs in conventional charge-pump topologies, one can consider the gate cross-coupled charge-pump (GCCCP) presented in Fig. 5 (a). With conventional MOSFET devices, this charge-pump was shown to present better conversion performance at low input voltage values compared to other converter topologies [17].

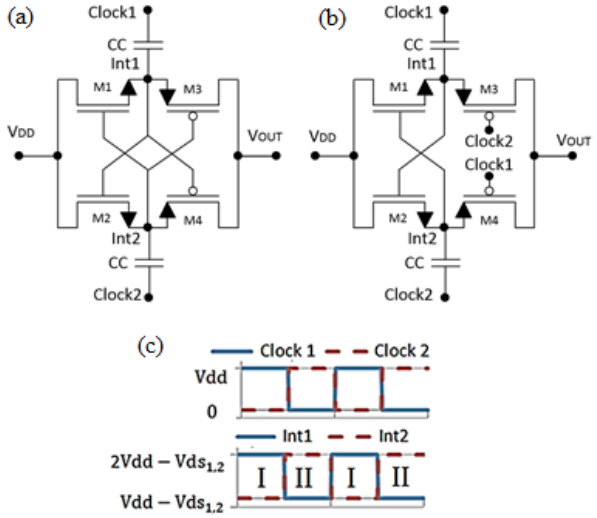

Fig. 5. (a) Gate Cross-Coupled Charge-Pump topology, (b) State-of-the-art TFET-based CP and (c) Regions of operation

The principle of operation of the GCCCP converter can be divided into two regions of operation as shown in Fig. 5 (c). In region I, the low to high transition of Clock 1 increases the voltage node "Int1" to $2V_{DD}$-V_{DS2}. During the same time, the voltage node of "Int2" is reduced to V_{DD}-V_{DS2}. In this region, transistors M1 and M4 are reverse biased (off-state) and transistors M2 and M3 forward biased (on-state). The bias characteristics in this region when considering steady state conditions are presented in Table I:

TABLE I BIAS CONDITIONS OF THE GCC CONVERTER IN REGION I

Reg. I	State	Vgs	Vds
M1 (n)	Off	Int2 - Int1 = -V_{DD}	V_{DD} - Int1 = - V_{DD} + Vds1
M2 (n)	On	Int1 - Int2 = V_{DD}	V_{DD} - Int2 = Vds2
M3 (p)	On	Int2 - Int1= - V_{DD}	Vout - Int1 = - Vsd3
M4 (p)	Off	Int1 - Int2 = V_{DD}	Vout - Int2 = V_{DD} - Vsd3

During the second region of operation, the high to low (low to high) transition of Clock 1 (Clock 2) and consequent reduction (increase) of voltage in node "int1" (int2) results in a forward bias condition of transistors M1 and M4 and reverse bias in M2 and M3. The bias conditions of the transistors are presented in Table II:

TABLE II BIAS CONDITIONS OF THE GCC CONVERTER IN REGION II

Reg. II	State	Vgs	Vds
M1 (n)	On	Int2 - Int1 = V_{DD}	V_{DD} - Int1 = Vds1
M2 (n)	Off	Int1 - Int2 = - V_{DD}	V_{DD} - Int2 = - V_{DD} + Vds2
M3 (p)	Off	Int2 - Int1= V_{DD}	Vout - Int1 = V_{DD} – Vsd4
M4 (p)	On	Int1 - Int2 = - V_{DD}	Vout - Int2 = - Vsd3

According to Tables I and II, and considering no forward losses in the transistors, the reverse bias condition of the transistors (off-state) is always characterized by a V_{GS}=V_{DS}. In Fig. 6, the electrical characteristics of the heterojunction TFET device biased according to Tables I and II is presented.

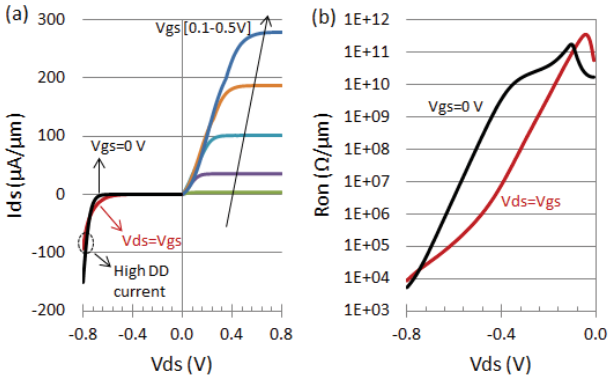

Fig. 6. Output characteristics of the Heterojunction n-TFET device applied in the gate cross-coupled charge-pump

As shown in Fig. 6 (a), when the heterojunction TFET is reverse biased with a $|V_{DS}| > 0.7$ V, the conduction of large reverse current is independent on the magnitude of gate to source voltage. In contrast, under a low bias condition of $|V_{DS}| < 0.7$ V, the reverse current can be attenuated if the V_{GS} of the reverse biased transistors is forced to be 0 V as shown by the increase of the device internal resistance in Fig. 6 (b). These characteristics constrain the use of heterojunction TFETs in charge-pumps for low voltage operation: if the magnitude of voltage between the drain and source junction of the TFET is higher than 0.7 V, the conducted reverse current is expected to degrade the power conversion efficiency (PCE) of the charge-pump. For lower voltage operation, modifications in the conventional GCCCP topology can improve the PCE by changing the magnitude of the gate to source voltage of the reverse biased TFETs.

In [9], the authors proposed a change in the topology of the conventional GCCCP that redirects the gate control signals of the two p-type transistors to the bottom of the two coupling capacitors as shown in Fig. 5 (b). This solution forces the V_{GS} of M3 and M4 to respectively V_{DS1} and V_{DS2} (approx. 0 V when considering low output current) when the transistors are reverse biased. However, the higher the required current, the higher are the resultant V_{DS1} and V_{DS2} and consequently the reverse losses. Furthermore, the reverse current conduction of M1 and M2 (under reverse bias conditions) is not attenuated and a different topology is mandatory.

B. Proposed TFET-based charge-pump

At a circuit level, a possible solution to attenuate the reverse current of TFETs operating during their off-state (reverse biased) is to set their gate to source voltage V_{GS} to 0 V. To perform this behavior, auxiliary transistors and capacitors can be used as shown in Fig. 7.

Considering as an example the n-TFET M1, the auxiliary transistor (M_{aux}) will fix the node V3 with a value equal to the highest voltage value of nodes V1 and V2. With this solution, the V_{GS} of the n-TFET will present a value close to 0 V (neglecting the forward losses of the auxiliary transistor) under reverse bias conditions and a positive value when the transistor is forward biased. A similar solution is proposed for p-TFET devices. In this case, an inverter circuit fixes the voltage at node V3 with a value equal to the lowest voltage of the clock signal.

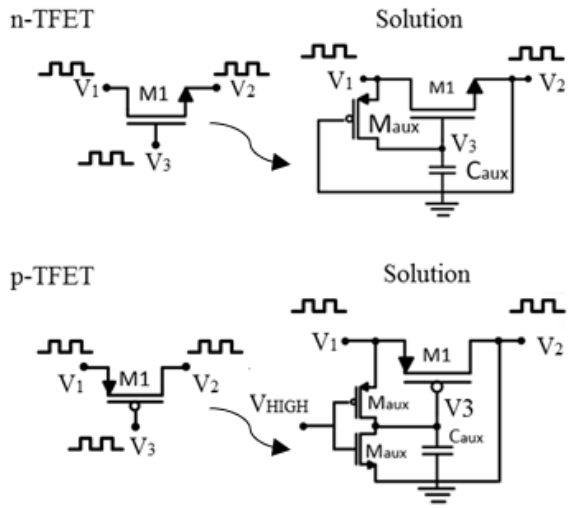

Fig. 7. Transistors in the gate cross-coupled charge-pump topology and solutions to decrease the reverse current conduction

In Fig. 8, a proposed TFET-based charge-pump for low voltage operation is presented. The gates of the main TFET transistors M1 and M2 are connected and biased with an auxiliary transistor $M1_{aux}$ and capacitor $C1_{aux}$ while the gates of the main transistors M3 and M4 are biased by an auxiliary inverter ($M2_{aux}$ and $M3_{aux}$) and capacitor $C2_{aux}$.

To highlight the advantage of using TFET devices for energy harvesting applications, the characteristics of a commercial ultra-low thin-film thermo-generator, in particular the MPG-D655 from Micropelt [18] are used to simulate the input power supply voltage of the proposed TFET-based charge-pump. As presented in Fig. 9, the thermo-generator presents a Seebeck coefficient of 80 mV/ K.

In Fig. 10, a performance comparison between the proposed, the conventional and the state-of-the-art TFET-based charge-pump topologies is presented. For the simulations, two different variations of temperature in the thermogenerator are considered: ΔK=2 K (V_{DD}=180 mV) and ΔK=6 K (V_{DD}=480 mV). The width of the main III-V heterojunction TFET transistors M1-M4 are set as 1 µm, the auxiliary transistors as 100 nm, auxiliary capacitors present a capacitance of 0.1 pF, coupling capacitors CC as 1 pF and the output capacitor as 10 pF. The clock signals in nodes CK1 and CK2 are simulated with a frequency of 100 MHz.

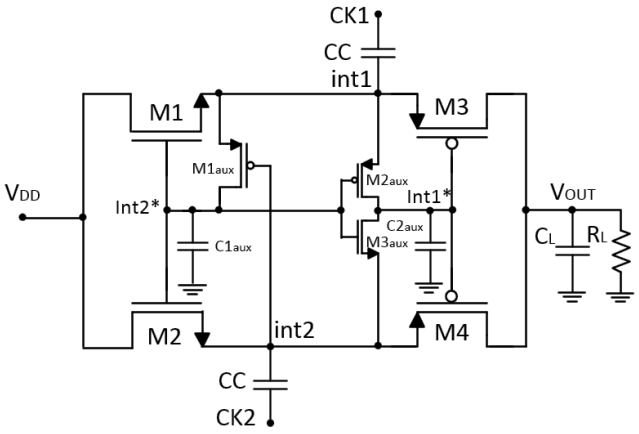

Fig. 8. Proposed TFET-based charge-pump.

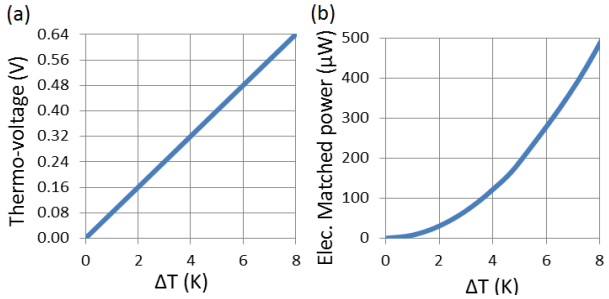

Fig. 9 Electrical characteristics of the MPG-D655, U=80mV/K (Tamb=25ºC). Rth=22 K/w, Relec=210Ω.

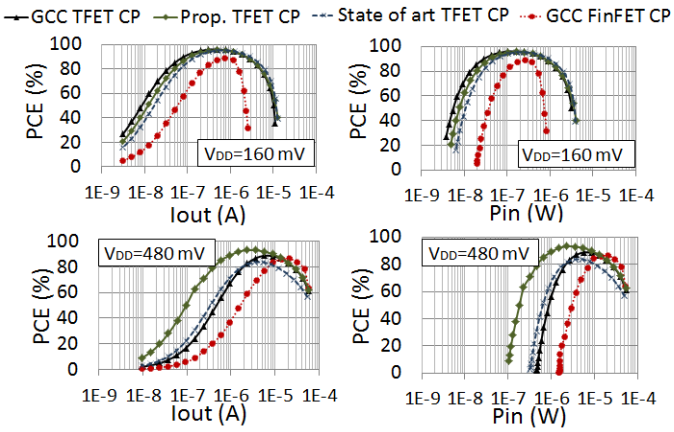

Fig. 10. Performance comparison between a GCC FinFET charge-pump and the proposed, state of-the-art and conventional GCC TFET charge-pumps.

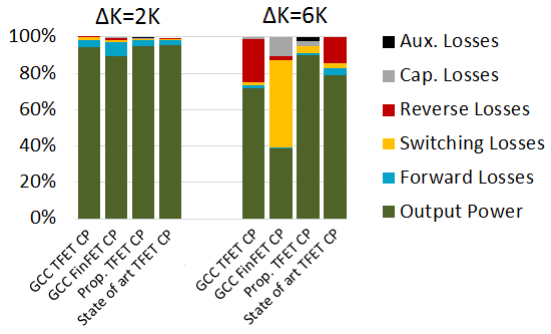

Fig. 11 Distribution of power losses for Iout=1µA considering V_{DD}=160mV (ΔK=2K) and V_{DD}=480mV (ΔK=6K)

For comparison purposes, the performance of a FinFET-based GCCCP is simulated and compared with the three TFET-based charge-pump topologies. The FinFET-based charge-pump is simulated with models describing a triple-gate FinFET with a gate-length of 20 nm, fin height of 28 nm and a fin width of 15 nm. The characteristics are based on a predictive technology model (PTM) from the NIMO group at ASU [19]. The power conversion efficiency of each charge-pump stage is calculated as (1):

$$PCE = \frac{P_{OUT,DC}}{P_{IN,DC}} = \frac{V_{OUT,DC} I_{OUT,DC}}{V_{IN,DC} I_{IN,DC}} \quad (1)$$

$$P_{losses} = P_{reverse} + P_{conduction} + P_{switching} \quad (2)$$

In order to increase the PCE of the charge-pump stage the power losses have to be as small as possible. In (2) the average power losses in a charge pump stage can be divided into three main sources: reverse, conduction and switching power. The first power loss is characterized by the current that flows from

the output to the input of the stage due to the non-fully closed transistors. With the different electrical characteristics of TFETs under reverse biasing conditions, this source of losses is important at large input voltage values. Conduction losses exist due to a non-zero channel resistance in the transistors working under forward bias conditions. For a specific transistor channel width, larger conduction of current results in larger forward voltage drop and consequently larger conduction losses. A possible solution to attenuate the conduction losses is the increase of the transistor width. However, larger transistor sizes results in larger parasitic capacitances and therefore larger switching losses.

For the two variations of temperature considered, one can observe that both TFET-based charge-pumps present a better performance than that of the FinFET counterpart. For a low input voltage V_{DD}=160 mV (ΔK=2 K), the proposed charge-pump presents a small degradation of efficiency for output current levels in the nA range due to the power consumption of the auxiliary circuitry. However, when the input voltage is increased to 480 mV (ΔK=6 K), the reverse biased transistors in both conventional and state-of-the-art TFET-based charge-pumps degrades the efficiency with conduction of high reverse current. In contrast, the proposed charge-pump is shown to be more efficient at a wider range of operation.

In Fig. 11, the power loss distribution for an output load of 1 μA is presented. For a ΔT=2 K, both TFET-based charge-pumps presents lower forward losses than the FinFET counterpart. This result is directly related to the possibility of heterojunction TFETs to conduct more current at sub-0.25 V. For a ΔT=6 K, one can observe that most of the losses of the FinFET CP are due to switching losses. At this load point, and despite the losses resultant from the auxiliary circuitry, the proposed charge-pump shows respectively a 240x and 130x reduction in the reverse current compared to the conventional and state of the art TFET-based charge-pumps.

IV. TFET-BASED RECTIFIERS

This section focuses on the proposal of new TFET-based rectifiers for RF energy harvesting that alleviates the losses suffered by the TFET transistors when subjected to reverse bias conditions. The heterojunction TFET and silicon FinFET models applied in the simulations of this section are the same than those presented in section III.

A. State-of-the-art TFET-based rectifier

In radio-frequency (RF) powered energy harvesting systems, the demonstrated low efficiency at sub-μW (sub -30 dBm) RF power levels is mainly related to the difficulty of conventional devices to present a good switching performance at very low voltage levels (sub-0.25 V). In [11] the authors have shown by simulations that the inclusion of TFET devices in passive rectifiers can improve the efficiency at such low power levels compared to similar rectifiers designed with FinFET technology. The TFET-based gate cross-coupled rectifier (GCCR) presented in Fig. 12 (a) was shown by the authors to present a better performance at a wider range of voltage/power operation in comparison to other rectifier topologies (PCE > 50 % with an RF input power ranging from -40 dBm to -25 dBm).

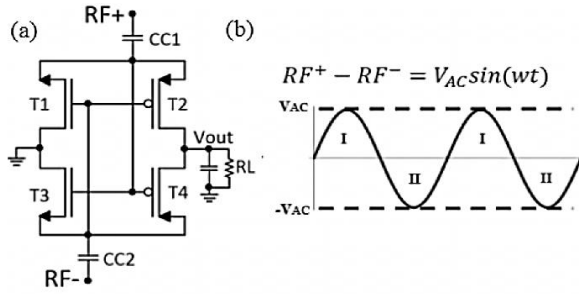

Fig. 12. (a) Conventional GCC Passive rectifier and (b) its two different regions of operation.

TABLE III STEADY-STATE BIAS CONDITIONS OF THE GCCR IN REGION I

Region I	State	VGS	VDS
T1 (n)	Off	$RF^- - RF^+ < 0$	$-RF^+ < 0$
T2 (p)	On	$RF^- - RF^+ < 0$	$Vout - RF^+ < 0$
T3 (n)	On	$RF^+ - RF^- > 0$	$-RF^- > 0$
T4 (p)	Off	$RF^+ - RF^- > 0$	$Vout - RF^- > 0$

TABLE IV. STEADY-STATE BIAS CONDITIONS OF THE GCCR IN REGION II

Region II	State	VGS	VDS
T1 (n)	On	$RF^- - RF^+ > 0$	$-RF^+ > 0$
T2 (p)	Off	$RF^- - RF^+ > 0$	$Vout - RF^+ > 0$
T3 (n)	Off	$RF^+ - RF^- < 0$	$-RF^- < 0$
T4 (p)	On	$RF^+ - RF^- < 0$	$Vout - RF^- < 0$

However, in a TFET-based GCCR the range of voltage/power operation demonstrated by the authors is degraded due to the losses presented by the TFET transistors during theirs off-state operation (reverse biased state). Therefore, a different TFET-based rectifier topology is required in order to improve the conversion performance at a wider range of operation

The operation of the conventional GCCR can be divided into two regions as shown in Fig. 12 (b): region I where the RF+ node is at a higher voltage than that of the RF- node and region II when the reverse behavior is observed. During the first region of operation, both T1 and T4 transistors are reverse biased, thus conducting reverse current to the circuit. In the second region of operation, transistors T2 and T3 present the same problem. The V_{GS} values of each transistor during the off-state operation are presented in Tables III and IV. In Fig. 13, a performance comparison of the TFET-based GCCR for two distinct frequencies (100 MHz and 915 MHz) and loads (RL=100 kΩ and RL=10 kΩ) is presented:

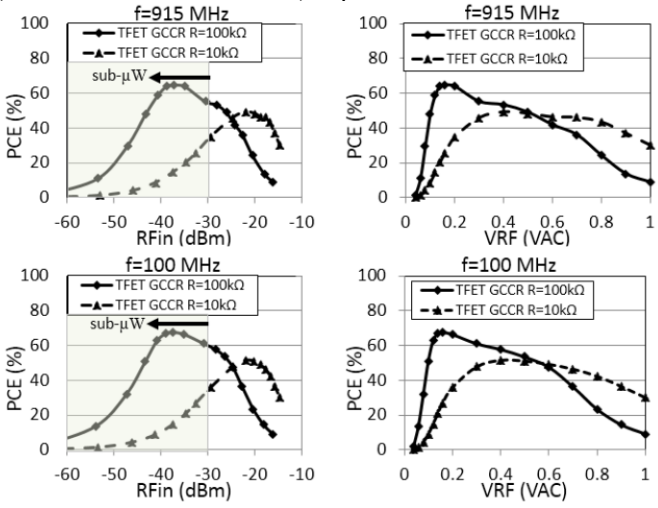

Fig. 13 Performance comparison of a TFET-based GCCR

The main four TFET devices T1 to T4 are simulated with channel widths of 1 µm. The output capacitor CL and the two coupling capacitors CC1 and CC2 presents the same capacitance value of 1 pF. The power efficiency of the rectifier stage is calculated as (3):

$$PCE = \frac{P_{OUT,DC}}{P_{IN,RF}} = \frac{V_{OUT,DC} I_{OUT,DC}}{\frac{1}{T}\int_0^T V_{AC}\sin(wt) I_{AC}(t)} \quad (3)$$

Similar to the charge-pump topology, the reverse, conduction and switching power are presented as the main losses in the rectification process.

As shown in Fig. 13 and in comparison with 10 kΩ, a load of 100 kΩ can enable higher power conversion efficiency (PCE) at sub-µW power levels and for both frequencies in study. The peak efficiency for this load is shown to be around a RF VAC 0.2 V. At higher voltage values, the decrease of the PCE is not only due to the increase of conduction losses by the transistors operating during their on-state but also due to non-fully closed transistors operating during their off-state, and consequent conduction of reverse current. As previously mentioned, a solution to decrease the reverse losses is to set the V_{GS} of the reverse biased TFET devices to 0 V.

B. Proposed TFET-based rectifier

In Fig. 14 a TFET-based rectifier topology is proposed. The aim of the proposed solution is to bias the gate of the main transistors T1 and T3 with the positive arcade of the RF^+-RF^- signal applied to the terminals of the rectifier, and transistors T2 and T4 with the negative arcade. In order to accomplish this solution, the gates of transistors T1 and T3 are connected together, as also the gates of T2 and T4. Two auxiliary TFET devices (T5 and T6) are required to bias the gates of T1 and T3 and two auxiliary transistors (T7 and T8) to bias the gates of T2 and T4. According to Table V when the main transistors are reverse biased (signaled in bold) their gate to source voltage V_{GS} will present a value close to 0 V (voltage drop of aux. transistors T5 to T8 is non-zero) and a similar V_{GS} value than those presented in the conventional GCCR for the transistors operating during their on-state.

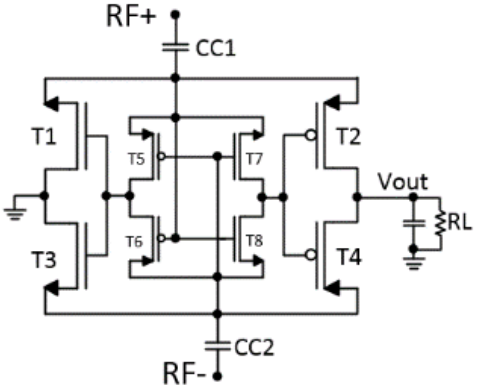

Fig. 14 Proposed TFET-based rectifier

TABLE V VGS CONDITIONS OF THE PROPOSED RECTIFIER IN BOTH REGIONS OF OPERATION (BOLD: TRANSISTORS IN OFF-STATE)

	VGS Region I	VGS Region II
T1 (n)	$(\mathbf{RF^+ - V_{SD5}}) - \mathbf{RF^+} < \mathbf{0}$	$(RF^- - V_{SD6}) - RF^+ > 0$
T2 (p)	$(RF^- - V_{SD8}) - RF^+ < 0$	$(\mathbf{RF^+ - V_{SD7}}) - \mathbf{RF^+} > \mathbf{0}$
T3 (n)	$(RF^+ - V_{SD5}) - RF^- > 0$	$(\mathbf{RF^- - V_{SD6}}) - \mathbf{RF^-} < \mathbf{0}$
T4 (p)	$(\mathbf{RF^- - V_{SD8}}) - \mathbf{RF^-} > \mathbf{0}$	$(RF^+ - V_{SD7}) - RF^- < 0$

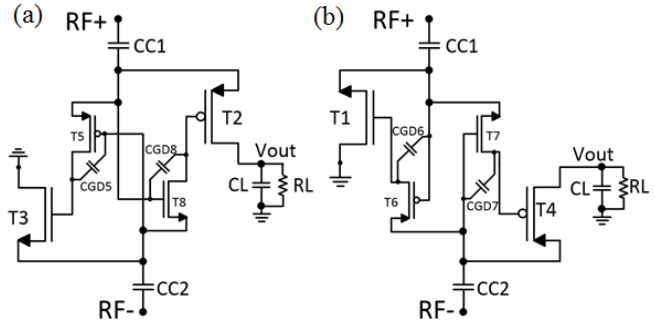

Fig. 15 Active transistors in (a) first and (b) second regions of operation

During the first region of operation shown in Fig. 15 (a) ($RF^+ > RF^-$) the main transistors T2, T3 and the auxiliary transistors T5 and T8 are active (T1, T4, T6 and T7 operate in off-state), while the second region of operation shown in Fig. 15 (b) ($RF^+ < RF^-$) characterizes T1, T4, T6 and T7 in on-state (T2, T3, T5 and T8 in off-state). In the proposed topology, the auxiliary transistors operating during their off-state condition present a non-zero magnitude of V_{GS} and therefore reverse current in these transistors is expected. In order to mitigate the consequent reverse losses and improve the PCE of the rectifier stage one can decrease the size of the auxiliary transistors in comparison with the main transistors.

As shown in Fig. 16, the increase of ratio between the main and auxiliary transistor widths is an effective way to increase the PCE at RF VAC values higher than 0.6 V. Despite the increased performance of the proposed TFET rectifier in comparison with the TFET-based GCCR at such values, there is a clear decrease of PCE for RF VAC values in the range of 0.1 V to 0.6 V. This behavior is explained by the enhanced gate-do-drain capacitance (C_{GD}) of the auxiliary TFET devices operating in the on-state (see Fig. 15). As shown in Fig. 17 (a), for a frequency of 915 MHz the parasitic C_{GD} cause delays between the voltage applied at the source and gates of the reverse biased main transistors, thus resulting a non-zero V_{GS}.

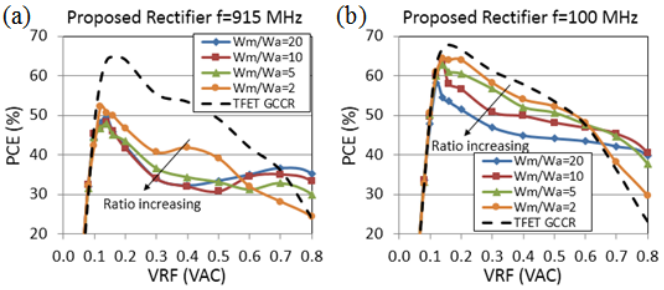

Fig. 16 Power conversion efficiency dependence on the ratio between the main and auxiliary transistors width for (a) f=915 MHz and (b) f=100MHz

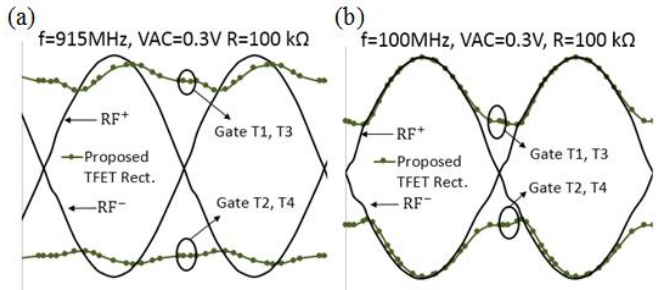

Fig. 17 Gate voltage applied to the main transistors T1 to T4 in the proposed rectifier for: a) f=915MHz, b) f=100MHz

In contrast, for a frequency of 100 MHz the gate values of T1 and T3 (T2, T4) are phased with the positive (negative) arcades of the applied RF voltage signals to the rectifier. As shown in Fig. 16 (b), a lower frequency operation of 100 MHz results in increased efficiency values in the RF VAC range of 0.1 V to 0.6 V when compared to an operating frequency of 915 MHz. Larger auxiliary transistor sizes can mitigate the delays by fasten the charge and discharge rate of the parasitic gate-to-drain capacitances (when forward biased), with a consequent increase of the reverse losses when subjected to reverse bias conditions.

C. A Hybrid TFET-FinFET rectifier

In order to improve the efficiency of TFET-based rectifiers in a wider range of operation, one can consider a hybrid rectifier with both TFETs and Silicon-based FinFETs. Considering the proposed TFET rectifier of section IV B., one can maintain the four main TFETs and replace the auxiliary transistors by FinFETs. As the intrinsic gate-to-drain capacitance of MOSFETs is presented as a small part of the total gate capacitance [14], lower delays are expected between the gate and source voltage signals applied in the main TFETs. This characteristic allows for the increase of power efficiency at low RF VAC values (sub-0.6V) maintaining the higher efficiency at higher RF voltage values when compared to the conventional TFET GCCR.

In Fig. 18 a comparison between three TFET-based rectifier topologies and a FinFET-based GCCR is presented. The TFET-based GCCR is simulated with TFET widths of 1 um, the FinFET-based rectifier present four FinFETs with 14 fins (equivalent to a channel width of 994 nm), the proposed TFET-based rectifier with a ratio of 10 between the main and auxiliary transistors and the hybrid rectifier with the main TFET devices with 1 µm and auxiliary FinFETs with 2 fins each (equivalent to a channel width of 142 nm).

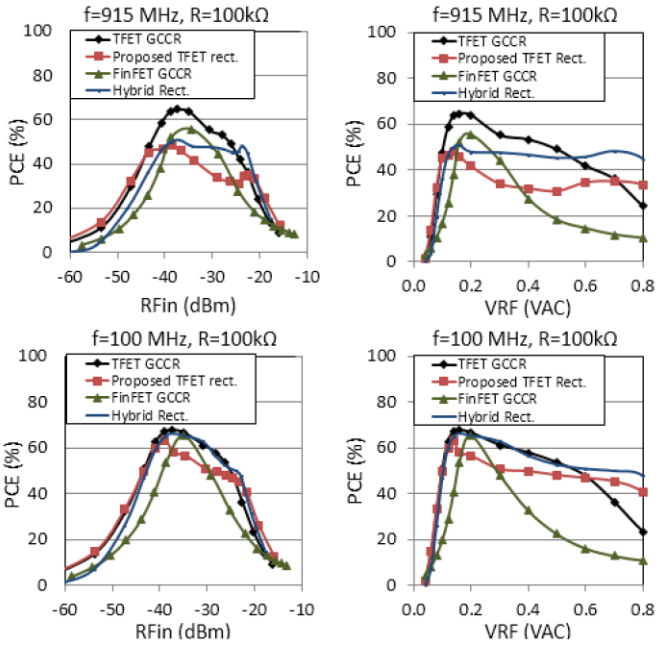

Fig. 18 Performance comparison of rectifiers considering different loads (10 kΩ and 100 kΩ) and frequency of operation (915 MHz and 100 MHz)

The results show that for both frequencies of operation the FinFET-based rectifier presents a competitive power efficiency in the short range of RF input power of -30 dBm to -40 dBm. For a frequency of 100 MHz, the hybrid rectifier presents the highest PCE values at a wider range of voltage/power operation when compared to the conventional GCCR and proposed TFET-rectifier. At a higher frequency of 915 MHz, the PCE of the hybrid configuration is shown lower than that of the conventional GCCR at a sub -35 dBm.

In Fig. 19, it is shown that despite the lower efficiency values at RF VAC values above 0.3 V, the FinFET-based GCCR presents the highest output voltage values. This characteristic is explained due to the higher current conducted by FinFETs at voltage values above 0.25 V when compared to heterojunction Tunnel FETs [15].

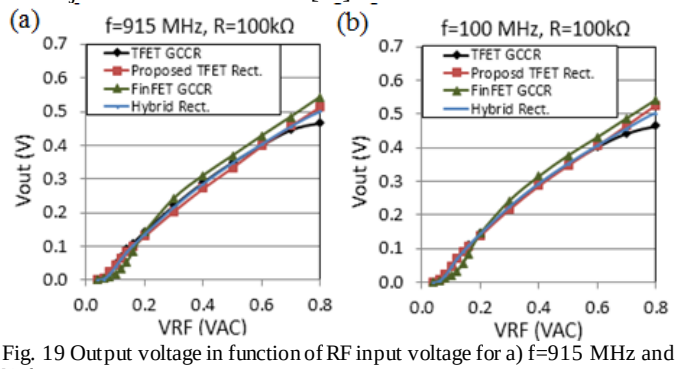

Fig. 19 Output voltage in function of RF input voltage for a) f=915 MHz and b) f=100MHz

V. CONCLUSIONS

In this work, the TFET device is explored as an alternative technology for front-end energy harvesting circuits as charge-pumps and rectifiers. Due to the intrinsic *p-i-n* structure, TFET devices present particular electrical characteristics under reverse bias conditions that limit the operation voltage/power of circuits due to the consequent reverse losses. Therefore, different circuit approaches are required in order to attenuate the reverse current conducted by TFET devices when operating during their off-state condition, i.e. when the intrinsic *p-i-n* diode is forward biased.

A comparison between a proposed TFET-based charge pump and the conventional topology shows improved performance at a wider range of voltage/power operation range. Similar performance improvements were shown for the proposed TFET-based rectifier at RF VAC values above 0.6 V when compared to the conventional gate-cross coupled topology. At a frequency of 915 MHz, the large gate-to-drain capacitance of TFETs in the proposed rectifier topology degrade the efficiency performance at sub-0.6 V operation. A hybrid TFET-FinFET rectifier can alleviate these losses, maintaining the good efficiency performance at RF VAC values above 0.6 V.

In summary, the performance of the heterojunction TFET in study with III-V materials is presented as an interesting alternative to replace conventional transistors in ultra-low power energy harvesting front-end circuits. With this technology, front-end circuits can operate efficiently at power supply voltage levels close to those produced by several energy harvesting sources as thermogenerators powered by

low temperature gradients and antennas with low output voltage values due to low RF electromagnetic radiation.

There are, however, many challenges to fabricate TFETs with the performance described in this work. The requirement of high quality III-V materials and oxides with high-k to remove effects as trap-assisted tunneling and the fabrication of ultra-thin body dimensions for a good gate electrostatic control are some examples of problems experienced by several groups.

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