Improved thermal isolation of silicon suspended platforms for an all-silicon thermoelectric microgenerator based on large scale integration of Si nanowires as thermoelectric material

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Improved thermal isolation of silicon suspended platforms for an all-silicon thermoelectric microgenerator based on large scale integration of Si nanowires as thermoelectric material

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Abstract. Special suspended micro-platforms have been designed as a part of silicon compatible planar thermoelectric microgenerators. Bottom-up grown silicon nanowires are going to bridge in the future such platforms to the surrounding silicon bulk rim. They will act as thermoelectric material thus configuring an all-silicon thermoelectric device. In the new platform design other additional bridging elements (usually auxiliary support silicon beams) are substituted by low conductance thin film dielectric membranes in order to maximize the temperature difference developed between both areas. These membranes follow a sieve-like design that allows fabricating them with a short additional wet anisotropic etch step.

1. Introduction

Silicon nanowires (Si NWs) thermoelectric properties are much better than those of bulk silicon [1,2]. Taking advantage of silicon microfabrication techniques and harmonizing the device fabrication with the growth of Si NWs, an all-silicon thermoelectric (micro) generator approach can be attempted. Such microgenerators would be useful as energy harvesting sources to power sensors nodes when a waste heat source is available. While standard thermoelectric modules use exotic materials and their assembling is hard to automate, especially when reducing their size, silicon microtechnology offers the possibility to exploit an abundant material and a mature technology that enables large volume fabrication and also offers an integration route for miniaturized devices. Moreover, silicon micromachining allows fabricating free surfaces or volumes physically coupling the device to the environment and also adds a third dimension to otherwise planar silicon devices. This additional dimension is useful to integrate the 3D nature of bottom-up growth methods of Si NWs.

2. Design and fabrication

Examples of this integration can be found in the literature such as in [3], where a trench is micromachined by DRIE on the silicon device layer of an SOI silicon wafer defining a silicon platform separated from the surrounding silicon rim (figure 1a). The handle wafer is patterned and the silicon under the platform region is removed for thermal isolation. Gold nanoparticles, with appropriate size and density, are selectively deposited in the opposing vertical walls of the silicon platform and rim by means of the galvanic displacement method. These gold nanoparticles act as seeds

for the Si NWs, which are then grown in a CVD following the VLS mechanism [4,5]. Si NWs grow preferentially on <111> planes. Vertical <111> walls are found in (110) silicon, so that the device layer of the starting SOI wafers should feature such orientation and the device design must follow the geometrical disposition of the two intersecting <111> family planes.

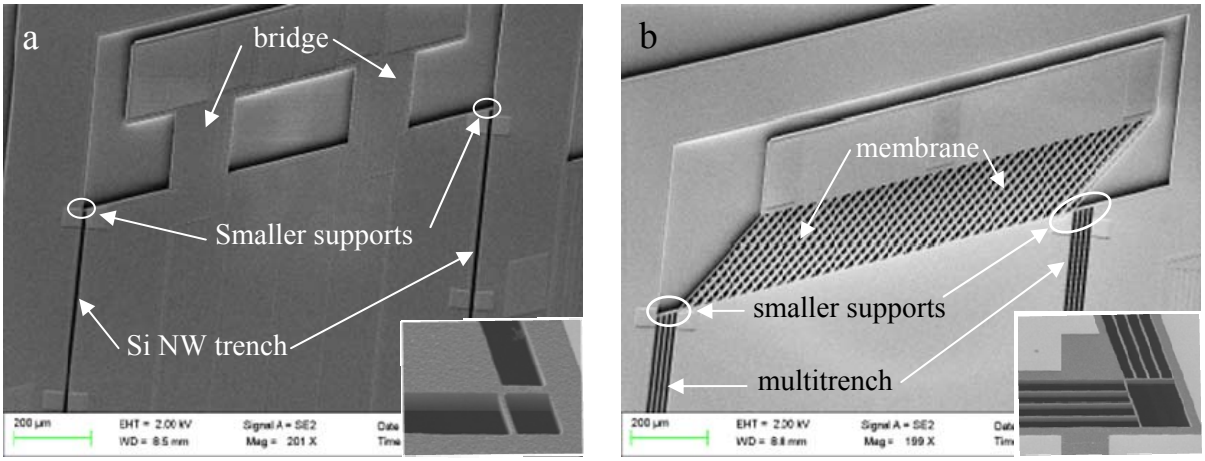

Figure 1. Suspended silicon platforms fabricated in SOI wafers. The platforms are supported by two bulk silicon bridges and other auxiliary bars (a) or by a perforated thin dielectric membrane (b). The later device also shows a set of spacers supported by longer auxiliary bars. The insets show a detail of the corners not shown that feature similar bars.

Once grown, Si NWs connect the silicon platform (the cold area) with the surrounding silicon bulk (the hot area) configuring the silicon leg of a (nanostructured) silicon-metal thermocouple. The length of the nanowires depends on the CVD process time, and it must be adjusted to cover the trench width. Nanowire tapering may occur at prolonged growth times. A given number of intermediate silicon spacers can be defined between the platform and the silicon rim (figure 1b). In this way, nanowires with arbitrary length can be designed/obtained as a multistage concatenation of shorter nanowires in a single controllable CVD process as in figure 2. Longer nanowires connecting heat source and heat sink shall feature higher thermal resistances and lead to a higher temperature drop across them [6]. Typical dimensions of the elements of those devices are 1 mm^2 platforms and 15 µm deep and 10 µm wide trenches (single or multi-trenches).

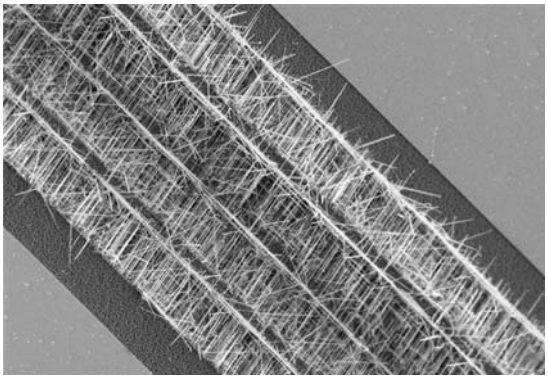

Figure 2. Silicon nanowires bridging four 10 µm (wide) x 15 µm (deep) trenches defined by three intermediate silicon spacers. These spacers are hold together between the suspended platform and the silicon rim by additional support bars (not shown). The growth of Si NWs into the current structures is still work in progress

In spite of the extra vertical dimension added by silicon micromachining to host the nanowires, the device is still essentially planar and its geometry obeys to the fact that vertical thermal gradients must be transposed in a the laterally assembled device. This is the reason why the suspended platform is needed in the first place: to force the heat flow through the laterally grown nanowires when the device is left to rest onto a hot surface. Material paths, other than the thermoelectric active ones, connecting the platform and the surrounding rim will negatively impact the thermal isolation of the suspended platform diminishing the attainable temperature difference. As shown in figure 1 and figure 2 and their insets, the 'suspended' platform is laterally supported by different features: two main bulk silicon bridges, which also host the electrical connection tracks; small secondary silicon bars at the four corners of the platform keeping it aligned to the silicon rim during Si NWs growth (stress gradients due to the metal and dielectric layers present in the platform may produce a vertical displacement); similar silicon bars in the multi-trench device holding the silicon spacers' ensemble in place.

Once the nanowires are grown, the smaller supporting bridges are no longer useful and they can be eliminated with FIB. This removal has a measurable impact on the thermal response of the platform [7]. However, this is not an option for the two main bridges hosting the metal tracks since they are the physical embodiment of one of the thermocouple legs. The purpose of this work is to find a larger thermal resistance alternative for those bridges. The solution devised consists of building a connecting dielectric membrane in substitution of the two bulky bridges. To do so, a sieve-like structure is defined in the supporting side of the device (figure 1b). The layers present in this region prior to any silicon DRIE are the silicon itself, a LPCDV silicon nitride layer, the patterned metal tracks and a PECVD oxide layer. The sieve holes and the trenches that will accommodate the Si NWs are defined by the same dry etch perforating the two dielectric layers and the silicon device layer of the SOI wafer till reaching the buried oxide (figure 3a). The sides of the sieve cavities are designed in a way their walls are aligned to fast-attacking silicon planes, so that a subsequent KOH wet anisotropic etch will remove laterally the silicon beneath the sieve area. Depending on the design, a few minutes etch may free the membrane, which is kept tight and flat by the tensile stress of the nitride (figure 3b). Metal tracks are defined finger-like to be accommodated in a distributed way on top of some of the nitride strips of the perforated membrane. The <111> vertical walls of the trenches to be covered by the Si NWs are preserved during the anisotropic etch releasing the membrane because such plane is very slowly etched by KOH. In fact, the final condition of the exposed <111> planes is improved because the typical scalloping found after DRIE is smoothed out.

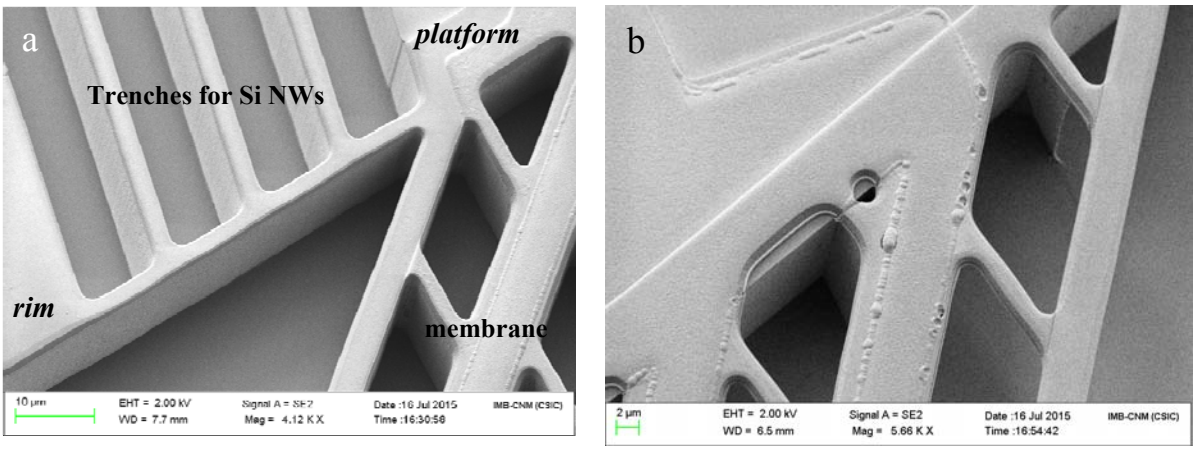

Figure 3. (a) Zoom-in of the perforated membrane and (multi)trench region after DRIE. Hole angles in the membrane are defined so that fast attacking planes are revealed. (b) Result after a KOH anisotropic etch that removes the silicon underneath the membrane.

3. Results

The thermal isolation offered by any physical support will depend on its cross-section, length and on the thermal conductivity of the building material. Silicon is a good thermal conductor so bridges of this material should be narrow and long for good thermal isolation. Since the main support structure should also host the metal leading to one of the terminals of the device, too narrow bridges will increase the internal electrical resistance of the generator. Typical silicon support bridges are 200 μm wide and 200 μm long. The nitride based membrane will offer a better isolation because, although wider (1 mm maximum), it will be ten times thinner (1.5 μm *vs.* 15 μm) than the bridges, and because silicon nitride and oxide have thermal conductivities five to one hundred times smaller than silicon.

In order to assess the thermal isolation provided by both alternatives, an indirect electrical way has been used. Both types of devices have the same built-in heater in their platforms. A similar power has been dissipated in the heaters of devices that only differ in the main support strategy. Those featuring a better thermal isolation will attain a higher platform temperature, which can be assessed by the value of the heater resistance itself (once its TCR is known). An example of such characterization is shown in figure 4. It can be seen that for any dissipated power the device with a membrane support reaches higher platform temperatures, so it can be concluded that such an approach will offer larger power densities in future generators implementations. Moreover, in the particular case shown in figure 4, the membrane length was half of the bridge length, so the membrane device occupy less area, which would also influence positively in the attainable power density.

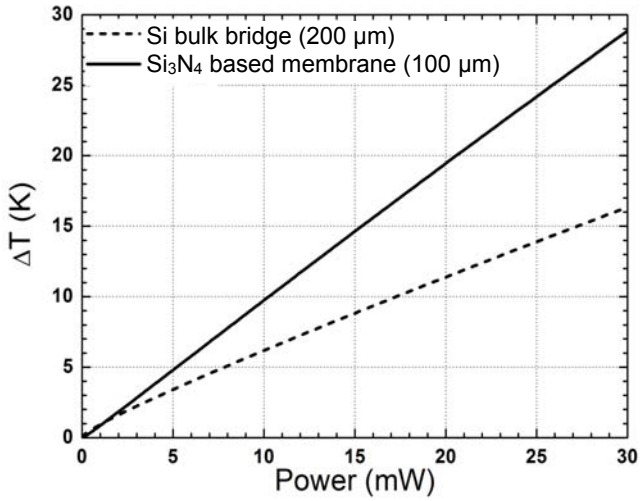

Figure 4. Platforms supported by dielectric membranes reach a higher temperature than the supported by bulk silicon bridges when the same power is dissipated by a built-in heater. This points to a much improved thermal isolation, even though in this particular example the membrane length (100 μm) was just half of the silicon bridges one. Power density will be thus further improved.

Acknowledgements

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