Circuit Modeling of a MEMS Varactor Including Dielectric Charging Dynamics

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Abstract. Electrical models for MEMS varactors including the effect of dielectric charging dynamics are not available in commercial circuit simulators. In this paper a circuit model using lumped ideal elements available in the Cadence libraries, and a basic Verilog-A model, has been implemented. The model has been used to simulate the dielectric charging in function of time and its effects over the MEMS capacitance value.

1. Introduction

Capacitive Micro-electromechanical Systems (MEMS) offer excellent performance combining mechanical and electrical components. They are the manufacturing of a wide variety of applications such as sensors, resonators, switches, ultrasonic transducers and varactors [1, 2]. However, their micro-scale size brings a number of reliability issues which prohibit their mass commercialization [3].

In particular, MEMS variable capacitors (varactors) suffer from deviations of their capacitance-voltage (C-V) characteristic. Their performance is limited by the dielectric charging effect which is an inherent reliability problem for these devices. The build-up process of trapping charges into the dielectric layer, can be treated as an offset voltage connected in series with the MEMS, provoking a voltage shift in the characteristic curve. To remove this trapped charge, techniques which apply bipolar width-modulated voltage pulse sequences have been recently introduced and tested with good results [4, 5, 6].

In modern circuit design the integration of MEMS with CMOS technology is a challenging step in micro-scale evolution. Computer aided design (CAD) tools play a significant role in the design and analysis process of chips [7, 8]. However, the complexity of MEMS, including failure mechanisms and reliability behavior, makes the modelling and simulation of chips which include these devices a task of high complexity.

In this paper, we present an adaptive system to implement a control method for the restriction of the dielectric charge of a MEMS varactor. The system's reliability relies highly on the MEMS capacitance measurement accuracy and resolution [9, 10]. Therefore, an accurate real-time measuring of the capacitance value is essential.

Electrical models for MEMS varactors including the effect of dielectric charging dynamics are not available in commercial circuit simulators. That is, here, for first time, we will focus in the implementation of a complete circuit model of a MEMS varactor using lumped ideal elements

available in the Cadence libraries along with a basic Verilog-A model. The model has been used to simulate the dielectric charging in function of time and its effects over the MEMS capacitance value.

2. Statement of the Problem

The complete description of the bipolar control method to deal with the dielectric charging issue is out of the scope of this study (for a full description see [4]). Here, we will only present briefly the whole system and we will focus mainly in the circuit modelling of the MEMS varactor, which is a crucial component for the successful design and simulation of the chip.

The system consists of a closed control loop as shown in Fig. 1 and it aims to restrict the build-up charge in the insulator of the MEMS varactor. Briefly, it works as follows: The value of the MEMS capacitance C_m is compared with the value of the reference capacitor C_r. Then the error signal e is fed to analogue processing stage which amplifies the capacitance difference. Finally, the output is converted into a digital word. This digital output is then used by the FPGA to set the duty cycle, and the polarity of the voltage to be applied to the MEMS using the DC voltage source V_B. The control loop is grouped into different sets: the MEMS varactor,

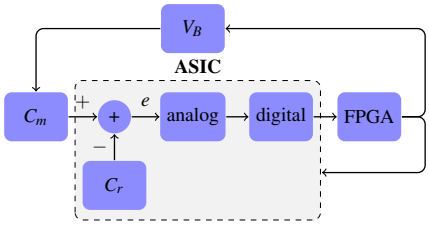

Figure 1: Control loop basic description at block level

the ASIC, the FPGA and the bias voltage. The ASIC consists of the input stage (including the reference capacitor), the analogue processing and the digital conversion. The FPGA reads and saves the digital output from the ASIC, and actuates the DC voltage, V_B. The capacitance difference measurement, the analogue processing and the digital conversion are performed inside the ASIC to reduce the second order effects and deviations introduced by parasitics. Since the accumulation of the dielectric charge is time dependent, in order to have reliable simulations for the ASIC design, is essential to include an electrical model for the MEMS that not only reflects the voltage dependence, but also the charge dynamics.

3. MEMS varactor DC model

The MEMS varactor consists of a moveable electrode which deflects due to the presence of an electrostatic force, and a fixed bottom electrode which includes a thin dielectric layer on the top (for a detailed description see [6, 11]). The device operates in two regimes, the contact-less operation (below pull-in) and the contacting (ON) operation (beyond pull-in). Pull-in denotes the value of the voltage where the varactor changes mode of operation.

The behavior of the MEMS C-V characteristic in the contact-less regime can be approximated by a parabola, eq. (1), whilst eq. (2) can be used to simulate the operation of the device in the regime beyond pull-in.

$$\text{Below pull-in: } C_m(V) = C_0 + aV^2 \tag{1}$$

$$\text{Beyond pull-in: } C_m(V) = b_1 - \frac{b_2}{\sqrt{V}} \tag{2}$$

Here, the values C_0, a, b_1 and b_2 can be calculated by the fitting of experimental data. These equations were integrated into a Verilog-A script to simulate the MEMS in a simulator for electric circuits.

Fig. 2 visualizes the curve fitting along with the simulation results obtained with the use of a Verilog-A model. The C-V curve for the Verilog-A model was simulated with the use of basic circuit consisting of the MEMS model itself, connected to a DC power supply and performing a DC sweep in Cadence ADE-L.

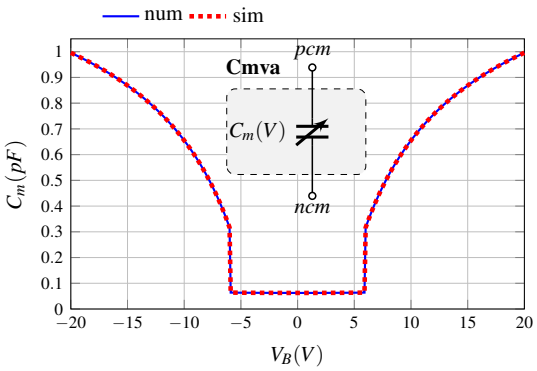

Figure 2: MEMS $C(V)$: numerical simulation in solid blue, cadence simulation in dashed red. $V_B = V_{pcm} - V_{ncm}$.

4. Equivalent electrical model for the dielectric charge dynamics

In principle, the charge dynamics of the dielectric is a complex dynamical procedure which can include more than one mechanisms [12] In this study, we will use a semi-empirical multi-exponential model (for a complete description see [13, 14]). The total charge consists of positive and negative multi-exponential components, in the most general case. Those components evolve in time, in principle, with different time constants, depending also on the polarity and the value of the applied voltage:

$$
\begin{aligned}
Q^p(t) &= \begin{cases} Q^p_{max} \sum_i \zeta^p_i e^{-t/\tau^p_{Di}} & V > 0 \\ Q^p_{max}(1 - \sum_i \zeta^p_i e^{-t/\tau^p_{Ci}}) & V < 0 \end{cases} \\
Q^n(t) &= \begin{cases} Q^n_{max}(1 - \sum_i \zeta^n_i e^{-t/\tau^n_{Ci}}) & V > 0 \\ Q^n_{max} \sum_i \zeta^n_i e^{-t/\tau^n_{Di}} & V < 0 \end{cases}
\end{aligned} \tag{3}
$$

where Q^p_{max} is the maximum value of the positive charge component, Q^n_{max} the maximum value of the negative charge component, τ_{Ci} and τ_{Di} the charging and discharging time constants and ζ_i coefficients which express the contribution of each exponential to the total charge. By definition $\sum_i \zeta_i = 1$ for each component. It is seen from this model that the time varying expression of the total charge $Q_d(t)$ in the dielectric is given as: $Q_d(t) = Q^p(t) + Q^n(t) = \sum q^p_n + \sum q^n_n$, and it is the sum of multiple *independent* charge components. For the simulations of this paper, a two exponential model have been used. Based on the form of this equation set, an equivalent electrical network consisting of resistors and capacitors can be found, see eqs.(4) and (5) (where for simplicity we use only two components, but these expressions can be easily generalized):

$$
Q_{cp} = C_{c1p}V(1 - e^{-\frac{t}{C_{c1p}R_{c1p}}}) + C_{c2p}V(1 - e^{-\frac{t}{C_{c1p}R_{c1p}}}) \tag{4}
$$

$$
Q_{dp} = C_{d1p}Ve^{-\frac{t}{C_{d1p}R_{d1p}}} + C_{d2p}Ve^{-\frac{t}{C_{d1p}R_{d1p}}} \tag{5}
$$

where the same sub-indexing rules for the positive and negative components apply. Note that the value of voltage V can be set arbitrarily because is not directly related with the bias voltage applied to the MEMS. The values for R and C can be calculated in order the values between the numerical model and the corresponding electrical equivalent model to be matched. It must be taken into account that:

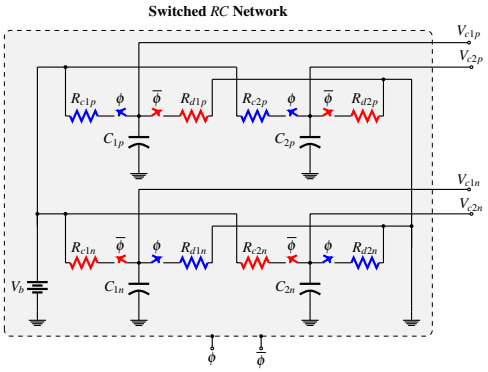

Figure 3: Equivalent switched RC network modelling the RF MEMS dielectric charging dynamics.

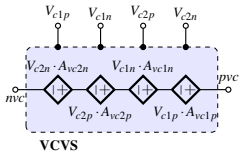

Figure 4: VCVS to generate equivalent V_{sh}.

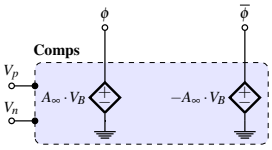

Figure 5: Comparators to generate $\phi - \overline{\phi}$.

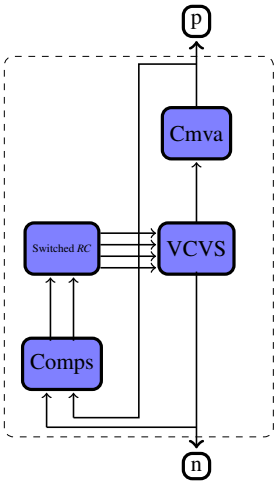

Figure 6: MEMS integrated model

- **for positive bias**, the capacitors C_{1p} & C_{2p} are *charged* to a positive voltage through the resistors R_{c1p} & R_{c2p}, respectively; and simultaneously, the capacitors C_{1n} & C_{2n} are *discharged* from the previous stored voltage (if exists) through the resistors R_{c1n} & R_{c2n}
- **for negative bias**, the capacitors C_{1p} & C_{2p} are *discharged* through the resistors R_{d1p} & R_{d2p}, respectively; and simultaneously, the capacitors C_{1n} & C_{2n} are *charged* through the resistors R_{c1n} & R_{c2n}

That is, the equivalent circuit must be switched according with these rules, and the control signals must be derived from the voltage applied to the MEMS. The equivalent switched RC network is shown in Fig. 3. The analog switches are modeled using Verilog-A with very high off-resistance, zero on-resistance and threshold voltage of $0.1mV$.

The resulting switched RC network models the dielectric charging and discharging times according to the applied voltage polarity. Moreover, in order to convert the voltage stored in every capacitor into an equivalent votlage shift, it must be amplified by a gain factor determined by the ratio between the corresponding capacitor in the network and the MEMS dielectric capacitance C_d. Once amplified, the resulting voltages must be added to calculate the total voltage shift. This must be connected to C_m as a voltage offset source.

To perform these tasks, a series-connected Voltage Controlled Voltage Sources (VCVS), every of them sensing the voltage on every capacitor and with the corresponding gain factor, is implemented, as depicted in Fig. 5. This source array is connected to the negative terminal of $Cmva$. In order to generate the control signals $\phi - \overline{\phi}$, two ideal comparators made of VCVS

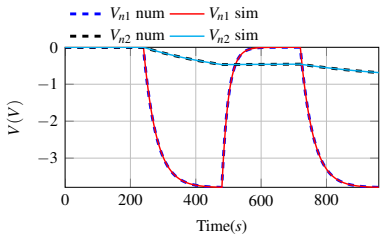

Figure 7: Negative charge contribution to V_{sh}

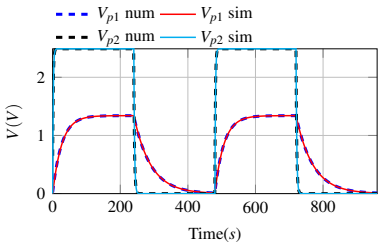

Figure 8: Positive charge contribution to V_{sh}

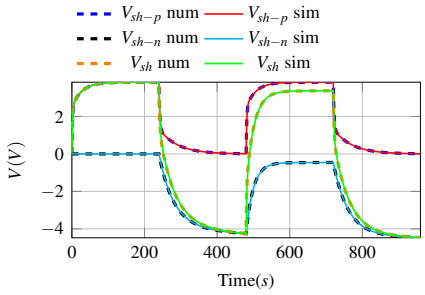

Figure 9: Positive and negative voltage shift and total V_{sh}

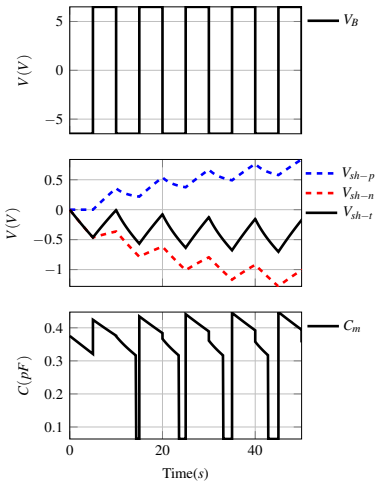

Figure 10: MEMS capacitance for a pulse voltage.

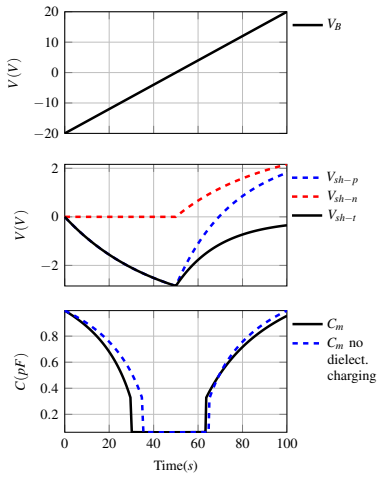

Figure 11: MEMS capacitance for a ramp voltage.

has been included. Comparators have extremely high voltage gain, no hysteresis, threshold voltage of $0.1mV$, minimum voltage of $0V$, and maximum voltage output of $1V$. The voltage applied to the MEMS integrated electrical model, between the node *pcm* in *Cmva* and node *nvc* in $VCVS$ block, is used as control voltage for the comparators. When the polarity is positive and larger than $0.1mV$, ϕ is high and $\overline{\phi}$ is low. When the polarity changes, the signals switch their values. Finally, the whole MEMS electrical model can be integrated as shown in Fig. 6.

5. Simulation results

The electrical model was simulated using the same circuit described in Section 3 for DC sweep, but now for transient analysis. The input signal (not shown in the plots) is a square pulse

with maximum voltage of $10V$ and minimum of $-10V$ and a period of $240s$. All the results are compared with the corresponding numerical simulations. In Fig. 7 the contribution of the components of the negative charge to the voltage shift are shown. Similarly in Fig. 8 for the positive charge. Additionally, in Fig. 9 the results for the total positive and negative charge are visualized along with the voltage shift V_{sh} considering all the contributions. The error is minimum, so the circuit effectively models the dielectric charging effects.

In Figs. 10 and 11 the resulting capacitance in function of time is shown. In Fig. 10, a pulse bias signal from $\pm 6.5V$ has been applied (top plot) provoking the voltage shift changes (middle plot) and then affecting the value of the capacitance (bottom plot). When the bias voltage is near to the pull-in value, it can be observed that the charge accumulation makes the V_{sh} large enough to provoke the MEMS to switch from high to low capacitance. In Fig. 11, a ramp is applied with voltage value of $\pm 20V$ (top plot). One can see that the evolution of the V_{sh} (middle plot) alters the C-V characteristic (bottom plot), in solid black, which deviates from the ideal behaviour (dashed blue) when no charge injection in the dielectric is considered.

6. Future work

In this paper an electrical model for a MEMS varactor, including the effects of dynamic dielectric charging has been presented. The model consists of ideal lumped elements available in the most common EDA Tools and Verilog-A code. A switched RC network that can be parametrized for different devices characteristics has been implemented. To improve the model, effects like temperature could be included via Verilog-A code or introducing some temperature factors for the lumped elements.

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