# Impedance-compensated grid synchronisation for extending the stability range of weak grids with voltage source converters

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**Abstract:** This paper demonstrates how the range of stable power transfer in weak grids with voltage source converters (VSCs) can be extended by modifying the grid synchronisation mechanism of a conventional synchronous reference frame phase locked loop (PLL). By introducing an impedance-conditioning term in the PLL, the VSC control system can be virtually synchronised to a stronger point in the grid to counteract the instability effects caused by high grid impedance. To verify the effectiveness of the proposed approach, the maximum static power transfer capability and the small-signal stability range of a system with a VSC HVDC terminal connected to a weak grid are calculated from an analytical model with different levels of impedance-conditioning in the PLL. Such calculations are presented for two different configurations of the VSC control system, showing how both the static power transfer capability and the small-signal stability range can be significantly improved. The validity of the stability assessment is verified by time-domain simulations in the Matlab/Simulink environment.

## 1 Introduction

Stability challenges related to interaction with the grid impedance are known to appear when voltage source converters (VSCs) are operating in very weak grids with low short-circuit ratio (SCR). Since very weak grids are most commonly encountered for HVDC transmission systems, several studies on the stability of VSC-based HVDC converter stations under such conditions have been published during the last years [1–8]. However, similar stability problems can also occur for VSCs utilised in grid integration of renewables or in weak distribution systems, as confirmed by several recent publications [9–12].

From the previous studies investigating VSC stability limitations under weak grid conditions, the identified instability phenomena can be mainly associated with two aspects:

(1) The reactive power flow in the system has a significant impact on the power transfer capability of a weak grid and by that on the stable operating range of grid connected VSCs. Thus, local voltage control and/or reactive power or current injection from the converter have been shown to improve both the steady-state power transfer capability and the large-signal transient stability range of the VSC [1, 3–7, 13–15]. However, the stability range and the effect of reactive power injection are closely related to the X/R ratio or impedance angle of the equivalent grid impedance [4, 5].

(2) The phase locked loops (PLLs) commonly used for grid synchronisation can strongly affect the dynamic performance and the stability range of VSCs operating in weak grids [5, 9, 11, 12, 16–19]. In general, stability problems associated with the PLL are related to the influence from the converter operation on the voltage measurements used for the grid synchronisation. This has been shown to cause a positive feedback mechanism which can provoke instability when the grid impedance is high [11, 12]. The corresponding effects on the VSC dynamics can be partially attenuated by reducing the bandwidth of the PLL, but this will result in a slower dynamic response of the converter [4, 5, 9, 17, 18].

To avoid instabilities caused by the influence from the converter operation on the local voltage measurements used for grid synchronisation, a voltage sensorless approach for synchronising to a remote and stronger point in a weak grid by a virtual flux-based estimation was proposed in [20, 21]. This approach was shown to significantly improve the VSC stability range and the power transfer capability in a weak grid. The stability improvement was attributed partly to the synchronisation to a remote and stiff voltage, but also to the corresponding change of reference frame orientation, which ensured an appropriate load-dependent reactive power injection from the VSC. In case the total impedance was known, sensorless synchronisation to the Thévenin equivalent voltage of the grid allowed for stable operation close to the theoretical limit of power transfer through the grid impedance, as long as the VSC dc-bus voltage was maintained sufficiently high to avoid over-modulation. A similar approach, combining a virtual impedance with the estimation of virtual flux in the grid from local voltage measurements rather than from a voltage-sensorless estimation, was further proposed in [22]. More recently, control systems, including a virtual impedance for similar purposes have also been proposed in [23, 24]. However, all these approaches require either a dedicated estimation method or an additional impedance-based control loop in the VSC control system.

Another possible approach for improving the stability range of VSC operation in weak grids is to apply control methods that determine the phase angle reference by introducing a power-balance-based synchronisation mechanism similar to the operation principle of traditional synchronous machines. Thus the 'power synchronisation controller' proposed in [2, 3] or other control methods that can be classified as virtual synchronous machines [25–27] could be relevant for operation in weak grid conditions. These control methods also have the advantage that they can inherently allow for islanded operation and black-start capability. However, a VSC cannot sustain the same large transient currents as a synchronous machine, and must limit its

currents during faults or temporary overload conditions. Thus, power-balance-based synchronisation cannot be maintained under severe transients and the VSC control system must be dynamically changed into current limiting operation [2, 28], which again leads to challenges related to on-line transfer between different control loops. Thus, as long as stability challenges due to weak grid conditions can be avoided, conventional current controlled operation with grid synchronisation by a PLL can still be considered as a simpler solution for VSCs that are not required to operate in islanded mode.

To avoid the stability limitations of a PLL-synchronised VSC in a weak grid, an impedance-based compensation term was introduced in the traditional synchronous reference frame (SRF) PLL in [29]. The resulting impedance-conditioned PLL (IC-PLL) can ensure quasi-stationary synchronisation to a remote point, and the same extension of the stability range in a weak grid as the more complicated control strategies discussed in [20–22]. The implementation requires only simple calculations based on voltage and current measurements to be included in the PLL. However, the analysis presented in [29] was limited to a control system configuration with a fixed value of the reactive current reference for the VSC while most practical applications of VSC HVDC systems in weak grids are required to control the local ac voltage through a voltage control loop. Therefore, starting from the results presented in [29], this paper will extend the analysis of the stability improvements that can be achieved with the IC-PLL to the case with an ac voltage control loop. The stability improvements with both control system configurations will be first identified from detailed state-space models and then verified by time-domain simulations in the Matlab/Simulink environment.

## 2 Grid synchronisation for increasing the stability range in weak grids

The influence of the proposed IC-PLL on the stability range is investigated for a VSC HVDC terminal connected to a weak grid. The system configuration, the assumed converter control structure and the IC-PLL implementation are presented in the following subsections.

### 2.1 Overview of the general system configuration

The investigated system consists of a VSC HVDC converter terminal connected to a high-impedance grid through an LC filter and a transformer as shown in Fig. 1. The converter currents are assumed to be controlled by conventional SRF decoupled proportional–integral (PI) current controllers [30]. To avoid that potential LC filter oscillations influence the stability range, an active damping algorithm provides stabilising voltage references $v_{AD}^*$, as indicated in the figure [31, 32].

As shown in Fig. 1, an outer loop PI power controller is assumed to provide the active current reference $i_{cv,d}^*$. However, in the same way as the virtual flux-based methods from [20–22], the IC-PLL will have a similar influence on the system stability for any implementation of the power control. Thus, impact on the stability range will be similar also in the case of feed-forward power control where the active current reference results from a division of the power reference by the measured grid voltage amplitude [33], or with an outer loop dc-voltage controller [34]. It is also indicated in Fig. 1 how two different control system configurations for providing the reactive current reference $i_{cv,q}^*$ are investigated. In the following, these two configurations will be referred to as:

(i) *Case 1:* The control system configuration from [29], where the reactive current reference is set to a fixed value ($i_{cv,q}^* = 0$).

(ii) *Case 2:* A control system configuration where the $q$-axis current reference is provided by a PI-controller regulating the local ac voltage, as indicated in grey within Fig. 1

### 2.2 Impedance-conditioned PLL

A conventional PLL implementation according to [35], as indicated in the upper part of Fig. 2, is assumed as the starting point for the design of an impedance-conditioned synchronisation mechanism. This PLL structure applies low-pass filters on the estimated $d$-axis and $q$-axis voltage components, while an inverse tangent function generates the phase angle error $e_\theta$. A PI-controller processing this phase error tracks the grid frequency, which is the input to an integrator producing the phase angle estimate $\theta_{PLL}$. The inverse tangent function is preferred to maximise the linear tracking range of the PLL, but the proposed impedance term can be included in any other PLL implementation for orienting the SRF to the $d$-axis (or $q$-axis) of a measured three-phase voltage signal [36].

The proposed impedance conditioning is obtained by subtracting a quasi-stationary voltage drop across a virtual impedance from the local voltage measurement input to the PLL. Thus, the PLL can synchronise to an estimated, 'remote' voltage $\tilde{v}_{VI}$, expressed as a complex space vector in (1) by assuming a virtual impedance
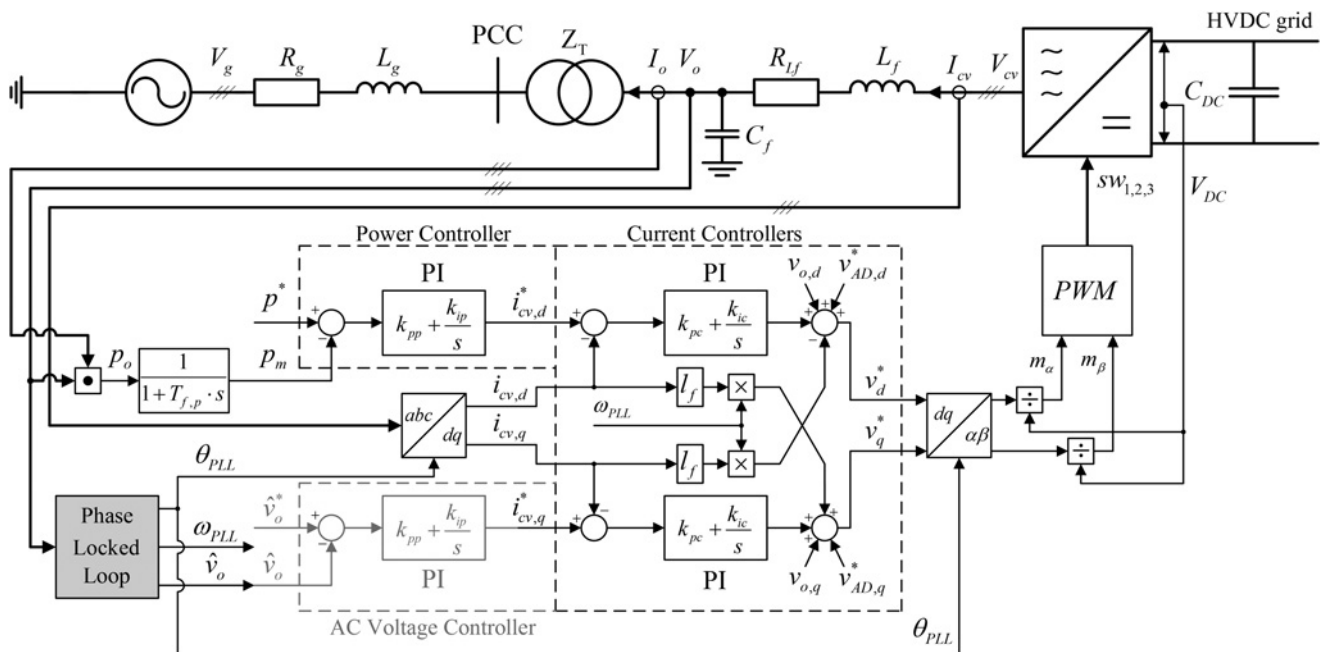


**Fig. 1** *Overview of investigated configuration and control system for VSC operated in a weak grid*
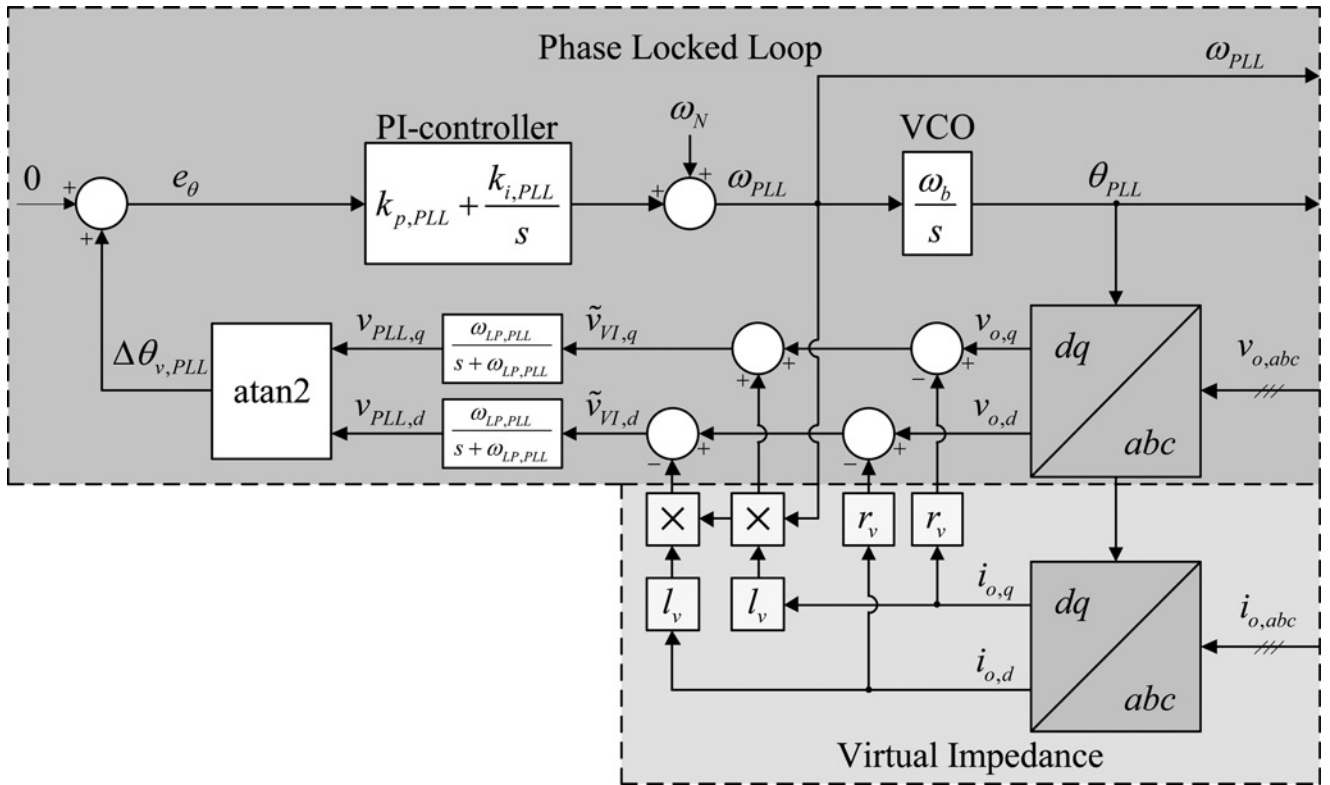
**Fig. 2** *Schematic of the proposed IC-PLL*

given in per unit as $z_v = r_v + j\omega_g l_v$. The only additional input to the PLL is the grid-side current $\boldsymbol{i}_o$, which also must be transformed into the $dq$ reference frame established by the PLL

$$\tilde{\boldsymbol{v}}_{VI} = \boldsymbol{v}_o - r_v \boldsymbol{i}_o - j \cdot \omega_{PLL} l_v \boldsymbol{i}_o \qquad (1)$$

The corresponding implementation of the $d$-axis and $q$-axis voltage drop across the virtual impedance term is shown in the lower right of Fig. 2. As seen from the figure and from (1), the voltage drop across the virtual inductance is proportional to the grid frequency estimated by the PLL.

A vector diagram illustrating the potential impact of the proposed impedance conditioning on the SRF orientation of the PLL is shown in Fig. 3. In this figure, $\delta_g$ is the phase displacement between the grid voltage $v_g$ and the voltage vector $\boldsymbol{v}_o$ at the filter capacitors. This angle indicates the range of SRF orientations that can be obtained by the IC-PLL. The phase angle $\delta\theta_{PLL,0}$ is the steady-state displacement between the grid voltage vector and the SRF orientation of the IC-PLL given by the voltage vector $\tilde{\boldsymbol{v}}_{VI}$. The instantaneous phase angle estimated by the PLL is given by $\theta_{PLL}$ and is used for the SRF transformations in the control system. The vector diagram in Fig. 3 indicates that the IC-PLL will synchronise directly to the measured voltage as any conventional PLL when the virtual impedance or the current flowing into the grid are equal to zero. However, when the system is loaded, the virtual impedance can be selected so that the PLL is synchronised to an estimated voltage at any electrical distance between the locally measured voltages and the equivalent grid voltage. Operation with zero reactive current reference will then impose approximately zero reactive power flow at the remote point of synchronisation. In case of high grid impedance and high values of virtual impedance, this can require excessively high output voltage and lead to over-modulation as discussed in [20, 21].

It should be noted that the equivalent grid impedance as seen from a converter is not always exactly known and might also change with reconfigurations of the grid. Thus, a complete compensation of the grid impedance might be impractical. However, it will be demonstrated that any partial impedance compensation improves

the stability range without any negative effects on the converter operation. Furthermore, the proposed approach can be combined with a remote measurement of active and/or reactive power flow to allow for estimating the equivalent grid impedance as proposed in [22].

## 3 Analysis of system stability limits

To characterise the improvements in terms of stationary power transfer capability and small-signal stability that can be achieved with the proposed IC-PLL, analytical models of the converter and the control system structures from Fig. 1 have been developed. These models are based on the modelling approach in [37] and are reported in Appendix 1, while the corresponding small-signal state-space representations are indicated in Appendix 2. This
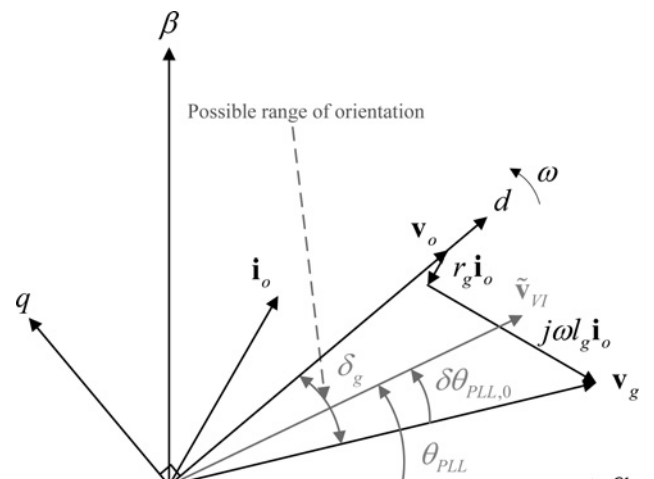


**Fig. 3** *Vector diagram showing the possible range of SRF orientation for the IC-PLL*

section presents an analysis of the two control system configurations indicated in Fig. 1 by applying these models and the parameters presented in Table 1 in Appendix 3. The results verify the claimed improvement in stability range and illustrate how the impedance conditioning can influence the operating conditions of the VSC terminal.

### 3.1 Stability limits with conventional PLL

The stability limitations of the system from Fig. 1 are first investigated with a conventional PLL for Case 1 and Case 2 in both inverter ($p > 0$) and rectifier ($p < 0$) operations. The static power transfer capability of the system is determined by solving the non-linear steady-state equations according to (22) and (23), and numerically searching for the maximum power transfer where these equations have a solution. The small-signal stability limitations are identified as the maximum active power transfer leading to stable poles for the linearised models according to (25) and (26). The results are plotted as a function of the equivalent grid impedance in Fig. 4a for Case 1 and in Fig. 4b for Case 2. For these plots, a grid impedance angle $\varphi_g$ of 80° is assumed ($\varphi_g = \tan^{-1}[l_g/r_g]$), where $l_g$ and $r_g$ are the equivalent per unit grid inductance and grid resistance, including the series impedance of the transformer indicated in Fig. 1.

The curves in Fig. 4 clearly indicate that the power transfer capability of the system is decreasing non-linearly as the grid impedance is increasing. For Case 1, the small-signal stability range is identical to the static power transfer capability of the system. Thus, attempting to transfer a power higher than the identified stability limitations will result in a voltage collapse. For rectifier operation, the power transfer capability is falling below 1.0 pu already for a grid impedance exceeding 0.4 pu (i.e. SRC = 2.5). As expected, the power transfer capability is higher for inverter operation, but still the grid impedance must be below about 0.6 pu (corresponding to an SCR of about 1.7) to transfer 1.0 pu power. Moreover, the plotted curves closely resemble an inverse function of the grid impedance, which translates into a power transfer capability linearly dependent on the SCR (since SCR = $1/|z_g|$), equivalently to the results presented in [4].

Several differences can be noticed between Figs. 4a and b. First, Case 2 results in a clear differentiation between the small-signal stability limit and the static power transfer capability limit. Thus, the system will experience small-signal instability as discussed in [17] before the static power transfer capability is reached. Second, the stability range is much wider for Case 2 than for Case 1. Thus,

with the parameters from Table 1, stable operation can be maintained for 1.0 pu power transfer up to almost 0.75 pu grid impedance (i.e. an SCR of about 1.3) in inverter operation, and to almost 0.65 pu grid impedance (i.e. an SCR of about 1.5) in rectifier operation. Indeed, this extended stability range is due to the voltage controller, ensuring a partial compensation of the reactive power consumed by the weak grid impedance compared to the case with unity power factor at the filter capacitors. However, the VSC cannot fully benefit from the increased static power transfer capability resulting from the voltage control action due to the small-signal stability limitations.

### 3.2 Impact of PLL tuning and impedance compensation on the small-signal stability limit

Since the small-signal stability limit for Case 1 is equal to the static power transfer capability limit, the PLL parameters do not have significant influence on this case when applying the symmetrical optimum (SO) tuning presented in Appendix 3. Thus, the stability limitations are mainly caused by the reactive power consumption of the large grid impedance. However, for Case 2 there is a significant difference between the small-signal stability limit and the static stability limit, which results from the interaction between the ac voltage controller and the PLL.

According to the results presented in [17], it should be expected that the small-signal stability limit can be extended towards the static stability limit by slowing down the PLL tuning compared to the parameters given in Table 1. Although the PLL used in this study has an additional filter which slightly changes the characteristics and the tuning approach compared to [17], this effect is demonstrated by the pole trajectory shown in Fig. 5a. In this plot, the system is analysed in inverter operation with a power reference of 1.0 pu and a grid impedance of 0.8 pu. From the curves in Fig. 4b, it can be seen that the system will experience small-signal instability with the PLL parameters from Table 1 in Appendix 1. The trajectory of the critical eigenvalue when sweeping the low-pass filter crossover frequency of the PLL, $\omega_{LP,PLL}$, while maintaining the tuning criteria given in Appendix 3, is shown in Fig. 5a. This corresponds to a reduction of the PLL closed loop bandwidth, and the arrows in the figure indicate how the critical eigenvalues are initially moving towards the left and become stable when the PLL bandwidth is reduced. However, the location of the critical eigenvalues reach a minimum real value before they start moving towards zero when the PLL becomes very slow. Even with the PLL parameters corresponding to the
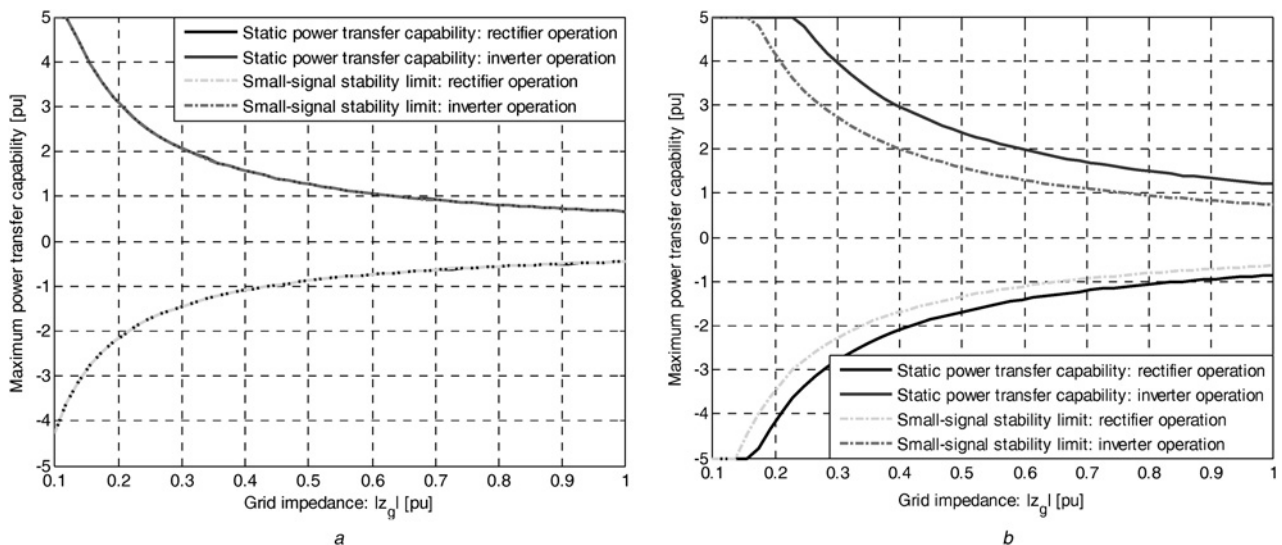


**Fig. 4** *Stability limits of the investigated system with conventional PLL, as a function of grid impedance ($\varphi_g = 80°$)*

*a* Case 1: fixed *q*-axis current reference equal to 0
*b* Case 2: ac voltage controller with 1.0 pu voltage reference

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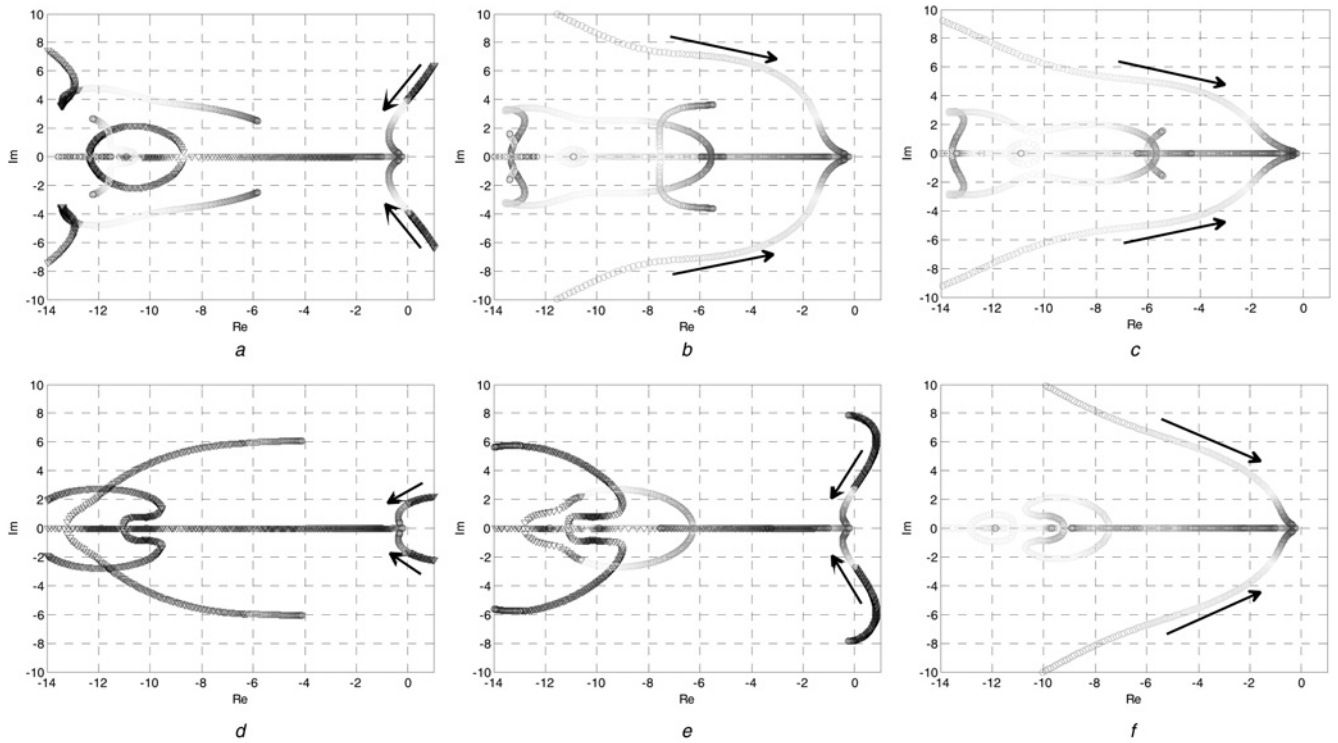
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**Fig. 5** *Eigenvalue trajectories for Case 2 for different cases of power reference and impedance compensation with PLL tuned according to Appendix 3, when sweeping $\omega_{LP,PLL}$ from 500 to 1 rad/s (direction indicated by arrows for the critical modes), (SCR = 0.8, $\varphi_g = 80°$). Black triangles represents unstable conditions*

*a* Operation as inverter with power reference of 1.0 pu and conventional PLL
*b* Operation as inverter with power reference of 1.0 pu and IC-PLL with 40% impedance compensation
*c* Operation as inverter with power reference of 1.0 pu and IC-PLL with 60% impedance compensation
*d* Operation as rectifier with power reference of −1.0 pu and conventional PLL
*e* Operation as rectifier with power reference of −1.0 pu and IC-PLL with 40% impedance compensation
*f* Operation as rectifier with power reference of −1.0 pu and IC-PLL with 60% impedance compensation

most negative real part of the eigenvalue, the system will still be very close to the stability limit and will have a relatively poor dynamic response due to the long settling time of the critical mode.

The effect on the trajectory of the critical eigenvalues from introducing a virtual impedance compensation of 40% of the grid impedance in the IC-PLL is shown in Fig. 5b. By comparing the trajectories in Figs. 5a and b, it can be seen how the virtual impedance in the IC-PLL is effectively eliminating the instability

effect caused by the weak grid and the interaction between the PLL and the ac voltage controller. Thus, by synchronising to a virtually stronger point in the grid, the interaction between the ac voltage controller and the PLL is mitigated. Thus, the eigenvalue trajectory becomes similar to a case where the PLL is based on voltage measurements in a stronger grid. This effect is even more noticeable in Fig. 5c plotted for an impedance compensation ratio of 60%.
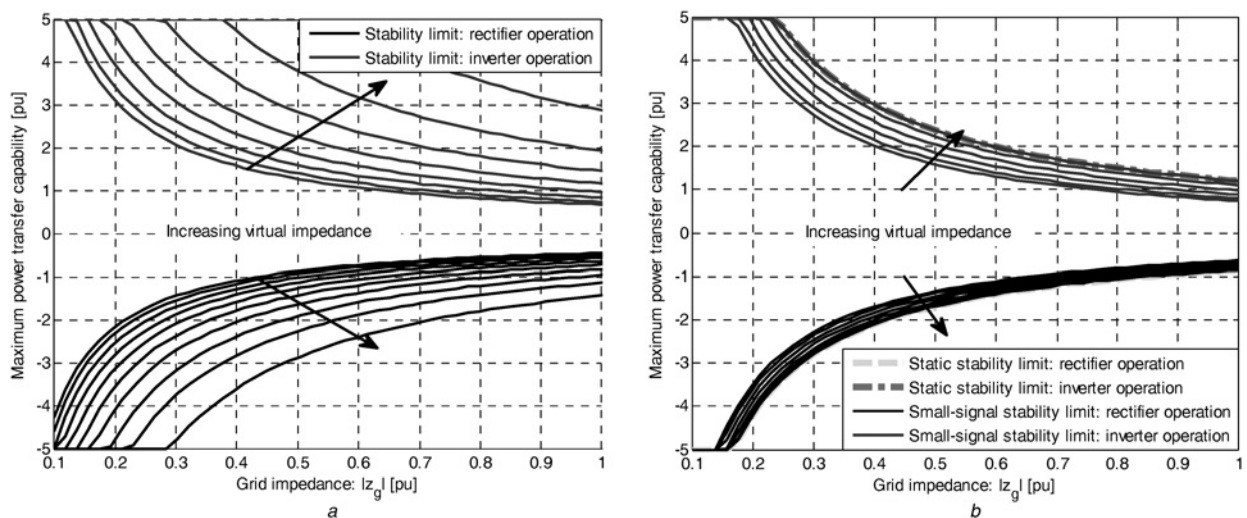


**Fig. 6** *Stability limits of the investigated system as function of the total grid impedance for increasing levels of impedance compensation ($\varphi_g = 80°$)*

*a* Case 1: fixed *q*-axis current reference equal to 0
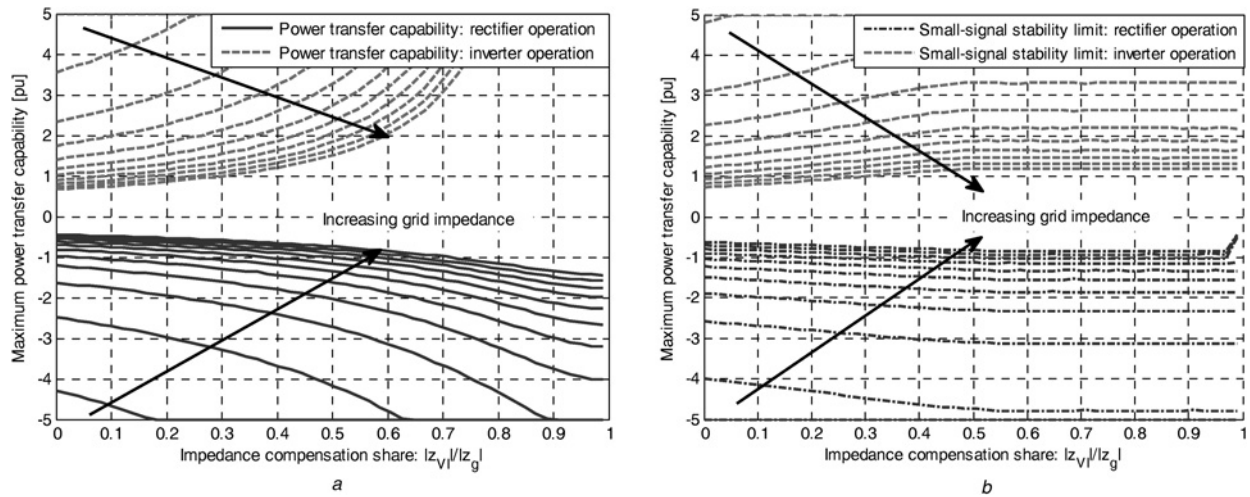*b* Case 2: ac voltage controller with 1.0 pu voltage reference

**Fig. 7** *Stability limits as a function of the impedance compensation level for different grid impedance ($\varphi_g = 80°$)*
*a* Case 1: fixed $q$-axis current reference equal to 0
*b* Case 2: ac voltage controller with 1.0 pu voltage reference

A similar set of results as in Figs. 5a–c are shown for rectifier operation with −1.0 pu power reference in Figs. 5d–f. From the rectifier side stability limits in Fig. 4b it can be seen that the system will be very close to the static stability limit for a grid impedance of 0.8 pu. Thus, from Fig. 5d it can be seen that the system has a very narrow stability range with the conventional PLL. Fig. 5e shows that introducing a virtual impedance share of 40% in the IC-PLL improves the stability range, but there is still a range of PLL tunings where the system will reach small-signal instability. Increasing the impedance compensation share to 60%, the PLL impact on the system stability due to the weak grid is almost eliminated and the system can be kept stable with any bandwidth of the PLL.

### 3.3 Stability limits with IC-PLL

The impact from grid synchronisation by the IC-PLL on the power transfer capability is illustrated in Fig. 6. In this figure, similar curves as shown in Fig. 4 are plotted for increasing levels of virtual impedance from 0 to 100%, with the share of compensation increased by 10% for each curve. For simplicity, the phase angle of the virtual impedance is kept equal to the grid impedance angle.

The curves in Fig. 6a demonstrate a significant increase of the power transfer capability for Case 1. Thus, it is possible to achieve 1.0 pu power transfer in both directions with 1.0 pu grid impedance (i.e. an SCR of 1.0). This case is also small-signal stable within the full range of static power transfer capability with all levels of virtual impedance in the IC-PLL. This is in agreement with the findings obtained by trial-and-error simulation for a virtual flux-based grid synchronisation in [20–22], and indicates that the quasi-stationary approximation in the IC-PLL implementation does not significantly affect the small-signal stability.

The impact of the impedance conditioning is less pronounced for Case 2 as shown in Fig. 6b, even if improvements are still noticeable. This is because the static power transfer capability limitation of the system is determined by the 1.0 pu reference value for the ac voltage control loop, which determines the steady-state capacitor voltage. Therefore, the impedance compensation cannot influence the steady-state stability limit for this case. However, increasing the level of impedance compensation in the IC-PLL is effectively moving the small-signal stability limit towards the static power transfer limitation of the system. This occurs inherently when increasing the virtual impedance without any modification of the PI-controller gains of the PLL. Further stability improvements beyond the static stability limits given in Fig. 6b can only be achieved by increasing the ac voltage reference, since this will

allow the VSC to supply more reactive power to the grid in a similar way as for Case 1 with high virtual impedance.

To further illustrate how the impedance conditioning is influencing the power transfer capability for different values of the grid impedances, the stability limits are plotted as a function of the impedance compensation share in Fig. 7. The curves in these plots are representing a range of grid impedances from 0.1 to 1.0 pu, with each curve representing a step of 0.1 pu, still assuming an impedance angle of 80°. The curves in Fig. 7a clearly show how increasing the virtual impedance can enable a theoretical power transfer capability of Case 1 exceeding 1.0 pu in both inverter operation and rectifier operation with a grid impedance of 1.0 pu. However, the power transfer capability is as expected always lower for rectifier operation than for inverter operation due to the voltage drop across the equivalent grid resistance.

For Case 2, the curves in Fig. 7b show how the power transfer capability is increased almost linearly with the virtual impedance until an impedance compensation share of about 50% is reached. At this point, the small-signal stability limit is approaching the static power transfer capability limit imposed by the ac voltage reference, as shown in detail for 1.0 pu grid impedance in Fig. 8. Thus, further increase in the virtual impedance is not helping to increase the power transfer capability, and the system is not able to achieve 1.0 pu power
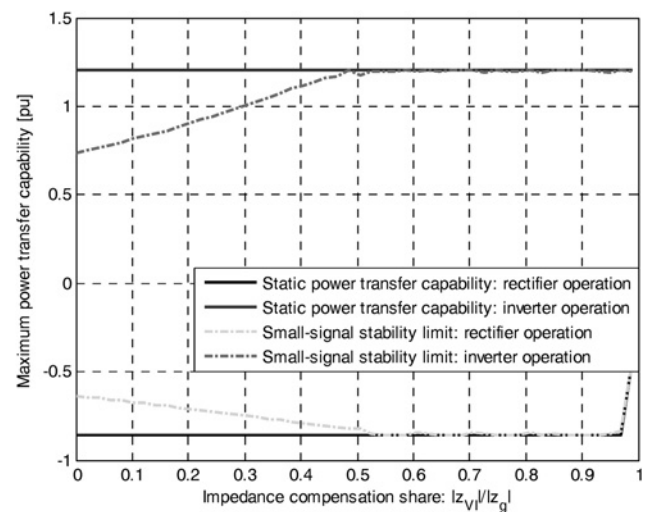


**Fig. 8** *Stability limitations of Case 2 as a function of the impedance compensation (SCR = 1, $\varphi_g = 80°$)*

transfer in rectifier operation. However, the improvement of the small-signal stability range demonstrated in Fig. 8 is significant and, as already mentioned, this is achieved without modifying any other parameters than the virtual impedance of the IC-PLL and without any other consequences for the converter operation.

For Case 1, full impedance compensation in a weak grid might lead to a very high reactive power injection, resulting in higher voltage and current requirements for the VSC. Thus, the consequences for the operating conditions should be taken into account when selecting the virtual impedance. To investigate these issues, the power transfer capability limit and the corresponding voltage and current amplitudes at the filter capacitors of the VSC are plotted in Fig. 9 as a function of the impedance compensation share for the case of 1.0 pu grid impedance (SRC = 1.0) with $\varphi_g = 80°$. These curves show that the converter voltage and currents can increase excessively for more than about 50% compensation since this implies significant reactive power injection from the converter. However, for inverter operation of the VSC, a virtual impedance share in the range of 30–40% of the equivalent grid impedance is enough to ensure a power transfer capability of 1.0 pu, with a filter voltage around 1.0 pu and a current amplitude of about 1.2 pu. Thus, the converter must be slightly over-rated in current capability to be able to achieve 1.0 pu power transfer.

A higher share of virtual impedance, and a correspondingly higher injection of reactive power, is required for Case 1 in rectifier operation to reach 1.0 pu power transfer capability with an SCR of 1.0, due to the effect of the resistive voltage drop across the equivalent grid resistance. However, when increasing the virtual impedance towards 70% of the grid impedance, stable operation can still be ensured with a 50% current over-rating, which results in about 1.2 pu voltage at the filter capacitor. Although it might not be realistic to design a VSC for such operating conditions, this proves that applying the proposed IC-PLL for grid synchronisation can ensure stability beyond the lower acceptable SCR limits of about 1.3 found in [17]. From practical considerations, it can be appropriate to set the virtual impedance equal to the known minimum impedances in the system, like for instance the equivalent series impedance of the transformer and the lines in the radial part of the transmission system.

## 3.4 Verification of calculated stability limits

The stability limits calculated in the previous sections have been verified by time-domain simulations in the Matlab/Simulink/SimPowerSystems environment. For reducing the computational effort, an average model of the VSC has been preferred for the simulations, since a switching model will not significantly influence the results as demonstrated in [17]. A set of simulation results obtained with 1.0 pu total grid impedance and $\varphi_g = 80°$ are shown in Fig. 10 for both Case 1 and Case 2, where a conventional PLL is compared to the IC-PLL with 50% impedance compensation.

The upper part of Fig. 10a shows a set of simulation results for Case 1 in inverter operation, when the power reference is increased in steps from 0 to 1.0 pu, with smaller steps around the calculated stability limit with the conventional PLL. At simulation time $t = 4.0$ s, the power reference is stepped from 0.650 to 0.675 pu, and the dashed curve in the figure clearly shows that instability is reached at this power level as predicted by the results from Fig. 4. With the IC-PLL, the system can reach the full 1.0 pu power transfer, as expected from the curves in Figs. 7a and 9. In the lower part of Fig. 10a, a similar simulation is repeated for rectifier operation of the VSC. In this case, the system with the conventional PLL becomes unstable when the power reference is stepped from −0.450 to −0.475 pu, corresponding to the stability limit shown in Fig. 4a, while the system with the IC-PLL is still stable. However, when the power reference is stepped from −0.650 to −0.675 pu, also the case with 50% virtual impedance in
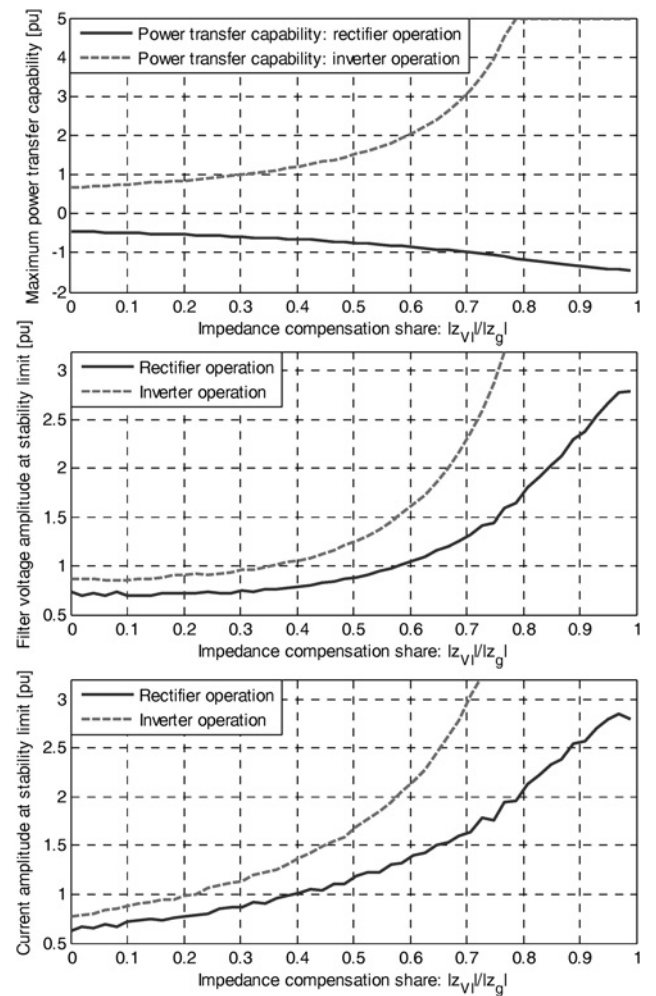


**Fig. 9** *Operating conditions at the stability limits for Case 1 as a function of the impedance compensation (SCR = 1, $\varphi_g = 80°$)*

the IC-PLL reaches its power transfer capability and the system collapses, as predicted by the curves in Figs. 7a and 9.

The same type of simulation results is presented for Case 2 in Fig. 10b. For inverter operation, the upper plot in this figure shows how the system becomes unstable when the power reference is stepped from 0.70 to 0.75 pu, matching well with the small-signal stability limit of about 0.74 that can be found from the plot in Fig. 4a. It can be noticed from the plot that even if the limitation for operation at 0.75 pu is given by a small-signal instability, the oscillations triggered by this instability and the transient step in the power reference quickly develop into a non-linear response which causes a voltage collapse of the system. However, the case with the IC-PLL can reach 1.0 pu power transfer without experiencing any stability problems. It can also be noted that the system shows a less oscillatory response with the IC-PLL, verifying that the critical eigenvalues of the small-signal model are more damped than with the conventional PLL as expected from Fig. 5.

The results in the lower part of Fig. 10b show the stability limits for Case 2 in rectifier operation with the conventional PLL and with the IC-PLL. From these curves, it can be seen that the system with the conventional PLL becomes unstable when the power reference is stepped from −0.6 to −0.65 pu while the case with the IC-PLL becomes unstable when the power reference is stepped from −0.80 to −0.85 pu. These results are in agreement with the curves in Figs. 4b, 7b and 8. Thus, the time-domain simulations effectively verify that the models presented in the Appendix can be used to accurately assess the stability limits and the power transfer capability of the investigated system configurations.
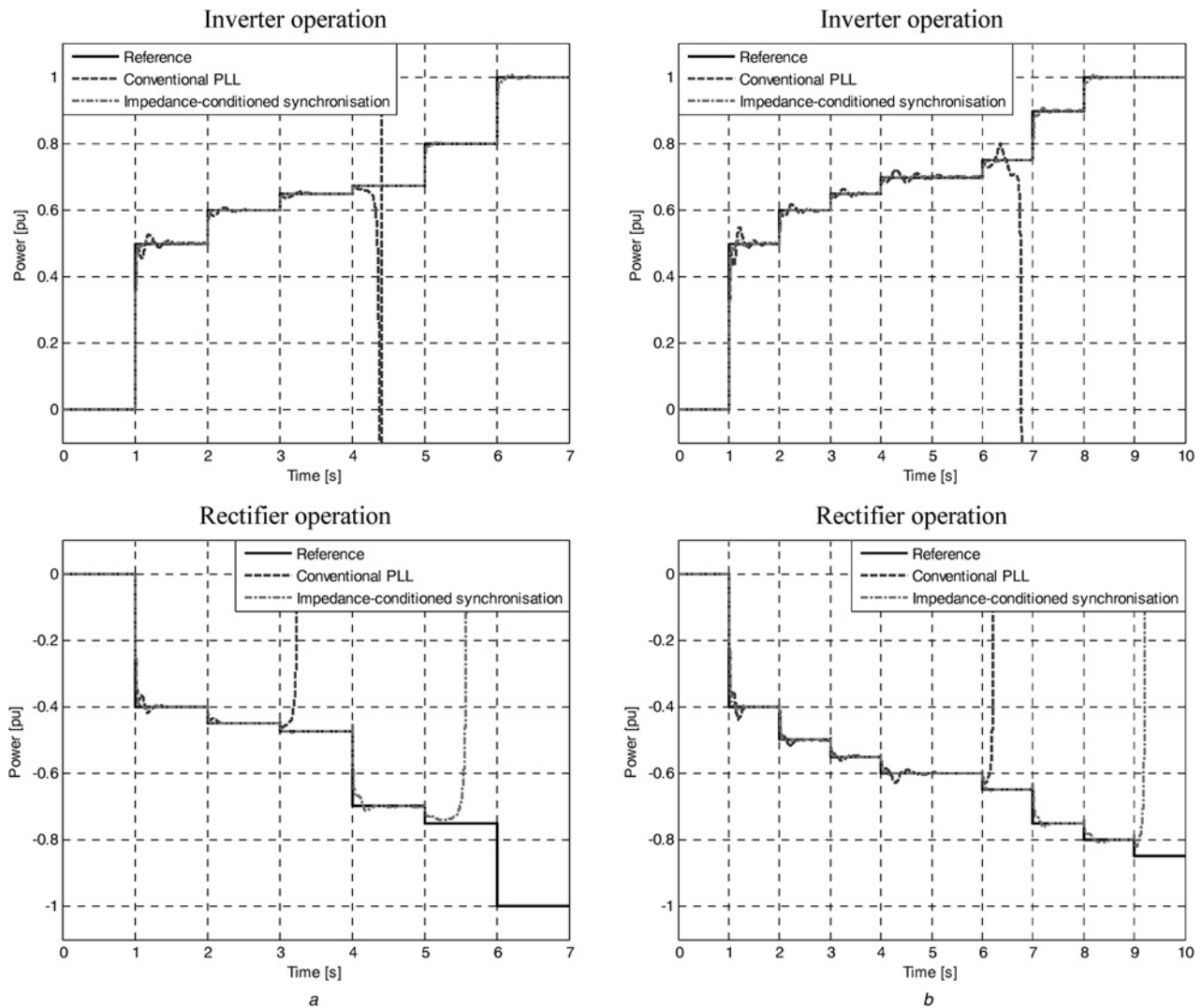
**Fig. 10** *Time domain simulations for verifying the stability limits calculated from the system model without impedance conditioning and with 50% virtual impedance*

*a* Case 1: fixed *q*-axis current reference equal to 0
*b* Case 2: ac voltage controller with 1.0 pu voltage reference

## 4 Conclusion

A method for extending the range of power transfer capability in weak grids with VSCs by introducing a virtual impedance in the voltage measurements used for grid synchronisation has been proposed. Such impedance conditioning can be utilised to synchronise the VSC control system to a virtual remote point in the grid, where the estimated voltage will be less influenced by the converter operation. The synchronisation to this virtually stronger point in the grid will influence the reference frame orientation of the VSC control system. When using a fixed *q*-axis current reference, this can be utilised to inherently provide load-dependent reactive power support from the VSC with a similar effect as inserting a virtual series capacitor in a weak inductive transmission line through the VSC control system. Thus, the power transfer capability can be correspondingly increased. If the VSC is operated with an ac voltage control loop, the static power transfer capability limit is given by the ac voltage reference, but the small-signal stability limit of the system with a conventional PLL will be reached at lower power levels. However, the proposed IC-PLL can increase the small-signal stability range towards the static power transfer capability limit and by that increase the practically achievable steady-state power transfer capability of the system. The stability limitations have been investigated by using a nonlinear analytical model for calculating the steady-state power transfer capability with various combinations of grid impedance values and levels of virtual impedance. The small-signal stability of the operating points has also been confirmed, and the validity of the stability improvements calculated from the analytical models has been verified by time-domain simulations.

## 5 Acknowledgments

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# 7 Appendices

## 7.1 Appendix 1: Non-linear system models

In this section, it is shown how the system from Fig. 1 can be represented by a non-linear state-space model. This model serves as a basis for calculating steady-state operating points and the steady-state stability limits of the system. Moreover, the model can be linearised into a small-signal state-space model for small-signal stability studies. The model development is based on [37], but is adapted to the investigated control system implementations and the synchronisation method proposed in this paper.

## 7.2 Electrical system model

The electrical system from Fig. 1 can be expressed by state-space equations in a synchronously rotating $dq$ reference frame as given by (2), where all bold symbols represent space vectors written in the form given by (3)

$$\frac{d\boldsymbol{i}_{cv}}{dt} = \frac{\omega_b}{l_f}\boldsymbol{v}_{cv} - \frac{\omega_b}{l_f}\boldsymbol{v}_o - \left(\frac{r_{l_f}\omega_b}{l_f} + j\cdot\omega_g\omega_b\right)\boldsymbol{i}_{cv}$$

$$\frac{d\boldsymbol{v}_o}{dt} = \frac{\omega_b}{c_f}\boldsymbol{i}_{cv} - \frac{\omega_b}{c_f}\boldsymbol{i}_g - j\cdot\omega_g\omega_b\cdot\boldsymbol{v}_o \qquad (2)$$

$$\frac{d\boldsymbol{i}_o}{dt} = \frac{\omega_b}{l_g}\boldsymbol{v}_o - \frac{\omega_b}{l_g}\boldsymbol{v}_g - \left(\frac{r_g\omega_b}{l_g} + j\cdot\omega_g\omega_b\right)\boldsymbol{i}_o$$

$$\boldsymbol{x} = x_d + j\cdot x_q \qquad (3)$$

Considering that the modulation index $\boldsymbol{m}$ used for the pulse-width modulation operation of the VSC is calculated as indicated in Fig. 1 from a division of the voltage reference from the control system by the actual dc voltage $v_{dc}$, the converter output voltage $\boldsymbol{v}_{cv}$ can be assumed to be equal to the reference voltage $\boldsymbol{v}_{cv}^*$, as expressed by (4). As this effectively decouples the ac side dynamics from the dc voltage of the VSC, the dynamics of the dc

side are not included in the modelling

$$m = \frac{v_{cv}^*}{v_{DC}}, \quad v_{cv} = m \cdot v_{DC} \rightarrow v_{cv} \simeq v_{cv}^* \tag{4}$$

### 7.3 Model of inner loop controllers

From the control system block diagram in Fig. 1, the voltage reference for the converter can be expressed by (5). In this equation, the integrator states of the PI current controllers are defined by (6), while the stabilising voltage reference from the active damping algorithm is given by (7). The applied scheme for active damping is based on the use of low-pass filters to extract the high frequency oscillating components in the voltage measurements as defined by (8) [31, 37]

$$v_{cv}^* = k_{pc}(i_{cv}^* - i_{cv}) + k_{ic} \cdot \boldsymbol{\gamma} + j \cdot l_1 \cdot \omega_{VSM} \cdot i_{cv} + v_o - v_{AD}^* \tag{5}$$

$$\frac{d\boldsymbol{\gamma}}{dt} = i_{cv}^* - i_{cv} \tag{6}$$

$$v_{AD}^* = k_{AD}(v_o - \boldsymbol{\varphi}) \tag{7}$$

$$\frac{d\boldsymbol{\varphi}}{dt} = \omega_{AD} \cdot v_o - \omega_{AD} \cdot \boldsymbol{\varphi} \tag{8}$$

### 7.4 Model of outer loop power controller

The active power flow from the VSC into the grid is defined by (9). A low-pass filter with an internal state variable defined by (10) is applied on the actual power flow before it is used as the feedback signal for the outer loop power controller indicated in Fig. 1. The active, $d$-axis, current reference resulting from the PI power controller is given by (11), where the internal state of the PI-controller is defined by (12)

$$p_o = \mathrm{Re}\left(v_o \cdot \breve{i}_o\right) = v_{o,d} \cdot i_{o,d} + v_{o,q} \cdot i_{o,q} \tag{9}$$

$$\frac{dp_m}{dt} = \omega_{LP,p} \cdot p_o - \omega_{LP,p} \cdot p_m \tag{10}$$

$$i_{cv,d}^* = k_{pp}(p^* - p_m) + k_{ip}\kappa_p \tag{11}$$

$$\frac{d\kappa_p}{dt} = p^* - p_m \tag{12}$$

### 7.5 Model of outer loop ac voltage controller

For the case of the ac voltage control, the voltage at the point of voltage measurements is controlled through the reactive current reference for the current controllers. Thus, the ac voltage amplitude feedback signal is defined as given by (13). A low-pass filter is also assumed to be included in the feedback loop for the ac voltage controller, and the filtered ac voltage measurement $v_{o,m}$ is given by (14). Considering that a negative value of the $q$-axis current will inject reactive power into the grid and by that increase the voltage amplitude, the $q$-axis current reference produced by the PI-controller for the ac voltage is given by (15), where the integrator state of the PI-controller is defined by (16)

$$\hat{v}_o = |v_o| = \sqrt{v_{o,d}^2 + v_{o,q}^2} \tag{13}$$

$$\frac{d\hat{v}_{o,m}}{dt} = \omega_{LP,v} \cdot \hat{v}_o - \omega_{LP,v} \cdot \hat{v}_{o,m} \tag{14}$$

$$i_{cv,q}^* = -k_{pv}(\hat{v}_o^* - \hat{v}_{o,m}) - k_{iv}\xi_v \tag{15}$$

$$\frac{d\xi_v}{dt} = \hat{v}_o^* - \hat{v}_{o,m} \tag{16}$$

### 7.6 Model of IC-PLL

The proposed IC-PLL can be modelled in the same way as the conventional PLL, as further described in [37]. Thus, the states of the low-pass filters used in the PLL are defined by (17). The only difference from the conventional PLL is that the voltage $\tilde{v}_{VI}$, calculated from the virtual impedance according to (1), is used as an input to the low-pass filter instead of the measured filter voltage $v_o$

$$\frac{dv_{PLL}}{dt} = -\omega_{LP,PLL} \cdot v_{PLL} + \omega_{LP,PLL} \cdot \tilde{v}_{VI} \tag{17}$$

The integrator state of the PI-controller used for tracking the grid frequency deviation is then defined by (18). Thus, the deviation of the PLL frequency from the grid frequency can be expressed by (19), and the phase angle deviation between the grid voltage vector and the orientation of the PLL can be defined by (20)

$$\frac{d\varepsilon_{PLL}}{dt} = \arctan\left(\frac{v_{PLL,q}}{v_{PLL,d}}\right) \tag{18}$$

$$\delta\omega_{PLL} = k_{p,PLL} \cdot \arctan\left(\frac{v_{PLL,q}}{v_{PLL,d}}\right) + k_{i,PLL} \cdot \varepsilon_{PLL} \tag{19}$$

$$\frac{d\delta\theta_{PLL}}{dt} = \delta\omega_{PLL} \cdot \omega_b \tag{20}$$

The resulting PLL phase angle displacement determines the orientation of the SRF used for the implementation of the VSC control system. The grid voltage can then be expressed in the corresponding SRF as given by (21)

$$v_g = \hat{v}_g \, e^{-j\delta\theta_{PLL}}. \tag{21}$$

### 7.7 Non-linear state-space models

A model of the overall system from Fig. 1 can be achieved by replacing the algebraic equations from the previous subsections into the differential equations. This results in a non-linear state-space model of Case 1 as given by (22). For Case 2, the system model will have two additional states according to (14) and (16), while the state equations for the $q$-axis current and for the integrator of the $q$-axis current controller will contain corresponding terms from the voltage control loop as given by (23). Thus a non-linear state-space model of Case 2 can be achieved by adding the state 17) and 18) and replacing 4) and 6) into (22) according to (23) (see equations (22) and (23) at bottom of the next page)

### 7.8 Steady-state system models

Steady-state system models for the two investigated cases can be directly obtained from (22) and (23) by setting all derivative terms to zero. The models are then reduced to a set of linear and non-linear algebraic equations that can be solved for the steady-state operating conditions of the system states as a function of the reference and input signals. These are the models used to calculate the steady-state power transfer limitations presented in Sections 3.1 and 3.3.

### 7.9 Appendix 2: Linearised small-signal state-space models

To verify the small-signal stability of the system in any operating point that can be calculated from the non-linear model, small-signal state-space models can be easily obtained by

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linearising (22) and (23). This will result in linearised small-signal models on the form given by (24). The state vector $\boldsymbol{x}$ and the input vector $\boldsymbol{u}$ are defined by (25) for Case 1 and by (26) for Case 2. These are the models that are used to identify the small-signal stability limits indicated in Fig. 4 and any other operating condition shown in the subsequent figures. The resulting model can also be used to analyse the dynamic response of the system for small deviations around any operating point, as for instance the dynamics observed when the system is settling around a new operating point as a consequence of the power reference step simulated in Fig. 10

$$\Delta\dot{\boldsymbol{x}} = \boldsymbol{A}\cdot\Delta\boldsymbol{x} + \boldsymbol{B}\cdot\Delta\boldsymbol{u} \tag{24}$$

$$\boldsymbol{x} = \begin{bmatrix} v_{o,d} & v_{o,q} & i_{cv,d} & i_{cv,q} & \gamma_d & \gamma_q & i_{o,d} & i_{o,q} & \varphi_d & \varphi_q \\ v_{PLL,d} & v_{PLL,q} & \varepsilon_{PLL} & \delta\theta_{PLL} & p_m & \kappa_p \end{bmatrix}^{\mathrm{T}} \tag{25}$$

$$\boldsymbol{u} = \begin{bmatrix} i_{cv,q}^* & p^* & \hat{v}_g & \omega_g \end{bmatrix}^{\mathrm{T}}$$

1) $\dfrac{\mathrm{d}v_{o,d}}{\mathrm{d}t} = \omega_b\omega_g v_{o,q} + \dfrac{\omega_b}{c_f}i_{cv,d} - \dfrac{\omega_b}{c_f}i_{o,d}$,  2) $\dfrac{\mathrm{d}v_{o,q}}{\mathrm{d}t} = -\omega_b\omega_g v_{o,d} + \dfrac{\omega_b}{c_f}i_{cv,q} - \dfrac{\omega_b}{c_f}i_{o,q}$

3) $\dfrac{\mathrm{d}i_{cv,d}}{\mathrm{d}t} = -\dfrac{\omega_b k_{AD}}{l_f}v_{o,d} - \dfrac{\omega_b(k_{pc}+r_f)}{l_f}i_{cv,d} + \dfrac{\omega_b k_{ic}}{l_f}\gamma_d + \dfrac{\omega_b k_{AD}}{l_f}\varphi_d - \dfrac{\omega_b k_{pc}k_{pp}}{l_f}p_m + \dfrac{\omega_b k_{pc}k_{ip}}{l_f}\kappa_m$

$\qquad - \omega_b k_{i,PLL}i_{cv,q}\varepsilon_{PLL} + \omega_b k_{p,PLL}i_{cv,q}\tan^{-1}\left(\dfrac{v_{PLL,q}}{v_{PLL,d}}\right) + \dfrac{\omega_b k_{pc}k_{pp}}{l_f}p^*$

4) $\dfrac{\mathrm{d}i_{cv,q}}{\mathrm{d}t} = -\dfrac{\omega_b k_{AD}}{l_f}v_{o,q} - \dfrac{\omega_b(k_{pc}+r_f)}{l_f}i_{cv,q} + \dfrac{\omega_b k_{ic}}{l_f}\gamma_q$

$\qquad + \dfrac{\omega_b k_{AD}}{l_f}\varphi_d + \omega_b k_{i,PLL}i_{cv,d}\varepsilon_{PLL} + +\omega_b k_{p,PLL}i_{cv,d}\tan^{-1}\left(\dfrac{v_{PLL,q}}{v_{PLL,d}}\right) + \dfrac{\omega_b k_{pc}}{l_f}i_{cv,q}^*$

5) $\dfrac{\mathrm{d}\gamma_d}{\mathrm{d}t} = -i_{cv,d} - k_{pp}p_m + k_{ip}\kappa - k_{pp}p^*$,  6) $\dfrac{\mathrm{d}\gamma_q}{\mathrm{d}t} = -i_{cv,q} + i_{cv,q}^*$

7) $\dfrac{\mathrm{d}i_{o,d}}{\mathrm{d}t} = \dfrac{\omega_b}{l_g}v_{o,d} - \dfrac{\omega_b r_g}{l_g}i_{o,d} + \omega_b\omega_g i_{o,q} - \dfrac{\omega_b\hat{v}_g\cos(\delta\theta_{PLL})}{l_g}$

8) $\dfrac{\mathrm{d}i_{o,q}}{\mathrm{d}t} = \dfrac{\omega_b}{l_g}v_{o,q} - \omega_b\omega_g i_{o,d} - \dfrac{\omega_b r_g}{l_g}i_{o,q} + \dfrac{\omega_b\hat{v}_g\sin(\delta\theta_{PLL})}{l_g}$

$\qquad\qquad\qquad\qquad\qquad\qquad\qquad\qquad\qquad\qquad\qquad\qquad\qquad\qquad\qquad\quad$ (22)

9) $\dfrac{\mathrm{d}\varphi_d}{\mathrm{d}t} = \omega_{AD}v_{o,d} - \omega_{AD}\varphi_d$  10) $\dfrac{\mathrm{d}\varphi_q}{\mathrm{d}t} = \omega_{AD}v_{o,q} - \omega_{AD}\varphi_q$

11) $\dfrac{\mathrm{d}v_{PLL,d}}{\mathrm{d}t} = \omega_{LP,PLL}v_{o,d} - \omega_{LP,PLL}r_v i_{o,d} - \omega_{LP,PLL}v_{PLL,d} + \omega_{LP,PLL}\omega_g l_v i_{o,q}$

$\qquad + \omega_{LP,PLL}k_{i,PLL}l_v i_{o,q}\varepsilon_{PLL} + \omega_{LP,PLL}k_{p,PLL}l_v i_{o,q}\tan^{-1}\left(\dfrac{v_{PLL,q}}{v_{PLL,d}}\right)$

12) $\dfrac{\mathrm{d}v_{PLL,q}}{\mathrm{d}t} = \omega_{LP,PLL}v_{o,q} - \omega_{LP,PLL}r_v i_{o,q} - \omega_{LP,PLL}v_{PLL,q} - \omega_{LP,PLL}\omega_g l_v i_{o,d}$

$\qquad - \omega_{LP,PLL}k_{i,PLL}l_v i_{o,d}\varepsilon_{PLL} - \omega_{LP,PLL}k_{p,PLL}l_v i_{o,d}\tan^{-1}\left(\dfrac{v_{PLL,q}}{v_{PLL,d}}\right)$

13) $\dfrac{\mathrm{d}\varepsilon_{PLL}}{\mathrm{d}t} = \tan^{-1}\left(\dfrac{v_{PLL,q}}{v_{PLL,d}}\right)$,  14) $\dfrac{\mathrm{d}\delta\theta_{PLL}}{\mathrm{d}t} = \omega_b k_{p,PLL}\tan^{-1}\left(\dfrac{v_{PLL,q}}{v_{PLL,d}}\right) + \omega_b k_{i,PLL}\varepsilon_{PLL}$

15) $\dfrac{\mathrm{d}p_m}{\mathrm{d}t} = -\omega_{LP,p}p_m + \omega_{LP,p}v_{o,d}i_{o,d} + \omega_{LP,p}v_{o,q}i_{o,q}$,  16) $\dfrac{\mathrm{d}\kappa_p}{\mathrm{d}t} = -p_m + p^*$

4) $\dfrac{\mathrm{d}i_{cv,q}}{\mathrm{d}t} = -\dfrac{\omega_b k_{AD}}{l_f}v_{o,q} - \dfrac{\omega_b(k_{pc}+r_f)}{l_f}i_{cv,q} + \dfrac{\omega_b k_{ic}}{l_f}\gamma_q + \dfrac{\omega_b k_{AD}}{l_f}\varphi_d$

$\qquad + \omega_b k_{i,PLL}i_{cv,d}\varepsilon_{PLL} + +\omega_b k_{p,PLL}i_{cv,d}\tan^{-1}\left(\dfrac{v_{PLL,q}}{v_{PLL,d}}\right) - \dfrac{\omega_b k_{pc}k_{pv}}{l_f}\hat{v}_{o,m} + \dfrac{\omega_b k_{pc}k_{iv}}{l_f}\xi_v + \dfrac{\omega_b k_{pc}k_{pv}}{l_f}\hat{v}_o^*$

$\qquad\qquad\qquad\qquad\qquad\qquad\qquad\qquad\qquad\qquad\qquad\qquad\qquad\qquad\qquad\quad$ (23)

6) $\dfrac{\mathrm{d}\gamma_q}{\mathrm{d}t} = -i_{cv,q} + k_{pv}\hat{v}_{o,m} - k_{iv}\xi_v + k_{pv}\hat{v}_o^*$

17) $\dfrac{\mathrm{d}\hat{v}_{o,m}}{\mathrm{d}t} = \omega_{LP,v}\sqrt{v_{o,d}^2 + v_{o,q}^2} - \omega_{LP,v}\hat{v}_{o,m}$,  18) $\dfrac{\mathrm{d}\xi_v}{\mathrm{d}t} = -\hat{v}_{o,m} + \hat{v}_o^*$

$$x = \begin{bmatrix} v_{o,d} & v_{o,q} & i_{cv,d} & i_{cv,q} & \gamma_d & \gamma_q & i_{o,d} & i_{o,q} & \varphi_d & \varphi_q \end{bmatrix}$$
$$\begin{matrix} v_{PLL,d} & v_{PLL,q} & \varepsilon_{PLL} & \delta\theta_{PLL} & p_m & \kappa_p & \hat{v}_{o,m} & \xi_v \end{bmatrix}^T \quad (26)$$
$$u = \begin{bmatrix} \hat{v}_o^* & p^* & \hat{v}_g & \omega_g \end{bmatrix}^T$$

## 7.10   Appendix 3: System parameters

This section is included to document the system parameters used for the presented investigations.

## 7.11   Parameters used for analysing system characteristics

The electrical parameters and the controller settings used for all analysis of system stability limits presented in this paper are listed in Table 1. The grid impedance and the virtual impedance are not listed in the table, as their values are varied for the different investigations.

## 7.12   PLL tuning

For the eigenvalue analysis in Section 3.2, the PI-controller parameters of the PLLs have been tuned according to the SO criterion in a similar way as discussed in [35]. This approach is based on the PLL open-loop transfer function, $h_{OL,PLL}(s)$ which can be approximated by (27) when linearising the inverse tangent function. Considering the current-dependent impedance terms as a disturbance to the PLL, the transfer function for the IC-PLL will be the same as for the conventional PLL.

$$h_{OL,PLL}(s) \simeq \underbrace{k_{p,PLL} \frac{1 + T_{i,PLL} \cdot s}{T_{i,PLL} \cdot s}}_{PI-controller} \cdot \underbrace{\frac{\omega_b}{s}}_{VCO} \cdot \underbrace{\frac{1}{1 + T_f \cdot s}}_{Filter},$$
$$T_f = \frac{1}{\omega_{LP,PLL}} \quad (27)$$

**Table 1**   Parameters of investigated system configuration

| Parameter | Value | Parameter | Value |
|---|---|---|---|
| rated voltage $V_{S,LL,RMS}$ | 220 kV | rated angular frequency $\omega_b$ | $2\pi \times 50$ Hz |
| rated power $S_b$ | 1200 MVA | filter inductance $l_f$ | 0.08 pu |
| current controller gains, $k_{pc}$, $k_{ic}$ | 1.27, 14.25 | filter resistance $r_{lf}$ | 0.003 pu |
| power controller gains, $k_{pp}$, $k_{ip}$ | 0.10, 50,0 | filter capacitance $c_f$ | 0.074 pu |
| power measurement filter, $\omega_{LP,p}$ | 200 rad/s | grid voltage $\hat{v}_g$ | 1.0 pu |
| ac voltage controller gains, $k_{pv}$, $k_{iv}$ | 0.1, 5.0, | PLL low-pass filter, $\omega_{LP,PLL}$ | 200 rad/s |
| ac voltage amplitude filter, $\omega_{LP,v}$ | 10 rad/s | PLL gains, $k_{p,PLL}$, $k_{i,PLL}$ | 0.05, 2.53 |

Applying the SO criterion to the transfer function of (27) results in expressions for the PI-controller parameters as given by (28) [38]. In this equation, $\zeta$ is the damping factor of the closed-loop transfer function resulting from (27) and $a$ is a design factor that can be freely selected to obtain a desired trade-off between damping and bandwidth of the PLL.

$$k_{p,PLL} = \frac{1}{a \cdot \omega_b \cdot T_{f,PLL}} = \frac{\omega_{LP,PLL}}{a \cdot \omega_b}, \quad a = 2\zeta + 1$$

$$T_{i,PLL} = a^2 \cdot T_{f,PLL} \rightarrow k_{i,PLL} = \frac{k_{p,PLL}}{T_{i,PLL}} = \frac{\omega_{LP,PLL}^2}{a^3 \cdot \omega_b \cdot T_{f,PLL}^2} \quad (28)$$

For the results in Section 3.2, $a$ is specified to be 3, corresponding to a damping factor $\zeta$ of 1 for the PLL closed-loop transfer function. For this tuning, it can be demonstrated that the effective closed-loop bandwidth of the PLL transfer will be about 0.55 times $\omega_{LP,PLL}$. Thus, the bandwidth of the PLL can be adjusted by changing the $\omega_{LP,PLL}$ or the corresponding filter time constant $T_{f,PLL}$.

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