(normal/ $\overline{\text{test}}$), and maintains $T/\bar{D}$ (test/ $\overline{\text{diagnose}}$) to 1. When the circuit is not in the DTM, the external input T_{in} directly controls the test process switching between normal operation $N/\bar{T}$ = 1 (no-test mode) and the normal test mode. Once in the DTM, T_{in} is isolated from $N/\bar{T}$ and the control unit drives the test.

Table 1: Operation modes of test architecture

$N/\bar{T}$	$T/\bar{D}$	Test mode
1	1	Normal operation (no test)
0	1	Normal test mode (NTM)
0	0	Diagnose test mode (DTM)

The active test mode is internally defined by $N/\bar{T}$ and $T/\bar{D}$ as shown in Table 1. In normal operation $N/\bar{T}$ is high and drives the set input of the DCR, setting all p_is to 1 and turning on all the sub-switches. When $N/\bar{T}$ goes to zero, while $T/\bar{D}$ = 1, the DCR is resettled turning off all the sub-switches. This causes the BIC sensor to sense all the CUT partitions and test the whole circuit. The multiplexer placed between the BIC sensor and the circuit output is controlled by ORing $N/\bar{T}$ and $T/\bar{D}$. The MUX connects the BIC sensor output to the circuit output test *pin* T_{out} when the circuit is not in the DTM.

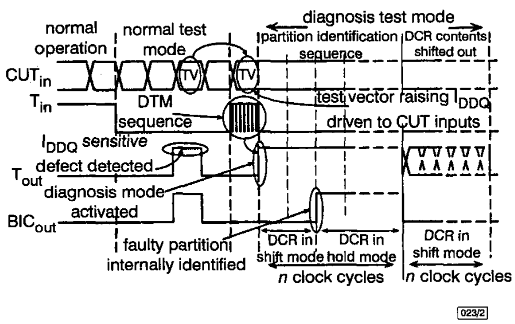

Fig. 2 *Input and output sequence for normal test mode and diagnosis test mode*

When the control unit detects the diagnose input sequence, it sets the DCR (p_i = 1 for all i), and drives the architecture to the DTM by setting $N/\bar{T}$ = 0 and $T/\bar{D}$ = 0. This switches the MUX driving T_{out} to the DCR output therefore driving the external output to a logic 1, to signal that the device is in DTM (see Fig. 2). The control unit then sets the DCR to the shift mode, starting a partition identification sequence that serially passes a single 0 through the DCR during n cycles using p_{in}. The DCR sequence passes all DCVs from D_1 to D_n into the DCR, measuring the quiescent current through each partition separately (when the DCV D_i is in the DCR, only the partition P_i is sensed by the BIC sensor).

The DCR is in the shift mode when the CUT enters DTM until the BIC sensor output goes high and stops the shift process. The BIC sensor output will go high when the partition passing the elevated quiescent current is monitored by the sensor, given that the test vector T that activated the defect in the NTM is driving the CUT inputs. The DCV in the DCR (D_j) when the BIC sensor output is activated identifies partition P_j as the partition which increases the quiescent current. When this happens, the BIC sensor output stops shifting the DCR. After n cycles of the partition identifying sequence, the control unit resets the BIC sensor and shifts out the DCR contents. A total of n additional clock cycles are required to completely shift out the DCV that identifies the partition passing the elevated quiescent current.

Reduced fault diagnosis procedure: The diagnosis test mode provides a DCV that identifies one partition as that passing the elevated quiescent current. Such a partition will be referred to as the failing partition (FP). The defect causing a given partition to be the FP may not physically belong to such a partition. Therefore, logic-based fault diagnosis must consider all faults in the FP plus additional circuitry. The FP and such additional circuitry will be referred to as the target partition (TP). Once the TP associated with the FP is known, a logic fault diagnosis can be performed considering only faults in the TP and not in the whole CUT. Assuming a uniform distribution of defects included in the fault list through all the partitions, a reduction in the number of faults of order n is obtained. The approach proposed is general and is not restricted to any particular fault diagnosis heuristic.

The extension of the FP to the TP is obtained including all the circuitry that may have defects that could induce an elevated quiescent current through the FP. These faults can be classified into three categories:

(i) *Category 1: Faults in FP domain:* These faults would appear in the fault list of a circuit being the FP alone (without the remaining partitions).

(ii) *Category 2: Logic extended domain:* This is composed of faults at gates in the logic border of the FP, i.e. gates that even drive or are driven by nodes of the FP. They are included in the TP because although the defect is outside the FP, the current path goes through the V_{DD} or ground rails of the FP. A defect physically far away from the partition increasing the current in the CUT may even be the source of such a current increase.

An example of such a defect would be a gate oxide short in the pMOS transistor of a gate driven by some output of the FP. Since the gate oxide short is activated when the faulty transistor gate is connected to ground [3], the current caused by the defect would be detected when the BIC sensor senses partition P_i while the defect causing such a leakage does not belong to such a partition.

(iii) *Category 3: Layout border domain:* This is composed of those defects that involve nodes physically close enough to nodes in the FP, so that a particle defect can short them.

Conclusions: An architecture for significantly enhancing IC fault diagnosis which is independent of the fault diagnosis heuristic has been presented. The method is applicable to circuits tested with the I_{DDQ} method using a BIC sensor circuit and is based on hardware partitioning. The diagnosis test mode is used to obtain a significant reduction in the fault list providing a reduction in the number of faults by a factor equal to the number of partitions.

Acknowledgments: This work has been supported by the Spanish 'Comisión interministerial de Ciencia y Tecnología' under the project CICYT-TIC98-0284.

10 May 1999
Electronics Letters Online No: 19990797
DOI: 10.1049/el:19990797

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Circuit model for slotline-to-coplanar waveguide asymmetrical transitions

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A new 'circuit-model' for slotline-to-coplanar waveguide asymmetrical transitions is presented and applied to the design of slotline resonators. The model, based on the separation of coplanar-waveguide (CPW) modes into two different ports, overcomes limitations of previous models because it explains the transition behaviour even if CPW air-bridges are not used.

Introduction: Slotline-to-coplanar waveguide transitions are widely used in uniplanar hybrid and monolithic (MMIC) microwave integrated circuits, such as phase inverters [1], frequency doublers [2], mixers [3, 4] and amplifiers [5]. The coplanar waveguide (CPW) is a multimode waveguide supporting two fundamental modes, the coplanar even-mode (CEM), or coplanar-mode, and coplanar odd-mode (COM), or slotline mode. Slotline supports only one fundamental (slotline) mode. A particular kind of slotline-to-CPW (asymmetrical) transition is shown in Fig. 1, in which one of the CPW slots is connected to the slotline, and the other is either short-circuited (Fig. 1*a*), or open-ended (Fig. 1*b*), or loaded with an arbitrary impedance (Fig. 1*c*).

In [1 – 5], the open-ended configuration of Fig. 1*b* is used to transform the slotline mode into the CEM mode or vice versa; to prevent excitation of the COM at the CPW side of the transition, air-bridges connecting the CPW ground planes are included. Other applications, such as slotline resonators (see Fig. 4) used in bandstop filters [6], require two slotline-to-CPW asymmetrical transitions, as shown in Fig. 1, but without air-bridges. Therefore, both modes, CEM and COM, are excited at the CPW section (resonator), and a detailed study of the resonance conditions requires a circuit-model for the transition in which both modes are taken into account. However, the circuit models proposed in [1 – 5] cannot be applied to the transitions without the air-bridges shown in Fig. 1, because they always assume an open-ended transition such as in Fig. 1*b* in which the COM is not excited due to the inclusion of air-bridges.

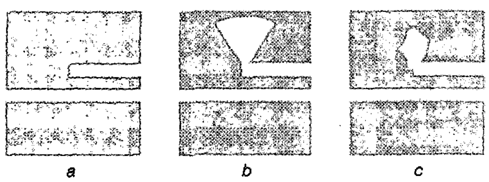

Fig. 1 *Slotline-to-CPW asymmetrical transmission*

a Short-circuited CPW slot
b Open-ended CPW slot
c CPW slot loaded with arbitrary impedance

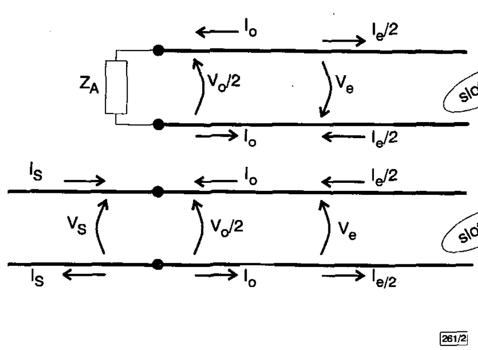

Fig. 2 *Voltages and currents at slotline-to-CPW transition*

In this Letter, a new three-port circuit model for asymmetrical slotline-to-CPW transitions, as shown in Fig. 1, is proposed. In contrast to previous works [1 – 5], we study a general case in which CPW air-bridges are not connected and a generic terminating impedance for the slot is used instead of an open circuit. Therefore, both CPW modes, CEM and COM, are excited, and other transitions such as those in Figs. 1*a*, and *c* can be analysed. The model is based on the separation of modes (slotline, CEM and COM) into different ports and, therefore, it provides a quantitative analysis of mode conversion (from slotline mode to CEM and COM, and vice versa) when the CPW section is loaded with general slot-terminating planar structures that present different responses to each mode. Transitions with air-bridges at the CPW section, such as those presented in [1 – 5], can also be analysed as a particular case. Validation of the model is achieved through its application to a double transition (slotline resonator) designed at K-band (18–26.5GHz).

Model derivation: Consider the asymmetrical slotline-to-CPW transition shown in Fig. 1, realised by connecting one of the slots of the CPW to an equal slotwidth slotline. The other CPW slot is loaded with any generic impedance, Z_A (Fig. 1*c*). As a particular case, the load can be either a short circuit (Z_A = 0) as in Fig. 1*a*,

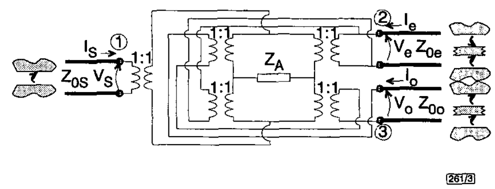

Fig. 3 *Circuit-model proposed for slotline-to-CPW asymmetrical transition*

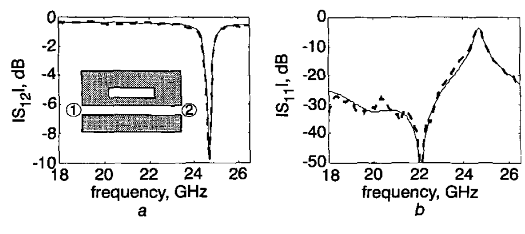

Fig. 4 *Slotline resonator S-parameters*

a Magnitude of S_{12}
b Magnitude of S_{11}
– – – – measured
——— simulated

or an open circuit ($Z_A \to \infty$) as in Fig. 1*b*. Since the CPW is excited asymmetrically by the slotline-mode, both modes (CEM and COM) are generated at the transition. Each CPW slot can be seen as a transmission line propagating both CEM and COM (Fig. 2). The slot voltages and currents at the transition plane, V_A, V_B, I_A, I_B are written as a function of the CEM and COM voltages and currents V_o, V_e, I_o, I_e:

$$V_A = (V_o/2) - V_e \qquad V_B = (V_o/2) + V_e \tag{1}$$

$$I_A = I_o - (I_e/2) \qquad I_B = I_o + (I_e/2) \tag{2}$$

By substituting eqns. 1 and 2 in the boundary conditions (Kirchoff laws) at the transition plane, $V_A = I_A \cdot Z_A$, $V_B = V_S$, $I_B + I_S = 0$, the following equation system is obtained for the normalised slotline, CEM and COM incident and reflected waves at the transition plane, a_s, a_e, a_o, and b_s, b_e, b_o, respectively

$$\begin{bmatrix} b_s \\ b_e \\ b_o \end{bmatrix} = \frac{1}{9(Z_A+A_0)} \begin{bmatrix} Z_A - Z_0 & 4(Z_0+2Z_A) & 4(2Z_0+Z_A) \\ 4(Z_0+2Z_A) & Z_A - 7Z_0 & 4(Z_0-Z_A) \\ 4(2Z_0+Z_A) & 4(Z_0-Z_A) & 7Z_A - Z_0 \end{bmatrix} \cdot \begin{bmatrix} a_s \\ a_e \\ a_o \end{bmatrix} \tag{3}$$

where $a_\alpha = (V_\alpha + Z_o I_\alpha)\cdot(4Z_o)^{-1/2}$, $b_\alpha = (V_\alpha - Z_o I_\alpha)\cdot(4Z_o)^{-1/2}$ ($\alpha = s, e, o$), and Z_o is a real arbitrary impedance to which the normalised waves and the 3 × 3 *S*-parameter matrix are referred. The *S*-matrix obtained in eqn. 3 leads to the circuit model proposed in Fig. 3 composed of the impedance Z_A connected to ideal transformers. The relevant features of the new model are:

(i) The two-port transition (one slotline input port and one multimode CPW output port) is modelled as a three-port device that separates the slotline, CEM and COM contributions into different singlemode ports, namely, one slotline input port, one CPW output port propagating only the COM (with characteristic impedance Z_{oo}), and one CPW output port propagating only the CEM (with characteristic impedance Z_{oe}).

(ii) Therefore, planar structures that present different responses to each mode (such as other slotline-to-CPW transitions and air-bridges) can be easily connected by loading the ports in Fig. 3 with proper impedances. This feature is of great importance for analysing slotline resonators (as in Fig. 4) because, since the resonator has different electrical lengths for either mode (CEM and COM), their contribution to the resonance must be separated.

(iii) In general, whenever a mode is cut off, its effect is also easily included by terminating the appropriate port in Fig. 3 with a reactive impedance.

(iv) As a particular case, the transitions presented in [1 – 5] with an open-ended slot (Fig. 1*b*) and an air-bridge at the transition plane can be analysed by connecting a short-circuit (air-bridge) to port 3 in Fig. 3, and letting $Z_A \to \infty$.

(v) Since the model contains circuit elements, it enables the energy transfer from one mode to any other mode in the transition to be quantitatively analysed, and can be easily implemented in microwave CAD.

Model application and experimental validation: The proposed model has been applied to a K-band (18–26.5GHz) slotline resonator fabricated on CuClad 217, ε_r = 2.17, thickness = 0.254mm. (see Fig. 4*a*) and placed in the *E*-plane of a WR-42 rectangular waveguide. The resonator consists of a CPW section loaded with two slotline-to-CPW asymmetrical transitions ($Z_A \simeq 0$ in Fig. 2). The slotline width and resonator slotwidth are 0.2mm. The resonator length is 4.7mm. The separation between the slotline and resonator slot is 0.1mm. Figs. 4*a* and *b* show a composition of its simulated *S*-parameters (obtained using the model shown in Fig. 3 for each transition) with its measured *S*-parameters. The excellent agreement between simulations and measurements (the model accurately predicts the resonance frequency) demonstrates the validity of the model and applicability.

Conclusions: A new 'circuit model' for slotline-to-coplanar waveguide asymmetrical transitions that separates the contributions of CPW modes into different ports has been proposed. The model overcomes limitations of previous models, because it enables a general case to be analysed in which air-bridges are not present, and slot-terminating impedances other than an open circuit can be used. It has been successfully applied to the analysis of slotline resonators, showing excellent agreement with experimental results.

Acknowledgment: This work has been supported by the research project TIC97-1129-C04-04 financed by the Spanish Government CICYT.

21 May 1999

Electronics Letters Online No: 19990779

DOI: 10.1049/el:19990779

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Cascaded $\chi^{(2)}$ wavelength converter in $LiNbO_3$ waveguides with counter-propagating beams

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A wideband wavelength converter is presented which is based on a cascaded second-order nonlinearity in periodically-poled $LiNbO_3$ waveguides pumped at 1.5µm. The converter uses counter-propagating beams in order to improve conversion efficiency and pump rejection. An internal conversion efficiency of –10dB and a conversion bandwidth of 68nm have been obtained in a 4cm long device.

Introduction: Wavelength conversion at 1550nm is carried out in a variety of ways [1]. One attractive way of implementing wavelength conversion is by using difference frequency generation (DFG) in a nonlinear optical medium [2 – 4]. This process is instantaneous and optically transparent, has a negligible noise floor, and has no intrinsic frequency chirp. Multiple channels can also be converted simultaneously with equal efficiencies. However, DFG-based wavelength converters require a singlemode 50–150mW pump operating at roughly half the signal wavelength, i.e. ~780nm [2 – 4]. This also implies mode-matching complications in the nonlinear waveguide due to the use of very different wavelengths. A solution to this problem by the use of a cascaded $\chi^{(2)}$ process ($\chi^{(2)}$:$\chi^{(2)}$) has been proposed [5] and demonstrated [6] in periodically poled $LiNbO_3$ (PPLN) waveguides. We recently demonstrated a device based on a cascaded interaction with internal conversion efficiency of –8dB, pumped by a laser also in the 1550nm region [7]. The implementation of this device used co-propagating pump and signal beams. Thus, considerable pump power is present at the output of the waveguide and consequently an appropriate blocking filter must be used. In this Letter, we report a wavelength converter that uses counter-propagating pump and signal beams. This configuration improves the overall conversion efficiency and alleviates the pump rejection requirements.

The ($\chi^{(2)}$:$\chi^{(2)}$) device using counter-propagation beams is implemented by launching the pump and signal beams from opposite facets of the waveguide and coating one facet with a dichroic dielectric mirror that reflects the second harmonic beam back into the waveguide. In this device, the pump at frequency ω_p is up-converted to frequency $2\omega_p$ by second harmonic generation (SHG). The generated $2\omega_p$ is reflected back into the waveguide and mixes with the input signal ω_s for co-propagating phase-matching to generate a wavelength shifted output $\omega_{out} = 2\omega_p - \omega_s$ by DFG. Phase-matching between interacting waves for both SHG and DFG is required, and can be accomplished by choosing an appropriate quasi-phasematching (QPM) grating period. Phasematching with counter-propagating beams is in principle possible but the poling period required is extremely small (< 1µm) and cannot therefore be easily achieved in a practical device.

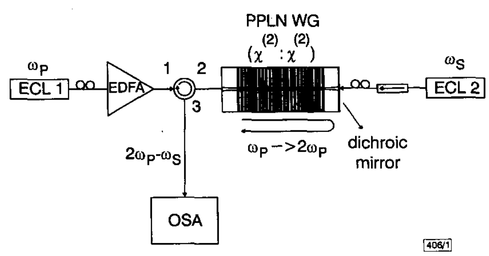

Fig. 1 *Experimental setup for counter-propagating beam wavelength converter based on cascaded $\chi^{(2)}$ nonlinearity*

ECL: external cavity laser; PPLN WG: periodically poled $LiNbO_3$ waveguide; EDFA: erbium-doped fibre amplifier; OSA: optical spectrum analyser

Fabrication: We fabricated the waveguides by annealed proton exchange in PPLN. The device used in this experiment is 4cm long, has a QPM period of 14.8µm, waveguide width of 12µm, proton exchange depth of 0.7µm, and was annealed for 26h at 325°C. We can tune the pump wavelength by using waveguides with different QPM period and/or temperature tuning. The