ELECTRONIC AND PHOTONIC SWITCHING IN THE ATM ERA[1]

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ABSTRACT

Broadband networks require high-capacity switches in order to properly manage large amounts of traffic fluxes. Electronic and photonic technologies are being used to achieve this objective both allowing different multiplexing and switching techniques. Focusing on the Asynchronous Transfer Mode (ATM), the inherent different characteristics of electronics and photonics makes different architectures feasible. In this paper, different switching structures are described, several ATM switching architectures which have been recently implemented are presented and the implementation characteristics discussed. Three diverse points of view are given from the electronic research, the photonic research and the commercial switches. Although all the architectures where successfully tested, they should also follow different market requirements in order to be commercialised. This characteristics are presented and the architectures projected over them to evaluate their commercial capabilities.

INTRODUCTION

Multimedia communications are expected to replace telephony as the predominant communications service. The current needs of 6.4 Gb/s of telephony to serve one million people may grow to 600 Gb/s when high definition MPEG video services (6 Mb/s) are deployed. Thus, very high-capacity (Tb/s) switching will be required in the future. ATM is the fast packet switch technique emerged with the aim of service integration and bandwidth gain.

There is no doubt about the leadership of photonics for the transport functions of Tb/s bandwidths. This is possible due to the unique properties of photonics: 25 THz bandwidth, low crosstalk between the photonic channels and strong interaction between light and semiconductors. Instead, switching functions are solidly based on electronics —high-speed electronic ATM switches are already commercially mature thanks to an extensive effort in function implementation (hardware-software codesign and VHDL automatic synthesis) and high density gate and interconnection capabilities (multi-chip modules). Nevertheless, a significant research effort in photonic switching implementation has been done in spite of the current poor processing capacity of the photonic technology. The scope is to surpass the speed limit of electronics (about 10 Gb/s) at a reasonable cost and to avoid the electro-optic conversion bottle-neck towards an all optical network. An ATM optical switch with electronic control is a first step. The emerging consensus is that switching at or above ATM should be done electronically, so photonics may still have a role in ATM switching.

In (1), complexity factors for electronic switching, traffic demands and optical trunk switching are discussed for broadband networks. Our purpose is to extend (1) providing a review for the ATM panorama, giving comparisons for future research developments focusing on architectural and commercial issues.

This paper is organised as follows: Section 2 identifies the generic switching functions. Section 3 projects them over both the electronic and photonic technologies. Section 4 describes the generic switch architectures. Section 5 presents the most recent implementations from the research and the commercial communities. Section 6 evaluates these implementations from different points of view. Finally, Section 7 concludes this paper.

GENERIC SWITCHING FUNCTIONS

Multiplexing. In order to properly manage large information flows, traffic concentration in different multiplexing layers is required at present, although the number of layers may be reduced. The interchange of information between different channels of the same layer is carried out by different switching functions according to the multiplexing

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strategy. There is a different technology and protocol for every layer which gives different characteristics to each one. A possible multiplexing hierarchy is shown in Figure 1. In this example, the multiplexing strategies are WDM (Wavelength Division Multiplexing), TDM (Time Division Multiplexing) and ATDM (Asynchronous TDM). WDM, uses the optical bandwidth split into fixed, non-overlapping spectral bands that are transparent to the bit-rate and code format. Conversely TDM divides the transmission time into frames, which in turn are split into slots and then one or more slots are assigned to a channel. TDM over multi-channel WDM will be based on the ITU (International Telecommunications Union) wavelengths standards. Specifications started in early 1997 and are not still finished, but a clear picture of the wavelength grid has emerged with a channel spacing fixed to multiples of 100 GHz within the 1.5 μm wavelength window. As can be seen, TDM over WDM has a fixed capacity per channel and the allocated resources cannot be exceeded when necessary and are wasted when not used. ATDM solves this problem by using a statistical allocation of the transmission capacity to a channel where information packets are multiplexed.

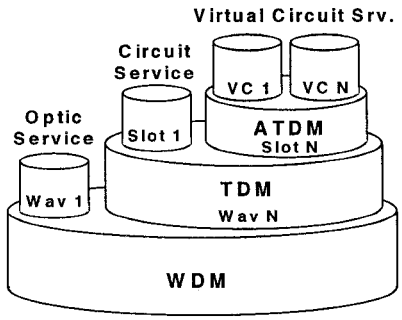


Figure 1. Multiplexing hierarchy.

Switching. The fundamental purpose of switching is the reconfiguration of routes and their capacities as the traffic demands across a network change over time. Any switch has to perform two basic functions irrespective of transfer mode: demultiplexing incoming channels according to a given routing pattern and multiplexing the channels on to the outgoing link. The switch is thus built for a particular multiplexing and routing strategy. The networks can be categorised according to the combination of these functions in circuit-switching (fixed capacity and route), virtual circuit-switching (statistical capacity and fixed route) and datagram-switching networks (statistical capacity and route). This paper is focused on ATM virtual circuit-switching.

Two different switching structures are possible, namely space-division and shared medium. Space-division interconnection structure where an input has dedicated links to all outputs and thus requires demultiplexing before multiplexing. Shared medium structure where all inputs share a common link to all outputs and thus multiplexing comes before demultiplexing. Basic switching elements are based on these structures and can be interconnected into a large switching fabric. Besides mux/demux, both structures require routing functions. The routing functions are static for WDM and TDM once the connection is made, but it is not static for ATDM since packets do not follow any order. Mux/demux for WDM channels require combinators and selectors for the different wavelengths, while TDM requires synchronisation to avoid channel overlapping and ATDM requires buffering to solve packet contention.

Electronic and Photonic Technologies State Of The Art

From above, for a general switching system, three main functions can be identified:

1. Temporal mux/demux with buffering and synchronisation.
2. Wavelength mux/demux with wavelength conversion (to improve routing).
3. Space-division switching.

The ATM switch architectures use these functions when they are available for fast packet switching (2). TABLE 1 summarises the state of the art for both electronic and photonic technologies when implementing the previous functions. Mature electronic technologies are currently available after decades of evolution. Electronic switching has mostly adopted CMOS technology, which allows for high hardware complexity, although with a line speed limited to 155 Mb/s (STM-1) in practice. Higher line speeds are achieved by either using parallel buses or more power consuming electronics than CMOS like GaAs. These technologies can implement all previous functions except for the wavelength domain. High-level integration is possible for space-division switching, which is only limited by currently available chip packages. Time division switching is limited by the electronic bandwidth, which is about 10 Gb/s.

One of the reasons for the slow progress of photonic penetration in switching is the immaturity of the photonic device technology, comparable to the state of electronics in the '60s. However, rapid progress in this field is being made specially in the development of integrated photonics. Optical TDM has contributed the last advances in temporal multiplexing and demultiplexing functions while buffering is solved using simple fiber delay lines. Synchronisation is not a completely solved problem yet. WDM and spatial switching technologies have evolved quickly and seem to be ready to be introduced in commercial devices. Their components can already operate at

ATM cell level as demonstrated in Section 4. For further information about the subjects of this section refer to (1) and (2).

D	Func.	Electronic tech.		Photo-elec. tech.		Photonic tech.	
T	Mux	A	Clock circuits Si-GaAs	C	On-off lasers	B	Short pulse combiner
	Demux	A	Clock circuits Si-GaAs	C	On-off receivers	B	Non linear loop mirror
	Buffer	A	Transistor memories	E		C	Fiber delay lines
	Synch.	A	Clock recoveriy circuit	E		D	Optical correlation
W	Mux	E		E		A	Combiners
	Demux	E		A	Spliters+receivers	B	Spliters+optical filters
	Conv.	E		B	O-e-o conversion	B	Semic. op. amplifiers
S	Switch	A	Gating transistors	B	Passive NT+e-o select.	A	Gating op. amplifiers

A- Ready for system B- Good performance C- Rudimentary D- Feasible E- Not feasible.

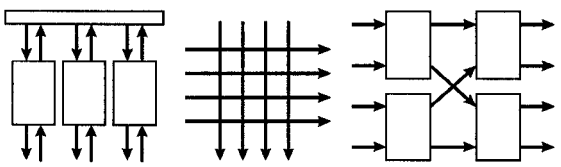
TABLE 1 - Electronic and photonic state of the art for switching functions.

RECENT SWITCHING IMPLEMENTATIONS

Next, after reviewing the main high capacity switching architectures, different ATM switching implementation architectures are described from three points of view: electronic research, photonic research and commercial switches. Implementation details are given in TABLE 2.

High Capacity Switching Architectures Review

Buffering in any packet switch is unavoidable. The need of contention resolution has generated different buffering strategies. Input buffers hold incoming packets (cells) while there is no possible path through the switch. In contrast, output buffers hold contending cells when there are multiple cell arrivals at the output ports. Output buffer is superior since input buffer suffers from *head of line* blocking, that is, cells with available paths can not be switched because of the FIFO discipline that holds one unswitchable cell on the head. However, input buffer is easier to implement because it does not require the speed necessary to support output buffers. Different high capacity switching architectures (Figure 2) are now presented according to their basic switching structure as presented in the previous section. Further information can be found in (3).



a) Shared Medium b) Crossbar c) Banyan Based

Figure 2. Switch fabrics.

Shared Medium Switches. The physical connection between input and output ports is implemented using a single high speed physical resource which can be a conducting medium or a memory. This resource is multiplexed among several input output connections, based on discrete time slots. A bus is an example of a physical conducting medium that can accommodate time-division multiplexing. A memory module can also implement connections based on time division since it holds cells supplied by input ports that are removed by output ports. This kind of switches are limited by bandwidth and there in scale. Multicasting and broadcasting are easy to accommodate since all outputs have access to all input data.

Crossbar Switches. This single stage, single path nonblocking switches were first developed for circuit switching and later used to connect multiprocessors. Many ATM switches are based on crossbar switches or use it as a basic building block. Crossbar switches are attractive because they are non-blocking, simple, modular and with minimal delays. Large full crossbars can be made with a few VLSI chips, whose integration is only limited by the available chip packages. However, they suffer from square complexity and fast control mechanisms for a crossbar switch are difficult. Many outputs selecting one input easily perform the broadcast functions. In order to improve the crossbar performance any of the buffer strategies explained in the first paragraph can be applied.

Banyan Based Switches. The multistage concept first appeared in the circuit switching area. This kind of switches were developed with the objective of a non blocking switch with lower complexity than crossbar switches. For instance, delta class networks have been proposed for multiprocessor systems. This networks have a single self-routing in/out path but suffer from internal blocking. These switches, which are usually referenced as Banyan based switches, are modular, have the same latency for all paths, support synchronous and asynchronous traffic and are suitable for VLSI implementation. The internal blocking makes the throughput decrease with a higher fabric dimension and increase with a higher switching element dimension. Their main drawbacks are the difficulty in dealing with congestion due to the extensive pipeline and buffering through the switch and also the difficulty to implement broadcasting and multicasting.

SWITCH	Link Speed	Switch Size	Max Throughput	Buffer Organization	Total Buffering	Max Expansion	Expansion Organization
HTXC	155 Mb/s		10-80 Gb/s	32x(#Base8)[1]		20-160 Gb/s	B8 ⇒ B16
Elec. Limits	40 Gb/s	4x4	320 Gb/s	16,000x18[2]	768,432	640 Gb/s	Speed-up 2
Delay Line	2.5 Gb/s	4x4	10Gb/s	4(x4)[3]	16	640 Gb/s	Banyan Net
Fiber Loop	2.5 Gb/s	2x2	5 Gb/s	1(x4)[4]	4	640 Gb/s	Banyan Net
Multidim Sw.	2.5 Gb/s	4x4	10 Gb/s	(4x4)[5]	16	640 Gb/s	Banyan Net
Fiber Bus	155 Mb/s	2x2	310 Mb/s				
El-op Switch	10 Gb/s	16x16	160 Gb/s			1 Tb/s	25x40 Gb/s
Commercial	622 Mb/s	4x4	2.5 Gb/s	4x13,312	53,248	10 Gb/s	4x2.5 Gb/s

[1] Internal buffering for each 8x8 shared memory switch. [2] Eighteen output FIFO. [3] Four delay lines with four different wavelenghts each. [4] One delay line with four different wavelenghts. [5] Four outputs with four different wavelenghts each.

TABLE 2 - Implementation details.

Electronic Switching Prototypes

There are many different approaches to the electronic switching. As Banyan based switches had VLSI implementation facilities several switches were developed. One of this multi-stage switches, together with a single stage switch operating on the electronic limits, are now presented.

A Banyan based switch. Figure 3 presents the UTXC architecture. It is organised in peripheral and central planes. The peripheral planes include the exchange termination performing header translation and policing. The central planes contain the ATM switching fabric where the BASE8 switching elements form a delta class network. The global throughput depends on the number of stages and planes. The BASE8 also serves as an interface between the peripheral and central planes.

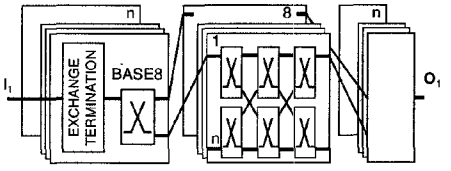


Figure 3. Electronic Banyan based switch (4).

The electronic limit switch. A simple architecture has been used to carry electronic technology towards its limits. As can be seen in Figure 4, cells arriving on each serial link are demultiplexed to 424 bits (cell width), routed to dedicated output-side FIFO storage according to the contents of the virtual channel and virtual path fields in the ATM cell header, then multiplexed back to serial form and transmitted to destination. There is a high-speed path with dedicated FIFO buffer from each incoming link to each of the other outgoing links.

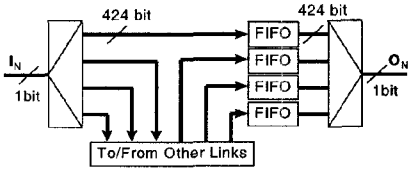


Figure 4. A fast electronic architecture (5).

Photonic Switching Prototypes

Based on realistic analysis of the potential capabilities and performance achievable by the photonic technology, three different approaches for ATM buffering and their integration in four different system concepts for the switching matrix are presented in (6). They are all composed of an all-optical high-speed routing network electronically controlled. Incoming ATM cells arrive in phase, accomplished by electrical interfaces in a first step while optical interfaces are a longer term objective. Follows a description for each concept and a mixed electro-photonic architecture in the last paragraph.

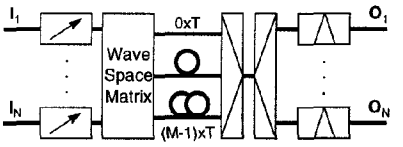


Figure 5. Fiber delay line switching matrix (6).

Fiber delay line switch concept. Signals are routed on the basis of their assigned wavelength and the contention is solved by optical fiber delay lines adjusted to multiples of the cell duration. As shown in Figure 5, a fast tuneable OWC (Optical Wavelength Converter) assigns to each ATM cell the wavelength corresponding to its target output. Then, the wave-space matrix provides access to the fiber delay lines of increasing length. Finally the output filters are tuned to a different wavelength defining the output address of the cell. The electronic control drives the OWCs and manages the wave-space matrix and delay lines as a FIFO.

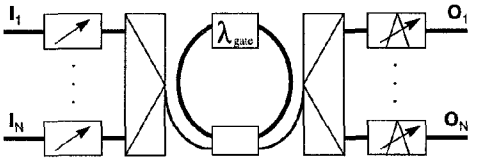


Figure 6. Fiber loop switching matrix (6).

Fiber loop memory switch concept. It is based on a fiber loop memory of one cell duration. The different wavelengths of the loop are used as different memory positions. In case of contention the cell is converted to one available wavelength in the loop and stored by tuning on the related optical gate in the loop. When contention is solved, the cell is routed to the destination link tuning the corresponding output tuneable filter and deleted from the loop tuning off the optical gate. The electronic control, on the basis of the attached tag, manages the memory positions as a shared buffer.

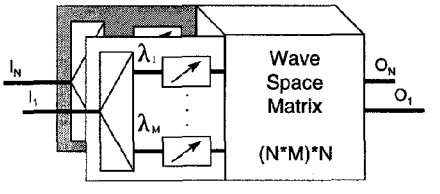


Figure 7. Multidimensional switching matrix (6).

Multidimensional switch concept. It exploits the wavelength domain to minimise the amount of optical buffers required in a multistage switch. In case of contention the cell is converted to a different

wavelength and transmitted at the same time slot. The contending cells are not delayed in a buffer, then buffers can be eliminated except at the last stage of the switch.

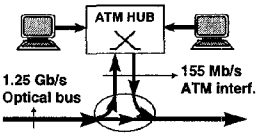


Figure 8. Corporate optical ATM network (6).

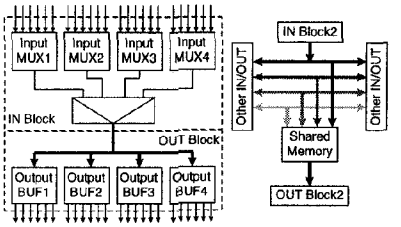
Corporate optical ATM network concept. Suitable for both access and private networks. In this case, electronic switches are interconnected with an optical double fiber ring through dedicated optical access nodes. Cells are inserted and dropped at the bit level using multi-functional high speed switches with dedicated hybrid drivers.

Electro-optic switch An architecture that also interconnects electronic switches through an optical core is presented in (7). The fiber ring is substituted by an optical crossbar. Then, a complex control management protocol establishes optical connections according to the buffer occupancy, the predicted loads and the connection set-up time.

Commercial Switches

Most commercial ATM switches use single-stage technologies for the sake of simple control and traffic management. They typically have a total switch throughput from 1 Gb/s to 10 Gb/s. Larger switches achieving a capacity close to 100 Gb/s either use multistage switching fabrics or interconnect smaller switches of several gigabit per second. In (8) various commercial switches are tested; the one with the best performance was ASX-200. This switch also has a good market penetration factor. So we have considered it as a good commercial example. Its architecture is explained now together with the next generation switch ASX-1000.

In the ASX-200 architecture (Figure 9.a), cells are processed in three steps. At the input, cells enter an ingress port, are sent through two stages of VPI/VCI translation and are checked for compliance with their traffic contract. Cells are then distributed, using TDM, to multiple shared memory switching outputs. In the ASX-1000 architecture (Figure 9.b), cells pass through the input functions in the same three-step order as in the ASX-200. The major output-side difference is the presence of a two-tier hierarchical switching/buffering system. Traffic is distributed from the inputs to the appropriate first-tier shared memory via as many as four individual 2.56 Gb/s unidirectional TDM distribution fabrics. These distribution buses use the same TDM technology as the ASX-200. The cells drain from the switching fabric memory to the second-tier shared memory switching/buffering modules, and from there, are transmitted to the network.



a) Commercial architecture. b) Architecture expansion.

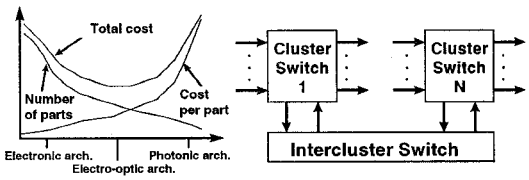
Figure 9. Commercial switch (9).

EVALUATION ISSUES

From the implementation point of view, optimum cost for a large switch is achieved by selecting a simple topology and using the highest-speed components available at a reasonable cost. Figure 10.a illustrates this idea: to construct a switch of a given capacity, fewer parts of a higher-speed technology can be used. The exact shapes of the curves depend on the architecture, and they can also shift with time. So low speed electronics require a large number of parts. If optical parts are introduced at a reasonable cost, the number of parts can be considerably reduced as the electro-photonic architectures do. Finally, if very high speed optics are used, the total cost increases at the moment but as mentioned earlier, costs could shift (7).

From the commercial point of view, acquisition and maintenance costs are not the only economics surrounding ATM due to the fast technological changes for its components. Many factors other than complexity and performance must be used to evaluate the previous architectures. They are enumerated and discussed now following the same structure used in (10).

Coexistence. Commercial markets require a high level of ATM integration in order to coexist with other LAN/WAN technologies. LAN emulation is the solution offered by the ATM Forum (11). In (12) different commercial ATM electronic switches where tested and results demonstrated a good performance in LAN emulation. Best performances where obtained with electronic conversion to ATM flows even for local switching. Optical switches with their higher capacity could be a desirable backbone if the reduced protocol functionalities did not became a drawback for LAN emulation. Coexistence of electronic and photonic technologies is also required. Existing electronic switches can benefit from photonic switching speed while evolving towards all-optical networks.



a) Technology costs (7). b) Hierarchical clustering (10).

Figure 10. Architecture costs and scalability.

Complexity and scalability. Scalability refers to a system capability of evolving or expanding in response to increased demands. This requirement is critical, since ATM technology is in its infancy stage and its commercial success depends on incremental deployment and a migratable strategy. Two aspects of the architecture must be scalable: the number of ports and the speed of terminating ports. They are somehow equivalent. Port scalability is closely related to the complexity measures of the architectures. They are summarised in TABLE 3, where the trivial conclusion is that the linear order of the shared medium architecture is preferred. However, the limited shared medium bandwidth limits its maximum scalability. A possible solution is to increase the level of parallelism within the switch fabric, that is, to route traffic flows through multiple and parallel paths like multiple buses within the switch. This was the solution adopted for the SX-1000. For those architectures with switching networks the solution would be to accommodate parallel network planes as the presented Banyan based architecture does. Finally, a cluster architecture with multiple switch fabrics interconnected via an intercluster switch (Figure 10.b) seems a good solution for electro-optical switches like the ones presented earlier. Upward scalability of the architecture relative to port data rates has a drastic implication for the internal resources of the switch fabric. Thus, scalability related to port data rates is more difficult to assess.

Architecture	Port Scalability
Shared Medium	Order of *i*
Banyan Network	Order of *i*(log of i)*
Matrix	Order of i^2

TABLE 3 - Port scalability (10).

Efficient use of bandwidth. The commercial market views bandwidth in terms of cost. ATM is attractive thanks to the capability of dynamic bandwidth allocation. Switching architectures that employ a complex protocol for establishing connection and routing decisions do not use the internal bandwidth efficiently. Contention resolution phases and cell duplication for broadcasting are some examples. ATM potentials are due to its hardware implementation capabilities; thus, complex software protocols used to provide optimal bandwidth management do not contribute to achieve a good performance on ATM. All presented architectures are electronically controlled. Thus, hardware or software bandwidth management protocols seem to feasible in all cases.

Reliability and fault tolerance. ATM as a LAN with a star topology requires a high level of reliability and fault tolerance from the switch. Multiple redundant switches that operate in primary and backup modes are a must since chip failures would most likely dismantle several (if not all) paths. Electro-optical switches can provide quit robust performance depending on the reliability of the optical core.

CONCLUSION

As of today, the most immediate evolution towards the commercial area seems to be dominated by photonics as a higher level switching, while electronics keep their interface position dealing with its limited bandwidth. Regarding the interface, electronic TDM architectures can support expandability, nonuniformity of port data rates and bandwidth management protocols. Inside the switch, photonic architectures can provide for concurrency and speed. Thus, the improvements in both electronic and photonic architectures should be integrated in order for commercial implementations to increase their cost-effectiveness.

REFERENCES

1. Hui, J. Y. and Cheung, K. W., 1996. Optical Versus Electronic Switching for Broadband Networks. IEEE Network, November/December 1996. pp. 21 to 25.

2. Thylén, L., Karlsson, G. and Nilsson, O., 1988. Switching Technologies for Future Guided Wave Optical Networks. IEEE Communications Magazine, February 1996. pp. 106 to 113.

3. Awdeh, R. Y. and Mouftah, H.T., 1994. Survey of ATM Switch Architectures. Computer Networks and ISDN Systems, vol. 27, 1995. pp. 1567 to 1613.

4. Claretto, S., Fassino, M., Licciardi, L. and Turolla, M., 1994. La Realizzazione del Circuito BASE8. Rapporto Tecnico CSELT, September 1994.

5. Butner, S. E. and Chivukula, R., 1996. On the Limits of Electronic ATM Switching. IEEE Network, November/December 1996. pp. 26 to 31.

6. Masetti, F. and others, 1996. High Speed, High Capacity ATM Optical Switches for Future Telecom. Transport Networks. IEEE J-SA in Communications, June 1996. pp. 979 to 998.

7. Munter, E. and others, 1995. A High-Capacity ATM Switch Based on Advanced Electronic and Optical Technologies. IEEE Communications Magazine, November 1995. pp. 64 to 71.

8. Mandeville, R., 1995. The ATM Stress Test. Data Communications, March 1995. pp. 68 to 82.

9. ForeRunner ATM Switch Architecture, April 1996.

10. Rooholamini and others, 1994. Finding the Right ATM Switch for the Market. IEEE Computer, April 1994. pp. 16 to 28.

11. ATM Forum Technical Committee. LAN Emulation over ATM. Version .1.0, January 1995.

12. Mandeville, R. and Johnson, J. T., 1996. Forget the Forklift. Data Communications, September 1996. pp. 121 to 134.

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