December 17th LECTURE

VIPS: Simple, Efficient, and Scalable Cache Coherence

Alberto Ros
University of Murcia

Abstract

Directory-based cache coherence is the de-facto standard for scalable shared-memory multi/many-cores and significant effort is invested in reducing its overhead. However, directory area and complexity optimizations are often antithetical to each other.

This talk presents VIPS, a family of cache coherence protocols based on self-invalidation and self-downgrade. VIPS protocols remove the complexity and cost associated with directories in their entirety, thus increasing multiprocessors scalability, and at the same time, provide better performance and energy efficiency than traditional directory-based protocols.

Short Bio

Alberto Ros received the MS and PhD degree in computer science from the University of Murcia, Spain, in 2004 and 2009, respectively. In 2005, he joined the Computer Engineering Department at the same university as a PhD student with a fellowship from the Spanish government. He has been working as a postdoctoral researcher at the Technical University of Valencia and at Uppsala University. Currently, he is Associate Professor at the University of Murcia. His research interests include cache coherence protocols and memory hierarchy designs for manycore architectures. His work has been published in some of the most prestigious international

conferences (ISCA, HPCA, PACT, IPDPS, HPDC) and journals (IEEE TPDS, IEEE TC).