UNIVERSITAT POLITÈCNICA DE CATALUNYA
BARCELONATECH

Departament d'Enginyeria Electrònica

4H-SiC Integrated Circuits for High Temperature and Harsh Environment Applications

Tesi doctoral presentada per a l'obtenció del títol de Doctor per la Universitat Politècnica de Catalunya, dins el Programa de Doctorat en Enginyeria Electrònica

Mihaela Alexandru

Director: *Philippe Godignon*

September 2013

UNIVERSITAT POLITÈCNICA DE CATALUNYA
BARCELONATECH
Escola de Doctorat

Acta de qualificació de tesi doctoral

Curs acadèmic: 2012 – 2013

Nom i cognoms
Mihaela Alexandru

Programa de doctorat
Ingeniería Electrónica

Unitat estructural responsable del programa
Universidad Politécnica de Catalunya UPC – Departamento de Ingeniería Electrónica

Resolució del Tribunal

Reunit el Tribunal designat a l'efecte, el doctorand / la doctoranda exposa el tema de la seva tesi doctoral titulada

4H-SiC Integrated Circuits for High Temperature and Harsh Environment Applications

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ACKNOWLEDGEMENTS

As a prelude to this thesis dissertation, I would like to express all my gratitude to the people which have contributed to the work here reported.

First, I would like to express my gratitude to the members of the examination panel for agreeing to evaluate this research work: Prof. Javier Sebastián Zúñiga (Universidad Politécnica de Madrid, Spain), Prof. Josep Altet Sanahujes (Universidad Politécnica de Catalunya, Spain) and Dr. Dominique Tournier (INSA-Lyon, France), as well as the substitute members, Dr. José Andrés Rebollo Palacios (IMB-CNM, Barcelona, Spain) and Prof. José Millán Gómez (IMB-CNM, Barcelona, Spain).

I would like to express my sincere gratitude to Prof. Francesc Guinjoan for having accepting me as Ph.D. student at UPC and tutoring me.

Then, I would like to express my deep gratitude and appreciation to my research supervisor Prof. Philippe Godignon for giving me the opportunity and supporting me along my Ph.D. studies in the SiC integrated circuits field. I am very grateful for his great advices and discussions concerning circuit's fabrication, and mainly because he made it possible! I would like to sincerely thank him for all the support related to reading and correcting papers, as well as this dissertation, and also for trusting in me.

Prof. Jose Millàn, the official head leader of Power Devices and Systems Department, I would like to deeply thank him for motivating me to follow a Ph.D. in the SiC research field, and also for his constant support and guidance during this research time.

I am indebted and deeply grateful to Viorel Banu, for having me guided during all this time, for his endless support, motivation and encouragements. I am deeply thankful for all the valuable and significant advices for both academic and daily life. He gave me a great practical view of the circuit's development and characterization. His constant assistance and long discussions are deeply and sincerely appreciated.

Part of the work presented in this dissertation strongly relies on clean room processes, and therefore I would like to thank all the clean room staff, especially Mónica Sarrión. Also I would like to thank Dr. Xavier Jordà, David Sánchez and Federico Rubio, for all their great

help concerning device packaging and measurements setups, as well as Dr. Miquel Vellvehi and Dr. Xavier Perpiñà.

I would like to thank all the current and former members of the power group for their constant advices, collaborations and friendship, specially to: Dr. Jesús Urresti – special thanks for his great friendship, encouragements and endless support, Dr. Pablo Fernández – for all the great advices concerning device radiation, Dr. Alessandra Caboni – my first officemate which become a great friend, and nevertheless to my all dearest colleagues and friends: Abel, Matthieu, Ana, Aurora, Arnau, Luis, Luisito, Maxime, Nacho, Andrés and Javier.

I would also like to express my gratitude to my former professor Prof. Gheorghe Brezeanu and Cristian Boianceanu for encouraging me to do this great study.

For all this time I have met many interesting people working on other fields, in and outside CNM, which I would like to thank for their help.

Nevertheless, I would like to express my sincere gratitude to my family, especially to my parents for their endless and permanent support, to my 88 year old grandmother and my aunty for encouraging me anytime. Also thanks to my two best friends Andra and Alexandra for their understanding, encouragements and valuable advices.

Last but not least, my particular thanks to Thomas for his constant warm kindness. Although distance is painful, sometimes overwhelming, thank you very much for always being close me, for your faithful trust and constant support for all this time.

Thanks to you all!

ABSTRACT

Silicon Carbide (SiC) has received a special attention in the last decades thanks to its superior electrical, mechanical and chemical proprieties. Nowadays, SiC is mostly used for applications where Silicon is limited, becoming a proper material for both unipolar and bipolar power device able to work under high power, high frequency and high temperature conditions.

Aside from the outstanding theoretical and practical advantages still to be proved in SiC devices, the need for more accurate models for the design and optimization of these devices, along with the development of integrated circuits (ICs) on SiC is indispensable for the further success of modern power electronics.

The design and development of SiC ICs has become a necessity since the high temperature operation of ICs is expected to enable important improvements in aerospace, automotive, energy production and other industrial systems. Due to the last impressive progresses in the manufacturing of high quality SiC substrates, the possibility of developing new circuit applications is now feasible. SiC unipolar transistors, such as JFETs and MESFETs show a promising potential for digital ICs operating at high temperature and in harsh environments.

The reported ICs on SiC have been realized so far with either a small number of elements, or with a low integration density. Therefore, this work demonstrates that by means of our SiC MESFET technology, multi-stage digital ICs fabrication containing a large number of 4H-SiC devices is feasible, accomplishing some of the most important ICs requirements. The ultimate objective is the development of SiC digital building blocks by transferring the Si CMOS topologies, hence demonstrating that the ICs SiC technology can be an important competitor of the Si ICs technology especially in application fields in which high temperature, high switching speed and harsh environment operations are required.

The study starts with the current normally-on SiC MESFET CNM state-of-the-art through a complete analysis of an already fabricated MESFET. It continues with the modeling and fabrication of a new planar-MESFET structure together with new epitaxial resistors

specially suited for high temperature and high integration density. A novel device isolation technique never used on SiC before is approached. A fabrication process flow with three metal levels fully compatible with the CMOS technology is defined. An exhaustive experimental characterization at room and high temperature (300ºC) and SPICE parameter extractions for both structures are performed.

In order to design digital ICs on SiC with the previously developed devices, the current available topologies for normally-on transistors are discussed. Furthermore, the circuits design using SPICE modeling, the process technology, the fabrication and the testing of the 4H-SiC MESFET elementary logic gates library at high temperature and high frequencies are performed. The MESFET logic basic behavior up to 300ºC is analyzed. Finally, this library has allowed us implementing complex multi-stage logic circuits with three metal levels and a process flow fully compatible with a CMOS technology.

This study demonstrates that the development of important SiC digital building blocks by transferring CMOS topologies (such as Master Slave Data Flip-Flop and Data-Reset Flip-Flop) is successfully achieved. Hence, demonstrating that our 4H-SiC MESFET technology enables the fabrication of mixed signal ICs capable to operate at high temperature (300ºC) and high frequencies (300kHz). We consider this study an important step ahead regarding the future ICs developments on SiC.

Finally, several experimental irradiations were performed on Tungsten-Schotthy diodes and mesa-MESFET devices (with the same Schottky gate than the planar SiC MESFET) in order to study their radiation hardness stability. The good radiation endurance of SiC Schottky-gate devices is proven. Hence, it is expected that the new developed devices with the same Tungsten-Schottky gate, to have a similar behavior in radiation rich environments.

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MOTIVATION

Based on The International Energy Agency (IEA) reports, a twofold increase in electrical power consumption from 1990 to 2020 is predicted. The United Nations have reported that the development and climate change are among the major global issues in this century that affect millions of people across the world. The modern society demands a reliable supply of electrical energy, both in the industrial and the private sectors. Also the recent industrial demands require applications that are exceeding the current semiconductors capabilities. Therefore, in order to overcome these demands, it is worthy to develop new strategies to reduce power losses and to distribute electrical energy more efficiently. Furthermore, the increase of the living standards and conditions of economic progress while human influence of the climate change is attributed to the increase of atmospheric CO_2 concentration from the emission of fossil fuel combustion. In this sense, this SiC technology will contribute to a more efficient energy control and also to offer viable and applicable solutions for industrial extreme environments.

Power electronic devices have a great impact on economy and environment due to the widespread use in many industrial and nonindustrial applications. More efficient power devices can provide cost effective and environment friendly tools for higher energy efficiency that is a required factor for the global issues.

Although Silicon (Si) based power devices are commercially available since 1950s, and have been extensively developed since then, the performance of these devices exhibits important limitations regarding power losses, operation temperature and switching speed. Therefore, it appears the must for introducing new materials for developing new generation of power devices in order to face the future global energetic challenges. It has been proven that wide bandgap (WBG) semiconductors are a viable solution. A significant part of the Scientific Community and Political Authorities have now interiorized that the next generation of power devices for efficient and eco-friendly power converters will be based on WBG semiconductors to replace traditional Si power switches. Consequently, recent intense research has demonstrated that WBG materials are a viable and efficient solution for many nonindustrial applications and also extreme environments operation.

Silicon Carbide (SiC) is one of the WBG that has been highly studied and investigated for the past 25-30 years, demonstrating that can overcome most of the current industrial needs. Great improvements regarding the SiC material quality have been recently reached leading to a vast majority of device developments on SiC. Although most of the typical Si devices have been implemented on SiC already, great efforts are still needed towards their performance and optimization. However, it is predicted that by introducing SiC power devices in the "power generation – conversion – consumption" chain the energy usage can be substantially decreased. Furthermore, great benefits related to many important industries will be earned by using SiC devices. Even though few SiC devices are currently commercially available, significant progresses are constantly made in this direction.

We consider that the next mandatory step necessary to overcome the present Si applications and to take advantage of the outstanding SiC properties, is the integration of the actual SiC develop devices into complex systems. The integrated circuits (ICs) design and its development on SiC is still at its early stage, being reported so far very simple circuits with a low integration density. However, the implementation of SiC ICs is considered a significant necessity for the future of modern power electronics. Moreover, there are great expectations of SiC ICs to become a competitor of smart Si power technology, and also to have a remarkable effect in automobile and aerospace industries, and also in telecommunications equipment.

Therefore, in order to help and to advance the research headed into this direction, following some important Si CMOS concepts, the design and development of SiC integrated circuits able to work in harsh environments and with a high integration density is the main topic of the present work.

THESIS OUTLINE

The main objective of this study is the demonstration of fully integrated circuits on 4H-SiC able to operate at high temperatures and in harsh environments. The work is divided into six chapters:

Silicon Carbide – Material and Based Electronics

In order to emphasize the SiC material outstanding proprieties, **Chapter I** is devoted to the comparison between the SiC fundamental material proprieties and other important wide bandgap semiconductors, together with the most common semiconductor material used nowadays in the big majority of electronic devices (Silicon). The efforts toward high quality and low defects density SiC wafers, as well as stable Ohmic and Shottky– SiC contacts are also reported. Furthermore, the rising developments with respect to the SiC electronics devices are summarized. A brief introduction concerning the wide applications range where SiC electronic devices can have a successful impact is as well presented, emphasizing the current status of the Integrated Circuits developments on SiC.

The 4H-SiC Device Library

The complete library of devices used for the development of integrated circuits on SiC is described in the next chapters. It starts with a brief presentation concerning the basic functionality of the active device of the present work – the MESFET (**Chapter II**). The development together with the theoretical and experimental analyses of the already fabricated normally-on mesa-4H-SiC MESFET are presented in **Chapter II**. The mesa-MESFET analyses will be used as reference in the development of a new MESFET structure. Adopting standard Si CMOS layout design and isolation technique (never used on SiC device isolation before) a complete new planar-MESFET suitable for high density integrated circuits (ICs) on 4H-SiC able to work at high temperatures has been design and fabricated using three metal levels, and further characterized up to 300ºC (**Chapter III**). The development and experimental characterization of scalable 4H-SiC epitaxial resistors is

presented in **Chapter IV**. These structures are highly necessary for future ICs developments, first due to a lack of complementary devices for the N-channel MESFETs, and second because the temperature matching between circuit elements is an important aspect for ICs proper temperature operation.

The 4H-SiC Digital Integrated Circuits

The complete development and experimental analysis of 4H-SiC MESFET basic logic gates and multi-stage ICs digital building blocks is the main topic of **Chapter V**. A general classification of digital ICs logic families including the most common MESFET topologies, together with the 6H-SiC JFET topology are first presented. The design and modeling of 4H-SiC elementary logic gates developed with normally-on MESFET devices and epitaxial resistors are the key gates for developing some of the most common CMOS multi-stage digital ICs blocks. Experimental results, showing the high temperature and the high frequency operations of the designed logic SiC ICs are analyzed. It is emphasized that using the present 4H-SiC MESFET topology, common Si CMOS standard topologies (containing a large number of devices) can be transferred for SiC ICs developments.

The 4H-SiC Schottky-Gate – Radiation Hardness

The radiation hardness of 4H-SiC Schottky-gate based devices is presented in the last **Chapter VI**. Encapsulated Schottky diodes and mesa-MESFETs (Chapter IV) have been submitted to several irradiation tests. The Tungsten-SiC semiconductor interface behavior has been investigated after high energy proton and electron radiation experiments.

This study provides important information concerning our present Tungsten-Schottky gate behavior in radiation rich environments, being able to predict a general behavior of the new developed MESFETs (as well as circuits) in radiation environments.

Finally, the **General Conclusions and Further Work** are commented at the end of the present dissertation.

CHAPTER I

GENERAL INTRODUCTION

The current trends for innovative electronic applications require every time more high frequency, high temperature, high electric power usage and/or even high radiation operation stability. Although the most dominant semiconductor material for commercial devices and integrated circuits applications is Silicon, it has been shown to be a non-ideal material for RF and harsh environment applications, due to its fundamental physical limitations, such as its relative small bandgap and low material conductivity [1,2]. Therefore, it appeared a strong motivation for switching to wide bandgap (WBG) materials which can offer a viable alternative solution for proper device performance in such extreme environments. From the WBG semiconductor materials that have been studied so far, Silicon Carbide (SiC) is between the most suitable compound materials that can overcome the previous limitations. It has become particularly interesting thanks to its long extended period of study and development, hence providing the real opportunity for producing dedicated devices and integrated circuits for harsh environmental usage.

Currently there is no major technical obstacle for SiC to penetrate the Si power electronics market, except the material cost. However, because of the great benefits resulting from SiC technology, this could offset part of the total costs for SiC power systems. Also the fact that the technology of producing SiC-based electronic devices is close to the well-known Si technology brings a great gain in developing new structures and circuits, therefore making realistic the possibility of switching to SiC devices and Integrated Circuits. Aside from tremendous theoretical and practical advantages still to be

realized in SiC devices, the need for more accurate models for the design and optimization of these devices, along with the development of ICs on SiC, is indispensable for the further success of modern power electronics.

1.1. Fundamental SiC Material Properties

In late 19th century SiC was an important material for sandpapers, grinding wheels and cutting tools. At the beginning of 20th century SiC started to become more interesting for industrial applications in refractory linings and heating elements for industrial furnaces, in wear-resistant parts for pumps and rocket engines, and in semiconducting substrates for light-emitting diodes. Later on, SiC has received a special attention in device research and development due to its highly suitable properties for high-power, high-frequency and high-temperature applications.

1.1.1. SiC Crystallography and Polytypism

SiC in natural form is exceedingly hard, being synthetically produced as crystalline compound of Silicon (Si) and Carbon (C). SiC can occur in different crystal structures that are called *polytypes* [3]. In nature the compound exists in more than 250 different polytypes [4], but only few are commonly in a reproducible form acceptable for use as an electronic semiconductor. The most common polytypes presently being developed for electronics are 3C-, 4H-, 6H- and recently 15R-SiC [5].

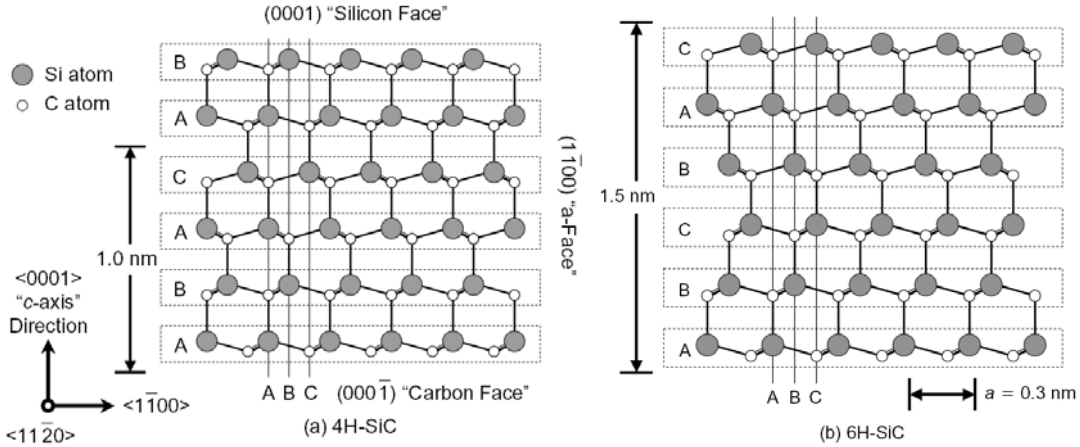

Fig.1.1. *Schematic representation of* ***(a)*** *4H-SiC and* ***(b)*** *6H-SiC atomic crystal structure, showing preferential crystallographic directions and surface [6]*

The above figure presents the atomic crystal structure of the two most common polytypes 4H- and 6H-SiC. These polytypes are composed from different stacking sequence of the hexagonally closed-packed double layers on Si and C atoms, where each single Si-C bilayer can simplistically be viewed as a planar sheet of Silicon atoms coupled with a planar sheet of Carbon atoms [3, 7].

Depending on the nearest neighbor atom arrangement, the atomic sites in SiC crystals are classified to be cubic or hexagonal. The polytypes are named according to Ramsdell's notations [8] showing the periodicity of the stacking sequences (represented by a number) and its crystalline structure (either C-cubic, H-hexagonal or R-rhombohedral). The sequences ABCB and ABCACB correspond to the 4H-SiC and respectively 6H-SiC polytypes. SiC is a polar semiconductor across the *c*-axis, having one surface normal to the *c*-axis terminated with Si atoms, and the opposite normal *c*-axis surface terminated with C atoms. As shown in Fig.1.1, these surfaces are typically referred to as *Si-face* and *C-face* surfaces, respectively.

SiC substrates can be both ***N***- and ***P***-type doped over a wide range of concentrations, using Nitrogen or Phosphorus as donors (*N*-type), and using Boron, Aluminum or Gallium as acceptors (*P*-type).

1.1.2. Physical and Electrical Properties

SiC shows excellent electrical and mechanical properties. Even though the amount of Si and C atoms is the same, these properties can vary significantly between different SiC polytypes because of the different crystal orientations, lattice sites and surface polarity. As Si is the semiconductor used in the vast majority of commercial electronic devices and circuits, in Table.1.1 some of the most important properties at room temperature of the 3C-, 4H- and 6H-SiC in comparison with Si and other well-known semiconductor materials are summarized [9-11]. Generally, WBG materials, such as SiC, GaN and Diamond have good chemical stability and mechanical properties, which makes them promising materials for next generation of high power, high frequency and high temperature electronics.

Among these WBG materials, Diamond is often cited as the ultimate semiconductor [11]. However, due to many uncontrolled fabrication processes, Diamond was kept away from electronics development for many years. Moreover, recently GaN has gained a lot of research and development attention, and has been proven to be a notable alternative for SiC [12]. However, SiC is by far the most mature in development, fabrication and commercially available WBG material compared with its alternatives.

Table.1.1. Material properties of the well-known semiconductors

	E_g [eV]	E_c [MV/cm]	λ [W/cmºK]	n_i [cm^{-3}]	v_s [10^7cm/s]	μ_n [cm^2/Vs]	μ_p [cm^2/Vs]	ε_r
Si	1.12	0.3	1.5	$1.5\text{x}10^{10}$	1.0	1350	450	11.8
3C-SiC	2.3	> 1.5	3-5	~10	2.5	750	40	9.6
4H-SiC	3.26	3.0	3-5	$\sim10^{-7}$	2.0	$800^{\parallel c}$ $800^{\perp c}$	120	9.7
6H-SiC	3.02	3.2	3-5	$\sim10^{-5}$	2.5	$60^{\parallel c}$ $400^{\perp c}$	90	9.7
GaN	3.39	3.3	1.3	$\sim10^{-11}$	2.5	900	30	9.0
GaAs	1.42	0.6	0.5	$1.8\text{x}10^{6}$	2.0	6500	320	12.8
Diamond	5.45	5.6	20	$\sim10^{-27}$	2.7	2200	1600	5.5

Concerning mechanical and chemical properties SiC, is known as a very hard material having Young's modulus of 424 GPa [13]. It is chemically inert showing a very poor reaction with any known material at room temperature and presenting a good endurance to radiation damage as well.

The most beneficial inherent material superiorities of SiC over Si listed in Table.1.1 are its higher high critical electric field (E_c), wide energy gap (E_g), high thermal conductivity (λ), and high carrier saturation velocity (v_s). For high power devices the main advantage that SiC has in front of Si, is the much wider bandgap (almost 3 times wider for 4H-SiC) that results in larger critical electric field and higher temperature capabilities. Due to these superior properties, it enables the usage of much higher doped thinner drift layers providing lower specific *on*-resistance and less leakage current at elevated temperatures for a desired breakdown voltage.

Table.1.2. *FOM for some of the previous mentioned semiconductors [14]*

		Si	4H-SiC	6H-SiC	Diamond
JFOM	$\frac{E_C^2 \cdot v_s}{4\pi^2}$	9	4410	2533	73856
BFOM	$\varepsilon\mu E_C^3$	1	34.7	16.6	128
KFOM	$\lambda\sqrt{\frac{c \cdot v_s}{4\pi\varepsilon}}$	13.8	229	90.3	101

The Figures-of-Merit (FOM) are based on the material properties and are used to summarize and evaluate the device performances and semiconductor materials targeting

particular applications (Table.1.2). The high power and high frequency capabilities of devices are expressed through JFOM figure-of-merit [15]; the BFOM is suggesting the low frequency and the static losses of the devices [16]; while the thermal limitations and also the switching speed of components performance at high frequency can be deduced from KFOM [17].

The recent SiC based electronics devices are typically fabricated on either 4H- or 6H-SiC due to the poor quality of 3C-SiC. Between 4H- and 6H-SiC, 4H-SiC has substantially higher carrier mobility, shallower N dopant ionization energies (4H-SiC – 45MeV against 6H-SiC – 85MeV [11]) , and low intrinsic carrier concentration (Table 1.1), thus being a more favorable polytype for rough environmental applications. Even more, from the Table.1.2 one can easily observe that 4H-SiC polytype is predicting better device performance than 6H-SiC, especially for high-frequency applications (JFOM) and for faster switching devices (KFOM). Therefore, the 4H-SiC FOMs present encouraging values for device and specially circuits development, hence justifying why many SiC device fabrication efforts have shifted towards 4H-SiC as it has become more readily available.

Another important aspect is the necessity of using ***semi-insulating substrates*** for devices and circuits operating at microwave frequencies in order to achieve low dielectric losses and reduce device parasitics. Using semi-insulating substrate, the loss of the signal due to the capacitive interactions with the substrate material is minimized. Also, for high temperature operation the leakage current is considerably reduced, allowing better device performance. “High-purity” 4H-SiC semi-insulating substrates have been obtained by eliminating the poor reliability owing to charge-trapping effects [18], together with the low residual dopant level. However, it was demonstrated that the lateral SiC MESFET fabricated on semi-insulating substrates are less sensible to micropipes than vertical high-power switching devices [6].

Therefore, in the present work the polytype that will be used in developing electronic devices and Integrated Circuits is the ***4H-SiC*** due to higher carrier mobility and more isotropic nature, and also due to its high quality semi-insulating substrates and wafers commercial availability.

1.2. SiC Fabrication Technology

Thanks to the intense effort that SiC process technology has recently received, the SiC device fabrication has been greatly improved and developed. Also great progress on the quality of the wafers and their increasing diameter has been achieved, currently 6 inch wafers being commercially available [19].

1.2.1. SiC Crystal Dislocation Defects

As one of the key issues in SiC process technology is to achieve a good yield, an immense effort has been invested in the controlled growth of the high quality epilayers.

Table.1.3. *Major types of extended crystal defects reported in SiC wafers and epilayers [6]*

Crystal Defect	Density in Wafer (cm^{-2})	Density in Epilayer (cm^{-2})	Comments
Miropipes (hollow-core axial screw dislocation)	~10-100	~10-100	High reduction of the breakdown voltage in power devices and increase of the leakage current
Stacking Faults (disruption of stacking sequence)	~10-10^4	~10-10^4	Bipolar power devices degradation, reduction of carrier lifetime
Closed-Core axial screw dislocation	~10^3-10^4	~10^3-10^4	Reduction of the breakdown voltage in power devices and increase of the leakage current
Basal plane dislocation	~10^4	~10^2-10^3	Source of stacking faults propagation, leading to bipolar power device degradation, reduction of carrier lifetime
Threading-edge dislocation	~10^2-10^3	~10^4	Impact not well known
Carrot defects	N/A	1-10	High reduction of power device breakdown voltage and increase of off-state leakage current
Low-angle grain boundaries	~10^2-10^3	~10^2-10^3	Typically more dense near wafer's edges, impact not well known

Even though, a new technique of producing ultra-high-quality SiC single crystal has been reported [20], the growth of SiC crystal still presents defects. The initial main problem in producing large area SiC devices were the micropipes defects, which generally lead to junction breakdown at electric fields well below the critical field [21]. However, the growth technique – High Temperature Chemical Vapor Deposition (HTCVD) [22-24], has shown to reduce micropipes by 80%, thus offering the possibility for stepping to industrial developments.

Furthermore, it has been observed that the stacking faults generated from base plane dislocations, are mainly degrading the bipolar power device [25-28]. Moreover, the electric field at which most micropipes and other SiC dislocations are failing is typically higher than the working electric fields of digital circuits, thus affecting much less the circuits operation than the high-field power devices [6]. In Table.1.3 the major crystal defects that have been reported in SiC wafers are summarized. Although, other defects still exist in SiC wafers and epilayers, not much information has been reported so far.

Eventually, we can conclude that as the possibility of achieving high quality SiC wafers has substantially increased, it has opened new opportunities and possibilities for a large range of SiC device development, and even more, for Integrated Circuits development, which is still a subject at its early stage on SiC.

1.2.2. SiC Ohmic and Schottky Contacts

Although SiC is following similar technical steps and shares several of the Si technology processes, many specific processes have been developed for SiC manufacturing, such as etchings, selective doping and dopant activation, together with ohmic and Schottky contacts. Over time, contacts and interconnections on SiC have received special attention. In order to benefit of SiC semiconductor advantages, the contact metallization of the SiC-based electronics needed to stand both high temperature and high current stresses.

The manufacturing of reliable and low-resistance SiC ohmic contacts is one of the most studied and analyzed issues, being primarily important for SiC devices. A high energy Schottky barrier is formed at a metal-semiconductor interface, which results in low-current driving, slow switching speed, and increased power dissipation. Although the SiC specific ohmic contact is higher than for Silicon, it is considered acceptable for most SiC applications. Lower specific contact resistances are usually obtained on *N*-type than on *P*-type 4H- and 6H-SiC. However, high temperature operation up to 600ºC [29] together with long term operation [30] of SiC ohmic contacts have been demonstrated.

Thanks to the SiC wide bandgap, most of the non-annealed metal contacts on lightly doped 4H- and 6H-SiC are rectifying. Up to now quite a large variety of studies concerning rectifying metal-semiconductor Schottky barrier contacts has been reported [31-34]. These contacts have been proven useful for a number of devices, including MESFET transistors and fast-switching rectifiers [19,35]. Due to the absence of minority carrier charge storage, the unipolar SiC Schottky diodes turn off faster than the Si ones, thus the SiC Schottky rectifiers owe the advantage of faster switching with less power losses, hence being successfully used in higher frequency operation applications [36,37]. However, because of

the metal-SiC interface and the reverse bias current degradation at elevated temperature, the operation of rectifying SiC Schottky diodes is typically limited to not more than 400ºC.

In the present work our interest is particularly orientated to this kind of devices. We have reported a comparison between Nickel (Ni) Schottky diodes and Titanium (Ti) Schottky diodes regarding the life test at high temperature (270ºC) [38]. It has been shown that the Ni Schottky barrier presents forward drift voltage at high temperatures due to the chemical instability of the interface, while the Ti diode was exhibiting high reverse leakage current due to its lower barrier height. By employing Tungsten (W) as Schottky metal, we have later reported that the forward voltage drift is eliminated, showing a steady metal-semiconductor interface, therefore achieving a very stable behavior of W-Schottky diodes at high temperatures [39].

Thanks to the great progresses in developing high quality SiC contacts, various companies (such as Cree, Infineon, RHOM, Microsemi, Semisouth, ST Miroelectronics) are commercializing SiC rectifiers. Therefore, the Schottky contacts have achieved a really good maturity fabrication level, being a great benefit for SiC MESFET manufacturing.

A very important aspect concerning fabrication processes is that SiC is one of the very few WBG materials that presents a real and unique potential to be thermally oxidized in order to form a SiO_2 film, and moreover is the only WBG semiconductor that has SiO_2 as a native oxide. This provides the great opportunity to develop Metal Oxide Semiconductor (MOS) power devices, analogous to the Si based technology. Because the MOSFET is a very important device for a modern technology development, great efforts have been made for improving the SiC/SiO_2 interface fabrication process [40].

1.3. Applications of SiC-Based Electronics

Currently SiC is mostly used for applications where Si cannot offer acceptable results. SiC has also shown that its physical and electrical properties make it a suitable material for harsh environment applications. The most beneficial advantages of SiC material are summarized in Fig.1.2, showing the device advantages in comparison to Si, and vast range of applications in which these can be implemented. The areas where SiC structures can achieve higher performance than Si devices are especially the high-temperature and high-power application fields.

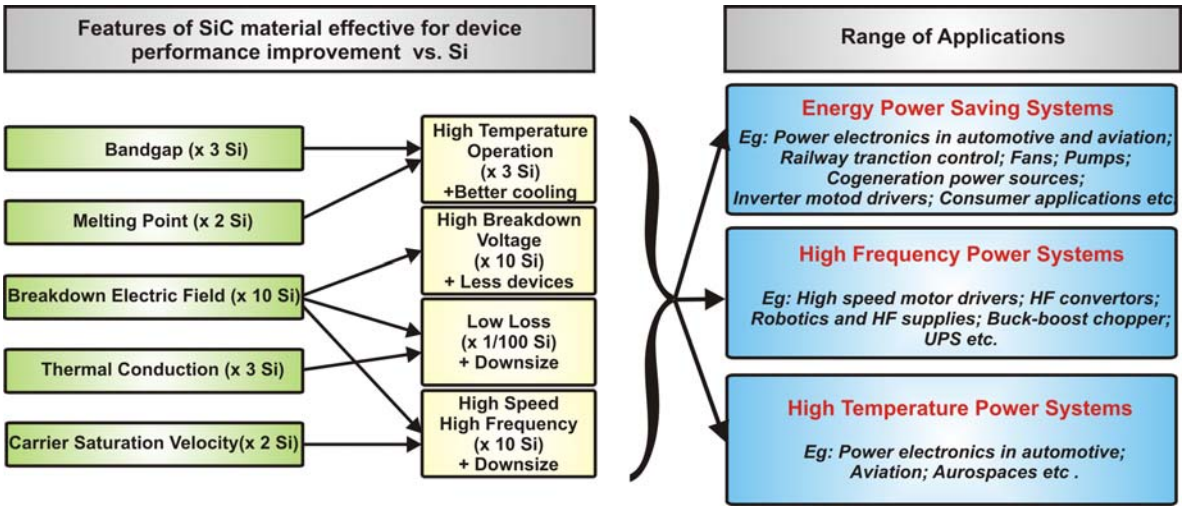

Fig.1.2. *The impact of SiC material in device performance vs. Si and the vast range of power applications that can derive from these features*

Thanks to the wide energy gap and the low intrinsic carrier concentration of the SiC material, it allows SiC based devices to operate at much higher temperatures than Si devices [41] without suffering from intrinsic conduction effects. Due to the lower breakdown field that Si owns, during time new transistor designs were developed in order to improve the device breakdown voltage, hence to achieve better power devices on Si; an example is the vertical insulated base transistor – the MOS-bipolar Darlington power device [42]. However, in SiC case the high breakdown electric field is enabling the fabrication of very high-voltage and high-power devices such as diodes, transistors and also microwave devices.The high electron drift velocity explains why SiC devices are able to operate at high frequencies. Therefore, the palette of applications that SiC based electronics covers a large field.

Nowadays there are many research groups and companies from automobile and major electrical equipment producers, to companies manufacturing industrial equipment, inverters, power supplies, and even the electric power utilities, that are involved in developing the next generation of SiC based power electronics. Up to now almost all types of SiC power devices (such as SBDs, PiN rectifiers, MOSFETs, JFETs, MESFETs, BJTs and IGBTs) have been reported, demonstrating their high voltage capability. The recent improvements of the fabrication processes leaded to the possibility of obtaining low doped, thick epitaxial layers that have brought great progress in terms of blocking voltage capabilities. The evolution of blocking voltages follows closely the constant improvements in epitaxial growth of low doped N-type layers and their commercial availability [19, 43] and a wide variety of electronic [44-46], optoelectronic [44,47] and electromechanical [47] devices have been successfully fabricated on SiC.

One of the global environmental issues is directly related to the improvement of energy usage. Reducing power losses in electronic devices is an important headline for all business sectors, where SiC devices have already earned great interest as a key material for the environmental-aware era. SiC technology is expected to have a significant impact on power electronics sector, solar cells, electric cars and traction, due to the power conversion losses in inverters, converters etc. that can be considerably reduced. This means that the devices can operate with less heating dissipation, which in turn makes smaller and lighter power converters possible.

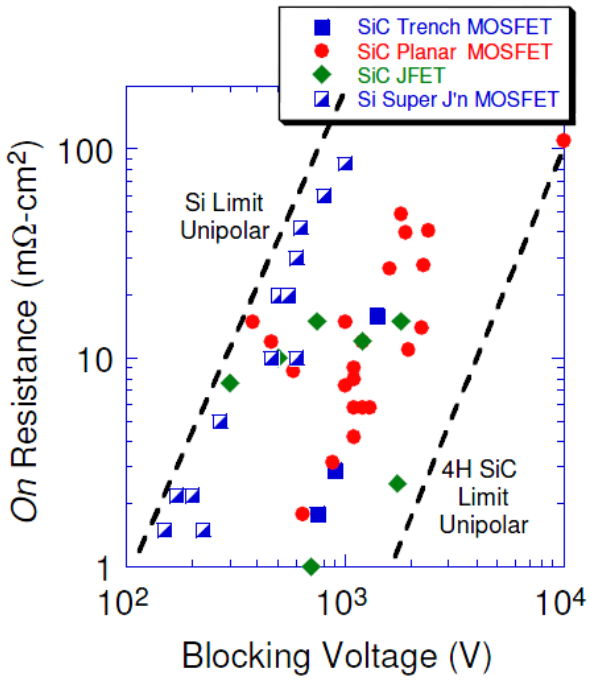

Fig.1.3. *Specific on-resistances versus breakdown voltages for SiC power devices [48]*

A large amount of power is lost from power generation to consumption during its conversion and transmission. It has been estimated that if, in Japan alone, all conventional power Si devices were replaced by SiC, the energy savings would be equivalent to the output of 4 nuclear power plants [49]. Therefore, it is expected that the mass production of SiC modules contributing to motor control and power conversions efficiency to have a major effect on energy saving worldwide. The actual SiC device market is being driven by inverters in household applications and industrial equipment; hybrid, electric and other vehicles; and distributed power systems such as solar cells. Yole Developpement predicts that SiC devices will grow into an US$800 million market by 2015 [50].

SiC is used for high-voltage switching in electric power distribution and electric vehicles. They can operate up to 600ºC [51], at switching frequencies in the 10Hz-100kHz range and at increased power densities. Fast-switching capability coupled with high power

density and high operating temperature make SiC high-frequency devices ideal for military aircrafts requiring lightweight, high-performance and powerful microwave electronics, radar and communications systems. Commercial communications industries such as air traffic control, weather radar stations and cell phone base stations, would also benefit from higher performance radio-frequency SiC devices.

There are other applications that are directly interested in the benefits of SiC-based devices. In military projects for developing hybrid-electric armed robotic vehicles, one of the key components are the high-power converters and motor drives able to operate in harsh environments, presumably achievable with SiC devices.

It has been estimated that the integration of solid-state “smart” power electronics into the power grid will reduce the required energy production by 5% and will allow carrying about 50% more power over the existing lines [52]. Because of the faster switching speed, it is not only increasing the power system conversion efficiency, but it also enables the use of smaller transformers and capacitors to greatly shrink the overall size and weight of the system. Thanks to the excellent high temperature capability of SiC devices, cooling system requirements, which are a substantial portion of the total size and cost of a power conversion and distribution system, are greatly reduced.

NASA is one of the major researchers and developers investigating in SiC devices, being interested in SiC power converters for spacecraft and satellite applications to increase the payload capability in lightweight solar arrays.

SiC electronics have gained a great interest in automotive industry as well. The Japanese company Toyota has commented that "SiC is as crucial as gasoline for the engines". Nissan has already prototyped an inverter using SiC diodes. And Honda was prototyping a power module using a SiC device jointly with Rohm [53].

The interest from many companies of using SiC based devices relies on the ability to place these devices, that require no additional cooling system, directly into hot environments, hence enabling important benefits to automotive, aerospace and deep-well drilling industries [41, 54].

1.4. Integrated Circuits on SiC

Another field where SiC is expected to play a major role is in ***Integrated Circuits*** (ICs). There are many applications where SiC ICs bring great advantages, such as sensors and control electronics used in conjunction with jet or rocket engines that must be removed from the target area, carefully shielded, protected and cooled.

To our knowledge, not many SiC ICs have been reported so far. The first power IC on SiC have been reported in 2008 [55]. Long term stability of high temperature operation of JFET ICs on 6H-SiC has been demonstrated [56] both analogical and digital with circuit operation at 500ºC for hundreds of hours. On 6H-SiC CMOS technology has been investigated in the early '90s [46] and recently reported in 4H-SiC [57] showing digital ICs operation at high temperature. Lately several bipolar ICs have been realized on 4H-SiC [58-62] showing a good operation up to 300ºC. However, the majority of the reported ICs on SiC were realized with a small number of devices. Although in [62] a ring oscillator using bipolar technology was presented, it has been realized with a very low density integration.

Therefore, in the present work the main goal is to demonstrate the development of ICs with a large number of devices, able to work in harsh environment and accomplishing the critical ICs requirements (wafer planarity, reduced ICs area, fast circuits etc.).

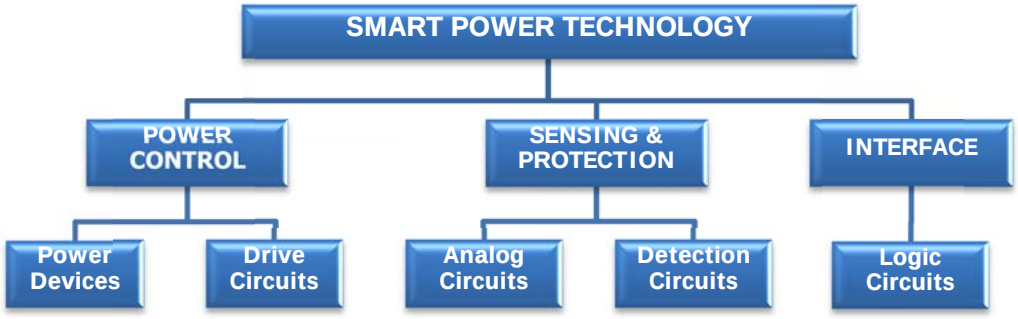

Fig.1.4. *Functional elements of the smart power technology on Silicon [63]*

Although currently investigations are carried out in this field, ICs on SiC development introduces an increased complexity into the problem. SiC power integration based on lateral devices is considered to raise important challenges to *smart Si power technology* [63] in the near future. Fig.1.4 shows an overview of the smart Si technology that consists of three modules, providing the interface between the digital control logic and the power load, aimed to control the power systems. The digital circuit's module has an important role in the smart system, generally needed for encoding/decoding operations.

1.5. Conclusions

The purpose of this first chapter is to make a brief introduction into the exciting world of SiC material, presenting its outstanding properties, its current process technology and the wide range of areas where SiC devices can be successfully implemented. Initially, it has been pointed out the most important properties of SiC in comparison with the semiconductor employed in the majority of commercial electronic devices and circuits (Silicon). From the material properties was shown that 4H-SiC is a more favorable polytype for high-power, high-frequency, and high temperature device applications and moreover, the FOM evaluation emphasized that 4H-SiC polytype have more suitable values for integrated circuits development. The recent fabrication breakthroughs reported in the fields of material growth and technological processes will promote the development of high-power SiC devices and integrated circuits. Among the SiC polytypes, 4H-SiC is increasingly considered for electronic devices since 4 and 6 inch wafers have been demonstrated with high quality and low defects density. Regarding the SiC contacts and interconnections, from previous CNM studies, it was shown that Schottky contacts made with Tungsten present a very stable behavior at elevated temperatures.

Therefore, the attention that SiC research has received in the last decade has resulted in a great industrial interest. The improvements of the epitaxial growth and their commercial availability have led SiC device fabrication into a vast variety of electronic applications. It has been shown that the SiC device interest is enlarging even in the consumer application field. It is predicted that with the SiC power device replacement in the "power generation – conversion – consumption" chain the power losses will be considerably reduced. Therefore one of the global environmental problems – the reduction of energy usage, can be a solvable problem. Great benefits are foreseen in the case of automotive and aerospace engines. Improved electronic telemetry and control from high-temperature engines are necessary to more precisely control the combustion process, thus improving fuel efficiency while reducing polluting emissions. High-temperature capability eliminates performance, reliability, and weight obstacles associated with liquid cooling, fans, thermal shielding and longer wire runs, typically needed to realize similar functionality in engines using conventional Silicon semiconductor electronics. Even though SiC devices are every day more commercially available, the development of Integrated Circuits on SiC is still in its early stage. It is predicted that SiC ICs can become a rival of the smart Si power technology having the aim to perform complex switching functions at high frequencies. Moreover, SiC ICs have shown to have a remarkable effect in automobile and aerospace industries, as well as in telecommunications equipment.

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CHAPTER II

The 4H-SiC Mesa-MESFET

Starting Device

A brief presentation concerning the basic functionality of the main active device of the present thesis – the MESFET transistor, is initially introduced. Afterwards, the experimental and theoretical characterization of the normally-*on* 4H-SiC MESFET transistor fabricated using *mesa isolation technique* is presented. These structures were first designed and fabricated in the frame of the Project SPACESiC. The main purpose of this project was to increase the power electronic system performance for space applications, using novel semiconductor devices and packaging materials. Finally, these power devices were evaluated in several space applications such as radar, energy distribution and propulsion systems, such as ion thrusters. Within this project specific process steps needed for manufacturing the proposed SiC devices were optimized leading to a mature fabrication process for the MESFET devices. Also a close analysis and investigation of the SiC structures concerning their performance and harsh environment working capabilities for space applications was performed. A deep modeling study of these existing MESFETs is the first necessary step in the progress of developing a new MESFET structure especially suitable for designing integrated circuits on 4H-SiC. This complete analysis and experimental investigation of the mesa-MESFETs will be used only as an input study for the new structure design and is essentially for the new technology adjustments applied later on in this present work.

2.1 The MESFET Basic Operation

The Metal Semiconductor Field Effect Transistor (MESFET) has quite a similar construction and terminology as the Junction Field Effect Transistor (JFET). The JFET, first analyzed by Shockley in 1952 [1], is basically a voltage-controlled resistor and its resistance can be changed by varying the width of the depletion layer extended into the channel region. The MESFET was proposed by Mead in 1966 and subsequently fabricated by Hooper and Lehrer using GaAs epitaxial layer on a semi-insulating GaAs substrate [2, 3]. It shows an identical operation to that of a JFET.

The main difference between the JFET and MESFET is that the latter is using a *Schottky junction* (metal-semiconductor junction) instead of a *pn junction* for the gate terminal. The MESFETs are usually constructed in compound semiconductor technologies lacking high quality surface passivation, such as SiC, GaAs or InP, and are faster than silicon-based JFETs or MOSFETs. MESFETs are operating up to approximately 45 GHz [4] and are commonly used for microwave frequency communications and radar.

A MESFET transistor can be designed using different topologies: *lateral MESFET*, which is the most widely used structure; *vertical MESFET* which is achieved by placing the gate fingers at the bottom of etched trenches, and is typically used in power applications; or the *V-groove gate FET* that can exhibit a higher transconductance and a lower turn-on resistance than the conventional planar FETs [5]. The device topology that will be further discussed is the lateral one, being the most common used MESFET design, where the channel is aligned in a moderately doped conducting layer at the surface.

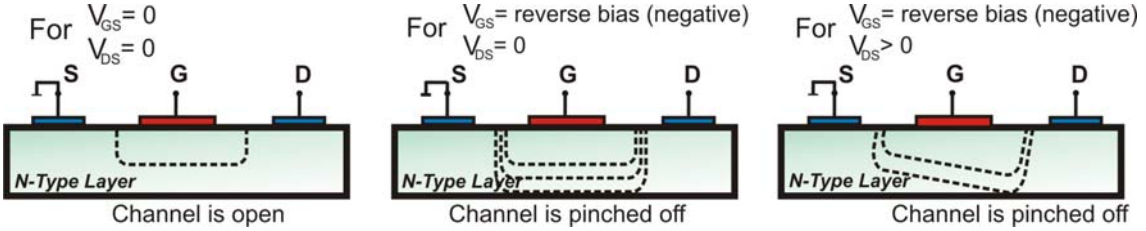


Fig.2.1. *Basic operation of the MESFET transistor*

The basic operation of a MESFET consists of a conducting channel positioned between the source and drain contact regions as shown in the previous figure. They are depletion mode type, being normally-*on* devices, thus requiring negative gate-source potential to deplete the carriers through the channel region and to turn the device off. The carrier flow from source to drain is controlled by the gate. The channel is depleted by applying a

negative voltage to the gate contact, which is in fact a Schottky junction. The control of the channel is obtained by varying the depletion layer width underneath the metal contact, which modulates the deepness of the conducting channel and thereby, reducing the current until it depletes at a certain gate voltage.

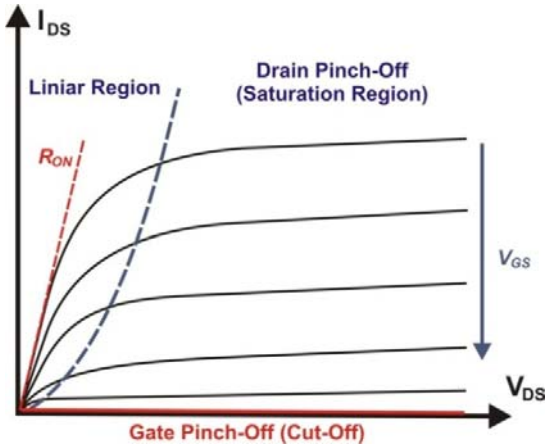


Fig.2.2. *Ideal current – voltage characteristics of a FET*

The MESFET is biased by applying two voltages, V_{GS} and V_{DS}. These voltages are used to control the I_{DS} current which is present between the drain and the source of the device by varying the electric field across the channel. The electric filed changes by varying the applied potential, giving rise to three distinct regions in the I-V characteristics of the device: Linear Region; Saturation Region and Pinch-Off Region.

At very low drain voltage, the drain current increases linearly with increasing drain voltage. In this linear region the FET exhibits a resistive characteristic with the resistance as a function of the gate voltage. As shown in Fig.2.2 the drain current increases with the drain voltage and becomes saturated at the pinch-off point. The "gradual channel approximation" can be considered in order to analyze the MESFET characteristics. This approximation, first done by William Schokley, essentially assumes that the gate width is much larger than its length (Z_G>>L_G).

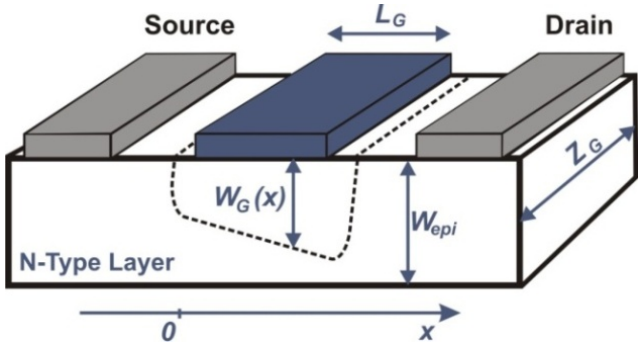


Fig.2.3. *Cross-section of a typical MESFET with main geometrical parameters*

By changing the geometrical parameters and technological processes, the saturation current can be adjusted and so the device can be optimized. In every case, this current mainly depends on the geometric parameters of the device: L_G-gate length, W_{epi}-epilayer depth, Z_G-Schottky gate width (see Fig.2.3); the N_D donor doping of the N epitaxial layer and the gate voltage V_{GS}.

$$I_{Dsat} = \frac{q^2 \mu {N_D}^2}{3\varepsilon_S} \cdot \frac{{W_{epi}}^3 Z_G}{L_G} \cdot \left[1 - 3\left(\frac{V_{GS}+V_{Bi}}{V_P}\right) + 2\left(\frac{V_{GS}+V_{Bi}}{V_P}\right)^{3/2}\right] \tag{2.1}$$

When the gate depletion region depth W_G equals the depth of the conducting epitaxial layer W_{epi} (see Fig.2.1b,c and Fig.2.3) the *channel is pinched-off*. The negative voltage at which no current flows from drain to source is called the ***pinch-off voltage*** (***V_P***) and it is a function of N-epilayer depth (W_{epi}) and its doping concentration (N_D). In the current-voltage characteristic (Fig.2.2), this behavior corresponds to the saturation region where the gate is pinched-off, and where the saturation drain current is described as in the eq. (2.1) [5].

The V_P expression is:

$$V_P = V_{DS} + V_{GS} + V_{Bi} = -\frac{q\, N_D\, {W_{epi}}^2}{2\, \varepsilon_s} \tag{2.2}$$

where V_{Bi} is the built-in voltage of the Schottky gate. When the gate bias is 0V, the saturation drain current is maximum:

$$I_{DsatMAX} = \frac{{W_{epi}}^3 q\, \mu\, Z_G}{3\, \varepsilon_S\, L_G} \cdot {N_D}^2 \tag{2.3}$$

The channel resistance (R_{ON}) is a function of the doping and determines the losses in the transistor. Therefore, R_{ON} is preferably as low as possible.

$$R_{ON} = \frac{1}{2\, q\, \mu\, N_D\, Z_G} \cdot \left(W_G - \sqrt{\frac{2\, \varepsilon_S}{q\, N_D} \cdot V_{Bi}}\right)^{-1/2} \tag{2.4}$$

As shown in Fig.2.2, the drain current I_D increases with the drain voltage V_D and becomes saturated at the pinch-off point.

Finally, the gain of the device, called *transconductance (g_m)*, represents the change of the drain current upon a change in gate voltage at a given drain voltage (eq. 2.5). A large transconductance is desirable to minimize the gate drive and provide a high power gain.

$$g_m = \left.\frac{\partial I_D}{\partial V_G}\right|_{V_{DS}=const} \tag{2.5}$$

2.2 The Mesa-MESFET Design and Fabrication

The MESFET structure is conventionally implemented on either semi-insulating substrates or *p*-type buffer epitaxial layers. In addition, the structure includes a thin highly doped *p*-type layer implanted at high energy, having the role of a second buried gate.

The mesa-devices were fabricated on 4H-SiC wafer supplied by CREE Research Inc. The P-layer grown on a semi-insulating substrate has a 5µm thickness with $5 \cdot 10^{15}$ cm^{-3} doping concentration, and the N-layer has 0,5µm thickness with 10^{17} cm^{-3} doping concentration. The fabricated mesa-MESFET has a single gate with the *p*-buried layer shorted to the source behaving as a buried gate. The schematic cross section of the fabricated device is presented in Fig.2.4. Employing the *p*-buried layer as a second gate allows the transconductance to increase [6].

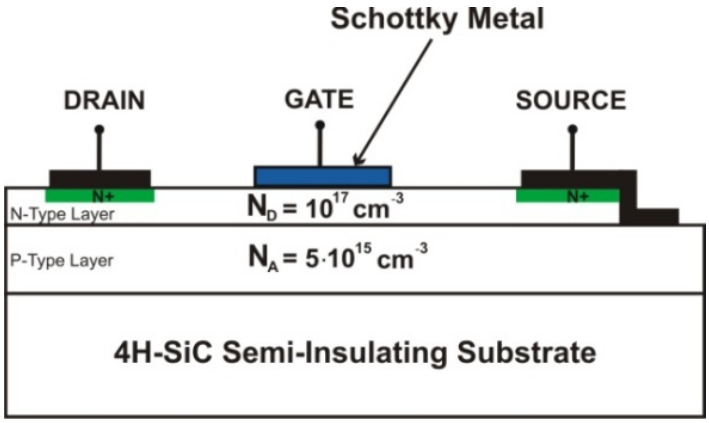


Fig.2.4. *Schematic cross-section of the 4H-SiC mesa-MESFET*

The technology developed in SPACESiC project is a multi-device process, demonstrating the fabrication compatibility between unipolar devices [7]. This technology has allows the integration of lateral MESFETs, LJFETs, Schottky, JBS, PiN diodes and small signal NPN bipolar transistor as well. It was also possible to integrate large value resistors with a reasonably small footprint thanks to the lightly doped P-epilayer. Varying the gate length (6, 8 or 12 µm) with a width of the devices varying from 400µm to 808µm, various MESFET structures were fabricated. However, due to our particular interest in investigating lateral MESFETs, the experimental analyses on a single mesa-MESFET type is satisfactory. Therefore, the experimental results presented in the following part are extracted from the transistors having 12µm of gate length with two different distances between the Source and Gate regions: 5µm and 7µm (see Fig.2.5).

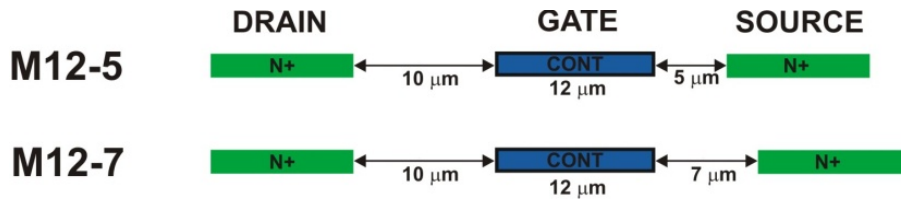
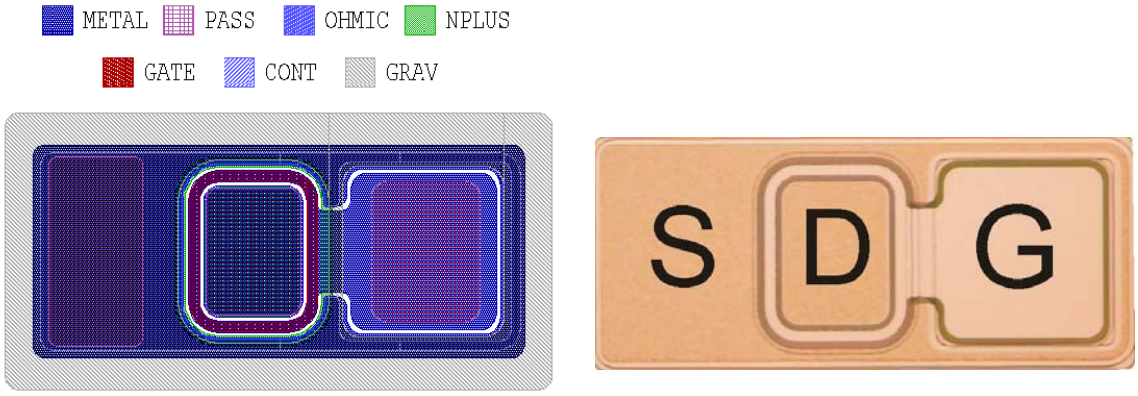


Fig.2.5. *Distances between electrodes of the analyzed MESFETs*

The geometrical approach used for the layout design is a *close-loop geometry* (Fig.2.6). This layout design has been proven to be suitable for the entire fabrication process, being perfectly suitable for mesa etching isolating technique. Moreover, this geometry layout is considered to be the best configuration for sustaining high voltages, as these devices have been specially designed for high power applications.



(a) ***(b)***

Fig.2.6.(a) *Layout design of the 4H-SiC Mesa-MESFET and* ***(b)*** *the fabricated MESFET transistors*

The fabrication process consists of 7 levels of photolithography masks, including mesa etching as the isolation technique, ion-implantation and impurity activation, field oxide formation, electrodes definition, ohmic contact formation, gate contact definition and pad metallization, and passivation. The mesa etching isolation was achieved in a standard reactive-ion etching (RIE) through a patterned deposited SiO_2 layer. Fig.2.6b shows a picture of the fabricated mesa-MESFET.

As our main interest is to develop a model for designing a new structure, to simplify the further analysis, in the next sections of the present chapter, the experimental results on mesa-MESFET M12-7 devices are presented.

2.3 The Mesa-MESFET Electrical Characterization

The normally-*on* lateral M12-7 MESFETs were characterized at room and at temperatures up to 300ºC. The aim of the present electrical characterization is to determine the entire set of electrical and geometrical parameters necessary for an accurate model development and after for designing a new MESFET structure.

2.3.1 Room Temperature Measurements

The DC characterization at room temperature was performed using the Keithley 251 IV SMU system, the Probe Station Wentworth A1050 and the ICS Metrics software. For the I_D-V_D forward characterization a gate potential was applied from 0V to –16V with –2V per step and with a drain bias ramping from 0V to +30V. The transconductance characteristics I_D-V_G were performed by keeping the drain bias constant at +30V and applying a gate bias ramping from 0V to –20V.

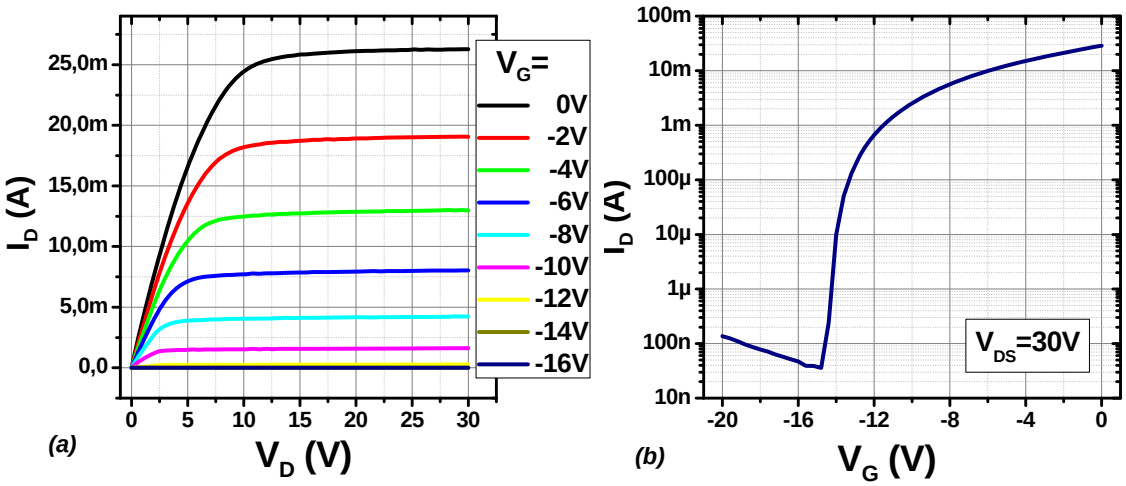


Fig.2.7. (a) *The output I_D-V_D characteristic and* ***(b)*** *the transconductance of M12-7 mesa-MESFET at room temperature*

From the output characteristic (Fig.2.7a) we can see that the saturation drain current for M12-7 is higher than 25mA at V_G=0V. From the transconductance curve can be roughly estimated that the pinch-off voltage is around V_P = -14.8V. The gain of the device (g_m) is calculated using eq. (2.6):

$$g_m = \frac{2 \cdot I_{DSS}}{|V_P|}\left(1 - \frac{V_{GS}}{V_P}\right) \tag{2.6}$$

The extracted transconductance value for the device at V_G=0V is g_m=3.901mS.

An important parameter for digital applications is the *on-off current ratio* (I_{ON}/I_{OFF}) which estimates the standby power consumption and the corruption of dynamic node voltages in logic and memory [8]. For the present mesa-MESFET the on-off current ratio is $\sim 2 \times 10^5$. For the Si CMOS logic products technology the general admitted values are between $\sim 5 \times 10^3$ and $\sim 2 \times 10^6$. Hence, this transistor is presenting acceptable values for future ICs development.

2.3.2 High Temperature Measurements

For the DC characterization at high temperature the Probe Station Wentworth s200 300ºC heating chuck system and two Keithley 2410 Source Meters, together with the LabVIEW software have been used. The measurement setup used was the same as for room temperature measurements, applying V_G from 0V to –16V with V_D ramping from 0V up to +30V, and keeping V_D constant at +30V while ramping V_G from 0V to –20V, for the I_D-V_D and I_D-V_G characteristics, respectively.

$$\mu_{n,p} = \mu_{min}\left(\frac{T}{300}\right)^{\beta} + \frac{\mu_{max}\left(\frac{T}{300}\right)^{\gamma} - \mu_{min}\left(\frac{T}{300}\right)^{\beta}}{1 + \left(\frac{N_A + N_D}{C_r}\right)^{\alpha}} \tag{2.7}$$

The detailed drain current expression was presented in eq. (2.1). Since the μ_n electron mobility eq. (2.7) varies as a function of temperature, the MESFET electrical parameters show a significant temperature dependency (Fig.2.8 and Fig.2.9).

In Fig.2.8 the drain current evolution for 6 different temperatures at 0V gate bias is presented. One can easily see that the drain current is strongly temperature dependent, decreasing approximately 3 times with the temperature increasing in the 25ºC-300ºC range. In accordance with literature [9, 10] the 4H-SiC electron mobility is decreasing with temperature, thus I_D follows the same trend. Due to this, the transconductance is decreasing at a proportional rate of approximately 80% at 300ºC.

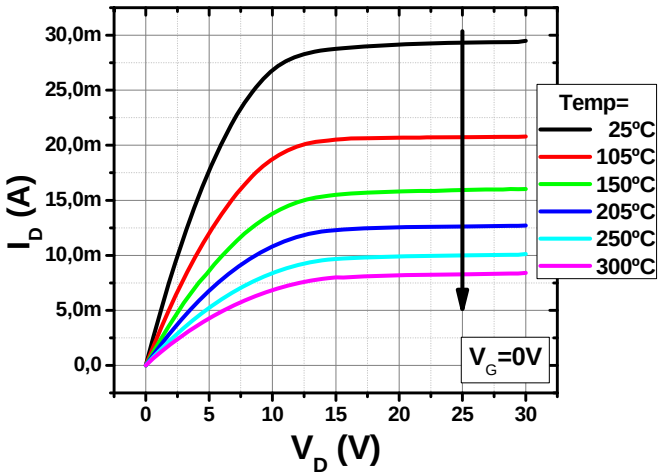


Fig.2.8. *The mesa-MESFT I_D-V_D characteristics for V_G=0V at 6 different temperatures*

From the transfer plot (Fig.2.9) it can be seen that the subthreshold leakage current shows a strong dependency with temperature as well, increasing nearly two orders of magnitude at 300ºC.

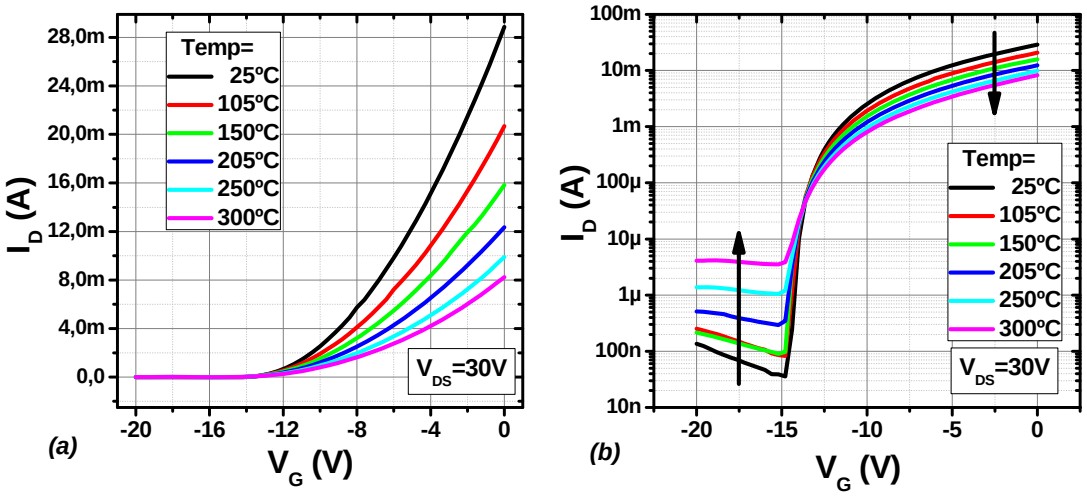


Fig.2.9. *The I_D-V_G at V_{DS}=0V characteristics of the mesa-MESFET in temperature* ***(a)*** *linear scale and* ***(b)*** *logarithmic scale*

From Fig.2.9 we can observe that the V_P is preserving a constant value in the whole temperature range, being in good agreement with theory (see eq. (2.2)). It is worth mentioning that for both MOSFET and Bipolar transistors, the threshold voltage shows an increasing dependence with temperature. Therefore, this is an important aspect that makes the MESFET and JFET much easier to model for high temperature operation.

2.4 The 4H-SiC Mesa-MESFET SPICE Model Definition

In order to be able to perform an electrical behavior forecast analysis of a prototype device, a proper simulation model is highly required. After almost three decades of running on various platforms around the world, SPICE [11] can be regarded as a standard in circuit's simulation. In the fast-advancing field of VLSI design, a sound knowledge of physical models used to describe the behavior of transistors and knowledge of various device parameters are essential for performing detailed circuit simulations and for an optimized design.

Although there is an increasing demand for intelligent power applications and intelligent sensors, there is a lack of high temperature SPICE models for SiC devices, which limits the design of embedded circuitry. However, several SiC devices are commercially available or have been demonstrated as prototypes. Thus, compact device models that are adequate for the simulations of power electronics circuits and systems are highly desirable. As one of the few commercial SiC switches, JFETs are now used in the build-up of power systems. As a MESFET has a similar structure and operation as the JFET, we have considered the SPICE model reported in [12] as a starting base in predicting the behavior of the 4H-SiC mesa-MESFET.

In order to develop an accurate SPICE model for the analyzed 4H-SiC mesa-MESFETs, the first step is to provide a correct extraction procedure for the electrical parameters employed in the model description, and later to include them in the model and verify if the simulated results are in good agreement with the experimental ones.

2.4.1 Parameters Extraction

In Table.2.1 the key parameters of the SiC MESFET that will be used for circuit simulation are summarized, including also the high temperature parameters. Beside intrinsic model parameters, extrinsic components are also considered for an accurate modeling.

Some of the parameters are extracted from the static characteristics of the device at room and at high temperature. The threshold voltage (V_{TO}), the transconductance modulation parameter (BETA), the channel length modulation parameter (LAMBDA), the

drain ohmic resistance (R_D), the source ohmic resistance (R_S), and the gate junction saturation current (I_S) are extracted from the room temperature characteristics.

Table.2.1. *MESFET Key SPICE Parameters*

Name	Parameter	*Units*
V_{T0}	Threshold voltage	*V*
BETA	Transconductance parameter	*A/V^2*
LAMBDA	Channel length modulation parameter	*V^{-1}*
R_D	Drain ohmic resistance	*Ohm*
R_S	Source ohmic resistance	*Ohm*
I_S	Gate junction saturation current	*A*
C_{GS}	Zero-bias G-S junction capacitance	*F*
C_{GD}	Zero-bias G-D junction capacitance	*F*
PB	Gate junction potential	*V*
M	Junction grading coefficient	-
KF	Flicker-noise coefficient	-
AF	Flicker-noise exponent	-
FC	Coefficient for forward-bias depletion capacitance - Formula	-
TNOM	Parameter measurement temperature	*ºC*
XTI	IS temperature coefficient	-
$VT0_{TC}$	Threshold voltage temperature coefficient	*V/ºC*
$BETA_{TCE}$	Transconductance exponential temperature coefficient	*1/ºC*

As shown in Fig.2.10a, the device transconductance parameter β and the threshold voltage V_{T0} are obtained from the transfer characteristics. After a linear fitting was performed, the results were:

$$\text{Slope} = \sqrt{\beta} = 0.012 \Rightarrow \beta = 0.144\ \text{m A/V}^2 \tag{2.8}$$

And the threshold voltage obtained at the intersection of the fitting with the *x*-axis, is resulting in:

$$V_{T0} = -14.202\ \text{V} \tag{2.9}$$

The channel-length modulation parameter λ is gained out from the output characteristics of the device. In Fig.2.10b the drain current is plotted only for gate potential V_G=0V and the value for the channel-length modulation parameter is:

$$\text{Slope} = \lambda \cdot I_D = 5.823 \cdot 10^{-5} \Rightarrow \lambda = 2 \cdot 10^{-3}\ 1/V \qquad (2.10)$$

Since the devices are designed to operate at high temperature, the temperature coefficients are especially important in the circuitry design. The key temperature parameters are: the I_S temperature coefficient (XTI), the threshold voltage temperature coefficient (VTO_{TC}), and the transconductance exponential temperature coefficient ($BETA_{TCE}$).

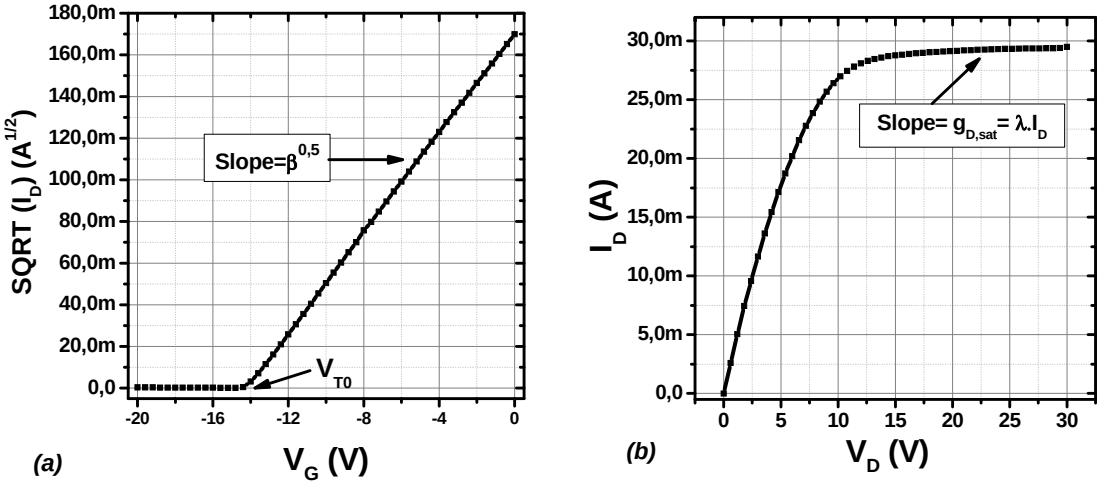


Fig.2.10. *The close-loop MESFET* ***(a)*** *transfer characteristic and* ***(b)*** *output characteristic at V_G=0V*

The threshold voltage temperature coefficient (VTO_{TC}) can be extracted if the V_{T0} is plotted as a function of temperature (Fig.2.10a). The threshold voltage V_{T0} varies with temperature according to the following equation:

$$V_{T0}(T_2) = V_{T0}(T_1) + VTO_{TC}(T_2 - T_1) \qquad (2.11)$$

As expected, the threshold voltage varies with temperature (Fig.2.11a) due to the higher subthreshold leakage current observed at elevated temperatures.

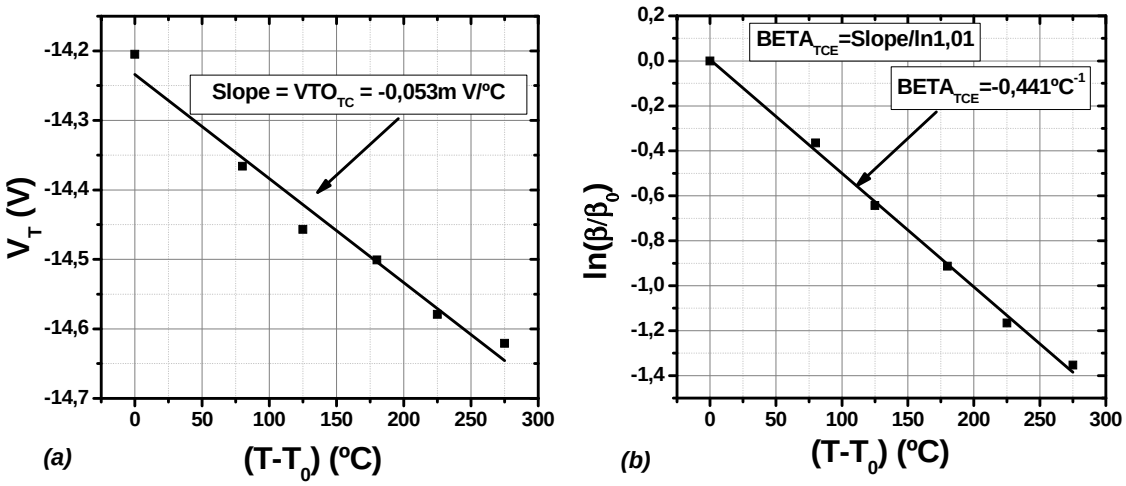


Fig.2.11.*The extraction method and values for* ***(a)*** *the threshold voltage coefficient (VTO_{TC}) and* ***(b)*** *the transconductance exponential temperature coefficient ($BETA_{TCE}$)*

The transconductance exponential temperature coefficient $BETA_{TCE}$ can be expressed in terms of the equation (2.12) below and determines the limit of saturation current level at elevated temperature:

$$\beta(T_2) = \beta(T_1) \cdot 1.01^{BETA_{TCE}(T_2 - T_1)} \qquad (2.12)$$

Moreover, due to the higher on-resistance which limits the current level, the device transconductance correspondingly drops as temperature increases (Fig.2.11b).

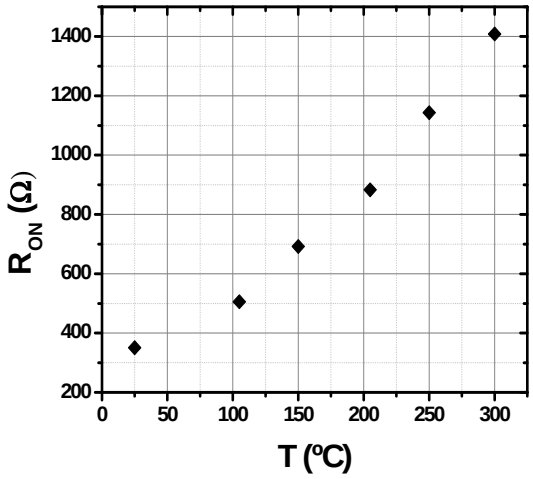


Fig.2.12.*Temperature dependence of the on-state resistance at V_G=0V for mesa-MESFET*

The on-state resistance (R_{ON}) contributes to the conduction losses of the device. As shown in Fig.2.12 the R_{ON} increases with temperature, following a parabolic law. Therefore, the conduction losses will become more important and not negligible when the device is operating at high temperatures. Equation (2.4) shows the R_{ON} dependence on mobility, thus its increment with temperature can be straight forward explained.

As the main difference between the JFET and MESFET devices lies on the gate architecture, some of the SPICE parameters have to be modified. For instance, the junction grading coefficient M and the gate junction potential PB are parameters dependent on the gate Schottky junction and they are considered 1 and 1.3V, respectively. However, other parameters will be considered as default from the SiC-JFET SPICE model because of the similarity.

Finally, all the extracted parameters from the experimental measurements will be introduced in the SPICE model in order to customize it for the mesa-MESFET transistor. Table.2.2 shows the extracted MESFET parameters, together with the default ones from JFET SPICE model. The complete mesa-SPICE model is described in ***Annex.A1*** *– Mesa-MESFET Extracted SPICE Model*.

Table.2.2. *The extracted key parameters for the 4H-SiC mesa-MESFET SPICE model:*

Parameter	Value	*Units*	Parameter	Value	*Units*
V_{TO}	-14.2	*V*	**M**	1	-
BETA	0.144	mAV^{-1}	**KF**	0	-
LAMBDA	2E-3	V^{-1}	**AF**	1	-
R_D	0	*Ohm*	**FC**	0.5	-
R_S	0	*Ohm*	**XTI**	3	-
I_S	0	*A*	**VTO_{TC}**	-0.053	mV^oC^{-1}
PB	1.3	*V*	**$BETA_{TCE}$**	-0.441	$^oC^{-1}$

An important specification should be made concerning the threshold voltage V_{T0} mentioned in the SPICE model parameter extraction procedure. In our case, the threshold voltage is considered to have the same meaning and value as the MESFET pinch-off voltage.

2.4.2 Simulated vs. Experimental Results

Using the customized SPICE model of our mesa-MESFET, typical electrical simulations were performed, being able to obtain a first comparison between the experimental and simulated characteristics of the device.

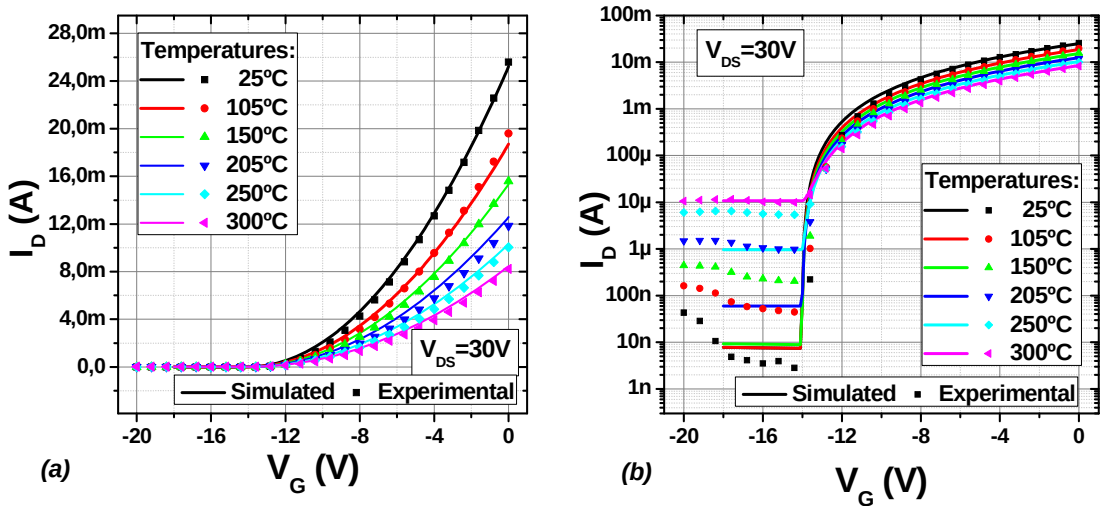


Fig.2.13. *The I_D-V_G simulated and experimental characteristics of a mesa-MESFET in temperature in* ***(a)*** *linear scale and* ***(b)*** *logarithmic scale*

Fig.2.13 shows with solid lines the SPICE simulations and with symbols the experimental measurements of the transconductance characteristic of the 4H-SiC mesa-MESFET for all measured temperatures. One can easily see that a good agreement between the extracted SPICE model and the experimental results is obtained in both linear and saturation regions, for both room and high temperature behavior. This indicates that the customized SPICE model of 4H-SiC mesa-MESFET can be considered a cogent starting point in the design and modeling of a new structure for high temperature operation.

Therefore, the proposed SPICE model for the mesa-MESFET is a key input parameter in future development of the new MESFET structure. This model can easily be modified and furthermore used in the new structure design and simulation.

2.5 Theoretical vs. Experimental Analysis Comparison

In order to see if the previous experimental analysis of the mesa-MESFET is corresponding to the theoretical one, this section deals with brief remarks concerning key electrical and geometrical parameters.

For the sake of simplicity, we remind that the 4H-SiC wafer consists of a semi-insulating substrate, with 5μm thickness P-type epilayer and a W_{epi}=0.5μm N-type epilayer thickness. The doping concentration are $N_A=5\cdot10^{15}$ cm^{-3} and $N_D=10^{17}$ cm^{-3}, respectively.

2.5.1 Theoretical Analysis

We have previously shown that the required voltage to fully deplete the doped channel layer of the MESFET is the threshold voltage:

$$V_T = V_{Bi} - \frac{q\cdot N_D\cdot W^2}{2\cdot\varepsilon_S} = V_{Bi} + V_P \tag{2.13}$$

where V_{Bi} is the build-in potential (1.3V) and V_P is the pinch-off voltage of the device. Considering the pinch-off voltage eq. (2.2), we can easily calculate its theoretical value:

$$V_P = -\frac{q\cdot N_D\cdot {W_{epi}}^2}{2\cdot\varepsilon_S} = -18.95\ V \tag{2.14}$$

From the equation (2.14), we can see that q and ε_S are known fixed constants, while the parameters that can vary are the N-layer doping and its thickness W_{epi}. However, the actual value of the N_D doping is provided by the wafer supplier. Since no additional implantation in the gate region was performed, the N-layer concentration remains constant along the entire manufacturing processes. Therefore, the only parameter able to be modified due to the extra cleaning procedures and etching steps during the device fabrication process is the W_{epi} thickness of the epilayer.

As can be seen from the device cross-section (Fig.2.14), the device contains two junctions: the metal-semiconductor junction – *the Schottky junction*, formed between the gate metal and N-type layer; and *the pn-junction*, formed between the N- and P-type layers. In order to evaluate them, we will analyze each separately.

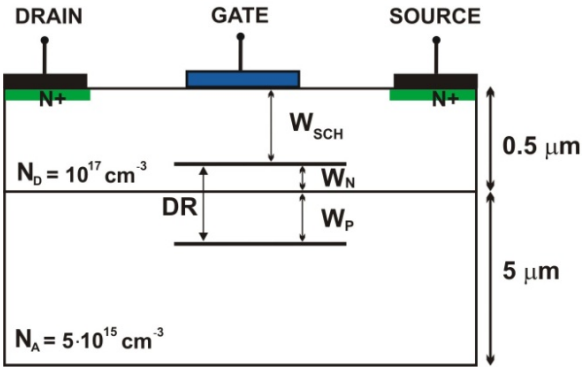


Fig.2.14. *The schematic cross-section of the 4H-SiC mesa-MESFET with the depletion-regions (DR)*

a) *PN* junction

Giving that the P-layer doping concentration is considerably lower than the N-layer one, the *pn*-junction depletion region (DR) expands more in the P substrate. In the neutral regions of the semiconductor the electric field has to be null; therefore, the total charges must be equal at both sides of the junction:

$$W_N \cdot N_D = W_P \cdot N_A \tag{2.15}$$

The theoretical expression of the total thickness of the depletion region is:

$$W_{DR} = W_N + W_P = \sqrt{\frac{2 \cdot \varepsilon_r}{q \cdot N_i} \cdot \Phi_0} \tag{2.16}$$

where Φ_0 is the internal potential of the *pn*-junction:

$$\Phi_0 = V_{th} \cdot \ln\left(\frac{N_A \cdot N_D}{{n_i}^2}\right) = 2.92\ \text{V} \quad \text{and} \quad N_i = \frac{N_A \cdot N_D}{N_A + N_D}$$

with the thermal voltage: $V_{th} = k \cdot T/q = 26\text{mV}$ at T=25ºC. The intrinsic carrier concentration n_i and the relative permittivity ε_r are taken from Table.1.1.

Combining the above equations, the depletion region thicknesses for each of the two doped layers can easily be calculated:

- for the N-type layer: W_N=0.038 μm and
- for the P-type layer: W_P=0.774 μm.

Therefore, the *pn*-junction DR is extending 0.038μm inside the N-type layer.

b) Schottky junction

In the Schottky junction case, the depletion region is expanded only in the N epilayer under the gate metal:

$$W_{SCH} = \sqrt{\frac{2 \cdot \varepsilon_r}{q \cdot N_D} (V_{Bi} - V_R)} \tag{2.17}$$

where the typical internal potential for a Schottky junction is $V_{Bi} = 1.28V$.

When the polarization voltage has reached the pinch-off voltage V_R=V_P=-18.95V the channel is completely depleted. From eq. (2.17) we yield the Schottky junction depletion region width: $W_{SCH} = 0.467\ \mu m$.

Therefore, in order to confirm if the theoretical analysis is reliable, we can verify if the calculated value of the N-type layer thickness corresponds to the initial one:

$$W_{epi} = W_{N-layer} = W_{SCH} + W_N = 0.5\ \mu m \tag{2.18}$$

Using the theoretical analysis, electrical and geometrical parameters were determined. We have shown that the analytical approach was correct. In the following part, the same parameters will be extracted from the experimental results.

2.5.2 Experimental Analysis

If we have a closer look at the experimental extracted parameters (Section 2.4.1) and the previous theoretical analysis, we can easily observe that between some theoretical and experimental electrical parameters there is a visible variation.

The extracted value from the experimental measurements of the pinch-off voltage resulted to be V_P=-14.2V (see eq. (2.9)). If we replace this value into the Schottky depletion region width equation (2.17), it will result that the actual Schottky-DR is in fact $W_{SCH} = 0.408\ \mu m$.

Therefore, in order to estimate the actual thickness of the N-type epilayer, we sum the actual Schottky-DR with the *pn*-junction DR (which maintains the same value):

$$W_{epi} = W_{N-layer} = W_{SCH} + W_N = 0.446\ \mu m \tag{2.19}$$

From the upper values we can observe that at the end of the manufacturing processes of the device, the experimental thickness of the epitaxial layer has resulted smaller than its initial value.

The variation between the theoretical and experimental values of different mesa-MESFETs geometrical and electrical parameters is a consequence of the various fabrication process steps, such as deep cleanings, surface oxidation or over-etchings of the oxides, and associated manufacturing tolerances.

Consequently, this analysis presents an important aspect – the fabrication processes' impact on the wafer and device parameters. This aspect will be taken into consideration for the future devices and circuits design, modeling and fabrication. In Fig.2.15 is shown the theoretical dependence of the V_P versus the N-substrate thickness pointing out the effects of the fabrication process steps.

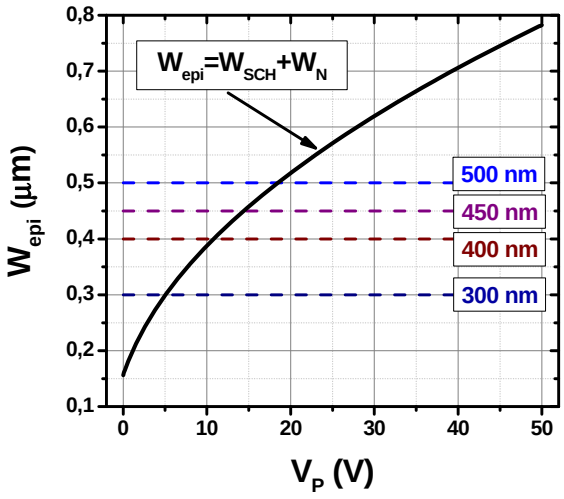


Fig.2.15. *The 4H-SiC N-substrate thickness versus MESFET pinch-off voltage*

Therefore, an important conclusion can be stated: the geometrical parameter W_{epi} – the N-type layer thickness can be varied in order to obtain the desired device parameters, such as V_P – one of the important electrical parameter on which the device electrical operation scaling is reflected on.

2.6 Conclusions

After presenting the basic MESFET transistor operation, pointing out the structural and functionality similarities with the JFET, the complete characterization of the existing mesa-MESFET device was reported. This device was isolated using mesa technique and has required 7 levels of photolithography for its fabrication.

From experimental measurements at room and high temperature, it was shown that the mesa-MESFET presents a good behavior in the 25ºC to 300ºC temperature range, showing again the 4H-SiC Tungsten-Schottky gate fabrication maturity.

It has been shown that starting from a SiC JFET SPICE model specially created for circuitry simulations, a new SPICE model for MESFET devices can be defined. Based on the experimental characterization, a first SPICE parameter extraction was performed at room and high temperatures. Introducing all the extracted parameters into the SPICE model, first simulations were carried out. A good agreement between the simulated results and the experimental ones for the whole temperature range (25ºC-300ºC) was obtained, demonstrating the effectiveness of the customized mesa-MESFET SPICE model.

It has been also pointed out that the fabrication process can induce variation from the theoretical values of different geometrical and electrical parameters of the device. It has been observed that a lower pinch-off voltage is obtained experimentally, due to the final lower thickness of the N-epilayer. This fact will be taken into consideration in the development of the future structure.

The study reported in this chapter has a significant importance as it will be used as an input base for the future developed devices.

2.7 References

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CHAPTER III

The Novel 4H-SiC Planar-MESFET

New Developed Device

This chapter reports the design, fabrication and characterization of the new developed ***4H-SiC planar MESFETs dedicated for high density circuit's integration***.

As the purpose of the new structure is to be integrated in future circuit development containing a large device number, it appears the necessity to accomplish some of the most important integrated circuits requirements, generally applicable to Si-ICs:

- *Wafer planarity* – it assures good interconnections between different metal levels of the circuit, especially when multiple metals are necessary for devices interconnection.
- *Device scalability* – it offers important advantages in circuit's design flexibility and chip area reduction.
- *Multi-level interconnection* – it highly increases the device integration density.

Therefore, some important and novel design and fabrication features have been applied in the development of the new structure:

a) The used *isolation technique* is a novel technique and, to our knowledge, has been utilized for the first time in SiC.

b) The *transistor layout* approach is typically used in the Si CMOS ICs.

c) The *process flow* is fully compatible with CMOS processes.

The groundwork of the present MESFET transistor mainly relies on the electrical and geometrical analysis performed in the previous chapter for the already fabricated mesa-MESFET.

3.1 The Planar-MESFET Design and Modeling

As already mentioned, the design and device modeling plays a crucial role in developing a new structure. Due to the changes that occur in the semiconductor device and also the difficulty encountered in performing measurements on these devices, a great emphasis has to be put on the theoretical results. At this stage, the new device structure is rigorously investigated prior fabrication.

Since the physical model of the device is already known thanks to its previous fabrication analysis (Chapter II), the design and modeling of the new structure will mainly refer to the equivalent circuit model approach, changing only few electrical and geometrical parameters. The key parameters which will be taken into consideration while designing a digital circuit at transistor level are: the saturated current (I_{Dsat}), the pinch-off voltage (V_P) and the leakage current (when the device is off). Furthermore, the most important changes for the new developed structures are described.

3.1.1 The P^+-Implanted Walls Isolation Technique

A significant aspect that we have considered in developing the new structure is the *isolation technique* of the devices. As we showed in the previous chapter, the isolation method used for the SPACESiC developed devices was the mesa etching isolation. Using mesa isolation technique, the 4H-SiC MESFETs have shown a proper behavior up to 300ºC (Section 2.3.2). This method has proven to assure a good isolation between devices and it is widely used for individual device definition due to its simplicity [1]. However, as the *planarity* is an important standpoint in developing ICs, using mesa isolation brings inappropriate differences between the necessary metal levels for circuit's device interconnections.

The isolation method widely used for the design and fabrication of Si ICs is the *junction isolation technique*. This technique was formerly used for the early design and fabrication technology of Si ICs based on bipolar transistors by P type diffusion. We have adapted the junction isolation technique, using fully implanted isolation walls, as the impurities diffusion in SiC is not possible.

The P^+-type impurities are deeply implanted into the N-type epitaxial layer so that it reaches the P-type substrate, creating N-type islands. This method generates N-type wells surrounded by P-type moats in which individual components are implemented. A comparison between the mesa and junction isolation techniques on SiC is reported in [2]. The schematic cross-section of the new proposed 4H-SiC MESFET structure using the P^+-implant technique as a device isolation method is showed in Fig.3.1.

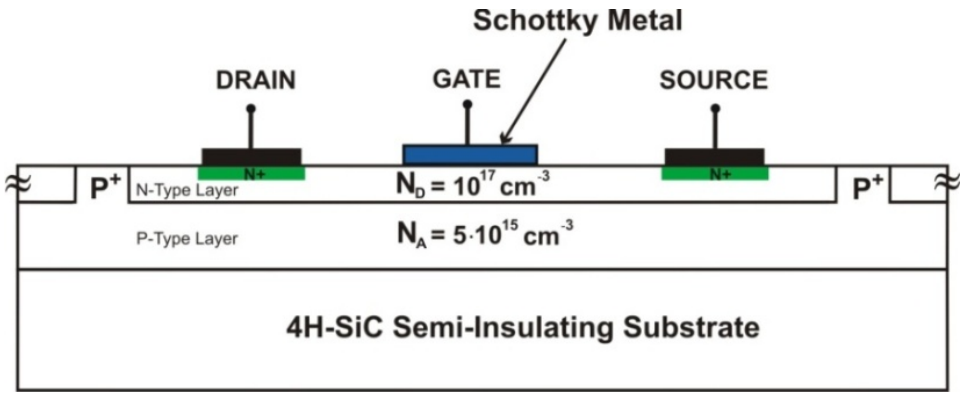


Fig.3.1. *Schematic cross-section of the 4H-SiC MESFET with P^+ implant isolation*

The *benefits* of using the P^+-implanted isolation process are the improvement of the device density per unit area and the wafer surface. Since a number of devices are to be fabricated on the same IC chip, it becomes necessary to ensure good isolation between various components and also good interconnections. Moreover, this method offers not only a good isolation between devices, but it also provides a *better planarization of the wafer surface*, and also reliable interconnection between various devices or circuits. Therefore, this isolation technique adapted from Si-CMOS technology is our choice for 4H-SiC individual device definition. More details about this technique will be provided in the device fabrication Section 3.2.

3.1.2 Device Scalability

One of the most important aspects in developing ICs is the necessity of having *scalable devices.* The technique widely used in CMOS ICs for achieving this aspect is the *finger-gate technique* [3]. Device scalability brings important advantages, such as the improvement of both circuit speed and density increase [4]: a) the circuit operational frequency increases with a reduction in gate length, allowing faster circuits; b) the chip area decreases while using finger-gate devices instead of close-loop gate structures, enabling higher integration density; c) the switching power density remains constant allowing lower

power per function or more circuit complexity for the same power; d) using finger-gated transistors, the drain-sharing technique becomes applicable.

The MESFETs are endowed with a higher degree of freedom in scaling, unlike MOSFETs in which the scaling requirements for various device parameters are highly interrelated [5]. The absence of the gate-oxide in the MESFETs enables the flexibility in the choice of the channel thickness and also of the channel doping. Moreover, the ion implantation enhances this flexibility [6].

Reference [4] shows several scaling schematics for the Si-MESFET varying either the channel thickness, the channel doping, or even both. These schemes are compatible with the techniques used for the V_P reduction in the depletion mode GaAs devices [7] and also for controlling the V_P in enhancement Si and GaAs MESFETs [8-11]. Depending on the required applications, different combinations concerning parameters scaling can be chosen.

The MESFET basic operation is presented in Section 2.1. As shown in [4] one of the most important electrical parameter concerning scaling is the V_P due to its dependency with geometrical and physical parameters of the structure.

3.1.3 The SiC Planar Transistor Layout

The device layout is another important matter in designing a new structure, mainly depending on its final application. The geometry adopted for the new SiC device is completely different than the one previously presented.

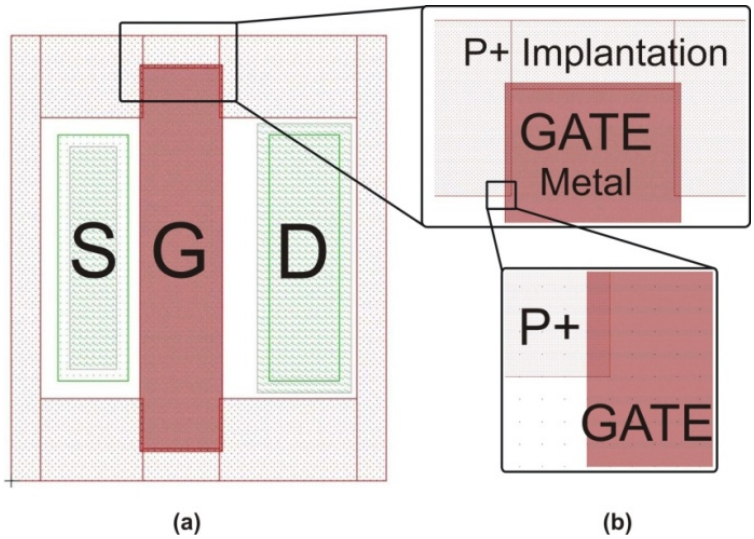


Fig.3.2. *The finger geometry layout for MESFET m=1 using P^+-implant isolation wall (a) general view and (b) geometry trick*

The embraced *finger-gate technique* allows applying *the concept of transistor multiplicity*, which accomplishes the *scalability* requirement. The proposed transistor layout is showed in Fig.3.2a where the P^+-implanted isolation ring can be observed (the light red ring).

In order to have an appropriate comparison with the closed-loop MESFET, the gate electrode ratio Z_G/L_G (see Fig.2.3) for the novel single gate device is considered to be roughly 10 times smaller than the mesa-MESFET's, hence having the effective gate contact dimensions of 48µm x 8µm. However, due to the special fabrication processes on SiC, the embraced geometry presents a built-in drain-source residual current at the terminals of the gate metal (Fig.3.2a). In order to minimize it, a geometry trick was adopted on the lateral edges of the gates (Fig.3.2b). An extra oxide gated MESFET, 25 times smaller than the main MESFET, was implemented under the prolonged gate metallization (0.5µm), in order to block any residual drain-source leakage current. This oxide gated MESFET shows a slightly higher V_P than the main one. In order to have a more accurate and realistic simulation setup, it was taken into consideration in the SPICE model (Fig.3.4).

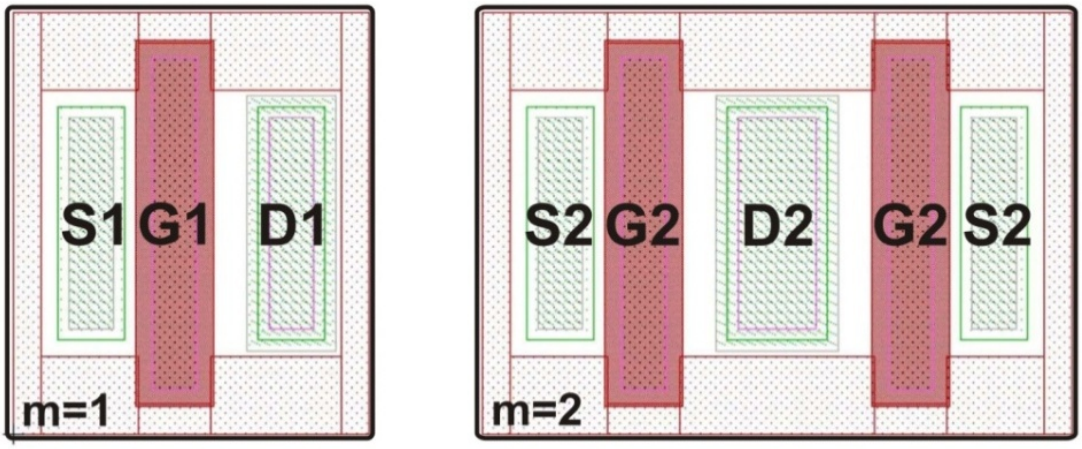


Fig.3.3. *The layout of different multiplicity MESFETs isolated with deep P^+-ring implantation*

Fig.3.3 shows the layout for the proposed multiplicity MESFETs isolated by implanted *pn*-junctions. As observed from the MESFET with multiplicity 2 (m=2) the *drain-sharing technique* was adopted [12], a method that brings great improvements in device area reduction, and also decreases the parasite source resistance with the increasing of the finger-gate number. Details concerning device dimensions and its design rules checking (DRC) can be found in ***Annex.B*** *– The Planar-MESFET Dimensions and DRC rules.*

3.1.4 The New MESFET Proposed SPICE Model

Section 2.4 reports the first extracted SPICE model customized and optimized for the 4H-SiC mesa-MESFET in order to accurately describe its static and switching performances. For designing a new and scalable MESFET device with the above proposed geometry layout, several geometrical and electrical aspects have to be considered in the SPICE simulation. As mentioned before, one of the most important electrical parameter is the device V_P.

As previously mentioned, the geometrical parameters which have to be changed for the novel MESFET are related with the width and length of the gate electrode. In addition, the gate trick adopted in order to block the residual drain-source leakage current, corresponds to a 25 times smaller (MESFET m=0.04) transistor, placed in parallel with the main MESFET.

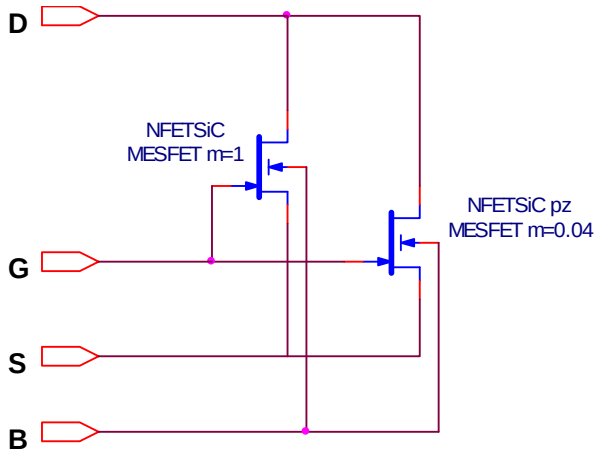


Fig.3.4. *SPICE equivalent circuit of the 4H-SiC MESFET*

Hence, the new planar MESFET structure requires a more complex SPICE model. As one can observe from Fig.3.4 the extrapolated SPICE model for a single IC transistor involves two devices in parallel. However, the difference between the two devices is only the Z_G/L_G ratio and the V_P. The equivalent MESFET is thus described by a sub circuit.

Table.3.1 is summarizing the key SPICE model parameters used for circuit simulations of the new 4H-SiC MESFET. We have previously shown that the device V_P is directly dependent on the N-type layer thickness. For the new structure we have targeted a smaller value for V_P, which implies to use a smaller thickness of the N-epitaxial layer. The corresponding value for the N-type epitaxial layer thickness for V_P=-8V is 0.35µm (see

Fig.2.15). The oxide gated transistor has a slightly higher pinch-off voltage than the main one (V_P=-12.5V) due to the oxide contribution.

The main reason why V_P has been considered lower was for lowering the power consumption and the logic levels of the digital circuits. For a proper functionality, the voltage level of the power supplies should be roughly 30% higher than 2 times the V_P of the SiC MESFETs. Thus, for a lower V_P the power supply voltage could decrease significantly. More explanations can be found in the circuitry section – Chapter V.

Table.3.1. *The key parameters for the main 4H-SiC planar-MESFET SPICE model:*

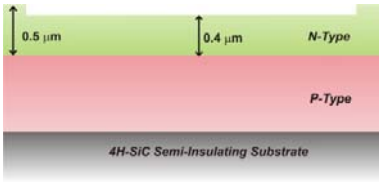
Parameter	Value	*Units*	Parameter	Value	*Units*
V_{TO}	-8	*V*	**M**	1	-
BETA	0.3125	AV^{-1}	**KF**	0	-
LAMBDA	2E-3	V^{-1}	**AF**	1	-
R_D	0	*Ohm*	**FC**	0.5	-
R_S	0	*Ohm*	**XTI**	3	-
I_S	0	*A*	**VTO_{TC}**	-0.053	mV^oC^{-1}
PB	1.3	*V*	**$BETA_{TCE}$**	-0.441	$^oC^{-1}$

The complete extrapolated SPICE model for the main new MESFET, corresponding to the equivalent circuit from Fig.3.4, can be found in ***Annex.A2*** *– SPICE Model for the Planar-MESFET – The Design Model*. This model was further used in designing and simulating all digital SiC ICs.

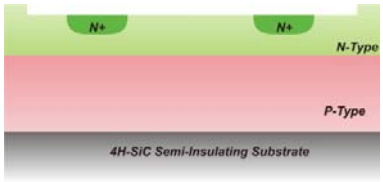
3.2 The Planar-MESFET Process Flow

The schematic cross-section of the proposed structure is shown on Fig.3.1. The devices are fabricated on 4H-SiC wafer supplied by CREE Research Inc. with similar material proprieties as for the mesa-MESFETs (Section 2.2). The major fabrication steps of the new MESFET are summarized in Table.3.2:

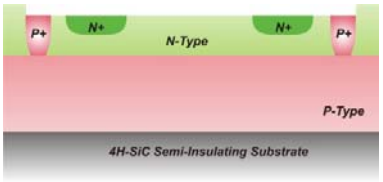
Table.3.2. *The main steps in the 4H-SiC integrated MESFETs fabrication process*



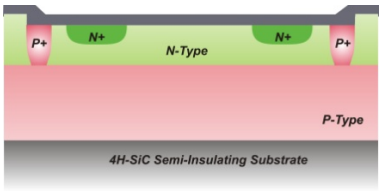
a. Align patterns



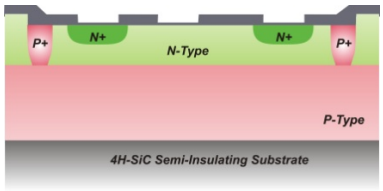
b. N^+ Nitrogen implant



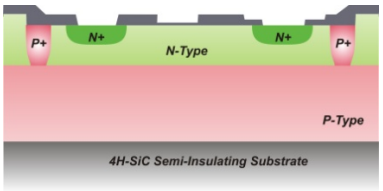
c. P^+ Aluminum implant



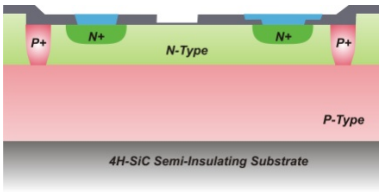
d. Field oxide deposition



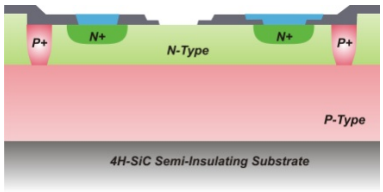
e. Partial contact openings for the 3 terminals



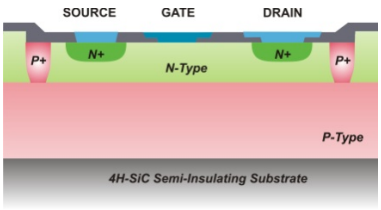
f. Source and Drain – Ohmic contact etch



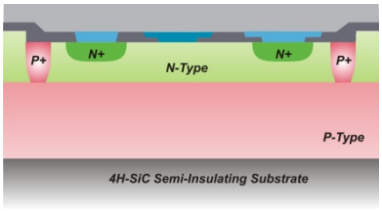
g. Source and Drain contacts metallization



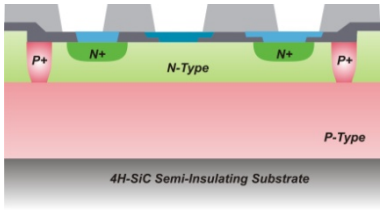
h. Gate contact etch



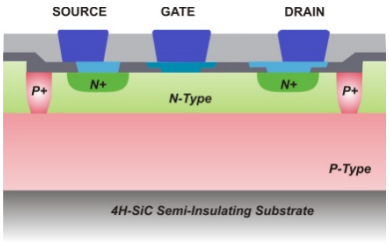
i. Gate contact metallization – Basic MESFET Transistor



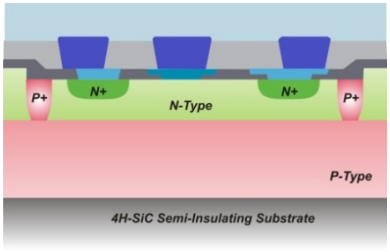
j. Inter-level oxide



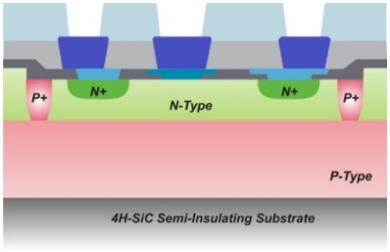
k. Contact oxide opening



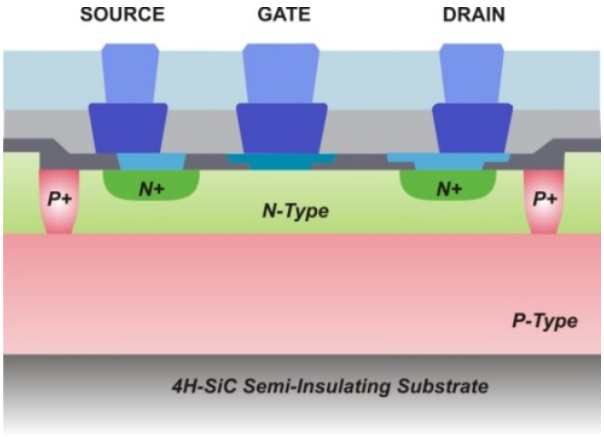
l. Second metallization level



m. Inter-level thick oxide



n. Via oxide opening



o. Third-level metallization – ***Integrated MESFET circuits connections***

1. The first step is the definition of the *alignment* pattern on the wafer surface. Within this step the N-type epitaxial layer thickness was 1000Å lowered on the active area through a dry etching step (Table.3.2a).

2. Next, the areas for high dose Nitrogen implantation (N^+ *implanted areas*) were patterned to define the *Source and Drain regions*. Multiply Nitrogen implants with high energies and doses up to $3 \cdot 10^{14}$ at/cm^2 were used to achieve a box doping profile (Table.3.2b).

3. The *P^+-implant* areas were patterned to define the isolation walls and obtained after several accumulated Aluminum implantations at energies around 160keV and doses up to $3.3 \cdot 10^{14}$ at/cm^2. The Aluminum implanted moats have a P^+ concentration higher than 10^{19}cm^{-3}, so that the penetration depth is higher than the N epilayer thickness in order to reach the buried P-type layer (Table.3.2c).

4. After the N^+ and P^+-implantations were performed, the wafer was annealed up to 1600ºC for 30min in N_2 atmosphere in order to electrically activate the impurities. A post oxidation process was performed to passivate the SiC wafer surface.

5. Next, a 3µm thick *field oxide* was deposited on the SiC surface. Through the *CONT mask* the oxide was not completely etched, and so the *contacts windows for the electrodes* were formed (Table.3.2d,e).

6. The *Source and Drain electrodes* were formed through the *OHMIC mask*. After etching the left field oxide, the source and drain ohmic contacts were formed with 100nm of Nickel patterned by lift-off and after annealed to 950ºC for 2 min to form a silicide (Table.3.2f,g). At this step, the drain overlap was realized.

7. The *Gate terminal* was formed by etching the left oxide through the *Gate mask*, thus realizing the gate overlap. A Tungsten layer of 100nm was deposited as the gate Schottky metal, patterned by lift-off and then annealed at 500ºC for 2min (Table.3.2h).

8. Furthermore, an *inter-level thick oxide* was deposited. Through the *first VIA mask* the oxide layer was opened at the source, drain and gate contact areas. It was patterned by a reactive ion etching (RIE), which allows well controlled etch rates with nearly vertical sidewalls (Table.3.2j,k).

9. On the terminal contacts, a *thick metal* was sputtered consisting of a *stack of Ti and W*, which was patterned by wet-etch. This contact metal alloy is the second metal level on the wafer and is used for further interconnections between devices (Table.3.2l).

10. Next, *one more inter-level thick oxide*, 1µm thick, was deposited. Using a *second VIA mask* the oxide layer was etched by RIE on different pre-selected areas defined in the layout, in order to make openings that reach the underneath metal level (Table.3.2m,n)

11. Finally, a last *thick metallization* level consisting of a stack of Ti and Al was patterned by wet-etch through the last *METAL mask* (Table.5.2o). This is the last photolithography necessary to complete the fabrication process of the SiC planar MESFET.

Then, the wafer was metalized on its back side with a thick stack of Ti, Ni and Au.

It is worthy to mention some observations concerning the previous process flow. An oxide overlap was used as a field plate for the Gate terminal (Table.3.2e,h). The gate overlapping between the gate and the source/drain regions is required to ensure that the depletion layer provides a conducting path between the source and drain areas. This overlap is made as small as possible in order to minimize its parasitic capacitance. The field plate was achieved after performing the contact openings, while the oxide, left on the gate contact, was etched.

The drain contact overlap was made in order to increase the device breakdown voltage by adding the additional depletion region created around the drain periphery, to the Schottky depletion region (Table.3.2e,f).

During the device fabrication, a special attention was paid to the lift-off technique. This method is applied in cases in which a direct etch of structural material would have undesirable effects on the layer below. However, the issues that may appear during this process can be overtaken by special cleaning techniques along the fabrication processes. This is why, in the next part, verification measurements after the contact metal deposition have been performed.

Therefore, the basic MESFET was isolated using an Aluminum implant process that forms a *pn*-junction. Once the P^+-impurities are deeply implanted into the N epilayer, they reach at the bottom the P layer forming N-wells surrounded by a P^+-ring. If the P-substrate is held at the most negative potential, the pn-junction will become reverse-biased, thus providing isolation between these islands.

Even though one of the challenges in designing a new device lies in the reduction of the fabrication step number, to achieve the final fabrication of the IC MESFET, 10 levels of photolithography masks were needed, three more than for mesa-MESFET. One was especially needed for the N-type tubs, whereas the last four were required for forming the interconnection metal strips between devices and circuits.

In the next part, the electrical characterization of fabricated devices is presented, pointing out the successful achievement of the novel isolation on SiC, the multiplicity device realization and the proper high temperature operation.

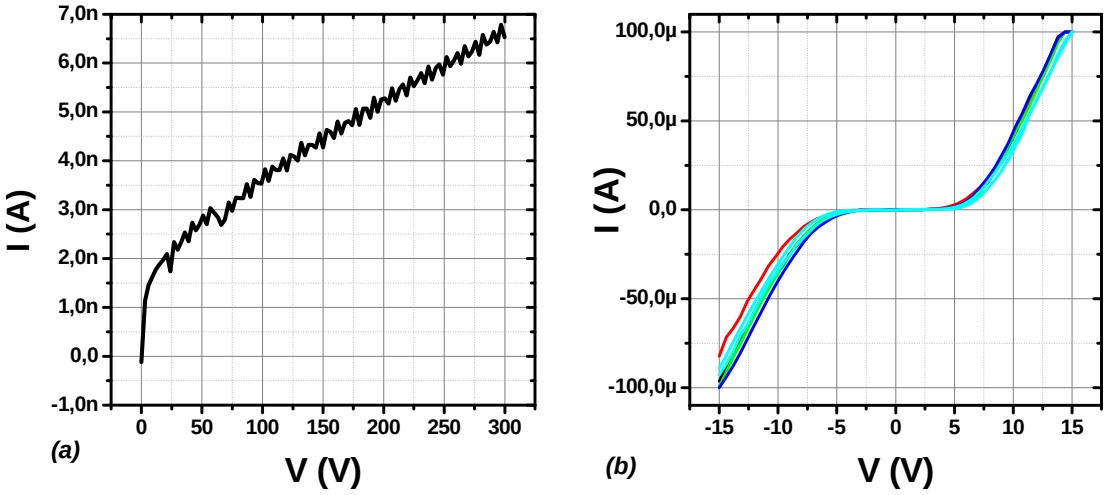
3.3 Electrical characterization

The electrical characterization of the fabricated devices is made out of three steps. First, electrical measurements were carried out in-line during the manufacturing process in order to verify the most critical fabrication steps. The second step consisted in performing electrical measurements at room temperature. And finally, high temperature measurements were carried out on the new IC MESFETs.

3.3.1 Electrical Verification In-Line during Device Manufacturing

In order to have an overview on the fabrication process evolution, several electrical measurements were necessary to be performed after key process steps. Several test pads and test devices were included from the very beginning on the mask set, having the purpose to be used for these electrical verification measurements.

First electrical measurements were carried out after the Nitrogen and Aluminum implantations were performed, in order to verify if P^+-walls are properly isolating the N-type islands. The measurements to examine the device isolation technique were performed between two different devices separated by a P^+-implanted wall. From Fig.3.5a we can see that *pn*-junction is isolating the N-islands up to at least 300V. From this measurement we can estimate that the breakdown voltage of the 4H-SiC *pn* junction is higher than 300V.



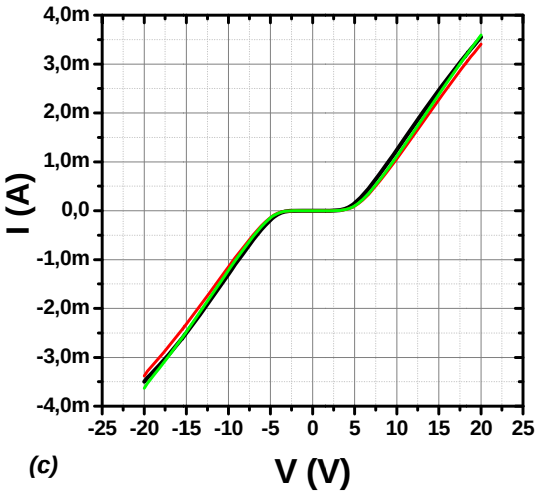


Fig.3.5. (a) *Isolation voltage of the P^+-implanted isolation walls,* ***(b)*** *I-V characteristics between two different P-type pads and* ***(c)*** *I-V characteristic of the rectifying contact between Source and Drain contact regions*

Moreover, Fig.3.5b shows that between two different P-type pads electric current passes; hence, demonstrating that the P-walls are touching at the bottom the P-epilayer. Therefore, this plot is showing that the devices isolation was successfully achieved.

After 100nm of Nickel patterned by lift-off, the Source and Drain electrodes were formed. The contact formation was verified before carrying out the rapid thermal annealing (RTA). As can be observed from the current-voltage characteristics (Fig.3.5c), the metal deposition was successfully achieved. Since the ohmic contacts are not yet annealed at this technological step, the characteristic has rectifier shape.

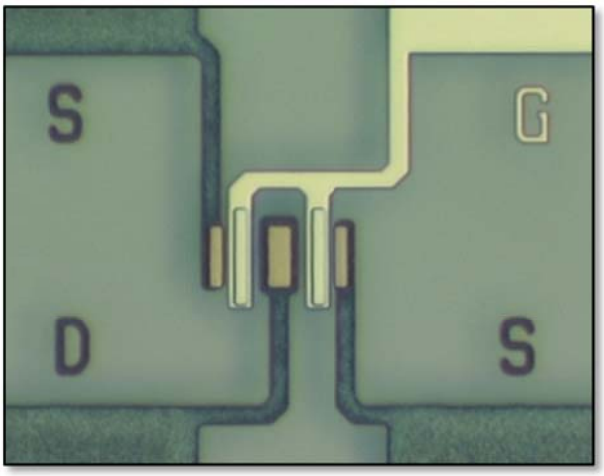


Fig.3.6. *The planar MESFET after the electrode metals were deposited*

After depositing the Gate metal, the structure has all the necessary terminals, becoming basic MESFET transistor (Table.3.2i). Fig.3.6 shows a photo of a test structure after depositing and annealing the gate metal. At this step in the process flow (Table.3.2i), it has been proven that all critical fabrication steps were successfully achieved (Fig.3.7).

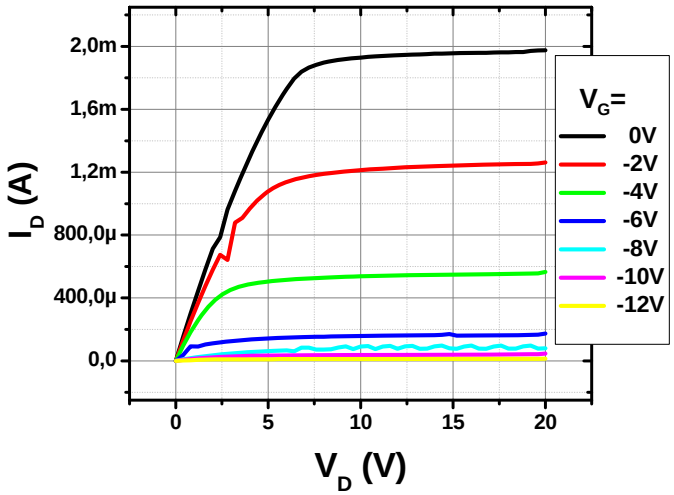


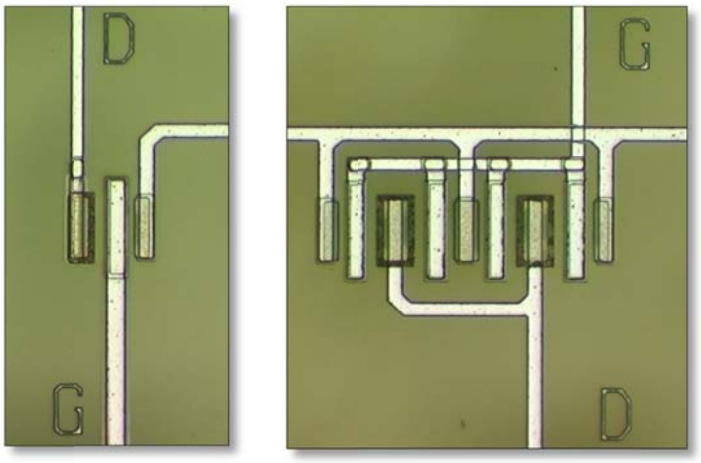
Fig.3.7. *The I_D-V_D characteristic of the basic IC MESFET*

The novel isolation technique on SiC has presented optimal results and, thus, the IC planar MESFET basic device fabrication was successfully realized (Fig.3.7). Furthermore, the last 2 metal levels and 2 via photolithography steps were performed as shown in Table.3.2. Afterwards, the detailed electrical characterization of the new fabricated MESFETs is completed.

3.3.2 The Planar-MESFET – Electrical Characterization

Fig.3.8 shows two photos of the new MESFETs after completing the fabrication process flow. In order to show the device scalability, the number of finger-gates is multiplying. The left photo shows the MESFET with a single gate (m=1), whereas on the right side is one with m=4 fingers-gate.

We remind that the new fabricated planar-MESFETs (Fig.3.8) are normally-*on* devices controlled by a negative gate potential. The electrical characterization was first carried out at room temperature and later at high temperatures up to 300ºC.



(a) ***(b)***

Fig.3.8. *The 4H-SiC MESFET* ***(a)*** *m=1 and* ***(b)*** *m=4 fabricated in N^+ tubs*

3.3.2.1 Room Temperature Measurements

The characterization at room temperature was carried out with the Probe Station Wentworth A1050 and the ICS Metrics software together with the Keithley 251 IV SMU system. The output characteristics were measured by ramping the drain voltage from 0V up to +30V while applying a gate potential from 0V to –16V with –2V per step. The I_D-V_G transfer characteristics were measured at V_D=30V with the same gate voltage ramp. The used measurement setup is the same as for the mesa-MESFET measurements.

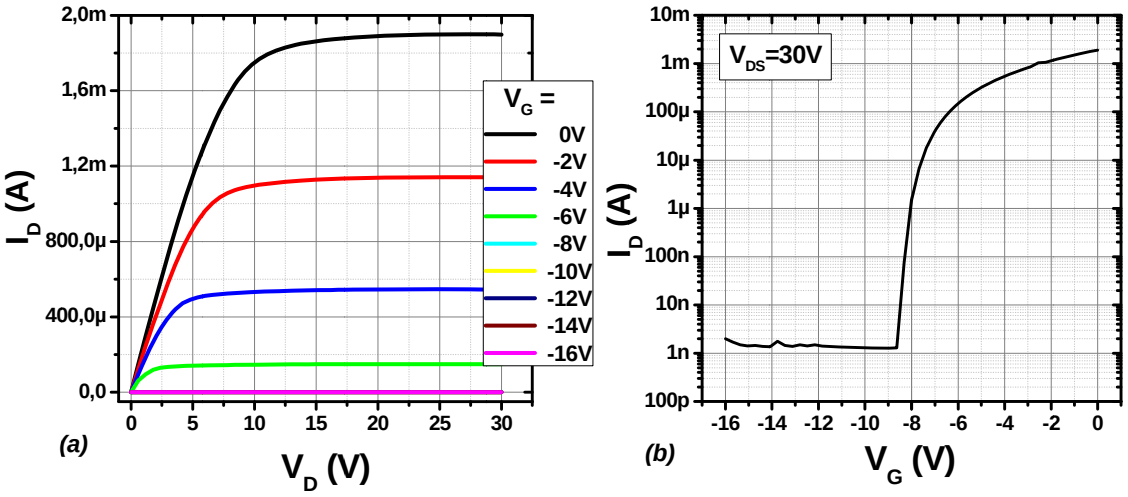


Fig.3.9. *The I-V characteristics of the 4H-SiC ICs MESFET m=1 (one finger-gate) at room temperature*

Fig.3.9 shows the I-V characteristics of the MESFET with a single finger-gate. From the output characteristics we can estimate that the saturation drain current for one finger-gate transistor is fairly close to 2mA at V_G=0V, and from the transfer plot (Fig.3.9b) the pinch-off voltage can be roughly estimated to be around -8V.

$$g_m = \frac{2 \cdot I_{DSS}}{|V_P|}\left(1 - \frac{V_G}{V_P}\right) \tag{3.1}$$

The transconductance g_m depends on the $\partial I_D / \partial V_G$ variation. Being dependent on another scalable parameter (I_{DSS}), the g_m supposes to show also its dependency with the new geometry. According to eq. (3.1) at V_G=0V and V_P=-8V, the transconductance values for the three scalable transistors are summarized in Table.3.3. In order to have a cogent comparison, we remind that for the new MESFET the ratio Z_G/L_G was considered roughly 10 times smaller than the one for the mesa-MESFET, maintaining the same gate length L_G.

In order to prove that the device scalability was achieved, Fig.3.10 shows the drain current evolution at V_G=0V and the transfer characteristics Table.3.3 summarizes the graphical estimated values for the maximum drain current at V_D=30V, the average leakage current (I_{LK}) - the on-off current ratio (I_{ON}/I_{OFF}) and the g_m transconductance calculated at V_G=0V.

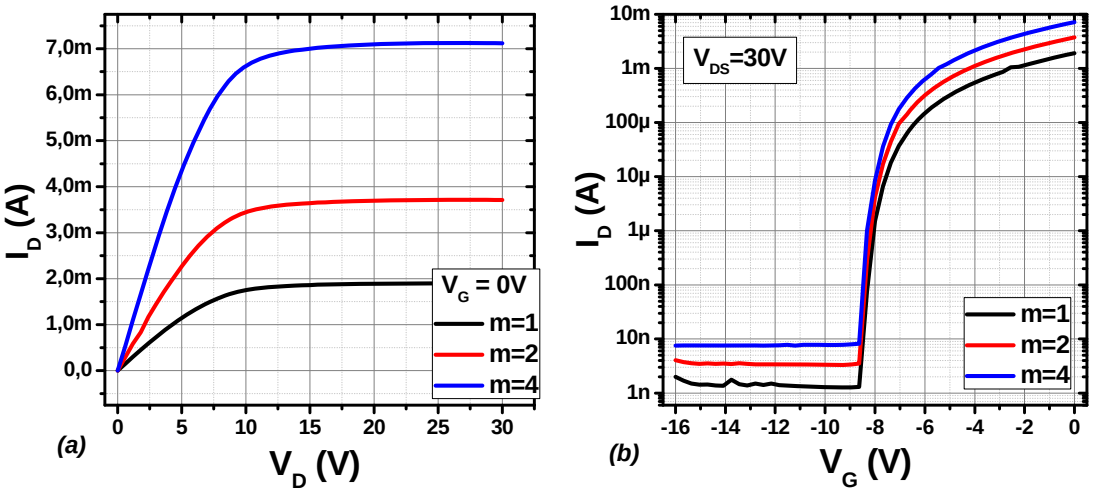


Fig.3.10. *The I-V characteristics of the 4H-SiC IC MESFETs with different number of finger-gates at room temperature*

Therefore, the experimental measurements demonstrate that the electrical scalability has been successfully achieved. From Table.3.3 it can be observed that the maximum drain current for the transistor with 2 finger-gates is approximately double than for the one with 1 finger-gate, and nearly half of the one with m=4. From the g_m values it can be seen that this

parameter is also scalable, showing the same ratios with respect to I_{DSS}. It can be also considered that the presented values are roughly 1/10 than those from the mesa-MESFETs.

Table.3.3. *Graphical estimated values on the MESFET m=1, m=2 and m=4:*

	I_{DSS} (mA) *@V_G=0V*	**g_m (mS)** *@V_G=0V, V_P=-8V*	**I_{LK} (nA)** *V_G = -16V÷V_P*	**I_{ON}/I_{OFF}** *(x10^6)*
m=1	1.96	0.49	*1.3*	*1.5*
m=2	3.64	0.91	*3.4*	*1.07*
m=4	7.18	1.795	*7.7*	*0.93*

Although the leakage current is not scalable, it is however proportional to the device area. Its value does not exceed 10nA for the transistor with 4 finger-gates. This leads to the conclusion that the additional oxide gated MESFET is accomplishing its purpose, blocking most of the residual drain-source leakage current, providing proper device functionality. As the multiplicity number of the transistor is higher, the leakage current increases, having larger oxide gated MESFETs. However, I_{LK} for the m=2 MESFET increases its value 60% than that of m=1, while the MESFET with 4 finger-gates increases its value 55% than that of m=2, showing a decreasing trend with respect to the increment of the finger-gates number.

The on-off current ratio shows really high values for the three devices. We remind that the I_{ON}/I_{OFF} current ratio is an important parameter for digital applications accounting for the standby power consumption and the corruption of dynamic node voltages in logic and memory [13]. For both static and dynamic ICs a large ratio between saturation current and off-current is required to achieve small signal propagation delay and therefore fast circuits. Moreover, [14] reports the I_{ON}/I_{OFF} ratio values required for Si high-speed transistors in 20nm CMOS logic technology (between $\sim 5 \times 10^3$ and $\sim 2 \times 10^6$). Therefore, the values showed in Table.3.3 for the three devices, make them perfectly suitable for logic ICs integration.

3.3.2.2 High Temperature Measurements

The high temperature characterization of the novel MESFETs is similar to the mesa-MESFET, using the Probe Station s200 300ºC heating chuck. The measurement setup is the same for room temperature measurements (Section 2.3.1).

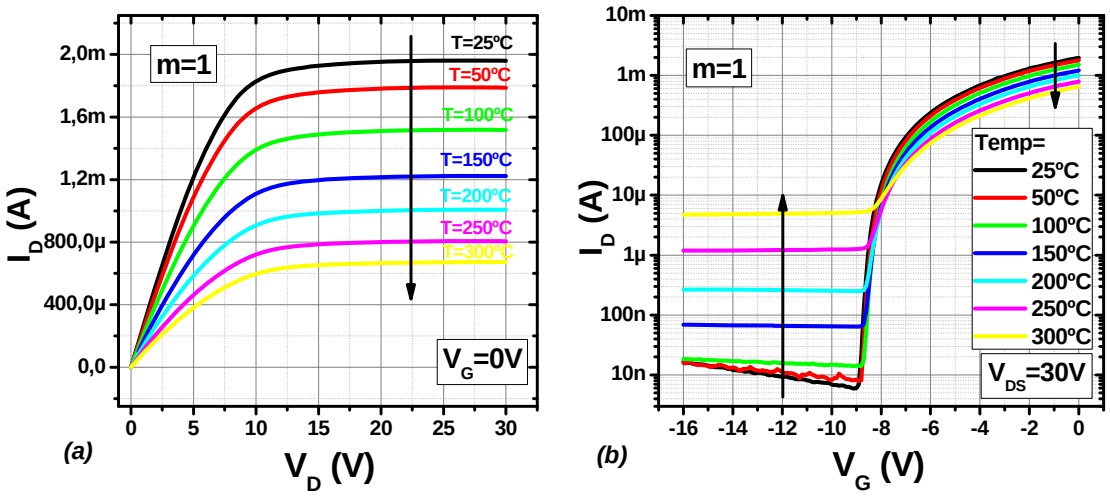


Fig.3.11. *The I-V characteristics of the 4H-SiC MESFET m=1 vs. temperature*

The high temperature measurements were performed at 7 different temperatures, from room temperature to 300ºC on the three scalable test MESFETs (m=1, m=2 and m=4). However, for simplicity reasons, Fig.3.11 and Fig.3.12 show the temperature behavior for m=1 and m=4 MESFETs, presenting the drain and leakage current temperature evolution, and also V_P evolution with temperature. The drain current evolution with temperature shows a decreasing trend for the three devices. The maximum I_{DSS} current at V_G=0V is decreasing 66% from 25ºC to 300ºC, nearly 3 times, fairly the same percent for the three devices. As expected, the V_P maintains constant in the whole temperature range for the three transistors, keeping its value close to -8V.

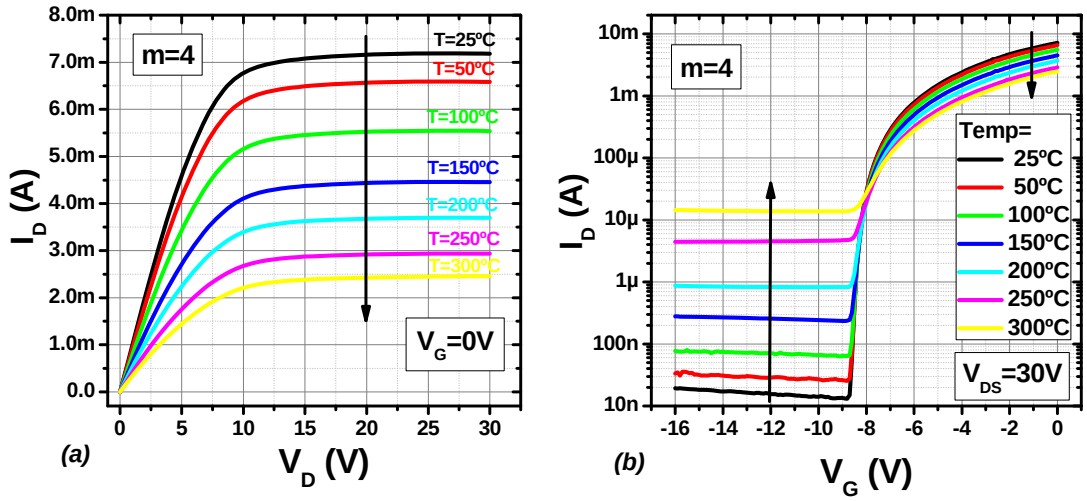


Fig.3.12. *The I-V characteristics of the 4H-SiC MESFET m=4 vs. temperature*

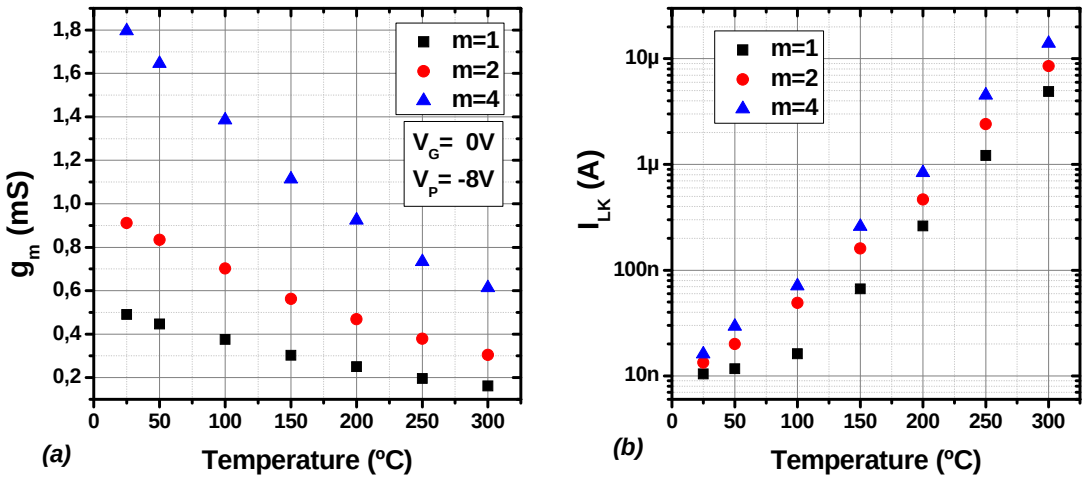


Fig.3.13. (a) *The transconductance and* ***(b)*** *the drain leakage current evolution with temperature for the three new scalable 4H-SiC MESFETs*

The g_m is proportional to the maximum saturation drain current, thus it shows a similar behavior as I_{DSS} in temperature for all devices (Fig.3.13a). Fig.3.13b shows the subthreshold drain leakage current evolution with temperature. For all devices at every measured temperature, the I_{LK} shows a linear behavior in the voltage range starting from V_P up to -16V. Its average value increases 3 orders of magnitude at 300ºC with respect to 25ºC, showing the same variation as the mesa-MESFET leakage current with temperature (see Fig.2.9).

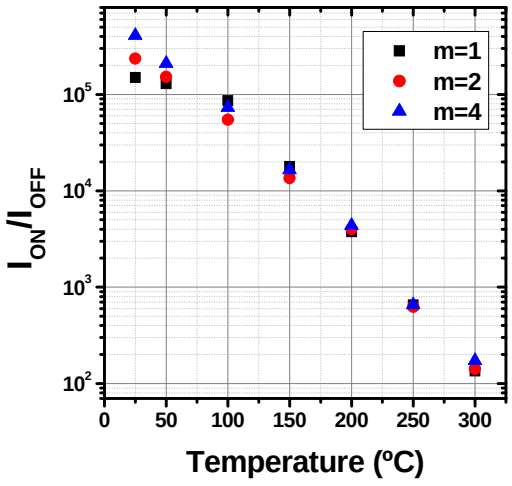


Fig.3.14. *The on-off current evolution in temperature of the 4H-SiC MESFETs*

As expected, due to the decreasing of drain current and the increasing of the leakage current, the on-off current ratio is strongly decreasing with temperature (Fig.3.14). Comparing with Si maximum working temperature (125ºC), the SiC MESFET I_{ON}/I_{OFF} ratio maintains a value above 10^4 at 150ºC, and $5 \cdot 10^3$ at 200ºC approximately, which still is in the Si CMOS logic range at 25ºC. For higher temperature operation, this ratio can be increased either by replacing the Schottky metal by another one with a higher barrier height, or by using JFETs instead of MESFETs. However, no relevant results concerning I_{ON}/I_{OFF} temperature evolution at 300ºC have been found so far in literature.

3.3.3 Simulated vs. Experimental Results

In order to verify the accuracy of the proposed SPICE model presented in Section 3.1.4, this section reports a comparison between the simulated I-V characteristics and the experimental measurements of the device. As the experimental scalability of the new fabricated devices is already demonstrated, the followings show the simulated vs. experimental characteristics only for the MESFET with multiplicity 1, in order to simplify the presentation. Therefore, Fig.3.15 and Fig.3.16 plot the output I_D-V_D and the transfer I_D-V_G experimental and simulated characteristics of the device at room and high temperature, respectively.

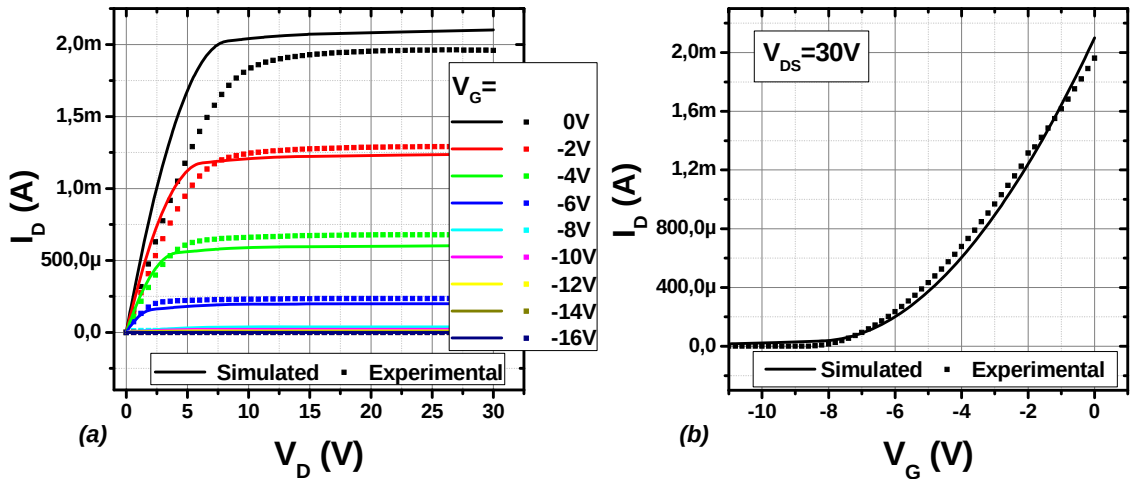


Fig.3.15. *Simulated vs. experimental I-V characteristics of the 4H-SiC MESFET m=1 at room temperature*

From the room temperature comparison one can notice that the experimental transfer characteristic of the fabricated device is in good agreement with the simulated one

(Fig.3.15b). From the output characteristics (Fig.3.15a) one can be observed that the experimental maximum drain current shows a small variation (5% lower) than the designed one. Even so, at lower gate bias, the simulated and experimental characteristics show a better matching.

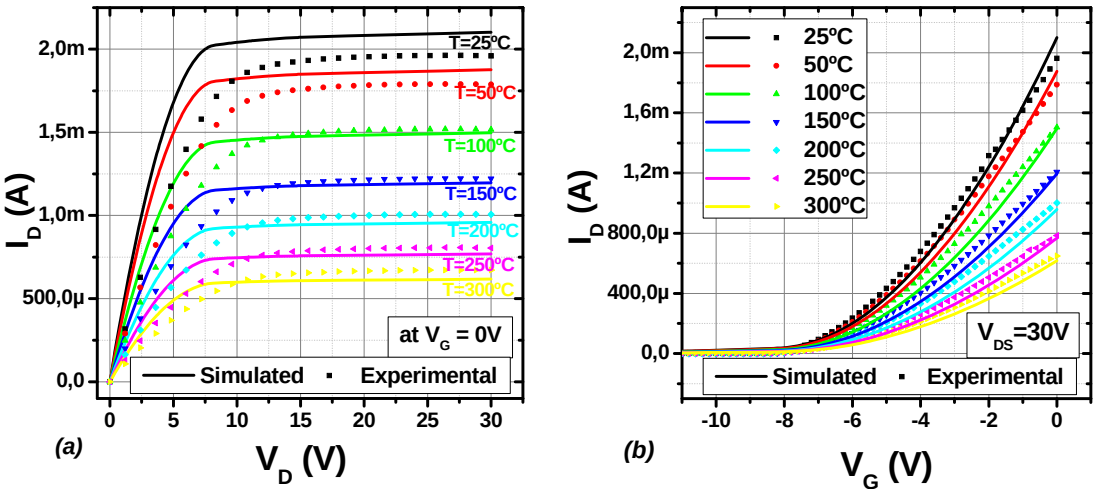


Fig.3.16. *Simulated vs. experimental I-V characteristics of the 4H-SiC MESFET m=1 in the 25ºC-300ºC temperature range*

From the above comparison (Fig.3.16), it can be observed that the best fitting between simulated and experimental characteristics is obtained at higher temperatures, while at lower temperatures (25ºC or 50ºC) there is a small dispersion between the two compared plots. In general, the on-resistance is higher in the experimental curves. This can be attributed to higher contact resistances than the one used in the model.

However, taking into account that the proposed SPICE model for new MESFETs was extracted and customized using a device with a different fabrication process and also different size and geometry (the close-loop MESFET), we can conclude that between both simulated and experimental results from the first planar MESFET generation, has been obtained a quite reasonable matching.

The presented comparison shows a good starting point for the future design of digital integrated circuits on 4H-SiC. Nevertheless, in the next section, in order to optimize the SPICE model, the key parameters will be extracted directly from the experimental measurements of the new MESFETs, followed by a new comparison between the optimized SPICE model simulations and the experimental results.

3.4 The 4H-SiC Planar-MESFET SPICE Model Definition

In order to optimize the proposed SPICE model extracted and extrapolated from the mesa-MESFET model (Section 2.4), we have performed a second parameter extraction on the new fabricated structures. It is important to mention that this new parameter extraction is in fact generating the real SPICE model of the novel MESFET. The proposed SPICE model was used only for the theoretically prediction and analysis of new structures prior its fabrication. However, it is important to remind that the new MESFET is a complete different device than the mesa-MESFET. Therefore, differences between various SPICE parameters are expected, as already observed in the previous comparison. Finally, a new comparison between the extracted MESFET SPICE model and its experimental results is exhibited.

3.4.1 Parameters Extraction

Following the same procedure used in Section 2.4.1, a new set of SPICE parameters is extracted from the experimental characteristics of the new fabricated MESFET. In order to point out the scalability aspect, the key SPICE parameters are extracted from the three transistors.

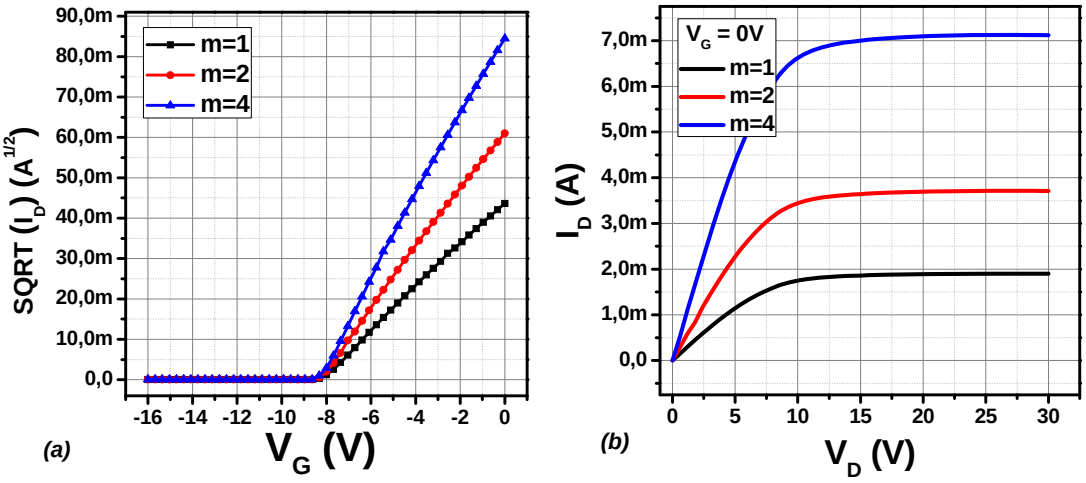


***Fig.3.17. (a)** The 4H-SiC ICs MESFET (a) transfer characteristic and **(b)** The output characteristic at V_G=0V*

From the transfer characteristics of the device at room temperature (Fig.3.17a) one can extract the transconductance modulation parameter β and the threshold voltage V_{TO}, in our case the pinch-off voltage. Furthermore, from the output characteristic at V_G=0V (Fig.3.17b) the channel-length modulation parameter λ is also extracted (see Table.3.4).

Table.3.4. *Room temperature extracted parameters for the planar-MESFET SPICE model*

	BETA (mA/V^2)	**V_{TO} (V)**	**LAMBDA (E-4/V)**
m=1	0.025	-8.26	4.64
m=2	0.051	-8.36	2.46
m=4	0.103	-8.41	1.34

One can easily notice that the extracted values of the V_P on the new devices present quite a constant value for the three structures. The V_P value in the proposed SPICE design model was established at -8V. Therefore, the extracted V_P shows to be in quite good agreement with the proposed value, evidencing the effectiveness of lowering the thickness of the N-epitaxial layer.

As the channel-length modulation parameter λ is inversely dependent with the drain current, the extracted value for MESFET m=1 presents a doubled value than for m=2, and almost 4 times higher than the m=4 structure. From the extracted values of the transconductance modulation parameter β, the scalability between the three devices can be also observed. If we compare these values with the ones from the proposed SPICE model (Table.3.1), one can see that the latterly extracted λ is almost one order of magnitude smaller and the transconductance modulation parameter is 6 times lower approximately.

The new MESFET SPICE temperature coefficients are also extracted in order to compare them with the initial extracted ones from the mesa-MESFET. The pinch-off voltage temperature coefficients (VTO_{TC}) that vary with temperature, according to eq. (2.11), are extracted from the V_{TO} plotted as a function of temperature (Fig.3.18a). The limit of maximum current level at elevated temperatures is determined by the transconductance exponential temperature coefficient $BETA_{TCE}$. These coefficients are extracted from Fig.3.18b.

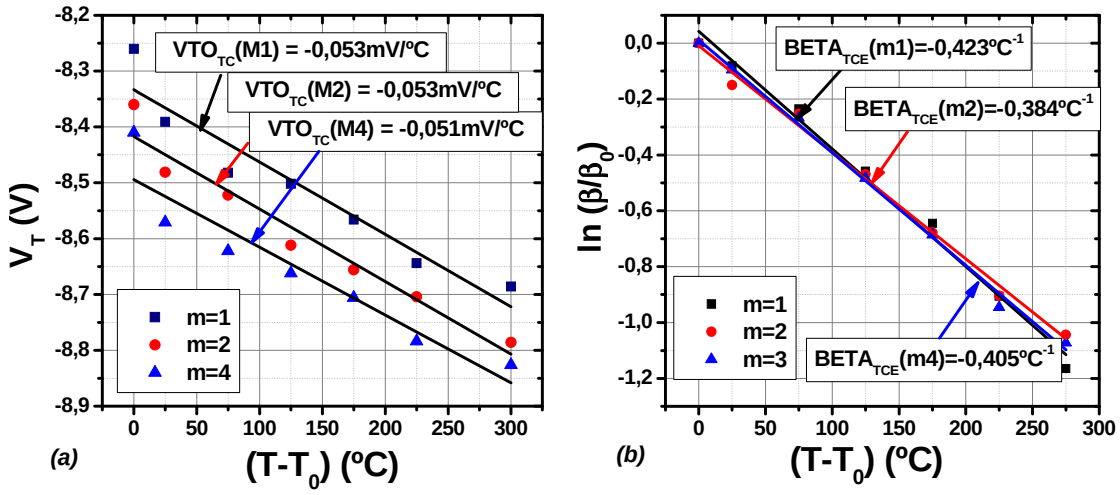


Fig.3.18. (a) *The pinch-off voltage coefficient (VTO_{TC}) and* ***(b)*** *the transconductance exponential temperature coefficient ($BETA_{TCE}$) extraction for ICs MESFET*

One can observe that the newly extracted valued for VTO_{TC} and $BETA_{TCE}$ coefficients for the three devices are in fairly good agreement with the previously extracted from the mesa device (see Section 2.4.1), showing fairly close values.

From the upper extractions one can see that the V_P of the new MESFETs presents a minor variation with temperature. In reality, the device depletion region is not temperature dependent, thus the V_P it supposed to have no variation with temperature, as it can also be seen from its theoretical expression (2.2). Going into details, the VTO_{TC} was considered in the SPICE model since the leakage current increases with temperature (Fig.3.11b, Fig3.12b), which in fact results in a slight moving of the V_P value with temperature.

Table.3.5. *High temperature extracted parameters for the planar-MESFET SPICE model*

	VTO_{TC} (mV/ºC)	**$BETA_{TCE}$ (1/ºC)**
m=1	-0.053	-0.423
m=2	-0.053	-0.384
m=4	-0.051	-0.405

The transconductance exponential temperature coefficient $BETA_{TCE}$ is expressed by eq. (2.12). The transconductance of device correspondingly drops as the temperature increases due to the higher *on*-resistance, which limits the current level.

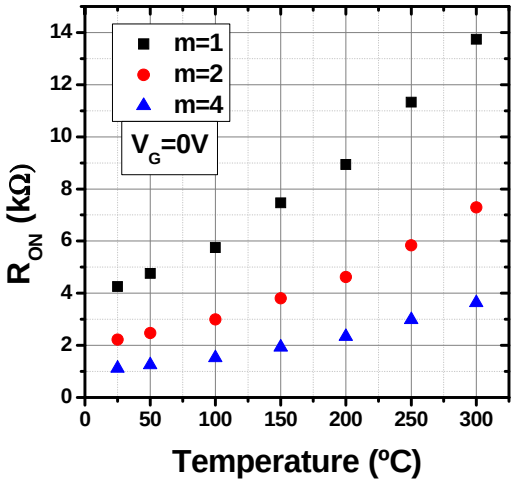


Fig.3.19.*Temperature dependence of the on-state resistance at V_G=0V for MESFET*

As expected, the *on*-state resistance R_{ON} shows a strong dependency with the temperature increment. From the above figure can be seen that for transistors with higher multiplicity order, the R_{ON} has a smaller variation in temperature, hence having a lower contribution to the device forward losses. The R_{ON} plot is represented at V_G=0V. Its variation with temperature for the new MESFET shows a parabolic dependency.

From the new parameter extraction it can be noticed that the experimental extracted values at room temperature differ from the ones previously proposed, while for the high temperature are in a quite good agreement with the ones extracted for the close-loop MESFET. The SPICE model for the new fabricated MESFETs can be found in ***Annex.A3*** *– SPICE Model Planar-MESFET – Extracted Model*. As some of the extracted parameters have shown a small variation, the following section reports a brief comparison between the extracted planar-MESFET SPICE model and its experimental results, in order to see their effect.

3.4.2 Simulated vs. Experimental Results

After updating the SPICE model with the previous extracted parameters, a new simulation vs. experimental comparison was performed at room and high temperature for the MESFET m=1, as can be seen in Fig.3.20 and Fig.3.21.

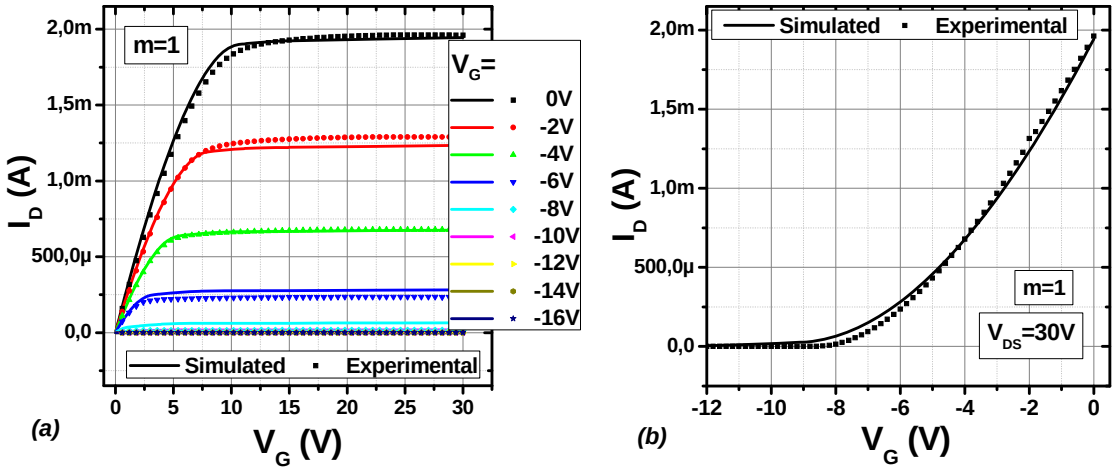


Fig.3.20. *SPICE results with the updated parameters vs. experimental I-V characteristics of the 4H-SiC MESFET m=1, at room temperature*

One can observe that the new extracted SPICE model provides a much better fitting with the experimental result (Fig.3.15 and Fig.3.16). This proves the necessity of extracting and defining a new SPICE model for the new planar devices. However, it should be mentioned that due to manufacturing processes, across the wafer exists a small dispersion between all experimental results. Therefore, the small variation that is observed, can as well owe to this reason.

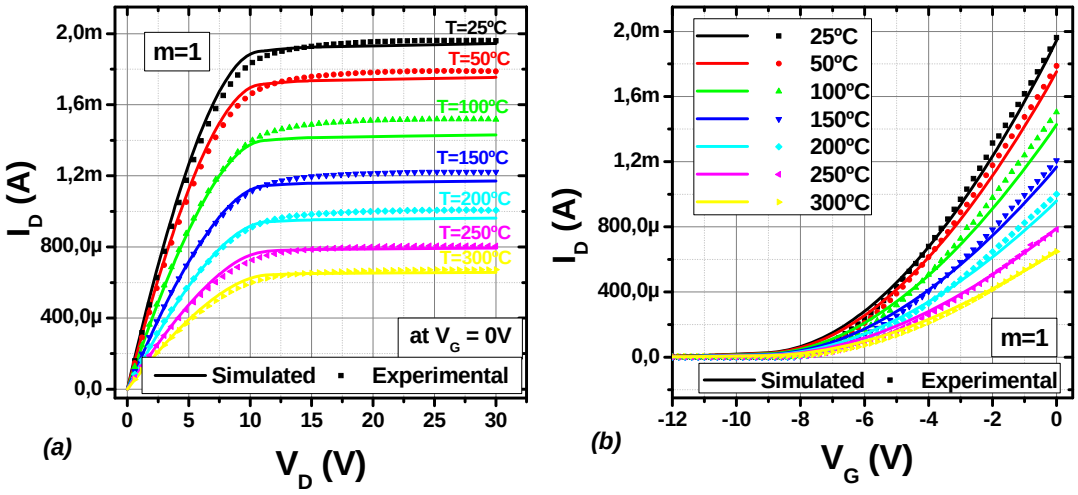


Fig.3.21. *SPICE results with the updated parameters vs. experimental I-V characteristics of the 4H-SiC MESFET m=1, for all temperatures*

We can conclude that the first proposed model and the new extracted SPICE model for the planar-MESFETs is in quite a proper agreement. The models are mostly comparable, especially concerning high temperature behavior. The observed differences can be related with the device geometry.

3.5 Nano-Scale Observation of the Fabricated Planar-MESFETs using Coupled FIB and SEM Technique

The Focus Ion Beam (FIB) coupled with SEM is a technique used particularly in the semiconductor industry, which allows the device investigation after its fabrication. Using the Scanning Electron Microscope (SEM) we can obtain images of the samples with a resolution better than 1nm. Using the FIB we performed a vertical cut of the device structure and together with the SEM, images of the cross-section device are taken with an accuracy down to 1μm.

From the SEM images we can see the difference of the doping type as a difference of contrast in the semiconductor, which allows us to observe the internal structure of the fabricated MESFET. After completing the device fabrication (Fig.3.22) we performed the FIB inspection on a multi-finger device. The device structure captured with SEM is shown in the next photo:

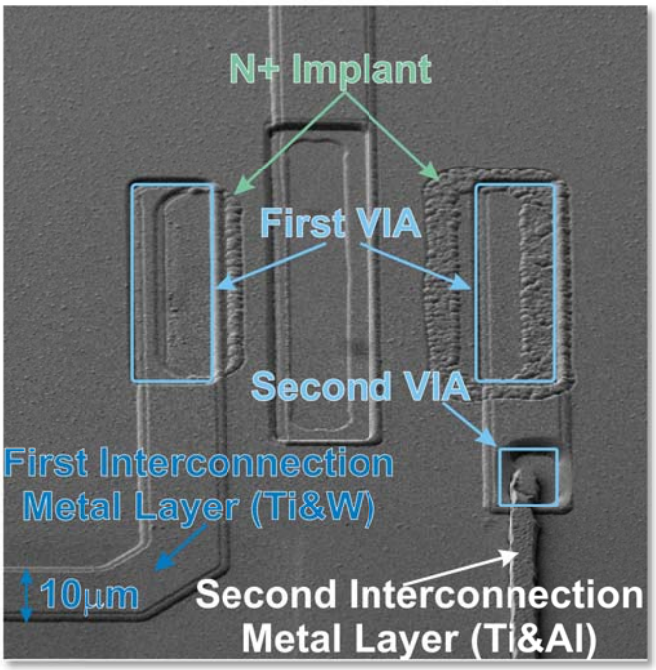


Fig.3.22. *SEM photo of the fabricated planar-MESFET before performing FIB*

From the SEM photos we can see in light grey the isolation layers and in dark gray the conductive layers. From Fig.3.23 we can distinguish that the P^+-implant was successfully realized, crossing the N epilayer and reaching the P-layer. It can be easily observed that the first metal layer interconnection is overlapping the field oxide and the Ni metal layer. However, some of the layers are too thin to be visible at this scale.

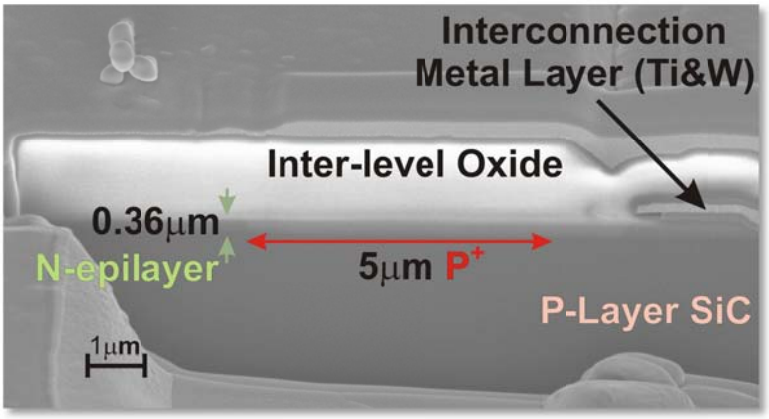


Fig.3.23. *SEM image of a FIB cut of the planar-MESFET*

After performing the FIB technique, we can confirm that the successfully fabricated device structure shows a good matching with the design dimensions.

3.6 Conclusions

The MESFET operation is commented in the present chapter, which also reported all necessary steps for the development of the planar-MESFET structure suitable for high device integration.

It has been shown that the layout for the new planar structure is similar to the ICs CMOS approach. The adopted *finger-gate* geometry was specially used to fulfill the ICs scalability requirement. Before establishing the fabrication process flow, a new set of SPICE key parameters has been defined. The proposed planar-MESFET SPICE model complexity was emphasized due to the geometry trick designed to block any residual source-drain current. The V_P of the new device was considered -8V, the thickness of the N-type epitaxial layer 0.35µm and the Z_G/L_G 10 times smaller than the mesa-MESFET in order to have a coherent comparison. In the fabrication flow section, the complexity and maturity of device manufacturing has been highlighted, showing that 10 levels of photolithography masks were necessary in order to achieve the device fabrication. It has been demonstrated as well that the current CNM SiC MESFET technology has allowed us to adopt an isolation technique widely used in Si CMOS ICs, yet not used in SiC. Moreover, our present technology has allowed the fabrication of MESFET devices with 3 metal levels, from which 2 levels were used for device interconnections.

After performing the electrical characterization on three test devices (m= 1, 2 and 4), it has been demonstrated that the device isolation is successfully accomplished with *deep P^+ implanted walls*, holding isolation voltages higher than 300V. The *device fabrication includes 3 metal levels and 2 via masks*.

Therefore, it has been proven that some of the most important ICs requirements are successfully achieved by the new designed and fabricated planar-MESFET structure: the scalability for various electrical parameters for all three test devices at room and also high temperature; a better wafer planarity is ensuring reliable interconnections between devices and circuits. Final comparisons have shown the good agreement between the proposed SPICE model and the experimental results. A new set of SPICE parameters was extracted in order to optimize the initial model.

Finally, the FIB investigation has shown the cross-section of the new developed MESFET, pointing out the device isolation, where the P^+-impurities are reaching the P-layer.

3.7 References

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CHAPTER IV

The 4H-SiC Epitaxial Resistors

An important aspect that must be mentioned is the lack of complementary devices for N-channel MESFETs necessary to implement ICs. At present, the fabrication technology of normally-*off* SiC MESFETs is not fully developed and optimized. Furthermore, the P-channel MESFET can bring important disadvantages such as reducing significantly the channel depth which adversely affects the saturation current and strongly enhances the temperature dependence of the R_{ON}.

Therefore, in order to overtake this issue, the usage of resistors is imposed. Using the novel isolation technique on SiC, we have designed and fabricated ***4H-SiC epitaxial resistors***. These devices have been specially developed to be integrated in the ICs development due to their good temperature matching with the previously developed planar-MESFETs (Chapter III). In this section, the modeling together with the electrical characterization up to 300ºC of the fabricated 4H-SiC epi-resistors are presented.

4.1 The ICs Resistors

Resistors are the most used passive components in electronics with the purpose to control the current and the voltage in a circuit. The current variety of resistors is quite large. In ICs development [1], the resistors are available for many years [2-5]. Many resistors in

the ICs fabrication utilize as a resistive material the semiconductor itself. The fabrication of the resistors is included in the mask set together with the rest of the devices of the IC process.

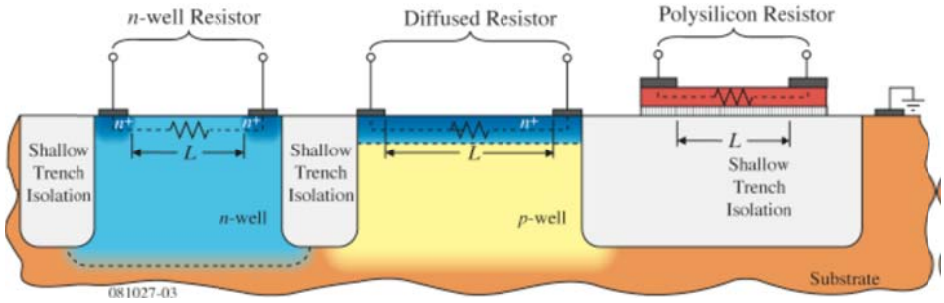

Fig.4.1. *CMOS compatible resistors [1]*

However, in order to have an overview of the currently existenting SiC technology, Table.4.1 summarizes the compatibility between the main resistors in the Si-CMOS technology, and those feasible in the SiC technology:

Table.4.1. *Compatibility between main Si-CMOS used resistors and SiC technology*

Resistors	Si-CMOS	SiC
Diffused	✓	✗
Implanted	✓	✓
Epitaxial	✓	✓
Polysilicon	✓	✓
Pinched	✓	✗
Metal	✓	✗

From the upper table can be distinguished that on SiC there are not so many compatible resistors with the current technology. Even though some other resistors can be realized on SiC, the reproducibly for these devices is low due to the growth defect density that can appear during the fabrication processes, and also because of the current SiC technology maturity. However, among the three achievable resistors on SiC, the polysilicon one is highly changing its proprieties at high temperature, while the implanted and epitaxial resistors show to be more stable in temperature.

For high temperature ICs operation the *temperature matching between various devices* is an important aspect concerning circuit's functionality. Reference [6] shows that using

4H-SiC epitaxial resistors, the temperature matching between the various components is accomplished. Thus, because the ***epitaxial resistor*** uses the bulk resistance of the same N-layer as the planar-MESFET, its value can be modeled by either modifying the effective cross-section area of the resistor structure or by using a particular doping concentration that forms the resistor body [7]. The values of the resistors are chosen as a function of the transistor's DC parameters. Furthermore, the modeling and electrical characterization of the fabricated 4H-SiC epitaxial resistors on the same N-type epitaxial layer are presented.

4.2 4H-SiC Resistor Modeling

To design the ICs epitaxial resistances it is necessary to know the sheet resistance of the semiconductor and its ohmic contact resistance. Even more, in order to use these epitaxial resistors in designing ICs it is also required to owe the scalability aspect. Thus, the theoretical calculation of the sheet resistance together with the resistors layout, and the ohmic contact formation are presented next.

4.2.1 The 4H-SiC Sheet Resistance

From the well-known resistor expression we see its dependency with the $\boldsymbol{\rho}$ resistivity of the semiconductor, the length ($\boldsymbol{L}$) and the cross-section area ($\boldsymbol{A}$) of the resistor:

$$R = \rho \frac{L}{A} \tag{4.1}$$

The ICs designers need to know the *sheet resistances* of the layers in order to model the desired resistors. The sheet resistance is controlled by the process designer depending on the substrate properties. The sheet resistance ($\boldsymbol{R_S}$) results from (4.1):

$$R = \rho \frac{L}{A} = \rho \frac{L}{a \cdot W} = R_S \frac{L}{W} \implies R_S = \frac{\rho}{a} \tag{4.2}$$

where $\boldsymbol{a}$ is the epitaxial layer thickness without the N-layer depletion region (Fig.4.3) (see Chapter II – Section 2.5).

From eq. (4.2) we can see that the R_S is a property of the particular layer resistivity and its thickness. It is well known that a material resistivity is the inverse of the conductivity:

$$\rho = \frac{1}{\sigma} = \frac{1}{q(\mu_n N_D + \mu_p N_A)} \tag{4.3}$$

where for the 4H-SiC N-type epi-layer the resistivity can be expressed as:

$$\rho = \frac{1}{\sigma} = \frac{1}{q\mu_n N_D} \tag{4.4}$$

Therefore, the sheet resistance is:

$$R_S = \frac{1}{q\mu_n N_D a} \tag{4.5}$$

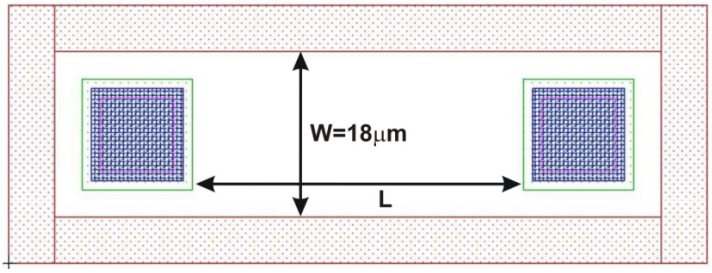

Fig.4.2. *The 4H-SiC Epitaxial resistance layout design*

The proposed 4H-SiC resistor layout is shown on Fig.4.2. As it can be seen from the layout design and its cross-section (Fig.4.3), the 4H-SiC epitaxial resistors are implemented on the same N-type epitaxial layer as the N-channel MESFET transistors, isolated by the same P^+-implanted walls. Thus, for an N-type layer uniformly doped with $N_D = 10^{17}\text{cm}^{-3}$ and $a = 0.3114\mu\text{m}$ thick, the theoretical sheet resistance value at room temperature is $R_S = 3.4\ \text{k}\Omega/\text{square}$.

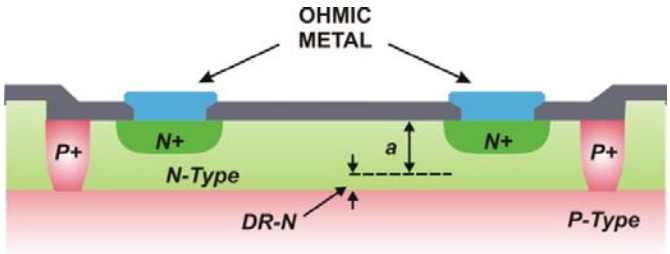

Fig.4.3. *The 4H-SiC Epitaxial resistance cross-section*

*(*DR-N – The N-Layer Depletion Region – see Fig.2.14)*

In order to achieve the ***scalability*** aspect for the proposed epitaxial resistors, we rewrite the resistance eq. (4.2) by separating the L/W ratio, which is the so called *number of square units* (N_{Sq}):

$$R = R_S \cdot N_{Sq} \qquad \text{where} \qquad N_{Sq} = \frac{L}{W} \tag{4.6}$$

The number of square units is established depending on the desired resistance value. From technological limitations we have chosen the minimum width for the resistor $W = 18\ \mu\text{m}$. To obtain resistors with different values, the parameter that will be varied is

the length L. In addition, in order to achieve a good scalability for these resistors, their contact resistance needs to have a negligible value compared to the sheet resistance value.

4.2.2 The Ohmic Contact Resistance - TLM

The ohmic contacts for planar devices are of great importance concerning the quality and reliability of monolithic circuits. This contact is a non-rectifying junction, has a linear and symmetric current-voltage characteristic and has to support a required current density with the minimum voltage drop compared with the one across the active area of the resistor.

The minimization of the metal /SiC contact resistance and the corresponding specific contact resistance is an issue in order not to compromise the device performance.

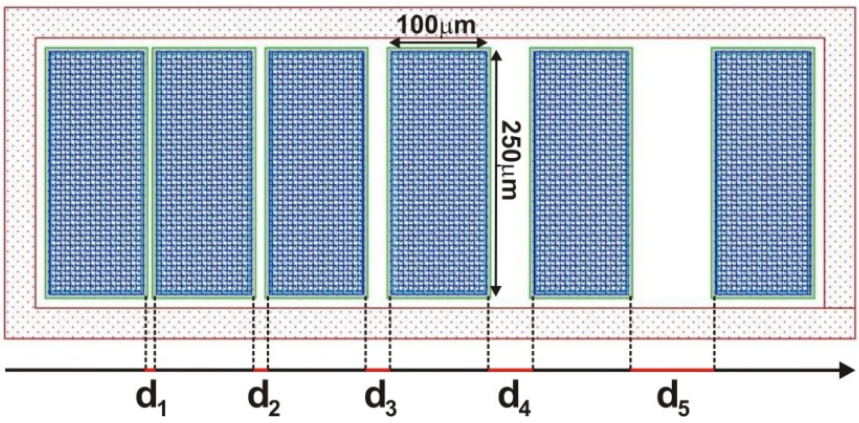

Fig.4.4. *Schematic layout of the 4H-SiC N-type TLM structure*

The ability to accurately measure the contact resistance is essential for the contact process development. For this purpose, a set of test structures have been fabricated (Fig.4.4) and their specific contact resistances derived using the Scott model of TLM [8] and a correction for the current distribution. The well-known – transmission line model (TLM) measurements is an accurate technique to measure the ohmic contact resistance and also the sheet resistance of a single epitaxial layer [9-11].

Furthermore, the ohmic contact regions first needed to be N^+ doped, as shown in Table.3.2b. After, the contact is formed by covering the 4H-SiC epitaxial layer with 100nm Nickel, patterned with lift-off, and thereafter annealed at 950ºC for 2 min to form Ni-silicide onto the SiC surface.

Table.4.2. *Distances between each TLM contact:*

	d_1	d_2	d_3	d_4	d_5
Distance	5 µm	10 µm	20 µm	40 µm	80 µm

Fig.4.4 shows the schematic of the TLM structure and Table.4.2 contains the detailed distances. The resistance of the ohmic contact is characterized by two important parameters: the *specific contact resistance* (ρ_C) and the *contact resistance* (R_C) [12-16]. Electrical measurements up to 300ºC have been performed on these structures and the experimental results are later presented in Section 4.4. Using the TLM electrical measurements the values of the epitaxial layer sheet resistance and the contact resistance are determined.

4.3 SPICE Model Definition - Temperature Coefficients

In the preset work, the developed epitaxial resistors are used instead of the habitual current sources, push pull stages or dropping diodes, in the future configurations of the SiC ICs logic gates. Thereby, a SPICE model definition is also required for these passive devices. As previously mentioned, in order to assure a proper operation of the ICs in temperature, we have overtaken a crucial issue in designing the optimal MESFET-resistor pair by considering the same N-type epitaxial layer for implementing them. The theoretical resistance dependence with temperature is plotted in Fig.4.5.

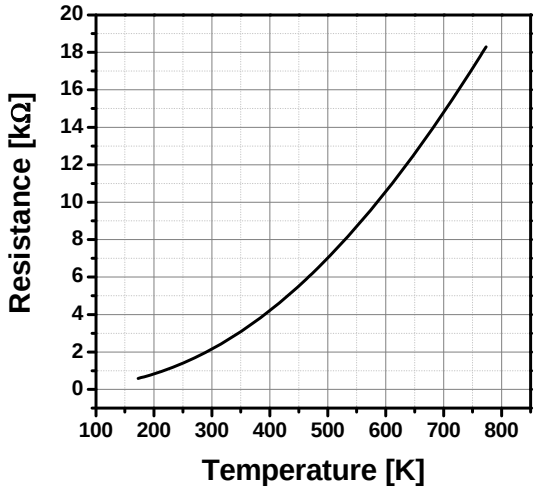

Fig.4.5. *The theoretical temperature dependence of the 4H-SiC epitaxial resistor*

Therefore, in order to obtain accurate simulation results of the ICs on 4H-SiC, a SPICE model has been defined for the epitaxial resistors. The effect of temperature on resistors is modeled by:

$$R(T) = R(T_0)[1 + TC_1(T - T_0) + TC_2(T - T_0)^2] \quad (4.7)$$

where T is the circuit temperature, T_0 is the nominal temperature, being considered 25ºC for SPICE modeling, and TC_1 and TC_2 are the first and the second order temperature coefficients, parameters required for the SPICE model.

The extracted values of the temperature coefficients after performing a polynomial fitting of Fig.4.5 are $TC_1 = 7.4798 \cdot 10^{-3}$K and $TC_2 = 1.8011 \cdot 10^{-5}$K. These values are considered in the resistance model, thus defining the epitaxial resistance SPICE model for high temperature operation.

4.4 Electrical Measurements

Electrical measurements on the fabricated samples were performed on differently valued resistors at room and high temperature. In order to demonstrate the scalability, four resistors with different N_{Sq} = 2, 4, 8, and 16 squares have been measured.

4.4.1 Room Temperature Measurements

The room temperature characterization has been performed with a Keithley 251 IV SMU, together with the Wentworth Probe Station A1050 and the ICS Metrics software.

a) Epitaxial Resistors Measurements

In order to demonstrate the resistors scalability, Fig.4.6a shows the linear characteristics of the 4 resistors and Fig.4.6b shows their experimental values extracted from a linear fitting of the I-V curves.

From Table.4.3 it can be easily observed the experimental scalability of the fabricating epitaxial resistors. The electrical measurements have been performed across the wafer. Giving that $R_S = 3.4\,k\Omega/square$, the theoretical values of the resistors can be easily calculated. Table.4.3 shows the theoretical calculated values together with the experimental extracted values for different lengths of the 4H-SiC epitaxial resistors (square numbers).

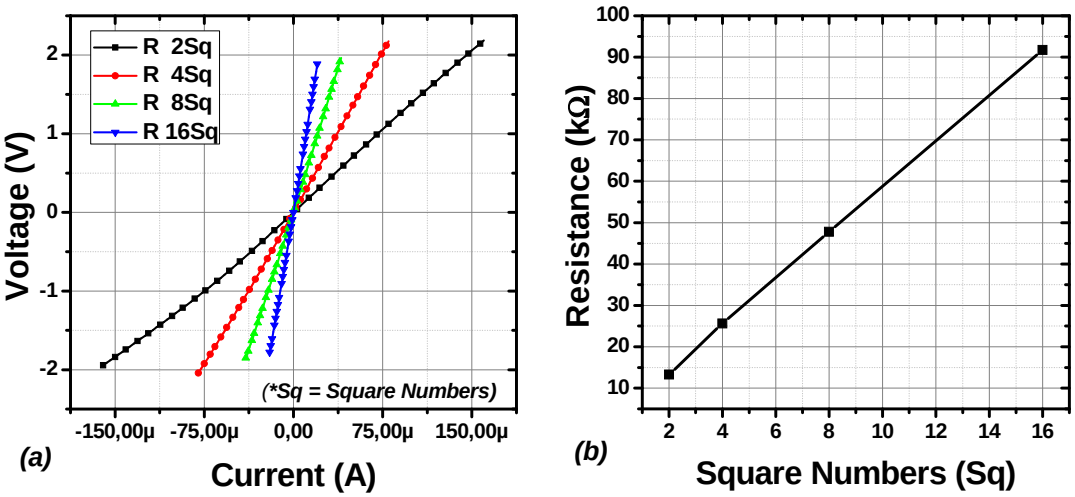

***Fig.4.6. (a)** Voltage vs. current characteristic and **(b)** Resistance vs. Square Numbers for the 4 different epitaxial resistors*

One can notice that there are differences between theoretical and extracted values. However, the ratio between the experimental and theoretical values is approximately the same for the 4 different resistors. It can also be observed that the experimental sheet resistance R_S varies between 6.6kΩ and 5.7kΩ per square, decreasing for larger length resistances. The almost double value of the experimental sheet resistance explains the difference between the designed and fabricated epitaxial resistors.

***Table.4.3.** Theoretical and experimental values of the 4H-SiC epitaxial resistors.*

	Theoretical Value [kΩ]	**Experimental Value [kΩ]**	**Experimental R_S [kΩ/Sq]**
$N_{Sq} = 2$	6.81	13.2	6.6
$N_{Sq} = 4$	13.62	25.6	6.4
$N_{Sq} = 8$	27.25	47.7	5.96
$N_{Sq} = 16$	54.50	91.7	5.73

Several causes may determine this variation, such as the non-uniformity doping concentration of the epitaxial layer, or the incomplete ionization of the N dopants at room temperature, or even the non-uniformity of the SiC etch rate. It was shown that the ionization degree decreases with increasing the doping concentration and decreasing the temperature, which finally leads to the freeze-out of N dopants at low temperatures [17].

Therefore, it can be expected that the N dopants are not completely ionized at lower temperatures, hence leading to a higher epilayer resistivity.

However, an important advantage in designing the ICs is that the resistance ratio is more important than the absolute resistance values. Therefore, the ratio between the experimental and theoretical values, which is approximately the same for all the four length resistors, will ensure a proper functionality of the voltage dividers and level shifters.

b) Contact Resistance Measurements – TLM measurements

The ohmic contact resistance has been measured by performing dedicated 4 points electrical characterization on the TLM structures (Fig.4.4). The R_C, the ρ_C together with the R_S outside the ohmic contact have been extracted from the experimental TLM measurements [12-16].

Table.4.4. *Extracted experimental values from TLM measurements at room temperature*

	R_C (Ω)	ρ_C ($\Omega \cdot cm^2$)	R_S ($k\Omega$)	R_C ($\Omega \cdot mm$)
Value	73.378	6.85E-4	5.182	18.844

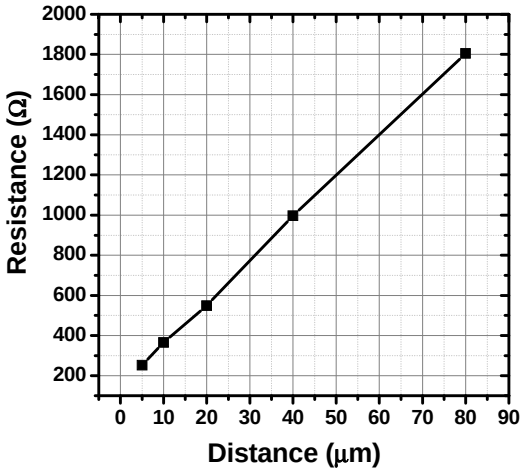

Fig.4.7. *Electrical characterization of the 4H-SiC TLM structure*

From the extracted values from the TLM structures it can be noticed that the sheet resistance R_S shows a different value than the theoretical one. However, one can observe that the ohmic contact resistance has a very small value compared with the sheet resistance

value of the SiC epi-layer. Therefore, its impact on the epitaxial resistance value, the ohmic contact resistance, can be neglected. The good scalability of these devices has also been achieved due to the small value of the ohmic contact resistance (Fig.4.7).

4.4.2 High Temperature Measurements

a) Epitaxial Resistors Measurements

Fig.4.8 shows the epitaxial resistor plots measured up to 300ºC. Fig.4.8a shows that the resistors dependency with temperature follows a similar parabolic trend as in Fig.4.5. From Fig.4.8b it can be noticed that the scalability criterion of the epitaxial resistors is well accomplished even at elevated temperatures. Therefore, the experimental epitaxial resistors evolution with temperature is consistent with theory.

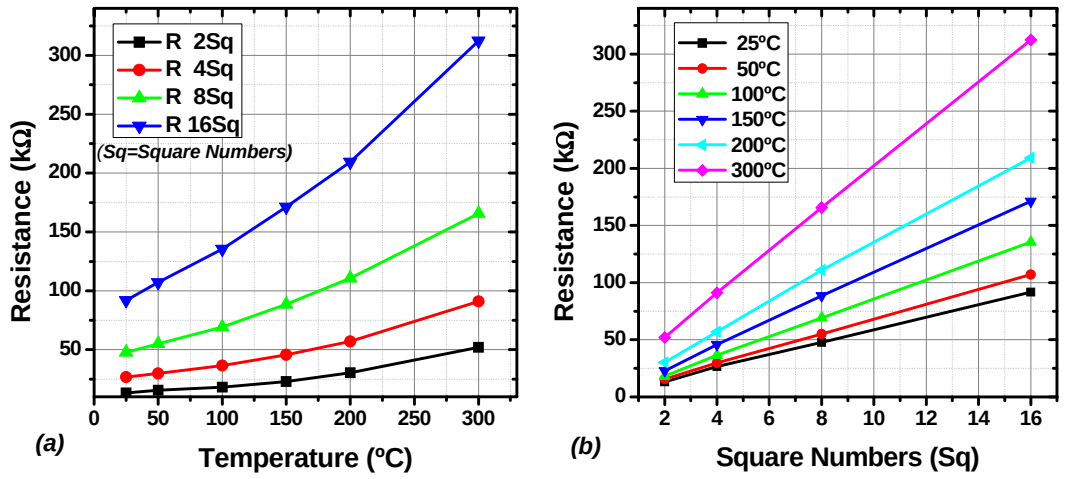

Fig.4.8. (a) *Resistance vs. Square Numbers for the 4 different epitaxial resistors and* ***(b)*** *the temperature dependence of the epitaxial resistors*

b) Contact Resistance Measurements – TLM measurements

From Fig.4.9 we can see that the TLM structure has a similar temperature dependency than the epitaxial resistors of Fig.4.8b. The temperature behavior is showing a linearly dependence up to 300ºC, thus demonstrating the quality of the Ni ohmic contacts.

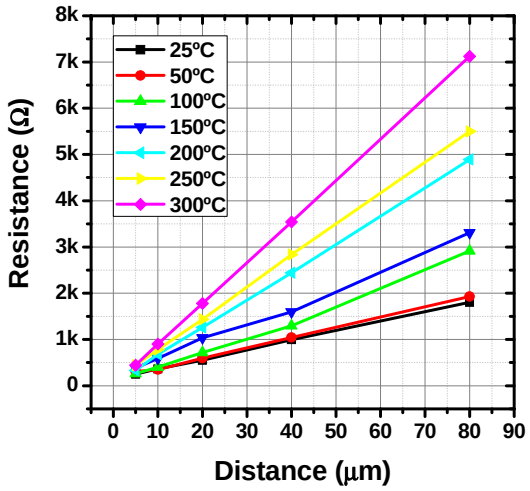

Fig.4.9. *Temperature dependence of the TLM structures*

4.5 Simulated vs. Experimental Results

In Section 4.3 we defined the theoretical SPICE temperature coefficients for the epitaxial resistance. As observed from the experimental results, the extracted values are quite different than the theoretical ones. Although the ratio between the experimental and theoretical values is fairly the same for the 4 different epitaxial resistors, this aspect will be taken into consideration in the circuits section.

Table.4.5. *The extracted epitaxial resistors temperature coefficients*

	$N_{Sq} = 2$	$N_{Sq} = 4$	$N_{Sq} = 8$	$N_{Sq} = 16$
TC_1	$1.3402 \cdot 10^{-3}$K	$2.7802 \cdot 10^{-3}$K	$4.9230 \cdot 10^{-3}$K	$4.9956 \cdot 10^{-3}$K
TC_2	$3.0989 \cdot 10^{-5}$K	$2.0889 \cdot 10^{-5}$K	$1.4481 \cdot 10^{-5}$K	$1.2871 \cdot 10^{-5}$K

From eq. (4.7), and by performing a polynomial fitting on the temperature vs. resistance curves for each resistor (Fig.4.8a), a new set of SPICE temperature coefficients are extracted (Table.4.5). The variation between all the extracted coefficients TC_1 and TC_2 for the different resistances is quite small. The order of magnitude is the same for all of them. However, this variation can be explained considering the R_C resistance as negligible for large distances, or high square numbers.

A last extraction of the temperature coefficients was performed on the sheet resistance dependency with temperature. The R_S was extracted from the TLM measurements in temperature (Fig.4.9). Applying the same polynomial fitting on the measurements of Fig.4.10, the extracted temperature coefficients were $TC_1 = 2.118 \cdot 10^{-3}\text{K}$ and $TC_2 = 5.367 \cdot 10^{-5}\text{K}$.

If a comparison is made between the theoretical and the experimental extraction, from both the epitaxial resistors and the TLM measurements, it can be concluded that the experimental temperature coefficients have a very low deviation, being of the same order of magnitude, thereby presenting a good agreement with the theoretical results.

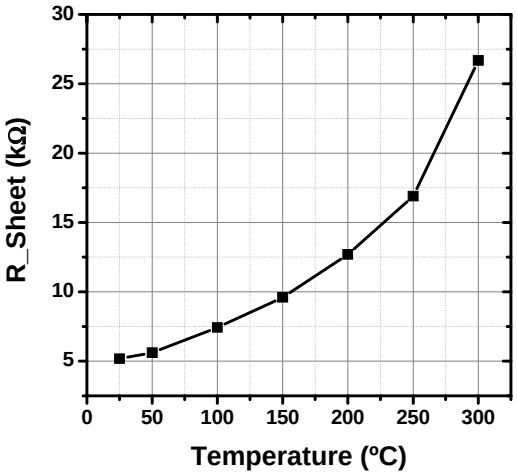

Fig.4.10. *Temperature dependence of the 4H-SiC sheet resistance*

With the extracted SPICE model for the epitaxial resistor, together with the extracted planar-MESFET SPICE model, the next generation of ICs on 4H-SiC will be modeled and simulated more accurately.

4.6 Conclusions

In this chapter we have presented the design and development of scalable *epitaxial resistors on 4H-SiC*. These resistors are, among the few resistors available to be fabricated on SiC, those that offer the best temperature matching with the 4H-SiC MESFETs. Therefore, the implementation of epitaxial resistors in the ICs development accomplishes one of the most important ICs functionality at high temperature requirements: *temperature matching between the various IC devices*.

We have also demonstrated the effectiveness of the P^+-implanted isolation technique through the resistors fabrication. The scalability of these devices has been proven at room and high temperature operations.

From the electrical measurements it has been shown that the sheet resistance presents quite a double value than the theoretical one, being verified through the double extractions that were preformed: from the epitaxial resistors measurements; and from the TLM structures measurements. However, in ICs functionality the resistance ratio is more important than the absolute resistances value, therefore no important implications are expected due to this.

From the TLM measurements it has been proven that the Ni-silicide contact offers a very good ohmic contact, having a very small value compared with SiC epilayer R_S. Therefore, the ohmic contact resistance can be neglected in the final resistance value.

Finally, the SPICE temperature coefficients were proven to be in good agreement with the theoretical ones.

4.7 References

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CHAPTER V

The 4H-SiC Digital Integrated Circuits

In this chapter we report the ***development and experimental analysis of 4H-SiC MESFET basic logic gates*** and ***multi-stage Integrated Circuits digital building blocks***.

After a general classification of the typical digital ICs logic families, the main functionality of the nucleus of digital circuitry – *the Inverter*, is described, followed by a brief description of the most common and used *MESFET logic families*, together with the *6H-SiC JFET topology*. Furthermore, the modeling at room and high temperature of *the 4H-SiC elementary logic gates library – INV, NAND and NOR* – implemented using 4H-SiC planar-MESFET devices and epitaxial resistors is submitted. The 4H-SiC MESFET Inverter was closely analyzed and evaluated in order to show the 4H-SiC MESFET logic family general performances. Using the 4H-SiC MESFET logic gates library, *multi-stage digital ICs blocks* were designed. Some of the most common Si-CMOS standard topologies have been transferred on our 4H-SiC MESFET technology, hence implementing important digital building block (such as *Flip Flops*) using a large number of devices and thus obtaining a higher device density integration.

Finally, experimental results and analyses of the fabricated digital IC are reported. The functionality at high temperature (from 25ºC up to 300ºC) and high frequency (up to 300 kHz) of the 4H-SiC MESFET logic gates library, together with complex multi-stage digital ICs are submitted. In this chapter we are demonstrating the fabrication of complex ICs on 4H-SiC using a large number of MESFETs and epitaxial resistors.

5.1 Digital ICs Logic Families

A *logic family* is a group of logic gates made with the same technology, having a similar circuit structure and exhibiting the same basic features. The logic gates, constructed using one of the several different designs, having compatible logic levels and power supply characteristics, are defining the logic family for a digital monolithic circuit. Depending on the network interconnection between the circuit components, the electronic circuits have a particular *topology*. Therefore, a way of classifying digital ICs is according to the design of the electronic logic gates. However, a more general classification is presented in the following subsection.

5.1.1 General Classification

Combining the semiconductor technology with the digital logic families, a more wide classification can be done. The chart below shows the major IC technologies and logic-circuit families that are currently in use [1]:

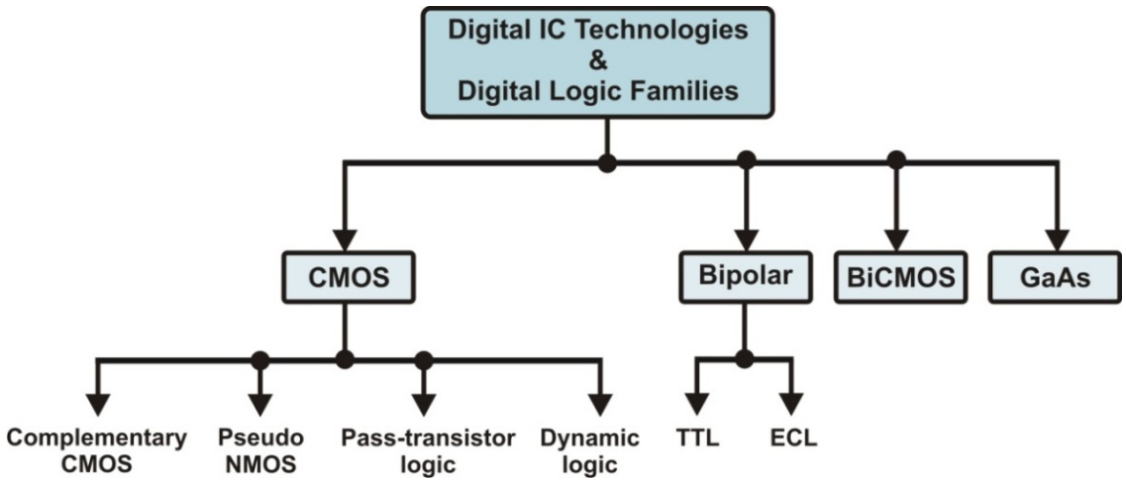


Fig.5.1. *Digital IC technology and Digital logic families – general classification*

The selection of the logic family is based on the final circuit requirements. Each logic family offers a unique set of parameters and characteristics. Four different digital ICs technologies are presented in the previous diagram.

The *transistor-transistor logic (TTL)* standard chips were introduced in 1965 [2] and for many years it was the most widely used logic family in designing digital circuitry. Once the VLSI (Very Large Scale Integration) era came in the 1970s, the TTL lost its power and latterly is no longer a significant used logic family.

The *Complementary Metal-Oxide-Semiconductor (CMOS)* is the most dominant of all the ICs technology available for designing digital ICs on Silicon nowadays. CMOS logic was first described by Wanlass and Sah in 1963 [3]. The CMOS circuitry requires both NMOS and PMOS transistors built on the same substrate.

The evolved semiconductor technology has made possible to integrate two formerly separate semiconductor technologies in a single process. The *BiCMOS* is combining the CMOS and the bipolar devices on the same substrate, which enables to combine the advantages of both technologies. Like CMOS, the BiCMOS allows implementing both analog and digital circuits on the same chip. This technology is successfully used in applications where high-density integration, low-power, high-input impedance and/or wide noise margins of MOS logic need to be combined with the current-driving capabilities of bipolar transistors.

The last three decades of microelectronics have been covered in a major percentage by the Silicon devices and ICs. Another semiconductor that has reached a mature technology is *Gallium Arsenide (GaAs).* The active devices available on this semiconductor are the MESFET transistor and the Schottky barrier diode (SBD) because of their simplicity. This technology is successfully used in digital and analog applications that require extremely high operation speed [4], due to its electron mobility which is 5-10 times higher than Si. However, taking into account that the present work active device is the MESFET, a special attention will be paid for the already existent MESFET logic gates.

Depending of the MESFETs operational state, two main approaches can be used for designing logic gates on GaAs. The *normally-on logic gates* consist of depletion-MESFETs. This was the first developed generation for GaAs digital circuits. The *normally-off logic gates* were introduced later and consist of both enhancement and depletion MESFETs [5].

In order to understand the logic gates operation, the most common element of the logic gates – the Inverter – is next introduced.

5.1.2 Digital Basic Element – The Inverter

The most basic element in logic circuitry is the *Inverter,* being the core of all digital designs. The analysis of Inverters can be extended to explain the behavior of more complex gates such as NAND, NOR, or XOR, which in turn form the building blocks for modules such as multipliers and processors. The electrical behaviors of all the other complex circuits can be derived by extrapolating the results obtained for the Inverter.

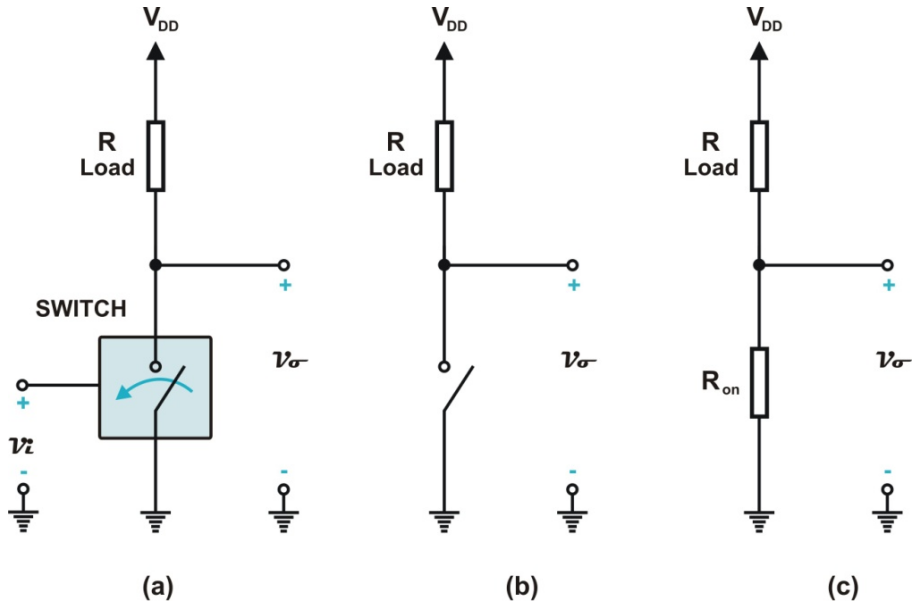
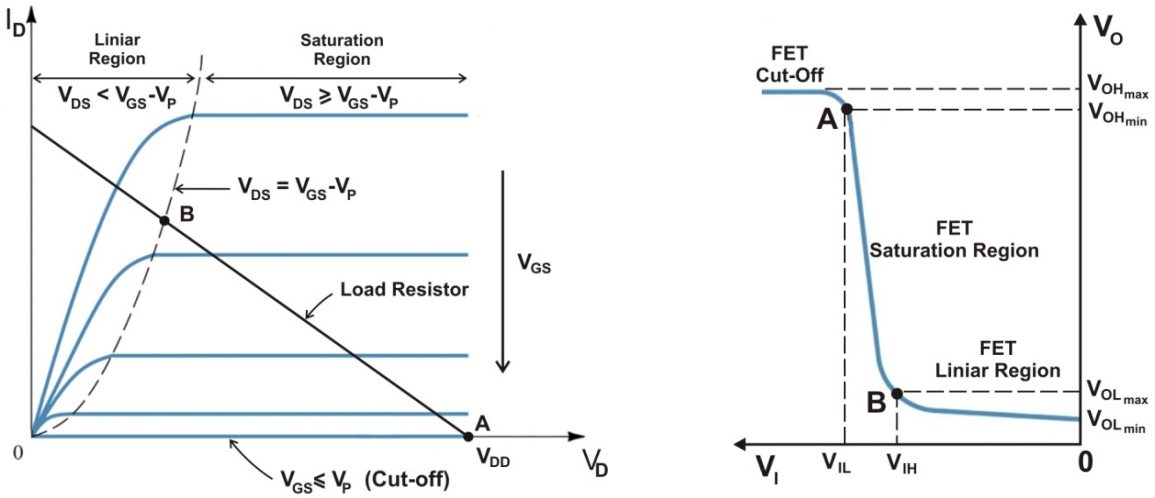


Fig.5.2. *The simplest configuration for a logic Inverter using a voltage-controlled switch*

The above figure shows the simplest implementation for an Inverter. The Inverter function is given by an ideal switch operation controlled by the input voltage $\boldsymbol{v_i}$ [6]. The Inverters are implemented with transistors operating as voltage-controlled switches. As previously presented (Fig.5.1), depending on the logic family there are many types of circuit configurations. For the sake of understanding, the switch from Fig.5.2 is replaced by a depletion MESFET, as it is the active device in the preset work.

Fig.5.3a shows the current-voltage characteristics of the Inverter circuit composed by the MESFET output I_D-V_D characteristics together with the load resistors R_L characteristic. This plot is used in order to obtain the voltage transfer characteristic (VTC) of the Inverter, which helps us to quantify easily its operation.



(a) *(b)*

Fig.5.3. (a) *The current-voltage characteristics and* ***(b)*** *the voltage transfer characteristic (VTC) of the basic MESFET Inverter*

Since the V_P of the depletion MESFET is negative, we need a negative voltage to turn the device off. Thus, for an input voltage $v_i < V_P$, the transistor is cut-off, similar state with the open switch (Fig.5.2b). Therefore, the V_{DD} potential is pulled up to the output through the R_L resistor.

Once the input voltage v_i increases over the V_P, the MESFET starts operating in the saturation region, and so the voltage dropped on the device is increasing. When v_i is increased over the MESFET saturation voltage, the device enters the linear region acting like a resistor; similar situation with the closed switch (Fig.5.2c). Assuming that the v_i and R_L values are chosen depending on the MESFET electrical characteristics, the V_{DD} supply voltage drops on the resistors such that the output voltage v_o is pulled down to the ground level.

It is important to mention that this approach can be used for any N-channel FETs, including SiC devices. In order to have a better perspective on the existing MESFET logic families, a brief overview of few important GaAs MESFET logic families is commented in the next section.

5.1.3 MESFET Logic Families

Most of the current digital ICs logic families are designed especially for Silicon applications. Even though the dominance of Silicon as the most widely used semiconductor is expected to continue for many years to come, new semiconductor materials have been making inroads into digital applications that require extremely high operation speeds, high temperature operation and also radiation hardness stability.

Gallium Arsenide (GaAs) technology has received a lot of interest in the 80s-90s mostly developing the N-channel MESFETs and the Schottky diode as main active devices. The two main approaches of the existing logic families on GaAs account for the operation mode of the devices. One family uses only normally-*on* devices, while the second contains both enhancement and depletion mode devices. For a general overview, two of the most representative logic families from these two main approaches are next presented.

5.1.3.1 Buffered FET Logic (BFL)

The Buffered FET Logic (BFL) on GaAs was first reported in [7, 8]. This circuit topology employs only depletion-mode MESFETs. The circuit configuration of the basic Inverter is shown in Fig.5.4. The core of the logic section is formed by the *switching* and the *load* transistors. Both transistors are depletion mode, being controlled with a negative voltage. On the other hand, the drain voltage is positive; therefore, the logic level at the drain of the *switch* is not compatible with the level required at the gate input. Thus, a *voltage level shifter* is necessary at some point so that the output logic levels match with the input ones.

In the BFL circuit, the *level shifter* is formed by two Schottky diodes always forward biased by the *source follower* transistor. To ensure that the *current source* transistor is always operating in the saturation region, it has its source connected to the negative supply voltage. It is necessary to mention that between circuit power supplies and DC devices parameters exists the following dependence:

$$V_{DD} = -V_{SS} = 2 \times \max(|V_P|) \tag{5.1}$$

As the load and the follower transistors are wired so that they are always working in saturation region supplying a constant current to the diodes, the operation of the circuit is given by the switching transistor.

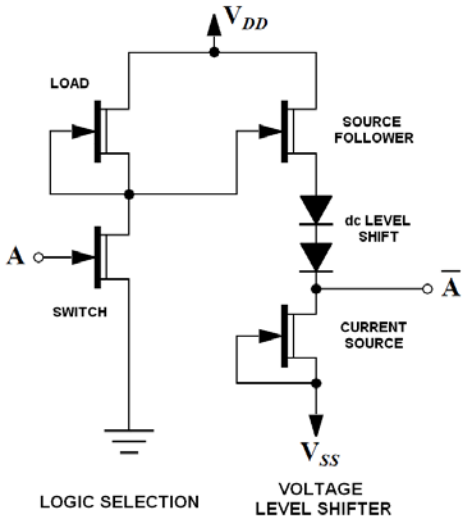
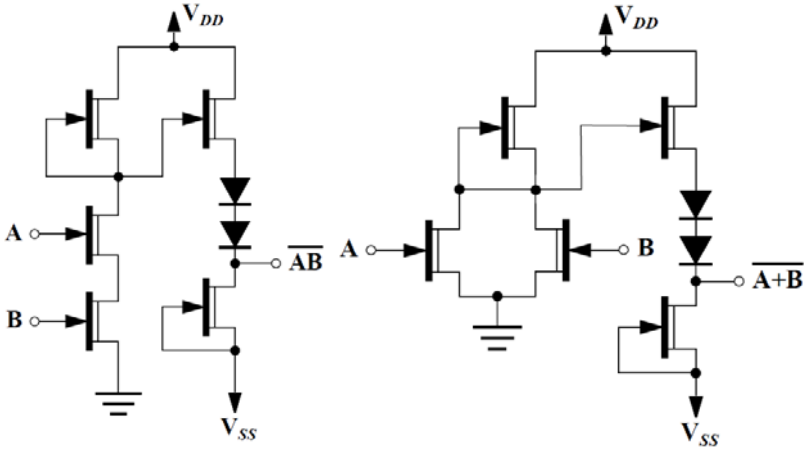


Fig.5.4. *Circuit configuration for a BFL of a basic Inverter circuit [8]*

Once the input voltage at the switching gate transistor is lower than its V_P, the device is turned off. Thus, the source of the follower transistor is pulled up to V_{DD}. As the current source transistor is pulling down to its drain the voltage V_{SS}, at the output of the circuits the voltage will be approximately 0V. When a voltage higher than the V_P is applied to the input, the switching transistor is working in the triode region and the follower's source is pulled down the ground level (0V). Thus the voltage output of the circuit is approximately half of V_{SS} (or close to V_P).



(a) ***(b)***

Fig.5.5. *Circuit implementation of a BFL a) NAND and b) NOR logic gates*

Starting from the Inverter circuit configuration, other basic logic gates can be obtained, as shown in Fig.5.5. The NAND and the NOR logic gates are obtained by adding more

transistors to the logic selection level. The NAND gate is realized by stacking two MESFETs in series, while the NOR is formed with two transistors in parallel.

5.1.3.2 Direct-Coupled FET Logic (DCFL)

The Direct-Coupled FET Logic (DCFL) is the first, simplest and most widely used enhancement/depletion mode GaAs logic family. This circuit topology employs both enhancement and depletion-mode MESFET devices, being very similar to the E/D NMOS logic circuit configuration.

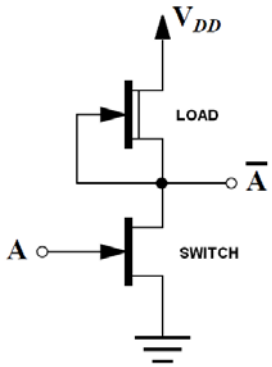


Fig.5.6. *Circuit configuration for a DCFL basic Inverter*

The Inverter gate utilizes only two devices: an enhancement MESFET for the input *switching* transistor, and a depletion MESFET for the *load* transistor. Because the *switching* transistor starts conducting at gate voltages higher than 0V, no level shifter is needed. The saturation voltage of an enhancement MESFET is lower than that of the depletion MESFET. Therefore, the power supply voltage can be lower than in the BFL case. The elementary logic gates NAND and NOR can be obtained using the same approach as for the BFL, adding an enhancement MESFET in series or in parallel for the NAND and the NOR gates, respectively.

The DCFL digital logic family uses both normally-*on* and -*off* devices, not being quite appropriate for our future approach in the present development. Thus, a novel circuit topology combining normally-*on* JFET with epitaxial resistors on 6H-SiC is proposed in the following section.

5.1.4 Normally-*on* 6H-SiC JFETs and Epitaxial Resistors Topology

Unlike CMOS or bipolar logic families on Silicon, on SiC there is a lack of standard logic families. Most digital circuits require a mixed use of complementary N- and P-channel devices, or mixed depletion and enhancement mode devices. Nevertheless, combining these kinds of structures the resulting logic circuit cannot work at extreme temperatures. However, [9] shows that the basic current-voltage characteristics of the 6H-SiC JEFT at 600ºC are quite similar to those of GaAs MESFET at room temperature employed in digital ICs. Recently, the NASA-Glenn Research Center has developed a circuit topology for a small number of devices able to build digital logic gates using normally-*on* 6H-SiC JFETs and epitaxial resistors [10] based on the BFL and DCFL GaAs digital logic families.

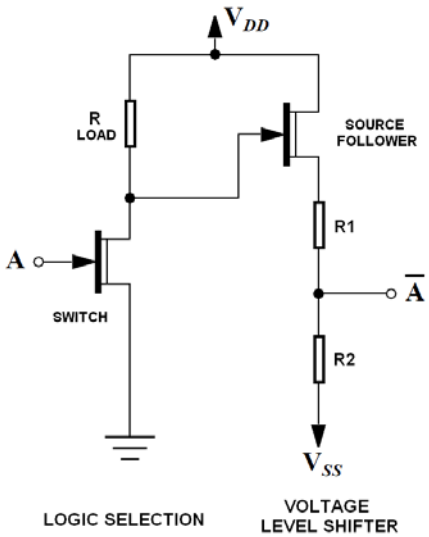
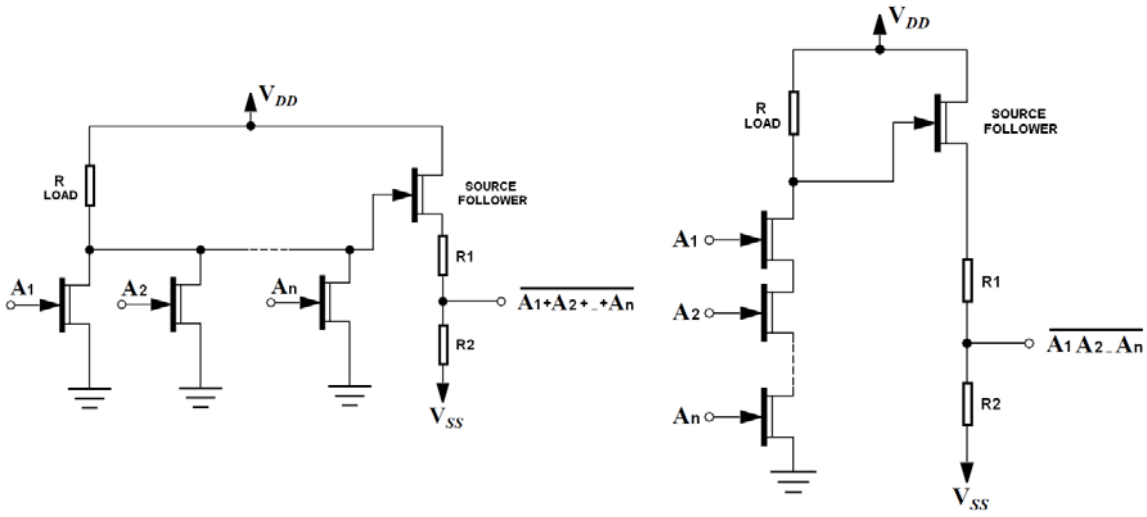


Fig.5.7. *Circuit configuration for a basic 6H-SiC JFET Inverter*

The circuit configuration of the Inverter (Fig.5.7) combines a normally-*on* JFET (switch) and an epitaxial load resistor (R_{LOAD}) in the front stage of the circuit. Like in the BFL case, a *voltage level shifter* (or buffer) is needed in order to match the output and input logic levels. In the present topology, the voltage level shifter is made up of a source follower transistor wired so it works always in saturation, together with two epitaxial resistors (R_1 and R_2) acting like a voltage divider.

If in the BFL case, a load transistor, a current source transistors and dropping diodes were used, here are used instead the *epitaxial resistors* performing the buffer operation. The values for the resistors are related to the characteristics of the transistors, as well as the

power rails V_{SS} and V_{DD}. Although the general operation of the circuit is very similar to the BFL, the resistor divider for the level shifter stage presents a disadvantage. This main drawback is that the gain on the whole gate is decreased because the resistor-voltage divider – the voltage drops across R_1 and R_2 are higher than the R_{ON} of the current source transistor and the dropping diodes. Following the same approach as for BFL and DCFL, when the *switching* transistor from Fig.5.7 is replaced by a series or parallel string of *n*-FETs, the circuit becomes an *n*-input NAND (Fig.5.8a) or an *n*-input NOR logic gate, respectively (Fig.5.8b).



(a) ***(b)***

Fig.5.8. *Circuit configuration for a SiC-JFET* ***(a)*** *NAND and* ***(b)*** *NOR basic logic gates*

One can obtain any desired logic function with different combinations of transistors in series and/or parallel in first logic level of the circuit. Any common digital building block can be configured using elementary logic gates and/or defined logic functions, which enables the synthesis of other complex combinational, pulse or edge devices.

The NASA-Glenn Research Center has shown that its current state-of-art in component production technology allows the fabrication of N-channel JFETs and epitaxial resistors on a substrate only for a small number of components. However, in our approach we have used the 4H-SiC MESFET, due to the technological maturity and simplicity [11-13]. In the following chapters the modeling of basic logic gates realized with normally-*on* 4H-SiC MESFETs and 4H-SiC epitaxial resistors are presented. The design of complex multi-stage digital circuits realized with a large number of devices is also tackled.

5.2 4H-SiC MESFET Basic Logic Gates

The design and development of SiC integrated circuits (ICs) is nowadays a necessity due to the increasing demand for high temperature intelligent power applications and intelligent sensors. There are current reasons for placing intelligent ICs near or within high temperature sources (300°C and higher) [14, 15]. Electronic components for use at these temperatures are typically made of SiC, which can operate successfully at temperatures as high as 500° C [16, 17]. However, processing either in an analog or digital domain requires components whose parameters are closely matched and, as a consequence, on the same die, as an IC case. Therefore, this section concerns the basic logic gates circuits design and simulations, together with the proposed layout design. The elementary logic gates library contains the Inverter, NAND and NOR gates, created with 4H-SiC MESFET and epitaxial resistors.

Our preference for MESFETs versus nMOSFET/JFET is due to the already proved stability of the Tungsten-Schottky barrier technology that was successfully used in the fabrication of stable SiC Schottky diodes for the European Space Mission BepiColombo [11]. Moreover, the MESFET shows a very stable pinch-off voltage behavior with temperature.

5.2.1 Design, Modeling and Simulation: INV, NAND, NOR

A very important step in achieving the desired ICs is the design, modeling and simulation of both used devices and circuits. In Chapter III the design, modeling, simulation and fabrication of the 4H-SiC MESFET was already presented. The ICs topology developed by NASA using normally-*on* 6H-SiC JFETs and epitaxial resistors based on the GaAs digital logic families BFL and DCF is presented in the previous section (5.1.4). This is the topology that will be adopted in the present design for the 4H-SiC MESFET elementary logic gates.

The design of the basic logic gates is constrained by the MESFET area, the load resistance, the influence of the pinch-off voltage on the logic gates levels and the recommended DC power supply voltage to obtain proper circuit functionality in the 25°C-300°C temperature range. These elementary logic gate designs will provide the basis for more complex integrated digital circuits on 4H-SiC.

5.2.1.1 Logic Gates Circuits Configuration

As stated in previous section, starting from the Inverter structure, which is the most basic element in digital circuitry, other elementary logic gates can be easily built up. As in the case of GaAs BFL and the SiC NASA's topology, a load resistor and a level shifter are necessary in order to match the output and input logic levels of the gates. The Inverter architecture using scalable 4H-SiC MESFETs and epitaxial resistors is shown in Fig.5.9.

The level shifter is made out of a voltage follower and a two-resistor divider. The Low (L) output logic level has negative value, close to the pinch-off voltage value V_P of the MESFET, while the High (H) voltage level is the ground value. The negative voltage control of the MESFET requires two voltage power supplies, a positive one V_{DD}, and a negative one V_{SS}, both referred to ground. The values of the voltage divider resistors are chosen as a function of the $I_{DSS(min)}$ of the device and the supply voltage.

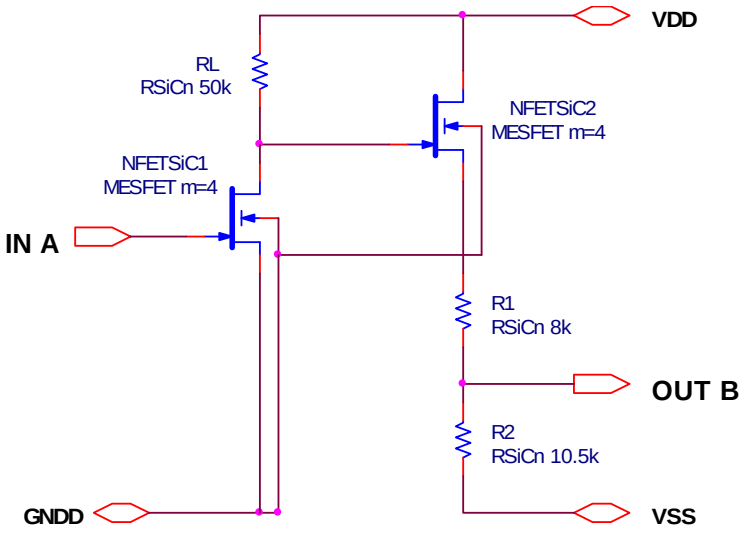


Fig.5.9. *The 4H-SiC MESFET Inverter circuit configuration*

The **main operation** of **the 4H-SiC MESFET Inverter** (Fig.5.9) is given by the logic level section; i.e., by the MESFET transistor (NFETSiC1), whose source is tied to ground and its drain to V_{DD} through the R_L resistor (load resistor). The second MESFET transistor (NFETSiC2) is configured as a voltage follower, always working in saturation, and has its source tied to the two-resistor divider (R_1 and R_2). Even though that there is a small voltage drop across the R_L and follower transistor, this is not affecting the circuit logic levels.

$$V_{OUT} = \frac{R_2}{R_1+R_2} \cdot (V_B + V_{SS}) \tag{5.2}$$

The Inverter function is controlled by the input voltage (***IN A***) applied to the front end MESFET's gate.

If the input voltage is at the ***High Logic Level*** (IN A=0V), *NFETSiC1 turns on*, thus acting like a closed switch (Fig.5.10a). The supply voltage V_{DD} drops across the load resistor. Therefore, the NFETSiC2 gate (point A) is pulled down to the ground level. As NFETSiC2 is wired so it always works in the saturation region, it pulls the ground to its source, in point B. Using the voltage-resistor divider eq. (5.2), we can then estimate that the output voltage has a value close to the MESFETs pinch-off voltage (eq. (5.1)), which is considered the *Low Logic Level*.

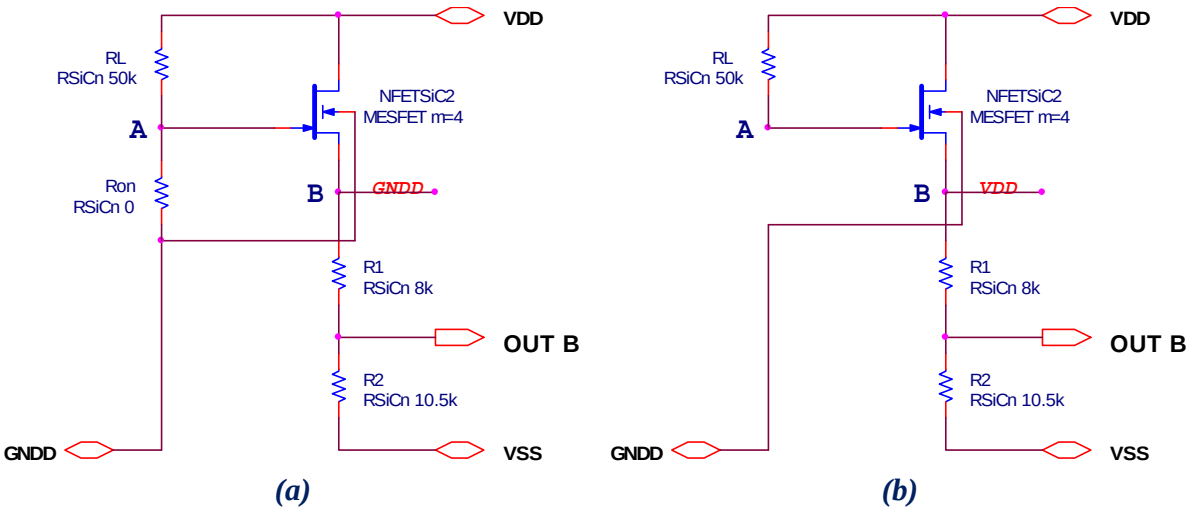


Fig.5.10. *The 4H-SiC MESFET Inverter circuit configuration equivalent to* ***a)*** *High-to-Low and* ***b)*** *Low-to-High Levels*

If the input voltage is at the ***Low Logic Level***, the NFETSiC1 MESFET's gate is tied to a ***lower*** voltage than its pinch-off, and *the device is turned-off* acting like an open switch (Fig.5.10b). Thus, the gate of the follower (point A) is pulled up at V_{DD} thought R_L. The source of the NFETSiC2 follower transistor (point B) will be at a potential approximately equal to the supply voltage V_{DD}. Therefore, the Inverter output will reach a value close to 0V, which is the *High Logic Level*.

If in the Inverter circuit from Fig.5.9 we replace NFETSiC1 by a string of two MESFETs in series, we get the NAND basic logic gate (Fig.5.11a). Furthermore, if we replace it by two MESFETs in parallel, we have the NOR logic gate (Fig.5.11b). Following the same approach presented in the previous chapter, and employing a string of transistors either in series or/and in parallel at the input logic level section, more complex logic functions can be derived.

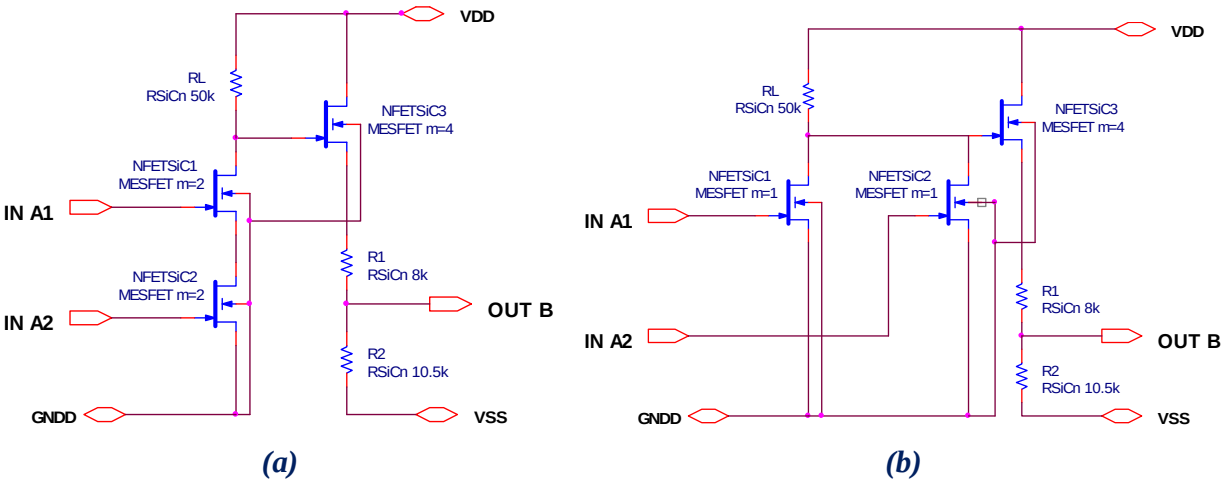
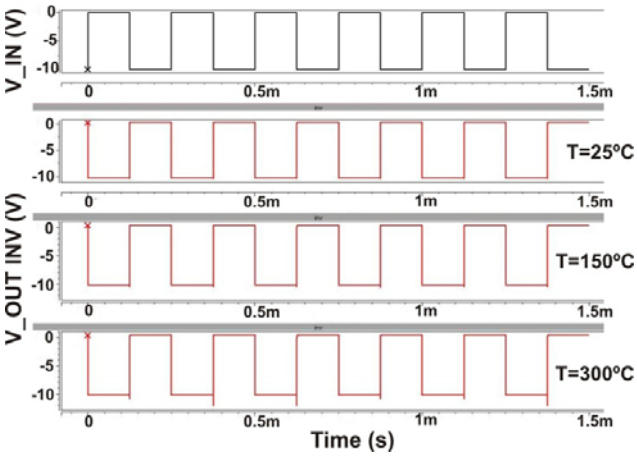


Fig.5.11. *The 4H-SiC* ***(a)*** *NAND and* ***(b)*** *NOR circuits configuration*

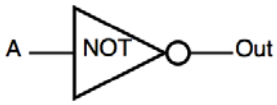
The *Fan-In* of a gate is the number of its inputs. The *Fan-Out* is the maximum number of similar gates that a gate can drive while performing a proper operation. Therefore, the simplest way to get a high fan-out of the logic gates is to use a higher multiplicity of the follower transistor (NFETSiC3) and a proportional reduction of the corresponding resistors of the voltage-divider.

5.2.1.2 Logic Gates Simulation

High temperature applications have been continuously increased in the last decades even though Silicon-based ICs have reached their physical limitations. Thereby, the SPICE analysis for high temperature operation is a part of the complete design cycle for experimental high temperature logic gates. In this sense, SPICE simulations were performed up to 300ºC. The SPICE model used for the circuit's simulations was the planar-MESFET initially proposed in Annex.A2. Fig.5.12 shows the simulated waveforms for each elementary logic gate (Inverter, NAND and NOR) together with its symbol and truth table. For a proper functionality, the voltage level of the power supplies should be roughly 30% higher than $\times 2V_P$ of the SiC MESFETs. In the initially proposed planar-MESFET SPICE model, the pinch-off voltage was established at –8V. Thus, we have used V_{DD}=+25V and V_{SS}=-30V power supplies in our simulations. However, the Low and High logic levels can be easily tuned by adjusting properly the supply voltages. Although these values might seem to be unusual, they are quite normal for this kind of logic and the specific high V_P value of the device. For a lower V_P, the power supply voltage could be decreased significantly.

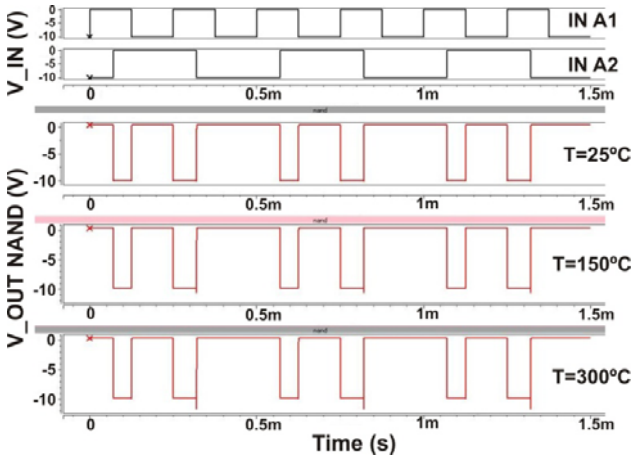


*(a) **INV** Simulated waveforms*



A	Out
0	1
1	0

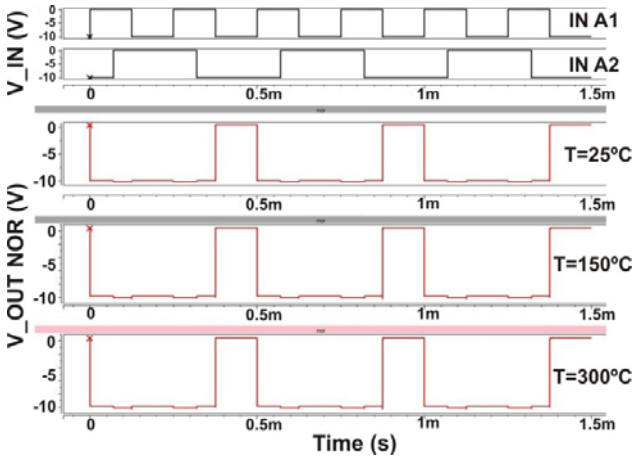
*(b) **INV** Symbol and Truth table*



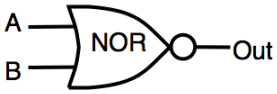
*(a) **NAND** Simulated waveforms*

A	B	Out
0	0	1
0	1	1
1	0	1
1	1	0

*(b) **NAND** Symbol and Truth table*



*(a) **NOR** Simulated waveforms*



A	B	Out
0	0	1
0	1	0
1	0	0
1	1	0

*(b) **NOR** Symbol and Truth table*

***Fig.5.12.** The 4H-SiC MESFET basic logic gates **(a)** simulated waveforms for three different temperatures and **(b)** their Gate Symbol together with the corresponding Truth Table*

The simulated output response diagram plotted on Fig.5.12a shows very similar waveforms for the whole temperature range and for every elementary logic gate at three different temperatures: 25ºC, 150ºC and 300ºC. From the MESFET's high temperature operation we have seen that its pinch-off voltage is keeping quite a constant value (around -8.5V – see Fig.3.11 and Fig.3.12) for the whole temperature range. Hence, the switching transistor (NFETSiC1) turns from *on* to *off* at around V_P, independently of the operation temperature. The slight variations observed in the simulated temperature waveforms are mainly explained in terms of the level shifter behavior in temperature. The R_1 and R_2 resistors show the same temperature coefficients; thus, the resistor-divider will show the same ratio within the entire temperature range. Therefore, the very small changes observed at higher temperatures are mainly caused by the follower transistor as it is biased so it always works in saturation. Due to the specific higher reverse leakage of the Schottky gate contact, the working temperature should be limited around 300ºC for a proper function of the MESFETs.

5.2.1.3 The 4H-SiC MESFET Inverter Performance

For the sake of a deeper analysis of the 4H-SiC MESFET digital logic family performance, its most basic digital element – the Inverter, is evaluated. The typical parameters that are generally used to characterize the operation and performance of a logic-circuit family are the *noise margins*, the *power dissipation* and the *propagation delay* of the gate [18].

The *Noise Margins* ***(NMs)*** – are important figures-of-merit for digital circuits, accounting for the robustness of a circuit, and showing its ability to provide a proper operation in noise presence. This parameter is extracted from the Inverter's VTC (voltage transfer characteristic):

$$NM_H = V_{OH,min} - V_{IH,min} \tag{5.3}$$

$$NM_L = V_{IL,max} - V_{OL,max} \tag{5.4}$$

where $V_{OH,min}$ and $V_{IH,min}$ are the minimum high output and the input voltage levels, respectively; and $V_{OL,max}$ and $V_{IL,max}$ are the maximum low output and the input voltage levels, respectively.

The *Power Dissipation* ***(P_D)*** – is also a key issue in digital circuits. As in modern digital systems a large number of gates are involved, it is mandatory to keep the total power requirements within reasonable boundaries. The static power consumption is the product of

the device leakage current and the supply voltage, causing static power dissipation in the devices. It refers to the power the gate dissipates when it is not *on*.

The *Propagation Delay* (T_P) – characterizes the dynamic performance of a logic family. It is defined as the switching time between the input and the output signals of the logic Inverter. As shorter the propagation delay as higher the speed at which the digital circuit can operate.

$$T_P = \frac{1}{2}(T_{PLH} + T_{PHL}) \tag{5.5}$$

Table.5.1. *The switching threshold voltage and the noise margins of the 4H-SiC MESFET Inverter gate*

	ΔV_M [V]	NM_L [V]	NM_H [V]
Temp = 25ºC-150ºC	0.15	-0.2	+0.25
Temp = 150ºC-300ºC	0.04	-0.1	+0.11

Fig.5.13 shows the simulated Inverter's VTC characteristics (similar to those of Fig.5.3b). For each temperature the input-output characteristic has been plotted together with its inverse in order to graphically estimate the gate NMs. Increasing the temperature from 25ºC to 300ºC, the output high and low voltage levels (V_{OH} and V_{OL}) show a very small positive voltage shift.

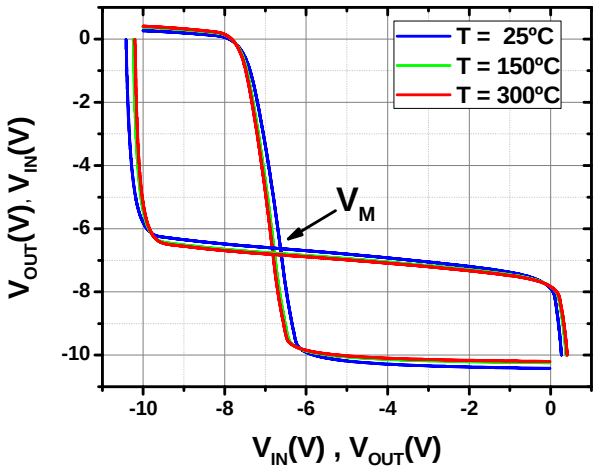


Fig.5.13. *The 4H-SiC MESFET Inverter simulated VTC at 25ºC, 150ºC and 300ºC*

The switching threshold voltage (V_M), defined as the central intersection point in the VTC, experiences a very small negative voltage shift as well (Table.5.1). This behavior can be explained in terms of the increase of the leakage current with temperature. However, this

small variation of the switching threshold voltage is not affecting the functionality of the gate in temperature. Moreover, the noise margins defined in eqs. (5.3) and (5.4) show quite a stable behavior in temperature. However, we have observed that V_M and the noise margins shift are lower at high temperatures. Thus, confirming that the circuit robustness ensures the functionality of the gate at high temperature.

Table.5.2. *Output static power dissipation and propagation delay of the 4H-SiC MESFET Inverter gate*

	$P_{OUT(LOW)}$ [mW]	$P_{OUT(HIGH)}$ [mW]	T_{PLH} [ns]	T_{PHL} [ns]
Temp = 25ºC	115	159	9.2	3
Temp = 300ºC	28.1	38.6	35	5.5

Table.5.2 summarizes the gate static power dissipation at the Low and High output levels. One can observe that the logic gate dissipation power decreases approximately 4 times at 300ºC; therefore, presenting quite a significant static power loss at high temperatures. Although the simulated waveforms of the Inverter (Fig.5.12a) show a good behavior at elevated temperatures, the resistance temperature coefficient is positive (Chapter IV). Therefore, the currents significantly decrease at elevated temperatures, which results in an important decrease of the gate power at high operation temperatures. However, the main static power losses in the circuit at high temperatures come from the voltage follower transistor since it is always working in saturation mode.

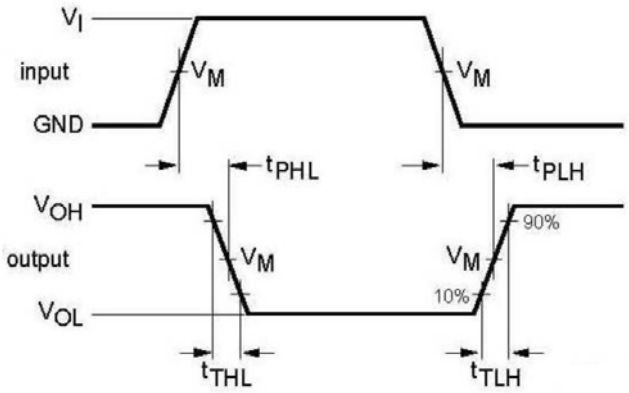


Fig.5.14. *Definition of propagation delay and switching time of a logic Inverter*

The average propagation delay (eq. (5.4)) at 25ºC is 6.15ns and 20.25ns at 300ºC. The estimated low-to-high T_{PLH} and high-to-low T_{PHL} propagation delays show a fairly small

variation in temperature, being comparable with a single high performance CMOS Inverter [19]. The input signal rise time has the same value as the fall time, which is 10ns. It can be observed that the average propagation time presents a short delay, hence ensuring a high speed of the gate and, therefore of the 4H-SiC logic family.

After analyzing the basic Inverter gate performance we can assert that the 4H-SiC MESFET logic family is predicting a good circuit performance. Moreover, since all the other elementary logic gates are designed starting from the basic configuration of the Inverter (Fig.5.11) they are expected to have a similar performance.

5.2.1.4 Layout Design

The ICs complexity has been highly increasing along the time, leading to several levels of metal interconnections to ensure that enough wires can be made to create all necessary connections between the components. The integration of wires with components (invention of Robert Noyce), which prevents the need to mechanically wire together components on the substrate, was one of the key inventions that made the integrated circuit feasible.

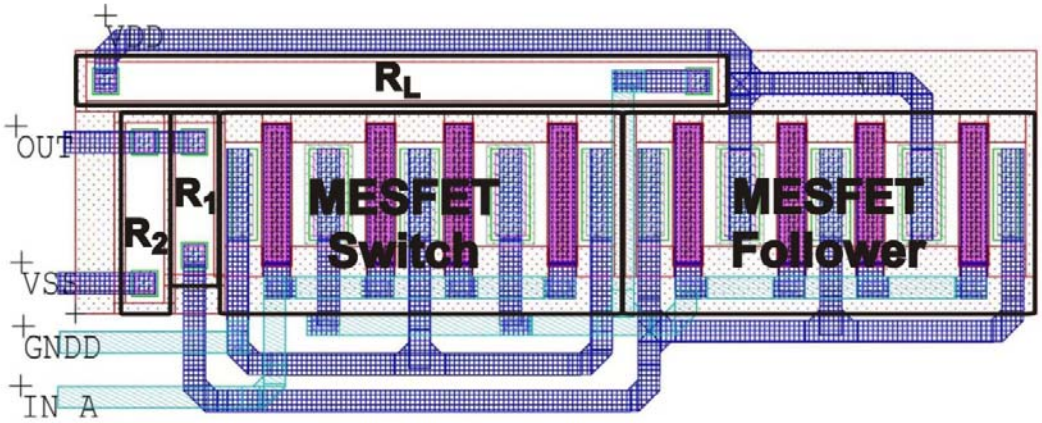


Fig.5.15. *The 4H-SiC MESFET Inverter circuit layout with the input and output signals connections*

In the presented SiC ICs layout design, due to the complexity of the circuits, three metal levels are used, from which two of them are used for component interconnections. In this way, a great freedom is achieved in placing the devices in the layout design of the circuits. The design rules are the same as those for designing the layout for the new MESFET devices, which are presented in Annex.B.

Fig.5.9 shows the Inverter circuit schematic architecture. From the above diagram one can easily observe the placement of each device in circuit. The layouts for NAND and NOR gates were drawn following the same approach.

5.2.2 Circuits Fabrication

Chapter III – Section 3.2 reports the fabrication process flow for the newly developed MESFET. 10 photolithography masks were needed to realize the complete fabrication of the device, four of which were needed for the metal and via levels (Table.3.2 – ICs MESFET fabrication), resulting in a 3 metal levels technology.

The last two metal levels were mandatory in order to easily connect all circuit components and to make transistors with a high multiplicity. All these have led to the development and fabrication of SiC ICs involving a large device number, as it will be presented in the next sections. To our knowledge, such a complex technology with 3 metal levels for designing ICs on SiC has not been reported so far. The circuits manufacture was quite a challenge for the current SiC state-of-the-art fabrication.

In order to emphasize the complexity of the fabrication process, the next figure shows a picture of the manufactured elementary logic gates: the Inverter and the NOR. It is important to remark that all fabrication steps were carried out at the CNM's Clean Room with a 2µm lithography standard. The metal interconnection tracks are 10µm width. Electrical characterizations of the fabricated elementary gates are presented in Section 5.4.

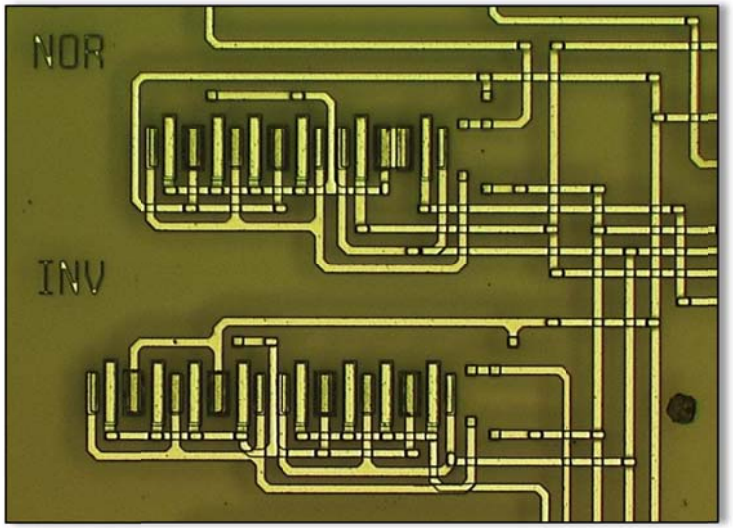


Fig.5.16. *The fabricated circuits of the 4H-SiC MESFET Inverter and NOT logic gates*

5.3 4H-SiC MESFET Multi-Stage Digital ICs

In the previous section we have presented the design, modeling and simulation of the elementary logic gates library built from normally-*on* 4H-SiC MESFET devices and epitaxial resistors using the topology developed for 6H-SiC JFET [20]. However, it has been shown that due to the current JFET SiC fabrication processing limitation, the ability of ICs production capabilities was limited to a reduced number of devices, leading to small logic gates and simple basic logic functions [9].

In this chapter, we present the design and modeling of multi-stage dynamic building blocks on SiC using the previously developed 4H-SiC MESFET basic logic gates library. The aim is to demonstrate the functionality of more complex digital SiC ICs and to provide a greater flexibility for integrating SiC MESFET logic gates in typical CMOS topologies. Standard CMOS topologies have been successfully transferred and embraced using the 4H-SiC MESFET elementary logic gates (Inverter, NAND and NOR).

5.3.1 Common Dynamic Building Blocks

The ability to produce embedded logic gates makes it possible to produce different complex circuits, such as pulse or edge triggered latches and Flip-Flops. The basic logic gates can be used to build other dynamic blocks like ring oscillators, voltage controlled oscillators, phase detectors, digital counters, phase locked loop circuits (PLL) and other typical digital logic schematics able to operate at high temperature.

In digital electronics systems *Flip-Flops (FF)* and *latches* are fundamental building blocks used in computers, communications and many other systems. Even though FF and latches are many times used interchangeably, a latch is mainly used for storage elements, being transparent during the entire time when the enabled signal is asserted, whereas the FF is a *synchronous* or *edge-triggered* device, being transparent only for a brief interval during the Clock edge [21, 22].

In this chapter we present some of the most common digital building blocks used in digital electronic systems: Toggle FF (TFF), Master-Slave FF (DFF) and Data-Reset FF (DRFF). The major differences between these FF types are the number of inputs they have, the way they change state, and the building technology. For each type, there exist also different variations that enhance their operation. Next, a brief presentation of each of these devices is exposed:

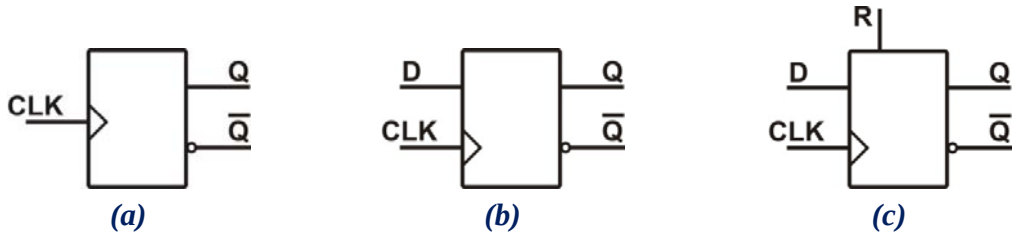


Fig.5.17. *The general graphical symbol of:* ***(a)*** *TFF,* ***(b)*** *DFF and* ***(c)*** *D-Reset FF*

a) The **Toggle FFs** is a bistable device with only one input, typically the Clock signal. It changes its output state on each negative Clock edge, giving at the output half of the frequency of the Clock input signal.

b) The **DFF** is the most common sequential element used in the digital design [21] not being transparent. It follows the input D (Data) only when the Clock is enabled. The states at the output change depending on the edges of the Clock signal. In CMOS technology these devices are implemented either at transistor level or using SR latches [23]. The TFF can be easily made from a DFF by connecting the Data to the negative output (Qb).

c) The main structure of the **D-Reset FFs** is similar to that of the DFF with an additional asynchronous Reset signal [24]. This signal has the purpose to set the circuit's proper state, this way avoiding undesired states of the device.

As Set-Reset Latch and Data Latch are included in the realization of two of the above mentioned digital blocks (D-Reset FF and DFF), these latches can be considered as the most basic sequential logic circuits [25].

5.3.2 Design, Modeling and Simulation

In the previous section we reported the complete high temperature design library for 4H-SiC MESFET basic logic gates. This elementary library allows us to implement multi-stage logic embedded in power management circuitry. In the following sections the design, modeling and simulation of previously mentioned complex digital building blocks are presented (Fig.5.17). They are realized at transistor level or adopting standard Si-CMOS topologies. This is an important aspect since the technology transfer from a logic family to another is not always straight forward.

The design and functionality of the present dynamic building blocks is constrained by the elementary logic gates operation. The SPICE model used in simulations is the same one used for modeling the basic logic gates (Annex.A2).

5.3.2.1 The XOR Gate

Although the Exclusive OR (XOR) is considered a single digital logic gate with two or more inputs and one output that performs an exclusive disjunction, we have considered it as complex ICs since its implementation requires more elementary logic gates. The output of an XOR gate is High exclusively when only one of its inputs is High. If all the inputs are Low, then the output of the XOR gate is Low:

$$\text{OUT XOR} = A\overline{B} + \overline{A}B = (A + B)(\overline{AB}) \tag{5.6}$$

In order to design the XOR gate, eq. (5.6) shows the logic expression of a XOR with two inputs (A and B). In CMOS technology the XOR gate can be implemented at transistor level, but also with different gates combinations. If a limited number of specific gates are available in a topology, the XOR gate circuit can be constructed using these gates.

The NAND and NOR are so-called “universal gates” because any logical function can be constructed with them. Therefore, a XOR circuit can be easily configured from NAND or NOR gates. Fig.5.18 shows the XOR circuit configuration with a NAND, an Inverter and two NOR basic gates. This XOR circuit topology is the one presented in [20] that was realized with SiC JFETs.

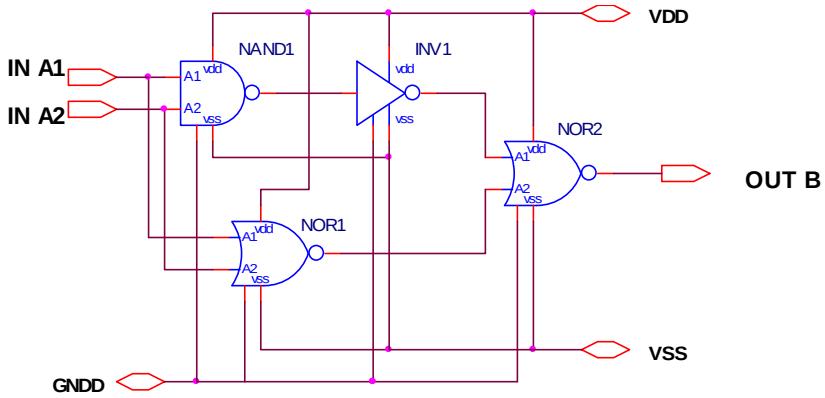
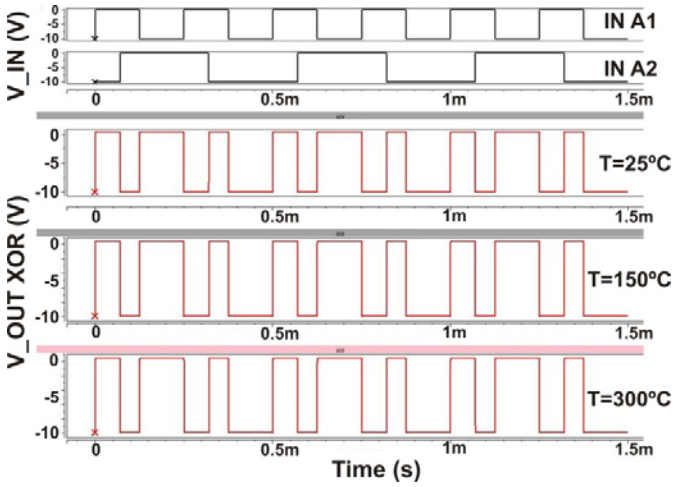


Fig.5.18. *XOR circuit architecture based on 4H-SiC MESFET universal gates*

Fig.5.19 shows the simulated diagrams of the XOR circuit together with its typical symbol and truth table. The output response presents a very similar waveform for the entire temperature range, being in a good agreement with the basic logic gates temperature behavior.



A	B	Out
0	0	0
0	1	1
1	0	1
1	1	0

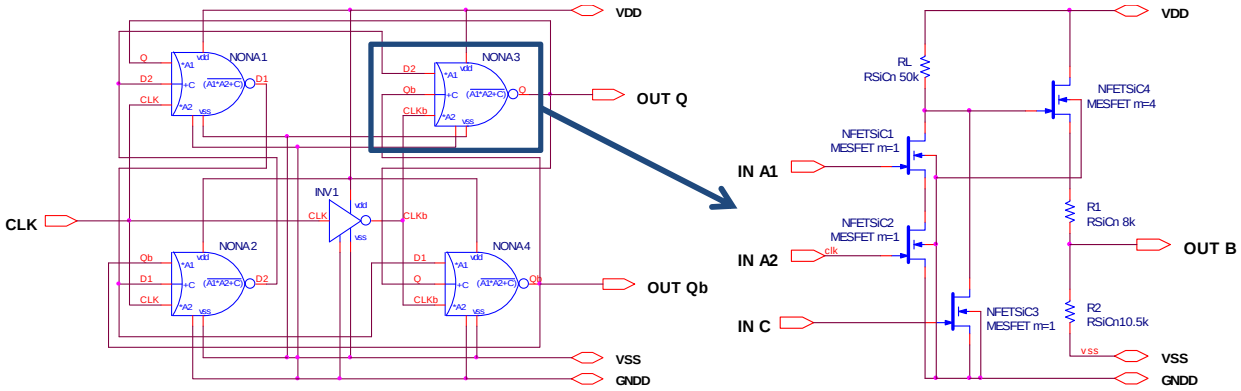
Fig.5.19. *XOR* ***(a)*** *Simulated diagram and* ***(b)*** *its Gate symbol with Truth Table*

The XOR circuit layout design was created using instances of the previous basic logic gates layouts. Therefore, at design and simulation level, it has been proven that using the previous elementary logic gates one can easily derive different logic functions. The XOR gates are particularly useful in arithmetic operations as well as in error-detection and correction circuits.

5.3.2.2 The Toggle Flip-Flop

The Toggle Flip Flop is the first designed digital building block. It is a single input device – trigger or clock, which changes its output on each Clock edge, giving at the output half of the frequency of the Clock input signal. The TFFs are useful digital blocks in constructing binary counters, frequency dividers and general binary addition devices. As previously mentioned, in CMOS technology the TFF is in fact a Data Flip-Flop that is obtained by connecting the D input to the negative output (Qb) of the device.

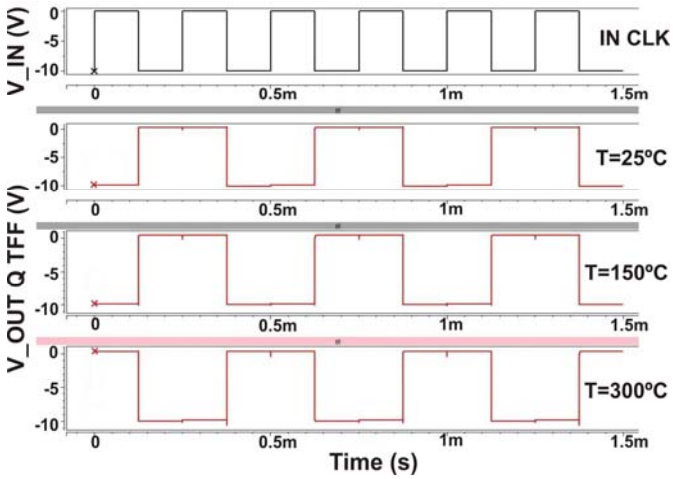
As already mentioned, there are more ways of realizing digital building blocks. In order to first verify the functionality of digital logic functions formed with normally-*on* 4H-SiC MESFETs, Fig.5.20a shows the TFF circuit configuration developed for normally-*on* 6H-SiC JFETs [1]. This TTF configuration was realized using 4 digital gates performing the logic function: $\mathrm{OUT\ B} = \mathrm{NOT}(\overline{\mathrm{A1} \cdot \mathrm{A2}} + \mathrm{C})$ (Fig.5.20b).



(a) *(b)*

***Fig.5.20. (a)** The 4H-SiC MESFET Toggle FF circuit configuration and **(b)** $OUT\ B = NOT(\overline{A1 \cdot A2} + C)$ additional logic function*

Although the above configuration utilizes special digital functions, this construction was optimized at transistor level. One can observe that the TFF implemented in Fig.5.20 is much smaller than the one implemented with the CMOS technology (Fig.5.22). We need a total of 33 individual devices, 18 of them are 4H-SiC MESFET transistors and 15 epi-resistors. As it will be presented in the DFF section, the CMOS design needs almost twice the number of devices.



Clk	Q
0	Change
1	Q_{n-1}

(a) *(b)*

***Fig.5.21.** Toggle FF **(a)** Simulated diagram and **(b)** Truth table*

From the simulated time diagrams one can observe that the circuits operate properly in the whole temperature range (25ºC – 300ºC) changing its output signal at each negative Clock edge. Although the 300ºC simulated waveform seems different, it should be noticed that the output response reading was done at the next negative Clock edge than for the other

temperatures. These changes can occur due to the delays that might appear while reading the input signal. The test circuit used for simulating the TFF can be found in Annex.C.

5.3.2.3 The Master-Slave Data Flip-Flop

In order to demonstrate the technological transfer for some important multi-stage digital building blocks from the CMOS technology to the 4H-SiC MESFET technology, we have designed the Master-Slave Data Flip-Flop (DFF) using 4H-SiC MESFET elementary logic gates library. The present DFF circuit is the most complex built multi-stage SiC circuit realized in the present work. It is built with two D gated latches in series, inverting the enable input (usually the Clock) to one of them.

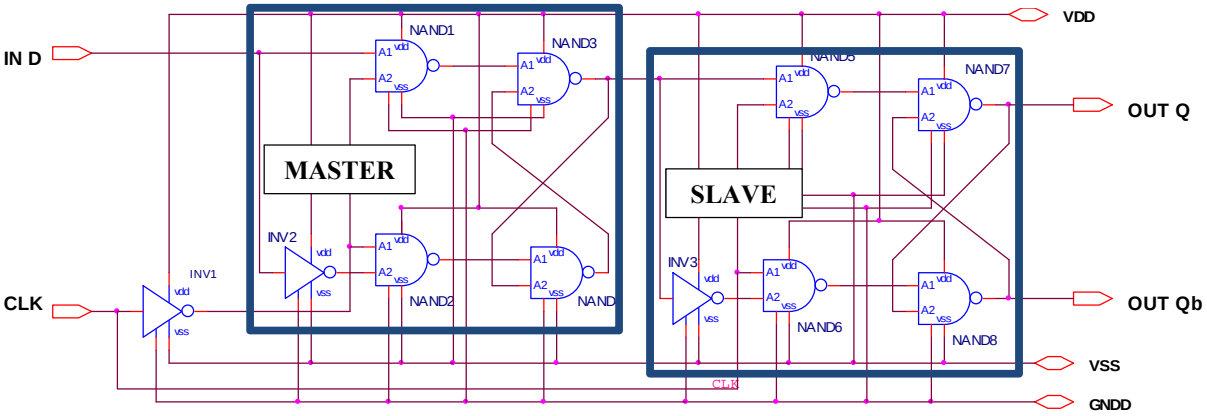
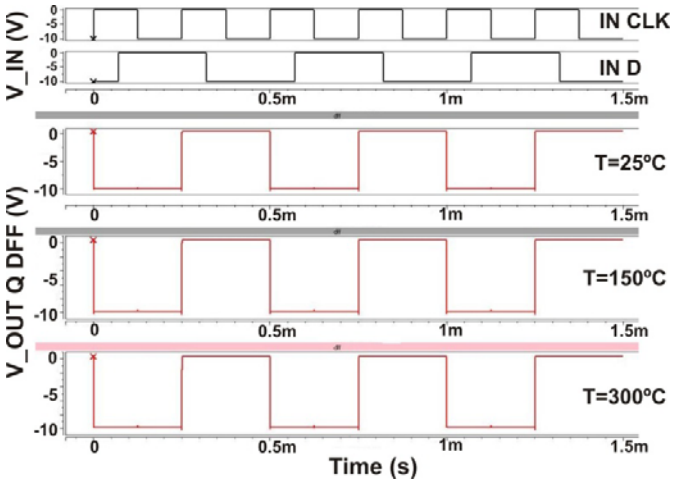


Fig.5.22. *Circuit configuration 4H-SiC MESFET Master-Slave DFF*

The present configuration of the Master-Slave DFF (Fig.5.22) contains two D latches. The Master stage is active during the half of Clock cycle (when Clock signal is at High) and the Slave stage is active during the other half (when Clock signal is at Low). It is called Master–Slave because the second latch in series only changes in response to a change in the first one. When the Clock is High, the Master D latch follows the Data input at the output on the trailing (final) edge of the Clock pulse, disabling the Master until the Clock goes High again. When the Clock goes Low the inverted Clock signal at the Clock input of the Slave enables it, taking the Master output at its output. The Slave gets enable every time the Clock goes Low. Connecting the negative output (Qb) of the DFF to the Data input, the circuit acts like a binary counter, or like a TFF.



Clk	IN D	Q	Q_{n+1}
0	×	0	0
0	×	1	1
1	×	0	0
1	×	1	1
↑	0	×	0
↑	1	×	1

(a) ***(b)***

Fig.5.23. *Master-Slave DFF* ***(a)*** *Simulated diagram and* ***(b)*** *Truth table*

Fig.5.23 shows the simulated waveforms of the DFF block together with its truth table. One can easily see that the simulated DFF output responses show a similar electrical behavior for the whole temperature range. The Mater-Slave DFF is made up of 8-NANDs and 3-Inverters 4H-SiC logic gates, with a total of 30 MESFETs devices and 33 epitaxial resistors, hence summing an amount of 63 4H-SiC devices in total. The simulation test schematics of the DFF can be found in Annex.C.

5.3.2.4 The D-Reset Flip-Flop

The D-Reset Flip-Flop is the second most complex digital block implemented on 4H-SiC. It is designed using three SR-Latches, each one made of two 4H-SiC MESFET - NAND gates with three inputs (Fig.5.24). The SR-Latch digital circuit is implemented using two elementary MESFET-NAND gates, similarly as for the CMOS topology. This latch can be considered one of the most basic asynchronous sequential logic circuits. Concerning its design complexity, it is the simplest ICs on SiC using MESFET logic gates. In general, latches are put together to form much more complex elements like flip-flops, as in this case.

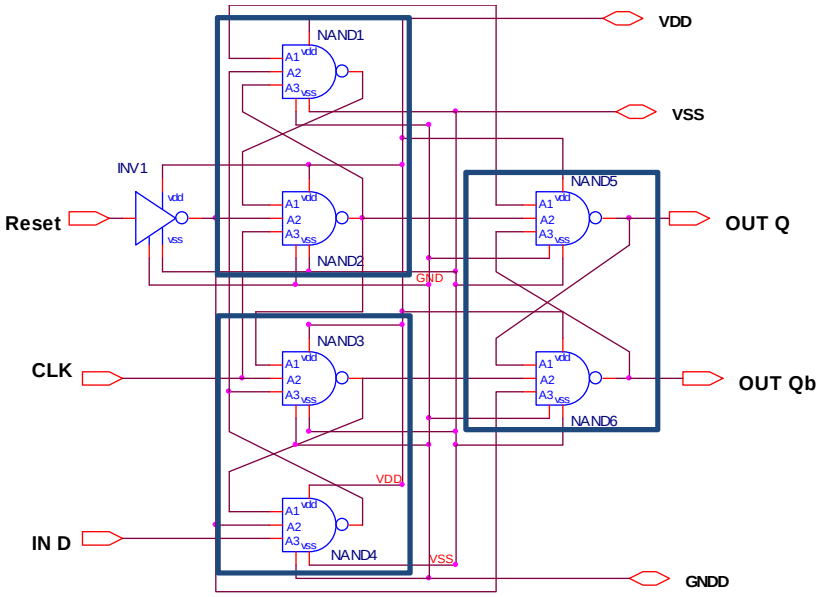
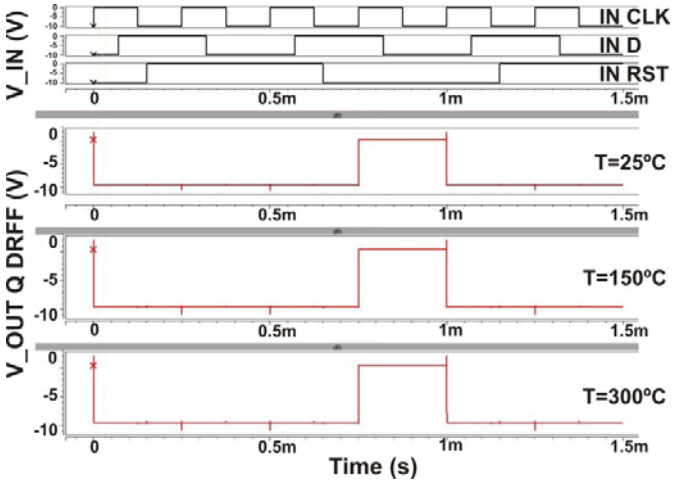


Fig.5.24. *Circuit configuration of the 4H-SiC MESFET D-Reset FF*

Fig.5.25a shows the simulated time diagrams of the D-Reset FF in the whole temperature range. One can observe that Data state is at the output only on positive Clock edge, and storing it when the Reset signal is at its Low level. The D-Reset FF shows a proper behavior for all simulated temperatures.



Clk	In D	RST	Q
0	0	1	×
1	0	1	×
0	1	0	0
1	1	0	1
0	0	0	1
1	0	0	0
0	1	1	×
1	1	1	×

(a) ***(b)***

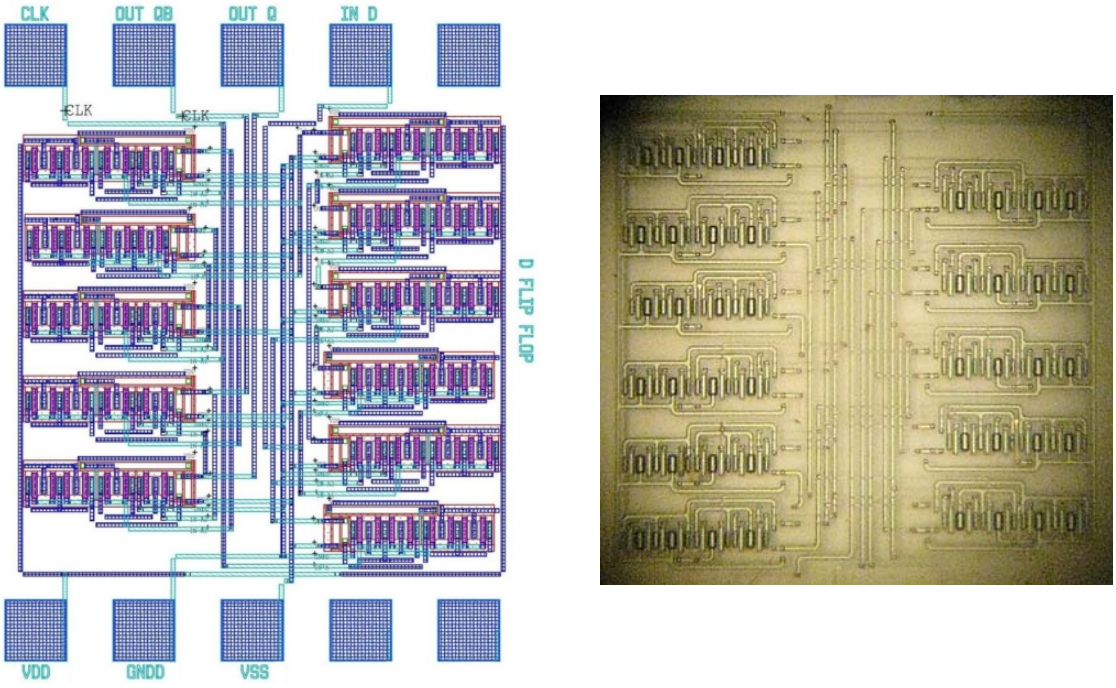
Fig.5.25. *D-Reset FF* ***(a)*** *Simulated diagram and* ***(b)*** *Truth table*

The D-Reset FF is made up of 6-NANDs with 3 inputs and 1-Inverter logic gates, with 20 transistors and 21 resistors, summing an overall of 41 4H-SiC devices. The test schematic used for the D-Reset FF simulation can be seen in Annex.C.

Concerning the simulations, we can state that the functionality of the previously multi-stage SiC circuits is ensured by the room and high temperature operation of the elementary logic gates they are made of.

5.3.3 Layout Design vs. Fabricated Circuits

In order to emphasize the complexity of the first fully integrated multi-stage complex digital blocks fabricated on 4H-SiC, Fig.5.26 shows the similarity between the layout design and the picture of the fabricated Master-Slave DFF.



(a) ***(b)***

Fig.5.26. *The similarity of the 4H-SiC Mater Slave Data Flip-Flop between the* ***(a)*** *circuit layout and* ***(b)*** *fabricated circuit*

This is the most complicated and largest ICs developed on 4H-SiC in the present work, which is made of 63 devices. One can easily observe the fabrication complexity of the ICs. The device scalability, wafer planarity and the novel implantation technique have brought a great improvement concerning device integration density, hence enabling the development of more complex ICs on SiC.

To our knowledge, up to now integrated circuits on SiC of such complexity and owing such a high integration density have not been designed before. The SiC ICs so far reported

were limited to the usage of a small number of devices and to a low device integration density.

The next section deals with the experimental results of these SiC ICs demonstrating the functionality of the complex circuits is ensured by the functionality of the elementary logic gates and limited by the defects of the SiC starting material.

5.4 Experimental Results of 4H-SiC MESFET Logic Gates and Multi-Stage Digital ICs

In the previous sections we first presented the design, modeling and simulations, of elementary logic gates able to operate in the 25ºC-300ºC temperature range. Furthermore, these logic gates were needed for developing multi-stage complex digital integrated circuits. We remind that the main devices used in these ICs developments are the 4H-SiC MESFET transistor (Chapter III) together with epitaxial resistors (Chapter IV). In order to demonstrate the functionality of the previously designed circuits, electrical characterizations of the fabricated ICs were performed. In this section, the experimental results are analyzed, presenting also the additional necessary steps for a proper electrical characterization of the circuits.

5.4.1 Input-Output Compatibility

An important aspect that needs to be considered in a first stage is the *Input-Output compatibility* between the external input signals and the fabricated SiC circuits. As MESFETs are normally-*on* devices, the SiC circuits need to be controlled with negative input logic levels. Therefore, the necessity of matching the input-output controlling signals comes along again. Generally, the incompatibility between input and output levels for logic families in a system gets solved with the use of *logic shifters*.

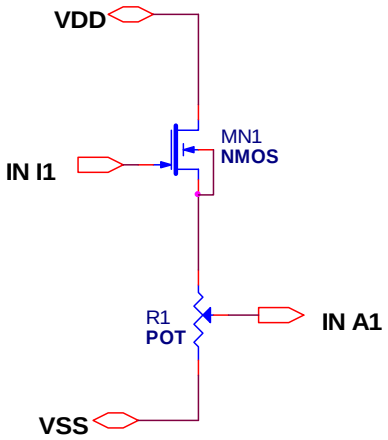


Fig.5.27. *The level shifter transforming the positive level signal IN I1 into negative level signal IN A1*

The increasing complexity of modern electronic systems made that most of the current digital circuits use consistent logic levels for all internal signals. We remind that a *logic shifter* is in fact connecting one digital circuit that uses a certain logic level to another digital circuit that uses another logic level. Therefore, an *external logic shifter* circuit has been built in order to match the input-output between the external signals necessary to supply the SiC logic circuits and the input logic levels. Fig.5.27 shows the general schematic for one of the levels shifters externally built for the SiC ICs characterization.

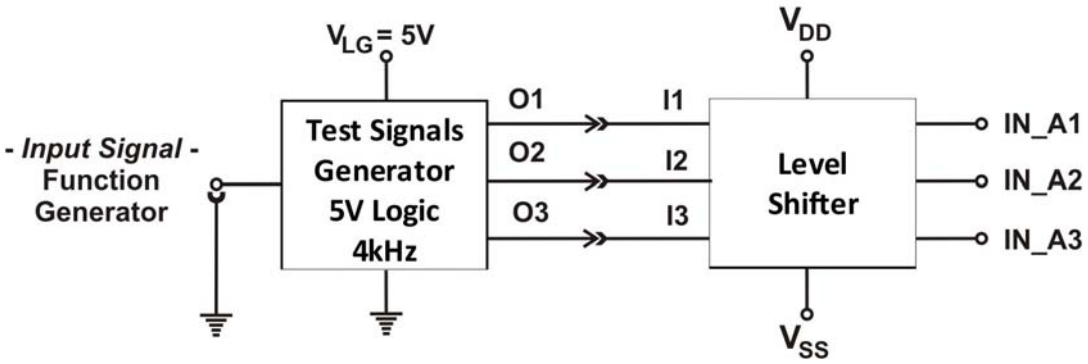


Fig.5.28. *External board circuit configuration of the Logic Test Interface*

Fig.5.28 shows the general schematic configuration of the external board circuit used as a *Logic Test Interface* for the future measurements. The input signals for biasing the SiC circuits are provided from a Function Generator. A Test Signal Generator 5V Logic digital block at 4 kHz is further used to generate three different delayed logic signals: O1 - 250µs, O2 - 500µs and O3 - 1000µs period, respectively. In order to provide the DC bias to the ICs on the SiC wafer, we have used the *DC coupling* (direct coupling) method [26] to interconnect the signals from the 5V Logic block to the SiC circuits.

The voltage level from the 5V Logic block is above ground potential. Therefore, three level shifter blocks (as shown in Fig.5.27) are used to shift the DC level at the output down to zero with respect to ground, thus releasing the IN_A1, IN_A2 and IN_A3 negative logic signals.

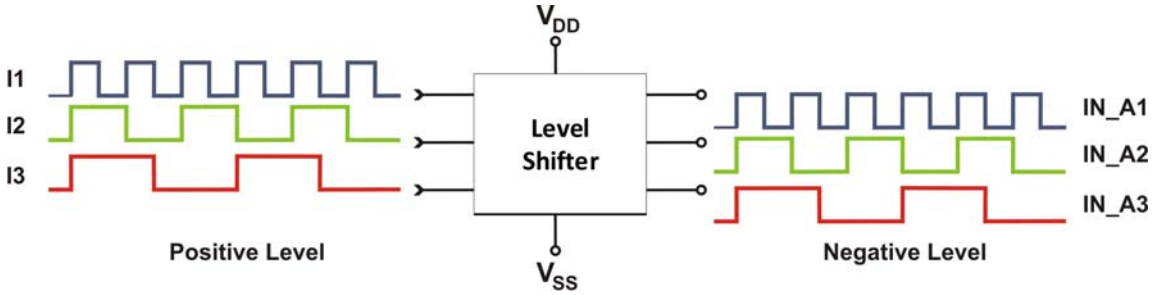


Fig.5.29. *Level shifting main operation*

The general operation of the level shifters is shown on Fig.5.29. One can easily see that each of them transforms the positive logic signals (I1, I2 and I2) into negative logic input levels (IN_A1, IN_A2 and IN_A3) suited to the input signals of our SiC digital circuits.

5.4.2 Packaging and High Temperature Setup

The wafer was diced (3700µm x 3700µm) as described in ***Annex.D*** *– Wafer-Dice - Circuits Configuration*, and then the dice encapsulated. For the packaging we have used a typical Dual In-Line case (DIL). DILs are commonly used in ICs industry, but also for device development and testing. The DIL has a ceramic housing with 40 leads of gold plated copper (leadframe) (Fig.5.30).

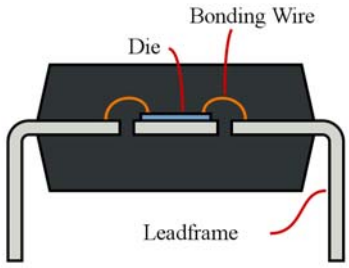


Fig.5.30. *Side view of a DIL case*

The back metallization of the dice is a thick Ti, Ni and Au metal stack. The die attachments have been realized with PbSnAg solder, alloy widely used for high temperature operation, of which the melting point is ~300ºC. A 75µm thick PbSnAg preform has been cut with the same die dimensions. The initial preform thickness gets thinner to around 50µm after the soldering process.

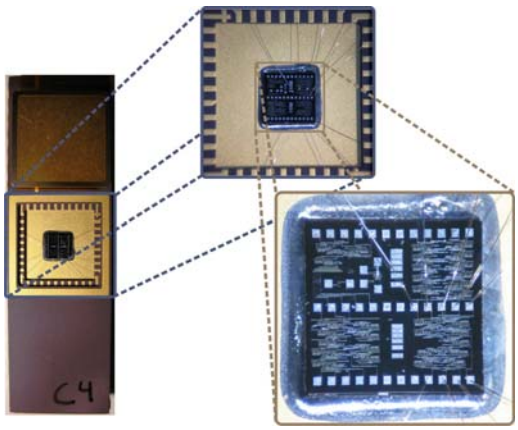


Fig.5.31. *DIL40 Case showing the SiC circuits bonding*

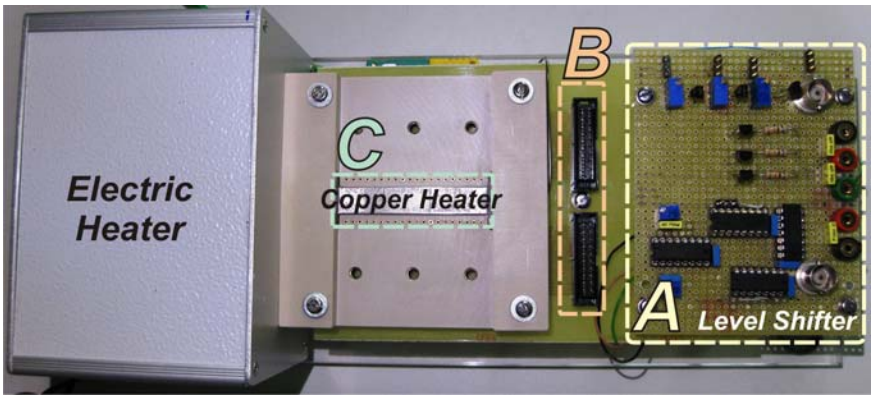


Fig.5.32. *High temperature setup specially made for DIL40 cases*

In order to perform accurate electrical measurements at high temperatures, a measurement setup has been built specially customized for the DIL40 case (Fig.5.32). It is made out of three main components. The first one (Fig.5.32–A) is the *Logic Test Interface* (Fig.5.28). The second one (Fig.5.32–B) is made out of two pin sockets; each one corresponds to the 40 leads of the DIL40 case. The last component (Fig.5.32–C) is the copper rail heater, which is directly connected to the electric heater (heater resistor), on which the DIL case (Fig.5.31) is placed for high temperature measurements. Furthermore, the electric instruments are connected to the Test Interface (right side–A) in order to supply the necessary voltages and the input signals to the SiC ICs.

5.4.3 Experimental Results on 4H-SiC MESFET Basic Logic Gates

Initially, the wafer is characterized at room temperature in order to have a general overview concerning the ICs functionality across the wafer. Then, measurements up to 300ºC and finally high frequency measurements are performed. The electrical measurements are carried out using three Keithley SMUs. Two SMUs are dedicated to supply the external level shifters from the Logic Interface and also to bias the SiC ICs. One SMU provides the 5V potential to the 5V Test Signal Generator Logic block. A Keithley Function Generator is necessary to generate the input signal of the Logic Interface. A Tektronix Oscilloscope is used for the visualization of the input/output waveforms of the SiC circuits. The voltage supplies used in the experimental measurements are tuned in order to set the proper High and Low levels to elementary gates, as will be further discussed.

5.4.3.1 Room and High Temperature Measurements

A. The Inverter Basic Gate

Fig.5.33 shows the Input and Output signals of the Inverter at room temperature. Initially, the voltage supplies used in the experimental measurements are ±25V. One can observe that the Input signal level is swept between 0V and -12.5V, ensuring the turn-off of the device. From the experimental Inverter waveforms, one can easily see that Output signal shows opposite logic levels with respect to the Input level, hence performing the proper Inverter operation at room temperature. It should be noticed that the Output response has amplitude of approximately 8V although the logic level has been negatively shifted at around -2.5V.

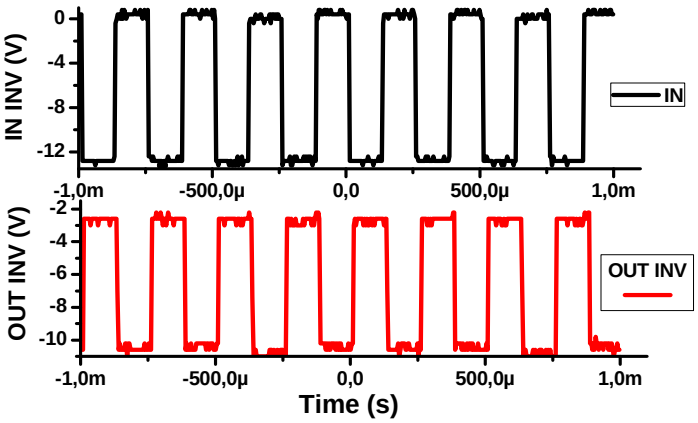


Fig.5.33. *The 4H-SiC Inverter's experimental waveforms at room temperature (V_{DD}=V_{SS}=±25V)*

In Chapter IV the experimental results of the fabricated epitaxial resistors were presented, showing that the 4H-SiC sheet resistance exhibits quite a double value than the theoretical one. Therefore, the -2.5V voltage shift that can be observed in the above output response diagram is due to an additional voltage drop on the follower transistor (Fig.5.9 – NFETSiC2), which is higher than the voltage drop initially considered in simulations. However, this voltage drift of the Output level can be easily manipulated by adjusting the voltage supplies (like V_{DD}=+25V and V_{SS}=-21.5V); thus, dragging the High level to 0V (Fig.5.34) and keeping the Output amplitude close to 8V. Although the resistors exhibit quite a double value, it is important to mention that the resistor divider ratio (Fig.5.9 – R_1 and R_2) is maintained to the same value since the individual resistors have the same increasing rate; hence, not affecting the Inverter output logic levels.

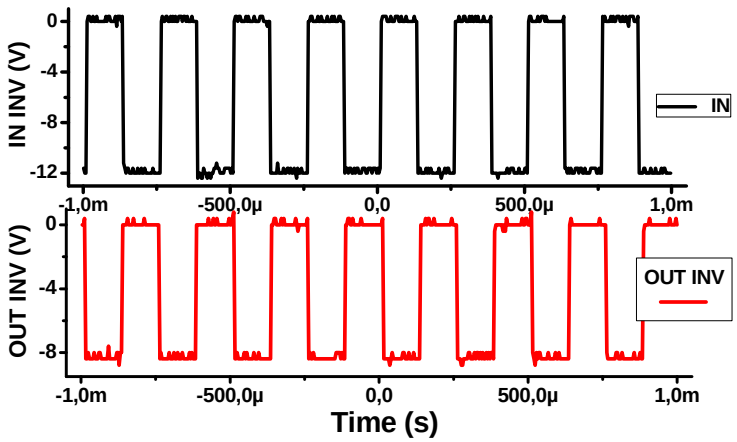


Fig.5.34. *The 4H-SiC Inverter's experimental waveforms at room temperature after the voltage tuning (V_{DD}=+25V; V_{SS}=-21.5V)*

Section 5.2.1.2 dealt with the logic gates simulation up to 300ºC. Therefore, Fig.5.35 shows the experimental waveforms of the Inverter up to 300ºC. The Output responses shows quite a similar behavior in the whole temperature range (25ºC-300ºC), performing its proper logic function.

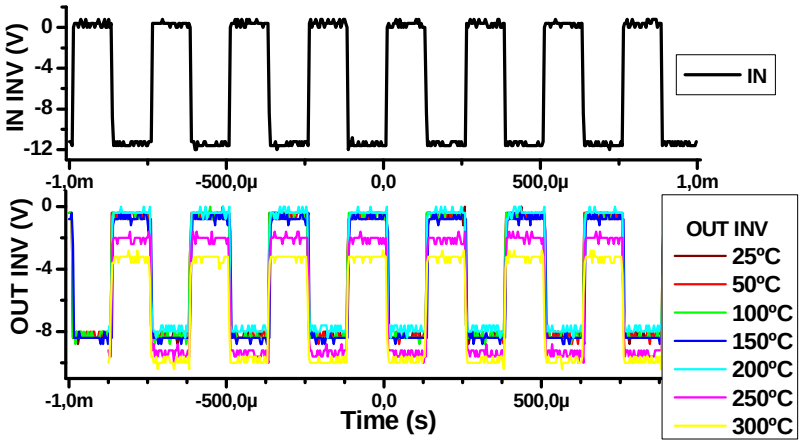


Fig.5.35. *The Inverter experimental waveforms vs. temperature (25ºC-300ºC)*

One can notice that up to 200ºC no voltage level changes of the Output waveform are observed with respect to the room temperature measurement. However, for the two highest temperatures (250ºC and 300ºC), the High and the Low levels negatively drift. This temperature evolution of the gates is mainly explained by the level shifter temperature behavior. The two-resistor divider show the same temperature coefficients, thus the voltage divider will maintain the same ratio in the whole temperature range, not affecting the Output response. Then, the observed changes are mainly caused by the follower transistor

temperature behavior. As the voltage follower transistor works in saturation, and because of the difference between the theoretical and experimental values of the epitaxial sheet resistance, the voltage drop across it significantly increases at high temperatures. The follower drain-gate leakage current also increases at high temperatures, adding a supplementary voltage drop, thus pushing down the Output logic levels of the gate.

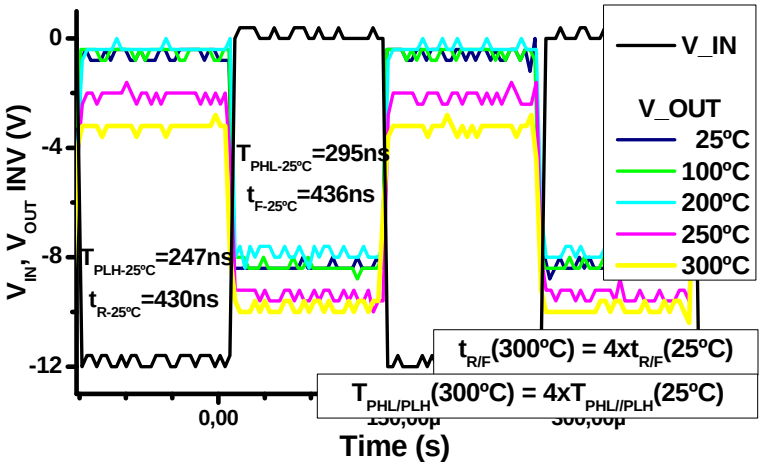


Fig.5.36. *The switching measurements of the Inverter in the 25ºC-300ºC temperature range*

The switching waveforms of the Inverter at room and high temperatures are shown in Fig.5.36. The Inverter Output signal exhibits quite a symmetric Low-to-High (T_{PHL}) and High-to-Low (T_{PLH}) propagation delay in the whole temperature range. The average propagation delay at 25ºC can be estimated around 270ns. The propagation delays together with the rise and fall times at 25ºC are shown in Fig.5.36. The difference between the experimental and the simulated values of these parameters is mainly caused due to the parasitic capacitances, linked to the measurement setup, which load the output of the Inverter gate. A new simulation was performed taking into account these external parasitic and oscilloscope input capacitances, which confirms the experimental results.

From the experimental switching waveforms at high temperatures we have observed that at 300ºC the Inverter Output signal exhibits approximately 4 times higher propagation delays (T_{PHL} and T_{PLH}).The rise and fall times (t_R and t_F), show quite symmetric values for the entire temperature range. The temperature evolution of these parameters is in a good agreement with the sheet resistance temperature behavior. In this sense, we have to comment that the experimental 4H-SiC epitaxial sheet resistance is approximately 4 times higher at 300ºC that at room temperature (see Table.4.3 and Fig.4.10), thus affecting the RC switching time constants (τ_i).

B. The Universal Gates: NAND and NOR

Section 5.2 reports the NAND and NOR circuits design, showing also their simulated waveforms together with their truth tables (Fig.5.12). From the experimental waveforms shown in Fig.5.37, one can observe that the NAND and the NOR basic logic gates properly perform their respective logic functions in the whole temperature range (25ºC-300ºC). In order to keep the proper High and Low levels, the circuits voltage supplies were the same as for the Inverter; i.e., V_{DD}=+25V and V_{SS}=-21.5V. The NAND and NOR Output amplitudes are close to 8V as well. However, by modifying the gates supply voltages, the Input and Output amplitudes can be easily adjusted.

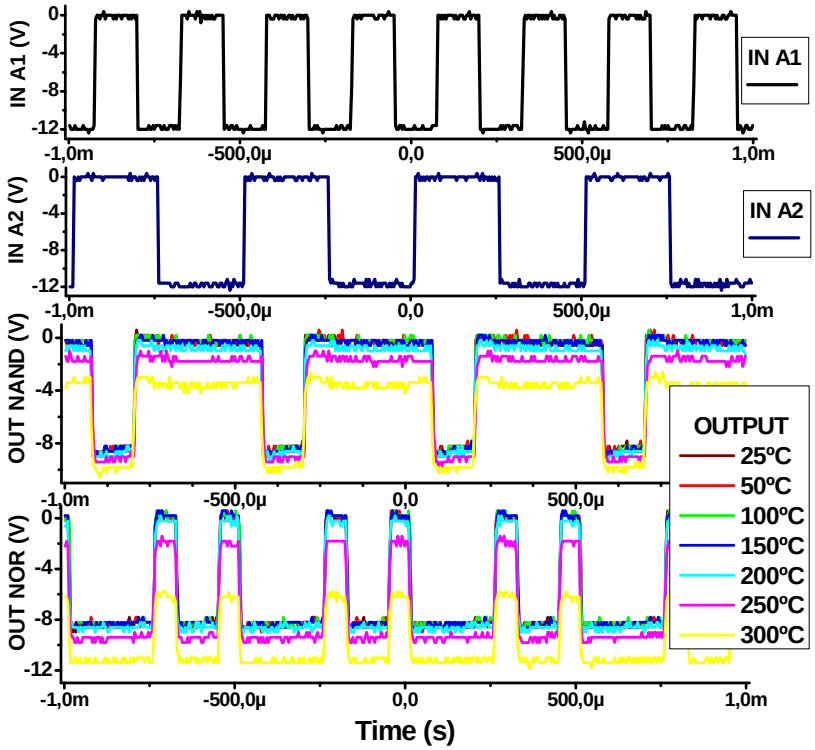


Fig.5.37. *The NAND and NOR experimental waveforms vs. temperature (25ºC-300ºC)*

The high temperature behavior of the universal logic gates shows similar evolution as the Inverter's (Fig.5.35). The difference between the experimental and simulated results is hence explained by the additional increasing potential across the MESFET follower at elevated temperatures. Nevertheless, the 4H-SiC MESFET logic gates output negative drift at higher temperatures can be minimized using a higher Schottky barrier for the MESFET gate contact. However, it is important to mention that the 4H-SiC MESFET logic gates exhibit their respective logic functions acceptably in the whole temperature range. Due to the imbedded high reverse leakage of the Schottky gate at high temperatures, we have limited the temperature measurements at 300ºC.

5.4.3.2 High Frequency Measurements

As our main interest is to confirm the functionality of the digital SiC ICs, the previous measurements were performed with a 4 kHz Input signal. Generally, low frequency and high frequency inverters perform the same function. In order to check the SiC MESFET logic family behavior in frequency, the Inverter's Output evolution up to 300 kHz was investigated.

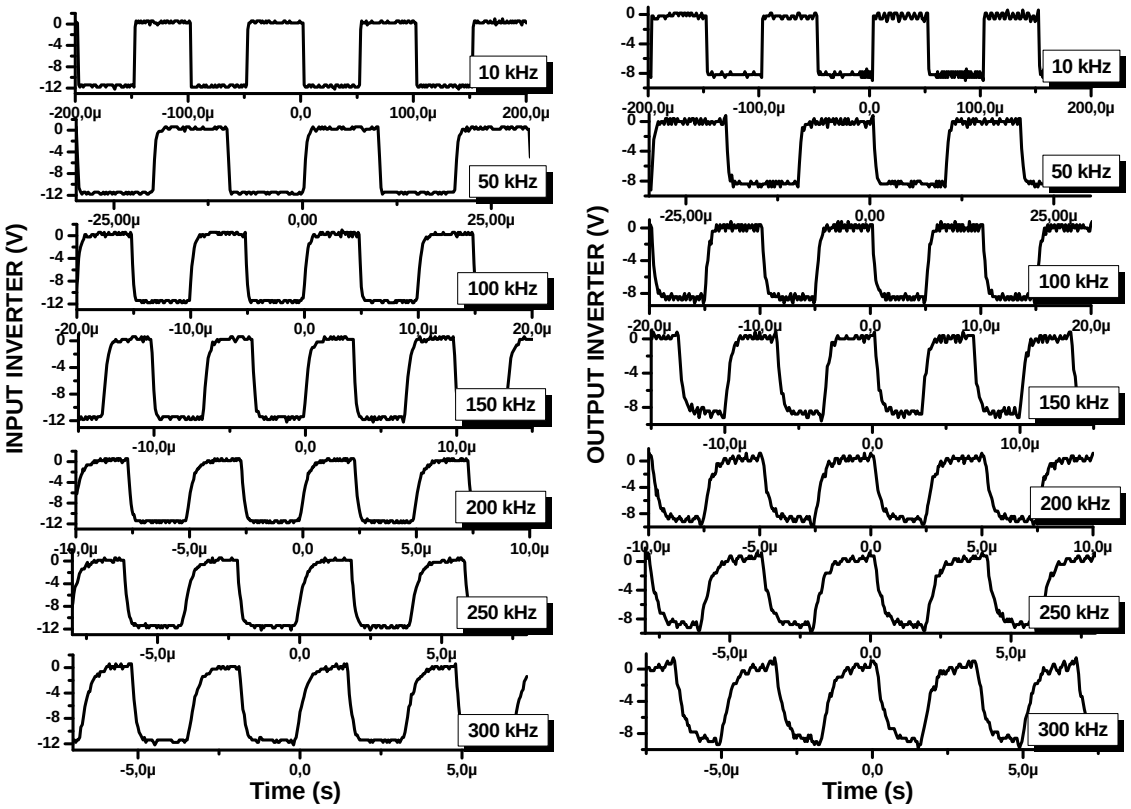


Fig.5.38. *The Input and Output Inverter experimental waveforms in the 10kHz - 300kHz frequency range*

These measurements were performed using the Test Interface circuit described previously. It should be mentioned that the Test Interface was initially built only for verifying the logic functions of the fabricated circuits, not being optimized for high frequency measurements. Therefore, the generated Input signals will deteriorate at high frequencies and will impact the output signal of the gates. However, our results still provide a good overview regarding the SiC circuit's performance in frequency.

Fig.5.38 shows the Output response of the circuit in relation to its Input signal. As one can observe the SiC ICs Inverter shows at its Output the inverted Input signal, showing a proper commutation from High-to-Low and from Low-to-High even at 300 kHz, although the Input signal gets deteriorated from 200 kHz. The additional noise observed on the Output responses is mainly caused by the parasitic environment. Anyway, the SiC Inverter performs the commutation properly even at high frequencies.

Depending on the final application, there are either low or high frequency commercial inverters. As the low frequency inverters have a larger surge capability, they are far better suited for applications which require high surge currents, such as motors, fridges, power tools, microwaves, pumps, etc.

5.4.4 Experimental Results on 4H-SiC Multi-Stage Digital Circuits

The DC electrical characterizations of the multi-stage digital ICs have been performed using the measurement setup as previously presented (Fig.5.32). We have limited the measurements up to 250ºC due to the solder alloy melting point (300ºC).

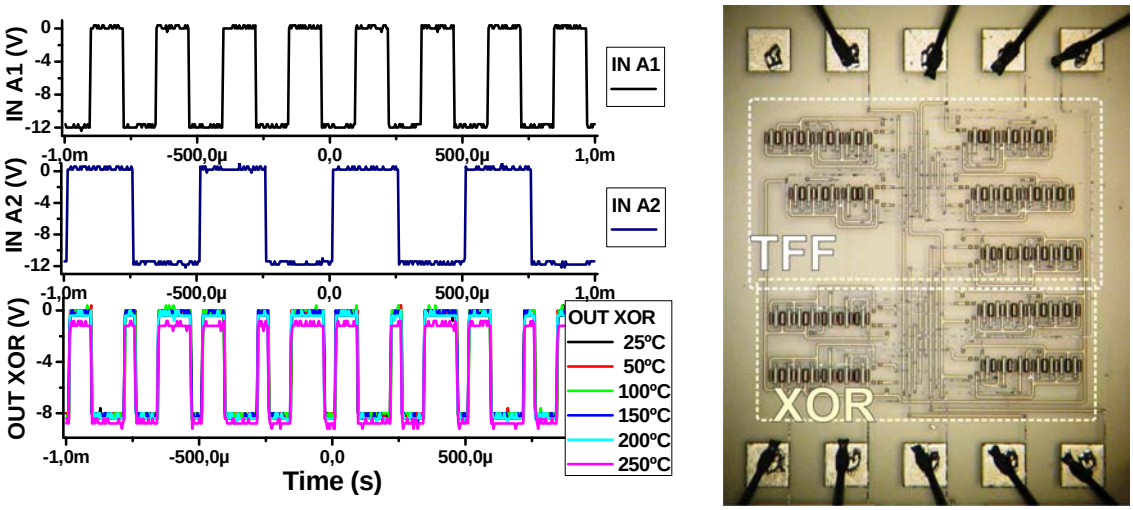
Previously we presented the design and modeling of complex digital ICs on SiC, demonstrating that, at simulation level, different digital topologies can be transferred to SiC, such as the CMOS standard topology for the Data and Data-Reset Flip-Flops (DFF and DRFF), as well as the NASA topology for Toggle Flip-Flop (TFF). Therefore, in order to demonstrate the functionality of the fabricated ICs, experimental characterization at room and high temperature, together with high frequency measurements are next presented.

5.4.4.1 Room and High Temperature Measurements

A. The XOR

The design and modeling of the XOR logic gate is made up of four digital gates: an Inverter, one NAND and two NOR gates. The supply voltages used for the electrical characterization were the same as for the basic logic gates characterization (V_{DD}=25V and V_{SS}=-21.5V). The Output amplitude is around 8V.

From the experimental waveforms of the XOR gate (Fig.5.39a), we can see that the Output is at High level whenever one of the Inputs is High, and is at Low level when both Inputs are Low.



(a) *(b)*

Fig.5.39. (a) *The XOR experimental waveforms vs. temperature (25ºC-250ºC) and* ***(b)*** *the XOR and TFF encapsulated die*

For the whole temperature range the complex SiC ICs perform their proper functionalities. However, at 250ºC the High and the Low levels start to negatively shift. A similar behavior has been observed for the elementary logic gates temperature evolution. Accordingly, the negative voltage drift of the logic levels is caused by the additional voltage drop on the follower transistor due to the gate-drain leakage current increment.

In order to show the fabrication complexity, Fig.5.39b shows the XOR and the TFF packaged circuits. From the comparison between the experimental and the simulated waveforms and its truth table (Fig.5.19), we can confirm that the SiC XOR logic gate properly performs its natural logic function.

B. The Toggle Flip-Flop

It was previously mentioned that the logic functions implementation at transistor level can bring important benefits, such as decreasing the circuit area, thus decreasing the risk of failure from the defects from the starting SiC material, and also increasing of the circuits speed operation. Therefore, the TFF digital block was realized at transistor level according to the NASA's topology [20].

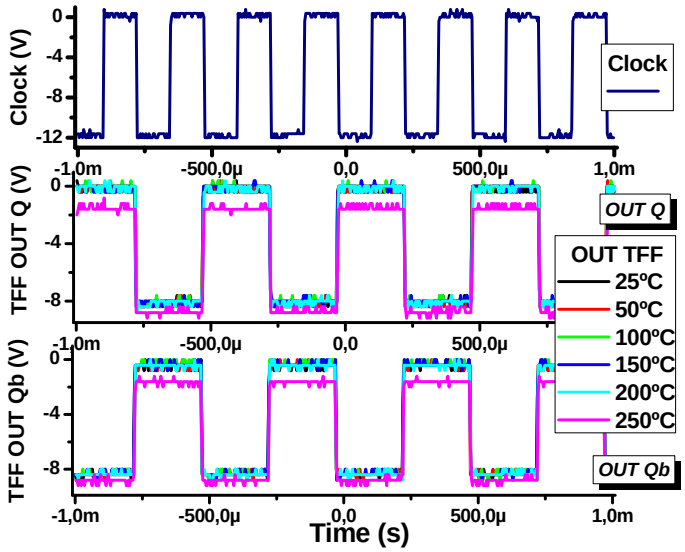


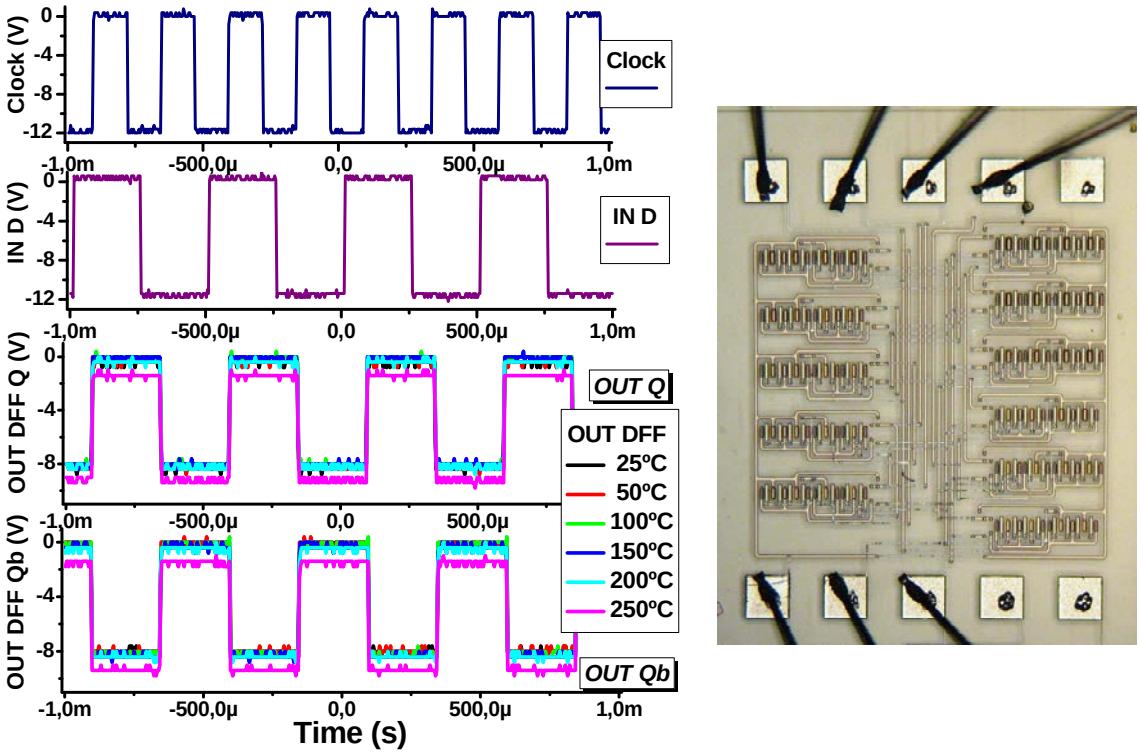
Fig.5.40. *The TFF experimental waveforms vs. temperature (25ºC-250ºC)*

Fig.5.40 shows the experimental TFF waveforms. It can be noticed that the Output *OUT Q* changes at each negative clock edge; hence, behaving as a frequency divider. The second Output *OUT Qb* performs the reverse function of the *OUT Q*. Comparing these experimental waveforms with the simulated ones (Fig.5.21a), we confirm that the fabricated SiC-TFF (Fig.5.39b) is properly exhibiting its digital logic function for the whole temperature range. The TFF temperature evolution is explained as for previously digital SiC ICs.

C. The Master Slave DFF

The most complex IC on 4H-SiC in the present work is the Master-Slave Data Flip-Flop (DFF), designed following the standard CMOS digital topology (Fig.5.22). It contains a total of 11 basic logic gates, with a total of 63 devices – 30 MESFETs and 33 epitaxial resistors (Fig.5.41b).

Fig.5.41a shows the measured Output signals of the Master D Flip-Flop and also the separately loaded Clock and In D Input signals. As one can see on the positive Clock edge of the logic level front, the Data input (*IN D*) is loaded and stored up till the next positive Clock edge, when the IN D logic level present in that moment is loaded. The loaded levels are transferred to the FF Output (*OUT Q*). The second Output *OUT Qb* is perfectly realizing the reverse function of *OUT Q* as expected. By comparing these waveforms with the simulated ones (Fig.5.23a) we confirm that the most complex digital circuit fabricated on SiC is successfully performing its appropriate logic function.

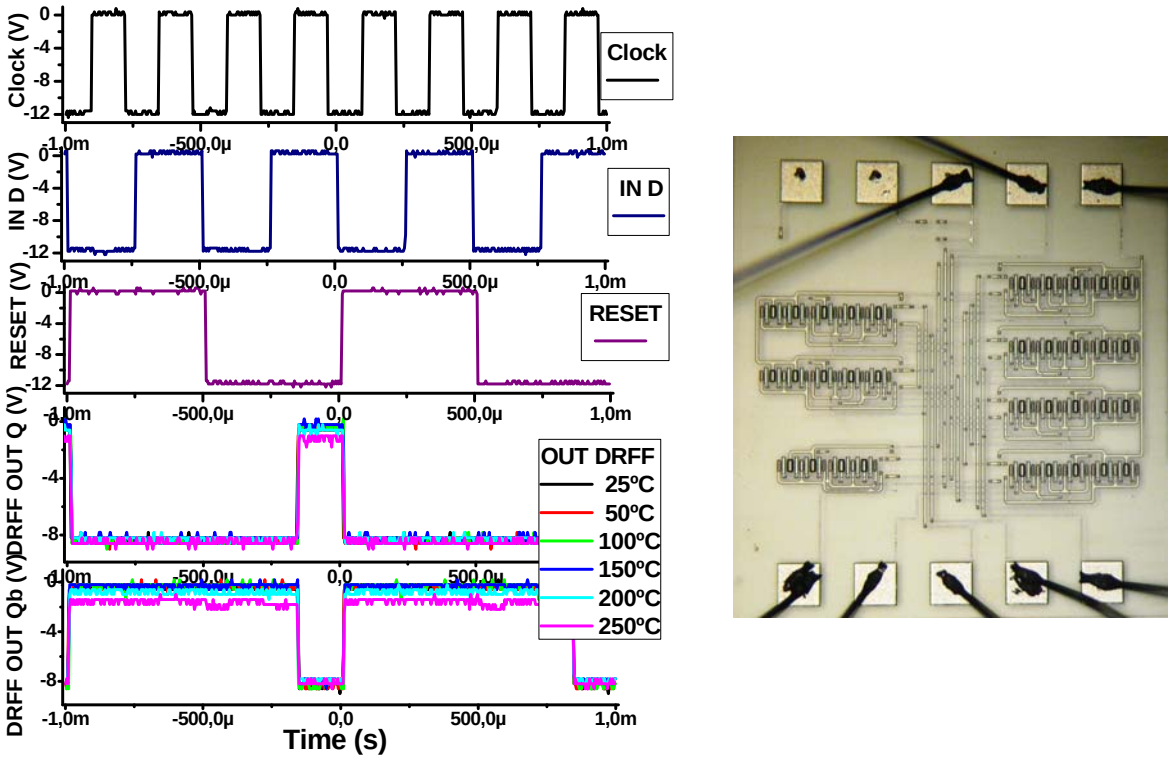


(a) *(b)*

Fig.5.41. *The DFF* ***(a)*** *experimental waveforms vs. temperature (25ºC-250ºC) and* ***(b)*** *the encapsulated die*

D. The D-Reset FF

D-Reset Flip-Flop (D-Reset FF) is the last digital block built by embracing the CMOS standard topology (Fig.5.24). This digital building block is the second largest ICs implemented on SiC containing a total of 7 logic gates. From the DRFF experimental waveforms (Fig.5.42a) we can see that Output signal is transferring the input Data signal only at the High Clock front when the Reset signal is at the negative (Low) level. The experimental waveforms are in good agreement with the simulated ones (Fig.5.25a); hence, confirming the DRFF appropriate operation. Fig.5.42b shows a photo of the encapsulated circuit.



(a) *(b)*

Fig.5.42. *The DRFF* ***(a)*** *experimental waveforms vs. temperature (25ºC-250ºC) and* ***(b)*** *the encapsulated die*

In conclusion, from our experimental results it has been proven that the *multi-stage digital ICs fabricated with 4H-SiC MESFET logic gates* preform their proper logic functionality, operation that has been ensured by the functionality of the individual basic logic gates and limited by the defects density of the starting material or process technology. Concerning the Output responses in temperature, the complex SiC ICs also perform their proper functionalities for the whole temperature range. However, at 250ºC the High and the Low levels start to negatively shift. As already mentioned, this negative voltage drift of the logic levels is caused by the additional increasing voltage drop on the follower transistor due to the gate-drain leakage current increment at 250ºC.

5.4.4.2 High Frequency Measurements

The high frequency operation of the multi-stage digital circuits is ensured by the basic logic gates evolution in frequency. Fig.5.43 and Fig.5.44 show the Toggle and Data Flip-Flop frequency behavior in the 10-300 kHz range. Similarly to the Inverter evolution (Fig.5.38), the TFF and DFF Output responses show a similar behavior with respect to their Inputs for the whole frequency range. One can observe that both flip-flops perform their correspondent natural logic function. The Output waveforms for the two FFs show a similar shape as of the Input waveforms, exhibiting a proper commutation from High-to-Low and Low-to-High, respectively, in the whole frequency range.

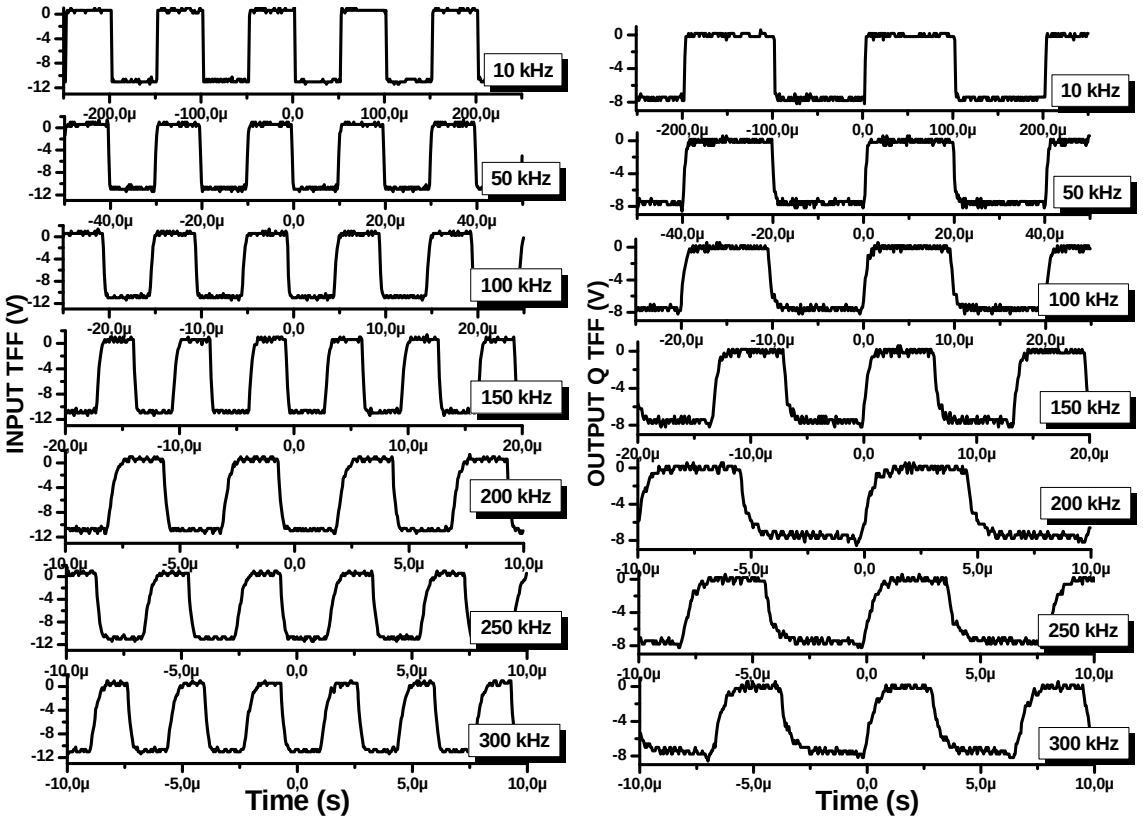


Fig.5.43. *The Toggle FF – Input and Q Output experimental waveforms in the 10kHz - 300kHz frequency rage*

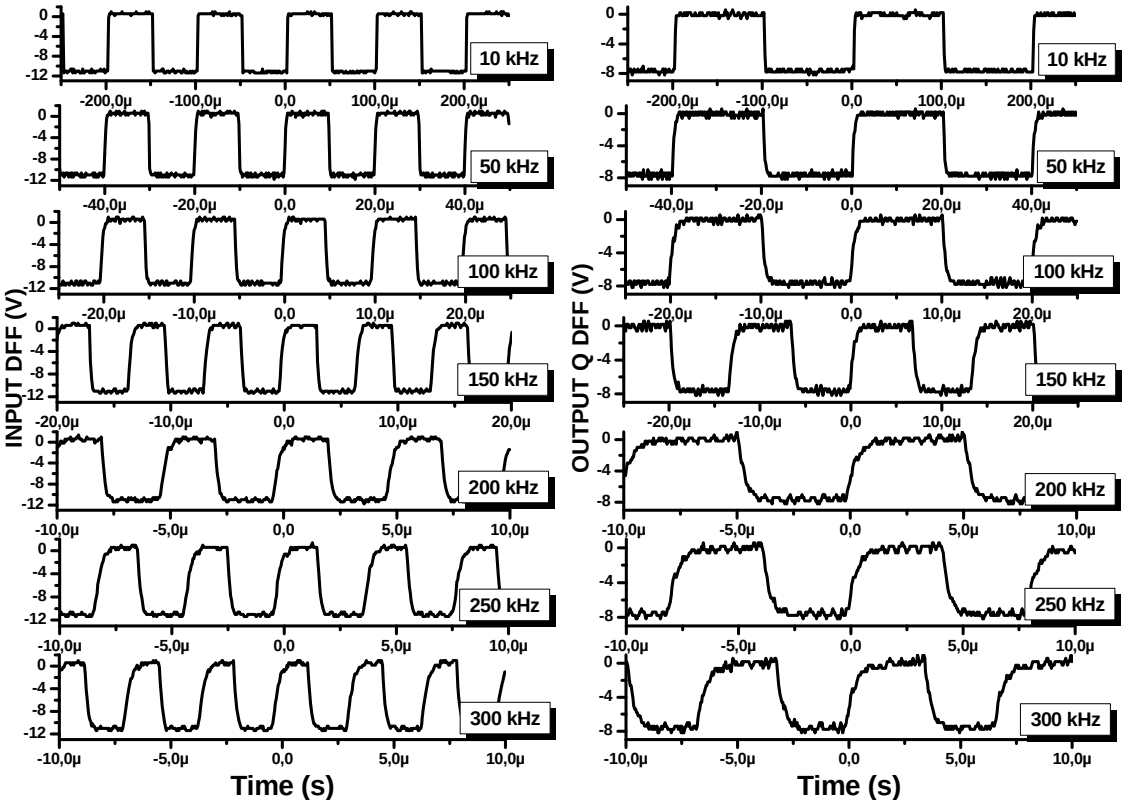


Fig.5.44. *The Data FF – Input and Q Output experimental waveforms in the 10kHz - 300kHz frequency rage*

The frequency measurement of the Data FF was performed by connecting the input signal IN D to the negative output Qb; hence, having the binary counter configuration.

In conclusion, it is demonstrated that the complex ICs on SiC are able to operate at high frequency. For a better Output response a new Test Interface circuit has to be built in order to have more accurate and not-deteriorated Input signals at higher frequencies.

5.4.5 Externally Wired 4H-SiC Circuits

Furthermore, in order to demonstrate that these SiC circuits are the basis for other digital functions, additional experimental measurements have been carried out by externally wiring different circuits; hence, creating new logic functions.

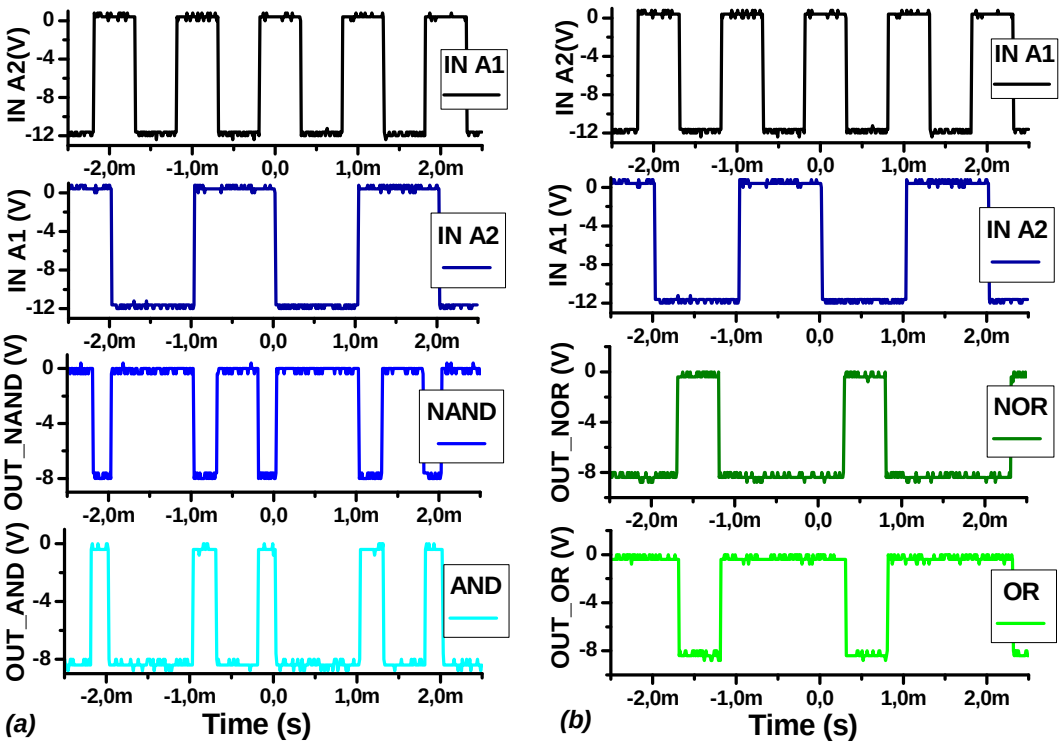


Fig.5.45. *Experimental integrated NAND, NOR and AND, OR waveforms*

Connecting a NAND or a NOR gates in series with an Inverter, we obtain some of the easiest basic logic gates;i.e., an ***AND*** gate and an ***OR*** gate, respectively. Fig.5.45 shows the experimental results using these external connections. This approach can be easily extended to various numbers of logic gates or complex multi-stage digital blocks, connected and/or in series and/or parallel.

5.5 Conclusions

The first section of this chapter is aimed at a brief introduction of the basics of digital circuits, presenting a general classification of ICs technologies and pointing out the lack of logic families on other semiconductor than Si, such as SiC. In order to understand the main operation of all digital designs, the most common element that stays at as the nucleus of every digital building block, the Inverter, has been presented and analyzed.

Having as our main device the SiC MESFET, two of the most representative GaAs logic families have been commented, showing the possibility of creating elementary logic gates using only normally-*on* MESFETs together with Schottky diodes. Furthermore, we presented the only existing logic family topology on SiC recently developed by NASA. This topology was specially designed for depletion mode 6H-SiC JFETs and epitaxial resistors. However, this topology was demonstrated for only a small number of components; therefore, for simple and small digital circuits. As our main active device is also a depletion mode transistor (4H-SiC N-channel MESFET), this topology approach is our choice for the digital SiC ICs developments.

Next, the design and modeling of elementary 4H-SiC logic gates library implemented with normally-*on* 4H-SiC MESFETs and epitaxial resistors is described. The main operation of the elementary logic gate – the Inverter, is presented emphasizing that the MESFET device from the logic selection level is the one that provides the behavior of the entire circuit. The necessity of using a load resistor and a level shifter due to the negative voltage control of the devices has been also highlighted. The NAND and NOR logic gates are also tackled. They were realized by replacing the device from the logic selection level with a string of two or more devices in series and in parallel, respectively, hence enabling the integration of other logic gates and even different logic functions.

From the circuits simulation we have observed that the output response of all elementary logic gates are quite similar for the whole temperature range, being limited at 300ºC due to the increase of the reverse leakage current of the Schottky gate electrode. The very slight changes were mainly caused by follower transistor operation in temperature.

From the Inverter performance analysis, we showed that the circuit noise margins show quite a small variation in temperature, thus, ensuring the robustness of the circuit. From the propagation time delay, it has been observed that 4H-SiC MESFET logic family presents a good switching speed for the entire temperature range. The power dissipation was

significantly reduced with temperature due to the currents increment with temperature. The Inverter's power loss was also increased due to the positive temperature coefficient of the resistors and of the follower transistor.

Furthermore, after presenting some of the most common dynamic building blocks, the design and simulation of the XOR, Toggle FF, Master-Slave DFF and D-Reset FF are carried out. At simulation level we have demonstrated that it is possible to successfully transfer some of the most common CMOS standard topologies on SiC technology. The Master-Slave DFF and the D-Reset CMOS digital building blocks are made using elementary logic gates with normally-*on* MESFETs and epitaxial resistors. We have also demonstrated that other types of topologies, like the one developed by NASA for XOR and Toggle FF using normally-*on* JFETs, can be also transferred and realized with MESFETs technology. It has been also proven that using the INV, NAND and NOR basic logic gates one can implement different logic functions; thus, showing that complex multi-stage digital ICs design with a large number of devices is possible on 4H-SiC using normally-*on* MESFETs logic gates. The logic building blocks shown on Fig.5.18, Fig.5.20, Fig.5.22 and Fig.5.24 can be further used for other logic application, for the implementation of memories, frequency dividers, counters, and latches among others. It has been also shown that the designed multi-stage digital blocks are able to operate at high temperature. The operation of these complex circuits is ensured by the high temperature functionality of the elementary logic gates they are made of.

In the characterization section, we have experimentally demonstrated the functionality of the 4H-SiC MESFET elementary logic gates library: Inverter, NAND and NOR gates. Due of the difference between the designed and experimental epitaxial resistors, at room temperature, the High and Low logic levels of the gates show a negative voltage shift mainly caused by the voltage follower transistor. This drop is easily eliminated by adjusting properly the circuits supply voltages. The gates functionality is also demonstrated up to 300ºC. It has been observed that for temperatures higher than 200ºC the gate-drain leakage current of the follower considerably increases; hence, affecting the Output response of the gates by drifting negatively their logic levels. However, this drift can be reduced for a better high temperature operation by using a different metal for the MESFET gate contact. From the characterization at frequencies up to 300 kHz, we have seen that the Inverter's output is fairly reproducing the reversed Input slopes, performing a proper commutation on each High-to-Low and Low-to-High front.

We have experimentally demonstrated that the standard CMOS topologies can be transferred to the Data and Data-Reset Flip-Flops and the NASA topology to the Toggle

Flip-Flop based on 4H-SiC MESFET basic logic gates. The multi-stage SiC ICs show a similar behavior at room and high temperature, and high frequency as the basic logic gates. We have also proved that the functionality of multi-stage ICs on SiC is provided by the elementary logic gates library operation. Moreover, we have shown that other logic function can be obtained with the fabricated circuits by connecting them externally.

From the complete on wafer characterization at room temperature, we have also observed that the circuit's functionality percentage decreases in relation with their areas. However, some important factors need to be pointed out:

i) This is the first attempt of using P^{+-}implant isolation technique for device and SiC circuits' fabrication;

ii) Three metal levels have been used in the circuits manufacturing, two of them dedicated to the interconnection levels;

iii) The SiC fabrication processes have to be established in order to fully control it without affecting the device/circuits functionality.

iv) There is also a starting material quality issue since the circuit area increases; the failure risk of the circuits due to the defects density of the starting SiC, eventually leads to the circuits non-functionality.

We consider that the current ICs fabrication and operation has been a successfully demonstrated. Hence, the ICs fabrication on SiC containing a large device number with a high integration density has been proven.

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CHAPTER VI

Radiation Impact on 4H-SiC Schottky-Gate Devices

Currently there is a great interest and a high demand for radiation-hard electronic components due to the large variety of terrestrial and spatial applications. Thanks to its material properties and also to its large extend of study and development, SiC has become a viable solution for harsh environment applications as well.

Because of radiation exposure, electronic devices can suffer changes in the electric parameters and/or crystal damage in the semiconductor, depending on the irradiation type, generally leading to the device electric performance alteration, or even to its irreversible failure.

Therefore, in order to demonstrate that the present investigated ICs devices are radiation resistant, in this chapter we present the ***experimental results on Schottky-gate based devices, such as encapsulated Schottky diodes and mesa-MESFET transistors*** (Chapter II), after high energy proton and electron irradiation. As the developed SiC circuits in the present work are based on Schottky-gate structures, we will assume this study as an input statement concerning MESFETs' ICs functionality in radiation rich environments.

6.1 Radiation Environments

The form that radiation interacts with material depends on the type, energy, mass and charge of the incident particle and target material. In general, there are two groups of radiation particles: charged and neutral particles. The charged particles are mainly protons, electrons and heavy ions; while the neutral particles are neutrons and photons. The manner that these particles react on the targeted material or electronic components is completely different. The effects that both charged and neutral particles have on the targeted matter are either related to ionization effects or to nuclear displacement. The neutrons, which are massive neutral particles, produce mainly nuclear displacements, whereas protons and electrons are responsible for ionization effects.

Typically, the radiation environments are characterized by its own spectrum of particles and energy distribution. It can be classified as [1]:

- Space
- High-energy physics experiments
- Nuclear
- Natural environments
- Processing-induced radiation

Table.6.1. *Earth's Space radiation environment summary*

Environment	Composition	Energy
Inner Van-Allen Belt	Protons (99%) Electrons Oxygen	10-50 MeV 1-100 keV
Outer Van-Allen Belt	Protons Electrons (99%) Alpha-Particles Oxygen	1MeV
Solar Cosmic Ray	Protons (96%) Alpha-Particles Heavy Ions	$10\text{-}10^3$ keV
Galactic Cosmic Rays	Protons (85%) Alp-Particles (145) Heavy Ions	10^5 MeV

Between the main sources of energetic particles in a space environment, protons and electrons trapped in the Van Allen belts are more usual [2]. The device radiation hardness for these two particles has received a great interest in investigation especially for space applications. Outside the Earth's atmosphere the intensity of the cosmic rays is much larger and consists in a large percentage of protons [3] (Table.6.1). Therefore, the radiation effects need to be considered in the design of electronics dedicated to space applications.

Due to our interest in developing devices for space applications, several radiation experimental tests have been carried out on 4H-SiC Schottky diodes and MESFET devices in the framework of this dissertation. The irradiations have been performed at different fluences/doses and energies with charged particles (proton and electron particles).

6.2 Radiation Effects in Microelectronics

The effects of radiation exposure play an important role in limiting the lifetime and reliability of microelectronic devices or circuits; hence, leading to the device/circuit failure. In general, the radiation effects in electronic components can be classified as [4]:

- Cumulative effects – that are the results of the accumulation of radiation energy in the electronic structures and especially in the isolation layers such as SiO_2;
- Single Event Effects (SSE) – they result from a single energetic particle interaction with the device.

The common materials used in semiconductor device fabrication are the dielectrics/insulators, various metallization layers, the semiconductor material and the packaging materials. Although insulators are those that generate most of the defects in electronic devices [5], the influence of radiation on insulating and conductive parts of the device is very different.

The most sensitive devices to ionization are the MOS transistors due to the Silicon Dioxide (SiO_2) sensitivity to ionizing radiation [6], typically creating holes-electrons pairs. After the electron-hole pair generation, a fraction of them will immediately recombine, whereas the rest can be displaced by a local electric field. Then, the holes can be trapped in the oxide or migrate to SiO_2 interface where they occupy undesired interface states, while the electrons drift to the gate. Both trapped holes and accumulated interface states affect the semiconductor's characteristics. Moreover, these can lead to malfunctioning of electronic devices and eventually of the circuits and applications in which they are implemented.

6.3 Radiation Hardness of SiC-Based Electronic Devices

As mentioned in Chapter I, up to date almost all kind of power devices have been developed on SiC. Although several companies (such as Cree, Infineon, RHOM, Microsemi, Semisouth, ST Miroelectronics, etc) are currently commercializing SiC devices (such as SiC rectifiers, MESFETs, JFETs and since 2012 power MOSFETs by Cree), the most mature commercial SiC devices so far are the power Schottky diodes and the vertical power JFETs [7]. Due to the excellent radiation hardness of SiC material [8], several studies have been lately performed on many of the developed SiC devices.

Radiation investigations such as irradiation with neutrons, protons, electrons, light ions, gamma and x-ray at different energies and fluences have been performed on MESFETs [9-14]. Additionally, studies on MESFETs have been carried out based on energetic electron irradiation [15] and high dose irradiation of gamma rays [16]. Concerning SiC Schottky diodes there is a large number of references in recent literature on proton, neutron, heavy ions and gamma irradiations [17, 18]. The general conclusion of these investigations is that these SiC-based devices show better radiation stability than the Si devices.

Recently, we have designed and fabricated 300V-5A 4H-SiC Schottky diodes for operating in the solar panel array for the Bepi-Colombo European Space Mission [19]. This mission is scheduled for 2015 and consists out two separate spacecraft's that will orbit around Mercury. The wide temperature range that the diodes are expected to work (from -170ºC up to +270ºC) and the radiation rich environment are significant aspects as the spacecraft will operate in the Inner Solar System. Therefore, [20] reports a first important study concerning radiation tests on the SiC diodes. Gamma rays irradiations with a dose up to 570 Krad and a rate of 3.6 Krad/hour were initially performed on the packed diodes. It has been shown that the effect of gamma rays on the SiC diodes is a reversible effect after quite a short time. Proton irradiations have been also carried out at 100MeV, 60MeV and 15MeV energy at same fluences ($1.6 \cdot 10^{11}$ p/cm^2). For the two highest energies no significant impact was detected on the forward characteristics, whereas for 15MeV a 2% increase of the forward voltage was observed. The slight increase of the barrier height was due to the Schottky interface modification. In the reverse mode, no significant modifications were noted. Also no SEE or catastrophic failures have been observed for these energies and fluences, hence concluding that the CNM high temperature SiC Schottky diodes present a high level of radiation hardness for high energy proton and gamma irradiation environments.

4H-SiC MOSFET devices have been recently designed and fabricated at CNM, and are in continuous development, progress and optimization [21]. So far not many studies have been either performed or published concerning SiC MOSFET ionization effects. Therefore, recently we have carried out a complex set of radiation experimental tests. Significant irradiation studies showing important and revolutionary results concerning device electrical behavior at high and low radiation energies have been published [22-24]. However, this topic is still at a very early stage; therefore, important results will be published in a near future.

6.4 Experimental Results on 4H-SiC Schottky-Based Devices

In our previous work [20] we reported that only for the lowest proton energy experiment (15MeV) slight Schottky interface modifications were observed. Therefore, in order to complete the previous study, complementary experimental studies were carried out on Tungsten-Schottky Diodes. Moreover, as in the present dissertation, the analyzed and developed devices are made with Tungsten-Schottky gate contacts, the mesa-MESFETs were irradiated with protons and electrons at different energies and fluences. We consider that this study can offer important information concerning Tungsten-Schottky contact radiation behavior, which can furthermore be extrapolated to the currently developed SiC planar-MESFETs and also to make initial hypothesis concerning SiC ICs response with radiation.

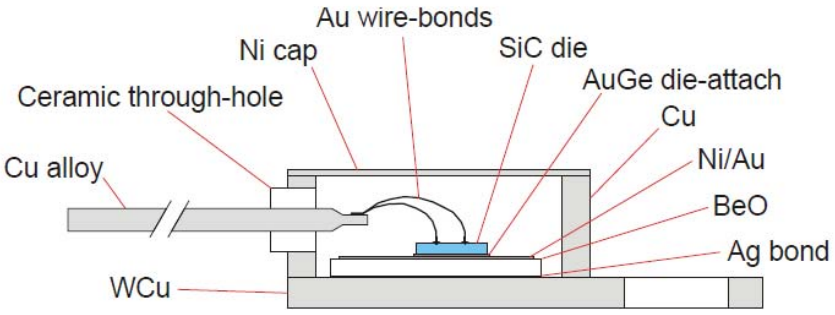


Fig.6.1. *Cross-section scheme of the packaged diodes showing the main parts*

The SiC Schottky diodes have been processed on 4H-SiC wafers supplied by CREE. The N-epilayer is 5μm thick and 10^{16} cm^{-3}doped. The processing steps are similar to those used for standard temperature range diodes [25]. The device package of these diodes was a

challenge as they supposed to endure high temperature operation. The schematic cross-section of the encapsulated diode shown in Fig.6.1 is a modified TO-257 metallic package from Kyocera. More details concerning device processing and packaging are described in [20, 25].

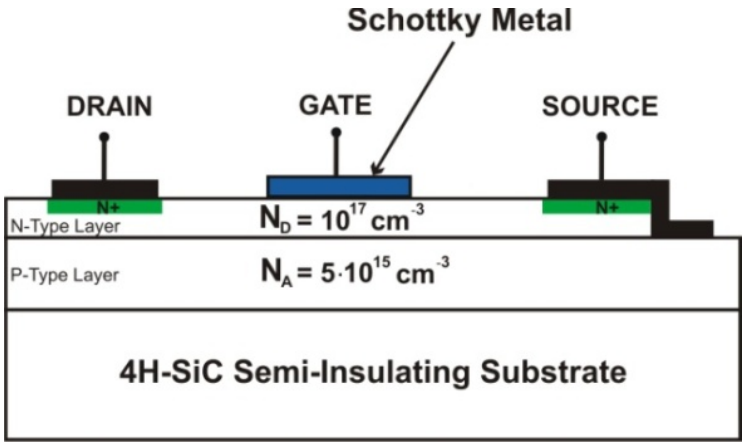


Fig.6.2. *Schematic cross-section of the 4H-SiC mesa-MESFET*

In Chapter II we show in detail the design and fabrication of the 4H-SiC mesa-MESFETs. These transistors have been fabricated as well on a 4H-SiC wafers supplied by CREE with a 5µm thick, $5 \cdot 10^{15} cm^{-3}$ doped P-epilayer grown on a semi-insulating substrate. The N-epilayer is 0.5µm thick with a doping concentration of $10^{17} cm^{-3}$ (Fig.6.2). These transistors have been used for the radiation experiments.

6.4.1 Proton Radiation

The proton irradiation experiments were carried out at HZDR – The Institute of Ion Beam Physics and Material Research using the 6MV Tandetron (High Voltage Engineering HVEE) with 10MeV ion energy at four different fluences: $5 \cdot 10^{11}\ p/cm^2$, $5 \cdot 10^{12} p/cm^2$, $5 \cdot 10^{13}\ p/cm^2$ and $5 \cdot 10^{14}\ p/cm^2$. After the irradiation, the devices were electrically characterized. Due to security reasons, two of the diodes submitted at the highest fluences ($5 \cdot 10^{13}\ p/cm^2$ and $5 \cdot 10^{14}\ p/cm^2$) have not been measured because the radiation activation limit of the cases was above the permitted level.

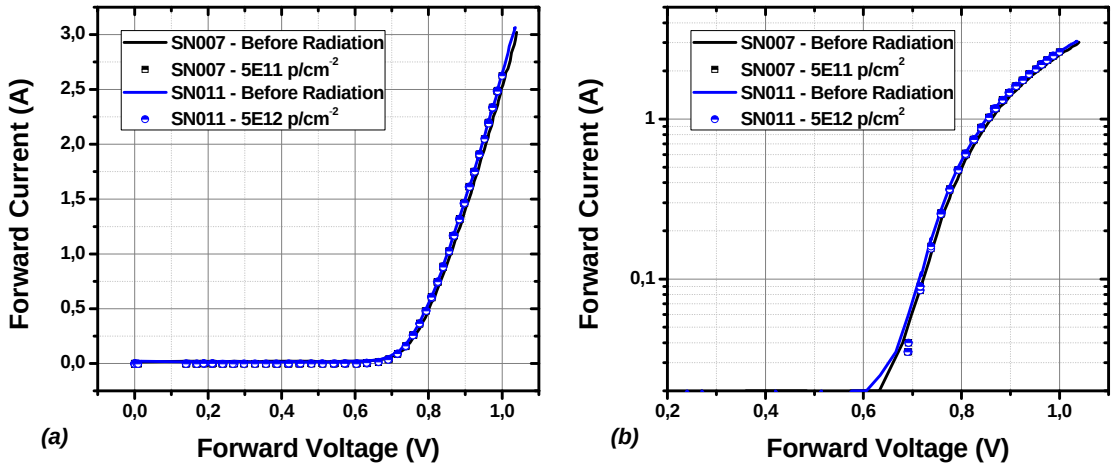


Fig.6.3. *Packaged 4H-SiC Schottky Diodes forward characteristics before/after proton irradiation in (a) linear and (b) logarithmic scale*

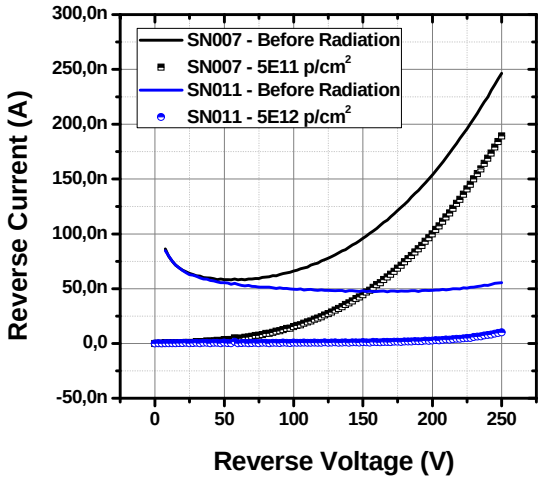


Fig.6.4. *Encapsulated 4H-SiC Schottky Diodes reverse characteristics before/after proton irradiation*

Fig.6.3 and Fig.6.4 show the forward and reverse characteristics of the diodes before (solid line) and after (symbols) irradiation. As one can see, in the forward mode no changes have been observed neither in the voltage or current evolution. From the reverse characteristics one can observe that the diodes reverse current decreases for both fluences. However, this decrease of the leakage current does not affect the device. On the contrary, it enhances the reverse mode device electric behavior. Comparing with the GaAs Schottky barrier evolution after irradiation [26], we may assume that the decrease of the reverse current can be attributed to the reduction of the net doping level. This behavior could be

explained as follows. The irradiation could produce donor compensation in the diode channel, which in turn reduces the tunneling contribution across the Schottky barrier, hence decreasing the tunneling current in the diode.

A first conclusion that can be drawn is that after 10MeV proton energy at $5 \cdot 10^{11}$ p/cm^2 and $5 \cdot 10^{12}$p/cm^2 fluence, the Schottky diodes show a stable and slightly improved electrical behavior. Together with the previous studies, we can now confirm that the SiC Schottky diodes are unaffected by high energy proton irradiation.

The mesa-MESFET devices were also irradiated at three different fluences, as shown in Fig.6.5. One can observe that the irradiation impact on these devices is more visible than in comparison with the Schottky diodes. The most notable effects are seen for the lowest irradiation fluence ($5 \cdot 10^{11}$ p/cm^2). We have observed that for this fluence, the pinch-off voltage of the device is slightly decreasing with 0.7V and the leakage current decreases with more than one order of magnitude. Also the maximum drain current is presenting a decrease with approximately 5mA with relation to the non-radiated device.

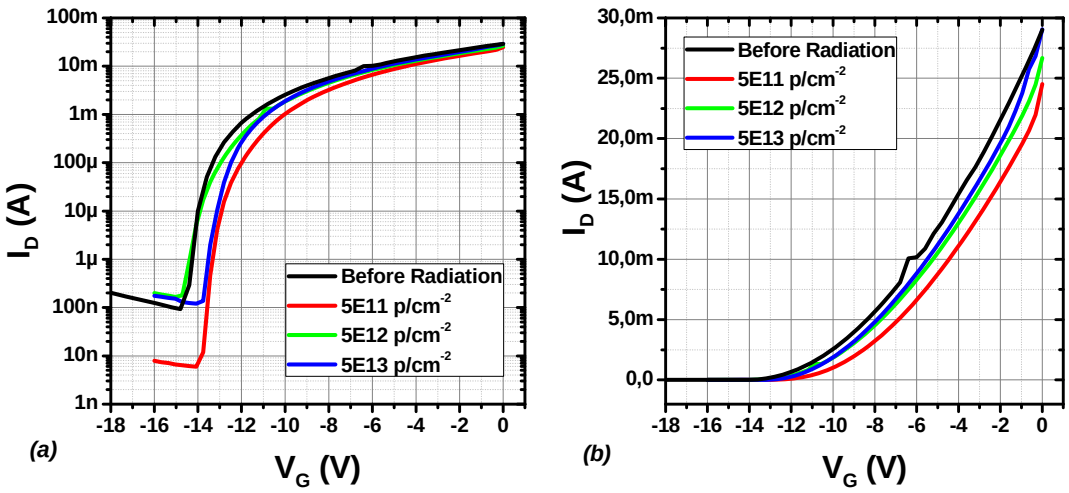
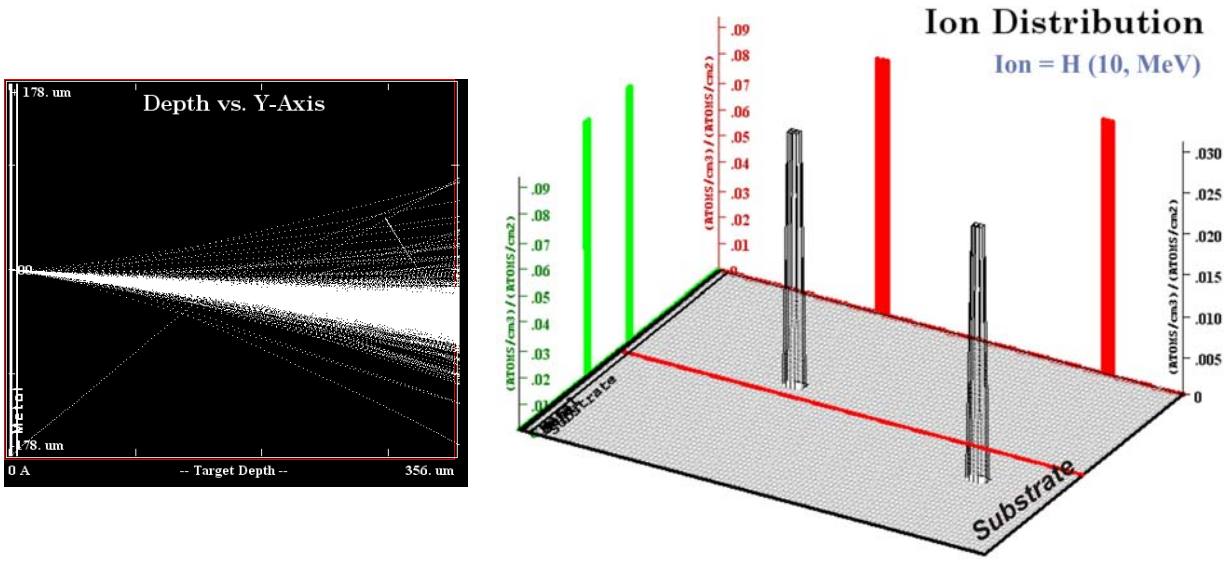


Fig.6.5. *The output characteristic of the 4H-SiC mesa-MESFETs irradiated with protons at 10MeV*

Increasing the fluence to $5 \cdot 10^{12}$ p/cm^2, the V_P shows no variation, having the nearly same value as before radiation; the subthreshold current shows a slight increment with relation to its initial value; and the maximum drain current shows a 3mA drop. For the highest fluence, V_P also decreases (around 1V); the subthreshold current is in the same range as for the previous fluence, being close to its initial value; and the maximum drain current experiments a 2mA reduction with respect to the non-radiated value. The decrease of the V_P can be mainly attributed to the radiation-induced decrease of the Schottky barrier

height at the gate contact, whereas the increase of the V_P is typically induced by the expansion of the depletion region [10]. The decrease of the drain current could be caused by the increase of the resistance in the bulk of the crystal [27]. However, some of these variations could be eventually caused by the lack of uniformity across the wafer introduced by the fabrication processes.

In order to have a better overview of the MESFET results, we have performed simulations with the SRIM simulator [28]. These simulations help us to forecast the protons track though the structure, and also different types of damages that can produced in the semiconductor devices. The 10MeV protons energy penetration depth in the SiC material is estimated to be around 483.11µm. The MESFET cross-section thickness, including all the metal layers, is approximately 356µm. The SRIM simulations predict that the 10MeV protons are completely cross the device (Fig.6.6a). From the SRIM simulation concerning the ion distribution in the devices after irradiation (Fig.6.6b), can be observed that even if the protons get completely through the device, several picks of damage are most likely to appear in the substrate; hence, affecting the device performances.



(a) ***(b)***

Fig.6.6. (a) *Protons trajectory and* ***(b)*** *ion distribution in the mesa-MESFET at 10MeV*

The radiation source dependence of the device performance degradation after proton irradiation can be mainly attributed to the difference of mass and the possibility of nuclear collision during the formation of SiC lattice damage [26]. However, although small changes have been observed on different parameters of the MESFET, we can still assume that these structures withstand important radiation levels.

Therefore, from both Schottky diodes and mesa-MESFETs experimental results, we can conclude that the Tungsten-Schottky junction shows a good endurance at high energy proton radiation; hence promoting these devices as suitable for harsh radiation environment applications.

6.4.2 Electron Radiation

The electron irradiation of the Schottky based devices was carried out at the HZDR – Rossendorf Electron Accelerator (ELBE Facility) at 15MeV energy, which provides a wide variety of doses. First, a total of 6 encapsulated Bepi-Schottky Diodes were irradiated with electrons at 15MeV with doses from 0.5kGy to 30kGy.

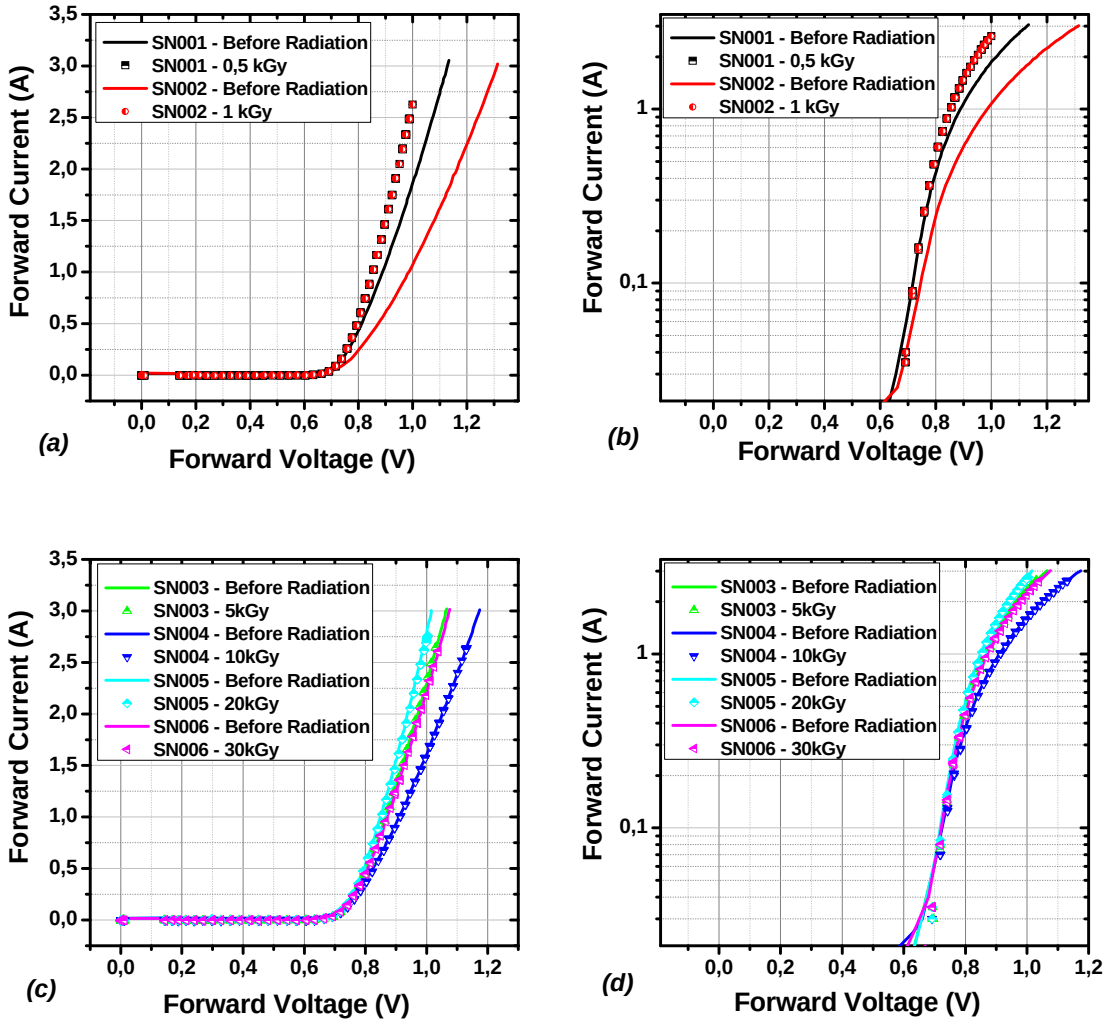


Fig.6.7. *Packaged Schottky Diodes irradiated with electrons – Forward Mode*

Fig.6.7 shows the forward characteristics of the Schottky diodes before and after irradiation. It can be observed that after irradiation, two out of the six diodes presented slight changes of their forward voltage. As one can see, changes in the forward mode have appeared only for the lowest doses: 0.5kGy and 1kGy (Fig.6.7a,b), whereas for the highest doses, the forward characteristic show no alteration (Fig.6.7c,d). However, the changes at 0.5kGy and 1kGy are in fact improving the forward voltage characteristic of the device with 0.06V and 0.218V respectively, measured at 2A.

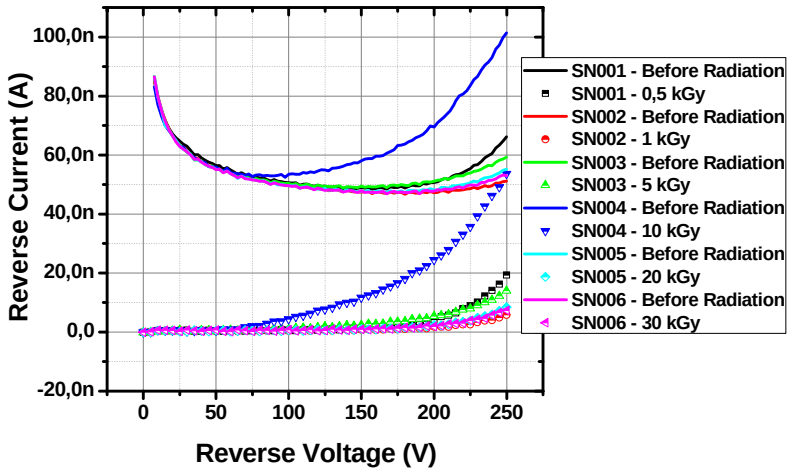


Fig.6.8. *Encapsulated Schottky Diodes irradiated with electrons – Reverse Mode*

From the reverse characteristics of the diodes (Fig.6.8) one can observe an improvement of the leakage current, decreasing for all doses. The reverse current is reduced by almost two orders of magnitude with respect to the non-irradiated case, showing a similar behavior as with the proton irradiation.

Therefore, we can assume that the Tungsten-SiC semiconductor interface improves after electron irradiation as well; hence, demonstrating that the Schottky diodes also show a good endurance in electron rich environments.

Two mesa-MESFETs were also submitted to electron irradiation at15MeV with doses of 5kGy and 10kGy. From the comparison between the before and after irradiation experimental results, no significant modifications have been observed for the main electrical parameters of the device. From Fig.6.9 one can see that no important changes have appeared in transconductance characteristic of the devices; hence, the Schottky gate being mainly unaffected by electron irradiation.

Therefore, we can now conclude that the mesa-MESFET transistor shows a good resistance against high energy electron radiation; hence, promoting these devices as suitable for high radiation environments, and even more for space applications.

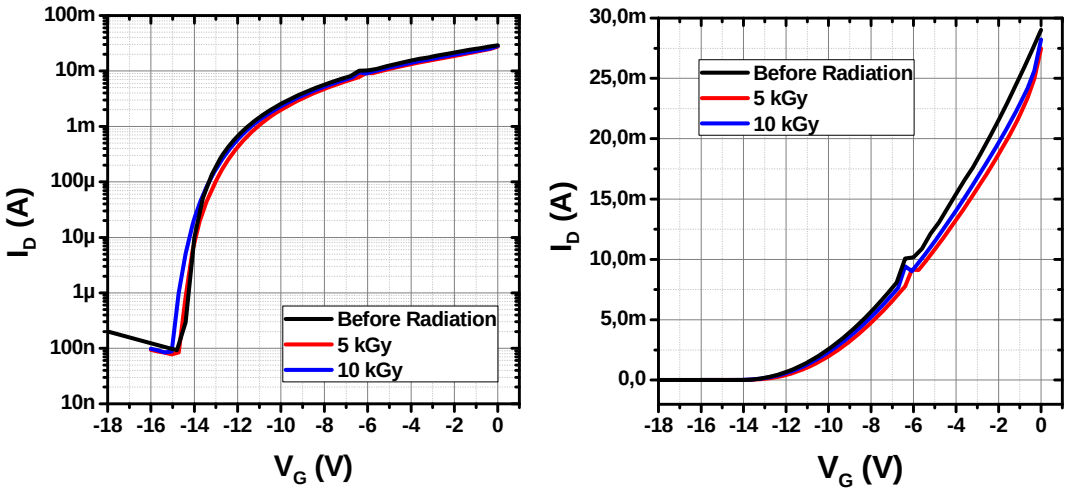


Fig.6.9. *The output characteristic of the mesa-MESFETs electron irradiated at 15MeV*

In conclusion, this Schottky interface (Tungsten-SiC) shows a positive behavior after high energy proton and electron irradiations for both Schottky diodes and mesa-MESFETs. Therefore, we expect that the new fabricated planar-MESFET together with the digital ICs block to show a similar behavior. However, as a part of the future work, a dedicated study concerning radiation hardness stability of the new structures (planar-MESFET and epitaxial resistors) together with the fabricated ICs is going to be performed.

6.5 Conclusions

Under different types of radiations, electronic semiconductor devices can be damaged, which can lead to different failures. As the main active device in the present work is the 4H-SiC MESFET device, we have focused our interest in analyzing the electrical behavior after high energy proton and electron irradiations of two Schottky-junction based devices: the Schottky diode and MESFET transistor.

It has been shown that after 10MeV proton irradiation, the packaged Schottky diodes show no changes on the forward current and voltage drop, whereas in the inverse mode an improvement of the SiC-Schottky interface has been observed, decreasing the reverse current and showing a stable reverse voltage. Although the protons completely cross the mesa-MESFET transistor at this energy, it appears the possibility of nuclear collision in the SiC lattice, thus creating crystal damage in the semiconductor by elastic scattering. Therefore, slight modifications have appeared in the electrical parameters of the mesa-MESFETs, but no critical SSE events have been noticed. However, these modifications did not lead to the irreversible device failure.

After 15MeV electron irradiation the Schottky diodes showed no failure in their electrical behavior. Moreover, in the forward mode at the lowest doses we observed an improvement of the forward voltage, while the reverse current experiments a decrease. Concerning the irradiated mesa-MESFETs no significant changes have been observed on any of the most relevant electrical parameters.

Therefore, the main conclusion of this chapter is that Schottky-junction devices show no variations on their electrical behaviors after proton and electron irradiations, proving their radiation hardness stability; hence, demonstrating that these components are perfectly suitable for harsh radiation applications.

Although a dedicated study will be performed in a near future, we are expecting that the new fabricated MESFET structures together with the multi-stage digital building blocks will show a similar behavior concerning radiation hardness.

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GENERAL CONCLUSIONS

This research work deals with 4H-SiC Integrated Circuits able to operate at high temperature, high frequency and in rich radiation environments. Different research areas have been involved: design, modeling and simulation, fabrication and electrical characterization. The present research starts with the development of new devices especially suitable for integrated circuits' development, and continues with the SiC ICs implementation and characterization. Therefore, this work contributes in several ways to the recent research effort toward the SiC device fabrication and optimization, leading to the realization of a complete integration system.

This dissertation is composed out of six chapters, which include the results of this research, and can be summarized as follows:

1. **Chapter I** is devoted to a general presentation regarding SiC material and the electronic based devices based on this WBG semiconductor. We have focused our effort on the 4H-SiC polytype due to its outstanding proprieties. This polytype is increasingly considered for electronic devices since 4 inch wafers have been demonstrated with high quality and low defects density. The potential that this material shows according to its Figures-of-Merit, made this WBG semiconductor especially suitable for the integrated circuit. These aspects are also tackled. Although most of the SiC electronic devices have received a considerable research attention during the last decade, most of them being already developed and some even commercially available, the development of SiC ICs is still in its early stage. Therefore, as SiC ICs can become a competitor of the smart Si power technology and also bring remarkable effect in automobile and aerospace industries, and telecommunication

equipment, among others, this work is orientated to developing high density integrated multi-**s**tage digital ICs on 4H-SiC.

2. The work continues with the description of the SiC device library that has been used in developing the SiC ICs.

The main active device that has been used in this development is the MESFET transistors (**Chapter II**). The state-of-art review of this topic is completed with the theoretical and experimental analyses of the already fabricated *normally-on 4H-SiC MESFETs with a mesa-etch isolation and a close-loop layout*, specially suitable for high voltage operation. An initial 4H-SiC MESFET SPICE model was extracted for high temperature operation from experimental results on this MESFET.

A ***new normally-on 4H-SiC MESFET*** structure based on the CMOS technology approaches and accounting for the typical ICs requirements has been successfully developed (**Chapter III**). One of the ***novelties*** in developing the new SiC device is the isolation technique that has been used. It was demonstrated for the first time on SiC that using the ***P^+-implanted walls*** the device isolation is successfully achieved, holding isolation voltages higher than 300V. It was also proved that this isolation technique provides a better wafer planarity, which ensures reliable interconnections between individual cells and circuits. The complexity and maturity of the device process technology is highlighted, showing that *10 levels of photolithography masks* were necessary to fabricate the device. Another ***important achievement*** of the present work is the usage of ***three metal levels*** for the MESFET development, two of which are for device and circuits interconnections. We have also demonstrated that the *finger-gate* layout geometry successfully fulfills the ***device scalability*** requirement. A new set of parameters were extracted in order to optimize the initial SPICE model for the new fabricated structures.

Concerning the best temperature matching between devices, **4H-SiC epitaxial resistors** have been as well fabricated (**Chapter IV**). From the experimental measurements it was shown that the sheet epitaxial resistance shows quite a double value than the theoretical expected value. Several causes are involved, such as the non-uniformity doping concentration of the epitaxial layer or even the non-uniformity of the SiC etch rate. It can be also expected that the N dopants are not completely ionized at low working temperatures, hence leading to a higher epitaxial resistivity. The scalability of these devices has been also proved at room and high temperature operation.

3. After defining and fabricating the device library and extracting their adequate SPICE models, the dissertation describes the ICs development (**Chapter V**). As there are not many logic families on different materials than Si and from normally-*on* devices, the NASA

topology on 6H-SiC using JFETs and epitaxial resistors, for a very small number of components or simple and small digital circuits is commented. This topology approach has been selected in the present digital circuits' development.

The extracted SPICE model from the fabricated MESFETs and epitaxial resistors allows designing the ***4H-SiC MESFET elementary logic gate library***. Multi-stage SiC ICs have been designed using this library. The transfer on SiC of some of the most common Si CMOS standard topologies has been proved at simulation level. In this sense, the ***Master-Slave Data Flip-Flop*** and the ***Data-Reset Flip-Flop*** topologies have been implemented. The ***Toggle Flip-Flop*** has been developed following NASA's topology.

From the experimental results it has been demonstrated that the development and fabrication of complex multi-stage ICs has been successfully achieved. It has been highlighted that the *functionality of the multi-stage ICs on SiC is provided by the elementary logic gates library operation* at room and high temperature, as well as at high frequency. Due to the difference obtained between the designed and experimental epitaxial resistors, several changes in the experimental results have been detected. We have shown that the tuning of the supply voltages helps to set the proper High and Low levels of the digital circuits at room temperature. In relation with the ICs performance in temperature, it was pointed out that the follower transistor causes a negative drift of the output response for temperatures over 200ºC. Even though, the SiC ICs show a proper operation in the whole temperature range. The ICs' high frequency operation has been also demonstrated. Therefore, we confirm that our normally-*on* SiC MESFET ICs technology enables the fabrication of digital ICs with a large device number, with a high integration density and consuming low areas.

4. Finally, we have demonstrated that ***Schottky-gated based device shows an excellent radiation hardness*** (**Chapter VI**). Encapsulated Schottky diodes specially design for the Bepi-Colombo space mission and mesa-MESFET transistors, both having the same Schottky metal as the previous designed MESFETs (Tungsten-Schottky metal), have been submitted to 10MeV proton and 15MeV electron irradiation at different fluences and doses. From the experimental characterization it was demonstrated that the packaged Schottky diodes show no alteration after both irradiation tests. Moreover, after proton irradiation the SiC-Schottky interface experienced an improvement by decreasing the leakage current. After electron irradiation both forward voltage and the reverse current improve. The mesa-MESFETs' electrical parameters show slight modifications after proton radiation, whereas after the electron irradiation they experiment no significant changes. These experiments confirm that these devices present good radiation hardness, hence being perfectly suitable for harsh radiation applications. A similar radiation hardness behavior is expected for the new fabricated MESFET structures together with the multi-stage digital building blocks.

FURTHER WORK

From the experimental characterization at high frequencies we have seen that the tested SiC ICs show quite a similar behavior with respect to their Inputs in the whole frequency range, although the Input shapes showed some deterioration at frequencies higher than 200 kHz. Therefore, in order to have more accurate measurements a new Test Interface circuit able to withstand high frequency signals will be built in a near future.

We have also demonstrated that by realizing external wiring between different circuits, new logic functions can be created. Therefore, another future topic is to connect more SiC ICs in different configurations in order to make more complex building blocks necessary for a specific application, such as the conventional phase frequency detector (PFD), which is obtained by connecting two DRFF, one NAND and one Inverter.

From the radiation experiment we have demonstrated that Schottky-gated devices are predicting good radiation hardness. However, for a more complete study, future radiation experiments on the new MESFET developed structures together with the fabricated integrated circuits will be performed.

LIST OF PUBLICATIONS

[1] V. Banu, P. Godignon, X. Jorda, M. Alexandru, J. Millan
"*Study on the Feasibility of SiC Bandgap Voltage Reference for High Temperature Applications*"
Materials Science Forum, Vol. 679 – 680, p.754-757 (2011)

[2] M. Alexandru, V. Banu, M. Vellvehi, P. Godignon, J. Millan
"*Design of Logic Gates for High Temperature and Harsh Radiation Environment Made of 4H-SiC MESFET*"
IEEE International Semiconductor Conference (CAS), Vol. 2, p. 413-416 (2010)

[3] M. Alexandru, V. Banu, M. Vellvehi, P. Godignon, J. Millan
"*Design of Digital Electronics for High Temperature using Basic Logic Gates made of 4H-SiC MESFETs*"
Materials Science Forum, Vol. 711, p. 104-108 (2011)

[4] M. Alexandru, V. Banu, M. Vellvehi, P. Godignon, J. Millan
"*Comparison between Mesa Isolation and P+ Implantation Isolation for 4H-SiC MESFET Transistors*"
IEEE International Semiconductor Conference (CAS), Vol. 2, p. 317-320 (2011)

[5] V. Banu, P. Godignon, X. Jordá, M. Alexandru, J. Millàn
"*SiC Schottky Diode Surge Current Analysis and Application Design Using Behavioral SPICE Models*"
IEEE International Semiconductor Conference (CAS), Vol. 2, p. 359-362, (2012)

[6] M. Alexandru, V. Banu, M. Vellvehi, P. Godignon, J. Millan
"*4H-SiC Digital Logic Circuitry Based on P+ Implanted Isolation Walls MESFET Technology*"
Materials Science Forum, Vol. 740 – 742, p.1048-1051 (2012)

[7] M. Florentin, M. Alexandru, A. Constant, B. Schmidt, P. Godignon
"*10 MeV Proton Irradiation Effect on 4H-SiC nMOSFET Electrical Parameters*"
Submitted and accepted to HeteroSiC – WASMPE 2013

[8] M. Alexandru, M. Florentin, A. Constant, B. Schmidt, P. Michel, P. Godignon
"*5MeV Proton and 15MeV Electron Radiation Effects Study on 4H-SiC nMOSFET Electrical Parameters*"
Submitted and accepted to RADECS 2013

[9] M. Alexandru, V. Banu, M. Vellvehi, P. Godignon, J. Millan
"*4H-SiC MESFET Specially Designed and Fabricated for High Temperature Integrated Circuits*"
Submitted and accepted to ESSDERC 2013

[10] V. Banu, P. Godignon, M. Alexandru, M. Vellvehi, X. Jordà, J. Millán
"*High Temperature-Low Temperature Coefficient Analog Voltage Reference Integrated Circuit Implemented with SiC MESFETs*"
Submitted and accepted to ESSCIRC 2013

[11] M. Alexandru, V. Banu, P. Godignon, X. Jordà, M. Vellvehi, D. Tournier
"*High Temperature Electrical Characterization of 4H-SiC MESFET Basic Logic Gates*"
Submitted to ICSCRM 2013

[12] M. Florentin, M. Alexandru, A. Constant, B. Schmidt, P. Godignon
"*Low Proton Radiation Impact on 4H-SiC nMOSFET Electrical Parameters*"
Submitted to ICSCRM 2013

[13] V. Banu, J. Montserrat, M. Alexandru, X. Jordà, J. Millán, P. Godignon
"*Monolithic Integration of Power MESFET for High Temperature SiC Integrated Circuits*"
Submitted to ICSCRM 2013

[14] M. Alexandru, V. Banu, P. Godignon, J. Millán
"*Monolithic Integration of High Temperature Silicon Carbide Integrated Circuits*"
Submitted and accepted to ECS 2013

LIST OF SYMBOLS AND ACRONYMS

Symbol	Name	*Unit*
A	The resistor cross-section area	m^2
a	The epitaxial layer thickness	*m*
AF	Flicker-noise exponent	
BETA=β	Transconductance parameter – SPICE	A/V^2
BETA$_{TCE}$	Transconductance exponential temperature coefficient – SPICE	$1/^oC$
BFOM	Baliga's Figure-of-Merit	
σ	Semiconductor conductivity	*S/m*
C_{GS}	Zero-bias G-S junction capacitance – SPICE	*F*
C_{GD}	Zero-bias G-D junction capacitance – SPICE	*F*
E_c	Critical electric field	*MV/cm*
E_g	Bandgap energy	*eV*
ε_r	Relative dielectric constant	
FC	Coefficient for forward-bias depletion capacitance – SPICE	
g_m	The device transconductance / gain	*S*
I-V	Current-Voltage characteristics	
ICs	Integrated Circuits	
I_{Dsat}	The saturation drain current	*A*
I_{DSS}	The saturation drain current	*A*
I_{LK}	Leakage current	*A*
I_{ON}/I_{OFF}	On-Off current ratio	
I_S	Gate junction saturation current	*A*
JFOM	Johnsoln's Figure-of-Merit	
KFOM	Keyes' Figure-of-Merit	
KF	Flicker-noise coefficient	
λ	Thermal conductivity	W/cm^oK
LAMBDA=λ	Channel length modulation parameter – SPICE	V^{-1}
L	Resistor length	*m*
L_G	Gate length	*m*
M	Junction grading coefficient	
μ_n	Electron mobility	cm^2/Vs
μ_p	Hole mobility	cm^2/Vs
N_A	Acceptor doping concentration	cm^{-3}

N_D	Donor doping concentration	cm^{-3}
n_i	Intrinsic carrier concentration	cm^{-3}
NM_H	Noise Margins High	V
NM_L	Noise Margins Low	V
NMs	Noise Margins	V
N_{Sq}	Square numbers	
PB	Gate junction potential	V
P_D	Power Dissipation	W
ρ	Semiconductor resistivity	$\Omega \cdot m$
ρ_C	Specific contact resistance	$\Omega \cdot cm^2$
R_C	Contact resistance	Ω
R_{LOAD}	Load resistor	Ω
R_{ON}	The on-state resistance	Ω
R_S	Sheet resistance	Ω
T	Temperature	K
T_P	Propagation Delay	s
T_{PLH}	Propagation Delay from Low-to-High	s
T_{PHL}	Propagation Delay from High-to-Low	s
t_F	Fall time	s
t_R	Rise time	s
TNOM	Parameter measurement temperature – SPICE	^oC
ϕ_0	The internal potential of the pn-junction	V
V_{Bi}	The built-in voltage of the Schottky gate	V
v_i	Input voltage	V
$V_{OH,min}$	Minimum high output voltage level	V
$V_{OL,max}$	Maximum low output voltage level	V
$V_{IH,min}$	Minimum high input voltage level	V
$V_{IL,max}$	Maximum low input voltage level	V
V_{OUT}	Output voltage	V
V_P	Pinch-off voltage	V
V_R	Polarization voltage	V
V_T	Threshold voltage	V
V_{th}	Thermal voltage	V
$VT0_{TC}$	Threshold voltage temperature coefficient – SPICE	$V/^oC$
V_M	Switching threshold voltage	V
XTI	IS temperature coefficient – SPICE	m
W	Resistor width	m
W_{epi}	N-epilayer depth	m
W_G	Schottky junction depth	m
W_{SCH}	Schottky junction depth	m
W_N	Depletion region in the N-layer	m
W_P	Depletion region in the P-layer	m
Z_G	Gate width	m

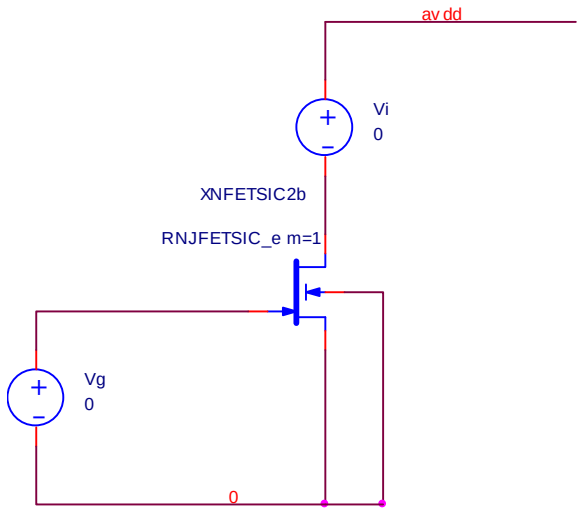
ANNEXES

ANNEX.A – 4H-SiC MESFET SPICE Models

ANNEX.A1 – SPICE Model Mesa-MESFET – Extracted Model

The heart of the SPICE model is the ***netlist***, which is simply a list of components and the nets (or nodes) that connect them together. Therefore, in the following part the netlist of the 4H-SiC mesa-MESFET extracted SPICE model is presented together with the device circuit SPICE test schematic:

```
*** Netlist Description 4H-SiC mesa-MESFET ***

.SUBCKT RNJFETSIC_e D G S B
Rd D D1 rsicn 12
Rs S S1 rsicn 10
J1 D1 J S1 RNJFETSIC
EJ J G B G 0.02

.MODEL RNJFETSIC NJF LEVEL=1
+Beta=0.000145
+Betatce=-.441
+Rd=0
+Rs=0
+Lambda=2e-3
+Vto=-14.2
+Vtotc=-0.53e-4
+Is=1E-17
+N=1
+Xti=3
*+Alpha=506.8u
+Cgd=3p
+M=1.00001
```



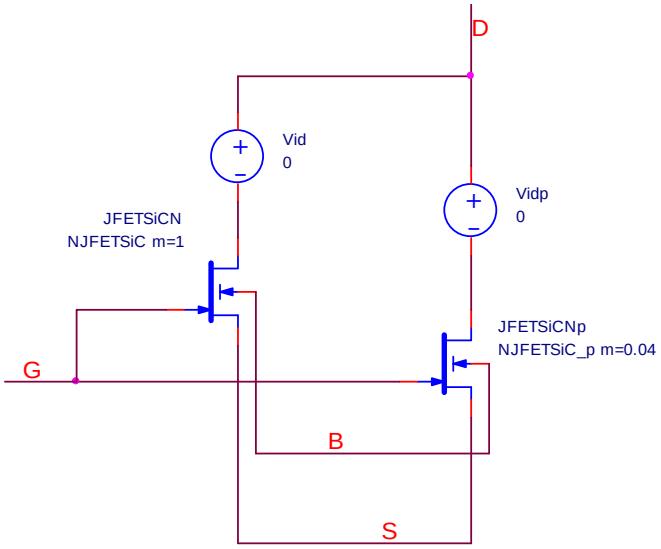
4H-SiC MESFET - Circuit Schematic of SPICE Simulation

```
+Pb=1.3
+Fc=0.5
+Cgs=10.083p
+Kf=1.259E-18
+Af=1
.ENDS RNJFETSIC_e
```

ANNEX.A2 – SPICE Model for the Planar-MESFET – The Design Model

The SPICE netlist for the proposed SPICE model that was used in the design chapter of the ICs MESFET is next presented, for both transistors. This model was derived from the mesa-MESFET SPICE model and has the purpose to predict the planar-MESFET operation prior fabrication. The SPICE circuit test schematic for the devices is also presented:

```
*** Netlist Description 4H-SiC ICs-MESFET - Extrapolated Model ***

*** Main ICs MESFET m=1 ***

.SUBCKT NJFETSiC D G S B
Rd D D1 rsicn 12
Rs S S1 rsicn 10
J1 D1 J S1 NJFETSiC
EJ J G B G 0.02 $2.680e-01

.MODEL NJFETSiC NJF LEVEL=1
+Beta=0.0003125
+Betatce=-.441
+Rd=0
+Rs=0
+Lambda=2e-3
+Vto=-8
+Vtotc=-0.53e-4
+Is=1E-17
+N=1
+Xti=3
*+Alpha=506.8u
+Cgd=3p
+M=1.00001
+Pb=1.3
+Fc=0.5
+Cgs=10.083p
+Kf=1.259E-18
+Af=1
```



4H-SiC ICs MESFET
Circuit Schematic of SPICE Simulation

```
.ENDS NJFETSiC
```

***** Oxide gated - ICs MESFET m=0.04 *****

```
.SUBCKT NJFETSiCp D G S B
Rd D D1 rsicn 12
Rs S S1 rsicn 10
J1 D1 J S1 NJFETSiCp
EJ J G B G 0.02 $2.680e-01

.MODEL NJFETSiCp NJF LEVEL=1
+Beta=0.0003125
+Betatce=-.441
+Rd=0
+Rs=0
+Lambda=2e-3
+Vto=-12.5
+Vtotc=-0.53e-4
+Is=1E-17
+N=1
+Xti=3
*+Alpha=506.8u
+Cgd=3p
+M=1.00001
+Pb=1.3
+Fc=0.5
+Cgs=10.083p
+Kf=1.259E-18
+Af=1
.ENDS NJFETSiCp
```

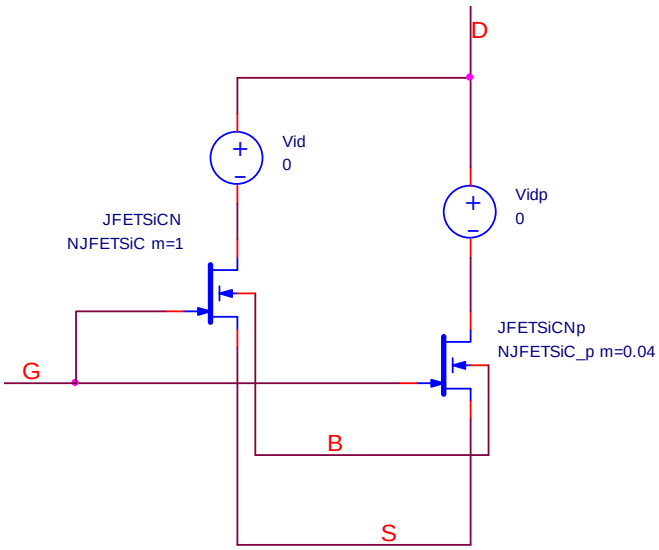
***** 4H-SiC Resistance SPICE proposed model *****

```
.model rsicn r tc1=7.4798E-03 tc2=1.8011E-05
```

ANNEX.A3 – SPICE Model Planar-MESFET – Extracted Model

Once the 4H-SiC ICs MESFETs were fabricated, a new parameter extraction was performed and the design SPICE model was updated with the new extracted parameters. Next the SPICE netlist for the fabricated ICs MESFETs is presented:

```
*** Netlist Description 4H-SiC ICs-MESFET - Extracted Model ***

*** Main ICs MESFET m=1 ***

.SUBCKT NJFETSiC D G S B
Rd D D1 rsicn 100
Rs S S1 rsicn 30
J1 D1 J S1 NJFETSiC
EJ J G B G 0.021 $2.680e-01

.MODEL NJFETSIC NJF LEVEL=1

+Beta=0.00025
+Betatce=-.374
+Rd=0
+Rs=0
+Lambda=5e-4
+Vto=-8.26
+Vtotc=-5.3e-5
+Is=1E-17
+N=1
+Xti=3
*+Alpha=506.8u
+Cgd=3p
+M=1.00001
+Pb=1.3
+Fc=0.5
+Cgs=10.083p
+Kf=1.259E-18
+Af=1

.ENDS NJFETSiC
```



4H-SiC ICs MESFET
Circuit Schematic of SPICE Simulation

***** Oxide gated - ICs MESFET m=0.04 *****

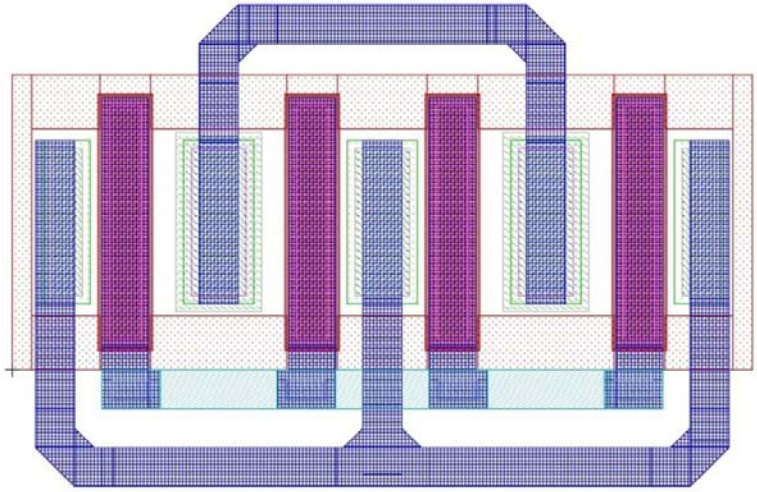
```
.SUBCKT NJFETSiCp D G S B
Rd D D1 rsicn 35
Rs S S1 rsicn 18
J1 D1 J S1 NJFETSiCp
EJ J G B G 0.02 $2.680e-01

.MODEL NJFETSiCp NJF LEVEL=1
+Beta=0.00024
+Betatce=-.374
+Rd=0
+Rs=0
+Lambda=4e-3
+Vto=-14
+Vtotc=-5.3e-5
+Is=1E-17
+N=1
+Xti=3
*+Alpha=506.8u
+Cgd=3p
+M=1.00001
+Pb=1.3
+Fc=0.5
+Cgs=10.083p
+Kf=1.259E-18
+Af=1

.ENDS NJFETSiCp
```

***** 4H-SiC Resistance SPICE extracted model *****

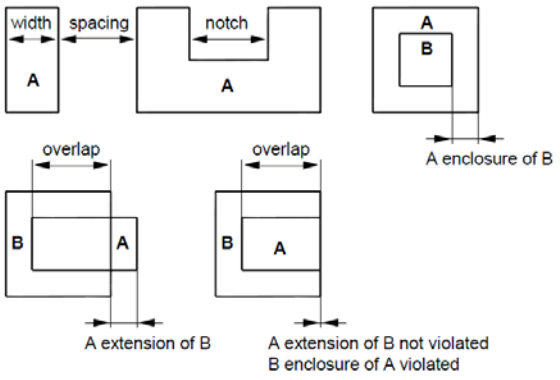
```
.model rsicn r tc1=7.4798E-03 tc2=1.8011E-05
```

ANNEX.B – The Planar-MESFET Dimensions and DRC rules

The Design Rule Checker (DRC) is an important step in developing integrated circuits. In this step of the design the DRC ensures that the circuit layout corresponds to the original electric schematic of the design. The DRC constrains may came as a requirement of the design itself or as a requirement of the fabrication process used to realize the devices and circuits. Due to the complexity of the created ICs on SiC we have defined a set of design rules relaying on the actual fabrication limitations. The layout of the *planar-MESFET transistor with 4 finger-gates* is next presented. This device contains all the masks that were used in the circuit's realization as well.



Geometric Relations



Dimensions *(length x width)* :

GATE Dimensions	14 µm x 66 µm
Gate CONT Dimensions	8 µm x 60 µm
Gate VIA2 Dimensions	12 µm x 64 µm
Source NPLUS Dimensions	12 µm x 42 µm
Source OHMIC Dimensions	8 µm x 38 µm
Source CONT Dimensions	8 µm x 38 µm
Single Drain NPLUS Dimensions	12 µm x 42 µm
Single Drain OHMIC Dimensions	16 µm x 46 µm
Single Drain CONT Dimensions	8 µm x 38 µm
Shared Drain NPLUS Dimensions	18 µm x 42 µm
Shared Drain OHMIC Dimensions	22 µm x 46 µm
Shared Drain CONT Dimensions	14 µm x 38 µm
Source & Drain VIA2 Dimensions	10 µm x 42 µm
Minimum VIA3 Dimensions	10 µm x 5 µm

The major structure and circuit **layout design rules** that we have applied are:

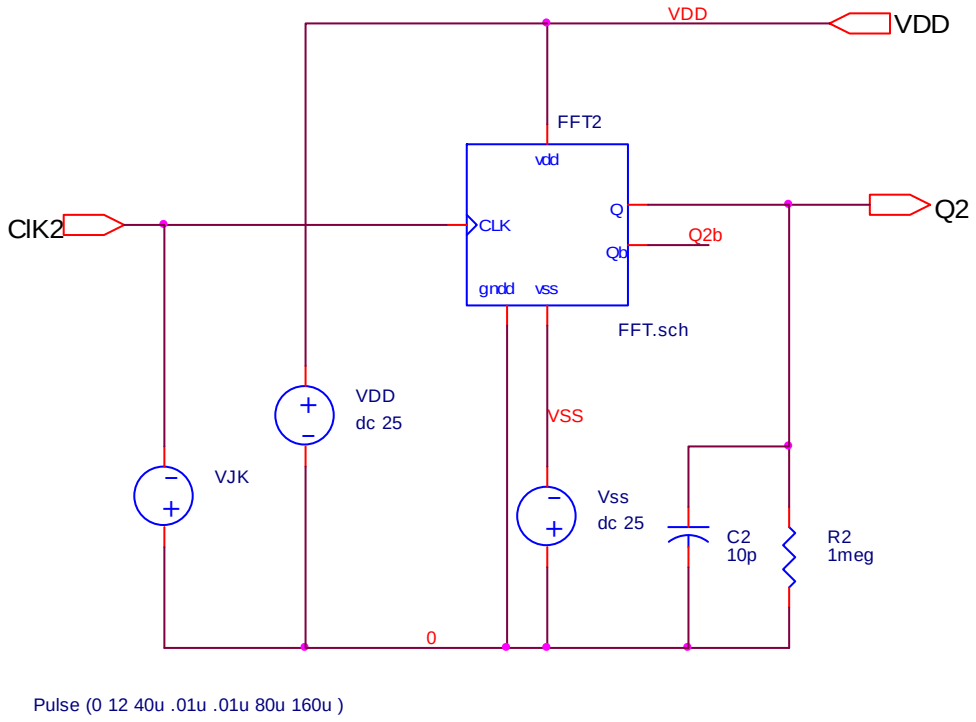
Minimum PPLUS width	5 µm
Minimum MET2 width	10 µm
Minimum MET3 width	10 µm
CONT without MET2	Not allowed
MET2 without VIA2	Not allowed
OHMIC without CONT	Not allowed
GATE without CONT	Not allowed
VIA3 without MET2 & MET3	Not allowed
Overlap of NPLUS and PPLUS	Not allowed
Minimum NPLUS spacing to NPLUS	11 µm
Minimum PPLUS spacing to NPLUS	3 µm
Minimum NPLUS spacing to GATE	2 µm
Minimum PPLUS spacing of OHMIC	1 µm
Minimum OHMIC spacing of PPLUS	1 µm
Minimum OHMIC spacing of GATE	4 µm
Minimum GATE spacing of NPLUS	2 µm
Minimum GATE spacing of OHMIC	4 µm
Minimum MET2 spacing to MET2	7 µm

Minimum VIA2 spacing to VIA2	7 µm
Minimum MET3 spacing to MET3	5 µm
Minimum OHMIC enclosure of CONT	0 µm
Minimum GATE enclosure of CONT	3 µm
Minimum GATE enclosure of MET2	1 µm
Minimum GATE enclosure of VIA2	1 µm
Minimum MET2 enclosure of VIA3	2 µm
Minimum MET3 enclosure of VIA3	2 µm

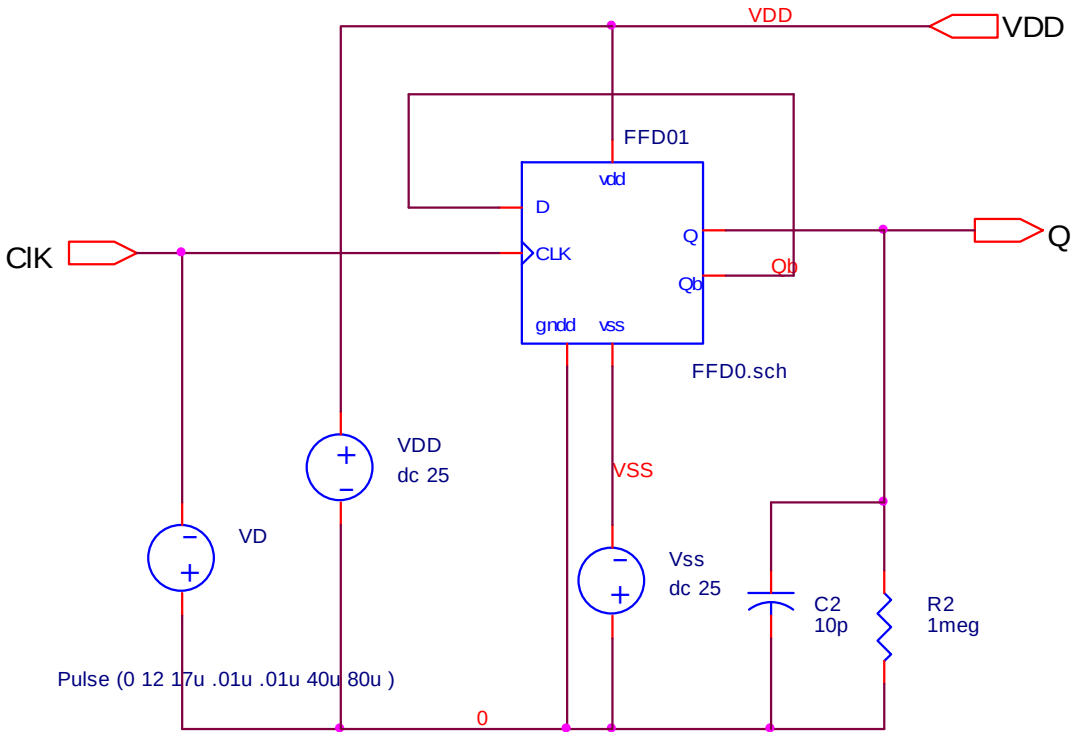
ANNEX.C –Test Circuits used for Digital ICs Simulation

In order to be able simulate the multi-level digital ICs presented in Chapter V, additional test circuits were necessary to be realized. The simulated diagrams presented for the Flip-Flops correspond to the next test schematics created for each of the complex logic 4H-SiC ICs:

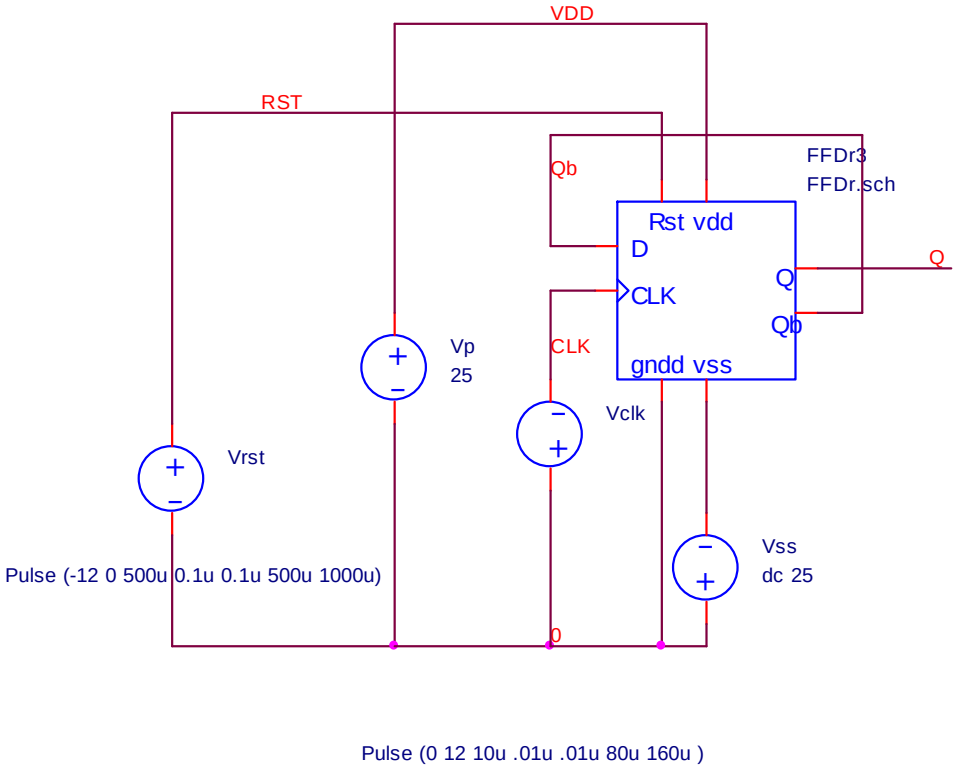
Toggle Flip-Flop



Master-Slave D Flip-Flop



D-Reset Flip-Flop



ANNEX.D – Wafer-Dice – Circuits Configuration

After all the fabrication steps have been completed the wafer looks like in Fig.AX.D.1 and contains 60 entire chips. One chip (Fig.AX.D.2) is composed from two parts having 3.5mm x 7mm. The chip was further divided into two equal parts (3.5mmx3.5mm) – dice that was after encapsulated. From Fig.AX.D.2 it can be observed all the fabricated SiC circuits. For a better electrical characterization and also due to the fabrication limitations, the pad dimension is 162µm x 162µm and the minimum distance in between them is 120µm. The distance between two different rows of pads is 1.5mm.

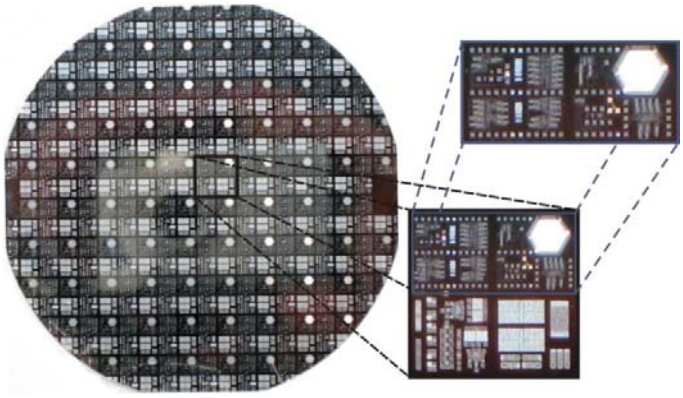


Fig.AX.D.1. *Fabricated SiC wafer – one entire chip – CNM chip*

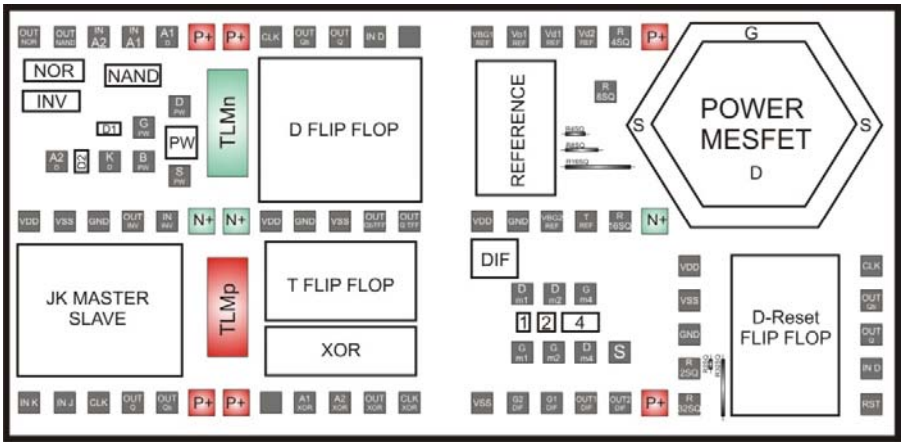


Fig.AX.D.2. *Device – circuit's distribution on the main chip*