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Design and Control of an Electric Energy Conditioning System for a PEM Type Fuel Cell

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by

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To my family Sharon, Dora and Luis.

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Abstract

Isolated electric energy generation systems are often needed to supply electric loads where the electrical network is not available. This could be caused due to geographic isolation, the necessity of load mobility, demanded values of voltage and current that are not compatible with the local networks, etc. This makes the design and construction of stand-alone energy generation systems a must.

Modern designs are being pushed towards cleaner technologies. The experience has shown that the usual methods employed to produce electrical energy are not sustainable, especially because of environmental concerns. Usual stand-alone energy generation systems employ batteries and fuel engines. Batteries offer a cheap mean to feed the generation system but need rigorous maintenance routines, the substances used in their construction are strong pollutants, offer relatively low durability and the ratio charge time/discharge time is too high. Fuel engines extract their energy from petroleum based fuels, and as its well known, pollute their surrounding environment in several ways producing smoke, noise and heat.

Polymer electrolyte membrane type fuel cells are among the new technologies that are being considered as a good alternative to the traditional power sources used for stand-alone energy generation systems. Although the basic principles of operation of the fuel cells are known since 1839, this is a technology that is far from being mature. More work needs to be done in order to make of the fuel cells systems with, high reliability, with maximum efficiency, and capable of providing electrical energy with quality comparable to the quality achieved using usual methods.

The problems when working with fuel cells can be split in two big groups of interest, the first, being the handling and control of the electrochemical variables, and the second, the handling and control of the electrical variables taking care of the limits imposed by the dynamics of the fuel cell unit. This work deals with the second group of concerns, looking at the fuel cell as a black-box dc power supply with certain current/voltage characteristics. The energy provided by the fuel cells needs to be conditioned to the levels and characteristics required by the loads to be fed. In Europe, for single-phase ac loads, the specifications are a sinusoidal output voltage with 230 V ac rms and a frequency of 50 Hz. This work presents the the analysis, design, construction, and control of the electric energy conditioning system for a polymer electrolyte membrane type fuel cell to act as an stand-alone dc-ac inverter to feed linear or nonlinear loads with big variations.

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A three months research internship has been developed from January/05/2009 to April/07/2009 at the *Division systèmes* of the *Laboratoire des signaux et systèmes* (L2S), located at Gif-Sur-Yvette, France. The L2S is a common facility to *L'École Supérieure d'Électricité* (SUPÉLEC), the French *Centre National de la Recherche Scientifique* (CNRS), and the *Université Paris-Sud 11*. This internship has been accomplished under the scientific guidance of Prof. Romeo Ortega and with the financial support of the "*Departament d'Innovació, Universitats i Empresa*" of the "*Generalitat de Catalunya*" by means of a BE travel grant ("*Beques per a estades de recerca fora de Catalunya*") with expedient number 2008 BE1 00091 (3,330.00 €) and the *Institut d'Organització i Control de Sistemes Industrials* (IOC), part of the *Universitat Politècnica de Catalunya* (UPC) (900.00 €).

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Notation and Acronyms

Common electric units and abbreviations

A	Ampere.
ac	Alternating current.
dc	Direct current.
Hz	Hertz.
kW	kilo-Watt.
kVA	kilo-Volt-Ampere.
MW	Mega-Watt.
MVA	Mega-Volt-Ampere.
rad/s	Rad/seconds.
rms	root mean square.
V	Volt.
VA	Volt-Ampere.
W	Watt.

Fuel cells

A-FC	Alkaline fuel cell.
DMFC	Direct methanol fuel cell.
FC	Fuel cell.
GVB	Gas voltaic battery.
MCFC	Molten carbonate fuel cell.
fgPAFC	Phosphoric acid fuel cell.
PEM	Polymer electrolyte membrane.
SOFC	Solid oxide fuel cell.
SPFC	Solid polymer fuel cell.

Power converters and hardware terminology

APU	Auxiliary power unit.
CCM	Continuous-conduction mode.
DCM	Discontinuous-conduction mode.
DG	Distributed generation.

Power converters and hardware terminology

EMI	Electro-magnetic interference.
IGBT	Insulated-gate bipolar transistor.
MOSFET	Metal-oxide-semiconductor field-effect transistor .
MSPI	Multiple-stage dc-ac power inverter.
PV	Photovoltaic.
PWM	Pulse-width modulation.
RCD	Resistor-capacitor-diode.
SC	Supercapacitor.
SSPI	Single-stage dc-ac power inverter.
UPS	Uninterruptible power supply.
VDSS	Drain-to-source breakdown voltage.
VRRM	Maximum repetitive reverse voltage.

Hardware/software implementation terminology

ADC	Analog-to-digital converter.
ADSP	Advanced digital signal processor.
DSP	Digital signal processor.
DMA	Direct memory access.
DAI	Digital application interface.
f_s	Sampling frequency.
f_{sw}	Switching frequency.
T_s	Sampling period $T_s = 1/f_s$.
T_{sw}	Switching period $T_{sw} = 1/f_{sw}$.
v_{bus}	Voltage at the common interconnection point between the step-up, APU and dc-ac inversion stages.
ZOH	Zero-order hold.

Power quality criteria

CF	Crest factor.
IEC	International electrotechnical commission.
THD	Total-harmonic distortion.
THD_i	Total-harmonic distortion of the current.
THD_v	Total-harmonic distortion of the voltage.
$\text{THD}_\text{i}^{\text{max}}$	Maximum allowed total-harmonic distortion of the current.
$\text{THD}_\text{v}^{\text{max}}$	Maximum allowed total-harmonic distortion of the voltage.
$\text{THD}_\text{i}^{\text{rms}}$	Total-harmonic distortion of the current with respect to the total rms value of the signal.
$\text{THD}_\text{v}^{\text{rms}}$	Total-harmonic distortion of the voltage with respect to the total rms value of the signal.

Control schemes

AFC	Adaptive feedforward cancellation.
DT-AFC	Discrete-time adaptive feedforward cancellation.
GPC	Global power balance control.
IMP	Internal model principle.

Step-up stage

Step-up converter - Hardware components and circuit description of the base converter topology

D_1	Diode D_1 of the step-up converter.
D_2	Diode D_2 of the step-up converter.
Φ_1	Total flux through the primary winding of the high-frequency transformer.
Φ_2	Total flux through the secondary winding of the high-frequency transformer.
Φ_{i_1}	Effective flux through the primary winding of the high-frequency transformer.
Φ_{i_2}	Effective flux through the secondary winding of the high-frequency transformer.
$\Phi_{\sigma_{i_1}}$	Loss flux through the primary winding of the high-frequency transformer.
$\Phi_{\sigma_{i_2}}$	Loss flux through the secondary winding of the high-frequency transformer.
i_1	Current through the primary winding of the high-frequency transformer.
i_2	Current through the secondary winding of the high-frequency transformer.
i_{C_1}	Current flowing through capacitor C_1 .
i_{C_2}	Current flowing through capacitor C_2 .
i_{D_1}	Current flowing through diode D_1.
i_{D_2}	Current flowing through diode D_2.
i_{sw}	Drain-to-source current present at the switch of the step-up converter.
i^{hvs}	Current present at the high-voltage side of the step-up converter.
i^{lvs}	Current present at the low-voltage side of the step-up converter.
L_1	Inductance of the primary winding seen at the terminals of the high-frequency transformer.
L_2	Inductance of the primary winding seen at the terminals of the high-frequency transformer.
L_{11}	Effective inductance of the primary winding of the high-frequency transformer.
L_{22}	Effective inductance of the secondary winding of the high-frequency transformer.

Step-up converter - Hardware components and circuit description of the base converter topology

L_{σ_1}	Loss inductance of the primary winding of the high-frequency transformer.
L_{σ_2}	Loss inductance of the secondary winding of the high-frequency transformer.
M	Coupling inductance between the primary and secondary windings of the high-frequency transformer.
N_1	Number of turns of the coil of the primary winding high-frequency transformer.
N_2	Number of turns of the coil of the secondary winding high-frequency transformer.
T_f	High-frequency transformer of the step-up converter .
u_1	Switch of the step-up converter.
v_1	Voltage present at the primary winding high-frequency transformer.
v_2	Voltage present at the secondary winding high-frequency transformer.
v_{C_1}	Voltage present at the terminals of capacitor C_1.
v_{C_2}	Voltage present at the terminals of capacitor C_2.
v_{D_1}	Voltage present at the terminals of diode D_1 .
v_{D_2}	Voltage present at the terminals of diode D_2 .
v_{sw}	Drain-to-source voltage present at the switch of the step-up converter.
v^{hvs}	Voltage present at the high-voltage side of the step-up converter.
v^{lvs}	Voltage present at the low-voltage side of the step-up converter.

Step-up stage - small-signal swept-sine analysis

A	Amplitude of the variation of the input current around $i_{fc_{ss}}$.
C_{in}	Capacitance used on the input filter of the step-up stage.
ε	Amplitude of the sinusoidal disturbance $\tilde{u}_1$ applied to the input variable $\hat{u}_1$.
ϕ	Phase shift of the variation of the input current around $i_{fc_{ss}}$.
i_{fc}	Current delivered to the step-up stage by the fuel-cell unit.
$i_{fc_{ss}}$	Steady-state current at the input of the step-up stage.
$\tilde{i}_{fc}$	Variation of the input current around $i_{fc_{ss}}$.
i_{ss}^{hvs}	Steady-state current delivered at the high-voltage side of the step-up converter.
L_{in}	Inductance used on the input filter of the step-up stage.
ω	Frequency of the sinusoidal disturbance $\tilde{u}_1$ applied to the input variable $\hat{u}_1$.
ω_1	Lower frequency value used for the swept-sine tests.
ω_2	Maximum frequency value used for the swept-sine tests.

Step-up stage - small-signal swept-sine analysis

p_{ss}^{hvs}	Steady-state power delivered at the high-voltage side of the step-up converter.
$r_{L_{in}}$	Parasitic resistance of the inductance used on the input filter of the step-up stage.
$\hat{u}_1$	PWM duty cycle applied to switch u_1 .
$\hat{u}_{1_{ss}}$	Steady-state PWM duty cycle applied to switch u_1.
$\tilde{u}_1$	Sinusoidal disturbance applied to the input variable $\hat{u}_1$.
v_{fc}	Voltage delivered to the step-up stage by the fuel-cell unit.
$v_{fc_{ss}}$	Steady-state voltage at the input of the step-up stage.
v_{ss}^{hvs}	Steady-state voltage delivered at the high-voltage side of the step-up converter.

Step-up stage - Input current control

$C_1(z)$	Input current controller.
$D_1(z)$	Derivative component of the input current controller $C_1(z)$.
$G_1(s)$	Step-up converer duty cycle $U_1(s)$ to input curent $I_1(s)$ continuous-time transfer function.
$G_1(z)$	Step-up converer duty cycle $U_1(s)$ to input curent $I_1(s)$ discrete-time transfer function.
$I_1(z)$	Integral component of the input current controller $C_1(z)$.
i_{fc}^{ref}	Input current controller reference .
K_{d_1}	Derivative constant of the input current controller $C_1(z)$.
K_{i_1}	Integral constant of the input current controller $C_1(z)$.
K_{p_1}	Proportional constant of the input current controller $C_1(z)$.
K_{aw_1}	Proportional constant of the anti-windup system for the controller $C_1(z)$.
$L_1(z)$	Open-loop transfer function of the controller $C_1(z)$ with the plant $P_1(z)$.
L_{aw_1}	Open-loop transfer function anti-windup system for the controller $C_1(z)$.
$P_1(z)$	Plant controlled by the input current controller $C_1(z)$.
$S_1(z)$	Closed-loop sensitivity transfer function of the controller $C_1(z)$ with the plant $P_1(z)$.
$\|\|S_1(z)\|\|_\infty$	∞-norm of the closed-loop sensitivity transfer function of the controller $C_1(z)$ with the plant $P_1(z)$.
$T_1(z)$	Closed-loop transfer function of the controller $C_1(z)$ with the plant $P_1(z)$.
$\|\|T_1(z)\|\|_\infty$	∞-norm of the closed-loop transfer function of the controller $C_1(z)$ with the plant $P_1(z)$.

Full-bridge dc-ac inverter

Full-bridge dc-ac inverter - Hardware components and circuit description

C_f	Capacitance used on the output filter of the full-bridge dc-ac inverter.
C_o	Capacitance used on the non-linear load..
L_f	Inductance used on the output filter of the full-bridge dc-ac inverter.
r_{L_f}	Parasitic resistance of the inductance used on the output filter of the full-bridge dc-ac inverter.
R_o	Resistance used on the non-linear load..
u_2	Upper switch of the second leg of the full-bridge dc-ac inverter.
u_2^*	Lower switch of the second leg of the full-bridge dc-ac inverter.
$\bar{u}_2$	Upper switch of the first leg of the full-bridge dc-ac inverter.
$\bar{u}_2^*$	Lower switch of the first leg of the full-bridge dc-ac inverter.
$\check{u}_2$	Discrete characterization of the behavior of the second leg of the full-bridge dc-ac inverter.
$\check{u}_2^*$	Discrete characterization of the behavior of the first leg of the full-bridge dc-ac inverter.
$\hat{u}_2$	PWM duty cycle applied to switch u_2 .
v	Midpoint voltage of the second leg of the full-bridge dc-ac inverter.
v^*	Midpoint voltage of the first leg of the full-bridge dc-ac inverter.
v_{out}	Output voltage of the full-bridge dc-ac inverter .

Full-bridge dc-ac inverter - DT-AFC control

$C_2(z)$	DT-AFC inner-loop controller.
$C_{AFC}(z)$	DT-AFC resonators-loop controller.
f_k	Resonating frequency of the kth controller in Hz.
φ_k	Phase shift of the kth resonator in rads.
$G_2(s)$	Duty cycle U_2 to output voltage V_{out} continuous-time transfer function.
$G_2(z)$	Duty cycle U_2 to output voltage V_{out} discrete-time transfer function.
g_k	Gain parameter of the kth resonator.
$H(z)$	Integrator module used on the discrete-time resonator structure $R_k(z)$.
K_0	DT-AFC proportional constant.
$L_2(z)$	Open-loop transfer function of the DT-AFC inner-loop controller $C_2(z)$ with the plant $P_2(z)$.
$L_{AFC}(z)$	Open-loop transfer function of the DT-AFC resonators-loop controller $C_{AFC}(z)$ with the plant $T_2(z)$.
ω_k	Resonating frequency of the kth controller in rad/s.
$P_2(z)$	Plant controlled by the DT-AFC inner-loop controller $C_2(z)$.
$R_k(s)$	Continuous-time AFC resonator structure.

Full-bridge dc-ac inverter - DT-AFC control

$R_k(z)$	Discrete-time DT-AFC resonator structure.
$S_2(z))$	Closed-loop sensitivity transfer function of the DT-AFC inner-loop controller $C_2(z)$ with the plant $P_2(z)$.
$\|\|S_2(z)\|\|_\infty$	∞-norm of the closed-loop sensitivity transfer function of the DT-AFC inner-loop controller $C_2(z)$ with the plant $P_2(z)$.
$S_{AFC}(z)$	Closed-loop sensitivity transfer function of the DT-AFC resonators-loop controller $C_{AFC}(z)$ with the plant $T_2(z)$.
$\|\|S_{AFC}(z)\|\|_\infty$	∞-norm of the closed-loop sensitivity transfer function of the DT-AFC inner-loop controller $C_{AFC}(z)$ with the plant $T_2(z)$.
$T_2(z)$	Closed-loop transfer function of the DT-AFC inner-loop controller $C_2(z)$ with the plant $P_2(z)$.
$\|\|T_2(z)\|\|_\infty$	∞-norm of the closed-loop transfer function of the DT-AFC inner-loop controller $C_2(z)$ with the plant $P_2(z)$.
$T_{AFC}(z)$	Closed-loop transfer function of the DT-AFC resonators-loop controller $C_{AFC}(z)$ with the plant $T_2(z)$.
$\|\|T_{AFC}(z)\|\|_\infty$	∞-norm of the closed-loop transfer function of the DT-AFC inner-loop controller $C_{AFC}(z)$ with the plant $T_2(z)$.

Auxiliary Power Unit (APU)

APU - Hardware components and circuit description

C_{bus}	Capacitance of the dc-bus linking capacitor .
C_{sc}	Total capacitance of the bank of SCs.
$\Delta_{max}\, E_{sc}$	Stored energy change of the bank of SCs.
E_{sc}	Total energy stored at the bank of SCs.
i_{apu}	Current delivered by the auxiliary power unit to the dc bus.
$\langle\, i_{apu} \rangle_{T_{sw}}$	Average current delivered by the auxiliary power unit to the dc bus over one switching period T_{sw} .
$i_{L_{apu}}$	Current flowing through the inductor L_{apu}.
$\langle\, i_{L_{apu}} \rangle_{T_{sw}}$	Average current flowing through the inductor L_{apu} over one switching period T_{sw}.
$i_{C_{bus}}$	Current flowing through the dc-bus linking capacitor C_{bus}.
$\langle\, i_{C_{bus}} \rangle_{T_{sw}}$	Average current flowing through the dc-bus linking capacitor C_{bus} over one switching period T_{sw} .
i_{sc}	Current flowing through the bank of SCs.
$\langle\, i_{sc} \rangle_{T_{sw}}$	Average current flowing through the bank of SCs over one switching period T_{sw}.
L_{apu}	Inductance used on the dc-dc interfacing converter of the APU.
$r_{L_{apu}}$	Parasitic resistance of the inductance used on the dc-dc interfacing converter of the APU.
u_3	Lower switch of the half-bridge module used on dc-dc interfacing converter of the APU.

APU - Hardware components and circuit description

$\bar{u}_3$	Upper switch of the half-bridge module used on dc-dc interfacing converter of the APU.
$\check{u}_3$	Discrete characterization of the behavior of the half-bridge module used on dc-dc interfacing converter of the APU.
$\hat{u}_3$	PWM duty cycle applied to switch u_3 .
$v_{L_{apu}}$	Voltage present at the terminals of the inductor L_{apu}.
$\langle v_{L_{apu}} \rangle_{T_{sw}}$	Average voltage present at the terminals of the inductor L_{apu} over one switching period T_{sw} .
v_{sc}	Voltage present at the terminals of the bank of SCs.
$v_{sc_{bd}}$	Break-down voltage of the bank of SCs .
$\langle v_{sc} \rangle_{T_{sw}}$	Average voltage present at the terminals of the bank of SCs over one switching period T_{sw}.
$\langle v_{bus} \rangle_{T_{sw}}$	Average voltage present at the dc bus over one switching period T_{sw}.

APU - SCs current controller

$C_3(z)$	SCs current controller.
$G_3(s)$	Auxiliary variable W to SCs current I_{sc} continuous-time transfer function.
$G_3(z)$	Auxiliary variable W to SCs current I_{sc} discrete-time transfer function.
$I_3(z)$	Integral component of the SCs current controller $C_3(z)$.
i_{sc}^{ref}	Reference delivered to the SCs current controller.
K_{aw_3}	Proportional constant of the anti-windup system for the controller $C_3(z)$.
K_{i_3}	Integral constant of the input current controller $C_3(z)$.
K_{p_3}	Proportional constant of the input current controller $C_3(z)$.
$L_{\text{aw}_3}(z)$	Open-loop transfer function anti-windup system for the controller $C_3(z)$.
$L_3(z)$	Open-loop transfer function of the SCs current controller $C_3(z)$ with the plant $P_3(z)$.
$P_3(z)$	Plant controlled by the SCs current controller $C_2(z)$.
$S_3(z)$	Closed-loop sensitivity transfer function of the SCs current controller $C_3(z)$ with the plant $P_3(z)$.
$\|\|S_3(z)\|\|_\infty$	∞-norm of the closed-loop sensitivity transfer function of the SCs current controller $C_3(z)$ with the plant $P_3(z)$.
$T_3(z)$	Closed-loop transfer function of the SCs current controller $C_3(z)$ with the plant $P_3(z)$.
$\|\|T_3(z)\|\|_\infty$	∞-norm of the closed-loop transfer function of the SCs current controller $C_3(z)$ with the plant $P_3(z)$.
w	Auxiliary variable used in the modeling of the APU .

Global power balance control

Global power balance control - Plant modeling

B	Amplitude of the step disturbance around $i_{fc_{ss}}^{\text{ref}}$.
$h(t)$	Heaviside step function.
i_{ss}^{hvs}	Steady-state current at the high-voltage side of the step-up stage.
$i_{fc_{ss}}$	Steady-state current delivered by the FC unit .
i_{fc}^{ref}	Input current controller reference .
$i_{fc_{ss}}^{\text{ref}}$	Steady-state input current controller reference.
$\tilde{i}_{fc}$	Input current variation around $i_{fc_{ss}}$.
i_{sc}^{ref}	Reference delivered to the SCs current controller.
$p_{fc_{ss}}$	Steady-state power delivered by the FC unit .
p_{ss}^{hvs}	Steady-state power at the high-voltage side of the step-up stage.
$p_{loss_{ss}}$	Steady-state power losses in the system .
v_{ss}^{hvs}	Steady-state voltage at the high-voltage side of the step-up stage.
$\tilde{v}^{\text{hvs}}$	Output voltage variation around v_{ss}^{hvs}.

Global power balance control - controller

$D_4(z)$	Derivative component of the global power balance controller $C_4(z)$.
$G_4(s)$	Global current reference I^{ref} to high-voltage side v^{hvs} continuous-time transfer function.
$G_4(z)$	Global current reference I^{ref} to high-voltage side v^{hvs} discrete-time transfer function.
GPC_PWR_MAX	Maximum power to be handled by the global power balance controller.
GPC_PWR_MIN	Minimum power to be handled by the global power balance controller.
$I_4(z)$	Integrative component of the global power balance controller $C_4(z)$.
K_{aw_4}	Proportional constant of the anti-windup system for the controller $C_4(z)$.
K_{d_4}	Derivative constant of the global power balance controller $C_4(z)$.
K_{i_4}	Integral constant of the global power balance controller $C_4(z)$.
K_{p_4}	Proportional constant of the global power balance controller $C_4(z)$.
$L_{\text{aw}_4}(z)$	Open-loop transfer function anti-windup system for the controller $C_4(z)$.
$L_4(z)$	Open-loop transfer function of the global power balance controller $C_4(z)$ with the plant $P_4(z)$.
max_v_{sc}	Absolute maximum voltage allowed at the terminals of the bank of SCs.
p^{ref}	Energy conditioning system global power reference.
$P_4(z)$	Plant controlled by the global power balance controller $C_4(z)$.

Global power balance control - controller

$P'_4(z)$	Closed-loop transfer function of the nominal plant $P_4(z)$ with the derivative part of the controller $D_4(z)$.
p_{out}	Power delivered at the output of the dc-ac inversion stage.
PWR_APU_CHRG_MAX	Maximum power allocated to the charge of the bank of SCs.
PWR_APU_MAX	Maximum power to be handled by the auxiliary power unit.
PWR_STP_MAX	Maximum power to be handled by the step-up stage.
$S_4(z)$	Closed-loop sensitivity transfer function of the global power balance controller $C_4(z)$ with the plant $P'_4(z)$.
$\|\|S_4(z)\|\|_\infty$	∞-norm of the closed-loop sensitivity transfer function of the global power balance controller $C_4(z)$ with the plant $P'_4(z)$.
$T_4(z)$	Closed-loop transfer function of the global power balance controller $C_4(z)$ with the plant $P_4(z)$.
$\|\|T_4(z)\|\|_\infty$	∞-norm of the closed-loop transfer function of the global power balance controller $C_4(z)$ with the plant $P_4(z)$.
v_{bus}^{ref}	Dc-bus voltage reference given to the global power balance control loop.
$v_{sc\_cnt\_chr}$	Maximum voltage at which the bank of SCs can be charged with the maximum power rererence PWR_APU_CHRG_MAX.

There is only one good, knowledge,
and one evil, ignorance.

Socrates

Part 1

– Framework –

CHAPTER I

Introduction and State of the Art

The birth of science was the death of superstition.
Thomas Henry Huxley

This Chapter gives an overall overview of the dissertation topics. The basic concepts regarding stand-alone electric energy generation/conditioning systems are discussed. The motivations for the development of this work are presented, the main objectives and the problem definition of the thesis are enounced.

I.1 Background and relevant work

Isolated electric energy generation systems are often needed to supply electric loads where the electrical network is not available. This could be caused due to geographic isolation, the necessity of load mobility, demanded values of voltage and current that are not compatible with the local networks, etc.. This makes the design and construction of stand-alone electric energy generation systems a must.

Modern designs are being pushed towards cleaner and more efficient technologies. The experience has shown that the traditional methods employed to produce electric energy are not sustainable, specially because of environmental concerns. Usual stand-alone energy generation systems employ batteries and fuel engines. Batteries offer a cheap mean to feed the generation system but need rigorous maintenance routines, the substances used in their construction are strong pollutants, offer relatively low durability and the ratio charge time/discharge time is too high. Fuel engines extract their energy from petroleum based fuels, and as its well known, pollute their surrounding environment in several ways producing smoke, noise, heat and having extremely low efficiencies.

Fuel cells (FCs) are among the "new" technologies that are being considered as a good alternative to the traditional power sources used for stand-alone electric energy generation systems (Riera *et al.* [72]). FCs are electrochemical devices that convert chemical energy directly into electrical and thermal energies. In terms of fuel efficiency, the levels reached by such devices usually lies in the range 40 % to 60 % , almost doubling the fuel efficiency of any state of the art diesel or gasoline engine as pointed out by Chau *et al.* [16], Gao *et al.* [32], von Helmolt and Eberle [38] and Van Mierlo *et al.* [93].

Although the basic principles of operation of the FCs have been known for many years, this is a technology that is still far from being mature. The FC effect was discovered by Professor Schönbein back in 1838 and first described in the English language in January 1839 [79]. Similar effects were, shortly thereafter, empirically confirmed and reported by Sir W. R. Grove in February 1839 [34]. Grove continued his experiments and invented the "Gas Voltaic Battery" (GVB), which was in fact, the first operative FC reported [35], using similar materials to the actual phosphoric acid fuel cell (PAFC). A series of thirty experiments over the GVB and detailed descriptions of the experimental results and constructive details are given by Sir W. R. Grove in [36].

At the present moment there are many different types of fuel cells, among the most well known are: Polymer electrolyte membrane (PEM) fuel cells, direct methanol fuel cells (DMFCs), alkaline fuel cells (A-FCs), phosphoric acid fuel cells (PAFCs), molten carbonate fuel cells (MCFCs), and solid oxide fuel cells (SOFCs). One type or another must be chosen depending on the conditions of the target application, such as desired output power, allowed maximum operating temperature, etc..

In order to be able to use FCs as general purpose dc power supplies, the electric energy provided by these devices needs to be conditioned to the levels and characteristics specified by the requirements of the load. In Europe, for monophasic ac loads, the specifications are a sinusoidal output voltage with 230 V ac rms and a frequency of 50 Hz. When this kind of electric energy is demanded from a stand-alone generation system, the system itself is responsible of holding the values and levels of the electrical variables (nominal rms value, frequency and shape of the signal) within their valid operational ranges as mentioned by O'Sullivan [64] and Wang *et al.* [98], even if important changes in the load and nonlinearities are present. This fact implies the use of efficient controllers. The design of these controllers is not a trivial task, due to the complexity of the phenomena involved, and specially due to the strong nonlinearities on the dynamics of the energy conversion systems.

One important consideration that should be made when designing stand-alone electric energy generation systems based on FCs, is that the dynamics of the fuel cell is relatively slow, and therefore the system cannot react rapidly to fast changes in the load. The use of an auxiliary power unit (APU) is mandatory in the system. This unit will store energy and will use it only when sudden excessive power demands are present, quickly supplying the amount of additional energy that the fuel cell is not able to provide. For this purpose, a high-power-density energy storing device must be considered.

Supercapacitors (SCs), have become the preferred choice for supplying these sudden/fast energy requirements in modern low/mid power level (1 kW to 100 kW) designs. This type of capacitors offer characteristics such as very high charge and discharge rates, and little degradation over a high number of charge/discharge cycles which translates in a long lifespan, constituting an interesting and modern technology to be applied. Some examples of their application to support the operation of FC supplied systems are given by Woojin Choi *et al.* in [18] and [19] , Dowgiallo *et al.* [26] and Thounthong *et al.* [90].

I.1.1 Polymer electrolyte membrane fuel cells

Formerly known as solid polymer fuel cells (SPFCs), PEM FCs have surged as attractive sources of electric power, due to their capability of providing clean energy with good levels of reliability and efficiency (Woojin Choi *et al.* [18] and [19]). Among all the different types of FCs available in the market, proton exchange membrane FCs, which are based in a polymeric electrolyte, have a working temperature range, between 80 °C and 100 °C, which constitutes an important advantage over the other types of FCs for near-human interaction applications, such as, automotive and low/mid power level stand-alone electric energy generation systems.

Nevertheless, there are still some shortcomings that limit the use of PEM FCs on a mass-market level, some of which are: The high cost, the use of platinum as catalizer, the CO_2 poisoning and the water management. All these problems encourage the synthesis of new membranes, through the use of new materials, components and configurations. The synthesis of new membranes is one of the main research areas in the field at the present time, some examples of such efforts can be found in Asensio *et al.* [4], Dobrovolsky *et al.* [25], Gómez-Romero *et al.* [33], Kulkarni *et al.* [50] and Leikin *et al.* [53].

On the other hand, more work needs to be done in order to improve the dynamic response and the reliability, to reduce the size, the weight and the cost of the systems; and to improve the air supply system and the management of the heat produced by the electrochemical reaction (Laurencelle *et al.* [52]). By making these improvements, the goal is to make of the PEM FC systems with high reliability, with maximum efficiency and capable of providing electric energy with quality comparable to the quality levels achieved using traditional methods.

Several works have been done regarding the steady-state modeling of the PEM type fuel cell, among these publications are included the contributions made by Amphlett *et al.* in [2] and [3], Hertwig *et al.* [39], Kulikovsky [49] and Springer *et al.* [88]. Recent works have been carried out about the control dynamics of the PEM type fuel cell, among these are the works of Corrêa *et al.* [21] and Pukrushpan *et al.* [70], even though in these models the very fast and very low dynamics are eliminated.

PEM type FCs are the most appropriate for applications in which the electrical charge is highly variable. Under these circumstances good transient behavior is mandatory. PEM FCs have been used to feed highly variable charges of different types, some examples of such applications are present in uninterruptible power supply (UPS) implementations by Woojin Choi *et al.* in [18] and [19]; hybrid generation systems by Dae-Kyu Choi *et al.* [17], Jain and Agarwal [42], Marambeas *et al.* [59] and Xu *et al.* in [100] and [101]; PEM FCs are the most attractive for vehicle propulsion (Panik [65]). For this kind of applications the system must show good start up dynamics and a reasonable durability (Adams *et al.* [1]). Another factor that encourages the use of FCs for this kind of applications is the efficiency, however the efficiency of the PEM FCs is high, the electric vehicle prototypes built and tested up to now, show a much more inferior efficiency than expected as shown by Gao *et al.* [32], Guezennec *et al.* [37] and Helmolt and Eberle [38].

I.1.2 Supercapacitors

Also known as ultracapacitors or double-layer capacitors (Kazimierczuk and Cravens [46]), supercapacitors (SCs) offer high-speed energy transactions due to their high power density, allowing large amounts of energy to be stored or extracted in short periods of time. This is particularly interesting for applications where sporadic short-duration high-power solicitations occur around a certain working point.

SCs owe their high capacitances to the novel materials used in their construction, including carbon-metal composites, aerogel carbon, cellulose-carbon foams, conducting polymers and ruthenium/tantalum oxides (Schempp and Jackson [77]).

The voltage levels handled by individual SC units usually vary between 2 V dc and 3 V dc, actual capacitances can reach levels as high as 5000 F at 2.7 V dc in a package of around 500 cm^3 (Zorpette [109]), one of such SCs can store as much as

$$E_{sc_{max}} = \frac{1}{2} C_{sc} v_{sc_{max}}^2 = 18225 \text{ J}.$$

Nevertheless, in practical applications, the total energy stored is not recoverable owing to several factors. Energy may be lost due to Joule heating in the electrodes and due to internal leakage currents and self discharge. Energy may be unrecoverable due to slow dielectric relaxation and the lowest voltage at which the SCs can be discharged (Schempp and Jackson [77]).

Due to the low voltage levels handled by the SCs, for higher voltage applications, arrays of several SCs connected in series/parallel are needed in order to meet the desired voltage/capacitance requirements. These arrays are called banks of supercapacitors. Schempp and Jackson [77], have worked on the considerations to be made when banks of SCs are needed in the design of a system. For an ideal capacitor the relationship expressed below is used to find the actual usable energy depending on the working voltages of the capacitor,

$$\Delta_{E_{sc}}^{max} = \frac{1}{2} C_{sc} v_{sc_{max}}^2 \left[1 - \frac{v_{sc_{min}}^2}{v_{sc_{max}}^2} \right] = E_{sc_{max}} \left[1 - \frac{v_{sc_{min}}^2}{v_{sc_{max}}^2} \right], \tag{I.1}$$

where $v_{sc_{min}}$ is the lowest voltage at which the supercapacitor is usable and $v_{sc_{max}}$ is the maximum allowed working voltage. The next consideration to take is to make $v_{sc_{max}}$ less than $v_{sc_{Bd}}$ (the breakdown voltage of the SC). It is common practice to set the effective $v_{sc_{max}}$ at 35 % to 50 % of $v_{sc_{Bd}}$.

When a bank of SCs is formed, new problems arise. SCs are very susceptible of suffering a failure due to over voltages. Special care must be taken in order to assure that the maximum applied voltage to the SC does not overpass the $v_{sc_{Bd}}$ value.

Because of the tolerances of the components, it is not easy to guarantee that the voltage applied to a series connection of SCs will be uniformly distributed among all the SC units in the string. To solve this, a voltage balancing system must be implemented, in order to equally spread the voltage applied to the series among all the SC units that form it, reducing in this way the possibilities of a failure caused by a local over voltage.

Basically, there are two families of voltage balancing circuits used when series connections of SCs are implemented, these are passive voltage balancing and active voltage balancing circuits. In the case of passive voltage balancing, the series string requires the installation of voltage balancing or "bleeding" resistors in parallel with each SC. The resistances values must be low enough to maintain protection during transients, but it also must be considered that the parallel resistors increase the net self discharge and reduce the round trip efficiency (Schempp and Jackson [77]).

In the case of active balancing being used, a more complex circuitry is added in parallel to each SC. The word "active" means that active components are being used, meaning that an over voltage control circuit is implemented for each SC. This approach does not increases the self discharge resistance of the series, improving the energy storage in each of the SCs used in the series, but having a higher economical cost.

I.1.3 Dc-ac power inversion and conditioning

Dc-ac power inversion and conditioning are two of the most important and active areas in power electronics. It is important to make a distinction between dc-ac power inversion and dc-ac power conditioning. In general, in the literature, the term "dc-ac power inverter" usually refers to the hardware topology used to achieve such task. Nevertheless, the term "dc-ac power conditioner" refers to a hardware topology together with a control strategy designed to accomplish the desired output voltage/current shapes.

The dc-ac inversion scheme to be used in a particular application depends on the restrictions imposed by the topology of the system. Dc-ac power inverters used in single-phase photo voltaic (PV) modules are generally required to provide good power decoupling between the PV modules and the grid. In small wind generation systems, the inverter must be able to handle large input voltage variations, etc..

There are essentially two big categories in which dc-ac inverters can be classified, these are: Single-stage dc-ac inverters and multiple-stage dc-ac inverters (Yaosuo Xue *et al.* [102]). On one hand, single-stage inverters consist, of only one power conversion stage for both, stepping-up the input voltage and modulating the output to have a sinusoidal voltage or current shape. On the other hand, multiple-stage inverters make use of several intermediate stages for stepping-up the input voltage and modulating the output voltage/current.

Single-stage dc-ac power inverters

In general, single-stage dc-ac power inverters (SSPIs) offer simple structure and low cost, but suffer from a limited range of input voltage variations and are often characterized by compromised system performance (Yaosuo Xue *et al.* [102]). Moreover, the advantages offered by these converters are compensated by the necessity of more elaborated and sophisticated controllers.

The general SSPI block diagram is presented in Fig. I.1. An analysis of several SSPI topologies has been performed by Yaosuo Xue *et al.* [102], some of the analyzed topologies can be found in the work of Cáceres and Barbi [14], Kasa *et al.* [45], Kjær and Blaabjerg [48], Kusakawa *et al.* [51], Myrzik [62], Nagao and Harada [63], Vázquez *et al.* [95] and Wang [97].

Differential converters as the presented in [14] and [95] have attracted the attention from the control theory community for a few years. It is interesting to note that, even though it is relatively easy to follow a sinusoidal reference with an offset, as in each individual boost converter in [14], the solution of the problem is not trivial when the load is differentially connected. The system does not behave as one may suppose when looking at the operation of each individual boost dc-dc converter alone, and the performance degrades even more when the load to be fed is nonlinear.

In order to achieve good sinusoidal output in differential dc-ac inverters many authors have worked on the tracking problem for different structures like the boost or the buck-boost dc-dc power converter. Papers in this area include the publications made by: Cortés *et al.* [22], Sira-Ramírez *et al.* in [84] and [85], and others. In these publications good tracking is achieved for a single boost dc-dc converter, yet good tracking when the converters are integrated into the differential output structure is not maintained. Other authors try to eliminate the system's non-minimum phase zero, which is the reason why good tracking cannot be attained in those systems, in this category can be found the work of Calvente *et al.* [15], in which a unidirectional boost converter is modified by the addition of an output filter where the input inductance and the filter inductance are magnetically coupled, by doing this they deduce the relationship between these two coils and demonstrate that with the appropriate selection of the component values, the converter can be designed to be minimum phase.

Sanchis *et al.* have used a dual-loop control technique over the differential boost converter scheme [75], introduced by Cáceres and Barbi [14], obtaining a good 220 V ac rms 50 Hz zero-offset differential output voltage. The authors have also adapted this control approach and applied it to the differential buck-boost inverter [76], initially presented by Vázquez *et al.* in [95], getting in this case a good 125 V ac rms 60 Hz zero-offset differential output voltage. Nevertheless these results, the use of differential boost or buck-boost converters is usually compromised by a limited allowed input voltage variations range. In addition, working with high conversion ratios in such systems imply duty cycle levels near to the saturation values. Under these circumstances, the conversion efficiency of such systems also becomes a concern.

All these complications make the use of SSPIs, however they are economically attractive, difficult to implement and therefore encourage the use of other configurations such as the multiple-stage topologies.

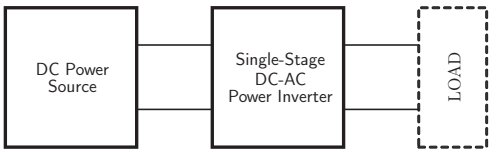


Figure I.1: Single-stage dc-ac power inverter (SSPI) block diagram.

Multiple-stage dc-ac power inverters

Multiple-stage dc-ac power inverters (MSPIs) offer advantages such as wide input voltage range and high reliability. The different stages can be independently controlled, obtaining, in general, systems that are easier to control. An evidence of these facts is that MSPIs are typically used in industry applications, where the ease of control and a high level of reliability are the most important criteria. The disadvantages include a higher cost, a more complex structure and usually lower efficiency levels than the achieved using single-stage dc-ac power inverters.

Multiple-stage dc-ac power inverters can be classified as dc-dc-ac, dc-ac-dc-ac and dc-ac-ac inverters according to the intermediate conversion stages used (Yaosuo Xue *et al.* [102]). The first category, the dc-dc-ac is the most well known. Several examples of this class of MSPIs can be found in industrial applications as well as in the literature, among them can be found the contributions made by Chomsuwan *et al.* [20], Funabiki *et al.* [31], Kang *et al.* [44], Kjær and Blaabjerg [47], Saha and Sundarsingh [74], Shimizu *et al.* [83] and Yang and Sen [103].

Dc-dc-ac MSPIs use a dc-dc step-up stage (which could be formed by one or various converters) to boost the input voltage. The voltage provided by the output of the step-up stage is fed to an intermediate dc bus, where usually a filtering capacitor is connected, from which the dc-ac inversion stage is fed. Fig. I.2 shows the typical configuration of a dc-dc-ac MSPI.

The overall efficiency of a MSPI can be improved by taking care of the efficiency of each of the intermediate stages, in the case of dc-dc-ac MSPIs the step-up stage and the dc-ac inversion stage. Efficiency becomes a major concern specially if high conversion ratios are demanded from a boost type converter. In these cases, it is desirable to have a high-gain high-efficiency topology to be used in the step-up stage of the inverter.

Recently, a new family of high-conversion-ratio topologies has been developed by Zhao *et al.* and presented in [105], [106], [107] and [108]. These converter topologies take advantage of the energy that is usually lost in common converters, recycling and redirecting it to the output through a magnetic path, and therefore, getting a higher level of output voltage. Moreover, the efficiencies reached by this type of converters are considerably high, and as a consequence, by using this type of dc-dc power converters the overall efficiency of a multiple-stage inverter can be improved. All this is achieved by using a single switch and a total component count that is reduced compared to other high-gain topologies.

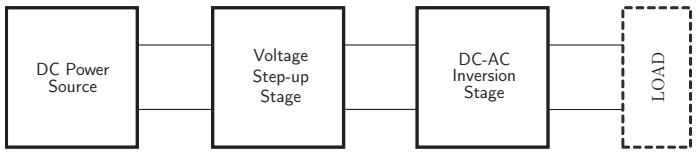


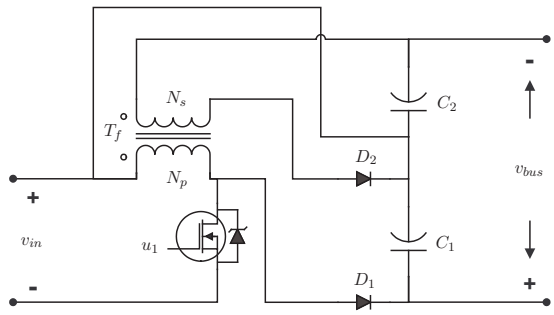
Figure I.2: Dc-dc-ac multiple-stage dc-ac power inverter (MSPI) block diagram. Usual configuration.

Four different high-gain coupled-inductor converter topologies are presented in Fig. I.3. Figs. I.3(a) and I.3(b) show two topological variations of the high-gain coupled-inductor buck-boost converter. The topology presented in Fig. I.3(a) was introduced by Zhao and Lee in [106], and the converter presented in Fig. I.3(b) has been analyzed by Zhao *et al.* in [107] and Zhao and Lee in [105]. Figs. I.3(c) and I.3(d) show two topological variations of the high-gain coupled-inductor boost converter. The converter presented in Fig. I.3(c) was introduced and analyzed by Zhao and Lee in [106]. The variation of Fig. I.3(d) was introduced by the authors in [105]. Latter, an extensive analysis over the eight topological variations of the high-gain coupled-inductor boost converter and their influence in the dimensioning of the components was performed by Van de Sype *et al.* [92].

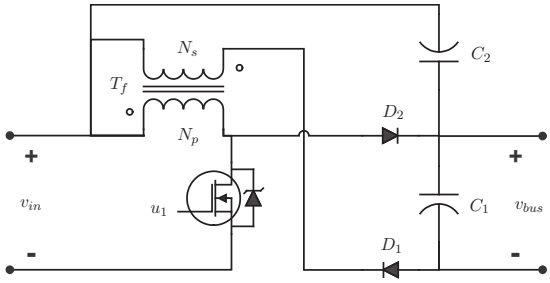
All these converters provide a non-isolated interconnection between the dc power source and the load. This is specially attractive for off-grid electric energy generation systems, where there is no need for galvanic isolation between the input and output ports. The topologies presented are current unidirectional, which is interesting for applications where current unidirectional power sources are used. The high-gain characteristics of these converters make them attractive to be used in applications where high output voltages are required when the voltage sources can provide only low voltages. Also, the high efficiency levels achieved using these converters make them appealing for applications where the efficiency is a major concern.

All these characteristics make this family of converters suitable for stand-alone electric energy generation systems based on FCs. The high-gain characteristic is necessary due to the low voltages handled by these devices. Current unidirectional converters are needed because, in this way, the FC unit is protected against reverse current flows which may damage it. Also, the use of high-efficiency converters is mandatory for this kind of applications.

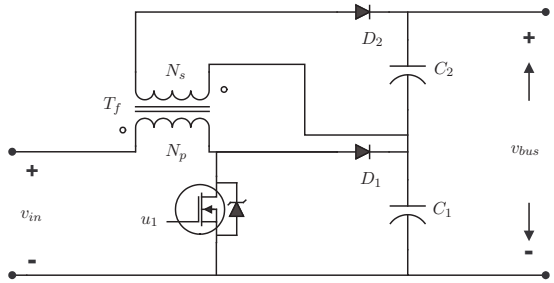
The last module where the efficiency can be improved in a multiple-stage inverter is the dc-ac inversion stage itself. Divan [24], has analyzed the most popular configurations in dc-ac conversion systems. According to Divan these topologies can be grouped in three categories, depending on application and design specifications, the configurations are classified under the following classes: Pulse-width modulated (PWM) inverters, soft switching inverters and high-frequency link inverters.



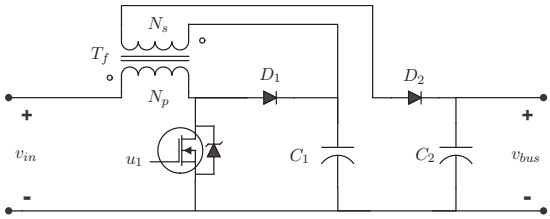
(a) High-gain coupled-inductor buck-boost converter, Zhao and Lee [106].



(b) High-gain buck-boost converter, Zhao and Lee [105] and Zhao *et al.* [107].



(c) High-gain coupled-inductor boost converter, Zhao and Lee [106].



(d) High-gain coupled-inductor boost converter, Van de Sype *et al.* [92] and Zhao and Lee [105].

Figure I.3: High-gain coupled-inductor converter topologies.

In the case of single-phase systems, the most obvious and popular configurations are the half-bridge and the full-bridge inverters, and in the case of three-phase systems, the inverter topology most frequently used is the PWM voltage source inverter. Although, in general, the most usual implementation for single-phase as well as for three-phase power inverters is carried out by means of PWM inverters, these inverters have important switching losses, acoustic noise and electro-magnetic interference (EMI) problems, offering at the same time, easy to implement and low-cost structures.

Soft switching inverters have the advantages of low switching loss, low EMI, silent operation and small reactive components. Although the spectral characteristics of discrete pulse modulated systems are significantly different from their PWM counterparts, it has been shown that typical resonant DC link systems are capable of substantially better performance than their hard switched counterparts (Divan [24]), yet their implementation complexity and cost are considerably higher.

Auxiliary power unit (APU)

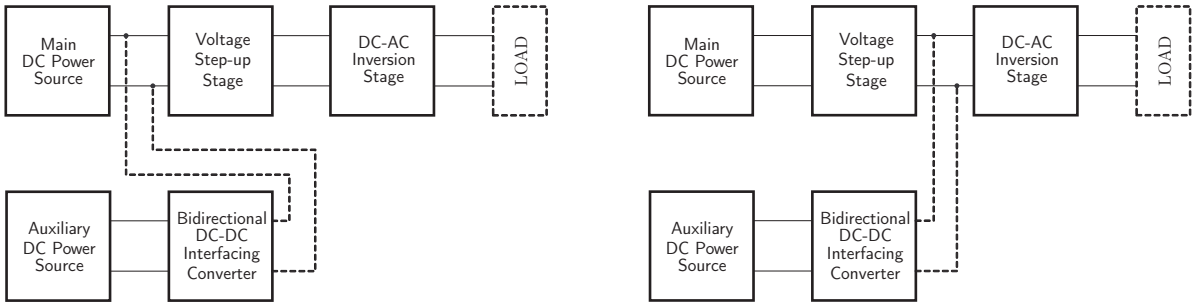
In the basic SSPI and MSPI topologies (see Figs. I.1 and I.2) the dc power source and conversion stages must be able to handle all the possible power solicitations that present at the load side. This can be achieved by dimensioning the dc power supply and the components used in the converters to operate at the absolute maximum power rating of the application. In order to take the maximum profit from the dc-ac inversion system, the use of this criteria is correct if the behavior of the load to be connected at the output of the inverter is known to have steady power solicitations near the maximum power specification.

Nevertheless, there are applications where momentary high output power demands can be experienced. The use of this criteria in such cases translates in an over dimensioning of the dc power supply and the converters used, and therefore, in an unrequired extra cost in the design of the system. It is necessary then to dimension the dc power source and the components used to the minimum size possible, but at the same time, the system must be able to handle the expected sudden high power requirements.

Moreover, the response speed of a system is limited by the slowest element in the chain. Fuel cells for example, have response speeds that are relatively slow for their use in some electrical systems. Certain conditions such as step load changes and/or pulsed power solicitations require a quick reaction from the power source being used. Although, these power requests can lie within the power specifications of a FC unit, the response speed needed can be beyond the bandwidth that the FC is able to provide.

In order to cope with these problems on dc-ac inverters, one possible solution is the addition of an auxiliary power unit (APU) to the system. The APU is a device that stores energy and uses it only when sudden/fast and/or excessive power demands (above the nominal value) are present, supplying the amount of additional energy that the dc power source is not able to provide. APUs can be used to improve the dynamic behavior of dc-ac inversion systems as well. As mentioned before, FCs have relatively slow responses when used as the main power source in electrical applications. The use of an APU to satisfy the fast power solicitations widens the overall bandwidth of the dc-ac inversion system, and lightens the stress applied over the FC.

An APU is formed by an energy-storing device and an interfacing converter which allows the interaction between the energy-storing unit and the dc-ac inversion system. In the APU design there are certain considerations that should be taken. The energy-storing component to be used is determined by the amount of energy to be accumulated/supplied as well as by the required response speed needed for the application. For fast energy transferences high-power-density devices such as SCs are needed. For long-duration overload supply, high-energy-density devices such as batteries are required. The combined use of high-power-density and high-energy-density devices is complementary. If used in combination, batteries can supply the extra energy demanded by long-duration overload power needs. On the other hand, SCs can be used to supply the fast/pulsed power demands, reducing the stress applied over the batteries, and therefore, extending their lifetime (Bauman and Kazerani [6]). This is the same case for applications that use FCs as the main power source, where the use of APUs with SCs as the energy-storing device has become almost a standard.



(a) MSPI with APU connected at the low-voltage side.

(b) MSPI with APU connected at the high-voltage side.

Figure I.4: Usual MSPI and APU interconnection topologies.

Besides the energy storage unit, there are other aspects that must be taken into account while designing an APU, one of these is the interconnection between the APU and the rest of the system. In practice, almost all the APU implementations are performed over MSPIs because they have a clear separation between the input stage, dc-dc elevation stage and the dc-ac inversion/output stage.

An analysis over various interconnection configurations of MSPIs and APUs for distributed generation (DG) systems was performed by Cacciato *et al.* in [13]. In this case SCs were selected as the energy-storing device. The authors identify two generalized interfacing schemes between the APU and the dc-ac power inverter, the series connection and the parallel connection. Under the series connection, full discharge of the bank of SCs is allowed, taking full advantage of the energy stored in the SCs, although this is not a usual configuration due to the filtering behavior of the SCs. On the contrary, the parallel connection does not allow the full discharge of the supercapacitor bank due to the limited gain of the dc-dc interfacing converter, but offer other advantages such as efficiency maximization and current harmonics compensation [13].

From the interconnection schemes between APUs and MSPIs explained before, the parallel connection prevails in the specialized literature. Fig. I.4 shows the parallel APU and MSPI interconnection schemes. Fig. I.4(a) shows the interconnection of the APU to the low voltage side of the MSPI. The parallel interconnection of the APU to the high voltage side of the MSPI is shown in Fig. I.4(b).

The APU/MSPI interconnection topologies presented in Figs. I.4(a) and I.4(b) have been widely used in the literature. The scheme presented in Figs. I.4(b) is the most well-known and used. Some examples of implementations of APUs using this architecture can be found in the work of Rufer and Barrade [73] for the energy manangement in an elevator application; Jain and Agarwal [42] on hybrid energy conversion systems; various energy conditioning and UPS systems applications by Cacciato *et al.* [13], Dae-Kyu Choi *et al.* [17], Woojin Choi *et al.* in [18] and [19], Marambeas *et al.* [59], Schenck *et al.* [78], Xu *et al.* in [100] and [101]; automotive applications by Bauman and Kazerani [6], Bertoni *et al.* [7], Gao *et al.* [32], Schupbach *et al.* in [80] and [81],

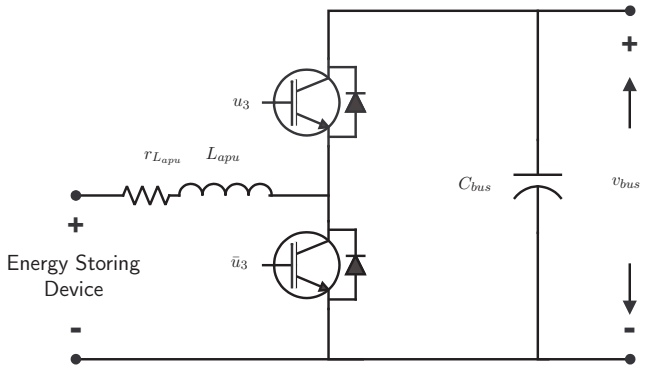


Figure I.5: Common APU interfacing converter.

Thounthong *et al.* in [89] and [90], and Yuwen *et al.* in [104]. The interconnection architecture presented in Fig. I.4(a) is less used, one example of its utilization on automotive applications can be found in Drolia *et al.* [28].

The scarce use of the topology presented in Fig. I.4(a) obeys, mainly, to safety and efficiency considerations. Most of the applications cited above use FCs as the main power source. Installing the APU at the low voltage side (*i.e.* in parallel with the FC), opens the possibility to accidentally injecting a reverse current, and eventually damaging the FC. The efficiency of the APU is also a concern, using the structure of Fig. I.4(b) instead, translates in less losses when the energy flows from the APU to the load, therefore allowing smaller energy-storing devices.

In general, regardless the APU and MSPI interconnection scheme used, bidirectional dc-dc converters are needed to interface the energy-storing device with the dc-ac inverter. The energy must be able to flow from the energy-storing device to the MSPI in order to cope with the overloads and/or the fast or pulsed energy requirements of the load.

The reverse energy flow is also necessary mainly due to two reasons. First, to be able to recharge the energy-storing unit after it has been depleted by an overload condition. Second, the APU must be able to deal with the parasitic losses in the storing components, this is necessary in order to guarantee a desired state of charge of the energy-storing device used in the APU.

The selection of the interfacing converter is a crucial step in the development of the APU. Its characteristics help to determine the energy-storage device to be used, its size and maximum/minumum operational conditions. An analysis of various bidirectional dc-dc converter topologies for their use in APU applications has been performed by Schupbach *et al.* in [80]. In this case the APU is designed to support the operation of an stand-alone energy generation system using a FC as main power source for automotive applications. The chosen topology is presented in Fig. I.5. This interfacing converter has been widely used in the literature and some examples of its use can be found in the work of Bertoni *et al.* [7], Woojin Choi *et al.* in [18] and [19], Drolia *et al.* [28], Schupbach *et al.* [81], and Thounthong *et al.* in [89] and [90].

I.2 Objectives

The main objective of the thesis is the analysis, design, construction, and control of the electric energy conditioning system for a PEM type fuel cell to act as an stand-alone dc-ac inverter to feed general (linear, nonlinear, dynamic) loads with big variations. The following sub-objectives must be accomplished:

- To study and evaluate the different topological alternatives for the electronic conditioning system and the selection of the most appropriate.
- Modeling of all the conditioning system's elements taking into account the dynamic response of the PEM type fuel cell.
- Digital control law design and implementation to comply with the design and operation specifications.
- Prototype construction and experimentation using the designed control laws.

I.2.1 System specifications

The designed electric energy conditioning system complies with the following specifications:

- Input:
  - Input voltage: 24 to 46 V dc depending on load condition.
  - Maximum power: 1 kW.
- Output:
  - Output voltage: 230 V ac rms.
  - Frequency: 50 Hz.
  - Nominal active output power: 1 kW.
  - Overload condition:
    - Maximum output power: 5 kVA.
    - Maximum active output power: 3 kW.
    - Maximum overload support time (at 5 kVA): 45 s.
  - Maximum output voltage total harmonic distortion (THD_v^{max}): 3 %.

I.3 Outline of the thesis

The thesis document has the following structure:

- Chapter I presents the state of the art in dc-ac conditioning systems fed by fuel cells. The basic concepts regarding fuel cells, supercapacitors, dc-ac inversion and conditioning systems and auxiliary power units are introduced. Also the objectives of the thesis are stated and the specifications of the system are enounced.

- Chapter II gives a description of the stand-alone dc-ac energy conditioning system. The general block diagram of the design is presented. The converters used in each module are presented and the control objectives are stated.

- Chapter III develops the input current regulation control scheme. A methodology to obtain a model of the converter suitable for control purposes is given. The control design and simulation results are also presented.

- Chapter IV presents the control scheme used to control the full-bridge dc-ac inverter. An analysis is performed over the control scheme used. The control design procedure and simulation results are presented.

- Chapter V describes the current regulation control scheme for the bank of supercapacitors used in the auxiliary power unit. The methodology used to obtain a model of the converter suitable for control purposes is presented. The control design and simulation results are also presented.

- Chapter VI shows the control methodology used to achieve voltage regulation at the dc bus of the dc-ac inversion topology. The power/bandwidth limitations of the devices that form the conditioning system are considered, by doing so, the global power balance controller is developed.

- Chapter VII describes the hardware/software implementation difficulties and considerations found while the stand-alone energy conditioning system was being build.

- Chapter VIII presents the set of tests performed over the experimental setup and the results obtained.

- Chapter IX concludes the thesis and the main contributions of this thesis are presented. Also, suggestions of some possible future lines of research are given based in the obtained results and experience.

CHAPTER II

Fuel-Cell Electric Energy Conditioning System Overview

One no longer loves one's knowledge enough
when one has communicated it.
Friedrich Nietzsche

In this Chapter the chosen architecture of the electric energy conditioning system is explained. The converters used in each conversion stage are presented. The considerations regarding the dimensioning of their components are stated. A general explanation of the control schemes used and the variables to control under each control scenario is given.

II.1 Conditioning system hardware architecture

The general block diagram of the energy conditioning architecture used is presented in Fig. II.1 as introduced in [55]. The scheme is based on a multiple stage inverter configuration, due to reliability considerations and ease of control. The system is fed by a PEM type FC, which for design purposes can be considered as a unidirectional current power supply, with certain specific voltage and current characteristics.

The FC unit feeds a voltage step-up stage, which elevates the input voltage and provides a regulated output voltage at the dc bus that feeds the dc-ac inversion stage. The dc-ac inversion stage has a full-bridge configuration, this stage must be able to feed linear and nonlinear loads while keeping the desired output voltage characteristics within the design specifications.

A bank of SCs is used as an energy storing unit for temporary overloads. Its purpose is to supply the extra energy that the step-up stage is not able to provide (up to 2 kW extra active power for 45 s, for a total of 3 kW at the ac load side) during the overload condition.

A current bidirectional dc-dc power converter is included to act as interface the bank of SCs and the dc bus. This power converter acts as a boost converter when the energy flows from the SCs to the dc bus (overload mode), and as a buck converter when the energy flows from the dc bus to the SCs (charging mode).

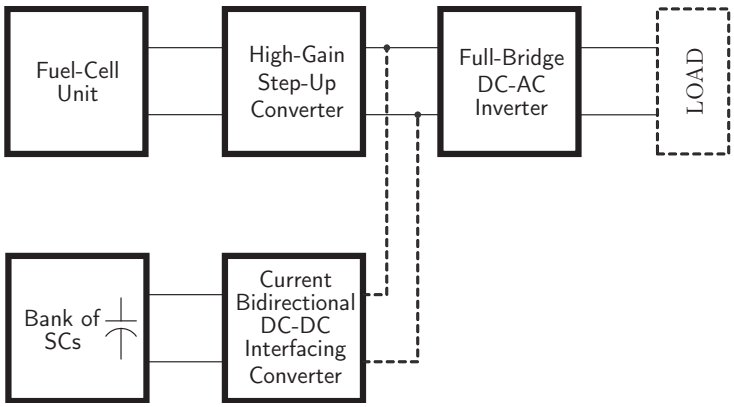


Figure II.1: General block diagram of the electric energy conditioning system.

II.1.1 Fuel-cell unit

A Ballard MAN5100078 PEM type FC stack has been chosen as the nominal power source. At 1 kW output power, the MAN5100078 provides about 30 V dc according to the product specifications [5]. PEM fuel cells exhibit high variations on their output voltages depending on the power demand. Fig. II.2 shows the polarization and power curves for the MAN5100078 as a function of the output current. As can be seen, the output voltage of the fuel cell presents high variations, going from around 24 V dc at full load condition to 46 V dc when the fuel-cell stack is in idle mode. Because of the parasitic losses in the system, the actual input voltage range varies from 24 to 36 V dc.

II.1.2 Step-up stage

As mentioned before, the step-up stage is in charge of elevating the voltage delivered by the FC unit (in the range of the tens of volts), to the level needed by the dc-ac inversion stage (in the range of the hundreds of volts). Because of the conversion requirements, the need of a high step-up dc-dc converter is implicit in the statement of the problem. It has to be taken into account that, when high conversion ratios are demanded, the efficiency of the energy conversion system becomes one of the main concerns in the design. From the high-efficiency, high-gain dc-dc conversion topologies introduced in Section I.1.3, the topology initially presented by Zhao *et al.* in [106] has been chosen to be used in the step-up conversion stage. This is a current unidirectional converter topology, and therefore, the power can only be extracted and no injected to the FC unit by the operation of this converter. The desired input/output requirements for this conversion stage are:

- Input:
  - Input voltage: variable from 24 to 36 V dc, depending on the load condition.
  - Maximum power: 1 kW.
- Output:
  - Output voltage: 425 V dc.

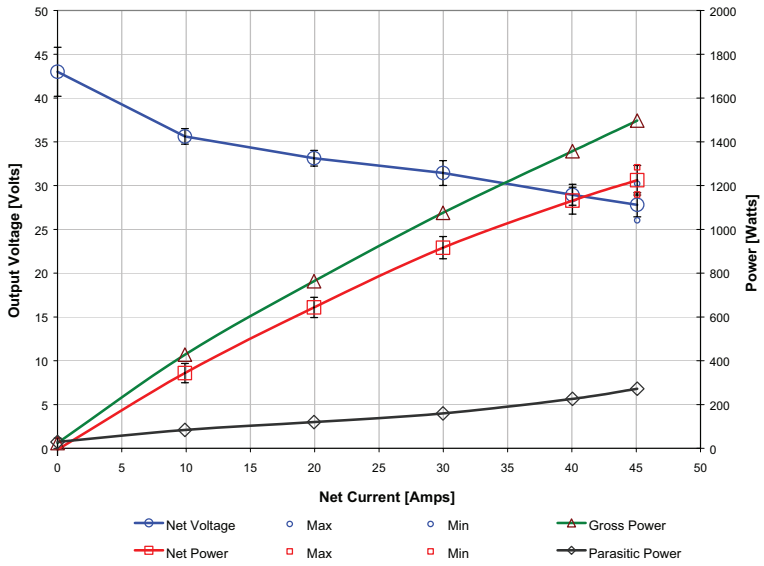


Figure II.2: Ballard MAN5100078 power and polarization curves [5].

The maximum power condition of the step-up stage is determined by the maximum power that can be provided by the FC unit, in this case 1 kW at 24 V dc. Considering the worst case scenario for this application, the step-up stage must be capable of elevating the output voltage from 24 V dc up to 425 V dc to feed the dc-ac voltage inversion stage, and therefore a maximum voltage elevation ratio of around 1 to 18 is required.

Fig. II.3 shows the chosen step-up topology [106], along with the current and voltage polarity definitions to be used on the Kirchoff analysis of the circuit.

Transformer model

The transformer used in the converter of Fig. II.3 has been modeled following the scheme presented in Fig. II.4. The total fluxes going through the primary and secondary windings can be expressed as:

$$\Phi_1 = \Phi_{i_1} + \Phi_{\sigma_{i_1}} + \Phi_{i_2}, \tag{II.1}$$

$$\Phi_2 = \Phi_{i_2} + \Phi_{\sigma_{i_2}} + \Phi_{i_1}, \tag{II.2}$$

where Φ_{i_1}, Φ_{i_2} are the effective fluxes, and $\Phi_{\sigma_{i_1}}$, $\Phi_{\sigma_{i_2}}$ are the loss fluxes induced by currents i_1 and i_2 respectively. Fluxes $\Phi_{\sigma_{i_1}}$, $\Phi_{\sigma_{i_2}}$ do not travel inside the core from one winding to the other, and therefore, their energy contribution is lost. By recalling the flux linkage concept we have that $N\,\Phi = L\,i$ for a single coil, where N is the number of turns, Φ is the flux and L is the inductance of the coil. By multiplying the flux going through each winding by its respective number of turns, the flux linkages of each coil can be found, obtaining

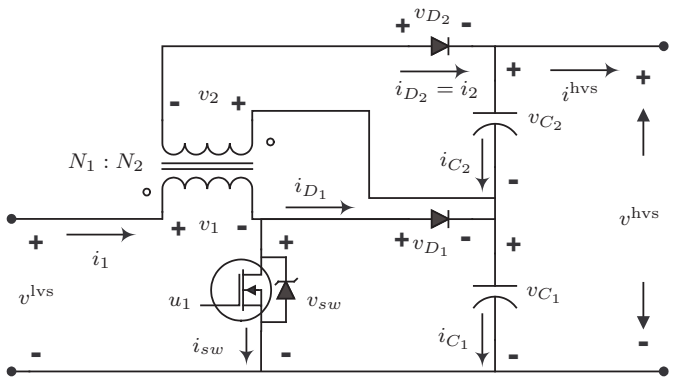


Figure II.3: High-gain, high-efficiency, coupled-inductor dc-dc power converter topology used on the step-up stage [106].

$$N_1\,\Phi_1 = N_1\,\Phi_{i_1} + N_1\,\Phi_{\sigma_{i_1}} + (N_1\,/N_2\,)\,N_2\,\Phi_{i_2}, \tag{II.3}$$
$$N_2\,\Phi_2 = N_2\,\Phi_{i_2} + N_2\,\Phi_{\sigma_{i_2}} + (N_2\,/N_1\,)\,N_1\,\Phi_{i_1}, \tag{II.4}$$

by replacing the quantities above by their current/inductance equivalents through the use of the flux linkage relationships, the following current/total flux linkage is found

$$\lambda_1 = L_{11}\,i_1 + L_{\sigma_1}\,i_1 + (N_1\,/N_2\,)\,L_{22}\,i_2, \tag{II.5}$$
$$\lambda_2 = L_{22}\,i_2 + L_{\sigma_2}\,i_2 + (N_2\,/N_1\,)\,L_{11}\,i_1, \tag{II.6}$$

where L_{11}, L_{22} are the effective winding inductances and L_{σ_1}, L_{σ_2} are the loss inductances of the primary and secondary windings respectively. By assuming that the core of the transformer is an homogeneous medium with constant permeability, it can be proved that $M = (N_1\,/N_2\,)\,L_{22} = (N_2\,/N_1\,)\,L_{11}$. And therefore the dynamics of the transformer can be rewritten as:

$$\lambda_1 = L_1\,i_1 \quad + \quad M\,i_2, \tag{II.7}$$
$$\lambda_2 = M\,i_1 \quad + \quad L_2\,i_2, \tag{II.8}$$

where L_1 and L_2 are the primary and secondary inductances seen at the transformer terminals, and M is called the coupling inductance. By differentiating the equations above, the dynamics of the transformer in terms of the voltages at the terminals of the coils and the currents in the conductors are found

$$v_1 = L_1\,\frac{d\,i_1}{dt} \quad + \quad M\,\frac{d\,i_2}{dt}, \tag{II.9}$$
$$v_2 = M\,\frac{d\,i_1}{dt} \quad + \quad L_2\,\frac{d\,i_2}{dt}. \tag{II.10}$$

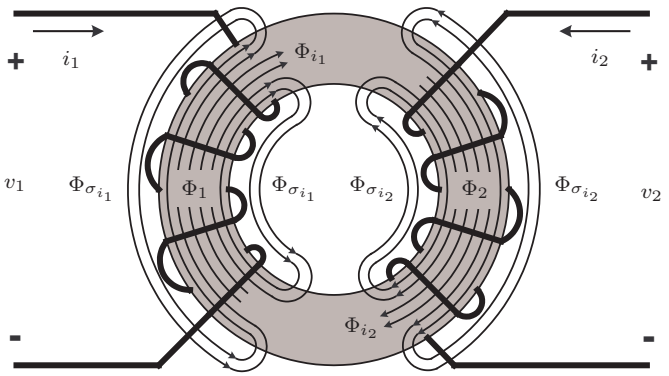


Figure II.4: Magnetic flux inside a two windings, toroidal transformer.

Kirchoff analysis and topological variations

By performing the current Kirchoff analysis at the nodes of the circuit of Fig. II.3, the relationships

$$i_1 - i_{D_1} - i_{sw} = 0, \tag{II.11}$$
$$i_{C_1} - i_{D_1} + i^{\text{hvs}} = 0, \tag{II.12}$$
$$i_{C_2} - i_{D_2} + i^{\text{hvs}} = 0, \tag{II.13}$$
$$-i_{D_1} + i_{D_2} + i_{C_1} - i_{C_2} = 0, \tag{II.14}$$

are obtained.

The voltage relationships

$$v^{\text{lvs}} - v_{r_{L1}} - v_1 - v_{sw} = 0, \tag{II.15}$$
$$v_{sw} - v_{D_1} - v_{C_1} = 0, \tag{II.16}$$
$$v_2 + v_{r_{L_2}} + v_{D_2} + v_{C_2} = 0, \tag{II.17}$$
$$v^{\text{hvs}} - v_{C_1} - v_{C_2} = 0, \tag{II.18}$$

are obtained by applying the Kirchoff voltage analysis over the circuit of Fig. II.3.

The dynamics of the capacitors connected at the output of the circuit are expressed by

$$i_{C_1} = C_1 \frac{d\, v_{C_1}}{dt}, \tag{II.19}$$
$$i_{C_2} = C_2 \frac{d\, v_{C_2}}{dt}, \tag{II.20}$$
$$i^{\text{hvs}} = \frac{v_{C_1} + v_{C_2}}{R_{ld}}, \tag{II.21}$$

assuming a resistive load R_{ld} connected at the output of the step-up converter.

The general dynamics of the converter of Fig. II.3 can be expressed by the system

$$\dot{x} = A_x\, x + A_v\, v + E\, v^{\text{lvs}}, \tag{II.22}$$

with

$$A_x = \begin{bmatrix} -a_1\, r_{L_1} & a_2\, r_{L_2} & -a_1 & a_2 \\ a_2\, r_{L_1} & -a_3\, r_{L_2} & a_2 & -a_3 \\ 0 & 0 & -\frac{1}{R_{ld}\, C1} & -\frac{1}{R_{ld}\, C1} \\ 0 & 0 & -\frac{1}{R_{ld}\, C1} & -\frac{1}{R_{ld}\, C1} \end{bmatrix}; A_v = \begin{bmatrix} -a_1 & a_2 & 0 & 0 \\ a_2 & -a_3 & 0 & 0 \\ 0 & 0 & -\frac{1}{C1} & 0 \\ 0 & 0 & 0 & -\frac{1}{C1} \end{bmatrix}; E = \begin{bmatrix} a_1 \\ -a_2 \\ 0 \\ 0 \end{bmatrix}$$

and

$$a_1 = \frac{L_2}{L_1\, L_2 - M^2}, a_2 = \frac{M}{L_1\, L_2 - M^2}, a_3 = \frac{L_1}{L_1\, L_2 - M^2}. \tag{II.23}$$

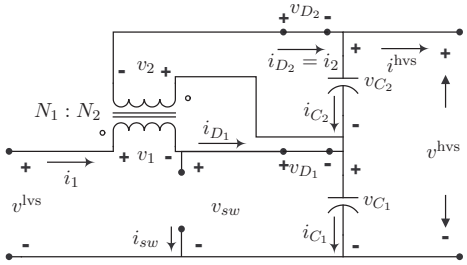
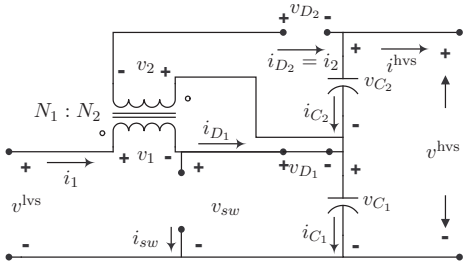
Therefore, the original inductance values can be recovered by

$$L_1 = \frac{a_3}{a_1\, a_3 - {a_2}^2}, L_2 = \frac{a_1}{a_1\, a_3 - {a_2}^2}, M = \frac{a_2}{a_1\, a_3 - {a_2}^2}. \tag{II.24}$$

where $x = [i_1, i_2, v_{C_1}, v_{C_2}]^T$. i_1 is the current at the primary winding of the transformer. i_2 is the current at the secondary winding of the transformer. v_{C_1} is the voltage of the output capacitor C_1, and v_{C_2} is the voltage of the output capacitor C_2. The parasitic resistances of the primary and secondary windings are r_{L_1} and r_{L_2} respectively. The vector $v = [v_{D_1}, v_{D_2}, i_{D_1}, i_{D_2}]^T$, where v_{D_1}, v_{D_2} are the voltages at the terminals of diodes D_1 and D_2 respectively, and i_{D_1} and i_{D_2} are their respective currents.

As this converter is to be operated by applying PWM over the commanded switch u_1 it is interesting to perform an analysis of the topological variations that the circuit of Fig. II.3 can take during a switching period. The commanded switch u_1, and diodes, D_1 and D_2 are considered as ideal switches. This means that, there is a null voltage drop across the switch if it is conducting (ON state), and an open circuit when the switch is open (OFF state). For the diodes, it is stated that the currents i_{D_1} and i_{D_2} can be only positive if the diodes are under conduction mode.

Taking the previous assumptions into account, the system can take up to eight different topological variations according to the conduction state of the commanded switch u_1, and the free-wheeling diodes D_1, D_2. Tables II.1 and II.2 show the different topological configurations/-operating modes that the converter of Fig. II.3 can take if the switch u_1 is in the OFF or ON positions, respectively.

<table>
<tr>
<td>Topological state (a):
 
</td>
<td>u_1 is OFF
D_1 is ON $\Big\}\Rightarrow$ $i_{D_1} = x_1$, $v_{D_1} = 0$
D_2 is ON $\Rightarrow$ $i_{D_2} = x_2$, $v_{D_2} = 0$
The system can be expressed as $\dot{x} = A\,x + B\,v^{\text{lvs}}$, with
$\text{A}=\begin{bmatrix} -a_1\,r_{L_1} & a_2\,r_{L_2} & -a_1 & a_2 \\ a_2\,r_{L_1} & -a_3\,r_{L_2} & a_2 & -a_3 \\ \frac{1}{C_1} & 0 & -\frac{1}{R_{ld}\,C_1} & -\frac{1}{R_{ld}\,C_1} \\ 0 & \frac{1}{C_2} & -\frac{1}{R_{ld}\,C_2} & -\frac{1}{R_{ld}\,C_2} \end{bmatrix}$ $\text{B}=\begin{bmatrix} a_1 \\ -a_2 \\ 0 \\ 0 \end{bmatrix}$</td>
</tr>
<tr>
<td>Topological state (b):
 
</td>
<td>u_1 is OFF
D_1 is ON $\Big\}\Rightarrow$ $i_{D_1} = x_1$, $v_{D_1} = 0$
D_2 is OFF $\Rightarrow$ $i_{D_2} = x_2 = 0 \Rightarrow \dot{x}_2 = 0 \Rightarrow$ $v_{D_2} = -v_2 - v_{r_{L_2}} - v_{C_2} \Rightarrow$ $v_{D_2} = -(a_2/(a_1\,a_3 - {a_2}^2))\,\dot{x}_1 - x_4$
The system can be expressed as $\dot{x} = A\,x + B\,v^{\text{lvs}}$, with
$\text{A}=\begin{bmatrix} -\frac{a_1\,a_3-{a_2}^2}{a_3}\,r_{L_1} & 0 & -\frac{a_1\,a_3-{a_2}^2}{a_3} & 0 \\ 0 & 0 & 0 & 0 \\ \frac{1}{C_1} & 0 & -\frac{1}{R_{ld}\,C_1} & -\frac{1}{R_{ld}\,C_1} \\ 0 & 0 & -\frac{1}{R_{ld}\,C_2} & -\frac{1}{R_{ld}\,C_2} \end{bmatrix}$ $\text{B}=\begin{bmatrix} \frac{a_1\,a_3-{a_2}^2}{a_3} \\ 0 \\ 0 \\ 0 \end{bmatrix}$</td>
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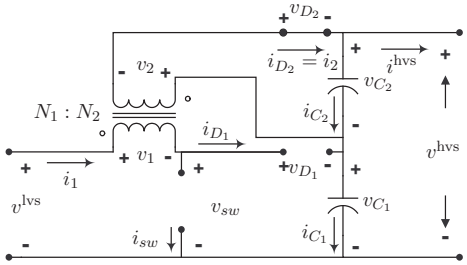
<td>Topological state (c):
 
</td>
<td>u_1 is OFF
D_1 is OFF $\Big\}\Rightarrow$ $x_1 = 0 \Rightarrow \dot{x}_1 = 0$, $i_{D_1} = 0$, $v_{D_1} = v_{sw} - v_{C_1}; v_{sw} = v^{\text{lvs}} - v_{r_{L_1}} - v_1 \Rightarrow$ $v_{D_1} = v^{\text{lvs}} - v_1 - v_{C_1} \Rightarrow$ $v_{D_1} = v^{\text{lvs}} - (a_2/(a_1\,a_3 - {a_2}^2))\dot{x}_2 - x_3$
D_2 is ON $\Rightarrow$ $i_{D_2} = x_2$, $v_{D_2} = 0$
The system can be expressed as $\dot{x} = A\,x + B\,v^{\text{lvs}}$, with
$\text{A}=\begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & -\frac{a_1\,a_3-{a_2}^2}{a_1}\,r_{L_2} & 0 & -\frac{a_1\,a_3-{a_2}^2}{a_1} \\ 0 & 0 & -\frac{1}{R_{ld}\,C_1} & -\frac{1}{R_{ld}\,C_1} \\ 0 & \frac{1}{C_2} & -\frac{1}{R_{ld}\,C_2} & -\frac{1}{R_{ld}\,C_2} \end{bmatrix}$ $\text{B}=\begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}$</td>
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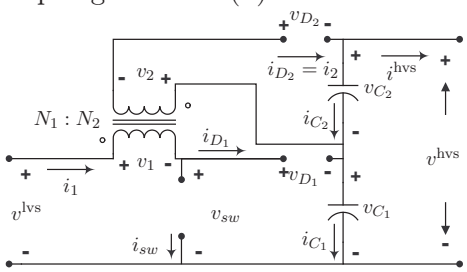
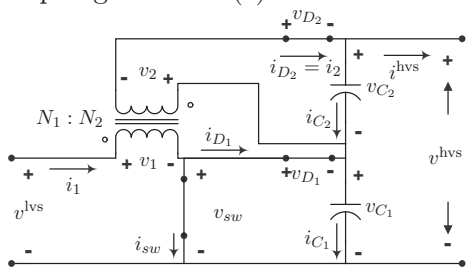
<td>Topological state (d):
 
</td>
<td>u_1 is OFF
D_1 is OFF $\Big\}\Rightarrow$ $x_1 = 0 \Rightarrow \dot{x}_1 = 0$, $i_{D_1} = 0$, $v_{D_1} = v_{sw} - v_{C_1}; v_{sw} = v^{\text{lvs}} - v_{r_{L_1}} - v_1 \Rightarrow$ $v_{D_1} = v^{\text{lvs}} - v_{C_1} \Rightarrow v_{D_1} = v^{\text{lvs}} - x_3$
D_2 is OFF $\Rightarrow$ $i_{D_2} = x_2 = 0 \Rightarrow \dot{x}_2 = 0 \Rightarrow$ $v_{D_2} = -v_2 - v_{r_{L_2}} - v_{C_2} \Rightarrow v_{D_2} = -x_4$
The system can be expressed as $\dot{x} = A\,x + B\,v^{\text{lvs}}$, with
$\text{A}=\begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & -\frac{1}{R_{ld}\,C_1} & -\frac{1}{R_{ld}\,C_1} \\ 0 & 0 & -\frac{1}{R_{ld}\,C_2} & -\frac{1}{R_{ld}\,C_2} \end{bmatrix}$ $\text{B}=\begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}$</td>
</tr>
</table>

Table II.1: Topological variations for the step-up converter with $u_1 = 0$.

Topological state (e):



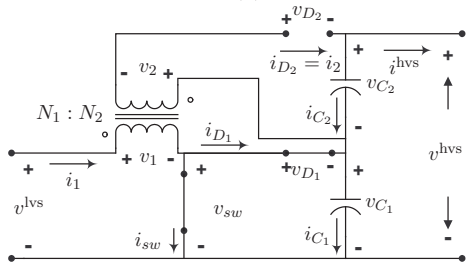
u_1 is ON, D_1 is ON $\Rightarrow$ $v_{D_1} = 0;\ v_{sw} = 0 \Rightarrow$ $v_{C_1} = x_3 = 0 \Rightarrow \dot{x}_3 = i_{C_1}/C_1 = 0 \Rightarrow$ $i_{D_1} = v_{C_2}/R_{ld} = x_4/R_{ld}$

D_2 is ON $\Rightarrow$ $i_{D_2} = x_2$, $v_{D_2} = 0$

The system can be expressed as $\dot{x} = A\,x + B\,v^{\text{lvs}}$, with

$$\text{A}=\begin{bmatrix} -a_1\,r_{L_1} & a_2\,r_{L_2} & 0 & a_2 \\ a_2\,r_{L_1} & -a_3\,r_{L_2} & 0 & -a_3 \\ 0 & 0 & 0 & 0 \\ 0 & \frac{1}{C_2} & 0 & -\frac{1}{R_{ld}\,C_2} \end{bmatrix} \quad \text{B}=\begin{bmatrix} a_1 \\ -a_2 \\ 0 \\ 0 \end{bmatrix}$$

Topological state (f):



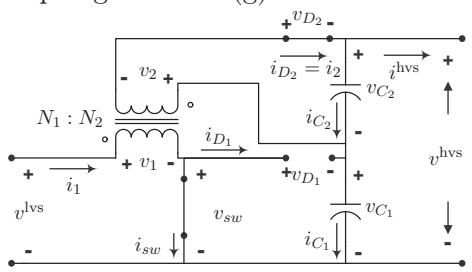
$u_1 =$ is ON, $D_1 =$ is ON $\Rightarrow$ $v_{D_1} = 0;\ v_{sw} = 0 \Rightarrow$ $v_{C_1} = x_3 = 0 \Rightarrow \dot{x}_3 = i_{C_1}/C_1 = 0 \Rightarrow$ $i_{D_1} = v_{C_2}/R_{ld} = x_4/R_{ld}$

D_2 is OFF $\Rightarrow$ $i_{D_2} = x_2 = 0 \Rightarrow \dot{x}_2 = 0 \Rightarrow$ $v_{D_2} = -v_2 - v_{r_{L_2}} - v_{C_2} \Rightarrow$ $v_{D_2} = -(a_2/(a_1\,a_3 - {a_2}^2))\,\dot{x}_1 - x_4$

The system can be expressed as $\dot{x} = A\,x + B\,v^{\text{lvs}}$, with

$$\text{A}=\begin{bmatrix} -\frac{a_1\,a_3-{a_2}^2}{a_3}\,r_{L_1} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -\frac{1}{R_{ld}\,C_2} \end{bmatrix} \quad \text{B}=\begin{bmatrix} \frac{a_1\,a_3-{a_2}^2}{a_3} \\ 0 \\ 0 \\ 0 \end{bmatrix}$$

Topological state (g):



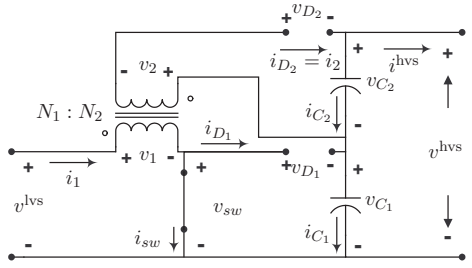
u_1 is ON, D_1 is OFF $\Rightarrow$ $i_{D_1} = 0$, $v_{D_1} = v_{sw} - v_{C_1}; v_{sw} = 0 \Rightarrow v_{D_1} = -v_{C_1} \Rightarrow$ $v_{D_1} = -x_3$

D_2 is ON $\Rightarrow$ $i_{D_2} = x_2$, $v_{D_2} = 0$

The system can be expressed as $\dot{x} = A\,x + B\,v^{\text{lvs}}$, with

$$\text{A}=\begin{bmatrix} -a_1\,r_{L_1} & a_2\,r_{L_2} & 0 & a_2 \\ a_2\,r_{L_1} & -a_3\,r_{L_2} & 0 & -a_3 \\ 0 & 0 & -\frac{1}{R_{ld}\,C_1} & -\frac{1}{R_{ld}\,C_1} \\ 0 & \frac{1}{C_2} & -\frac{1}{R_{ld}\,C_2} & -\frac{1}{R_{ld}\,C_2} \end{bmatrix} \quad \text{B}=\begin{bmatrix} a_1 \\ -a_2 \\ 0 \\ 0 \end{bmatrix}$$

Topological state (h):



u_1 is ON, D_1 is OFF $\Rightarrow$ $i_{D_1} = 0$, $v_{D_1} = v_{sw} - v_{C_1}; v_{sw} = 0 \Rightarrow v_{D_1} = -v_{C_1} \Rightarrow$ $v_{D_1} = -x_3$

D_2 is OFF $\Rightarrow$ $i_{D_2} = x_2 = 0 \Rightarrow \dot{x}_2 = 0 \Rightarrow$ $v_{D_2} = -v_2 - v_{r_{L_2}} - v_{C_2} \Rightarrow$ $v_{D_2} = -(a_2/(a_1\,a_3 - {a_2}^2))\,\dot{x}_1 - x_4$

The system can be expressed as $\dot{x} = A\,x + B\,v^{\text{lvs}}$, with

$$\text{A}=\begin{bmatrix} -\frac{a_1\,a_3-{a_2}^2}{a_3}\,r_{L_1} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & -\frac{1}{R_{ld}\,C_1} & -\frac{1}{R_{ld}\,C_1} \\ 0 & 0 & -\frac{1}{R_{ld}\,C_2} & -\frac{1}{R_{ld}\,C_2} \end{bmatrix} \quad \text{B}=\begin{bmatrix} \frac{a_1\,a_3-{a_2}^2}{a_3} \\ 0 \\ 0 \\ 0 \end{bmatrix}$$

Table II.2: Topological variations for the step-up converter with $u_1 = 1$.

When the converter is working under steady-state condition, the energy transfer process starts with a switch transition from $u_1 = 1$ to $u_1 = 0$. First, the energy is stored in the transformer while the commanded switch is conducting ($u_1 = 1$). When the switch changes from $u_1 = 0$ to $u_1 = 1$ diode D_1 starts to conduct, transferring part of the energy stored in the transformer from the primary winding to the output capacitor C_1. Because of the magnetic coupling, a direct biasing current for diode D_2 is induced in the secondary winding of the transformer, making diode D_2 to conduct. From this, it can be inferred that, during the energy transfer when $u_1 = 0$, the conduction of diode D_1 causes the conduction of diode D_2, and therefore the topological state (b) from Table II.1 is not feasible.

From the operating modes described in Table II.2, modes (e) and (f) are not feasible. The converter under analysis has a step-up structure. Under normal operation, the voltage v_{C_1} will be always greater than zero, making the diode D_1 to be reverse biased if the switch u_1 is ON, and therefore, diode D_1 and switch u_1 will never be in conduction mode simultaneously.

Topological states transition analysis

Having determined the valid topological variations that can be found on the steady-state operation of the converter, it turns out that from the eight possible topologies that can be present depending on the conduction states of u_1, D_1 and D_2, there are only five that can actually be present in the normal functioning of the converter.

It is interesting now to perform an analysis over the valid topology transitions that can take place on the circuit, either by natural evolution of the states or forced by a state transition of the commanded switch. The topology transitions can be characterized by the evolution of the state variables under each position of the commanded switch u_1. Table II.3 shows the characteristics of the state variables under each of the valid topological states of the converter. When the switch is under conduction mode $u_1 = 1$, the current at the primary winding of the transformer x_1 will be always positive, and its derivative will be positive as well. The states included in the $u_1 = 1$ condition are the energy storing states. The energy stored during this condition is after transferred to the output capacitors after a transition from $u_1 = 1$ to $u_1 = 0$ occurs. Let now group the topology states presented in Table II.3 by their state variable characteristics. As can be seen states (a) and (g) share the same condition over the state variables $x_1 > 0$, $x_2 > 0$, $x_3 > 0$ and $x_4 > 0$, therefore let $\Omega_1 = \{\text{state (a)}, \text{state (g)}\}$. As it can be observed in Table II.3, states (c), (d), and (h) do not share the same conditions over the state variables, and then let $\Omega_2 = \{\text{state (c)}\}$, $\Omega_3 = \{\text{state (h)}\}$ and $\Omega_4 = \{\text{state (d)}\}$.

By analyzing the state transitions either by the evolution of the states, or the forced state transitions caused by the change in the position of the switch, a sequence of topological states can be determined. Fig. II.5 summarizes all the possible transitions that can occur among the five valid topological configurations of the step-up converter.

Commanded switch position	Topological state	State variables
$u_1 = 0$	(a)	$x_1 > 0\,(\dot{x}_1 < 0)$ $x_2 > 0\,(\dot{x}_2 > 0)$ $x_3 > 0$ $x_4 > 0$
	(c)	$x_1 = 0 \Rightarrow \dot{x}_1 = 0$ $x_2 > 0\,(\dot{x}_2 < 0)$ $x_3 > 0$ $x_4 > 0$
	(d)	$x_1 = 0 \Rightarrow \dot{x}_1 = 0$ $x_2 = 0 \Rightarrow \dot{x}_2 = 0$ $x_3 > 0$ $x_4 > 0$
$u_1 = 1$	(g)	$x_1 > 0\,(\dot{x}_1 > 0)$ $x_2 > 0\,(\dot{x}_2 < 0)$ $x_3 > 0$ $x_4 > 0$
	(h)	$x_1 > 0\,(\dot{x}_1 > 0)$ $x_2 = 0 \Rightarrow \dot{x}_2 = 0$ $x_3 > 0$ $x_4 > 0$

Table II.3: Topological states and state variables characteristics for the step-up converter.

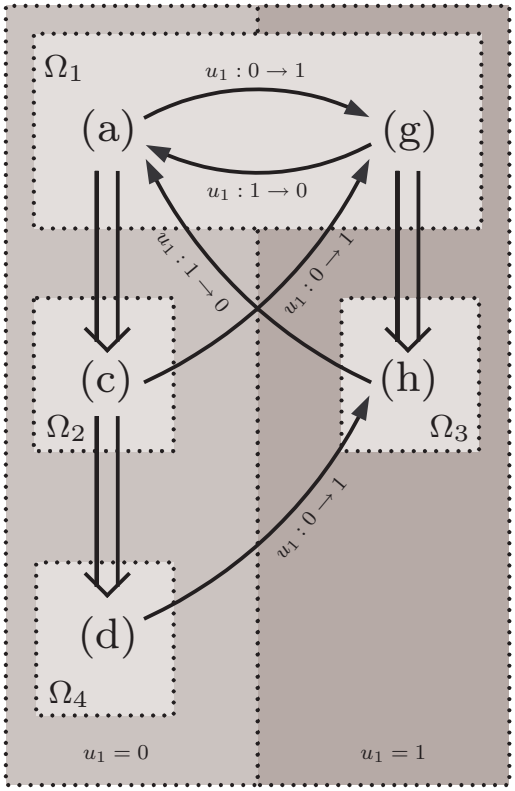


Figure II.5: Steady-state topological state evolution chart for the step-up converter.
Notation : $\Rightarrow$: State evolution topology change.
$\to$: Commanded switch transition topology change.

Dimensioning of the components

The first step to be taken in the component dimensioning process, is to define the desired range of operation for the duty cycle. With this and the input and output voltage requirements, the turns ratio of the transformer can be determined.

From Fig. II.3 it can be seen that the structure of the converter looks like the combination of a regular boost converter and a fly-back converter. Zhao *et al.* [106] use this fact to find the static output/input voltage relationship

$$v^{\text{hvs}} = v_{C_1} + v_{C_2} \approx \frac{1}{1-\hat{u}_1} v^{\text{lvs}} + \frac{\hat{u}_1 \frac{N_2}{N_1}}{1-\hat{u}_1} v^{\text{lvs}} = \frac{1+\hat{u}_1 \frac{N_2}{N_1}}{1-\hat{u}_1} v^{\text{lvs}}, \tag{II.25}$$

where $\hat{u}_1 \ \epsilon \ [0,1]$ is the PWM duty cycle applied to switch u_1. v^{lvs} is the voltage at the low voltage side of the converter. v^{hvs} is the voltage at the high voltage side of the converter. N_1 is the number of turns at the primary winding, N_2 is the number of turns at the secondary winding, hence N_2/N_1 is the turns ratio of the transformer. The total output voltage is written as the sum of the voltages of capacitors C_1 (the boost part capacitor) and C_2 (the fly-back part capacitor). The first ($v_{C_1} \approx (1/(1-\hat{u}_1))v^{\text{lvs}}$) and the second ($v_{C_2} \approx (\hat{u}_1(N_2/N_1)/(1-\hat{u}_1))v^{\text{lvs}}$) components of Eq. (II.25), correspond to the static output/input relationships for the standard boost and fly-back converters respectively, both working in CCM (continuous conduction mode) [29].

It would be convenient to have a design duty cycle value $\hat{u}_1$ that is far from the upper saturation level of 1. In this way, the control algorithm will be able to provide control commands within a safe region, avoiding the saturation of the control variable $\hat{u}_1$. The maximum desired value for the duty cycle is set to be $\hat{u}_1 = 0.675$. This value will be used when the maximum elevation ratio is required. A fixed output voltage of 425 V dc is demanded from the converter, and hence, the maximum elevation ratio will be present when the minimum input voltage level is present. As it has been mentioned before, this situation presents when the maximum power extraction from the FC unit takes place. This fact can be observed in Fig. II.2, as the output power of the FC unit grows, the voltage that the device is able to give decreases, reaching 24 V dc when the device is delivering around 1 kW.

This information can be used to have an estimation on the appropriate turns ratio of the transformer to be used. By replacing the values of the maximum desired duty cycle $\hat{u}_1 = 0.675$, the desired output voltage $v^{\text{hvs}} = 425$ V dc when the minimum input voltage $v^{\text{lvs}} = 24$ V dc is present in Eq. (II.25) a reference turns ratio for the design of the transformer can be obtained, in this case $N_2/N_1 \approx 7$.

The final number of turns for the primary as well as for the secondary windings of the transformer will depend on the switching frequency, desired maximum current ripple, input current average value, duty cycle value at the desired operating point, maximum flux saturation level of the magnetic core to be used, type of wire used in the windings, etc..

For the operation of the system a switching frequency of $f_{sw} = 20$ kHz has been chosen. The input current average value can be extracted from the maximum output power condition of the FC. At 1 kW the FC voltage is 24 V dc, which means that an average current of $i_1^{\text{ave}} = 41.667$ A is given to the step-up stage. The duty cycle at the 1 kW operating point is $\hat{u}_1 = 0.675$. The maximum desired input current ripple at the operating point is set to 10 %.

The inductance value for the primary winding (L_1) of the high-frequency transformer is determined by the desired current ripple and the maximum input current level. The average input current i_1^{ave} can be analytically determined by applying the integral

$$i_1^{\text{ave}} = \frac{1}{T_{sw}} \int_0^{T_{sw}} i_1(\tau) d\tau, \tag{II.26}$$

over one switching period $T_{sw} = 1/f_{sw}$. The the input current can be split in two parts, when switch u_1 conducts (during the period $[0, \hat{u}_1\, T_{sw}]$) and when switch u_1 does not conduct (during the period $[\hat{u}_1\, T_{sw}, T_{sw}]$), and therefore, the average input current can be rewritten as

$$i_1^{\text{ave}} = \frac{1}{T_{sw}} \int_0^{\hat{u}_1\, T_{sw}} i_1^{\text{on}}(\tau) d\tau + \frac{1}{T_{sw}} \int_{\hat{u}_1\, T_{sw}}^{T_{sw}} i_1^{\text{off}}(\tau) d\tau \tag{II.27}$$

In order to be able to determine the primary winding inductance value (L_1), first some assumptions have to be made. Let first assume that $i_1^{\text{off}}(t) = 0$. This fact can be concluded by analyzing the input current curves shown by Zhao *et al.* in [106] and Van de Sype *et al.* in [92]. When switch u_1 is not conducting, the contribution of the current flowing through the primary winding is scarce Then the calculations are simplified by assuming $i_1^{\text{off}}(t) = 0$. Let now neglect the input current ripple and assume that $i_1^{\text{on}}(\tau)$ is constant. The effect of the desired maximum input current ripple will be latter taken into consideration. By making the assumptions mentioned before, the relationship

$$i_1^{\text{ave}} = \frac{1}{T_{sw}} \int_0^{\hat{u}_1\, T_{sw}} i_1^{\text{on}}(\tau) d\tau = \frac{1}{T_{sw}}\, i_1^{\text{on}} \Big|_0^{\hat{u}_1\, T_{sw}} = i_1^{\text{on}}\, \hat{u}_1, \tag{II.28}$$

is found. From Eq. (II.28), and using the values of the quantities given before, it is obtained that $41.667 = i_1^{\text{on}}\, 0.675$, and therefore $i_1^{\text{on}} = 61.7284$ A.

Now the desired input current ripple can be considered. As mentioned before, the maximum allowed current ripple for the design of the transformer has been set to 10 %. This means that $i_1^{\text{on}}\ \epsilon\ [61.7284 - \Delta\, i_1^{\text{on}}, 61.7284 + \Delta\, i_1^{\text{on}}]$, with $\Delta\, i_1^{\text{on}} = 61.7284 * 0.1 = 6.1728$ A. From this, it can be obtained that the net input current change during the ON condition of switch u_1 is $2\, \Delta\, i_1^{\text{on}} = 12.3456$ A. The design of the transformer is being performed under the worst case scenario conditions, maximum output power that can be provided by the FC unit (1 kW), and therefore, the lowest input voltage level for the step-up converter (24 V dc). Under these circumstances, the input current ripple and the input voltage determine a reference design value for the primary winding during the ON condition of switch u_1. These quantities are related by

$$v^{\text{lvs}} = L_1\, \frac{d}{dt} i_1 \ \Rightarrow\ v^{\text{lvs}} = L_1 \frac{2\, \Delta\, i_1^{\text{on}}}{\hat{u}_1\, T_{sw}} \ \Rightarrow\ 24 = L_1 \frac{12.3456}{0.675(1/20000)}, \tag{II.29}$$

and therefore, $L_1 = 61.65\ \mu$H. From the relationship $N_2/N_1 \approx \sqrt{L_2/L_1}$, the inductance value of the secondary winding is determined, taking the value $L_2 = 3.215$ mH.

Parameter	Value
Switching frequency:	$f_{sw} = 20$ kHz
Primary winding turns:	$N_1 = 20$ turns
Primary winding inductance:	$L_1 = 72.45$ μH
Primary winding parasitic resistor:	$r_{L_1} = 3.35$ mΩ
Secondary winding turns:	$N_2 = 136$ turns
Secondary winding inductance:	$L_2 = 3.49$ mH
Secondary winding parasitic resistor:	$r_{L_2} = 85.64$ mΩ
Magnetic coupling:	$M = 493$ μH

Table II.4: High-frequency transformer parameters

With this information a high-frequency transformer has been designed and built. The resulting parameters of the transformer used on the experimental setup are summarized in table II.4. As can be observed, although the actual values for L_1 and L_2 differ from the reference design values presented previously, the differences are small. The high-frequency transformer has been built using a Micrometals T400-60D iron powder core. The windings have been constructed using 2.7 mm diameter H-180 class copper wire from Ederfil.

The voltage rating of capacitors C_1 and C_2 can be found by following the guidelines given by Van de Sype *et al.* in [92]. From these guidelines, the voltage ratings for capacitors C_1 and C_2 take the form

$$v_{C_1}^{\max} = \frac{1}{1-\hat{u}_1}\, v^{\text{lvs}}\,;\; v_{C_2}^{\max} = \frac{N_2}{N_1}\frac{1}{1-\hat{u}_1}\, v^{\text{lvs}}. \tag{II.30}$$

By replacing the values for the worst case scenario given before into Eq. (II.30), it is obtained that $v_{C_1}^{\max} = 73.85$ V dc and $v_{C_2}^{\max} = 516.92$ V dc. As it can be observed, the value for $v_{C_2}^{\max}$ looks exaggerated for this application, as the total required output voltage is $v^{\text{hvs}} = v_{C_1} + v_{C_2} = 425$ V dc. In this case, the criteria applied has been to have $v_{C_1}^{\max} = 425 - v_{C_2}^{\max} = 351.15$ V dc.

The criteria used to determine the capacitance value for C_1 and C_2 has been the desired output voltage ripple. As mentioned in [92], in this topology the dominant output voltage ripple is caused by the voltage variations of C_1, as the current levels handled by C_2 are smaller. A value of $C_1 = C_2 = 220$ μF has been chosen in order to have a small output voltage ripple. With this capacitance value, the worst case voltage ripple can be estimated by studying the current levels handled by C_1 at the maximum output power condition for the step-up stage (1 kW). After the switch u_1 changes from ON state (topological state (h) in Table II.2) to OFF state (topological state (a) in Table II.1), the current flowing through the primary winding of the converter, is routed to capacitor C_1 by the action of diode D_1. At the switch transition point, the maximum the value of current i_1 is $i_1^{\max} = i_1^{\text{on}} + \Delta\, i_1^{\text{on}} = 67.9$ A, obtained from the assumptions taken during the transformer design process.

At the maximum output power condition, and from the topological state (a) (shown in Table II.1), it can be shown that the current flowing through capacitor C_1 is $i_{C_1}^{\max} = (i_1^{\max} - 1000\text{ W}/425\text{ V dc})$, and therefore, the voltage change rate can be obtained in the form $d\,v_{C_1}/dt = i_{C_1}/C_1$. If considering that this current flows through capacitor C_1 during $(1-\hat{u}_1)\,T_{sw}$, then a maximum voltage ripple of 4.84 V dc, which is only a 1.14 % of the desired total output voltage $v^{\text{hvs}} = 425$ V dc. As mentioned in [92], the output voltage ripple of capacitor C_2 will be lower than the ripple present at C_1, and therefore, in this case negligible.

For the dimensioning of diodes D_1 and D_2 there are two factors that must be taken into account. The first consideration is regarding the maximum current ratings that the diodes must support. For diode D_1, the maximum current that will flow through it coincides with the peak current at the primary winding of the high-frequency transformer. As mentioned before, the estimated value obtained during the design process of the transformer is $i_{D_1}^{\max} = i_1^{\max} = 67.9$ A. For diode D_2, an estimation on the maximum current can be obtained by using the secondary to primary current relationship $i_{D_2}^{\max} = i_{D_1}^{\max}/(N_2/N_1)$. Therefore it is obtained that the current rating for diode D_2 is ≈ 10 A.

The second consideration when dimensioning diodes D_1 and D_2 regards the maximum repetitive reverse voltage (VRRM) supported by the semiconductors. When the diodes are not conducting, they must support the voltage that is present at their terminals. From the topology analysis performed in Section II.1.2 it is obtained that for diodes D_1 and D_2, the maximum reverse voltages present when the topological state (h), shown in Table II.2 is present in the system. Diode D_1 must support a worst case maximum reverse voltage of $v_{D_1}^{\max} = -v_{C_1}^{\max} = -73.85$ V dc. It can be proven that under topological state (h), $v_{D_2}^{\max} = -M\,\dot{x}_1 - x_4$. An steady-state estimation for $\dot{x}_1$ can be obtained from the assumptions made during the design of the transformer. The estimation for $\dot{x}_1$ can be obtained from the approximation for the derivative of the input current under the ON state of switch u_1 presented in Eq. (II.29) and therefore $\dot{x}_1 \approx 2\,\Delta\,i_1^{\text{on}}/\hat{u}_1\,T_{sw} = 12.3456 * 20000/0.675$. The maximum expected value for x_4 is $v_{C_2}^{\max} = 351.15$ V dc. Therefore, the expected maximum voltage for diode D_2 is $v_{D_2}^{\max} = -(493 \cdot 10^{-6} * 12.3456 * 20000/0.675) - 351.15 = -531.48$ V dc.

The commanded switch should be dimensioned to have a maximum current rating that corresponds to the maximum current that will flow through the primary winding of the transformer. Again, the maximum current rating for the switch of $i_{sw}^{\max} = i_1^{\max} = 67.9$ A is expected. From the topology analysis performed in Section II.1.2 it can be concluded that the maximum voltage between the terminals of the switch, will coincide with the maximum voltage present at capacitor C_1, and therefore $v_{sw}^{\max} = v_{C_1}^{\max} = 73.85$ V dc.

Fig. II.6 presents the final configuration of the step-up structure used. An input current low-pass filter (L_{in} and C_{in}) has been added, in order to protect the FC unit against the high-frequency, discontinuous input current shape of the converter originally presented by Zhao *et al.* in [106]. The cut-off frequency of such low-pass filter can be easily obtained by applying $f_{in}^{\text{co}} = 1/(2\,\pi\,\sqrt{C_{in}\,L_{in}})$, in this case $\approx$ 550 Hz. The values of the components used in the converter of Fig. II.6 are: $v_{fc} = 24$ to 36 V dc provided by the FC unit. The input current filter is formed by a $L_{in} = 42$ μH inductance with a 10 mΩ series parasitic resistance and a

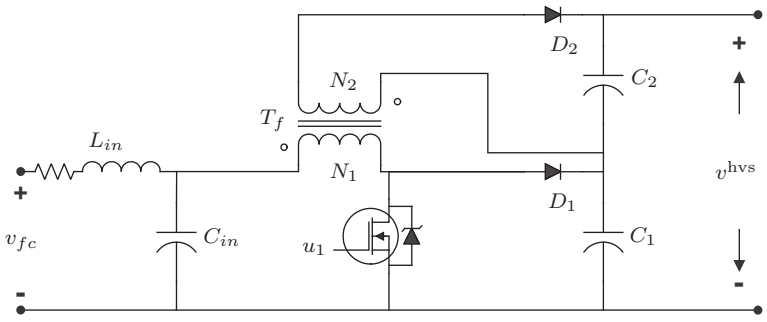


Figure II.6: Step-up converter topology and input current filter.

$C_{in} = 2000$ μF capacitor. Capacitors C_1 and C_2 are 220 μF 400 V dc rated capacitors. T_f is a high-frequency transformer with $N_1 = 20$ turns, $N_2 = 136$ turns. The total inductance seen at the primary winding is $L_1 = 72.45$ μH in series with a parasitic resistance $r_{L_1} = 3.35$ mΩ. The total inductance seen at the secondary winding is $L_2 = 3.49$ mH in series with a parasitic resistance $r_{L_2} = 85.64$ mΩ. The magnetic coupling has a value of $M = 493$ μH. The switch u_1 is commanded by using regular centered pulse, single-update mode, pulse-width modulation (PWM) at $f_{sw} = 20$ kHz.

The output voltage must be maintained at $v^{\text{hvs}} = 425$ V dc in order to be able to feed the dc-ac inversion stage and the step-up stage full-load condition is set to 1 kW output power.

The main switch u_1 has been implemented using four IRFPS40N50L 500 V_{DSS}, 46 A in parallel with a total $Rds_{on} = 20$ mΩ, and 1.5 V dc forward voltage drop for the recovery diode. D_1 is a DPG60I400HA 60 A average, 400 V_{RRM} HiPerFRED2 diode with 1.5 V dc forward drop from IXYS. D_2 is formed by a series of two DSEI60-10A 60 A, 1000 V_{RRM} FRED diode with 2 V dc forward drop from IXYS.

Dynamic behavior and component dimensioning verification

The step-up converter presented in [106] has only one commanded switch u_1, which can take only two states. The presence of free-wheeling diodes D_1 and D_2 on the system introduces more topological states in the steady state behavior of the converter than main switch positions. From Section II.1.2 it is known that up to five different topological states can present in the steady-state operation of the converter, being these the topologies (a), (c) and (d) shown in Table II.1; (g) and (h) shown in Table II.2.

The presence of these topological states has a load dependent behavior, some of them can disappear/show up under certain load conditions. This situation complicates the obtention of averaged models of this converter suitable for control purposes. The allowed state transitions between the five possible topologies has been summarized in Fig. II.5. The transitions among these five states is determined by the behavior of the state variables under each of the topologies, a summary of the characteristics of the state variables under each topology can be found in Table II.3.

The aim of this part of the work is twofold. In the first place, by means of numerical simulations of the converter using the values of the components found before, confirm that the components will be working within their allowed current/voltage ratings. The simulation environment used and the general considerations to be taken when performing the simulations will be described in detail in Section II.3, in this case a time step of $1 \cdot 10^{-9}$ s is used. Second, to illustrate the load dependence on the apparition/vanishing of the operating modes when varying the output power condition, while working with the worst case input voltage $v_{fc} = 24$ V dc, at the desired output voltage level of $v^{\text{hvs}} = 425$ V dc.

Fig. II.7 shows the steady-state operation of the converter of Fig. II.6, using the values of the components found previously. The switching frequency is $f_{sw} = 20$ kHz. The main switch u_1 is driven by using centered pulse, single-update mode, PWM. The duty cycle has been empirically adjusted to provide an output voltage of $v^{\text{hvs}} = 425$ V dc. The input voltage is $v^{\text{lvs}} = 24$ V dc, and a load $R = 3.61$ kΩ has been used to provide an output power of 50 W. By making and analysis of the curves of Fig. II.7 and matching them with the states of Tables II.1 and II.2, it can be seen that the states (a), (c), (d) and (h) are clearly identifiable.

Fig. II.8 shows the steady-state behavior of the final converter configuration presented in Fig. II.6, but now it is driven to give an output power of 100 W. In this case a load resistor of $R = 1.8$ kΩ has been used. By making the matching between the states and the observed behavior, it can be seen now that only three states are evident. States (a), (c) and (h) are clearly identifiable. State (d) although present, which allows the transition to state (h), has a contribution that is not noticeable.

Fig. II.9 shows the steady-state behavior of the converter while feeding a 500 W load. In this case a load resistor of $R = 361\Omega$ has been used. By making the matching between the states and the observed behavior, states (a), (c), (g) and (h) appear. Finally, Fig. II.10 shows the steady-state behavior of the converter while driving a 1000 W resistive load. In this case a load resistor of $R = 181\Omega$ has been used. In this case, states (a), (c), (g) and (h) are also present. From this, one can conclude that more or less the same dynamic behavior of the converter can be expected in the range 500 W and 1000 W.

It can be observed in all cases, that the current demanded by the step-up stage to the power source v_{fc} has been filtered, showing a practically dc behavior. This fact can be noticed by the green trace with the label I(RLf) in all plots. Eq. (II.25) constitutes a good starting point to determine the turns ratio of the transformer, but is not an accurate way to estimate the output voltage. By examining the current shapes of Fig. II.10 and Fig. II.8, it can be observed that the assumption that the boost part is working in CCM is incorrect. The current through diode D_1 decreases rapidly, reaching a value of 0 A while the switch is still not conducting, and this is the behavior of a boost converter working in DCM [29].

This assumption introduces inaccuracy in the obtained results, meaning that the dynamics of the converter are more complex than expected in [92] and [106], this is mainly caused because of the mutual interactions between the coils, that makes it difficult to determine the switching behavior of the free-wheeling diodes.

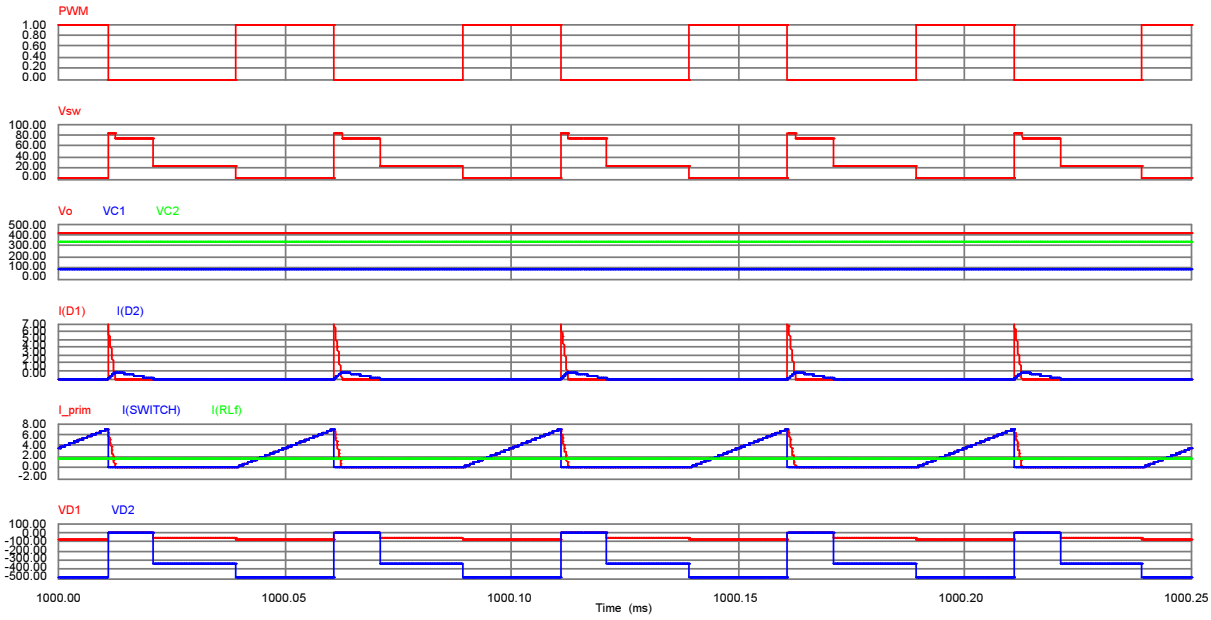


Figure II.7: Step-up converter steady-state behavior at 50 W output power ($v^{\text{lvs}} = 24$ V dc, $v^{\text{hvs}} = 425$ V dc)

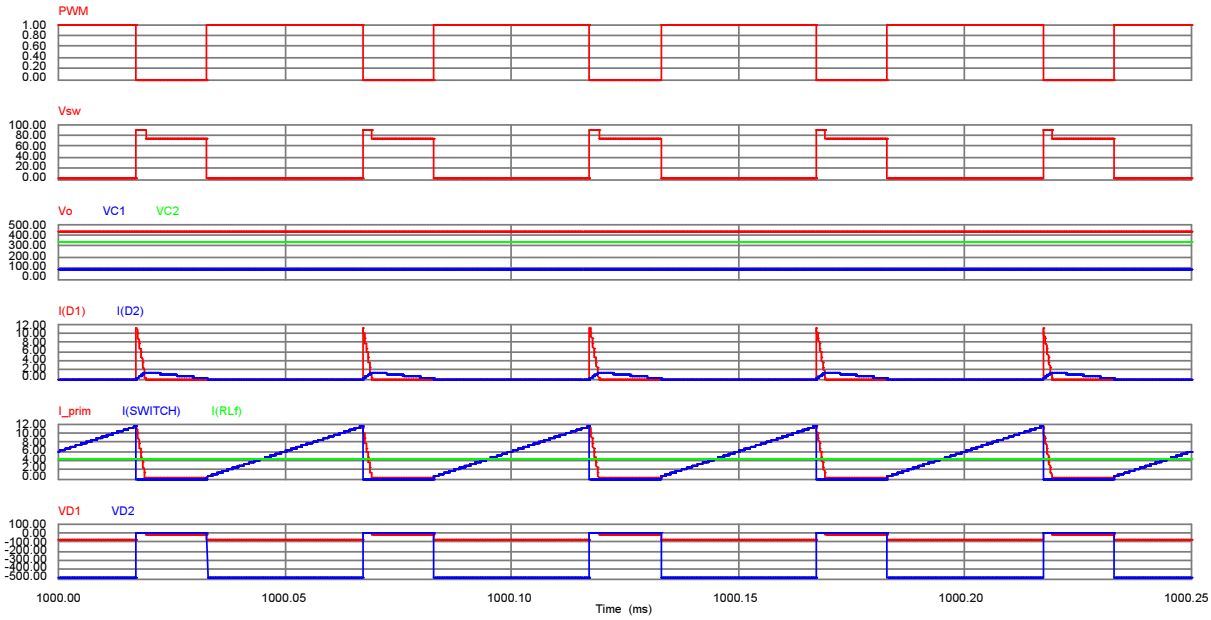


Figure II.8: Step-up converter steady-state behavior at 100 W output power ($v^{\text{lvs}} = 24$ V dc, $v^{\text{hvs}} = 425$ V dc)

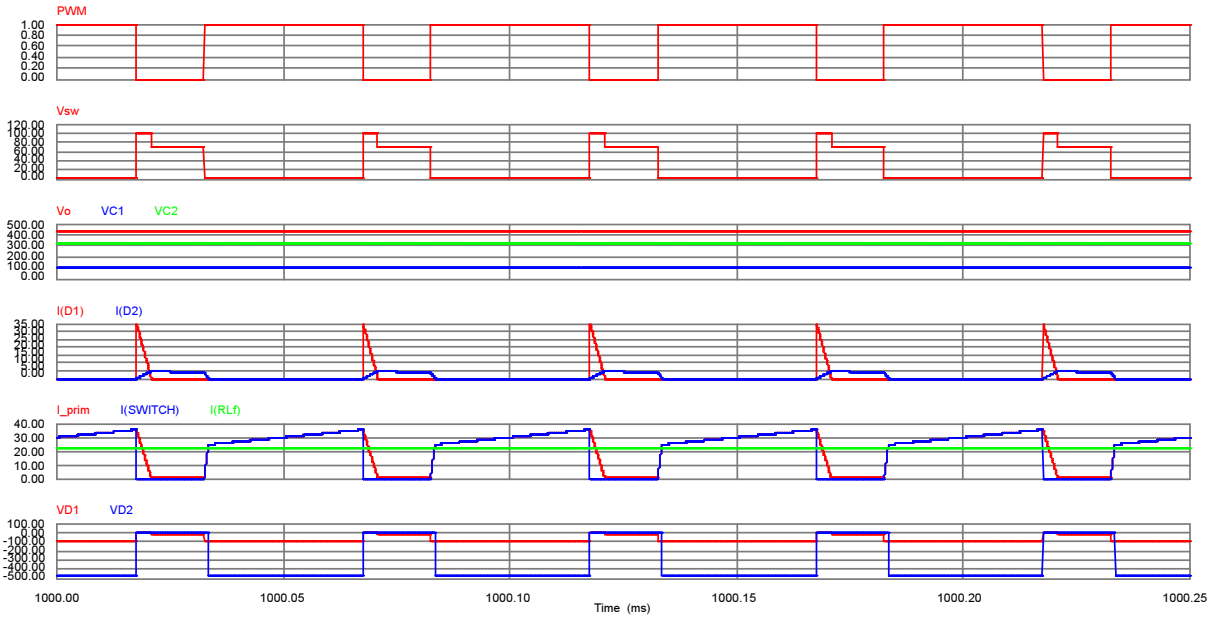


Figure II.9: Step-up converter steady-state behavior at 500 W output power ($v^{\text{lvs}} = 24$ V dc, $v^{\text{hvs}} = 425$ V dc)

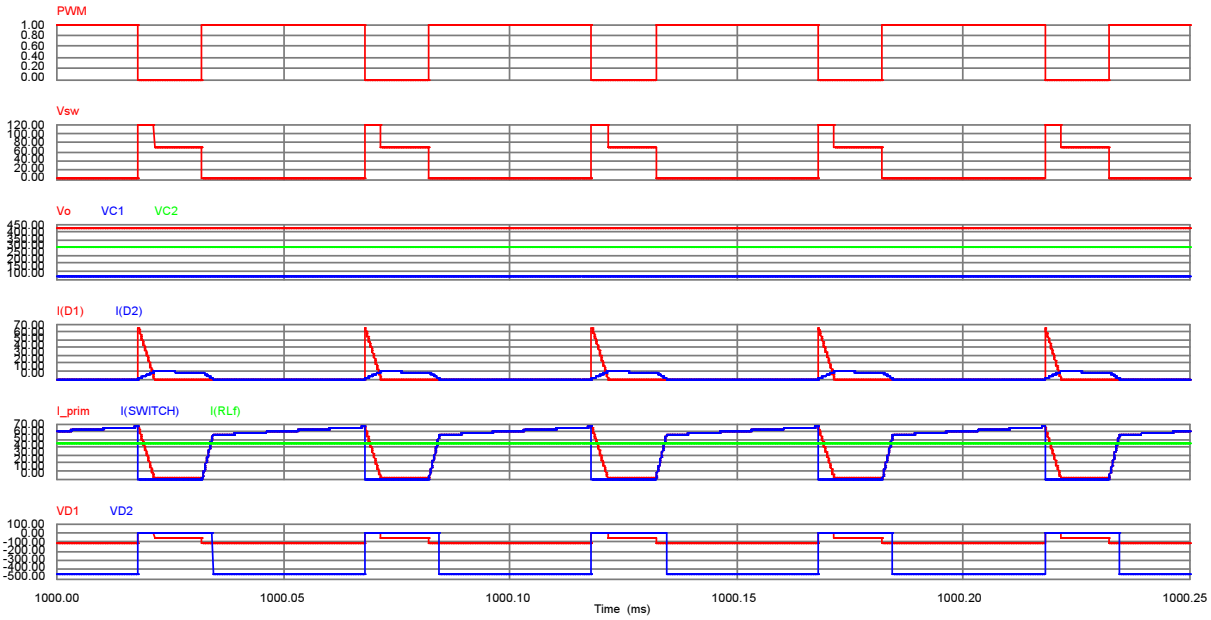


Figure II.10: Step-up converter steady-state behavior at 1000 W output power ($v^{\text{lvs}} = 24$ V dc, $v^{\text{hvs}} = 425$ V dc)

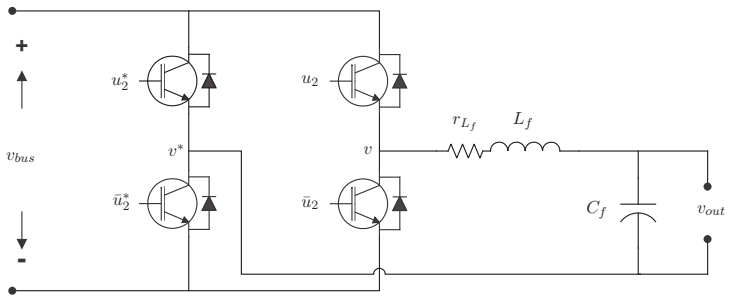


Figure II.11: Full-bridge dc-ac inverter and LC output filter.

The difficulties on the implementation of this family of converters appear when the traditional tools of the control theory are applied. Up to now, neither transfer function model nor nonlinear averaged differential model have been developed. The difficulties to find an accurate model for these converters are increased not only by the structure of the system, but also by the fact that these converters are designed to operate all the time under discontinuous conduction mode.

II.1.3 Dc-ac inversion stage

The dc-ac inversion stage consists of a full-bridge dc-ac inverter presented in Fig. II.11. The full-bridge dc-ac inverter is formed by two legs, each of them composed by the pairs of switches u_2^* and $\bar{u}_2^*$; and u_2 and $\bar{u}_2$ respectively. Both legs are connected in parallel, and fed by the dc bus, at a common interconnection point with the step-up stage and the APU. The converter is driven by using centered pulse, single-update mode, three-level PWM with a switching frequency of $f_{sw} = 20$ kHz with the switches working under hard switching.

The output is the differential voltage obtained between the midpoint of each of the legs, denoted by v^* and v in Fig. II.11. The voltage $v^* - v$ shows a square shape at 20 kHz. The differential voltage is latter filtered by a LC low-pass filter formed by the inductor L_f and the output capacitor C_f. The voltage to be fed to the ac load is the voltage present at the terminals of the filter capacitor.

Conversion requirements and dimensioning of the components

The output voltage must follow a sinusoidal reference with a fundamental frequency of 50 Hz and 230 V ac rms feeding linear and nonlinear loads. The dc-ac inversion stage must be able to provide 5 kVA peak apparent power (overload condition), with a maximum active component of 3 kW composed by 1 kW supplied by the step-up stage and 2 kW given by the auxiliary power unit at the dc side of the inverter.

As mentioned in previous Sections, a voltage at the common interconnection point $v_{bus} = 425$ V dc is used to feed the dc-ac inversion stage, and therefore, the semiconductors must have a break down voltage level higher than this. Regarding the maximum current consideration, first, the needed rms current can be obtained from the maximum apparent power and the rms value of voltage to be supplied. The apparent power relationship $p_{out}^{\text{rms}} = v_{out}^{\text{rms}}\, i_{out}^{\text{rms}}$, where v_{out}^{rms} and i_{out}^{rms}

are the rms values of the voltage and the current provided to the ac load. v_{out}^{rms} is well known, as in the specifications is stated that this inversion stage must provide a voltage of 230 V ac rms. p_{out}^{rms} is the maximum apparent power to be provided by the dc-ac inversion stage, and therefore $p_{out}^{\text{rms}} = 5$ kVA. From this, a maximum rms current of $i_{out}^{\text{rms}} = p_{out}^{\text{rms}}/v_{out}^{\text{rms}} = 21.74$ A ac rms is expected.

As nonlinear loads are to be fed, the Crest Factor (CF) can be used to determine the maximum current that will flow through the semiconductors. The CF is defined as the ratio between the peak value of a periodic signal divided by its rms value. For this work, a maximum CF value of 4 has been considered. From this fact, the peak current that the semiconductors must stand is $i_{out}^{\text{pk}} = i_{out}^{\text{rms}} * \text{CF} = 86.96$ A.

The next thing to consider is the dimensioning of the output filter L_f, C_f. The cut-off frequency of the filter must allow a good tracking of the desired 50 Hz output voltage, but at the same time it must filter the high-frequency components of the differential voltage $v^* - v$. In this case a desired cut-off frequency of 900 Hz has been chosen. The cut-off frequency can be easily related to the values of the components of the low-pass filter by the relationship $f_{out}^{\text{co}} = 1/(2\,\pi\,\sqrt{C_f\,L_f})$.

With this information the components to be used have been chosen. In summary, the dc-ac inversion stage consists of a full-bridge dc-ac inverter (see Fig. II.11) formed by two 1200 V dc, 100 A dc Semikron SKM100GB123D IGBT half-bridge modules with 2 V dc drop for the IGBTs and 0.8 V dc drop for each of the antiparallel diodes. The output voltage must follow a sinusoidal reference with a fundamental frequency of 50 Hz and 230 V ac rms feeding linear and nonlinear loads. The dc-ac inversion stage must be able to provide 5 kVA peak apparent power (overload condition), with a maximum active component of 3 kW composed by 1 kW supplied by the step-up stage and 2 kW given by the auxiliary power unit at the dc side of the inverter. The components used have the following values: $v_{bus} = 425$ V dc provided by the step-up stage and the auxiliary power unit when extra power is needed, $L_f = 384$ μH inductance in series with a $r_{L_f} = 700$ mΩ parasitic resistance, $C_f = 81$ μF.

II.1.4 Auxiliary power unit (APU)

The design of the APU and the dimensioning of its components must complement the power/bandwidth characteristics/limitations of the other parts that form the stand-alone energy conditioning system. As mentioned in Section II.1, the chosen architecture for the electric energy conditioning system used in this work is based on a multiple-stage dc-ac power inverter configuration.

From Fig. II.1 it is clear that, the chosen APU interconnection topology is the one connected at the high voltage side of the step-up stage. In this way, there is no risk of damaging the FC unit because of the accidental injection of an inverse current. At the same time, the efficiency of the APU system increases, as the energy passes through less conversion stages when flowing from the energy storing device to the load as pointed out in Section I.1.3.

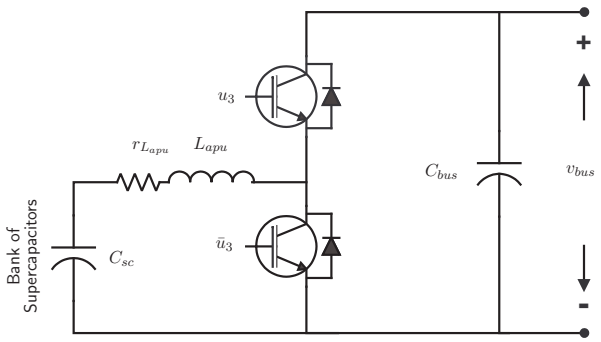


Figure II.12: Auxiliary power unit.

In this case, Supercapacitors (SCs) have been chosen as the energy storing device due to their energy and power density characteristics. As the APU is connected to the high voltage side of the dc-dc step-up stage, in general, it can be considered that the voltage at the dc bus is going to be higher than the voltage at the terminals of the bank of SCs, due to the low voltages handled when this kind of storage devices are used. This implies that dc-dc interfacing converter ought to work as a step-up converter when the energy flows from the bank of SCs to the dc bus (overload condition), and as a step-down when the energy flows from the dc bus to the bank of SCs (charging condition).

Because of the reasons explained before, a current bidirectional dc-dc converter topology is used on this stage. Fig. II.12 shows the schematic diagram of the bank of SCs and the dc-dc interfacing converter used.

Conversion requirements and dimensioning of the components

Recalling the specifications of the system from Section I.2.1, the energy conditioning system must be able to provide an ac voltage shape with an active power component up to 3 kW (1 kW given by the step-up stage and 2 kW extra given by the APU) for up to 45 s.

The components to be dimensioned in this case are three. The first is the bank of SCs, which should be dimensioned so there is enough energy stored to supply the overload requirements taking into account the possible losses that will present in the operation of the system. The second, the inductor to be used in the dc-dc interfacing converter, and the third, the switches used in the interfacing converter. We start with the dimensioning of the bank of SCs. The energy stored in the bank of SCs is expressed by

$$E_{sc} = \frac{1}{2} C_{sc} v_{sc}^2.$$

Schempp *et al.* in [77] summarize the considerations to take into account during a bank of SCs dimensioning process. When utilizing SCs in practical applications, the total energy stored is not recoverable as, generally, the voltage can not be reduced to zero on the bank of SCs, specially due to the limited gain of the interfacing converter. Moreover, the minimum bank of SCs operational voltage will be determined by the minimum voltage permitted by the APU's interfacing converter when the energy is being transferred from the SCs to the dc bus.

Although variations on the capacitance of the bank of SCs are present due to frequency, voltage and temperature conditions, as noted by Rafik *et al.* in [71], for the sake of simplicity, a constant capacitance C_{sc} is considered in this work. The energy to be supplied by the APU when an overload is present is the difference between the initial energy and the final energy on the bank of SCs. The contribution, of the power provided by the APU to the active power delivered at the ac output of the system, is the rate at which this energy change has been supplied in the form

$$p_{ovl} = \frac{\Delta E_{sc}}{t_{ovl}}\, k_1\, k_2 = \frac{(E_{sc_i} - E_{sc_f})}{t_{ovl}}\, k_1\, k_2 = \frac{1}{2}\, C_{sc}\, \frac{(v_{sc_i}^2 - v_{sc_f}^2)}{t_{ovl}}\, k_1\, k_2. \tag{II.31}$$

Constants k_1 and k_2 account for the conversion efficiencies of the APU interfacing converter and the dc-ac inverter respectively. It is important to take into account these factors, as the losses in the system affect the dimensioning of the bank of SCs to be used. E_{sc_i} is the initial energy stored in the bank of SCs (in Joules), E_{sc_f} is the final energy stored at the bank of SCs after it has been discharged by the presence of an overload condition. p_{ovl} is the power contribution of the APU to the active power component delivered at the output of the dc-ac inversion stage (in watts) during the overload, t_{ovl} is the duration of the overload condition in the system (in seconds).

The output power requirement of 2 kW for 45 s can be translated into a total energy change requirement. The total energy to be supplied by the APU at the output of the inverter can be extracted from Eq. (II.31) in the form $p_{ovl}\, t_{ovl} = 2000{*}45 = 90$ kJ $= (E_{sc_i} - E_{sc_f})\, k_1\, k_2$. In this case a conservative efficiency consideration has been taken for both, the APU and the dc-ac inverter. The value of the product of the efficiency coefficients k_1 and k_2 is set to $k_1\, k_2 = 0.75$. Therefore, the amount of energy to be supplied by the bank of SCs is $\Delta\, E_{sc} = E_{sc_i} - E_{sc_f} = 120$ kJ. Having a constant capacitance for the bank C_{sc}, its initial and final energy levels are determined by the respective voltage levels under each condition.

Woojin Choi *et al.* [18] determine the amount of usable energy as a function of the voltage drop in the bank. In their design case the minimum allowed level of stored energy is set to 50 % of the capacity of the bank of SCs. In this design it has been chosen to extract 85 % of the energy stored from the bank of SCs to fulfill the overload requirements and the losses. As stated above, the energy to be provided by the bank of SCs is $\Delta\, E_{sc} = 120$ kJ. The 85 % energy extraction limit is translated into a voltage drop requirement from Eq. (II.31), obtaining

$$\Delta E_{sc} = \frac{1}{2} C_{sc} (v_{sc_i}^2 - v_{sc_f}^2) = \frac{1}{2} C_{sc} (v_{sc_i}^2 - (1 - 0.85) v_{sc_i}^2) = 0.85 \frac{1}{2} C_{sc} v_{sc_i}^2. \tag{II.32}$$

It is clear from the equation above that $v_{sc_f} = \sqrt{1 - 0.85}\, v_{sc_i}$, and therefore, the relationship above can be rewritten in terms of the desired final voltage at the bank of SCs, obtaining

$$\Delta E_{sc} = \frac{1}{2} C_{sc} v_{sc_f}^2 \left(\frac{0.85}{1 - 0.85} \right),$$

and therefore, the capacitance to be used in the bank of SCs can be expressed as

$$C_{sc} = 2 \left(\frac{1 - 0.85}{0.85} \right) \frac{\Delta E_{sc}}{v_{sc_f}^2}. \tag{II.33}$$

The desired voltage levels to be used on the bank of SCs are determined by the desired elevation ratios at the APU dc-dc converter. The maximum elevation ratio is achieved when the bank of SCs reaches its minimum allowed voltage. If an 85 % of the energy is to be extracted from the bank of SCs, the relationship $v_{sc_f} = \sqrt{1 - 0.85}\, v_{sc_i}$ holds between the initial and the final voltage at the SCs. As mentioned before, the converter shown in Fig. II.12 must work as a boost converter during an overload, and therefore $v_{sc} \leq v_{bus} = 425$ V dc. The maximum initial voltage that the bank of SCs can have is then $v_{sc_i} = 425$. By using this initial voltage, a final voltage of $v_{sc_f} = 425\sqrt{1 - 0.85} = 164.6$ V dc needs to be achieved in order to guarantee an 85 % energy extraction. At $v_{sc_f} = 164.6$ V dc, a step-up ratio of 2.58 will be demanded from the interfacing converter in order to achieve the 425 V dc at the dc-bus side. Higher elevation ratios will imply lower voltage levels handled by the bank of SCs, but at the same time more switching and conduction losses of the converter. A good choice for the maximum elevation ratio will range from 2.58 to 3.5 times from the bank of SCs voltage to the desired 425 V dc at the dc bus. In this way the current levels are relatively low, the losses due to high currents are reduced and therefore the efficiency of the APU unit remains within acceptable levels.

Having the capacitance C_{sc} expressed in terms of the desired energy extraction percentage, the needed energy change in the bank and the required minimum voltage at the bank of SCs, the maximum allowed elevation ratios for the converter can be accounted. The maximum elevation ratio of 2.58 implies a minimum voltage at the bank of SCs of $v_{sc_f} = 164.6$ V dc. By replacing this value and the desired energy change at the bank of SCs $\Delta E_{sc} = 120$ kJ in Eq. (II.33) a capacitance $C_{sc} = 1.56$ F is found. In the case of a maximum elevation ratio of 3.5 used, the final value at the bank of SCs is $v_{sc_f} = 425/3.5 = 121.43$ V dc.

In this last case the capacitance obtained is $C_{sc} = 2.87$ F. Hence, by taking the converter losses and the maximum desired elevation ratios for the interfacing converter into account, it is found that the values for the desired capacitor lie in the range $[1.56, 2.87]$ F, with a minimum allowed voltage at the bank of SCs in the range $[121.43, 164.6]$ V dc. In these cases, the maximum allowed voltages for the bank of SCs lie in the range $[313.53, 425]$ V dc, which guarantee the operation of the APU dc-dc interfacing converter as a boost in the whole range. With this information, a series connection of 23, 58 F 15 V dc, BPAK0350-15EA SC packs from Maxwell has been chosen as the energy storing unit for the APU. The final values for the bank of SCs are $C_{sc} = 2.52$ F and 345 V dc as maximum operating voltage.

Now that a suitable bank of SCs has been found, the dimensioning of the inductor L_{apu} can take place. The inductance value to be used will depend on the maximum allowed current ripple of the converter at the maximum power condition, in this case 10 %. The maximum power condition presents when the maximum elevation ratio is demanded, and therefore, when the minimum allowed voltage is present at the bank of SCs. With the bank of SCs used in this work, a minimum voltage $v_{sc_f} = 345\sqrt{1 - 0.85} = 133.6$ V dc is to be achieved. As the converter is expected to work under CCM, an estimated duty cycle can be obtained from the relationship $v_{bus} = v_{sc}/\hat{u}_3$ (Erickson *et al.* [29]), where $\hat{u}_3$ is the applied PWM duty cycle to switch u_3. Under these conditions $425 = 133.6/\hat{u}_3 \;\Rightarrow\; \hat{u}_3 = 0.3144$ with $\hat{u}_3 \,\epsilon\, [0, 1]$.

The APU dc-dc interfacing converter is operated by using centered pulse, single-update mode, PWM with a switching frequency of $f_{sw} = 20$ kHz. The maximum power to be extracted from the SCs is $p_{sc}^{\max} = 120000/45 = 2.66$ kW, and therefore the demanded current is $i_{sc} = 2666.66/133.6 = 19.96$ A. A maximum variation of 1.996 A above and below this value is allowed as ripple. The allowed peak to peak variation during the ON condition of switch $\bar{u}_3$ is then $2 * 1.996 = 3.992$ A. This peak to peak variation occurs during the conduction state of switch $\bar{u}_3$ and therefore during $(1 - \hat{u}_3)\, T_{sw}$, with $T_{sw} = 1/f_{sw}$. From the inductance voltage/current relationship

$$v_{L_{apu}} = L_{apu}\, \frac{d\, i_{L_{apu}}}{dt} = v_{sc}, \tag{II.34}$$

it can be obtained that: $133.6 = L_{apu}\, 3.992/((1 - 0.3144)/20000)$ and therefore a minimum value of $L_{apu} = 1147.25$ μH is needed to comply with the desired ripple specifications. A $L_{apu} = 1600$ μH inductance in series with a $r_{L_{apu}} = 200$ mΩ parasitic resistance has been used in the experimental platform, and therefore, a less than 10 % current ripple is expected at the maximum load condition of the converter. A $C_{bus} = 6000$ μF 450V dc capacitor is used as linking capacitor among the APU dc-dc interfacing converter, the step-up stage and the dc-ac inversion stage.

The current specifications for the semiconductors must stand expected peak current at the inductor L_{apu}, and therefore around 25 A. The switches must be able to support the voltage level of the dc bus, and therefore a minimum voltage rating of 425 V dc is needed. A standard Semikron SKM100GB123D 1200 V dc, 100 A IGBT bridge with 2 V dc drop for the IGBTs and 0.8 V drop for each of the antiparallel diodes is used.

II.1.5 Computing device and signal acquisition

The computing device is in charge of making all the calculations and delivering the PWM signals with the appropriate duty cycles to drive the switching devices. The duty cycles to be used are determined by the control algorithms which run on a floating point microprocessor which is used as computing device. The physical signals are read by the current/voltage sensors, whose outputs are conditioned by means of filters implemented with operational amplifiers and then fed to an analog to digital conversion module. The digital signals are taken then by the microprocessor through a parallel port.

The duty cycles of the PWM signals generated by the computing and sensing units are fed to a switch drivers, which are in charge of conditioning the voltage/current levels from the logical levels provided by the computing device to the voltage/current levels needed by the switching devices.

Computing unit

An Analog Devices ADSP21364 EZ kit lite starter kit module is used as computing device. The ADSP21364 32-bit/40-bit floating-point floating point processor has been configured to run at 331.776 MHz. This ADSP provides of 16 configurable PWM outputs.

The PWM outputs are configured to generate a regular centered-pulse, single-update mode PWM signals at $f_{sw} = 20$ kHz. The control algorithms are implemented in such a way that they run in sync with the PWM signals generated. The PWMSYNC signal is used to trigger the reading of the ADC data by using Direct Memory Access (DMA).

Sensing unit

Two MAX1324ECM, 8 channel simultaneous sampling analog to digital converters (ADCs) from Maxim are used as interfaces from the sensing devices to the processor. The ADCs are installed in the analog to digital conversion module. The conversions are synchronized using the PWM-SYNC signal provided by the ADSP. The resulting data from the conversion is read by the ADSP using DMA through the DAI (Digital Audio Port) configured as a fast speed parallel port and therefore, the sampling frequency is $f_s = f_{sw} = 20$ kHz.

For the current measurements, closed-loop hall-effect transducers with 200 kHz bandwidth from LEM are used. One 100 A rms LA100-P current sensor is used to measure the output current of the dc-ac inversion stage. Two 50 A rms, LA55-P current sensors are used to measure the current provided by the FC unit and the current extracted/injected from/towards the bank of SCs.

Tree 500 V dc max LV25-P closed-loop hall-effect voltage transducers with 10 kHz bandwidth from LEM are used to measure the voltage at the terminals of the FC unit, the voltage at the terminals of the bank of SCs and the voltage at the dc bus. One AD215-AY voltage sensor is used to measure the output voltage of the dc-ac inversion stage.

The voltage/current levels provided by the sensors are conditioned to voltage/current levels suitable of being fed to the analog to digital conversion module. In the case of the currents measurements, this task is achieved by using continuous-time differential low-pass filters implemented with operational amplifiers. As fast variations are expected in most of the current measurements, the high-frequency components of the signals obtained from the sensors are removed by using low-pass filters. In the case of the voltage sensors, as most of the voltages are dc, the signals are just scaled to meet the input specifications of the ADCs used.

II.2 Conditioning System Control objectives

As mentioned before, the energy conditioning system architecture used is based on a multiple stage power inverter architecture. From Fig. II.1, it is clear that, besides the FC unit, there are three other blocks that form the energy conditioning system. The FC unit is just considered as a black-box power supply with certain electrical characteristics. The control loops included in the system take only into account the characteristics/limitations of the FC, but no direct control is applied over it. On the other hand, there are three other modules, the step-up stage, the dc-ac inversion stage and the auxiliary power unit. Each of this conversion stages has a particular control objective in order to assure that the energy conversion system will be able to deliver an output voltage shape as desired. All these control loops are "coordinated" by a higher-level control loop, which takes care that the provided output is within the system specifications and that all the modules are working within their limits.

II.2.1 Global power balance control

This control stage is in charge of holding the power balance between the power provided/demanded by the different power sources/loads that are present in the energy conditioning system. The power balance control loop must take into account the restrictions/limitations of the modules included in the system. The power is extracted from the FC unit by the step-up stage. As FCs in general do not support reverse currents, in this work a current unidirectional dc-dc converter has been used. This control loop must take into account that the power can only be extracted and not injected to the FC, and at the same tame consider the bandwidth limitation of the FC to fast variations on the output voltage. On the other hand, the power can be extracted or injected from/towards the bank of SCs depending on the load condition. This control stage must assure that the this extracted/injected power is within the allowed limits of the components/especifications.

Power balancing means that this control stage will control that neither the fuel-cell unit nor the supercapacitor bank try to provide more power than they are capable of, and therefore, meaning at the same time a protection system for the dc-ac inverter and its parts. The power balance is achieved by generating the appropriate references for the step-up control stage and the APU's interfacing converter control, these references are generated depending on the output power conditions in order to assure a regulated voltage at the common interconnection point of the step-up stage, the APU and the dc-ac inversion stage. In this way, if the output power has reached the maximum power allowed to be supplied by the FC unit, then a reference command is generated and given to the APU control stage, in order to guarantee a steady dc bus voltage,

until the overload condition is overcome. After the bank of SCs has been depleted, this stage generates a reference that will allow the charging process to start, this process will continue until the maximum voltage level of the bank is reached.

This control stage monitors all the voltages and currents present in the system, and with these inputs generates the APU and step-up stage control references, taking into account, the available power that can be supplied by the FC unit, the power demanded to the system at the output, and the power supplied or received by the bank of SCs.

II.2.2 Step-up stage - input current control -

In order to be able to control the power extracted from the FC unit, the input current to the step-up stage (output current of the FC unit) has been chosen as the variable to be controlled by this control loop. The current reference is generated by the global power balance control loop. The input current control is achieved by controlling the PWM duty cycle applied to switch u_1 of the converter presented in Fig. II.6. The changes in the input current provoke, as a side effect, a change in the voltage at the high-voltage side of the step-up converter. These changes are read by the global power balance control and the adequate input current reference is generated in order to achieve steady voltage $v_{bus} = v^{\text{hvs}}$.

II.2.3 APU - supercapacitor bank current control -

For the control of the auxiliary power unit the current extracted/injected from/towards the banks of SCs has been chosen as the control variable. The control of this current permits the biderectional operation of the device, allowing to charge or to extra power the bank of SCs. The direction of this current is determined by the operation of switches u_3 and $\bar{u}_3$ of the converter presented in Fig. II.12. The input/output current reference for the SCs is generated by the global power balance control. If the bank of SCs is discharged, and there is enough available power at the FC unit, a positive current reference is generated in order to allow the charge of the bank of SCs. On the other hand, if an overload presents, a negative current reference is generated in order to allow the energy to flow from the bank of SCs to the dc bus, and in this way, provide the needed power above the FC power limitation.

II.2.4 Dc-ac inversion stage - output voltage control -

The dc-ac inversion stage must assure that a good ac voltage is provided at the output of the energy conditioning system. This conversion stage interacts only as a load with the step-up and APU stages. From the global power balance control point of view, the dc-ac inversion stage is seen as a dc load.

As the energy conditioning system must be able to feed linear and/or nonlinear loads, the control scheme used must assure good rejection of the harmonics of the fundamental frequency (50 Hz). The control used must allow good harmonic rejection and good tracking of the fundamental 50 Hz frequency by controlling the PWM duty cycles applied to switches u_2, $\bar{u}_2$, u_2^* and $\bar{u}_2^*$ of the full-bridge dc-ac inverter presented in Fig. II.11.

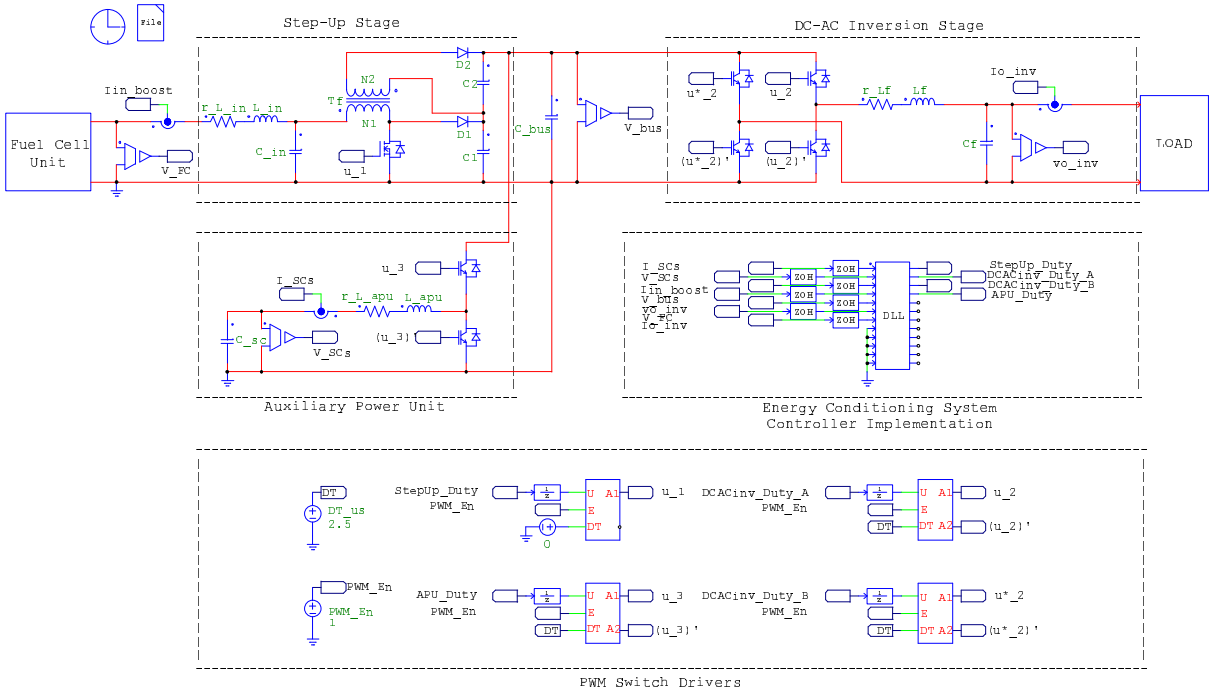


Figure II.13: Energy conditioning system simulation environment.

II.3 Conditioning System Simulation Environment

The simulations of the behavior of the power converters that form the energy conditioning system, working under hard switching conditions, are performed using PSIM®. This is a commercial software specially designed for the simulation of power electronics circuits and its control. PSIM® uses nodal analysis with the trapezoidal rule integration algorithm as solver, and a fixed time step throughout the simulation. PSIM® implements an interpolation technique which calculates the exact switching instants, significantly reducing the error due to the misalignment of switching instants and discrete simulation points [69].

This software allows the simulation of control algorithms working over switching power converters by allowing the user to employ a combination of mathematical blocks simultaneously with electrical switching devices such as diodes, IGBTs, MOSFETs, BJTs, etc.. This characteristic lets the designer to test control algorithms over the switched system, instead of using the averaged model, reflecting in a better way the expected behavior of the closed-loop system under analysis.

II.3.1 Description of the simulation modules

The power converters used in the simulations are built by using standard PSIM® components such as: voltage sources, resistor-inductor branches, single-phase transformers, diodes, capacitors, resistors and MOSFET and IGBT switches. The working conditions of the physical components are simulated by also considering the parasitic losses at the linear components and saturation voltages at the switching devices. Fig. II.13 shows the implementation of the converters that form the energy conditioning system, PWM modulators and control algorithm under PSIM®.

A regular, centered-pulse, single-update mode, pulse-width modulation (PWM) scheme is implemented to drive all the power converters. A switching frequency of $f_{sw} = 20$ kHz is used to generate the PWM signals. The PWM modulators are built by comparing a triangular signal with peak to peak amplitude 1 and a dc offset of 0.5 with the duty cycle $\hat{u} \; \epsilon \; [0, 1]$ at the target switching frequency f_{sw}. A one switching/sampling period delay ($T_{sw} = 1/f_{sw}$) is added at the input of the PWM modulator to account for the PWM load register delay present in the experimental setup. A 2.5 μs dead time has been included into the PWM modulators when generating complementary PWM signals, $\hat{u}$ and $\hat{\bar{u}}$, to account for the non-instantaneous switching capabilities of the IGBT modules used on the APU and the dc-ac inversion stages of the experimental setup. The PWM synchronization signal is used to latch the measured signals, and therefore the sampling frequency is also $f_s = f_{sw} = 20$ kHz, reflecting the sampling/switching behavior present on the experimental platform.

The control algorithms are implemented in C++ code, using the same code that will later be used over the experimental setup. The C++ code of the control algorithms is used to generate a DLL block which reads the input variables from the simulation environment and gives as output the appropriate duty cycles to be used by each of the conversion modules. The control algorithm is implemented directly in the z-domain using a sampling frequency of f_s. Zero-order hold (ZOH) blocks with a sampling period of $T_s = 1/f_s$ have been added between the sampled signals and the DLL block in order to have a realistic consideration of the ADCs to be used on the experimental setup (described in Section II.1.5).

Part 2

– Conditioning System Control Design –

CHAPTER III

Step-Up Converter Control - Input Current Control -

All models are wrong, but some are useful.
George Edward Pelham Box

This Chapter presents the input current control scheme used on the step-up stage. A description of the system identification procedure used to obtain a model of the plant suitable for control purposes is given. After the model of the plant has been obtained, a discrete-time controller is designed and tested by means of numerical simulation.

The purpose of the input current control loop is to control the current that is provided by the fuel cell i_{fc}, by means of changes in the applied PWM duty cycle to the switch u_1. Fig. III.1 shows the general block diagram of the control scheme used for the step-up stage. The input current reference is generated by the power balance control loop, in order to maintain a regulated voltage at the dc bus, which is shared by the step-up and the APU stages. This scheme offers the possibility of imposing a hard limit to the input current reference amplitude, and therefore, protecting the components against excessive current values. In order to develop the input current controller, first a model of the input current response to variations on the duty cycle must be known.

A description of the general considerations and methodology followed to find a model for the step-up converter suitable for control purposes is given in Section III.1. The plant identification procedure is presented in Section III.1.1. Some considerations must be taken into account before performing the tests, these are discussed in Section III.1.2. Section III.1.3 describes the application of the procedure presented in Section III.1.1 and the considerations given in Section III.1.2 first, over a simulation environment, and latter over the experimental platform. After, a model of the converter has been obtained, the input current controller is designed, the design of this controller is described in Section III.2. The controller is latter tested over a simulation environment. The general considerations taken for the test of the controller are given in Section III.3, and finally the results of the input current reference changes are discussed in Section III.3.1.

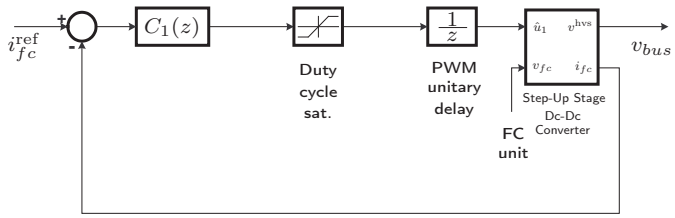


Figure III.1: General block diagram of the control architecture for the step-up stage.

III.1 Step-up converter modeling

The power converter used in the step-up stage (see Fig. II.6) has only one commanded switch u_1, and two free-wheeling diodes D_1 and D_2. As mentioned in II.1.2, under steady-state operation at a desired dc output voltage, the converter can take up to five different topological states during a single PWM switching period of the main switch u_1.

Moreover, Sype et al. [92] and Zhao et al. [106] assume that this converter follows a fixed and unique sequence of four different topological states depending on the conduction states of u_1, D_1 and D_2. As shown in Section II.1.2 (see Figs. II.7, II.8, II.9 and II.10), there are various sequences of topological states that can present depending on the desired output power, input and output voltages, etc., with a total of nine different possible sequences during a single PWM switching period of the main switch u_1 (according to Vento [96]). This behavior is caused by the free-wheeling diodes which work independently of the commanded switch u_1, introducing more topological states into the dynamics of the system than main switch positions, and therefore making it difficult to find an averaged model. Up to now, there are no generalized mathematical models of this kind of converters useful for control purposes that can be found in the literature.

In order to design a controller for the scheme of Fig. III.1, a model of the input current variations to variations on the duty cycle must be known. Due to the complexity of the structure, the development of useful mathematical models of the converter for control purposes becomes difficult, making the closed-loop control of these devices a challenging task. Some examples of the difficulties found on the analysis and modeling of this type of power converters can be found in the work of Pérez-Rivas in [66] and Pérez-Rivas *et al.* in [67].

The input current filter L_{in} and C_{in} is added to the original configuration of Fig. I.3(c) (Zhao et al. [106]) with the purpose of protecting the FC unit from the high-frequency, discontinuous input current shape of the converter. And therefore, under steady-state operation, a dc current is demanded from the FC. Profit can be obtained from the addition of the input current filter from a converter modeling perspective. The addition of this filter makes it possible to perform a small-signal swept-sine analysis from the changes in the current demanded from the FC i_{fc} in front of changes on the applied PWM duty cycle to switch u_1. With the resulting data of the small-signal swept-sine analysis, frequency-domain system identification techniques can be used to obtain the nominal plant models to be used in the design of the controllers.

III.1.1 Duty cycle to input current model identification procedure

Let $\hat{u}_1$ be the PWM duty cycle applied to switch u_1. The procedure to be followed to find a valid frequency-domain model of the variations in the input current to variations on the duty cycle is:

1. Fix the value of the input voltage source to $v_{fc} = v_{fc_{ss}}$. Where $v_{fc_{ss}}$ is the mid scale value of the input voltage specifications.
2. Determine the desired output power condition for the test by choosing the appropriate values for the load resistor R and a desired output voltage level v_{ss}^{hvs}. The steady-state output power is determined by the desired output voltage v_{ss}^{hvs} and the load resistor R by the relationship: $p_{ss}^{\text{hvs}} = v_{ss}^{\text{hvs}} i_{ss}^{\text{hvs}} = (v_{ss}^{\text{hvs}})^2/R$. Where v_{ss}^{hvs}, i_{ss}^{hvs} and p_{ss}^{hvs} are the steady-state voltage, current and power delivered at the high-voltage side of the step-up stage, respectively.
3. Connect the load resistor R to the output and bring the converter to steady state at the desired v_{ss}^{hvs} output voltage by finding an appropriate value for the applied duty cycle $\hat{u}_{1_{ss}}$.
4. Perform small-signal swept-sine analysis around $\hat{u}_{1_{ss}}$, having as input the applied duty cycle and as output the input current. From the obtained data discard the known intrinsic time delays (microprocessor register loads, etc.) included in the system, if any.
5. Repeat steps 1 to 4 for the converter under different load conditions.
6. From the small-signal swept-sine analysis results obtained, select a representative Bode (gain and phase) plot to be used as the nominal plant.
7. Fit a continuous-time system to the selected Bode plot.
8. Include in the resulting system the appropriate time delays if necessary (discarded time delays during the data acquisition, etc.).

III.1.2 Small signal swept-sine analysis setup and test considerations

The purpose of the use of this methodology in this work is to obtain a model of the system for the variations on the input current in front of variations on the duty cycle. The use of the small signal swept-sine analysis is based on the assumption that the system under analysis behaves in an almost linear form around the desired operating point. In this way, if the changes performed over the input signal are small enough, the changes on the output signal can be approximated by a linear relationship.

To perform a small signal swept-sine analysis, first, the system must be brought to the desired operating point. The analysis can be performed once the system has reached its steady state and the values of the desired input and output variables can be considered constant. Then, a sinusoidal disturbance with known amplitude and frequency is applied to the input variable. If the amplitude of the input disturbance is small enough, the variations of the output variable around its steady-state value will have a sinusoidal form with known frequency, amplitude and phase shift.

In the system, these relationships can be summarized in the following form:

$$\hat{u}_1(t) = \hat{u}_{1_{ss}} + \tilde{u}_1(t) \tag{III.1}$$

$$\Downarrow$$

$$i_{fc}(t) = i_{fc_{ss}} + \tilde{i}_{fc}(t). \tag{III.2}$$

with

$$\tilde{u}_1(t) = \varepsilon \sin(\omega t),$$
$$\tilde{i}_{fc}(t) = A \sin(\omega t + \phi),$$

where $\hat{u}_1(t)\ \epsilon\ [0,1]$ (applied PWM duty cycle to switch u_1) and $i_{fc}(t)$ (input current) are the input and output variables respectively. $\hat{u}_{1_{ss}}$ and $i_{fc_{ss}}$ are the steady-state values at the desired operating point. $\tilde{u}_1(t)$ is the sinusoidal disturbance applied to the input variable, with known amplitude ε and frequency ω. $\tilde{i}_{fc}(t)$ is the resulting variation of the input current around $i_{fc_{ss}}$. Because of the linearity assumption, this response must have a sinusoidal shape with known frequency ω, amplitude A and phase shift ϕ.

By performing a sweep of the parameter ω for a frequency range $[\omega_1, \omega_2]$ of interest, a gain/phase shift vs. frequency plot can be constructed for the system under analysis. The gain in such plot would be the ratio of the output/input (A/ε) sinusoid amplitudes, and the phase shift would be the resulting phase-shift value (ϕ) of the output with respect to the input sinusoids. The resulting plot would then reflect the behavior of the linearized system around the operating point.

Before performing the test, it is mandatory to determine the maximum allowable disturbance amplitude (ε) around the steady-state value of the input signal $(\hat{u}_{1_{ss}})$. This amplitude must be big enough to allow the proper reading of the variations of the output signal $(\tilde{i}_{fc}(t))$, but at the same time small enough to avoid the damage of any physical component in the system while assuring the validity of the linearity assumption. The determination of this maximum amplitude is usually done by experimentation, starting from a very small ε and going up until an appropriate value is found. The suitability of a value of ε is determined by several aspects that need to be accounted before doing the tests such like ADC/DAC resolution, maximum voltage/current ratings in the physical components, etc..

The desired output voltage level v_{ss}^{hvs} must be kept constant on all the tests. The reason for doing this is because the purpose of the application of this technique is to obtain a model that reflects the behavior of the system as if it were under normal operation condition. The normal operation condition of the overall system will be to provide a regulated output voltage $v^{\text{hvs}} = v_{ss}^{\text{hvs}}$. The output power condition of the test is determined by the value of the load resistor R at the desired output voltage v_{ss}^{hvs}. At each output power condition the appropriate steady-state duty cycle $\hat{u}_{1_{ss}}$ is determined empirically, and this determines the value of $i_{fc_{ss}}$.

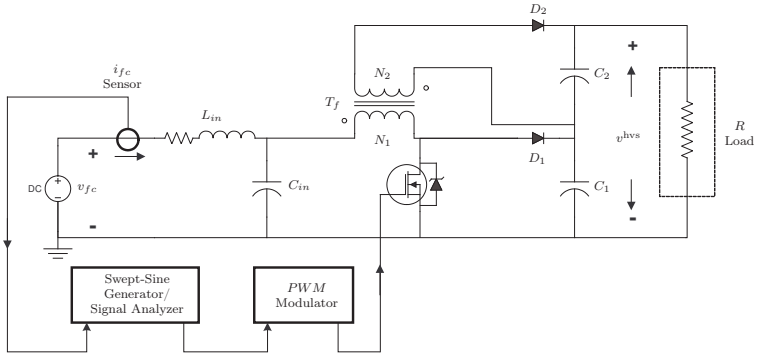


Figure III.2: Swept-sine analysis experimental setup scheme.

A schematic diagram of the swept-sine analysis experimental setup is presented in Fig. III.2. The steady-state duty cycle value $\hat{u}_{1_{ss}}$ is fed to the swept-sine generator/signal analyzer, which feeds a PWM modulator that drives the commanded switch u_1. The swept-sine generator will produce small-signal sinusoidal variations around $\hat{u}_{1_{ss}}$ with known amplitude and phase shift, for a specified frequency range $[\omega_1, \omega_2]$. At the same time the signal analyzer will read the amplitude and phase shift of the input current variations $\tilde{i}_{fc}(t)$. By analyzing the system responses in the frequency range $[\omega_1, \omega_2]$, an empirical bode plot of the changes on the input current as a function of the changes in the duty cycle is generated.

III.1.3 Experimental setup model identification

Recalling the conversion requirements given for the step-up stage in Section II.1.2, the following desired input/output characteristics are stated:

- Input:
  - Input voltage (v_{fc}): from 24 V dc up to 36 V dc depending on the load condition.
  - Maximum power: 1 kW.
- Output:
  - Output voltage (v^{hvs}): Regulated 425 V dc.

As a first step, in order to gain some insight into the dynamical behavior of the converter, a small-signal swept-sine analysis has been performed over a simulation model as presented in [57]. The simulation environment used and the considerations taken to perform the simulations are described in detail in Section II.3. The time step used on the solver of the simulation environment in this case is $4.5 \cdot 10^{-7}$ s. Following the criteria explained in III.1.1 and III.1.2 the values used for the small-signal swept-sine analysis are determined. The desired input voltage has been fixed to $v_{fc_{ss}} = 30$ V dc, value that lies in the middle of the range given in the specifications ([24..36] V dc). The desired output voltage value used in all tests is $v_{ss}^{\text{hvs}} = 400$ V dc. Table III.1 summarizes the parameters used on each particular output power condition to perform the small-signal swept sine analysis. The measured values of the steady-state input/output voltages used are included.

p_{ss}^{hvs}	v_{ss}^{hvs}	$v_{fc_{ss}}$	$i_{fc_{ss}}$	R	$u_{1_{ss}}$	ε
200 W	400.03 V dc	30.0 V dc	6.8834 A dc	800.00 Ω	0.6184580	$3.0000 \cdot 10^{-3}$
300 W	400.04 V dc	30.0 V dc	10.3435 A dc	533.33 Ω	0.6214500	$6.3750 \cdot 10^{-3}$
400 W	400.05 V dc	30.0 V dc	13.8249 A dc	400.00 Ω	0.6241980	$9.7500 \cdot 10^{-3}$
500 W	400.07 V dc	30.0 V dc	17.3174 A dc	320.00 Ω	0.6268610	$1.3125 \cdot 10^{-2}$
600 W	400.08 V dc	30.0 V dc	20.8044 A dc	266.67 Ω	0.6294850	$1.6500 \cdot 10^{-2}$
700 W	400.09 V dc	30.0 V dc	24.3017 A dc	228.57 Ω	0.6322180	$1.9875 \cdot 10^{-2}$
800 W	400.10 V dc	30.0 V dc	27.8298 A dc	200.00 Ω	0.6348880	$2.3250 \cdot 10^{-2}$
900 W	400.11 V dc	30.0 V dc	31.3765 A dc	177.78 Ω	0.6375630	$2.6625 \cdot 10^{-2}$
1000 W	400.12 V dc	30.0 V dc	34.8977 A dc	160.00 Ω	0.6403320	$3.0000 \cdot 10^{-2}$
1100 W	400.13 V dc	30.0 V dc	38.4788 A dc	145.45 Ω	0.6430830	$2.0000 \cdot 10^{-2}$
1200 W	400.14 V dc	30.0 V dc	42.0704 A dc	133.33 Ω	0.6458300	$2.0000 \cdot 10^{-2}$
1300 W	400.15 V dc	30.0 V dc	45.6592 A dc	123.08 Ω	0.6486210	$2.0000 \cdot 10^{-2}$
1400 W	400.15 V dc	30.0 V dc	49.2541 A dc	114.29 Ω	0.6515260	$2.0000 \cdot 10^{-2}$
1500 W	400.11 V dc	30.0 V dc	53.0023 A dc	106.67 Ω	0.6546097	$2.0000 \cdot 10^{-2}$

Table III.1: Small-signal swept-sine analysis simulation test parameters.

The small-signal swept-sine analysis has been performed over the simulation model using the parameters of Table III.1 from 10 Hz up to 10 kHz (half of the sampling/switching frequency used, $f_s = 20$ kHz), with output power conditions from 200 W up to 1500 W with increments of 100 W from test to test. For all the output power conditions, 200 linearly distributed points in the LOG_{10} frequency scale are generated, and the amplitude ε for the excitation source is kept constant for all the frequency range. The minimum output power condition is set to 200 W to match the expected parasitic losses of the dc-ac inversion stage which is fed by the step-up converter. The maximum 1500 W output power test condition is set above the 1 kW specification to evaluate the behavior of the converter beyond the maximum power specification.

Fig. III.3 shows the small-signal swept-sine analysis results for the simulation model under the fourteen different load conditions of Table III.1. From the results obtained it can be seen that the converter presents a very uniform behavior when working within the minimum (200 W) and maximum (1.5 kW) output power conditions used on the test. By analyzing the gain and phase characteristics at the beginning of the band (10 Hz) it can be found that: At 200 W output power condition, the gain of the converter is about 47 dB and it increases more or less uniformly with each increase of output power, reaching about 52 dB for the 1.5 kW test. On the other hand, the phase of the converter at 200 W lies around 63 ° and it decreases as the output power condition is increased, reaching about 14.5 ° at 1.5 kW.

At the maximum frequency used on the test (10 kHz), the gain and phase shift have the following behavior: At 200 W output power condition, the gain of the converter lies around −23 dB and this gain increases more or less uniformly as the output condition increases, achieving −9 dB under the 1.5 kW test. The phase shifts behave similarly, having −234 ° at 200 W and increasing with the output power condition up to −195 ° at the 1.5 kW test. A resonant peak can be observed in the gain plots at about 620 Hz. Associated to these resonant peaks phase drops varying from −170 ° for the 200 W test up to −150 ° for the 1.5 kW test are present.

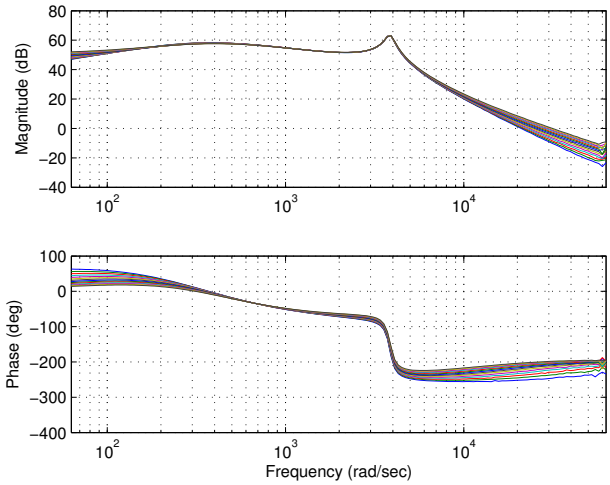


Figure III.3: Small-signal swept-sine analysis results for the simulation model of the converter at different working points. Input variable: variations on the duty cycle $\tilde{u}_1(t)$. Output variable: variations on the input current to the converter $\tilde{i}_{fc}(t)$.

In general, it can be observed that all the gain and phase traces for the intermediate output power tests are confined between the traces for the minimum and the maximum output power conditions. Having the previous results in mind, the minimum desired output power condition for the test over the experimental setup is set to 180 W, approximately the minimum load that will be always present at the output of the step-up stage, consisting of the parasitic losses of the full-bridge dc-ac inverter. The midpoint output power level 500 W, and 1000 W to match the maximum output power on the specifications of the system.

The small-signal swept-sine analysis over the experimental setup is implemented by using a HP 35670A dynamic signal analyzer. This device is able to produce a swept-sine signal with a desired amplitude for a frequency range $[\omega_1, \omega_2]$ at the desired input/output channel. The response of the system is read by another channel and processed to look for the gain and phase shift of the output respect to the input signals.

Because of the input/output voltage levels handled by the dynamic signal analyzer in use, the swept sine signal is taken from the HP 35670A and fed to one channel of the analog to digital conversion module of the experimental setup. The system response is read by the HP 35670A from the sensor conditioning board. In this way, the test is performed using low voltage levels and the resulting system response will include the influence of the sensing/conditioning elements included in the loop.

In order to be able to accurately retrieve the appropriate gain from the resulting data, the gains of the ADC channel and sensor/sensor-conditioning filter in use need to be known and adjusted before doing the tests. For all the output power conditions, 401 linearly distributed points in the LOG_{10} frequency scale are generated. The amplitude ε for the excitation source is kept constant for all the frequency range.

p_{ss}^{hvs}	v_{ss}^{hvs}	v_{fc}	$i_{fc_{ss}}$	R	$u_{1_{ss}}$	ε
180 W	400.90 V dc	30.00 V dc	6.90 A	883.04 Ω	0.613	$4.7935 \cdot 10^{-3}$
500 W	400.40 V dc	29.99 V dc	18.60 A	316.40 Ω	0.627	$1.4250 \cdot 10^{-2}$
1000 W	400.00 V dc	29.92 V dc	38.60 A	160.42 Ω	0.651	$1.4695 \cdot 10^{-2}$

Table III.2: Experimental small-signal swept-sine analysis parameters for each particular output power condition.

Again, following the criteria explained in III.1.1 and III.1.2 the values used for the small-signal swept-sine analysis over the experimental platform are determined. The desired input and output voltages used have the same values to the ones used over the simulation model $v_{fc_{ss}} = 30$ V dc and $v_{ss}^{\text{hvs}} = 400$ V dc. Table III.2 summarizes the parameters used on each particular output power condition to perform the small-signal swept sine analysis. The measured values of the steady-state input/output voltages used are included.

The small-signal swept-sine analysis has been performed using the parameters of table III.2 from 10 Hz up to 10 kHz (half of the sampling/switching frequency used, $f_s = 20$ kHz), at 180 W, 500 W and 1 kW output power conditions, with the fixed desired input voltage of $v_{fc} = 30$ V dc and a fixed desired output voltage $v_{ss}^{\text{hvs}} = 400$ V dc. The contribution of the delay introduced by the load of the pulse-width modulation (PWM) register of the ADSP is discarded during the data acquisition. Fig. III.4 shows the small-signal swept-sine analysis results for the system under different load conditions.

By following the procedure explained in III.1.1, it is now necessary to choose one of the small-signal swept-sine analysis results. This selection must contain all the main characteristics of the dynamic response of the converter, and therefore, the result from applying system identification techniques over this set of data will reflect, in a more accurate way, the dynamical behavior of the converter. From the results obtained it can be seen that the 500 W would be a representative choice as its path lies in the middle of the 180 W and 1000 W traces for the amplitude as well as for the phase shift. By using the system identification toolbox of MATLAB© a parametric black-box state-space identification algorithm was applied to the 500 W data, the following continuous-time three state system is found,

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \\ \dot{x}_3 \end{bmatrix} = \begin{bmatrix} -419.58 & 8686.8 & 1250.9 \\ -344.92 & -509.41 & -21053 \\ 17.435 & 421.01 & -565.48 \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \\ x_3 \end{bmatrix} + \begin{bmatrix} -3085.5 \\ -2457.5 \\ 476.35 \end{bmatrix} \tilde{u}_1,$$

$$\tilde{i}_{fc} = \begin{bmatrix} -52.586 & 89.157 & 121.95 \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \\ x_3 \end{bmatrix}, \tag{III.3}$$

where x_1, x_2 and x_3 are the internal states of the model, generated by a black-box system identification algorithm, and hence, with no physical interpretation.

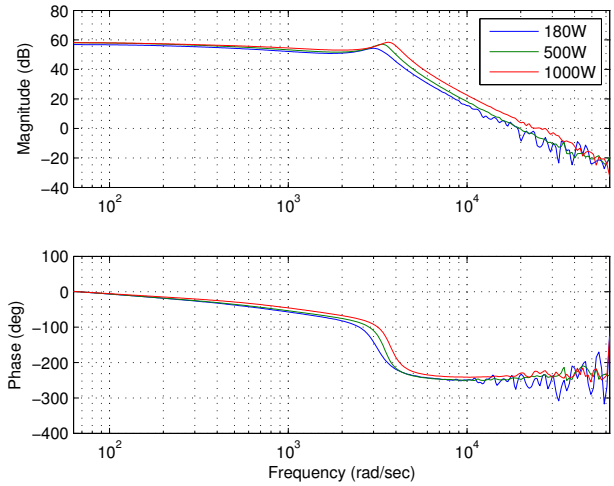


Figure III.4: Small-signal swept-sine analysis results for the system at different working points. Input variable: variations on the duty cycle $\tilde{u}_1(t)$. Output variable: variations on the input current to the system $\tilde{i}_{fc}(t)$.

By applying the laplace transform to the system of Eq. (III.3), the transfer function from the changes in the duty cycle $\tilde{u}_1$ to the changes in the input current of the converter $\tilde{i}_{fc}$ is found:

$$G_1(s) = \frac{\tilde{I}_{fc}(s)}{\tilde{U}_1(s)} = \frac{1.2443 \cdot 10^3\, s^2 + 1.7184 \cdot 10^8\, s + 6.6061 \cdot 10^{12}}{s^3 + 1.4945 \cdot 10^3\, s^2 + 1.2577 \cdot 10^7\, s + 8.8931 \cdot 10^9} \tag{III.4}$$

Eq. (III.4) has two stable complex conjugate zeros, with natural frequency $7.2864 \cdot 10^4$ rad/s and a damping of 0.9477. $G_1(s)$ has a real stable pole at 739.9521 rad/s and two stable complex conjugate poles, with natural frequency $3.4668 \cdot 10^3$ rad/s and a damping ratio of 0.1088, whose effects can be seen in the resonant peak of the 500 W trace in Fig. III.4. As the controller is to be implemented by means of an ADSP, it would be convenient to make the controller design directly in the z-domain. $G_1(s)$ must be converted to a discrete-time model. Eq. (III.5) shows the conversion result into the z-domain, by using a sampling frequency of $f_s = 20$ kHz and a ZOH.

$$G_1(z) = \frac{\tilde{I}_{fc}(z)}{\tilde{U}_1(z)} = \frac{0.4035\, z^2 + 0.4044\, z - 0.01429}{z^3 - 2.897\, z^2 + 2.826\, z - 0.928} \tag{III.5}$$

When implementing the controller, the load of the PWM register of the microprocessor introduces a delay of one sampling period $T_s = 1/f_s$. Its effects now need to be accounted into the nominal plant in order to consider its influence into the behavior of the overall system. Eq. (III.6) shows the actual nominal plant to be used in the controller design process. This controller must have as much bandwidth as possible while attaining good stability margins.

$$P_1(z) = \frac{1}{z}\, G_1(z) = \frac{0.4035\, z^2 + 0.4044\, z - 0.01429}{z^4 - 2.897\, z^3 + 2.826\, z^2 - 0.928\, z} \tag{III.6}$$

III.2 Input current controller design

Now, with the nominal plant $P_1(z)$ of Eq. (III.6), a discrete-time controller can be designed to regulate the current that the step-up stage demands from the main power source, the FC unit. After the controller has been designed, the analysis of its robustness and stability characteristics is performed in two stages. First, the stability margins are determined for the design using $P_1(z)$ and later, in order to assure a good robustness over all the output power condition range, the designed controller is evaluated against the experimental data obtained from the small-signal swept-sine analysis results. From this evaluation, the actual stability margins are obtained for the designed controller.

With $P_1(z)$ as the nominal plant, a discrete-time PID controller of the form

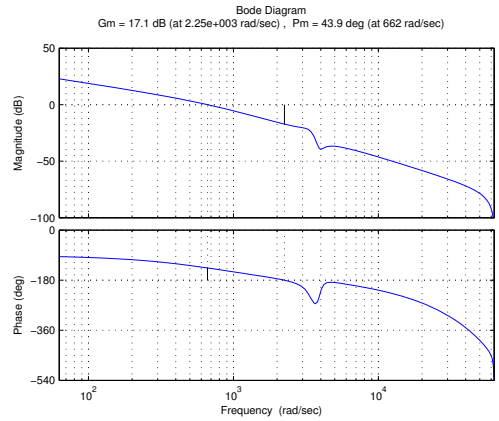
$$C_1(z) = K_{p_1} + \frac{K_{i_1}\, T_s}{2}\frac{(z+1)}{(z-1)} + \frac{K_{d_1}}{T_s}\frac{(z-1)}{z}, \tag{III.7}$$

has been designed by finding convenient pole/zero locations. The values of the coefficients are $K_{i_1} = 1.188$, $K_{p_1} = 1.349 \cdot 10^{-6}$, $K_{d_1} = 7.642 \cdot 10^{-8}$ and the sampling period $T_s = 1/f_s = 1/20$ kHz.

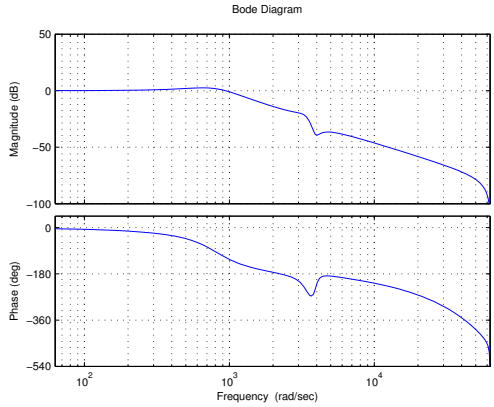
Fig. III.5 shows the open/closed-loop plots for the design of controller $C_1(z)$ using Eq. (III.6) as the plant to be controlled. Fig. III.5(a) shows the Bode plot for the open-loop transfer function $L_1(z) = C_1(z)\, P_1(z)$. This design presents a gain margin of 17.1 dB at 2250 rad/s and a phase margin of 42.9 ° at 662 rad/s. The Bode plot of the closed-loop transfer function $T_1(z) = C_1(z)\, P_1(z)/(1 + C_1(z)\, P_1(z))$ shows no significative closed-loop resonances as can be noticed by the peak closed-loop gain of $||T_1(z)||_\infty = 2.53$ dB at 658 rad/s shown in Fig. III.5(b). This fact can be also observed in the Nyquist plot for the open loop transfer function presented in Fig. III.5(c). Under these conditions this design still presents a good stability margin of $||S_1(z)||_\infty = 4.6$ dB at 889 rad/s according to Doyle *et al.* [27], where $S_1(z) = 1/(1+C_1(z)\, P_1(z))$ is the closed-loop output sensitivity transfer function whose Bode plot is shown in Fig. III.5(d).

Now that the controller has been designed and evaluated against the nominal plant $P_1(z)$, the stability margins of the controller $C_1(z)$ can be evaluated against the small-signal swept-sine analysis results obtained from the experimental platform. In order to be able to do this, the phase-shift contribution of the one sampling period delay introduced by the load of the PWM register of the ADSP is added to the phase shifts of the 180 W, 500 W and 1000 W small-signal swept-sine analysis results presented in Fig. III.4.

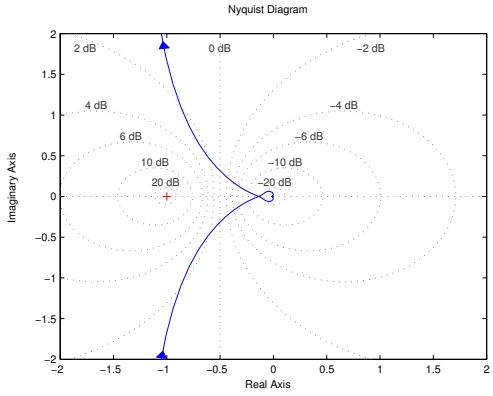
Fig. III.6 shows the open/closed-loop plots of controller $C_1(z)$ with the 180 W, 500 W and 1000 W small-signal swept-sine analysis results obtained from the experimental platform, the stability margins achieved are summarized in Table III.3 for each output power condition. By taking the worst case scenario for each case, the global set of stability margins is obtained.



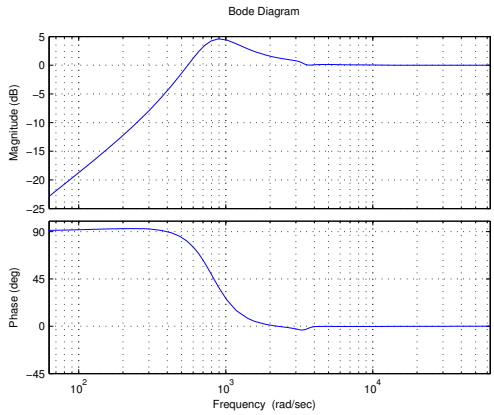
(a) Open-loop Bode plot ($L_1(z)$).



(b) Closed-loop Bode plot ($T_1(z)$).



(c) Open-loop Nyquist plot ($L_1(z)$).

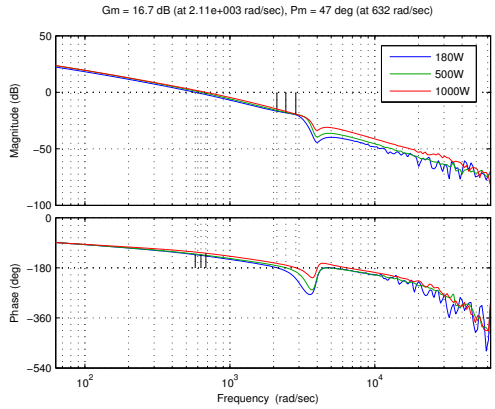


(d) Bode plot of the output sensitivity transfer function ($S_1(z)$).

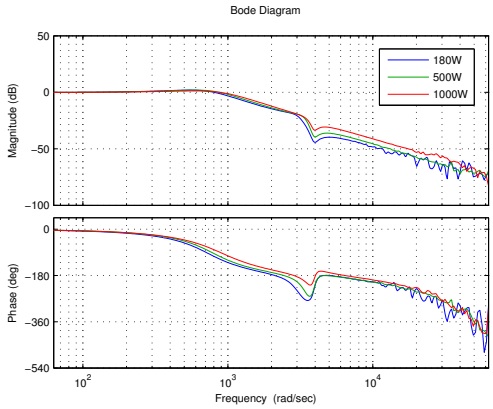
Figure III.5: Open and closed loop Bode and Nyquist plots for the controller $C_1(z)$ with the nominal plant $P_1(z)$.

Fig. III.6(a) shows the Bode plot for open-loop system. As it can be observed, this design presents a minimum gain margin of 16.7 dB at 2110 rad/s that presents for the 180 W data, and a minimum phase margin of 47 ° at 632 rad/s which presents for the 500 W data. Additionally no significative closed-loop resonances are present as can be noticed by the peak closed-loop gain of $||T_1(z)||_\infty = 2$ dB at 593 rad/s which presents for the 500 W data and is shown in Fig. III.6(b). This fact can be also observed in the Nyquist plot for the open-loop transfer function presented in Fig. III.6(c). Under these conditions this design presents a $||S_1(z)||_\infty = 4.06$ dB at 824 rad/s which is present in the 180 W case, where $S_1(z)$ is the closed-loop output sensitivity transfer function of Fig. III.6(d).

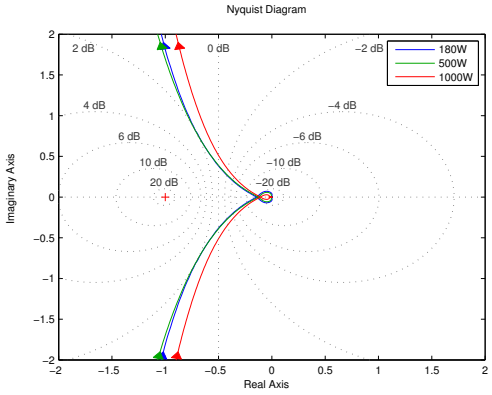
Now that a controller with good stability margins has been found, it is necessary to make some considerations that will affect its behavior over the switched system. The switched system includes an intrinsic saturation of the duty cycle value, which must lie within the range $[0, 1]$, as



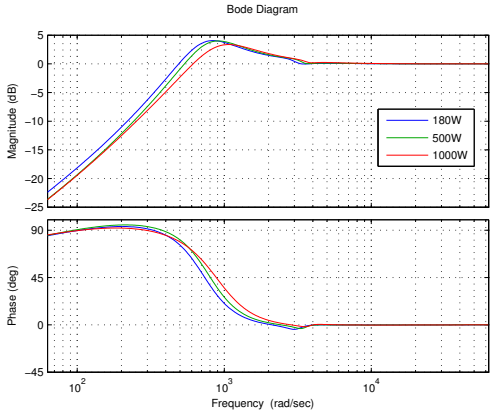
(a) Open-loop Bode plot.



(b) Closed-loop Bode plot.



(c) Open-loop Nyquist plot.



(d) Bode plot of the output sensitivity transfer function.

Figure III.6: Open and closed loop Bode and Nyquist plots for the controller $C_1(z)$ with the 180 W, 500 W and 1000 W experimental data.

p_{ss}^{hvs}	G.M.	P.M.	$\|\|T_1\|\|_\infty$	$\|\|S_1\|\|_\infty$
180 W	16.7 dB at 2110 rad/s	47.2 ° at 577 rad/s	1.98 dB at 544	4.06 dB at 824 rad/s
500 W	17.8 dB at 2430 rad/s	47 ° at 632 rad/s	2 dB at 593	4 dB at 913 rad/s
1000 W	19.3 dB at 2850 rad/s	52.4 ° at 683 rad/s	1.19 dB at 583	3.37 dB at 1070 rad/s

Table III.3: Stability margins of controller $C_1(z)$ against the small-signal swept-sine analysis results obtained from the experimental platform (including the one sampling period PWM register load delay).

defined by the structure of the system. There are some circumstances under which, the saturation of the control variable could cause the instabilization of the closed-loop system. If the saturation of the duty cycle value is reached, the feedback loop is broken, because of the output of the saturating duty cycle is not influenced by its input.

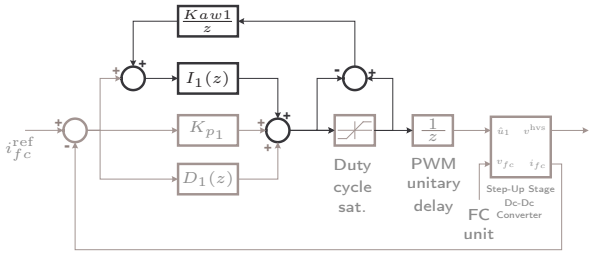


Figure III.7: Step-up stage control anti-windup loop.

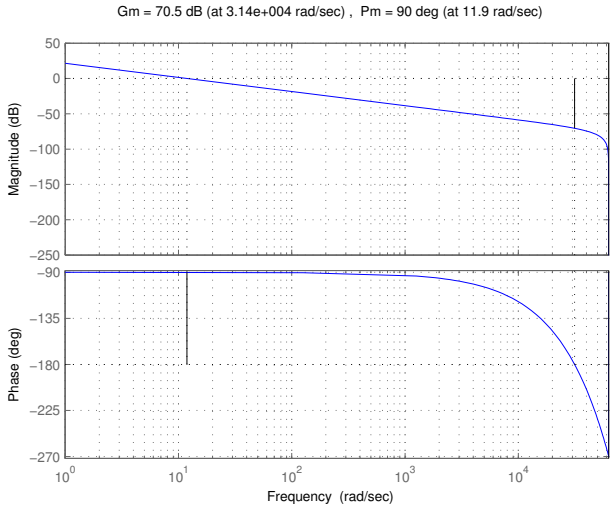


Figure III.8: Bode plot of the anti-windup open-loop transfer function L_{aw_1} used on the control of the step-up stage.

Lets suppose that the input current reference is constant and that the applied duty cycle value reaches the saturation level when having a constant charge at the output. The error signal will then be constant and the derivative part will have a null contribution. The proportional part will have a constant output. The integral part instead, will have a constant value at its input. This could drift the output of the integrator to very large values. Lets now suppose that the load is changed and that the input current level is equal to the current reference, the derivative and proportional parts output is zero. As the integral part value is very large, it could take a long time to recover, and this can cause the destabilization.

Fig. III.7 shows the input current control loop under such condition. An anti-windup loop has been added to the integral part in order to help it to recover from a saturation condition. The black boxes and lines show the new closed loop that is formed when the system reaches the saturation scenario. A one sampling period delay is included because of the sequential implementation of the algorithm. An anti-windup constant K_{aw_1} will determine, how fast is the integrator going to recover from a drift caused by a saturation state.

Care must be taken when adding this new loop, the stability of the system must be guaranteed. The open-loop transfer function of this new loop takes the following form:

$$L_{\mathrm{aw}_1}(z) = \left(\frac{K_{\mathrm{aw}_1}}{z}\right)\left(\frac{K_{i_1}\ T_s}{2}\frac{(z+1)}{(z-1)}\right) \tag{III.8}$$

The values $T_s = 1/f_s$ and K_{i_1} are known, the only free parameter is the constant K_{aw_1}. The stability of the anti-windup loop is checked by using the Jury test and assuming $K_{i_1} > 0$. After

applying the test to the open-loop transfer function $L_{\mathrm{aw}_1}(z)$, the condition imposed over the anti-windup constant K_{aw_1} can be summarized as:

$$0 \; < \; K_{\mathrm{aw}_1} \; < \; \frac{2}{K_{i_1} \; T_s}. \tag{III.9}$$

In this particular case the condition given above translates in $0 \; < \; K_{\mathrm{aw}_1} \; < \; 33670.59$. An anti-windup constant of $K_{\mathrm{aw}_1} = 10$ has been chosen. Fig. III.8 shows the Bode plot of the open anti-windup loop, as can be observed, a gain margin of 70.5 dB at 31400 rad/s and a phase margin of 90° at 11.9 rad/s guarantee the stability of the closed-loop system.

III.3 Input current control simulation results

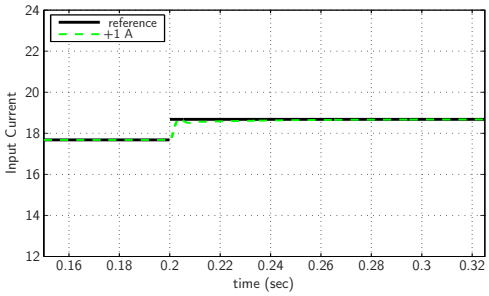
The designed discrete-time controller has been tested over a simulation model of the converter working under hard switching. The controller has been implemented using the same C++ code that will be used on the tests over the experimental setup. The commanded switch of the converter implemented on the simulation is operated by centered pulse, single-update mode, PWM with a switching frequency of $f_{sw} = 20$ kHz. The PWM synchronization signal is used to latch the measured signals, and therefore, the sampling frequency is also $f_s = 20$ kHz. A delay of one sampling period is included at the input of the PWM module to account for the delay introduced by the load of the PWM register that will be present at the ADSP of the experimental setup. The conduction losses of the semiconductors are included into the model, the parasitic losses of the components are also considered. The simulation environment used and the considerations taken to perform the simulations are described in detail in Section II.3. The time step used on the solver of the simulation environment in this case is $1 \cdot 10^{-6}$ s.

III.3.1 Input current reference step changes

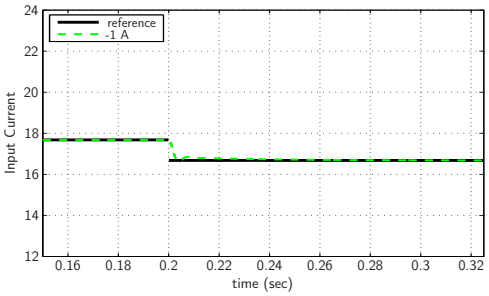
The input current control loop has been closed for the test. The converter is brought to operate at the desired output power condition p_{ss}^{hvs} by appropriately setting the values for desired output voltage v_{ss}^{hvs}, the load resistor R, and the input current reference $i_{fc_{ss}}^{\mathrm{ref}}$. The steady-state output power is determined by the desired output voltage v_{ss}^{hvs} and the load resistor R by the relationship: $p_{ss}^{\mathrm{hvs}} = v_{ss}^{\mathrm{hvs}} i_{ss}^{\mathrm{hvs}} = (v_{ss}^{\mathrm{hvs}})^2 / R$.

The input voltage source is set to $v_{fc} = v_{fc_{ss}}$. Where $v_{fc_{ss}} = 30$ V dc is the mid scale value of the input voltage range specifications ([24..36] V dc). The desired output voltage level is set to $v_{ss}^{\mathrm{hvs}} = 400$ V dc. The desired output power condition is set to $p_{ss}^{\mathrm{hvs}} = 500$ W. The input current reference found for the desired output power condition is set to $i_{fc_{ss}}^{\mathrm{ref}} = 17.68$ A dc. This current reference makes the step-up converter work at the desired output power condition, with the desired output voltage, compensating the switching and parasitic losses present in the device.

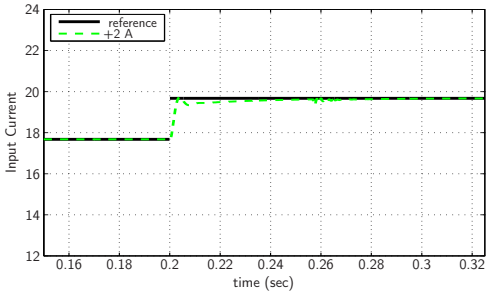
Once the converter is working at the desired steady-state condition, step changes are applied over the input current reference $i_{fc_{ss}}$. Step changes of magnitude +1 A dc, +2 A dc, +3 A dc, +4 A dc, +5 A dc, −1 A dc, −2 A dc, −3 A dc, −4 A dc and −5 A dc are applied over the input current reference that is given to the controller on the simulation environment.



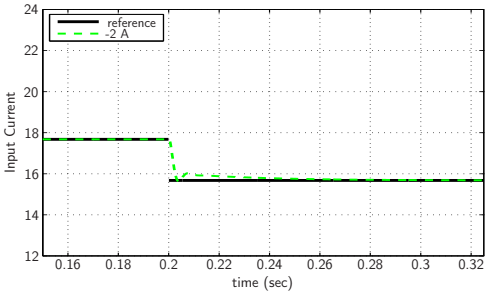
(a) +1 A reference change.



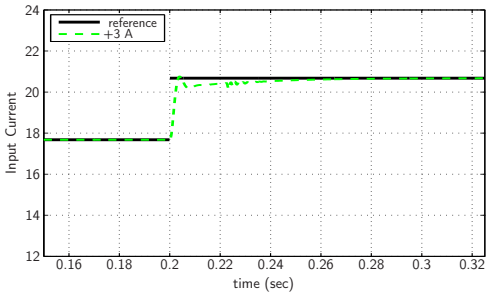
(b) -1 A reference change.



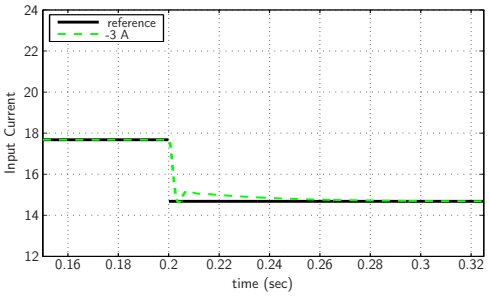
(c) +2 A reference change.



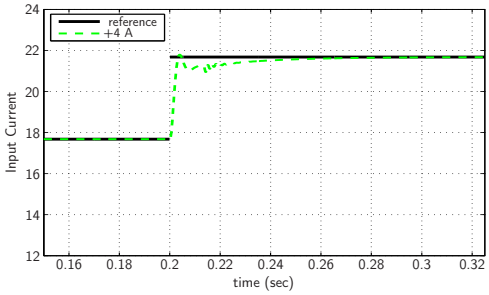
(d) -2 A reference change.



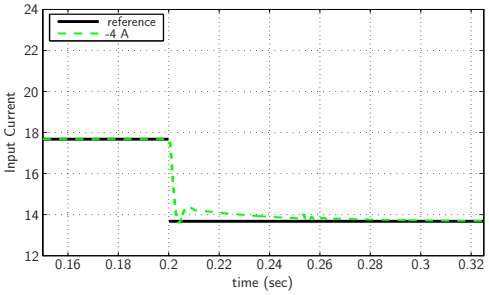
(e) +3 A reference change.



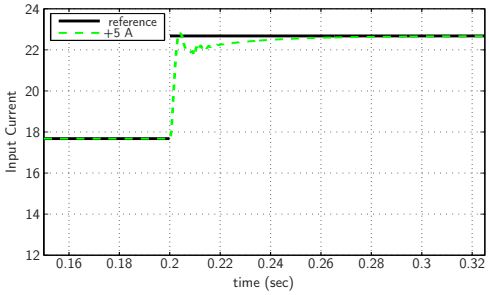
(f) -3 A reference change.



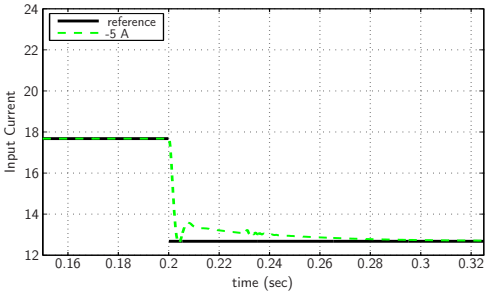
(g) +4 A reference change.



(h) -4 A reference change.



(i) +5 A reference change.



(j) -5 A reference change.

Figure III.9: Simulation results: Input current reference step changes.

Fig. III.9 shows the simulation results for the step reference changes over the steady-state input current reference. The black traces show the input current references applied to the input current controller. The dashed green traces show the input current response of the converter. As it can be observed, in all cases zero steady-state error is achieved over the input current of the converter for all the input current range covered on the test.

chapter IV

Full-Bridge DC-AC Inverter Control - Output Voltage Reference Tracking -

What leads and controls the world is not locomotives, but ideas.
Les Miserables - Victor Hugo

This Chapter presents the control architecture used on the dc-ac inversion stage of the conditioning system. The control methodology used is a discrete-time version of the Adaptive Feedforward Cancellation (AFC) control scheme. An analysis is performed over the discrete-time characteristics of the control strategy. The control design procedure is shown and then the simulation results are presented.

Feeding an isolated load with a dc-ac inversion system is a challenging task, generally due to the lack of knowledge about the nature of the load (linear or nonlinear) to be supplied. Because of the isolation characteristic, the system itself must keep the desired output voltage attributes (frequency, amplitude, THD_v, etc.,) within certain limits that determine the quality of service to be provided. These quality indicators are compromised by the presence of disturbances whose effects must be rejected. When designing dc-ac power inverters, nonlinear loads, such as diode rectifiers and fluorescent lights with electronic ballasts, are well known to be important sources of disturbances. When this class of load is fed by a dc-ac inverter, odd harmonics of the fundamental ac frequency, generally 50 Hz or 60 Hz, are introduced into the output voltage shape of the dc-ac inversion system [68].

As the nature of the load is not known *a priori*, for the purpose of producing a good sinusoidal output voltage shape, the control strategy must be able to reject periodic output disturbances. Also, the control strategy used on this stage must be robust in front of load level changes.

This Chapter describes the development of a discrete-time version of the Adaptive Feedforward Cancellation (AFC) control scheme to achieve the control/functioning goals stated before. Section IV.1 gives a brief description of the dc-ac inverter used. Section IV.2 presents the obtention of the continuous-time model of the converter used for the control design. Section IV.3 presents an introduction to the discrete-time version of the Adaptive Feedforward Cancellation (DT-AFC) control scheme. The characteristics of the DT-AFC are analyzed in Section IV.3.1,

where the validity of the assumptions made under the continuous-time case is evaluated. The design of the controller for the dc-ac inversion stage of the energy conditioning system is performed in Section IV.3.2. Finally, the performance of the controller designed is evaluated by means of numerical simulation in Section IV.3.3.

IV.1 Description of the dc-ac inversion stage

As mentioned in Section II.1.3, For this application a full-bridge dc-ac inverter topology with a LC filter has been chosen.

Recalling the design specifications for the dc-ac inversion stage given in Section II.1.3,

- Dc-ac inversion stage specifications:
  - Output voltage: 230 V ac rms.
  - Frequency: 50 Hz.
  - Maximum aparent output power: 5 kVA.
  - Maximum active output power: 3 kW.
  - Maximum output voltage total harmonic distortion ($\text{THD}_{\text{v}}^{\text{max}}$): 3 %.

The dimensioning of the components used on this conversion stage was performed in Section II.1.3 as well. Recalling the values of the electronic components given:

> *In summary, the dc-ac inversion stage consists of a full-bridge dc-ac inverter (see Fig. II.11) formed by two* 1200 *V dc,* 100 *A dc Semikron SKM100GB123D IGBT half-bridge modules with* 2 *V dc drop for the IGBTs and* 0.8 *V dc drop for each of the antiparallel diodes. The output voltage must follow a sinusoidal reference with a fundamental frequency of* 50 *Hz and* 230 *V ac rms feeding linear and nonlinear loads. The dc-ac inversion stage must be able to provide* 5 *kVA peak aparent power (overload condition), with a maximum active component of* 3 *kW composed by* 1 *kW supplied by the step-up stage and* 2 *kW given by the auxiliary power unit at the dc side of the inverter. The components used have the following values:* $v_{bus} = 425$ *V dc provided by the step-up stage and the auxiliary power unit when extra power is needed,* $L_f = 384$ μH *inductance in series with a* $r_{L_f} = 700$ $m\Omega$ *parasitic resistance,* $C_f = 81$ μF.
>
> *The dc-ac full-bridge inverter works at* $f_{sw} = 20$ *kHz, using regular three-level pulse-width modulation (PWM) with centered pulse.*

It is important also to remember from Section II.1.5 that the sampling frequency $f_s = 20$ kHz coincides with the switching frequency $f_{sw} = 20$ kHz used to operate the switches through PWM.

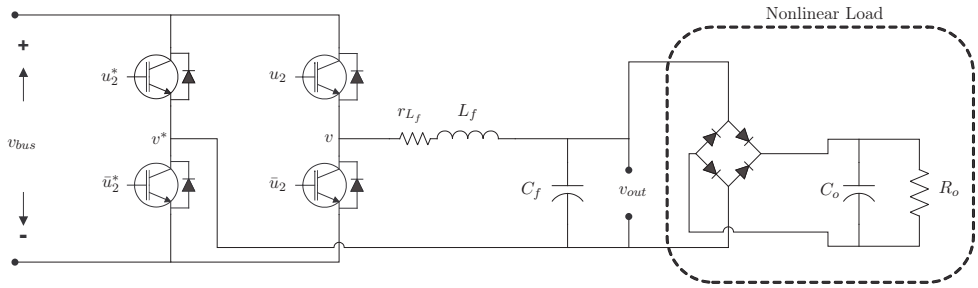


Figure IV.1: Full-bridge dc-ac inverter with a non-linear load (full-bridge diode rectifier with a RC load).

IV.2 Full-bridge dc-ac inverter modeling

Fig. IV.1 shows the schematic electronic diagram of the full-bridge dc-ac inverter feeding full-bridge diode rectifier with a RC load. The full-bridge dc-ac inverter is formed by two legs composed by the pairs of switches u_2,$\bar{u}_2$ and u_2^*,$\bar{u}_2^*$ respectively. The switches u_2 and $\bar{u}_2$ work in a complementary way, which means that when u_2 conducts $\bar{u}_2$ does not and viceversa. u_2^* and $\bar{u}_2^*$ work complementarily as well. As the operation of the switches is complementary, the behavior of each leg can be described by the discrete variables

$$\breve{u}_2 = \begin{cases} 1 \; if \; u_2 \text{ conducts and } \bar{u}_2 \text{ does not} \\ -1 \; if \; \bar{u}_2 \text{ conducts and } u_2 \text{ does not,} \end{cases}$$

and

$$\breve{u}_2^* = \begin{cases} 1 \; if \; u_2^* \text{ conducts and } \bar{u}_2^* \text{ does not} \\ -1 \; if \; \bar{u}_2^* \text{ conducts and } u_2^* \text{ does not.} \end{cases}$$

By using the definitions above and considering the transistors u_2,$\bar{u}_2$,u_2^* and $\bar{u}_2^*$ as lossless ideal switches, the instantaneous voltages at points v and v^* of Fig. IV.1 can be found by using the relationships

$$v = v_{bus}\frac{(\breve{u}_2+1)}{2} \text{ and } v^* = v_{bus}\frac{(\breve{u}_2^*+1)}{2}.$$

Now let $\hat{u}_2,\ \hat{u}_2^* \,\epsilon\, [-1, 1]$ be the averaged duty cycles applied to each of the half-bridge modules characterized by $\breve{u}_2$ and $\breve{u}_2^*$ respectively. In order to get a suitable continuous-time model for control design purposes, the averaged duty cycles are used instead. When using the averaged values for the duty cycle, the averaged values for the voltages at v and v^* become

$$\hat{v} = v_{bus}\frac{(\hat{u}_2+1)}{2} \text{ and } \hat{v}^* = v_{bus}\frac{(\hat{u}_2^*+1)}{2}.$$

For this application a three-level single-update centered pulse PWM scheme has been chosen to operate the full-bridge dc-ac inverter. This modulation scheme offers some advantages such

as reduction of the harmonic content of the switching frequency (Holmes and Lipo [40]), and only one duty cycle command is generated to control the two legs that form the full-bridge dc-ac inverter. Having the PWM scheme into account, the first leg (u_2,$\bar{u}_2$) is driven by the averaged duty cycle command $\hat{u}_2$, and the second leg (u_2^*,$\bar{u}_2^*$) is driven by $\hat{u}_2^* = -\hat{u}_2$. The averaged differential voltage between points v and v^* is then

$$\hat{v} - \hat{v}^* = v_{bus}\frac{(\hat{u}_2 + 1)}{2} - v_{bus}\frac{(-\hat{u}_2 + 1)}{2} = v_{bus}\ \hat{u}_2. \tag{IV.1}$$

The average output voltage, that feeds the low pass filter formed by r_{L_f}, L_f and C_f in Fig. IV.1 is then $\hat{v} - \hat{v}^* = v_{bus}\,\hat{u}_2$. The output voltage of the dc-ac inverter v_{out} is the voltage at the terminals of C_f which is the filtered differential voltage between the two half-bridge modules. With Eq. (IV.1) as input voltage to the low pass filter, an averaged state space representation of the behavior of the system is obtained as follows

$$\begin{bmatrix} \dot{v}_{C_f} \\ \\ \dot{i}_{L_f} \end{bmatrix} = \begin{bmatrix} 0 & 1/C_f \\ \\ -1/L_f & -r_{L_f}/L_f \end{bmatrix} \begin{bmatrix} v_{C_f} \\ \\ i_{L_f} \end{bmatrix} + \begin{bmatrix} 0 & -1/C_f \\ \\ v_{bus}/L_f & 0 \end{bmatrix} \begin{bmatrix} \hat{u}_2 \\ \\ i_{out} \end{bmatrix},$$
$$v_{out} = \begin{bmatrix} 1 & 0 \end{bmatrix} \begin{bmatrix} v_{C_f} \\ i_{L_f} \end{bmatrix},$$
$$\text{with } \hat{u}_2 \in [-1, 1]. \tag{IV.2}$$

From Eq. (IV.2) the transfer function that models the influence of the applied averaged duty cycle $\hat{u}_2$ on the output voltage v_{out} is obtained, having

$$G_2(s) = \frac{v_{bus}}{C_f\ L_f\ s^2 + C_f\ r_{L_f}\ s + 1}. \tag{IV.3}$$

The influence of the output current i_{out} on the output voltage v_{out} is modeled by the transfer function $G_2'(s) = -(L_f\, s + r_{L_f})/(C_f\ L_f\ s^2 + C_f\ r_{L_f}\ s + 1)$. This has the physical interpretation of being the output impedance of the LC filter used. The output current passing through $G_2'(s)$ can be considered an output disturbance by the output voltage control scheme.

IV.3 Discrete-time adaptive feed-forward cancellation (DT-AFC)

Adaptive Feed-forward Cancellation (AFC) is a control technique that has been successfully used to selectively reject periodic output disturbances in continuous-time mechanical systems. This paper deals with the use of AFC to control the output voltage of an electrical system, in this case, a dc-ac full-bridge inverter, to produce a standard European ac voltage signal, 230 V ac rms and 50 Hz, accomplishing the design of the controller directly in the z-domain.

Adaptive Feed-forward Cancellation (AFC) is a control technique that allows the designer to reject or attenuate, in a selective manner, specific harmonics of periodic disturbance signals. AFC has successfully been used in mechanical systems ([9],[12] and [54]), to reject periodic disturbances that are harmonics of some fundamental frequency. It is interesting to note that under certain circumstances ([10],[11]), the AFC problem becomes equivalent to that of the Internal Model Principle (IMP) ([30]), and therefore, perfect disturbance rejection of the selected harmonics can be expected. The IMP states that a model of the disturbance must be included into the open-loop transfer function, requiring then, previous knowledge of the disturbance signal. The design and the equivalence of controllers between the AFC and IMP schemes were treated by Bodson in [8] and Messner and Bodson in [60], and a loop shaping approach is given by Byl *et al.* in [12] in order to help the designer in the selection of the design parameters.

The AFC approaches treated in [8], [9], [10], [11], [12], [54] and [60] assume continuous-time variables and controller design, although in practice, almost all controllers need to be implemented by means of digital computers, and hence, in discrete-time. This work deals with the design of an AFC controller directly in the z-domain as introduced in [56] and [58], being in this cases applied to the control of a full-bridge dc-ac inverter.

IV.3.1 DT-AFC characteristics analysis

In the continuous-time framework, the advantage on the use of the AFC control structure to reject periodic disturbances lies in the placement of an infinite gain on the open-loop transfer function at the desired ω_k frequency by means of the $R_k(s)$ resonator. By following the IMP, perfect disturbance rejection at such frequency can be expected. In order to obtain a feasible discrete-time realization, it needs to be shown that the main characteristics of the continuous-time realization are preserved. Fig. IV.2 shows the block diagram of the AFC closed loop. A proportional block with constant K_0 is added in order to help the reference tracking. Fig. IV.3 shows block diagram for the proposed discrete-time resonator.

Construction of the discrete-time resonator $R_k(z)$

The main difference between the continuous-time and the discrete-time realizations of the AFC controller resides in the construction of the $R_k(z)$ resonator modules. The $H(z)$ block in Fig. IV.3 can be any discrete-time integrator structure. The resonator shown in Fig. IV.3 can be expressed by the z-domain transfer function

$$R_k(z) = \frac{1}{2} g_k \left[H(z e^{-j\omega_k T_s}) e^{-j\varphi_k} + H(z e^{j\omega_k T_s}) e^{j\varphi_k} \right]. \tag{IV.4}$$

In this work, a Backward Euler integrator has been chosen for the $H(z)$ block, having then

$$H(z) = \frac{z}{(z-1)}. \tag{IV.5}$$

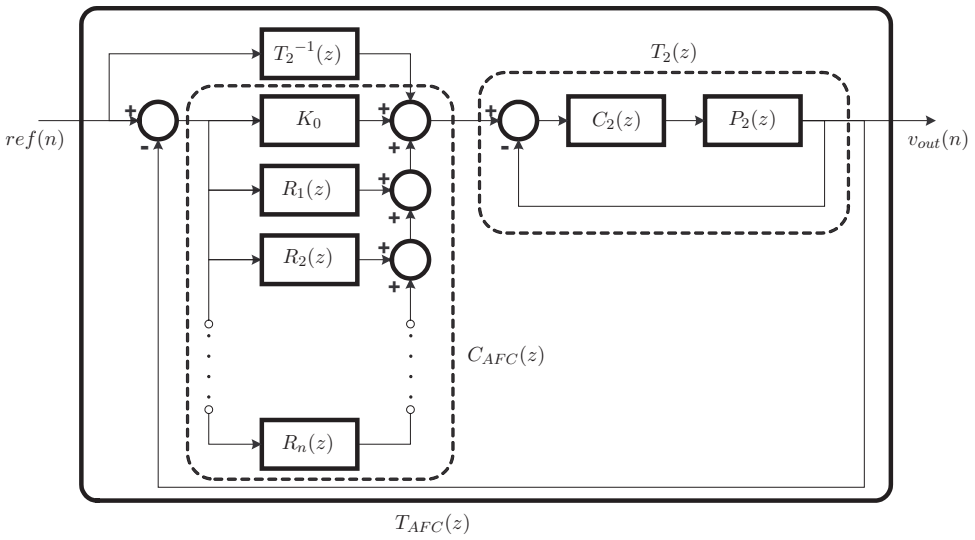


Figure IV.2: Discrete-time AFC controller structure, used for the control of the full-bridge dc-ac inversion stage.

By replacing Eq. (IV.5) into Eq. (IV.4) and simplifying, the z-domain transfer function of the resonator becomes

$$R_k(z) = g_k \frac{\cos(\varphi_k)z^2 - \cos(\omega_k T_s + \varphi_k)z}{z^2 - 2\cos(\omega_k T_s)z + 1}. \tag{IV.6}$$

Eq. (IV.6) shows the resulting structure for the discrete-time resonator implementation by selecting the first order structure of Eq. (IV.5) as integrator. The parameters involved in the discrete-time resonator structure are: g_k, ω_k, φ_k and T_s. Where g_k is a positive real gain, ω_k is the frequency, in rad/s at which the desired resonating gain is to be placed, φ_k is the phase-shift parameter for the kth resonator in rad, and finally $T_s = 1/f_s$ is the sampling period in seconds for the discrete-time system.

Phase of $R_k(z)$ at the resonating frequency ω_k

First, the phase and gain characteristics of the discrete-time resonator at the ω_k frequency are explored. The behavior of the system around the resonating frequency ω_k can be studied departing from Eq. (IV.4).

When the continuous-time frequency ω approaches ω_k, the z variable becomes $z = e^{j(\omega_k T_s + \varepsilon)}$, for a sufficiently small value of $|\varepsilon| \geq 0$. Having substituted this value in Eq. (IV.4) and simplifying, the resonator structure becomes

$$R_k(z) = \frac{1}{2} g_k \left[H(e^{j\varepsilon})e^{-j\varphi_k} + H(e^{j(2\omega_k T_s + \varepsilon)})e^{j\varphi_k} \right]. \tag{IV.7}$$

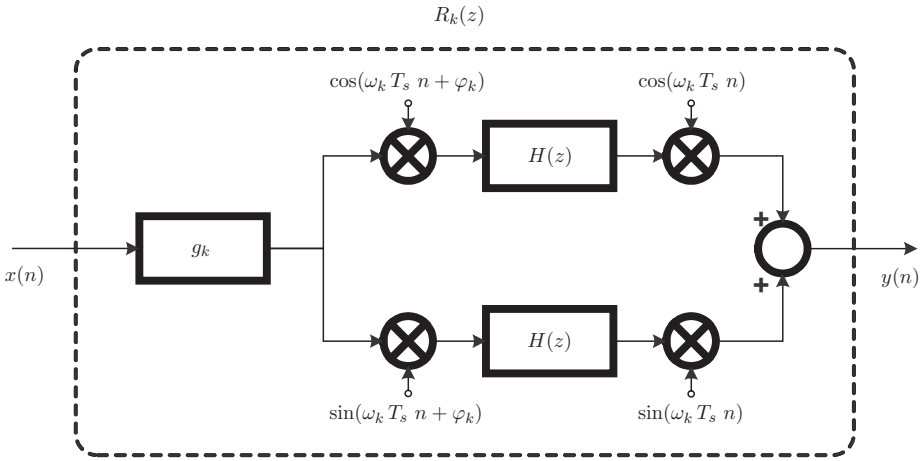


Figure IV.3: Discrete-time AFC resonator structure.

By substituting Eq. (IV.5) in Eq. (IV.7) the first half of Eq. (IV.7) can be rewritten as:

$$\frac{1}{2}g_k\left[H(e^{j\varepsilon})e^{-j\varphi_k}\right] = \frac{1}{4}g_k\left[\frac{e^{j(\frac{\varepsilon}{2}-\frac{\pi}{2}-\varphi_k)}}{\sin(\frac{\varepsilon}{2})}\right]. \tag{IV.8}$$

For the sake of simplicity, let us assume a unitary gain $g_k = 1$. As ε approaches zero from either right or left sides, the modulus of Eq. (IV.8) goes to infinite, as the denominator $\sin(\varepsilon/2)$ goes to zero. The effects of the second half of Eq. (IV.7) are marginal at this point, and Eq. (IV.8) dominates the behavior of the resonator structure $R_k(z)$.

When ε approaches zero from the left, which is equivalent to say that the input frequency approaches the resonating frequency from the left ($\omega \to \omega_k^-$), the phase shift of the system becomes

$$\angle\, R_k(e^{j\omega T_s})\big|_{\omega\to\omega_k^-} = -\varphi_k + \frac{\pi}{2}.$$

When ε approaches zero from the right, the phase component of the resonator structure becomes

$$\angle\, R_k(e^{j\omega T_s})\big|_{\omega\to\omega_k^+} = -\varphi_k - \frac{\pi}{2}.$$

Therefore, the phase shift of the resonator at the resonating frequency ω_k, is the average of

the phase shifts of the resonator when ω approaches ω_k from the right and from the left, hence

$$\angle R_k(e^{j\omega_k T_s}) = -\varphi_k. \tag{IV.9}$$

Phase of $R_k(z)$ at $\omega = 0$ and $\omega = \pi/T_s$

Let us now inspect the phase characteristics of the resonator structure at the dc frequency. When $\omega = 0$, then $z = e^{j\,0\,T_s} = 1$ and Eq. (IV.6) takes the form:

$$R_k(1) = g_k \frac{\cos(\varphi_k) - \cos(\omega_k T_s + \varphi_k)}{2 - 2\cos(\omega_k T_s)}. \tag{IV.10}$$

Let us assume $g_k = 1$. All the values in the equation above are real, and therefore $R_k(1)$ is a real number. A deeper inspection on the values would be necessary to determine the phase of such quantity.

The resonating frequency ω_k lies within the operating band and therefore $0 < \omega_k < \pi/T_s$, and then the denominator $(2 - 2\cos(\omega_k T_s))$ is always greater than zero, as the $\cos(\omega_k T_s)$ value is always lower than 1. In the numerator $(\cos(\varphi_k) - \cos(\omega_k T_s + \varphi_k))$, the ω_k frequency is fixed as the independent variable, as this value is determined by the disturbance frequency to be rejected. The sampling period T_s is fixed as well. The sign change conditions can be examined by looking at the locations of the zero crossings of the numerator. From the assumptions above the following phase conditions are imposed over $R_k(1)$,

$$\angle R_k(1) = \begin{cases} \pi \; if & \varphi_k < -\omega_k T_s/2, \\ 0 \; if & \varphi_k > -\omega_k T_s/2. \end{cases} \tag{IV.11}$$

At the maximum allowed frequency by the discrete-time system a similar analysis can be performed. When $\omega = \pi/T_s$, $z = -1$, Eq. (IV.6) takes the form:

$$R_k(-1) = g_k \frac{\cos(\varphi_k) + \cos(\omega_k T_s + \varphi_k)}{2 + 2\cos(\omega_k T_s)}. \tag{IV.12}$$

In this case the denominator $(2 + 2\cos(\omega_k T_s))$ is always positive. When examining the numerator $(\cos(\varphi_k) + \cos(\omega_k T_s + \varphi_k))$, the following conditions are derived from fixing ω_k as independent variable, with T_s fixed by the hardware constraints:

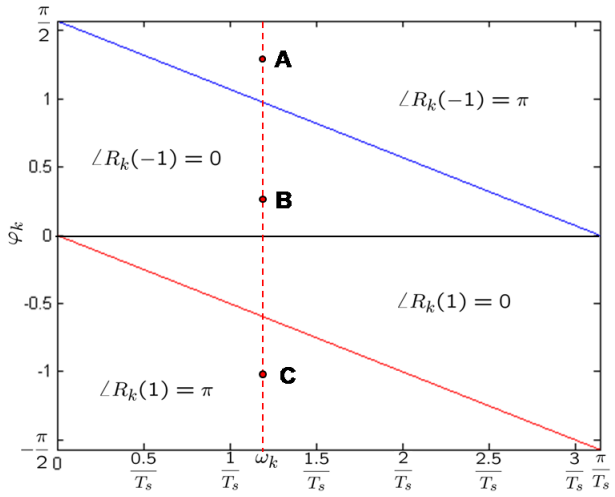


Figure IV.4: Phase-shift boundaries for $\omega = 0$ and $\omega = \pi/T_s$ for the discrete-time resonator structure $R_k(z)$.

$$\angle R_k(-1) = \begin{cases} 0 \; if & \varphi_k < (\pi - \omega_k T_s)/2, \\ \pi \; if & \varphi_k > (\pi - \omega_k T_s)/2. \end{cases} \tag{IV.13}$$

From the conditions above, it can be concluded that the resonator structure will have a phase drop of $-\pi$ rad at the resonating frequency ω_k, and the shift will be centered at $-\varphi_k$ as stated in Eq. (IV.9). The phase value at the beginning ($\omega = 0$) and at the end of the band ($\omega = \pi/T_s$) will be determined by Eq. (IV.11) and Eq. (IV.13).

A single resonator $R_k(z)$ can show three different combinations for the phase value at the start ($\angle R_k(1)$) and at the end of the band ($\angle R_k(-1)$) depending on the selection of ω_k and φ_k. Fig. IV.4 shows the phase-shift boundaries for the discrete-time resonator structure $R_k(z)$ as a function of the resonating frequency ω_k. The upper line shows the boundary condition imposed to $\angle R_k(-1)$ ($\omega = \pi/T_s$) by Eq. (IV.13). The lower line shows the boundary condition imposed to $\angle R_k(1)$ ($\omega = 0$) by Eq. (IV.11). As can be seen, a single resonator can change its start and finish phase values depending on the selection of the φ_k parameter. If φ_k = A is chosen (see Fig. IV.4), the start and finish phase values will be $\angle R_k(1) = 0$ and $\angle R_k(-1) = \pi$ respectively. If φ_k = B the start and finish angles would be, $\angle R_k(1) = 0$ and $\angle R_k(-1) = 0$. If φ_k = C, then $\angle R_k(1) = \pi$ and $\angle R_k(-1) = 0$.

Fig. IV.5 shows the effect on the change of the phase-shift parameter φ_k above or below the boundaries of Fig. IV.4. In this case a resonating frequency of $\omega_k = 10$ k rad/s has been chosen, the sampling frequency is 20 Hz which produces a sampling period of $T_s = 1/f_s = 50$ μs, a unitary gain g_k has been used, and three different values for the parameter φ_k have been considered. The φ_k values considered were, $\varphi_k = 1.396$ rad lying in the A region of Fig. IV.4, producing the

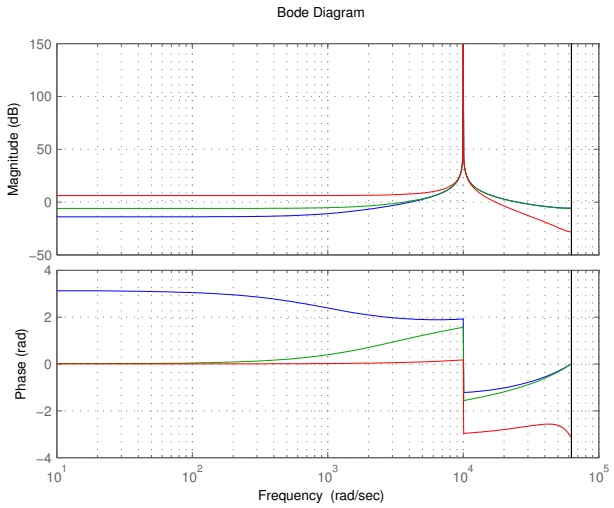


Figure IV.5: Bode diagram for a single resonator $R_k(z)$ using different values for the phase-shift parameter $\varphi_k(-0.349$ rad, 0 rad and 1.396 rad), $g_k = 1$, $\omega_k = 10,000$ rad/s, $T_s = 1/f_s = 50$ μs.

red trace in Fig. IV.5. The $\varphi_k = 0$ rad value lies in the B region, and produces the green trace, and $\varphi_k = -0.349$ rad lies in the C region producing the blue trace.

It is interesting to note that for the lower frequency range, when the resonating frequency ω_k is farther from the end of the band value ($\omega = \pi/T_s$), the phase-shift conditions are equivalent to the continuous-time conditions given by [12]. Conversely, these conditions will be equivalent if the sampling period trends to zero, which will make the discrete-time system response trend to the continuous-time one.

Gain characteristics of $R_k(z)$ at $\omega = 0$ and $\omega = \pi/T_s$

From Eq. (IV.10) the gain characteristics at $\omega = 0$ can be analyzed. Again, the values of ω_k and T_s are fixed by the conditions imposed by the problem to be solved. The phase-shift parameter φ_k is the independent variable. The gain growth or decrease regions at $\omega = 0$ ($|R_k(1)|$) can be determined by examining the location of the sign changes (see Fig. IV.4) and the inflection points of Eq. (IV.10) respect to the parameter φ_k. Assuming $g_k = 1$, only one inflection point is found for $R_k(1)$ ($\omega = 0$) when varying φ_k. This point is located at $(\pi - \omega_k T_s)/2$ having positive slope before the inflection point and negative slope after it.

It is also necessary to take into account the phase change conditions expressed in Fig. IV.4 for $R_k(1)$. These conditions have an straight forward interpretation respect to its relationship with the sign of $R_k(1)$. If $\angle R_k(1) = \pi$, then $R_k(1) < 0$ and if $\angle R_k(1) = 0$, therefore $R_k(1) > 0$. If a decrease in the value of φ_k produces an increase on $|R_k(1)|$ this increase will happen until φ_k reaches the inflection point at $(\pi - \omega_k T_s)/2$, and after the inflection point, a decrease on $|R_k(1)|$ must happen, until the sign change condition ($\angle R_k(1)$ changes from 0 to π) is reached at $-\omega_k T_s/2$. At $\varphi_k = -\omega_k T_s/2 \Rightarrow R_k(1) = 0$, and if φ_k continues decreasing, then $|R_k(1)|$ must increase again.

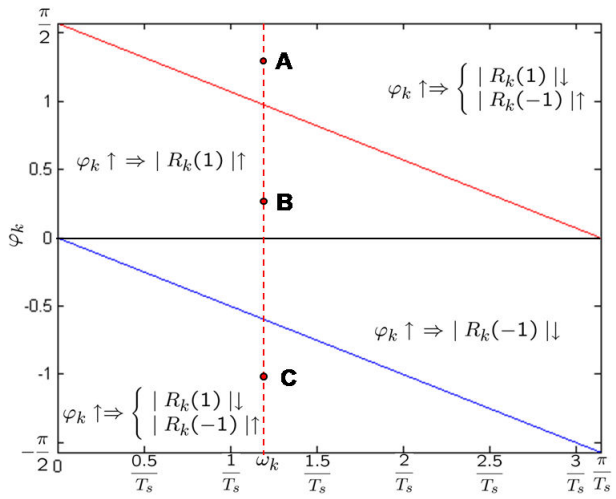


Figure IV.6: Gain growth/decrease boundaries for $\omega = 0$ and $\omega = \pi/T_s$ for the discrete-time resonator structure $R_k(z)$.

The relationship between the growth/decrease on the gain of the resonator $R_k(z)$ in function of ω_k at $\omega = 0$ can be summarized as follows:

- $|R_k(1)|$ decreases if φ_k increases and $\varphi_k > -\omega_k T_s/2$.
- $|R_k(1)|$ increases if φ_k increases and $-\omega_k T_s/2 < \varphi_k < (\pi - \omega_k T_s)/2$.
- $|R_k(1)|$ decreases if φ_k increases and $\varphi_k > (\pi - \omega_k T_s)/2$.

A similar analysis can be performed for the frequency at the end of the allowed band, where $\omega = \pi/T_s$, $z = -1$. In this case the gain increase/decrease characteristics can be studied departing from Eq. (IV.12). Again, ω_k and T_s are fixed by the problem statement and $g_k = 1$. The gain increase/decrease characteristics can be examined by determining the location of the sign changes (see Fig. IV.4) and the inflection points and of Eq. (IV.12) respect to φ_k. Only one inflection point is found at $-\omega_k T_s/2$, when varying φ_k, and the sign change condition is located at $(\pi - \omega_k T_s)/2$. In this case the increase/decrease relationship can be summarized as follows

- $|R_k(-1)|$ increases if φ_k increases and $\varphi_k < -\omega_k T_s/2$.
- $|R_k(-1)|$ decreases if φ_k increases and $-\omega_k T_s/2 < \varphi_k < (\pi - \omega_k T_s)/2$.
- $|R_k(-1)|$ increases if φ_k increases and $\varphi_k > (\pi - \omega_k T_s)/2$.

The relationships imposed over the growth/decrease of $|R_z(1)|$ ($\omega = 0$) and $|R_z(-1)|$ ($\omega = \pi/T_s$) are summarized in Fig. IV.6. The upper line shows the location of the inflection point of $R_z(1)$ when varying φ_k as a function of ω_k. The lower line shows the location of the inflection

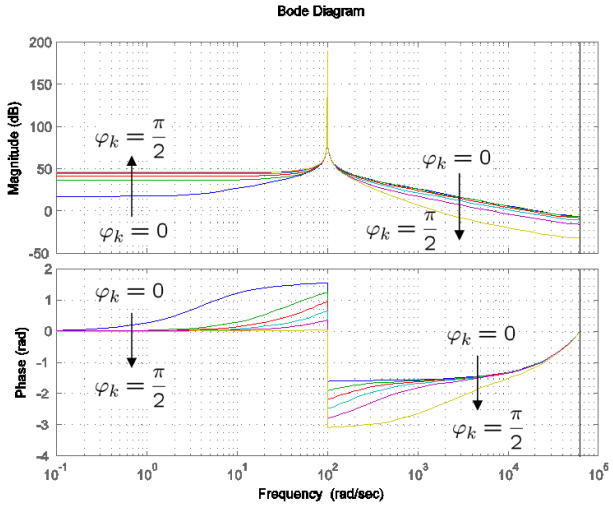


Figure IV.7: Effect of the change on the phase-shift parameter φ_k within the B region on a single resonator $R_k(z)$, with $\omega_k = 100$ rad/s, $T_s = 1/f_s = 50$ μs and $g_k = 1$ ($\varphi_k = 0.0349$ rad, 0.3316 rad, 0.6283 rad, 0.9250 rad, 1.2217 rad and 1.5184 rad).

point of $R_z(-1)$ when varying φ_k as a function of ω_k. It is interesting to note that the location of the inflection points of $R_k(1)$ and $R_k(-1)$ as a function of ω_k coincides with the location of the phase change boundaries presented in Fig. IV.4. For a single resonator $R_k(z)$ with resonating frequency ω_k, if φ_k is chosen to lie in the A area, an increase on the value of φ_k will cause a decrease in $|R_z(1)|$ and an increase on the value of $|R_z(-1)|$. If φ_k is chosen to lie in the B area, an increase on its value will cause an increase in $|R_z(1)|$ and a decrease $|R_z(-1)|$. If φ_k is chosen to lie in the C area, an increase on its value will cause a decrease in $|R_z(1)|$ and an increase in $|R_z(-1)|$.

Fig. IV.7 shows the effect over the gain and phase characteristics for a single resonator $R_k(z)$ with resonating frequency $\omega_k = 100$ rad/s, sampling period $T_s = 1/f_s = 50$ μs, unitary g_k gain and changes applied to the φ_k value within the B region. As can be observed, with values of φ_k lying within the B region, the start ($\angle R_k(1)$) and finish ($\angle R_k(-1)$) phases of the resonator are located at 0 rad. The upper boundary for $|R_k(1)|$ is located at $1.5683 \approx \pi/2$ rad, and the lower boundary for $|R_k(-1)|$ is located at $-0.0025 \approx 0$ rad. The angles used to change the φ_k values are: 0.0349 rad, 0.3316 rad, 0.6283 rad, 0.9250 rad, 1.2217 rad and 1.5184 rad. It can be noted in that as φ_k increases, $|R_k(1)|$ increases, and $|R_k(-1)|$ decreases as stated in Fig. IV.6.

IV.3.2 DT-AFC output voltage controller design

This new approach on the AFC controller design has been used to control the output voltage of a full-bridge dc-ac inverter (see Fig. IV.1), following the loop-shaping approach presented in [12]. The output voltage must follow a sinusoidal reference with a fundamental frequency of 50 Hz and 230 V ac rms. Disturbance rejection has been planned to take place in the first 30 harmonics and the inner closed loop has been designed to provide as much bandwidth as possible.

Inner-loop controller design

As a first step to be able to design the controller for the inner loop of the DT-AFC control scheme, the numerical values of the components used (recalled in Section IV.1), are substituted into Eq. (IV.3), obtaining

$$G_2(s) = \frac{1.3664 \cdot 10^{10}}{s^2 + 1823s + 3.215 \cdot 10^7}. \tag{IV.14}$$

The transfer function presented in Eq. (IV.14) has two stable complex conjugate poles with natural frequency $5.6701 \cdot 10^3$ rad/s and a damping ratio of 0.1607. As the controller is to be implemented by means of an ADSP, it would be convenient to make the controller design directly in the z-domain. $G_2(s)$ must be converted to a discrete-time model. Eq. (IV.15) shows the conversion result into the z-domain, by using a sampling frequency of $f_s = 20$ kHz and a ZOH,

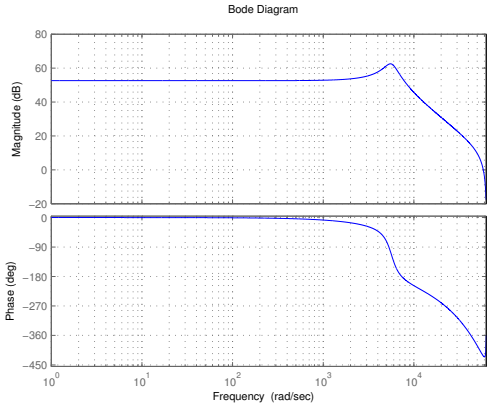
$$G_2(z) = \frac{16.46z + 15.97}{z^2 - 1.837z + 0.9129}. \tag{IV.15}$$

When implementing the controller, the load of the PWM register of the microprocessor introduces a delay of one sampling period $T_s = 1/f_s$. Its effects now need to be accounted into the nominal plant in order to consider its influence into the behavior of the overall system. Eq. (IV.16) shows the actual nominal plant to be used in the controller design process,

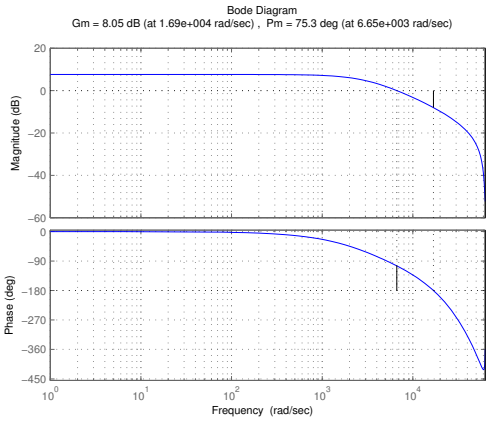
$$P_2(z) = \frac{1}{z} G_2(z) = \frac{16.46z + 15.97}{z^3 - 1.837z^2 + 0.9129z}. \tag{IV.16}$$

The inner-loop control is designed to provide as high closed-loop bandwidth as possible. The overall behavior of the AFC control loop is also determined by the behavior of the closed inner control loop (Byl *et al.* [12]), and therefore, the premise is to get a well behaved inner-loop control ($T_2(z)$ in Fig. IV.2). The sinusoidal reference tracking and periodic disturbance rejection capabilities will be provided by the AFC control loop. Having these facts in mind, a controller $C_2(z)$ has been designed by appropriate pole and zero location, obtaining

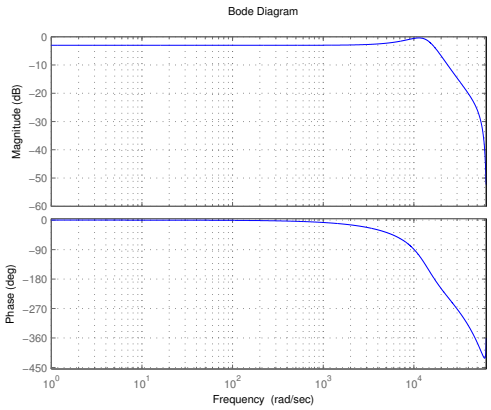
$$C_2(z) = \frac{0.0098z^2 - 0.018z + 0.008946}{z^2 - 0.934z + 0.06677}. \tag{IV.17}$$



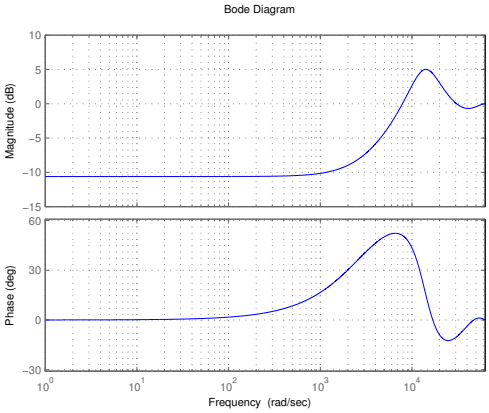
(a) Bode plot of the nominal plant ($P_2(z)$).



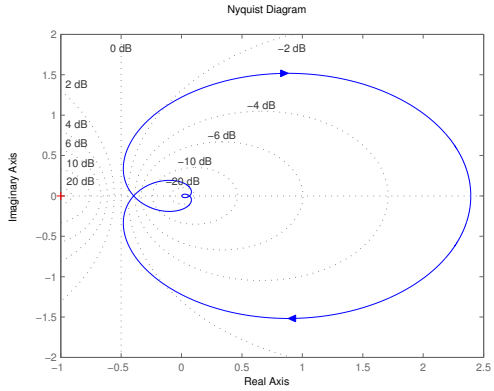
(b) Open-loop Bode plot ($L_2(z)$).



(c) Closed-loop Bode plot ($T_2(z)$).



(d) Bode plot of the output sensitivity transfer function ($S_2(z)$).



(e) Open-loop Nyquist plot ($L_2(z)$).

Figure IV.8: Open and closed loop Bode and Nyquist plots for the controller $C_2(z)$ with the nominal plant $P_2(z)$.

Fig. IV.8 shows the open/closed-loop plots for the design of the controller $C_2(z)$. Fig. IV.8(a) shows the Bode plot for the discrete-time transfer function $P_2(z)$ that models the behavior of the full-bridge dc-ac inverter. Fig. IV.8(b) shows the Bode plot for the open-loop transfer function $L_2(z) = C_2(z)\,P_2(z)$. As it can be observed, this design presents a gain margin of 8.05 dB at $1.69 \cdot 10^4$ rad/s, and a phase margin of 75.3 ° at $6.65 \cdot 10^3$ rad/s. The Bode plot of the closed-loop transfer function $T_2(z) = C_2(z)\,P_2(z)/(1 + C_2(z)\,P_2(z))$ presents no significative closed-loop resonances as can be noticed by the maximum peak closed-loop gain of $||T_2(z)||_\infty = -0.425$ dB at $1.14 \cdot 10^4$ rad/s shown in Fig. IV.8(c). This fact can be also observed in the Nyquist plot for the open-loop transfer function $L_2(z)$ presented in Fig. IV.8(e). Under these conditions this design presents a $||S_2(z)||_\infty = 5$ dB at $1.42 \cdot 10^4$ rad/s, where $S_2(z) = 1/(1 + C_2(z)\,P_2(z))$ is the closed-loop output sensitivity transfer function shown in Fig. IV.8(d), and that according to Doyle *et al.* [27] is an adequate stability margin.

Resonators-loop controller design

Having found an inner-loop controller $C_2(z)$ the inner control loop is closed, and therefore, the closed-loop transfer function $T_2(z)$ takes the form:

$$T_2(z) = \frac{0.16133(z + 0.97)(z^2 - 1.837z + 0.9129)}{(z + 0.2774)(z^2 - 1.837z + 0.9129)(z^2 - 1.211z + 0.5641)}. \tag{IV.18}$$

Eq. IV.18 acts as the new plant to be controlled by the DT-AFC control loop. As stated in Section IV.3.1, the phase shift of the resonator $R_k(z)$ at the ω_k frequency will be centered at $-\varphi_k$. As in the continuous-time case presented by Byl *et al.* in [12], a selection of $\varphi_k = \angle T_2(z_k)$ with $z_k = e^{j\omega_k T_s}$ will cause the AFC transmission loop to center all the phase shifts around 0 °, and therefore providing the system of the highest phase margin available.

The parameters g_k have been chosen by using the hyperbolic profile $g_k = 1.5 \cdot 10^{-2}(1/k^{0.9})$. This profile gives more gain to the low frequencies and less gain to the high frequencies. This shape allows the control system to provide the highest energy levels to the region of the fundamental frequency and the lower harmonics where the highest levels of disturbance are usually located. The feed-forward path ${T_2}^{-1}(z)$ will reinforce the tracking of the reference signal. As in this case the reference signal is a fixed 50 Hz (fundamental frequency) sinusoid, a constant value of ${T_2}^{-1}(z) = 1/(T_2(z_1))$ with $z_1 = e^{j\omega_1 T_s}|_{\omega_1 = 2\pi 50}$ has been chosen, and finally the proportional path K_0 has a value of 0.01.

Having chosen all the parameters, the resonators control loop takes the form

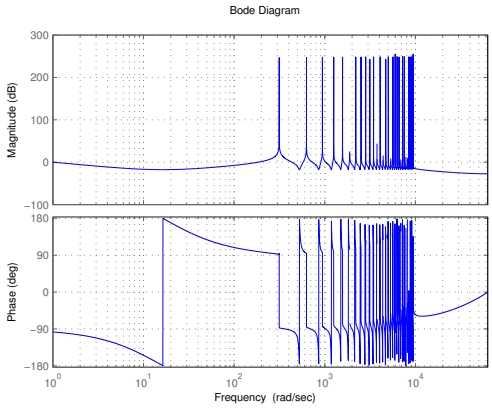
$$C_{AFC}(z) = K_0 + \sum_{k=1}^{30} R_k(z). \tag{IV.19}$$

k	f_k	ω_k	g_k	φ_k
1	50 Hz	$2\,\pi\,50$ rad/s	$1.500000000000000 \cdot 10^{-2}$	$-3.944793185550562 \cdot 10^{-2}$ rad
2	100 Hz	$2\,\pi\,100$ rad/s	$8.038300969022198 \cdot 10^{-3}$	$-7.894057669278164 \cdot 10^{-2}$ rad
3	150 Hz	$2\,\pi\,150$ rad/s	$5.580615870169522 \cdot 10^{-3}$	$-1.185228896256773 \cdot 10^{-1}$ rad
4	200 Hz	$2\,\pi\,200$ rad/s	$4.307618831238882 \cdot 10^{-3}$	$-1.582403107274952 \cdot 10^{-1}$ rad
5	250 Hz	$2\,\pi\,250$ rad/s	$3.523856829264056 \cdot 10^{-3}$	$-1.981390091673154 \cdot 10^{-1}$ rad
6	300 Hz	$2\,\pi\,300$ rad/s	$2.990577997128289 \cdot 10^{-3}$	$-2.382661290995805 \cdot 10^{-1}$ rad
7	350 Hz	$2\,\pi\,350$ rad/s	$2.603172951512286 \cdot 10^{-3}$	$-2.786700374824091 \cdot 10^{-1}$ rad
8	400 Hz	$2\,\pi\,400$ rad/s	$2.308395775021718 \cdot 10^{-3}$	$-3.194005736126330 \cdot 10^{-1}$ rad
9	450 Hz	$2\,\pi\,450$ rad/s	$2.076218232692529 \cdot 10^{-3}$	$-3.605092996335739 \cdot 10^{-1}$ rad
10	500 Hz	$2\,\pi\,500$ rad/s	$1.888388117691250 \cdot 10^{-3}$	$-4.020497505601424 \cdot 10^{-1}$ rad
11	550 Hz	$2\,\pi\,550$ rad/s	$1.733156748013828 \cdot 10^{-3}$	$-4.440776814308445 \cdot 10^{-1}$ rad
12	600 Hz	$2\,\pi\,600$ rad/s	$1.602611067483519 \cdot 10^{-3}$	$-4.866513079829807 \cdot 10^{-1}$ rad
13	650 Hz	$2\,\pi\,650$ rad/s	$1.491221793208652 \cdot 10^{-3}$	$-5.298315356889568 \cdot 10^{-1}$ rad
14	700 Hz	$2\,\pi\,700$ rad/s	$1.395005843911573 \cdot 10^{-3}$	$-5.736821700101634 \cdot 10^{-1}$ rad
15	750 Hz	$2\,\pi\,750$ rad/s	$1.311019423039750 \cdot 10^{-3}$	$-6.182700982312751 \cdot 10^{-1}$ rad
16	800 Hz	$2\,\pi\,800$ rad/s	$1.237038666349588 \cdot 10^{-3}$	$-6.636654301338132 \cdot 10^{-1}$ rad
17	850 Hz	$2\,\pi\,850$ rad/s	$1.171351477842811 \cdot 10^{-3}$	$-7.099415809565306 \cdot 10^{-1}$ rad
18	900 Hz	$2\,\pi\,900$ rad/s	$1.112617802116927 \cdot 10^{-3}$	$-7.571752754801439 \cdot 10^{-1}$ rad
19	950 Hz	$2\,\pi\,950$ rad/s	$1.059773408654293 \cdot 10^{-3}$	$-8.054464466104110 \cdot 10^{-1}$ rad
20	1000 Hz	$2\,\pi\,1000$ rad/s	$1.011962135755172 \cdot 10^{-3}$	$-8.548379955166274 \cdot 10^{-1}$ rad
21	1050 Hz	$2\,\pi\,1050$ rad/s	$9.684872190670334 \cdot 10^{-4}$	$-9.054353733252916 \cdot 10^{-1}$ rad
22	1100 Hz	$2\,\pi\,1100$ rad/s	$9.287757044684611 \cdot 10^{-4}$	$-9.573259368568404 \cdot 10^{-1}$ rad
23	1150 Hz	$2\,\pi\,1150$ rad/s	$8.923520108648823 \cdot 10^{-4}$	$-10.10598023479823 \cdot 10^{-1}$ rad
24	1200 Hz	$2\,\pi\,1200$ rad/s	$8.588180064478982 \cdot 10^{-4}$	$-10.65339683765213 \cdot 10^{-1}$ rad
25	1250 Hz	$2\,\pi\,1250$ rad/s	$8.278377968767289 \cdot 10^{-4}$	$-11.21637006691916 \cdot 10^{-1}$ rad
26	1300 Hz	$2\,\pi\,1300$ rad/s	$7.991259723584086 \cdot 10^{-4}$	$-11.79571972736047 \cdot 10^{-1}$ rad
27	1350 Hz	$2\,\pi\,1350$ rad/s	$7.724384279532829 \cdot 10^{-4}$	$-12.39219778035224 \cdot 10^{-1}$ rad
28	1400 Hz	$2\,\pi\,1400$ rad/s	$7.475651217937349 \cdot 10^{-4}$	$-13.00645591368785 \cdot 10^{-1}$ rad
29	1450 Hz	$2\,\pi\,1450$ rad/s	$7.243243092886530 \cdot 10^{-4}$	$-13.63900738740737 \cdot 10^{-1}$ rad
30	1500 Hz	$2\,\pi\,1500$ rad/s	$7.025579132418230 \cdot 10^{-4}$	$-14.29018361462070 \cdot 10^{-1}$ rad

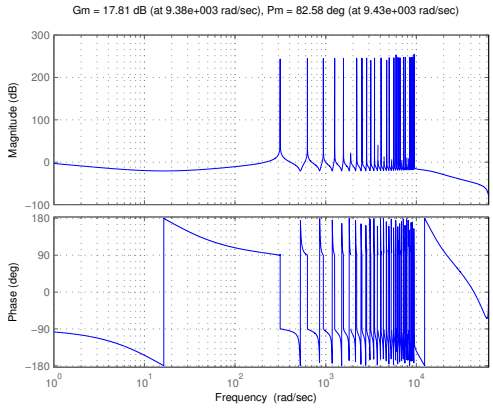
Table IV.1: AFC Control loop - parameters used on the resonators.

The parameters used on the AFC control loop of Eq. (IV.19) are presented in Table IV.1. The closed-loop system shows gain and phase margins within good levels while keeping good rejection at the desired harmonic frequencies.

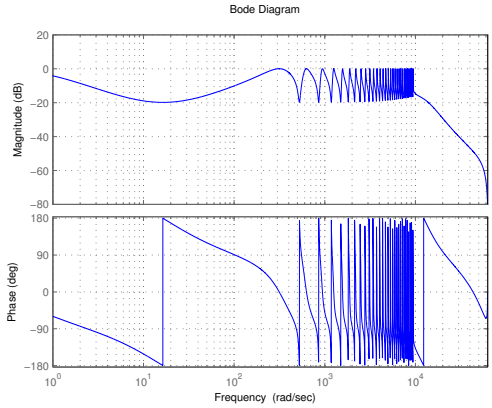
Fig. IV.9 shows the open/closed-loop Bode plots for the design of the resonators loop of the DT-AFC control scheme. Fig. IV.9(a) shows the Bode plot of the resonators controller $C_{AFC}(z)$. The Bode plot of the DT-AFC open loop transfer function $L_{AFC}(z) = C_{AFC}(z)\,T_2(z)$ is presented in Fig. IV.9(b). As it can be observed, there are 30 resonant peaks at 50 Hz and its respective harmonics. The phase shifts are all centered at 0 °, which guarantees the maximum phase margin on the system. An overall gain margin of 17.81 dB at $9.38 \cdot 10^3$ rad/s, and a phase margin of 82.58 ° at $9.43 \cdot 10^3$ rad/s are obtained. The Bode plot of the DT-AFC closed-loop transfer function $T_{AFC}(z) = C_{AFC}(z)\,T_2(z)/(1 + C_{AFC}(z)\,T_2(z))$ is shown in Fig. IV.9(c).



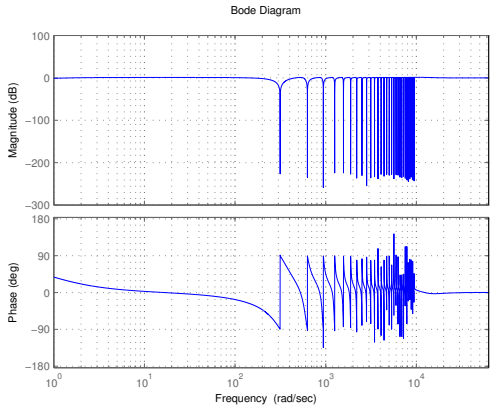
(a) Bode plot of the DT-AFC controller ($C_{AFC}(z)$).



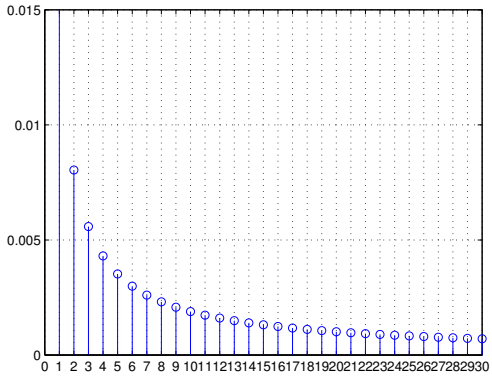
(b) Bode plot of the DT-AFC open-loop transfer function ($L_{AFC}(z)$).



(c) Bode plot of the DT-AFC closed-loop transfer function ($T_{AFC}(z)$).



(d) Bode plot of the DT-AFC closed-loop output sensitivity transfer function ($S_{AFC}(z)$).



(e) Hyperbolic profile used for gains of the resonators g_k.

Figure IV.9: DT-AFC controller design plots.

The closed loop transfer function $T_{AFC}(z)$ shows perfect tracking capabilities at the harmonic frequencies $\omega_k = 2\,\pi\,k\,50$ for $k = 1, 2, ..., 30$, this property can be observed by the 0 dB gains and 0 ° phase shifts at the ω_k frequencies of Fig. IV.9(c). The attenuating peaks shown for the Bode plot of the output sensitivity transfer function $S_{AFC}(z) = 1/(1+C_{AFC}(z)\,T_2(z))$ presented in Fig. IV.9(d) reflect the perfect output disturbance rejection at the ω_k frequencies. Also, the low peak response of $||S_{AFC}(z)||_\infty = 1.19$ dB at $9.37 \cdot 10^3$ rad/s, is a good stability indicator [27].

IV.3.3 DT-AFC simulation results

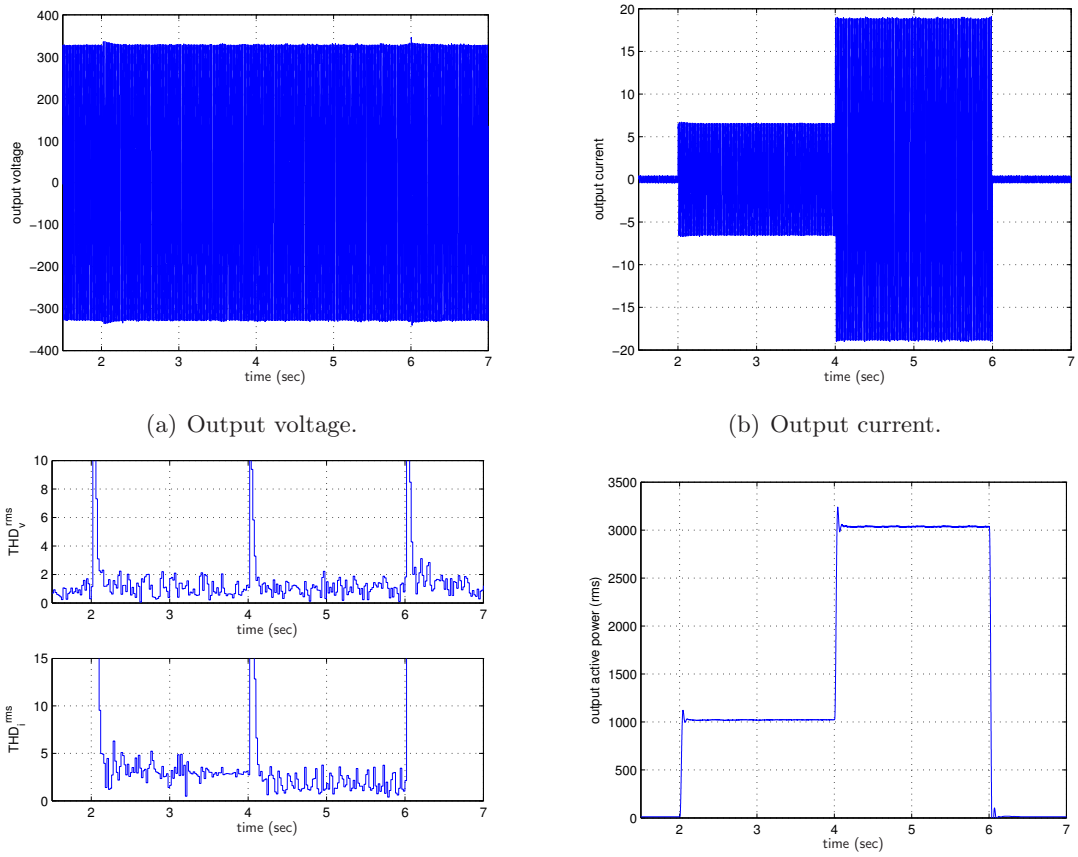
The discrete-time controllers of Eq. (IV.17) and Eq. (IV.19), designed for the discrete-time averaged model of the converter given in Eq. (IV.16), have been tested over a simulation model of the full-bridge dc-ac inverter working under hard switching as presented in [56]. The controllers have been implemented using the same C++ code that will be used on the tests over the experimental setup. The simulation environment used and the considerations taken to perform the simulations are described in detail in Section II.3. The time step used on the solver of the simulation environment in this case is $1 \cdot 10^{-6}$ s.

The full-bridge dc-ac inverter is implemented by means of IGBT elements. The switches are operated by centered pulse, single-update mode, PWM with a switching frequency of $f_{sw} = 20$ kHz. The conduction losses of the semiconductors are included into the model, the parasitic losses of the components are also considered. The PWM synchronization signal is used to latch the measured signals, and therefore, the sampling frequency is also $f_s = 20$ kHz. A delay of one sampling period is included at the input of the PWM module to account for the delay introduced by the load of the PWM register that will be present at the ADSP on the experimental setup. A 2.5 μs dead time is included at the PWM module between the complementary signals on each of the IGBT bridges. The inclusion of the dead time on the PWM scheme introduces some distortions on the output voltage of the dc-ac inverter (Seung-Gi Jeung *et al.* in [43] and [82], Wu *et al.* in [99]). In this case the most important disturbances caused by this fact are expected to take place on the odd harmonics of the fundamental 50 Hz frequency [99]. From the DT-AFC control scheme point of view, the output voltage variations caused by the dead time are seen as external disturbances at the target frequencies of the controller, therefore rejecting them.

The quality of the output voltage signal is measured by means of the Total Harmonic Distortion (THD). There are two possible definitions for the THD, in this work, the definition used by the International Electrotechnical Commission (IEC) is used [87], the equation that defines this quality indicator is

$$\mathrm{THD}_{\mathrm{v}}^{\mathrm{rms}} = \frac{\sqrt{(V^{\mathrm{rms}})^2 - (V_1^{\mathrm{rms}})^2}}{V^{\mathrm{rms}}}, \tag{IV.20}$$

where V^{rms} is the rms value of the voltage being measured, V_1^{rms} is the rms value of the first harmonic component of the voltage being measured, in this case the 50 Hz component. The formula given in Eq. (IV.20) can also be used to measure the THD of some desired current by replacing the appropriate quantities. The simulation tests carried out on the full-bridge dc-ac inverter cover the linear and nonlinear loads cases.



(a) Output voltage.

(b) Output current.

(c) $\mathrm{THD}_{\mathrm{v}}^{\mathrm{rms}}$ and $\mathrm{THD}_{\mathrm{i}}^{\mathrm{rms}}$.

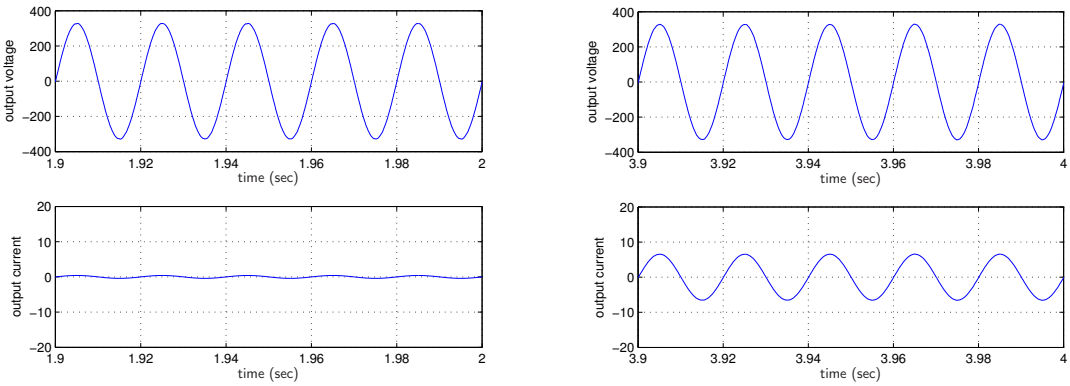
(d) Active output power (rms).

Figure IV.10: Simulation results of the behavior of the full-bridge dc-ac inverter with the DT-AFC control under load changes tests (linear loads).

Linear loads and linear load changes

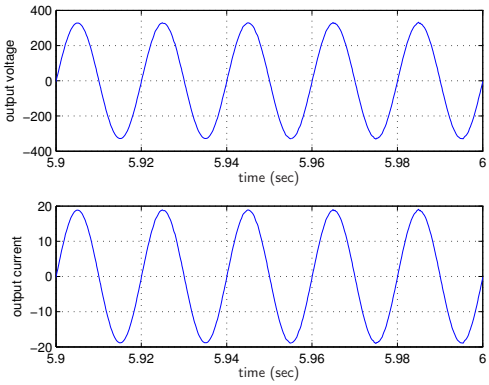
For the linear loads case, a resistor has been connected to the output terminals of the converter. The value of the output resistance R_o has been chosen to meet the desired output power level.

For these tests, the system has been brought to work under steady state. First, the system is working without any load connected at the output terminals. At $t = 2$ s, a $R_o = 53.5\ \Omega$ resistor is connected, and then the dc-ac inverter must provide $p_{out} \approx 1000$ W active output power. The system is let to achieve its steady state behavior while feeding the $p_{out} \approx 1000$ W load. At $t = 4$ s the behavior of the system has already reached its steady state. At this point, an output resistor of $R_o = 17.8\ \Omega$ is connected, requiring the inverter to feed a $p_{out} \approx 3000$ W load. The system is again allowed to reach its steady state behavior under this output power condition. At $t = 6$ s the behavior of the system is steady, and then the load resistor R_o is disconnected and the converter returns to its initial state.



(a) 0 W load.

(b) 1000 W load.



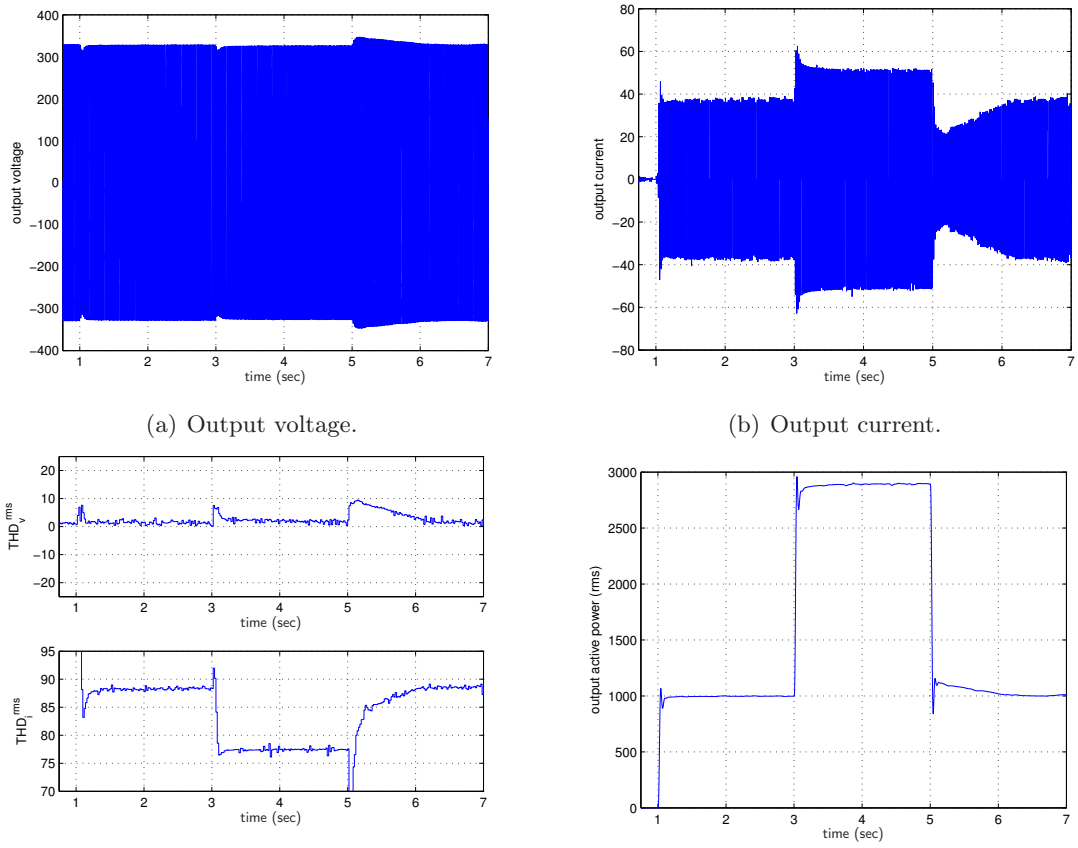
(c) 3000 W load.

Figure IV.11: Steady-state simulation results of the behavior of the full-bridge dc-ac inverter with the DT-AFC control under different load conditions (linear loads).

The process described before can be observed in Fig. IV.10. Fig. IV.10(a) shows the behavior of the output voltage shape during the test. As can be noticed, there are not important overshoots on the output voltage amplitude during the load level changes. The worst case overshoot occurs around $t = 6$ s, during the last load change from $p_{out} \approx 3000$ W to empty. In this case, the output voltage amplitude reaches 345.5 V which translates in a 6.3 % overshoot. After the overshoot, the system returns to its nominal values in approximately 10 cycles.

Fig. IV.10(b) shows the output current that is being supplied by the dc-ac inverter. As the loads being supplied are linear, the output current is sinusoidal. This fact can be observed by the low $\text{THD}_{\text{i}}^{\text{rms}}$ levels in Fig. IV.10(b), where the high quality of the output voltage is also evident by the low $\text{THD}_{\text{v}}^{\text{rms}}$ levels achieved. Fig. IV.10(d) shows the rms output power delivered to the loads by the full-bridge dc-ac inverter.

The steady-state behavior of the full-bridge dc-ac inverter using the DT-AFC control scheme under the different load conditions of the test is presented in Fig. IV.11. Fig. IV.11(a) shows the behavior of the dc-ac inverter under empty output power condition. In this case, the



(a) Output voltage.

(b) Output current.

(c) $\text{THD}_\text{v}^\text{rms}$ and $\text{THD}_\text{i}^\text{rms}$.

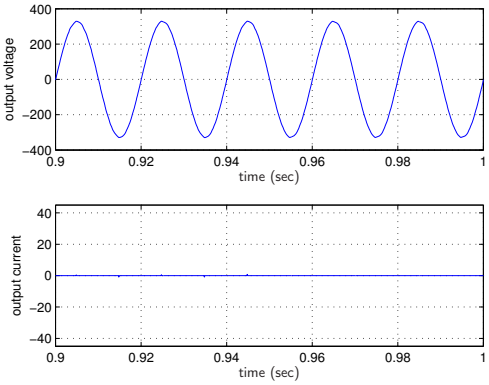
(d) Active output power (rms).

Figure IV.12: Simulation results of the behavior of the full-bridge dc-ac inverter with the DT-AFC control under load changes tests (nonlinear loads).

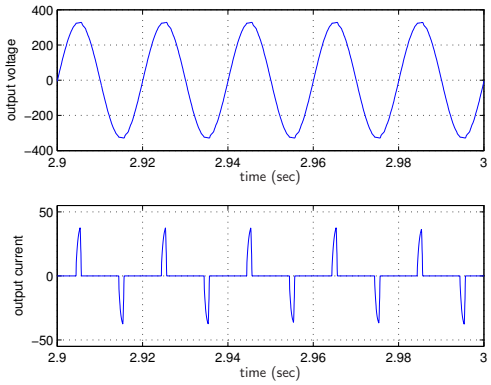
$\text{THD}_\text{v}^\text{rms} = 0.45$ %. Fig. IV.11(b) shows the behavior of the dc-ac inverter while feeding a 1000 W load. The $\text{THD}_\text{v}^\text{rms} = 0.89$ % for this test. Fig. IV.11(c) shows the behavior of the dc-ac inverter while feeding a 3000 W load. The $\text{THD}_\text{v}^\text{rms} = 0.85$ % under these conditions. The low $\text{THD}_\text{v}^\text{rms}$ levels achieved show the good tracking and output disturbance rejection of the DT-AFC control scheme.

Nonlinear loads and nonlinear load changes

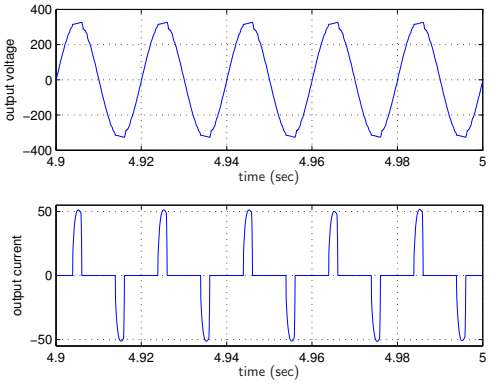
Fig. IV.1 shows the nonlinear load to be used on these tests. This load is formed by a full-bridge diode rectifier with a RC load. The output capacitor has the value $C_o = 6400$ μF, the output resistance R_o is adjusted depending on the desired output power. This nonlinear load has been dimensioned following the guidelines given by the International Electrotechnical Commission in [41] for the test of dc-ac inverters of Uninterruptible Power Supplies (UPS).



(a) 0 W load.



(b) 1000 W load.



(c) 2900 W load.

Figure IV.13: Steady-state simulation results of the behavior of the full-bridge dc-ac inverter with the DT-AFC control under different load conditions (nonlinear loads).

For these tests, the system has been brought to work under steady state. First, the system is working without any load connected at the output terminals. At $t = 1$ s, a $R_o = 105.625\ \Omega$ resistor is connected, and then the dc-ac inverter must provide approx. 2225 VA (app. 1000 W active output power). The system is let to achieve its steady state behavior while feeding the 2225 VA load. At $t = 3$ s the behavior of the system has already reached its steady state. At this point, an output resistor of $R_o = 35.21\ \Omega$ is connected, requiring the inverter to supply approx. 4750 VA (app. 2900 W active output power) load. The system is again allowed to reach its steady state behavior under this output power condition. At $t = 5$ s the behavior of the system is steady, and then the load resistor R_o is changed back to $R_o = 105.625\ \Omega$ and the converter returns to its previous output power requirement.

The process described before can be observed in Fig. IV.12. Fig. IV.12(a) shows the behavior of the output voltage shape during the test. As can be noticed, the worst case overshoot occurs around $t = 5$ s, during the last load change from 4750 VA down to 2225 VA. In this case, the output voltage amplitude reaches 363.6 V which translates in a 11.7 % overshoot. After the overshoot, the system returns to its nominal values in approximately 1 s.

Fig. IV.12(b) shows the output current that is being supplied by the dc-ac inverter. As the loads being supplied are nonlinear, the output current is periodic but non sinusoidal. This fact can be observed by the high $\text{THD}_{\text{i}}^{\text{rms}}$ levels in Fig. IV.12(c), where the high quality of the output voltage is also evident by the low $\text{THD}_{\text{v}}^{\text{rms}}$ levels achieved. Fig. IV.12(d) shows the rms output power delivered to the loads by the full-bridge dc-ac inverter.

The steady-state behavior of the full-bridge dc-ac inverter using the DT-AFC control scheme feeding the different nonlinear load levels of the test is presented in Fig. IV.13. Fig. IV.13(a) shows the behavior of the dc-ac inverter under empty output power condition. In this case, the $\text{THD}_{\text{v}}^{\text{rms}} = 0.52$ %. Fig. IV.13(b) shows the behavior of the dc-ac inverter while feeding the 2225 VA (1000 W) load. The $\text{THD}_{\text{v}}^{\text{rms}} = 1.04$ % for this test. In the case of the current, an additional indicator can be used to assess its nonlinearity. One indicator that is used for this kind of evaluation is the Crest Factor (CF). The CF is defined as the ratio between the peak value of a periodic signal divided by its rms value. The high nonlinearity of the current presented in Fig. IV.13(b) is verified by the CF = 3.88. Fig. IV.13(c) shows the behavior of the dc-ac inverter while feeding the 4750 VA (2900 W) load. The $\text{THD}_{\text{v}}^{\text{rms}} = 1.46$ % under these conditions. On this case the output current has a CF = 2.5. The low $\text{THD}_{\text{v}}^{\text{rms}}$ levels achieved show the good tracking capabilities of the DT-AFC control scheme. The good output disturbance rejection of the DT-AFC controller is evidenced by the high CF levels of the output current.

CHAPTER V

APU Control - Current Control of the Bank of Supercapacitors -

To doubt everything or to believe everything are two equally convenient truths; both dispense with the necessity of reflection.
Henri Poincaré

This Chapter presents the current control scheme used on the APU dc-dc interfacing converter. The modeling process of the converter is presented. The obtained model is then averaged and linearized. After a linear model of the plant has been obtained, a discrete-time controller is designed and tested by means of numerical simulation.

The objective of the Auxiliary Power Unit (APU) is to supply the excessive and/or fast/high-frequency repetitive power demands that the main power source is not able to provide. Therefore, the designed controller must allow a closed-loop system response with a bandwidth as wide as possible. Recalling from Section II.1.4, the APU used in this work is formed by a bank of supercapacitors (SCs) used as energy storing device, and the current bidirectional dc-dc power converter of Fig. II.12 that acts as interface between the dc-bus and the bank of SCs. The first problem on the control of the APU consists on choosing a control variable on the interfacing unit that can be handled when the energy flows from or towards the APU. One variable that fulfills this requirement is the current that flows between the bank of SCs and the APU interfacing unit. Fig. V.1 shows the general block diagram of the control scheme used for the control of the APU stage.

Fig. V.2 shows the schematic diagram of the APU system. This control stage is responsible of regulating the current i_{sc} that is extracted/injected from/towards the SCs, by means of changes in the applied PWM duty cycle to the complementary switches u_3 and $\bar{u}_3$. The current reference i_{sc}^{ref} to follow is generated by the power balance control loop, in order to maintain a regulated voltage at the dc bus, which is shared by the step-up and the APU stages. This scheme offers the possibility of imposing a hard limit to the i_{sc}^{ref} current reference amplitude, and therefore, protecting the components against excessive current values. In order to develop the SCs current controller, first a model of the response of the current of the SCs in front of changes on the applied duty cycle must be known.

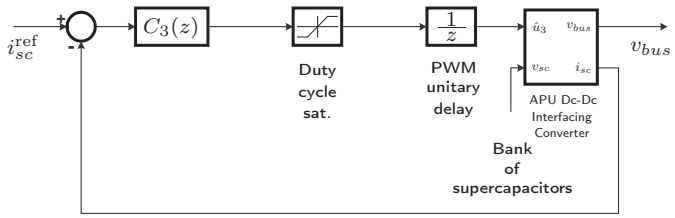


Figure V.1: General block diagram of the control architecture for the APU dc-dc interfacing converter.

The Kirchoff analysis of the APU topology of Fig. V.2 and the obtention of the dynamic model of the system are presented in Section V.1. The model obtained is latter averaged, the averaging process is presented in Section V.1.1. The linearization of the averaged system and the obtention of the transfer functions to be used in the controller design are presented in Section V.1.2. After a linearized model of the converter has been obtained, the SCs current controller is designed, the design of this controller is described in Section V.2. The controller is latter tested by means of numerical simulation. The general considerations taken for the realization of the simulation tests are discussed in Section V.3. Finally, the simulation results of the system in front of i_{sc}^{ref} step reference changes are presented in Section V.3.1.

V.1 APU dc-dc interfacing converter modeling

Fig. V.2 shows the dc-dc converter initially described in Section II.1.4 along with the bank of SCs which has been chosen as the energy storing device. Although variations on the capacitance of the bank of supercapacitors are present due to frequency, voltage and temperature conditions, as noted in by Rafik *et al* in [71], for the sake of simplicity, a constant capacitance C_{sc} is considered for the whole bank of supercapacitors, and therefore, the dynamic behavior of the bank is considered as the one of an ideal capacitor.

The dimensioning of the components used on this conversion stage was performed in Section II.1.4 as well. Recalling the values of the electronic components given:

> *...a series connection of* 23, 58 *F* 15 *V dc, BPAK0350-15EA SC packs from Maxwell has been chosen as the energy storing unit for the APU. The final values for the bank of SCs are* $C_{sc} = 2.52$ *F and* 345 *V dc as maximum operating voltage. ...A* $L_{apu} = 1600$ μH *inductance in series with a* $r_{L_{apu}} = 200$ $m\Omega$ *parasitic resistance has been used... A* $C_{bus} = 6000$ μF 450 *V dc capacitor is used as linking capacitor among the APU dc-dc interfacing converter, the step-up stage and the dc-ac inversion stage. ... A standard Semikron SKM100GB123D* 1200 *V dc,* 100 *A IGBT bridge with* 2 *V dc drop for the IGBTs and* 0.8 *V drop for each of the antiparallel diodes is used.*

The switches u_3 and $\bar{u}_3$ work in a complementary way, which means that when u_3 conducts $\bar{u}_3$ does not and viceversa. As mentioned in Section II.1.4, the dc-dc interfacing converter has been designed to work under Continuous Conduction Code (CCM). By assuming CCM, the converter of Fig. V.2 takes only to possible electrical topologies depending on the conduction state of the

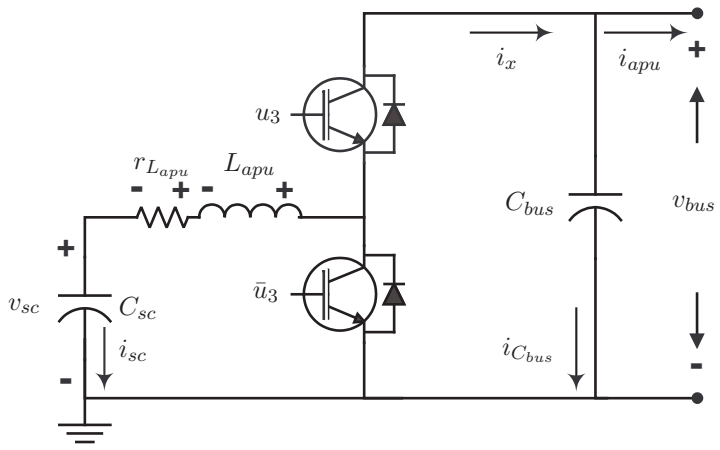


Figure V.2: APU dc-dc interfacing converter.

complementary switches u_3 and $\bar{u}_3$.

Fig. V.2 shows the definitions of the voltage polarities and current directions for the realization of a Kirchoff analysis over the circuit. The analysis is performed over the two possible electrical topologies, latter these two topologies are joined into a single dynamic model by performing a parametrization of the switch positions. Let first analyze the electrical topology that presents when switch u_3 conducts and $\bar{u}_3$ does not conduct. Under this condition, by performing the current Kirchoff analysis at the nodes of the circuit of Fig. V.2, the relationships

$$i_x + i_{sc} = 0, \tag{V.1}$$
$$i_x - i_{C_{bus}} - i_{apu} = 0, \tag{V.2}$$

are obtained.

The voltage relationship

$$v_{L_{apu}} + v_{r_{L_{apu}}} + v_{sc} - v_{bus} = 0, \tag{V.3}$$

is obtained by applying the Kirchoff voltage analysis over the circuit of Fig. V.2 when switch u_3 conducts and $\bar{u}_3$ does not conduct. Now the analysis is performed over the electrical topology that presents when switch u_3 does not conduct and $\bar{u}_3$ conducts. Under this condition, by performing the current Kirchoff analysis at the nodes of the circuit of Fig. V.2, the relationships

$$i_x = 0, \tag{V.4}$$
$$i_x - i_{C_{bus}} - i_{apu} = 0, \tag{V.5}$$

are obtained.

The voltage relationship

$$v_{L_{apu}} + v_{r_{L_{apu}}} + v_{sc} = 0, \tag{V.6}$$

is obtained by applying the Kirchoff voltage analysis over the circuit of Fig. V.2 when switch u_3 does not conduct and $\bar{u}_3$ conducts.

The dynamics of the capacitors connected to the circuit are expressed by

$$i_{sc} = C_{sc}\,\frac{d\,v_{sc}}{dt}, \tag{V.7}$$

$$i_{C_{bus}} = C_{bus}\,\frac{d\,v_{bus}}{dt}, \tag{V.8}$$

and the dynamic behavior of the inductance is expressed as

$$v_{L_{apu}} = L_{apu}\,\frac{d\,i_{sc}}{dt}. \tag{V.9}$$

As the operation of the switches is complementary, the behavior of switches u_3 and $\bar{u}_3$ can be described by the discrete variable

$$\check{u}_3 = \begin{cases} 1\ if\ u_3 \text{ conducts and } \bar{u}_3 \text{ does not} \\ 0\ if\ \bar{u}_3 \text{ conducts and } u_3 \text{ does not.} \end{cases} \tag{V.10}$$

The expressions for the currents of the capacitors given in Eq. (V.7) and Eq. (V.8) and the inductor voltage of Eq. (V.9) are substituted then into Eqs. (V.1) to (V.6). Then, the redundant equations are simplified. The parametrization $\check{u}_3$ given in Eq. (V.10), is used to group the separate dynamics into a single equations set. By solving for the inductor voltage and the capacitors currents, the dynamics of the interfacing converter of the APU can be expressed as

$$\begin{aligned} L_{apu}\frac{d\,i_{sc}}{dt} &= -r_{L_{apu}}\,i_{sc} - v_{sc} + \check{u}_3\,v_{bus}, \\ C_{sc}\frac{d\,v_{sc}}{dt} &= i_{sc}, \\ C_{bus}\frac{d\,v_{bus}}{dt} &= -\check{u}_3\,i_{sc} - i_{apu}, \end{aligned} \tag{V.11}$$

with $\check{u}_3\ \epsilon\ \{0, 1\}$.

V.1.1 Averaged dynamics and transfer functions

As stated in Section II.1.4, the APU interfacing converter is operated by centered pulse, single-update mode, Pulse-width Modulation (PWM). The switching frequency is $f_{sw} = 20$ kHz and therefore a switching period of $T_{sw} = 1/f_{sw} = 50$ μs is present on the system. The model of the converter described by Eq. (V.11) uses the discrete variable $\breve{u}_3$ which takes values in the set $\{0, 1\}$.

In order to develop a model of the converter that could be used for control purposes, some approximations must be made. As the converter is operated by PWM, it is convenient to get a model of the converter which includes the PWM duty cycle as the input variable. By using standard averaging procedures, as the one presented by Erickson in [29], an averaged model of the converter can be obtained, having the averaged duty cycle as the input variable. The average value of the converter variables over a switching period T_{sw} is obtained by applying the integral

$$\langle x\,(t)\rangle_{T_{sw}} = \frac{1}{T_{sw}} \int_{t}^{t+T_{sw}} x\,(\tau)\,d\tau. \tag{V.12}$$

The converter has been designed to operate under CCM. The capacitors C_{sc} and C_{bus} have been dimensioned to have small if not negligible voltage ripples when working within the power and switching frequency specifications. The inductor L_{apu} has been dimensioned in order to obtain a ripple of the inductor current as small as possible taking into account the expected current levels and switching frequency specifications. The moving average expressed by Eq. (V.12) has a low-pass effect over the averaged variables. The high-frequency components, which according to the considerations above, must be small, are filtered, and the dominant low-frequency behavior is obtained.

Having into account the considerations above, a good approximation on the dynamics of the converter would consist on using the averaged values of the variables instead of the instantaneous ones. The dynamic behavior of the converter is evaluated now under the two possible switch positions. First, the dynamics of the system when $\breve{u}_3 = 1$ is evaluated. The approximated inductance voltage and capacitor currents take the form

$$\begin{aligned}
L_{apu}\,\frac{d\,i_{sc}}{dt} &\approx -r_{L_{apu}}\,\langle\, i_{sc}\,\rangle_{T_{sw}} - \langle\, v_{sc}\,\rangle_{T_{sw}} + \langle\, v_{bus}\rangle_{T_{sw}},\\
C_{sc}\,\frac{d\,v_{sc}}{dt} &\approx \langle\, i_{sc}\rangle_{T_{sw}},\\
C_{bus}\,\frac{d\,v_{bus}}{dt} &\approx -\langle\, i_{sc}\rangle_{T_{sw}} - \langle\, i_{apu}\rangle_{T_{sw}}.
\end{aligned} \tag{V.13}$$

Now the dynamics of the system when $\check{u}_3 = 0$ is evaluated. The approximated inductance voltage and capacitor currents take the form

$$\begin{aligned} L_{apu}\frac{d\,i_{sc}}{dt} &\approx -r_{L_{apu}}\langle\, i_{sc}\,\rangle_{T_{sw}} - \langle\, v_{sc}\,\rangle_{T_{sw}}, \\ C_{sc}\frac{d\,v_{sc}}{dt} &\approx \langle\, i_{sc}\rangle_{T_{sw}}, \\ C_{bus}\frac{d\,v_{bus}}{dt} &\approx -\langle\, i_{apu}\rangle_{T_{sw}}. \end{aligned} \tag{V.14}$$

With the dynamics of Eq. (V.13) and Eq. (V.14) the average inductor voltage and capacitor currents can be calculated then by applying the integrals

$$\begin{aligned} L_{apu}\frac{d\,\langle\, i_{sc}\rangle_{T_{sw}}}{dt} &= \langle\, v_{L_{apu}}(t)\rangle_{T_{sw}} = \frac{1}{T_{sw}}\int_t^{t+T_{sw}} v_{L_{apu}}(\tau)\,d\tau, \\ C_x\frac{d\,\langle\, v_{C_x}\rangle_{T_{sw}}}{dt} &= \langle\, i_{C_x}\,(t)\rangle_{T_{sw}} = \frac{1}{T_{sw}}\int_t^{t+T_{sw}} i_{C_x}(\tau)\,d\tau. \end{aligned}$$

Let $\hat{u}_3$ be the proportion of the switching period T_{sw} that the switches are on position $\check{u}_3 = 1$ defined in Eq. (V.10). Then, $\hat{u}_3$ is a continuous variable in the range $[0, 1]$, with the physical interpretation of being the PWM duty cycle applied to switch u_3. As the switches u_3 and $\bar{u}_3$ work in a complementary way, the applied PWM duty cycle to switch $\bar{u}_3$ is $(1 - \hat{u}_3)$, and therefore, the relationship $T_{sw} = \hat{u}_3\,T_{sw} + (1 - \hat{u}_3)\,T_{sw}$ holds. With the above definitions, the averaged dynamics of the APU interfacing converter can be written as

$$\begin{aligned} L_{apu}\frac{d\,\langle\, i_{sc}\rangle_{T_{sw}}}{dt} &= -r_{L_{apu}}\,\langle\, i_{sc}\,\rangle_{T_{sw}} - \langle\, v_{sc}\,\rangle_{T_{sw}} + \hat{u}_3\,\langle\, v_{bus}\rangle_{T_{sw}}, \\ C_{sc}\frac{d\,\langle\, v_{sc}\rangle_{T_{sw}}}{dt} &= \langle\, i_{sc}\rangle_{T_{sw}}, \\ C_{bus}\frac{d\,\langle\, v_{bus}\rangle_{T_{sw}}}{dt} &= -\hat{u}_3\,\langle\, i_{sc}\rangle_{T_{sw}} - \langle\, i_{apu}\rangle_{T_{sw}}. \end{aligned} \tag{V.15}$$

For the sake of simplicity let, from now on, drop the $\langle\,\cdot\,\rangle_{T_{sw}}$ notation. By doing so, and isolating the derivatives of the inductor current and capacitor voltages, the averaged dynamics of the converter take the form

$$\begin{aligned} L_{apu}\frac{d\,i_{sc}}{dt} &= -r_{L_{apu}}\,i_{sc} - v_{sc} + \hat{u}_3\,v_{bus}, \\ C_{sc}\frac{d\,v_{sc}}{dt} &= i_{sc}, \\ C_{bus}\frac{d\,v_{bus}}{dt} &= -\hat{u}_3\,i_{sc} - i_{apu}, \end{aligned} \tag{V.16}$$

with $\hat{u}_3 \,\epsilon\, [0, 1]$.

V.1.2 Model linearization and transfer functions

The auxiliary power unit must be able to follow the current references generated by the power balance control loop. The averaged system described by Eq. (V.16) is not linear, as it presents products between the control variable $\hat{u}_3$, the bus capacitor voltage v_{bus} and the SCs current i_{sc}. This system needs to be linearized in order to be able to apply linear control techniques over it. Let first assume that the voltage v_{bus} is constant. This assumption is based on the fact that the power balance control will produce the appropriate current references to assure a voltage at the dc bus of $v_{bus} = 425$ V dc. Having this in mind, the average dynamic behavior of the converter is linearized and can be written as the state-space system

$$\begin{bmatrix} \dot{v}_{sc} \\ \dot{i}_{sc} \end{bmatrix} = \begin{bmatrix} 0 & 1/C_{sc} \\ -1/L_{apu} & -r_{L_{apu}}/L_{apu} \end{bmatrix} \begin{bmatrix} v_{sc} \\ i_{sc} \end{bmatrix} + \begin{bmatrix} 0 \\ v_{bus}/L_{apu} \end{bmatrix} \hat{u}_3$$
$$i_{sc} = \begin{bmatrix} 0 & 1 \end{bmatrix} \begin{bmatrix} v_{sc} \\ i_{sc} \end{bmatrix}, \tag{V.17}$$

with $\hat{u}_3 \in [0, 1]$.

Using the linearized dynamics expressed by Eq. (V.17) a transfer function from the duty cycle ($\hat{U}_3(s)$) to the supercapacitor current ($I_{sc}(s)$) is found, and takes the form

$$\frac{I_{sc}(s)}{\hat{U}_3(s)} = \frac{C_{sc}\, v_{bus}\, s}{C_{sc}\; L_{apu}\; s^2 + C_{sc}\; r_{L_{apu}}\; s + 1}. \tag{V.18}$$

The zero at $s = 0$ imposes a restriction on the controller design, an integral action can not be included in the controller because the system would become internally unstable (Skogestad and Postlethwaite [86]). Therefore, it becomes complicated to develop a controller with the capability to follow dc i_{sc}^{ref} references. For this reason, it is necessary to obtain a model of the converter that allows the designed controller to provide dc reference tracking capabilities.

Variable change and model reformulation

To avoid this, an auxiliary variable w is used. The variable change

$$w = \hat{u}_3\, v_{bus} - v_{sc} \tag{V.19}$$

has been performed. By doing this, the linearized state-space system presented in Eq. (V.17),

can be rewritten as

$$\begin{bmatrix} \dot{v}_{sc} \\ \\ \dot{i}_{sc} \end{bmatrix} = \begin{bmatrix} 0 & 1/C_{sc} \\ \\ 0 & -r_{L_{apu}}/L_{apu} \end{bmatrix} \begin{bmatrix} v_{sc} \\ \\ i_{sc} \end{bmatrix} + \begin{bmatrix} 0 \\ \\ 1/L_{apu} \end{bmatrix} w$$
$$i_{sc} = \begin{bmatrix} 0 & 1 \end{bmatrix} \begin{bmatrix} v_{sc} \\ i_{sc} \end{bmatrix}, \tag{V.20}$$

with $w \in [-v_{sc}, v_{bus} - v_{sc}]$.

From Eq. (V.20) a transfer function from the auxiliary variable $W(s)$ to the current flowing through the bank of SCs $I_{sc}(s)$ is found

$$G_3(s) = \frac{I_{sc}(s)}{W(s)} = \frac{1}{L_{apu}\ s + r_{L_{apu}}}. \tag{V.21}$$

V.2 Supercapacitor bank current controller design

The variable change of Eq. (V.19) has achieved the objective of eliminating the derivative term included in Eq. (V.18). The transfer function presented in Eq. (V.21) presents then, more convenient conditions for the design of the current controller of the bank of SCs. Having Eq. (V.21) as the plant to be controlled, as a first step to be able to design the controller, lets substitute the numerical values of the components used (recalled in Section V.1) into Eq. (V.21), obtaining

$$G_3(s) = \frac{625}{s\ +\ 125}. \tag{V.22}$$

The transfer function presented in Eq. (V.22) has one stable pole at 125 rad/s and no zeroes. As the controller is to be implemented by means of an ADSP, it would be convenient to make the controller design directly in the z-domain. $G_3(s)$ must be converted to a discrete-time model. Eq. (V.23) shows the conversion result into the z-domain, by using a sampling frequency of $f_s = 20$ kHz and a ZOH

$$G_3(z) = \frac{0.031153}{z - 0.9938}. \tag{V.23}$$

When implementing the controller, the load of the PWM register of the microprocessor introduces a delay of one sampling period $T_s = 1/f_s$. Its effects now need to be accounted into the nominal plant in order to consider its influence into the behavior of the overall system. Eq. (V.24) shows the actual nominal plant to be used in the controller design process.

$$P_3(z) = \frac{1}{z}\, G_3(z) = \frac{0.031153}{z(z - 0.9938)} \tag{V.24}$$

Now, with the nominal plant $P_3(z)$ of Eq. (V.24), a discrete-time controller can be designed to regulate the current that the step-up stage extracts/injects from/towards the energy storing device of the APU, in this case, the bank of supercapacitors. With $P_3(z)$ as the nominal plant, a discrete-time PI controller of the form

$$C_3(z) = K_{p_3} + \frac{K_{i_3}\, T_s}{2} \frac{(z+1)}{(z-1)}, \tag{V.25}$$

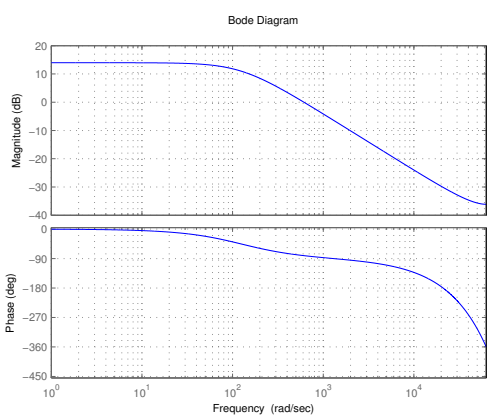
has been designed by finding convenient pole/zero locations. The values of the coefficients are $K_{i_3} = 1.7631\text{x}10^3$ and $K_{p_3} = 3.61$ and the sampling period $T_s = 1/f_s = 1/20$ kHz.

Fig. V.3 shows the open/closed-loop plots for the design of the controller $C_3(z)$. Fig. V.3(a) shows the Bode plot for the discrete-time transfer function $P_3(z)$ that models the behavior of the APU dc-dc interfacing converter. Fig. V.3(b) shows the Bode plot for the open-loop transfer function $L_3(z) = C_3(z)\, P_3(z)$. As it can be observed, this design presents a gain margin of 18.9 dB at $2.07 \cdot 10^4$ rad/s, and a phase margin of 71.2 ° at $2.3 \cdot 10^3$ rad/s. The Bode plot of the closed-loop transfer function $T_3(z) = C_3(z)\, P_3(z)/(1 + C_3(z)\, P_3(z))$ presents no significative closed-loop resonances as can be noticed by the maximum peak closed-loop gain of $||T_3(z)||_\infty = 0.836$ dB at 751 rad/s shown in Fig. V.3(c). This fact can be also observed in the Nyquist plot for the open-loop transfer function $L_3(z)$ presented in Fig. V.3(e). Under these conditions this design presents a $||S_3(z)||_\infty = 1.37$ dB at $1.07 \cdot 10^4$ rad/s, where $S_3(z) = 1/(1 + C_3(z)\, P_3(z))$ is the closed-loop output sensitivity transfer function shown in Fig. V.3(d), and that according to Doyle *et al.* [27] is an adequate stability margin.

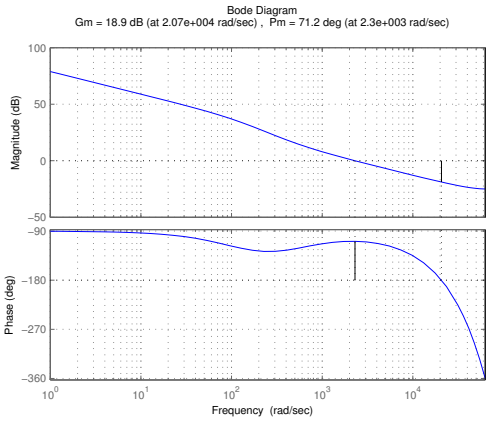
An anti-windup loop has been added to avoid unbounded growth of the integral part of the controller of Eq. (V.25). This loop acts over the auxiliary variable w, which must be bounded to assure a value of $\hat{u}_3$ within the interval $[0, 1]$. The upper bound for w presents when $\hat{u}_3 = 1$ and then, $w_{\max} = v_{bus} - v_{sc}$. On the other hand, the lower limit for w presents when $\hat{u}_3 = 0$ having a value for the auxiliary variable of $w_{\min} = -v_{sc}$. These bounds are not fixed and depend on the values of v_{bus} and v_{sc}.

Fig. V.4 shows the anti-windup loop that shows up only when the value of the variable w lies outside the range $[-v_{sc}, v_{bus} - v_{sc}]$. Care must be taken when adding this new loop, the stability of the system must be guaranteed. The open-loop transfer function of this new loop takes the following form:

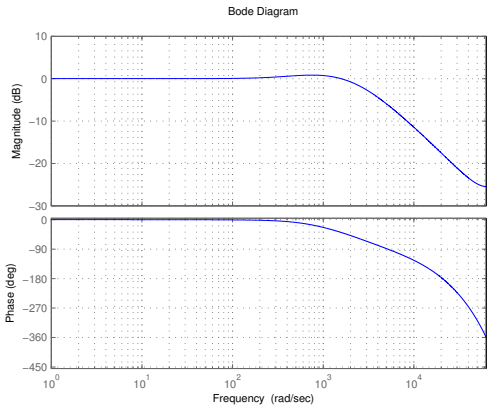
$$L_{\text{aw}_3}(z) = \left(\frac{K_{\text{aw}_3}}{z}\right)\left(\frac{K_{i_3}\, T_s}{2}\frac{(z+1)}{(z-1)}\right) \tag{V.26}$$



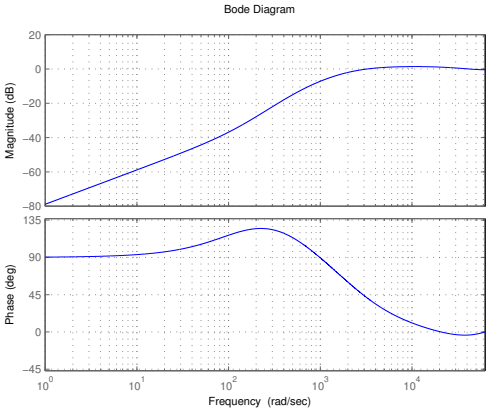
(a) Bode plot of the nominal plant ($P_3(z)$).



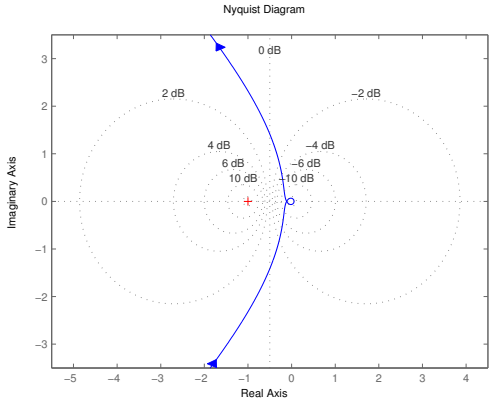
(b) Open-loop Bode plot ($L_3(z)$).



(c) Closed-loop Bode plot ($T_3(z)$).



(d) Bode plot of the output sensitivity transfer function ($S_3(z)$).



(e) Open-loop Nyquist plot ($L_3(z)$).

Figure V.3: Open and closed loop Bode and Nyquist plots for the controller $C_3(z)$ with the nominal plant $P_3(z)$.

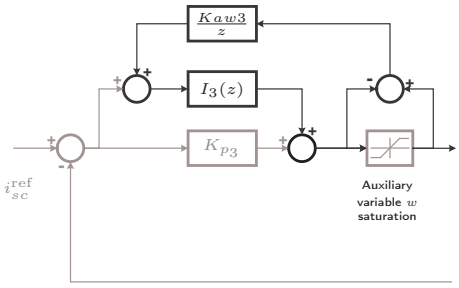


Figure V.4: Anti-windup control loop used used on the control of the current of the bank of SCs.

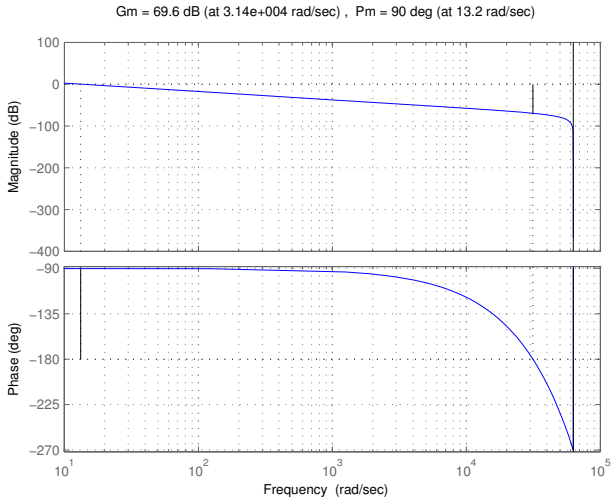


Figure V.5: Bode plot of the anti-windup open-loop transfer function L_{aw_3} used on the APU control loop.

The values $T_s = 1/f_s$ and K_{i_3} are known, the only free parameter is the constant K_{aw_3}. The stability of the anti-windup loop is checked by using the Jury test and assuming $K_{i_3} > 0$. After applying the test to the open-loop transfer function $L_{\text{aw}_3}(z)$, the condition imposed over the anti-windup constant K_{aw_3} can be written as:

$$0 \; < \; K_{\text{aw}_3} \; < \; \frac{2}{K_{i_3} \; T_s} \tag{V.27}$$

In this particular case the condition given above translates in $0 \; < \; K_{\text{aw}_3} \; < \; 22.69$. An anti-windup constant of $K_{\text{aw}_3} = 0.0075$ has been chosen. Fig. V.5 shows the Bode plot of the anti-windup open-loop transfer function $L_{\text{aw}_3}(z)$, as can be observed, a gain margin of 69.6 dB at $3.14 \cdot 10^4$ rad/s and a phase margin of 90 ° at 13.2 rad/s guarantee the stability of the closed-loop system.

The resulting control scheme used for the regulation of the current that is extracted/injected from/towards the the bank of SCs is presented in Fig. V.6. The controller $C_3(z)$ of Eq. (V.25) is represented by the $I_3(z)$ and K_{p_3} blocks in Fig. V.6. The applied duty cycle $\hat{u}_3$ is obtained by reverting the effects of the variable change in the form $\hat{u}_3 = (w + v_{sc})/v_{bus}$. The variable upper and lower saturation bounds for w are calculated and represented as the light gray lines above and below the saturation block respectively.

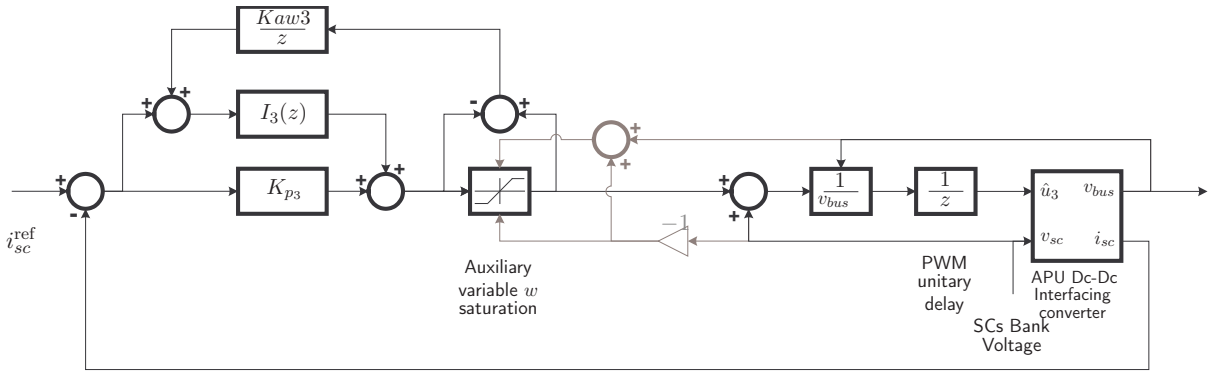


Figure V.6: Auxiliary power unit (APU) SCs bank current control scheme.

V.3 Supercapacitor bank current control simulation results

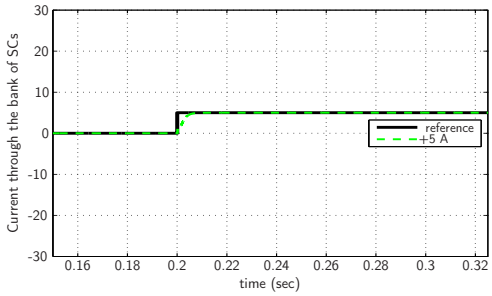
The designed discrete-time controller of Eq. (V.25) has been tested over a simulation model of the converter working under hard switching. The controller has been implemented using the same C++ code that will be used on the tests over the experimental setup. The commanded switches of the converter implemented on the simulation are operated by centered pulse, single-update mode, PWM with a switching frequency of $f_{sw} = 20$ kHz. A 2.5 μs dead time is included at the PWM module between the complementary signals of the IGBT bridge. The simulation environment used and the considerations taken to perform the simulations are described in detail in Section II.3. The time step used on the solver of the simulation environment in this case is $5 \cdot 10^{-8}$ s.

The PWM synchronization signal is used to latch the measured signals, and therefore, the sampling frequency is also $f_s = 20$ kHz. A delay of one sampling period is included at the input of the PWM module to account for the delay introduced by the load of the PWM register that will be present at the ADSP of the experimental setup. The conduction losses of the semiconductors are included into the model, the parasitic losses of the components are also considered.

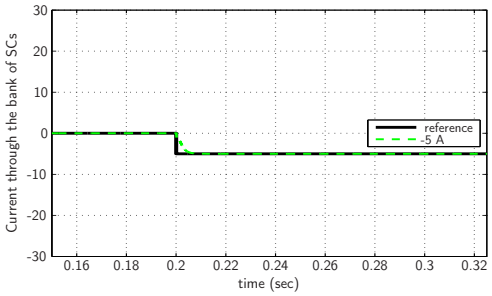
V.3.1 Supercapacitor bank current reference step changes

A constant $v_{bus} = 425$ V dc has been considered during the execution of the tests. The APU system has been brought to steady state with a SCs current reference of $i_{sc}^{\text{ref}} = 0$. An initial SCs voltage of $v_{sc} = 150$ V dc has been considered in order to evaluate the functioning of the system near the lower energy condition of the bank of SCs. From the maximum power requirements and from the voltage level of $v_{sc} = 150$ V dc, it can be determined that the average current can move in the range $[-20, 20]$ A dc.

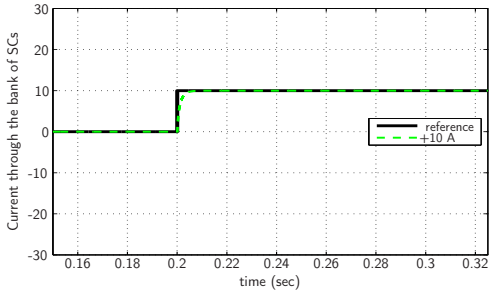
Once the converter is working at the desired steady-state condition, step changes are applied over the SCs current reference i_{sc}^{ref}. Step changes of magnitude +5 A dc, +10 A dc, +15 A dc, +20 A dc, +25 A dc, −5 A dc, −10 A dc, −15 A dc, −20 A dc and −25 A dc are applied over the SCs current reference that is given to the controller on the simulation environment.



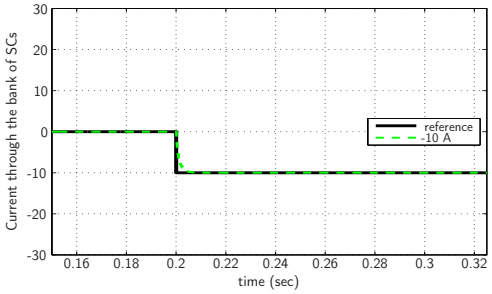
(a) +5 A reference change.



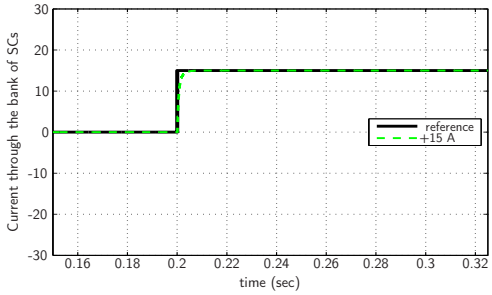
(b) -5 A reference change.



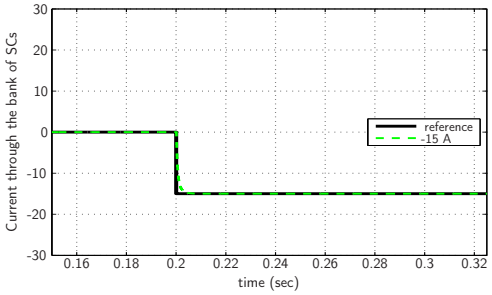
(c) +10 A reference change.



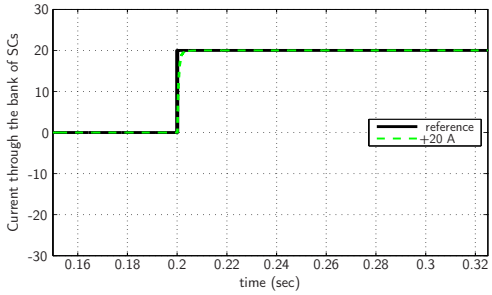
(d) -10 A reference change.



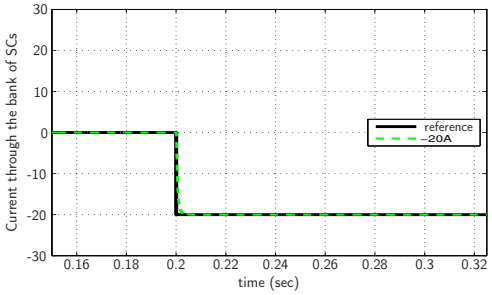
(e) +15 A reference change.



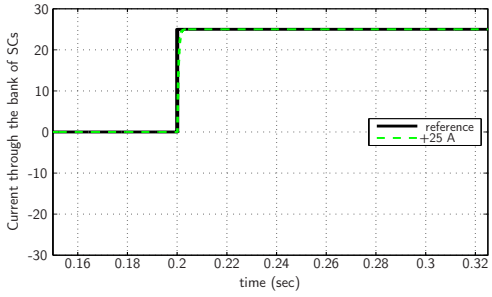
(f) -15 A reference change.



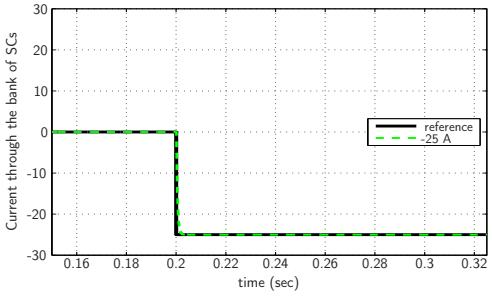
(g) +20 A reference change.



(h) -20 A reference change.



(i) +25 A reference change.



(j) -25 A reference change.

Figure V.7: Simulation results: SCs current reference step changes.

Fig. V.7 shows the simulation results for the step reference changes over the SCs current reference. The black traces show the current references delivered to the APU control. The dashed green traces show the SCs current response. As it can be observed, in all cases zero steady-state error is achieved over the SCs current of the converter for all the input current range covered on the test.

The tests presented in Fig. V.7 show the maximum range of current variations that can be present in the functioning of the APU. To lower SCs voltage levels, higher SCs current levels are demanded, in order to supply a certain extra power demand. The negative current variations test the response of the APU system to power requirements that extract energy from the bank of SCs. This situation will be present under an overload condition, where the extra energy stored at the bank of SCs is used to supply the load. The positive current variations test the behavior of the APU system to power requirements that inject energy to the bank of SCs. This situation will be present during the charging process of the bank of SCs.

chapter VI

Global Power Balance Control

The whole of science is nothing more than a refinement of everyday thinking.
Albert Einstein

This Chapter presents the design process of the Global Power Balance Control. The power balance is achieved by generating the appropriate current references for the step-up and the APU control loops. First, the plant to be controlled is determined and obtained. With this plant, a global power controller is initially designed under less restricting conditions. The global power control is then modified by taking into account the different limitations and/or restrictions included in the system. By doing this, the step-up and APU current references are obtained. Once the controller has been designed, it is tested by means of numerical simulation.

The objective of this control stage is to assure that the power levels demanded/injected from/towards the main power source (FC unit), the auxiliary power source (bank of SCs), and the load are coherent with the input/output power conditions and the specifications of each of the modules that compose the energy conditioning system. The power balance is achieved by regulating the voltage at the dc bus, which is the common interconnection point shared by the step-up, APU and dc-ac inversion stages. At this point, the step-up stage acts as a power source. The APU acts as a power source during the presence of an overload condition, and as load when charging the bank of SCs. Finally, the dc-ac inversion stage acts as a load.

The voltage regulation at the dc bus is achieved by generating the appropriate current references for the step-up (i_{fc}^{ref}) and the APU (i_{sc}^{ref}) current control loops presented previously in Chapters III and V respectively. These current references must assure a constant voltage of $v_{bus} = 425$ V dc at the common point. These references are generated depending on the output power conditions, taking into account the response speeds of the different modules involved and their maximum/minimum voltage/current ratings.

In order to be able to perform the design of the controller, first, the plant to be controlled must be known. This plant is determined according to the control objectives and characteristics of the system in Section VI.1. The procedure followed and the considerations taken to find a suitable model of the plant are discussed in Section VI.1.1. The application of the model identification methodology over the experimental platform is presented in Section VI.1.2.

The design of the global power balance control is presented in a constructive way in Section VI.2. First, it is considered that the system is fed only by the main power source (FC unit), neglecting its absolute maximum power rating, and considering only the bandwidth limitation of the device. By assuming this, an initial controller design is performed and presented in Section VI.2.1. The absolute maximum power ratings of the different conversion stages are considered. The introduction of these constraints in the controller design process is presented in Section VI.2.2. Latter, the frequency decoupling between the step-up stage (i_{fc}^{ref}) and APU (i_{sc}^{ref}) current references is then considered to cope with the bandwidth limitations of the FC unit. The introduction of this consideration is presented in Section VI.2.3. Finally, the generation of the current reference for the charge of the bank of SCs during the normal operation of the conditioning system is presented in Section VI.2.4.

To conclude, Section VI.3 presents the simulation results for the whole energy conditioning system including all the conversion stages. First, a set of tests performing load changes over the conditioning system feeding linear loads is presented. The simulation results of the system under this condition are presented in Section VI.3.1. A set of load changes tests feeding non-linear loads has also been performed, these simulation results are presented in Section VI.3.2.

VI.1 Determination and modeling of the plant to be controlled

Let first make an analysis over the desired behavior of the energy conditioning system. Under normal operation, the dc-ac inversion stage will be feeding linear or nonlinear loads with an active power component that lies within the specifications of the main power source. Therefore, the power demanded by the dc-ac inverter/load is provided by the FC unit alone. This power level is determined by the amplitude of the input current reference given to the step-up stage control loop (i_{fc}^{ref}) and the voltage present at the input of the step-up converter (v_{fc}).

As stated in the specifications of the energy conditioning system given in Section I.2.1, the system must be able to handle temporary high power demands with an active power component up to 3 kW with a maximum duration of 45 s. During an overload condition, the FC unit must be made to work at full load condition, and the remaining power should be extracted from the bank of SCs. The required extra power level is determined by the amplitude of the current reference (i_{sc}^{ref}) given to the APU SCs current control loop and the voltage level present at the bank of SCs (v_{sc}).

One important limitation that must be taken into account is the bandwidth of the FC unit. The global power balance control must generate current references for the step-up stage input current control (i_{fc}^{ref}) including this constraint. In this way, the stress applied over FC unit is reduced, and therefore the lifespan of the device is not compromised. As a consequence, the fast

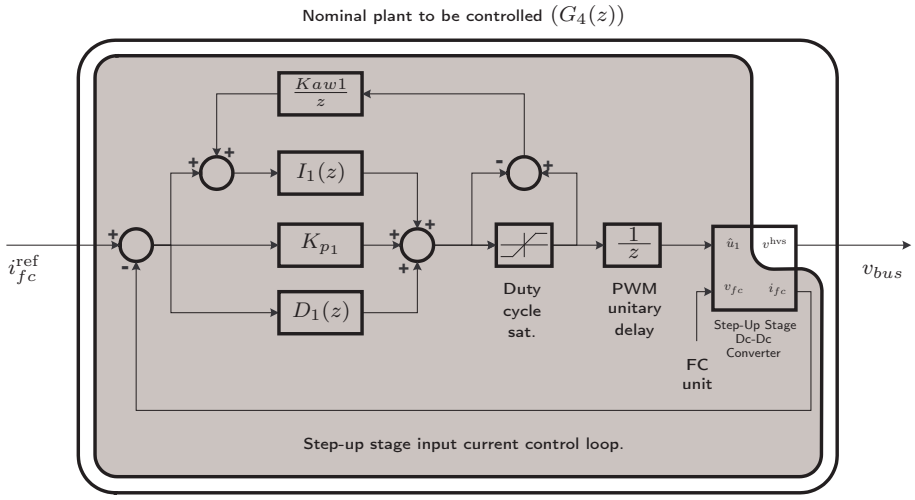


Figure VI.1: Nominal plant $G_4(z)$ to be controlled by the global power balance control.

energy requirements that the FC is not able to satisfy must be compensated by the APU, and therefore, the high-frequency power requirements must be included into the current reference given to the APU SCs current control loop (i_{sc}^{ref}).

From the global power balance control point of view, the dc-ac voltage inversion stage along with the ac load are seen as a dc load connected at the dc bus. The problem is then reduced to provide the necessary power to this particular load. The dc-ac voltage inverter requires a regulated input voltage of $v_{bus} = 425$ V dc in order to comply with the considerations made when designing the dc-ac inversion control loop in Chapter IV.

From the considerations made above, it can be concluded that the control objective is to obtain a regulated dc-bus voltage of $v_{bus} = 425$ V dc required by the dc-ac voltage inverter, regardless of the output power condition level. Hence, the plant to be controlled is the system shown in Fig. VI.1. Under normal operating conditions, the FC is in charge of supplying the power needed by the energy conditioning system. The voltage at the high-voltage side of the step-up converter ($v^{\text{hvs}} = v_{bus}$) is controlled indirectly by giving the appropriate current reference (i_{fc}^{ref}) to the step-up stage control loop. The response speed of the APU needs to be fast, in order to be able to deal with the fast energy requirements that the FC is not able to satisfy. This assumption is reasonable as per the response speeds obtained in Chapter V, when controlling the current that flows through the SCs.

As has been mentioned before, the dynamics of the converter used on the step-up stage (see Fig. II.6) are analytically hard to find. In this case, time-domain system identification techniques have been used to obtain the transfer function that describes the dynamic behavior of the step-up converter with the input current control loop closed. The procedure followed keeps structure used to find the plant to be controlled by the outer control loop on the output voltage regulation scheme presented in [57].

VI.1.1 Step-up stage - Input current reference to output voltage modeling

The plant to be controlled in this case is modeled by the transfer function from the input current reference I_{fc}^{ref} to the voltage V^{hvs} at the high-voltage side of the step-up converter. In order to obtain an appropriate model of the plant to be controlled by the global power balance control loop the procedure taken was:

1. Fix the value of the input voltage source to $v_{fc} = v_{fc_{ss}}$. Where $v_{fc_{ss}}$ is the mid scale value of the input voltage range given in the specifications.

2. Determine the desired output power condition for the test by choosing the appropriate values for the load resistor R and a desired output voltage level v_{ss}^{hvs}. The steady-state output power is determined by the desired output voltage v_{ss}^{hvs} and the load resistor R by the relationship: $p_{ss}^{\text{hvs}} = v_{ss}^{\text{hvs}} i_{ss}^{\text{hvs}} = (v_{ss}^{\text{hvs}})^2/R$. Where v_{ss}^{hvs}, i_{ss}^{hvs} and p_{ss}^{hvs} are the steady-state voltage, current and power delivered at the high-voltage side of the step-up stage, respectively.

3. Connect the load resistor R to the output and bring the system (step-up converter working with the input current control loop closed) to steady state at the desired v_{ss}^{hvs} output voltage by finding an appropriate value for the input current reference $i_{fc_{ss}}^{\text{ref}}$ (this is determined by the desired output power condition for the test).

4. Apply different step reference variations around $i_{fc_{ss}}^{\text{ref}}$, read the variations at the output voltage around v_{ss}^{hvs}.

5. Normalize the output voltage variations results around v_{ss}^{hvs}, with respect to the magnitudes of the step variations around $i_{fc_{ss}}^{\text{ref}}$.

6. Determine if the normalized output voltage variations results can be approximated by a low-order continuous-time system.

7. Fit a low-order continuous-time system to each of the normalized output voltage variations results.

8. Average the dc gain, pole values, zero values for all cases. The nominal plant will be the low-order system formed by the average values.

9. Include the appropriate time delays into the low-order model if necessary.

Fig. VI.2 shows a block diagram of the experimental setup used for the identification of the plant $G_4(s)$. The input current control loop is closed, the input current reference is generated by a reference generator which will produce the step variations around the steady-state input current reference $i_{fc_{ss}}^{\text{ref}}$. The input current control loop feeds the PWM modulator with the duty cycle to be applied $\hat{u}_1$. Finally, the output voltage v^{hvs} is read to look for the variations around the steady-state value v_{ss}^{hvs}.

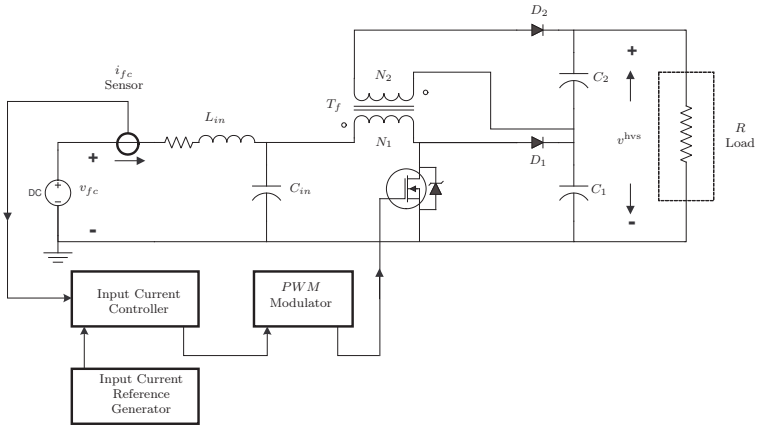


Figure VI.2: $G_4(s)$ plant identification experimental setup scheme.

Considerations and assumptions

Again the intention is to obtain a model that reflects the behavior of the system as if it were under normal operation condition. As explained before, The normal operation condition of the overall system will be to provide a regulated output voltage $v^{\text{hvs}} = v_{bus} = 425$ V dc. The output power condition of the test is determined then by the value of the load resistor R and the desired output voltage v_{ss}^{hvs} for the test. At the desired output power condition the appropriate steady-state input current reference value $i_{fc_{ss}}^{\text{ref}}$ needs to be determined.

The shaded region in Fig. VI.1 shows the closed input current control loop used on the step-up stage (presented in Chapter III), which guarantees the appropriate regulation of the current that is extracted from the FC (i_{fc}). At the desired output power condition, a good starting value for $i_{fc_{ss}}^{\text{ref}}$ can be obtained based on the steady-state power balance equation of the system: $p_{fc_{ss}} = p_{ss}^{\text{hvs}} + p_{loss_{ss}}$. First, it could be assumed that the steady-state power losses in the system are low, and that in fact can be neglected, and therefore $p_{fc_{ss}} = p_{ss}^{\text{hvs}}$. The output power of the system is fixed by the conditions of the test, and then $p_{fc_{ss}} = v_{ss}^{\text{hvs}}\, i_{ss}^{\text{hvs}}$. The current at the output can be determined by using the value of the load resistor R, hence $p_{fc_{ss}} = {v_{ss}^{\text{hvs}}}^2/R$. Substituting now the input power variables and solving for $i_{fc_{ss}}$ the starting value for the steady-state input current reference is found

$$i_{fc_{ss}}^{*} = {v_{ss}^{\text{hvs}}}^2/(v_{fc_{ss}}\, R). \tag{VI.1}$$

This starting value needs then to be increased to account for the losses in the system. The adjustment of the $i_{fc_{ss}}^{\text{ref}}$ is an iterative process, in which, the system (converter with the input current control loop closed and the load resistor R) is initially brought to steady-state by using $i_{fc}^{\text{ref}} = i_{fc_{ss}}^{*}$ as reference for the inner control loop. The value of $i_{fc_{ss}}^{\text{ref}}$ is then gradually increased until the output voltage v^{hvs} reaches the desired steady-state value v_{ss}^{hvs}. Now the step variations around $i_{fc_{ss}}^{\text{ref}}$ can be performed. Each of these step variations has, as a consequence, a variation

in the output voltage level around v_{ss}^{hvs}, this relationship can be summarized in the following form:

$$i_{fc}^{\text{ref}}(t) = i_{fc_{ss}}^{\text{ref}} + \tilde{i}_{fc}(t) \tag{VI.2}$$

$$\Downarrow$$

$$v^{\text{hvs}}(t) = v_{ss}^{\text{hvs}} + \tilde{v}^{\text{hvs}}(t), \tag{VI.3}$$

with

$$\tilde{i}_{fc}(t) = B\ h(t)$$

$$\tilde{v}^{\text{hvs}}(t) = \text{Output voltage variation around } v_{ss}^{\text{hvs}},$$

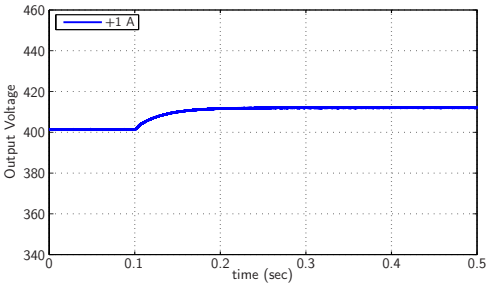
where $h(t)$ is the Heaviside step function and B is the magnitude of the step variation. Before performing the tests, it is mandatory to determine the minimum/maximum allowed values for the amplitude B to be used on the step variations around $i_{fc_{ss}}^{\text{ref}}$. In the case of negative values of B, $i_{fc_{ss}}^{\text{ref}} + B$ must always be positive, as the converter used in the step-up stage is a current unidirectional dc-dc converter. In the case of positive values of B, care must be taken to have a disturbed test current reference $i_{fc_{ss}}^{\text{ref}} + B$ whose value does not cause current and/or voltage values that overpass the maximum current/voltage ratings of the of the electric/electronic components.

Having determined the values of B for which the tests are to be performed, first the system must be brought to steady state by using the final value found for the steady-state input current reference $i_{fc}^{\text{ref}} = i_{fc_{ss}}^{\text{ref}}$, which will cause the converter to deliver an output voltage of v_{ss}^{hvs} with a load resistor R. The system is now working in steady state and the step changes in the input current reference can be performed. The output voltage $v^{\text{hvs}}(t)$ is acquired during the test.

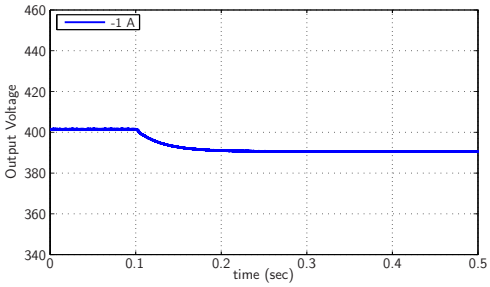
After the step variations to the input current reference have been performed, the output voltage variations $\tilde{v}^{\text{hvs}}(t)$ around v_{ss}^{hvs} are found by doing $\tilde{v}^{\text{hvs}}(t) = v^{\text{hvs}}(t) - v_{ss}^{\text{hvs}}$. Now, the output voltage variations are normalized with respect to the magnitudes B of the input current step variations. The resulting normalized responses have the form $\overline{v}^{\text{hvs}}(t) = \tilde{v}^{\text{hvs}}(t)/B$. Finally, the shapes of $\overline{v}^{\text{hvs}}(t)$ are analyzed and a low order continuous time system is fitted to each normalized time response.

VI.1.2 Experimental setup model identification

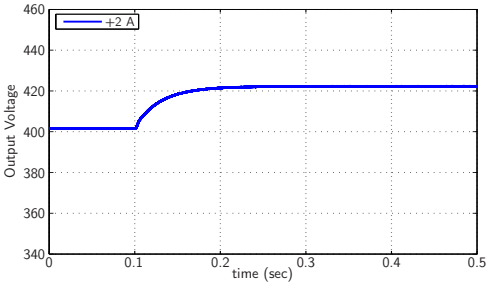
Now the methodology explained before can be applied over the experimental setup in order to find a transfer function from the input current reference (I_{fc}^{ref}) to the voltage at the high-voltage side (V^{hvs}) of the step-up converter. First, it is necessary to determine the nominal output power condition for the test. An output power condition of 500 W has been chosen to keep consistency with the model identification process previously presented in Chapter III. Again, the input voltage has been fixed to $v_{fc} = 30$ V dc and the desired output voltage value for the test is fixed to $v_{ss}^{\text{hvs}} = 400$ V dc. An output resistor $R = 320\ \Omega$ is used.



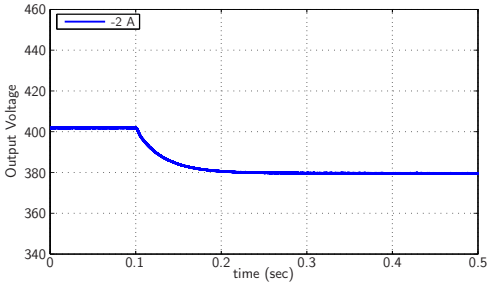
(a) +1 A reference change.



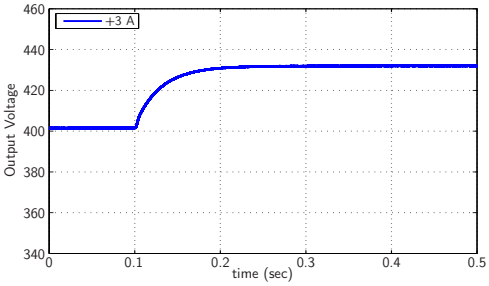
(b) -1 A reference change.



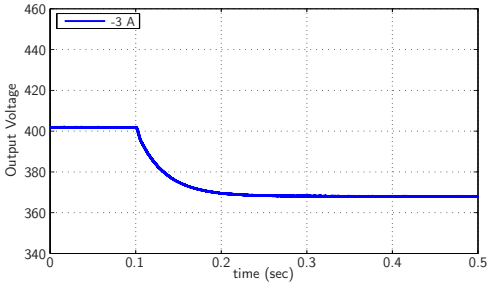
(c) +2 A reference change.



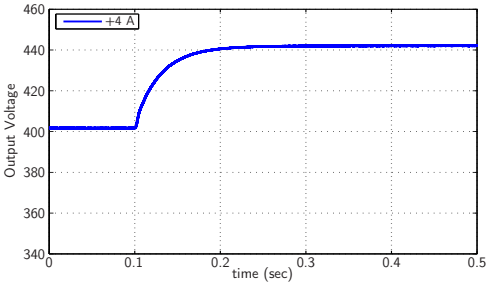
(d) -2 A reference change.



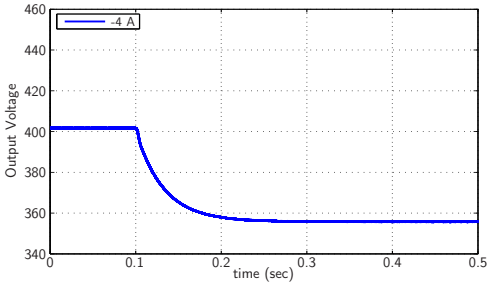
(e) +3 A reference change.



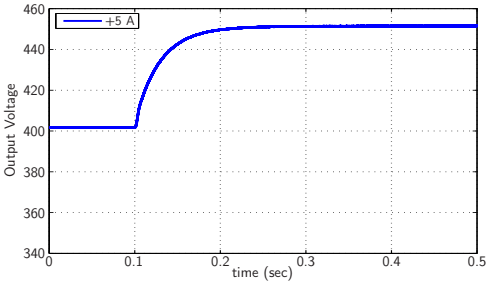
(f) -3 A reference change.



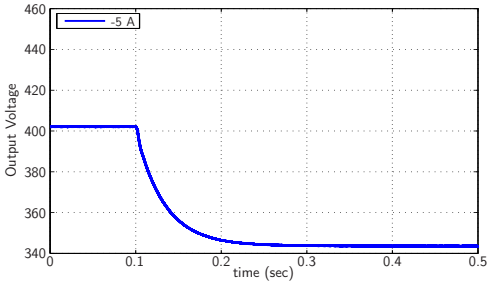
(g) +4 A reference change.



(h) -4 A reference change.



(i) +5 A reference change.



(j) -5 A reference change.

Figure VI.3: Experimental results, step-up stage with the input current control closed. Output voltage changes in front of input current reference step changes.

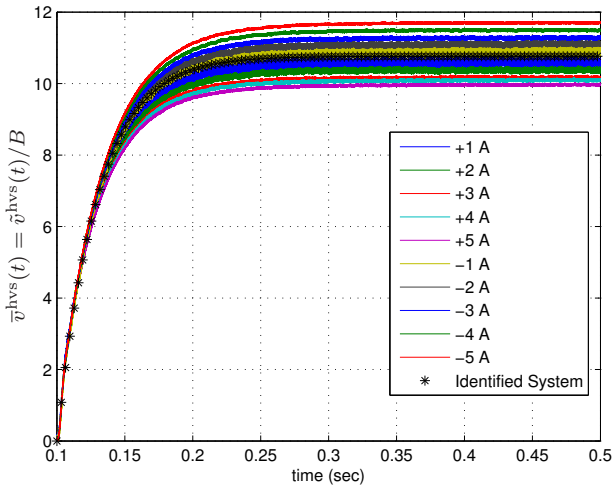


Figure VI.4: Normalized v^{hvs} responses to different magnitude step changes in the input current reference around $i^{\text{ref}}_{fc_{ss}}$. The step change magnitudes are 1A,2A,3A,4A,5A,-1A,-2A,-3A,-4A,-5A. Colored: normalized v^{hvs} responses. *: system average approximation.

With this resistor, the initial value for i^{ref}_{fc} is determined using Eq. (VI.1). This gives an initial input current reference without considering the losses in the system of $i^{*}_{fc_{ss}} = 16.66$ A. As explained in Section VI.1.1 this value needs to be adjusted, so the output voltage reaches the desired $v^{\text{hvs}}_{ss} = 400$ V dc level. By making the experimental setup work, with the input current control loop closed and gradually increasing the value of $i^{\text{ref}}_{fc_{ss}}$, a final value of $i^{\text{ref}}_{fc_{ss}} = 18.00$ A is found.

Once $i^{\text{ref}}_{fc_{ss}}$ has been found, it is necessary to define the amplitudes of the step disturbances (B parameter of Eq. (VI.2)) to be applied. The chosen magnitudes for the step variations of the input current reference around $i^{\text{ref}}_{fc_{ss}}$ are ± 1 A, ± 2 A, ± 3 A, ± 4 A and ± 5 A. The procedure described in Section VI.1.1 has been performed over the experimental platform, the output voltage variation results around v^{hvs}_{ss} are presented in Fig. VI.3 for all the input current step reference changes around $i^{\text{ref}}_{fc_{ss}}$.

Fig. VI.4 shows the normalized output voltage responses of the system. These traces been obtained by applying the relationship $\overline{v}^{\text{hvs}}(t) = \tilde{v}^{\text{hvs}}(t)/B$ over each data set, with $\tilde{v}^{\text{hvs}}(t)$ as defined in Eq. (VI.3). As it can be noticed in Fig. VI.4 each system response can be approximated by a first-order, linear time-invariant system with relative degree one. These systems can be characterized by a dc gain and a time constant. The dc gain is defined in this work by the steady-state value of each normalized output voltage variation in the form $\overline{v}^{\text{hvs}}_{ss} = \tilde{v}^{\text{hvs}}_{ss}/B$. Fig. VI.4 shows the system's step responses, and therefore the time constant τ is the time it takes to the system to reach approximately 63% of its final value.

B	v_{ss}^{hvs}	$v_{ss}^{\text{hvs}} + \tilde{v}_{ss}^{\text{hvs}}$	$\tilde{v}_{ss}^{\text{hvs}}$	$\bar{v}^{\text{hvs}} = \tilde{v}_{ss}^{\text{hvs}}/B$	τ
1A	401.4291	411.9965	10.5674	10.5674	0.0294
2A	401.5186	422.2439	20.7253	10.3627	0.0288
3A	401.4982	431.9575	30.4593	10.1531	0.0285
4A	401.6858	442.0377	40.3519	10.0880	0.0284
5A	401.6479	451.4602	49.8123	9.9625	0.0279
−1A	401.5147	390.5630	−10.9518	10.9518	0.0305
−2A	401.8307	379.5902	−22.2405	11.1203	0.0301
−3A	401.8618	368.0142	−33.8476	11.2825	0.0312
−4A	401.7027	355.7162	−45.9865	11.4966	0.0316
−5A	402.0543	343.5503	−58.5040	11.7008	0.0320
			Average	10.7686	0.0298

Table VI.1: Experimental input current reference variations and output voltage results for the identification of the plant $G_4(s)$.

Table VI.1 summarizes the input and output conditions of the application of the test over the experimental platform. The table includes the amplitudes of the step input current variations around $i_{fc_{ss}}^{\text{ref}} = 18.00$ A (column B). The steady-state value of the net output voltage due to the input disturbance defined in Eq. (VI.3) (column $v_{ss}^{\text{hvs}} + \tilde{v}_{ss}^{\text{hvs}}$). The steady-state value of the output voltage variation around v_{ss}^{hvs} is also presented (column $\tilde{v}_{ss}^{\text{hvs}}$) along with the normalized steady-state output voltage variation respect to the input current variation magnitude (column $\bar{v}_{ss}^{\text{hvs}} = \tilde{v}_{ss}^{\text{hvs}}/B$). The settling time (column τ) of the output voltage variation is included.

From the data presented in Table VI.1, an empirically obtained, average first-order system can be characterized by the averaged values of the dc gains and the time constants, presented in columns $\bar{v}_{ss}^{\text{hvs}} = \tilde{v}_{ss}^{\text{hvs}}/B$ and τ respectively. This and other methodologies used to choose a nominal plant to be used on the controller design, in the presence of parametric uncertainties, are explored by Skogestad and Postlethwaite in [86]. The trace of this averaged system is presented in Fig. VI.4 with the "*" mark, and the resulting average first-order, linear time-invariant system takes the form

$$G_4(s) = \frac{V^{\text{hvs}}(s)}{I_{fc}^{\text{ref}}(s)} = \frac{10.7686}{0.0298s + 1}, \tag{VI.4}$$

In our case, the output voltage controller is also to be implemented by means of an ADSP, so the continuous-time system must be discretized. Eq. (VI.5) shows the conversion result of Eq. (VI.4) into the z-domain. The sampling frequency is $f_s = 20$ kHz, and a ZOH is used.

$$G_4(z) = \frac{0.01804}{z - 0.9983} \tag{VI.5}$$

Current ripple limitation of the fuel-cell unit and general considerations

As mentioned in Section III.1 an input current low-pass filter, formed by the inductor L_{in} and the capacitor C_{in}, has been added to the chosen step-up converter topology with the purpose of protecting the FC unit from the high-frequency, discontinuous input current shape demanded by the converter. Recalling from Section II.1.2, this filter has a cut-off frequency of approximately 550 Hz.

These component values have allowed the application of frequency-domain system identification techniques to find a model of the converter that was latter used on the input current control design of the step-up stage in Chapter III. Nevertheless, the 550 Hz cut-off frequency is not restrictive enough to comply with the allowed bandwidth given in the specifications of the FC unit [5]. In order to cope with this limitation, the current references generated by the global power balance control loop are filtered, in this way, the input current control loop used on the step-up stage will demand, time responses from the FC within the recommended limits.

A discrete-time, first-order low-pass filter is added to the system in order to account for the bandwidth limitation on the response of the fuel cell. This filter has the discrete-time transfer function

$$H_{lp}(z) = \frac{3.1318 \cdot 10^{-3}(z+1)}{z - 0.9937}, \tag{VI.6}$$

with a cutoff frequency of 20 Hz. Also, a one sampling cycle delay needs to be included to account for the propagation of the one sampling period delay included into the input current control loop used for the step-up stage. Hence, the model of the plant to be controlled becomes:

$$P_4(z) = H_{lp}(z)\,\frac{1}{z}\,G_4(z) = \frac{5.6484 \cdot 10^{-5}(z+1)}{z(z-0.9937)\,(z-0.9983)}. \tag{VI.7}$$

VI.2 Global power balance controller design

The design of the global power balance control can be split in three parts:

The first one, the design of an output voltage regulation for the step-up stage alone. This controller regulates the dc bus voltage at $v^{\text{hvs}} = 425$ V dc, despite changes in the input voltage and/or the load. This is achieved by generating the appropriate i^{ref} current reference used to command the plant $P_4(z)$.

The second, in which the bounds on the FC power and the frequency decoupling of the current references are considered. The bounds on the power assure that the current references are within the design specifications for each of the modules. The frequency decoupling scenario routes the high-frequency requirements as a part of i_{sc}^{ref} and the low-frequency components as a part of i_{fc}^{ref}.

The third part is the design of the supercapacitor charge policy. This stage generates the charge current reference for the SCs bank, according to the power availability on the system.

VI.2.1 Unbounded global power balance controller design

Now, a discrete-time controller can be designed with the purpose of generating the appropriate current reference to be used by the plant $P_4(z)$ given in Eq. (VI.7), in order to obtain a constant step-up stage output voltage of $v^{\text{hvs}} = v_{bus} = 425$ V dc. With $P_4(z)$ as the nominal plant, a discrete-time PI-D controller of the form

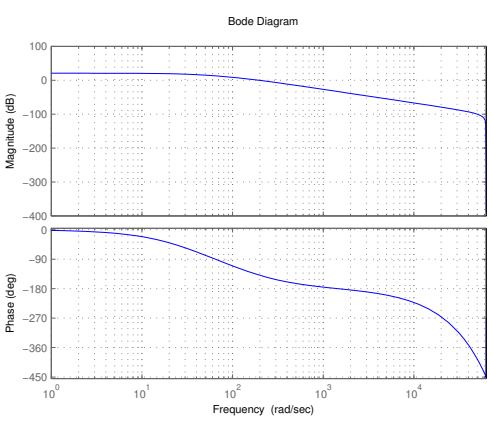
$$\begin{aligned} I^{\text{ref}}(z) &= (K_{p_4} + I_4(z))\,(V_{bus}^{\text{ref}}(z) - V_{bus}(z)) - D_4(z)\,V_{bus}(z) \\ &\quad \text{with} \\ I_4(z) &= K_{i_4}\,T_s \frac{z}{(z-1)} \\ D_4(z) &= \frac{K_{d_4}}{T_s}\frac{(z-1)}{z} \end{aligned} \tag{VI.8}$$

has been designed by finding convenient pole/zero locations. The values of the coefficients are $K_{i_4} = 22.7910$, $K_{p_4} = 0.7746$ and $K_{d_4} = 0.0027$ and the sampling period $T_s = 1/f_s = 1/20$ kHz.

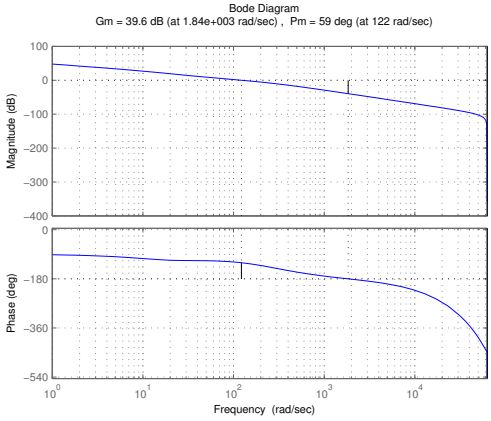
Fig. VI.5 shows the open/closed-loop plots for the design of the controller presented in Eq. (VI.8). Fig. VI.5(a) shows the Bode plot for the discrete-time transfer function $P_4(z)$, presented in Eq. (VI.7). Fig. VI.5(b) shows the Bode plot for the open-loop transfer function $L_4(z) = (K_{p_4} + I_4(z))\,P_4'(z)$, with $P_4'(z) = P_4(z)/(1 + D_4(z)\,P_4(z))$. As it can be observed, this design presents a gain margin of 39.6 dB at $1.84 \cdot 10^3$ rad/s, and a phase margin of 59 ° at 112 rad/s. The Bode plot of the closed-loop transfer function $T_4(z) = (K_{p_4} + I_4(z))\,P_4'(z)/(1 + (K_{p_4} + I_4(z))\,P_4'(z))$ presents no significative closed-loop resonances as can be noticed by the maximum peak closed-loop gain of $||T_4(z)||_\infty = 0.799$ dB at 65.1 rad/s shown in Fig. VI.5(c). This fact can be also observed in the Nyquist plot for the open-loop transfer function $L_4(z)$ presented in Fig. VI.5(e). Under these conditions this design presents a $||S_4(z)||_\infty = 2.39$ dB at 208 rad/s, where $S_4(z) = 1/(1 + (K_{p_4} + I_4(z))\,P_4'(z))$ is the closed-loop output sensitivity transfer function shown in Fig. VI.5(d), and that according to Doyle *et al.* [27] is an adequate stability margin.

An anti-windup loop has been added to avoid unbounded growth of the integral part of the controller of Eq. (VI.8). This loop acts over the global current reference i^{ref}, which must be bounded to assure demanded current values to the FC unit and the step-up stage that lie within the allowed limits. The open-loop transfer function of this new loop takes the form

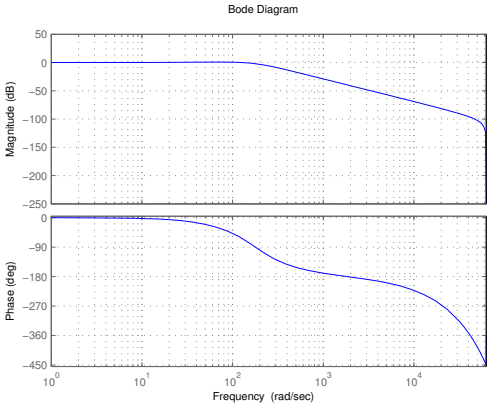
$$L_{\text{aw}_4}(z) = \left(\frac{K_{\text{aw}_4}}{z}\right)\left(K_{i_4}\,T_s\frac{z}{(z-1)}\right). \tag{VI.9}$$



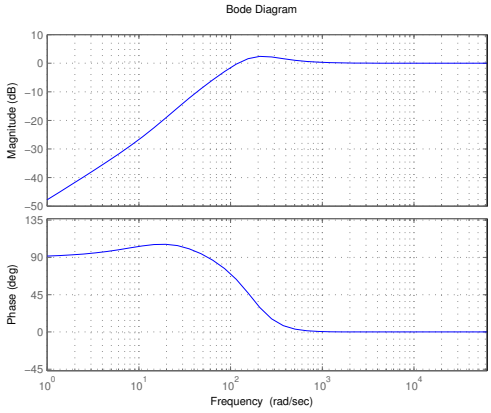
(a) Bode plot of the nominal plant ($P_4(z)$).



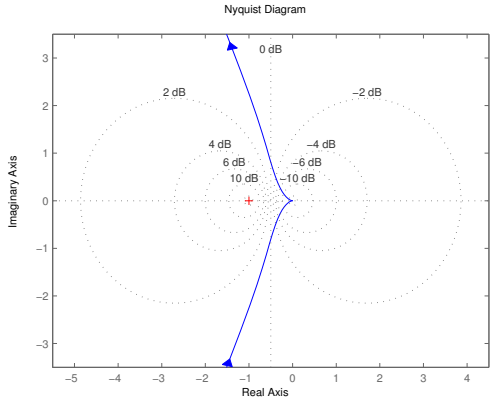
(b) Open-loop Bode plot ($L_4(z)$).



(c) Closed-loop Bode plot ($T_4(z)$).



(d) Bode plot of the output sensitivity transfer function ($S_4(z)$).



(e) Open-loop Nyquist plot ($L_4(z)$).

Figure VI.5: Open and closed loop Bode and Nyquist plots for the initial global power balance controller with the nominal plant $P_4(z)$.

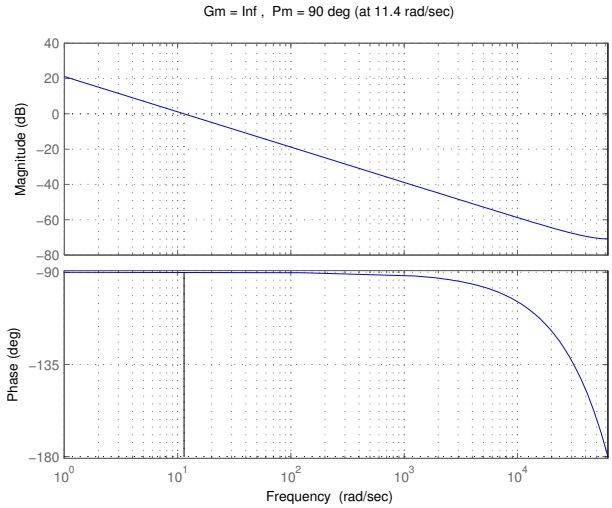


Figure VI.6: Bode plot of the anti-windup open-loop transfer function L_{aw_4} used on the unbounded global power balance control.

The global current reference anti-windup control loop is stable for values of K_{aw_4} within the range

$$0 < K_{aw_4} < \frac{2}{K_{i_4}\, T_s}. \tag{VI.10}$$

By replacing the values of K_{i_4} and T_s given before into Eq. (VI.10), the bounds on the anti-windup constant K_{aw_4} become $0 < K_{aw_4} < 1755.08$. In this case, the chosen anti-windup constant is $K_{aw_4} = 0.50$. Fig. VI.6 shows the Bode plot of the open anti-windup loop. As can be observed, the high levels achieved on the gain and phase margin guarantee the stability of the closed-loop system.

Now that a v^{hvs} controller has been developed for the step-up converter working with the input current control closed, a calculation on the power that the FC unit must provide can be performed. This is achieved by multiplying the current reference given by the power balance control by the voltage of the FC unit $p^{\mathrm{ref}} = i^{\mathrm{ref}}\, v_{fc}$, this is the power that the FC would have to provide if there were no limitations on its bandwidth and/or the maximum power. This new variable p^{ref} is the expected global power that the energy conditioning system must provide.

Fig. VI.7 shows the block diagram of the controller presented in Eq. (VI.8) using the variable p^{ref}. The use of p^{ref} instead of i^{ref} as the control variable, turns out to be advantageous, as the current references can be obtained by dividing the power reference by the voltage of the module to be commanded. By performing this change, the bounds used for the anti-windup loop become power level instead of current level bounds. Now let $[\mathrm{GPC\_PWR\_MIN}, \mathrm{GPC\_PWR\_MAX}]$ be

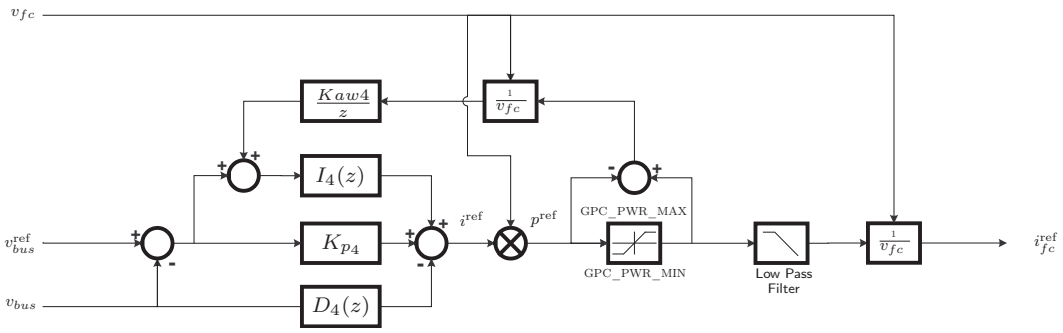


Figure VI.7: Unbounded power balance control scheme.

the allowed operative power range of the energy conversion system. Therefore, the actual global power reference is

$$p_{\text{sat}}^{\text{ref}} = sat_{\text{GPC\_PWR\_MIN}}^{\text{GPC\_PWR\_MAX}}(p^{\text{ref}}), \tag{VI.11}$$

with

$$sat_{\text{a}}^{\text{b}}(x) \begin{cases} a, & \text{if } x < a, \\ x, & \text{if } a < x < b, \\ b, & \text{if } x > b. \end{cases} \tag{VI.12}$$

VI.2.2 Maximum power ratings/specifications considerations

If the output power has reached the maximum power allowed to be supplied by the FC unit, then a current reference command must be generated for the APU until the overload condition is overcome. To account for the maximum power limitations of the fuel-cell unit and the APU, hard limits are imposed on the power references that are given to each of the modules. A saturation on the maximum power reference to the step-up stage has been added in the form

$$p_{fc}^{\text{ref}} = sat_{0}^{\text{PWR\_STP\_MAX}}(p_{lp}^{\text{ref}}), \tag{VI.13}$$

where $p_{lp}^{\text{ref}} = h_{lp}(p_{\text{sat}}^{\text{ref}})$ and PWR_STP_MAX corresponds to the maximum power that the FC unit is able to provide. As the FC is a current unidirectional power supply, the lowest power level that can be demanded from it is 0 W.

In the case of an overload condition, the remaining power reference above PWR_STP_MAX is routed as part of the power reference for the APU and, after the appropriate translation, it becomes part of the total current reference to the APU bank of SCs control current reference

(i_{sc}^{ref}). Let PWR_APU_MAX be the maximum power that can be extracted/injected from/towards the APU. Then, the maximum GPC_PWR_MAX and the minimum GPC_PWR_MIN bounds over the global power reference variable p^{ref} are determined by the values of PWR_STP_MAX and PWR_APU_MAX, taking the form

$$\text{GPC\_PWR\_MAX} = \quad \text{PWR\_APU\_MAX} + \text{PWR\_STP\_MAX} \tag{VI.14}$$

$$\text{GPC\_PWR\_MIN} = \; - \; \text{PWR\_APU\_MAX} \tag{VI.15}$$

Fig. VI.8 shows the resulting power balance control loop including the maximum/minimum power considerations of each of the modules. The power reference given to the step-up stage is the global power reference p^{ref} when it is in the range $[0, \text{PWR\_STP\_MAX}]$. This can be observed by the addition of the saturation after the low-pass filter block. If the global power balance control has generated a power reference beyond this interval, the overflow power reference is extracted in the form

$$p_{ovl}^{\text{ref}} = p_{lp}^{\text{ref}} - sat_0^{\text{PWR\_STP\_MAX}}(p_{lp}^{\text{ref}}), \tag{VI.16}$$

and it is routed as part of the power reference to the APU. A sign change is performed, in order to match the sign convention of the APU SCs current control loop. After this, the current reference for the APU control loop is obtained by dividing the exceeding power reference by the voltage present at the bank of SCs v_{sc}.

Finally, the rms measurement of the power delivered at the output of the dc-ac inversion stage (p_{out}), is added to the control system by means of a feed-forward path, in order to improve the response time of the system to load variations. The power reference generated by the global power balance control becomes:

$$p^{\text{ref}} = p_{out} + i^{\text{ref}}\, v_{fc}, \tag{VI.17}$$

By doing this change, the global power balance controller is only in charge of handling the variations around the power demanded at the output of the dc-ac inversion stage (p_{out}), and therefore, the response speeds of the controller are improved. Fig. VI.8 shows the modified version of the controller designed in Section VI.2.1, now including the maximum/minimum power ratings of the step-up and the APU stages.

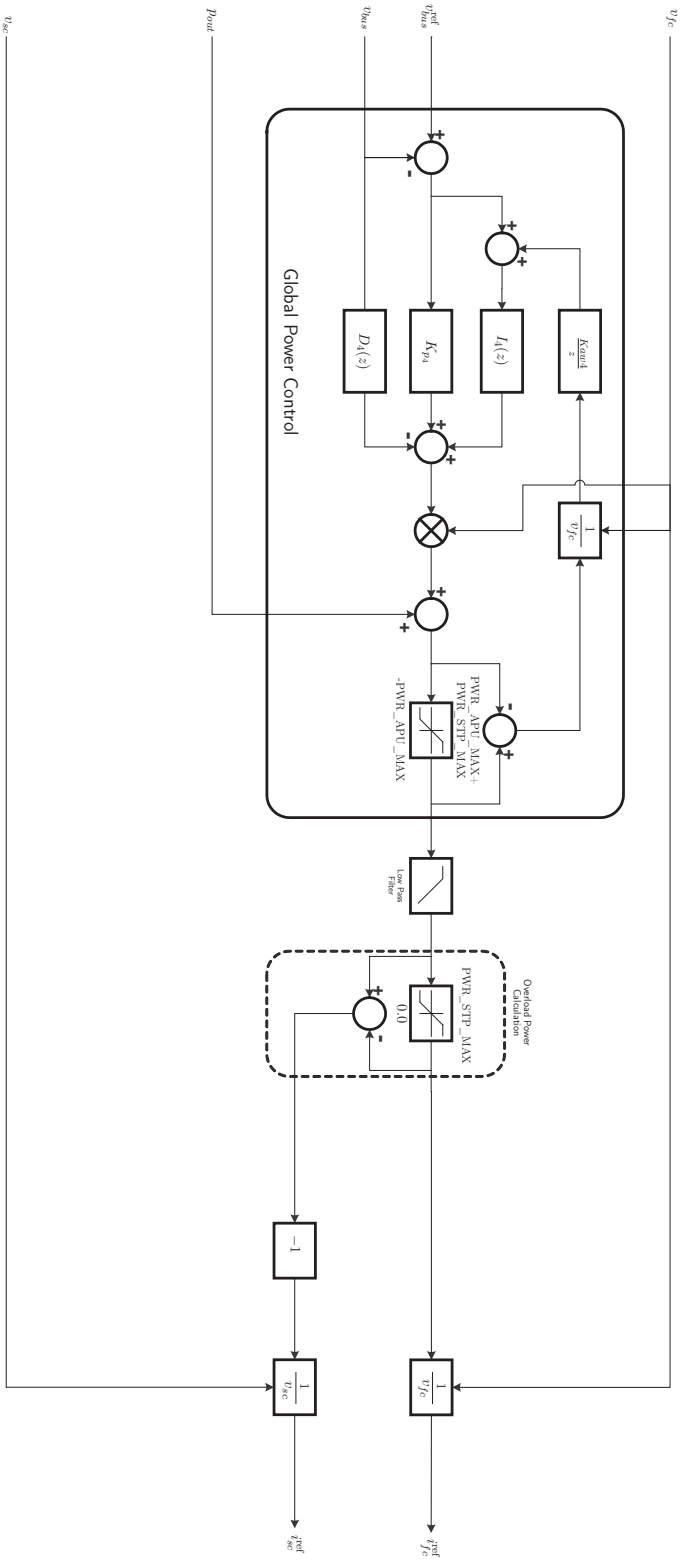


Figure VI.8: Power balance control scheme including the minimum/maximum power limitations of the modules.

VI.2.3 Frequency decoupling scenario consideration

As mentioned before, the FC unit has a relatively slow response to fast variations on its electrical quantities, to overcome this, a frequency decoupling scenario between the input current to the step-up converter and the APU current has been considered. The APU is in charge of supplying extra energy not only when the nominal output power level (PWR_STP_MAX) is overpassed, but also for the high-frequency power requirement variations that the FC unit is not able to satisfy. The fuel-cell unit is in charge of supplying only the low-frequency power demands while working within the limits defined by the specifications of the system.

The high frequency variations must now be included as a part of the APU power reference p_{sc}^{ref}. This is achieved by applying the complementary high-pass filter h_{hp} to the global power balance reference $p_{\text{sat}}^{\text{ref}}$. The low/high-frequency filters used (h_{lp} and h_{hp}) have been designed in such a way that they comply with the relationship

$$p_{\text{sat}}^{\text{ref}} = p_{lp}^{\text{ref}} + p_{hp}^{\text{ref}}, \tag{VI.18}$$

with $p_{lp}^{\text{ref}} = h_{lp}(p_{\text{sat}}^{\text{ref}})$ and $p_{hp}^{\text{ref}} = h_{hp}(p_{\text{sat}}^{\text{ref}})$. In this way, the whole bandwidth of the global power balance control reference is kept. The relationship held by the low/high-pass filters above can be rewritten into the z-domain as

$$1 = H_{lp}(z) + H_{hp}(z), \tag{VI.19}$$

and by taking the definition for $H_{lp}(z)$ given in Eq. (VI.6), the z-domain transfer function of the high-pass filter $H_{hp}(z)$ is found. Fig. VI.9 shows the power balance control loop with the absolute maximum/minimum power ratings of the modules and the frequency decoupling between the step-up and the APU current references included.

As it can be observed, the APU power reference is formed, up to now, by two components which compensate the dynamic behavior of the FC. The high-frequency component compensates the limited response speed capabilities of the FC, and the low-frequency component compensates the maximum output power limitation of the fuel-cell unit. These two power reference components are added and latter the current reference for the APU SCs control stage is obtained dividing by the voltage present at the bank of SCs v_{sc}. Again, a sign change is performed over the APU power reference to match the sign convention used on the APU SCs current control loop.

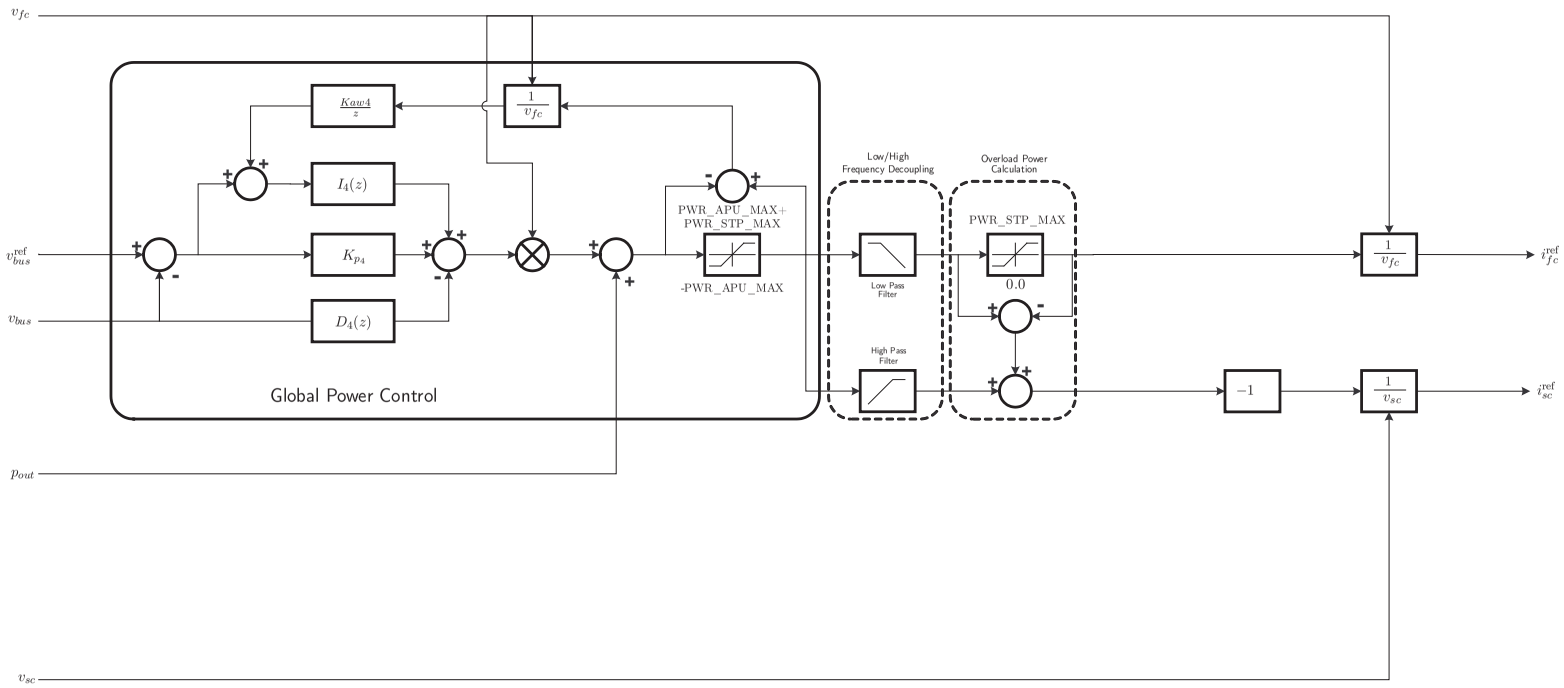


Figure VI.9: Power balance control scheme including the frequency decoupling of the power references delivered to the APU and step-up stages.

VI.2.4 Supercapacitor bank charge power reference generation

After an overload condition, or during the start-up process of the energy conditioning system, this part of the global power balance control loop generates a power command for the APU that allows the charging process of the bank of SCs to start. This process continues until a voltage level of v_{sc} =Vsc_MAX is reached at the bank of SCs, where Vsc_MAX is the full charge voltage level. At this point, the charge component of the APU power reference is set to zero, until a new overload condition presents. In order to generate the appropriate SCs charge power reference for the APU, two things have to be considered: the first, the available power that the FC can provide, and the second, the state of charge of the bank of SCs.

Let PWR_APU_CHRG_MAX be the maximum allowed power level to be provided by the FC for the purpose of the charging the bank of SCs. As the energy used to charge the bank of SCs is extracted from the FC unit, then PWR_APU_CHRG_MAX must comply with the relationship PWR_APU_CHRG_MAX $\leq$ PWR_STP_MAX. The available power that can be provided by the FC unit can be found in the form

$$p_{fc}^{\text{available}} = sat_0^{\text{PWR\_STP\_MAX}}(\text{PWR\_STP\_MAX} - p_{out}), \tag{VI.20}$$

where p_{out} is the rms measurement of the power delivered at the output of the dc-ac inversion stage.

On the other hand, the state of charge of the bank of SCs is directly related to the voltage v_{sc} present at its terminals. If v_{sc} $\geq$Vsc_MAX, then the SCs charge power reference must be zero. If v_{sc} <Vsc_MAX, then a SCs charge power reference must be generated, but only if $p_{fc}^{\text{available}} > 0$.

The SCs charge policy has been designed introducing a scaling factor (dependent on the stat of charge of the bank of SCs,) over the available power $p_{fc}^{\text{available}}$, following the criteria:

1. Let Vsc_CNT_CHR, with Vsc_CNT_CHR < Vsc_MAX. The system must generate the maximum SCs charge power reference possible if v_{sc}<Vsc_CNT_CHR. This means that for values of v_{sc}<Vsc_CNT_CHR, the scaling factor over $p_{fc}^{\text{available}}$ is 1.

2. If v_{sc}>Vsc_CNT_CHR, then the power reference must be reduced in a uniform way, reaching a value of 0 when v_{sc} $\geq$Vsc_MAX

By analyzing the desired behavior criteria, two scaling factor points are determined depending on the voltage level of v_{sc}. The first point (Vsc_CNT_CHR,1) is determined by the point v_{sc} =Vsc_CNT_CHR at which the scaling factor must begin to decrease, with an starting value of 1. The second point for the desired scaling factor behavior (Vsc_MAX,0) is determined by the full charge voltage level v_{sc} =Vsc_MAX beyond which, a null charge power reference must be generated.

With these two points, and affine relationship can be found between the desired scaling factor and the voltage present at the bank of SCs. If this affine relationship is saturated for those values grater than one and lower than zero, the final expression for the scaling factor is found, and then, the power reference for the charge of the bank of SCs becomes

$$p_{sc}^{\text{charge}} = p_{fc}^{\text{available}}\, sat_0^1 \left(\frac{\text{Vsc\_MAX} - v_{sc}}{\text{Vsc\_MAX} - \text{Vsc\_CNT\_CHR}} \right), \tag{VI.21}$$

that is the product between the available power that can be provided by the FC unit p_{fc}^{charge}, and the scaling factor, which is dependent on the state of charge of the bank of SCs.

By adding the overload, the high-frequency, and the SCs charge power references (as defined in Eqs. (VI.16), (VI.18) and (VI.21) respectively) with the adequate sign convention, the APU power reference, and hence, the complete APU power reference is found as

$$p_{sc}^{\text{ref}} = -(p_{ovl}^{\text{ref}} + p_{hp}^{\text{ref}}) + p_{sc}^{\text{charge}}. \tag{VI.22}$$

From Eq. (VI.22), the current reference to be delivered to the APU SCs current control loop is found as $i_{sc}^{\text{ref}} = p_{sc}^{\text{ref}}/v_{sc}$. Fig. VI.10 shows the final configuration of the global power balance control loop. This control stage receives as inputs: the voltage of the FC unit v_{fc}, the voltage of the bank of SCs v_{sc}, the output power measurement p_{out}, the reference voltage at the dc bus v_{bus}^{ref} and the voltage present at the dc bus v_{bus}. With all those inputs, the global power balance control scheme delivers the current reference to be used by the input current control loop of the step-up conversion stage i_{fc}^{ref}, and the SCs current reference used on the control of the dc-dc interfacing converter of the APU i_{sc}^{ref}.

VI.3 Energy conditioning system simulation results

The designed global power balance control scheme has been tested over a simulation model of the energy conditioning system. All the conversion stages work under hard switching. All the inner control loops have been closed, the step-up stage input current control, the APU SCs current control and the dc-ac output voltage control. The global power control has been implemented using the same C++ code that will be used on the tests over the experimental setup. This control scheme delivers the current references for the inner current control loops (i_{sc}^{ref} and i_{fc}^{ref}). The commanded switches of the converters implemented on the simulation environment are operated by centered pulse, single-update mode, PWM with a switching frequency of $f_{sw} = 20$ kHz. The simulation environment used and the considerations taken to perform the simulations are described in detail in Section II.3. The time step used on the solver of the simulation environment in this case is $1 \cdot 10^{-6}$ s.

The PWM synchronization signal is used to latch the measured signals, and therefore, the sampling frequency is also $f_s = 20$ kHz. A delay of one sampling period is included at the input of the PWM module to account for the delay introduced by the load of the PWM register that will be present at the ADSP of the experimental setup. The conduction losses of the semiconductors are included into the model, the parasitic losses of the components are also considered.

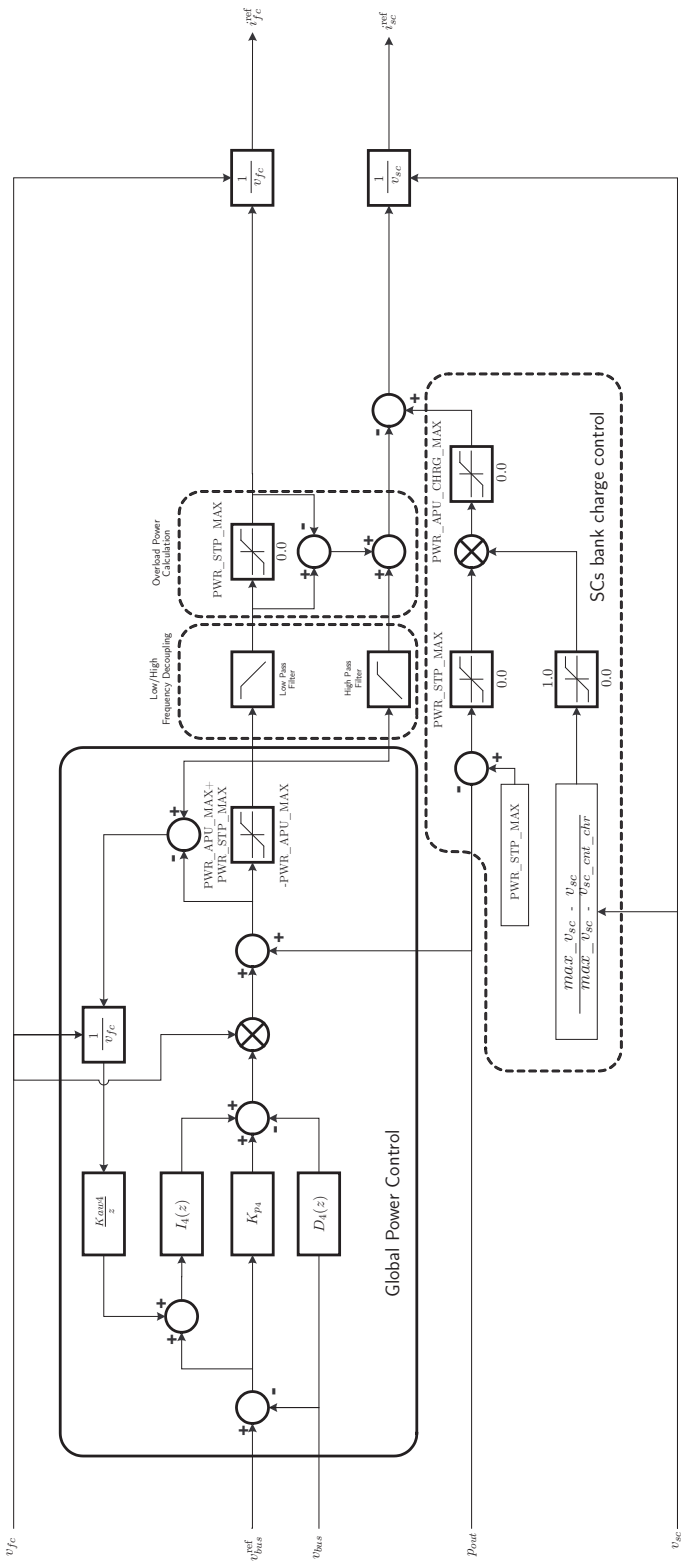


Figure VI.10: Global power balance control scheme.

The electrical behavior of the FC unit has been implemented by programming the power and polarization curves of the MAN5100078 FC unit (see Fig. II.2) over a look-up table. An output voltage reference is delivered to a voltage-controlled voltage source according to the current level demanded by the step-up stage. A low-pass filter with a cut-off frequency of 5 Hz has been used to account for the response speed of the FC unit. The low-pass filter acts over the current measurement which is feedback and used as input by lookup table.

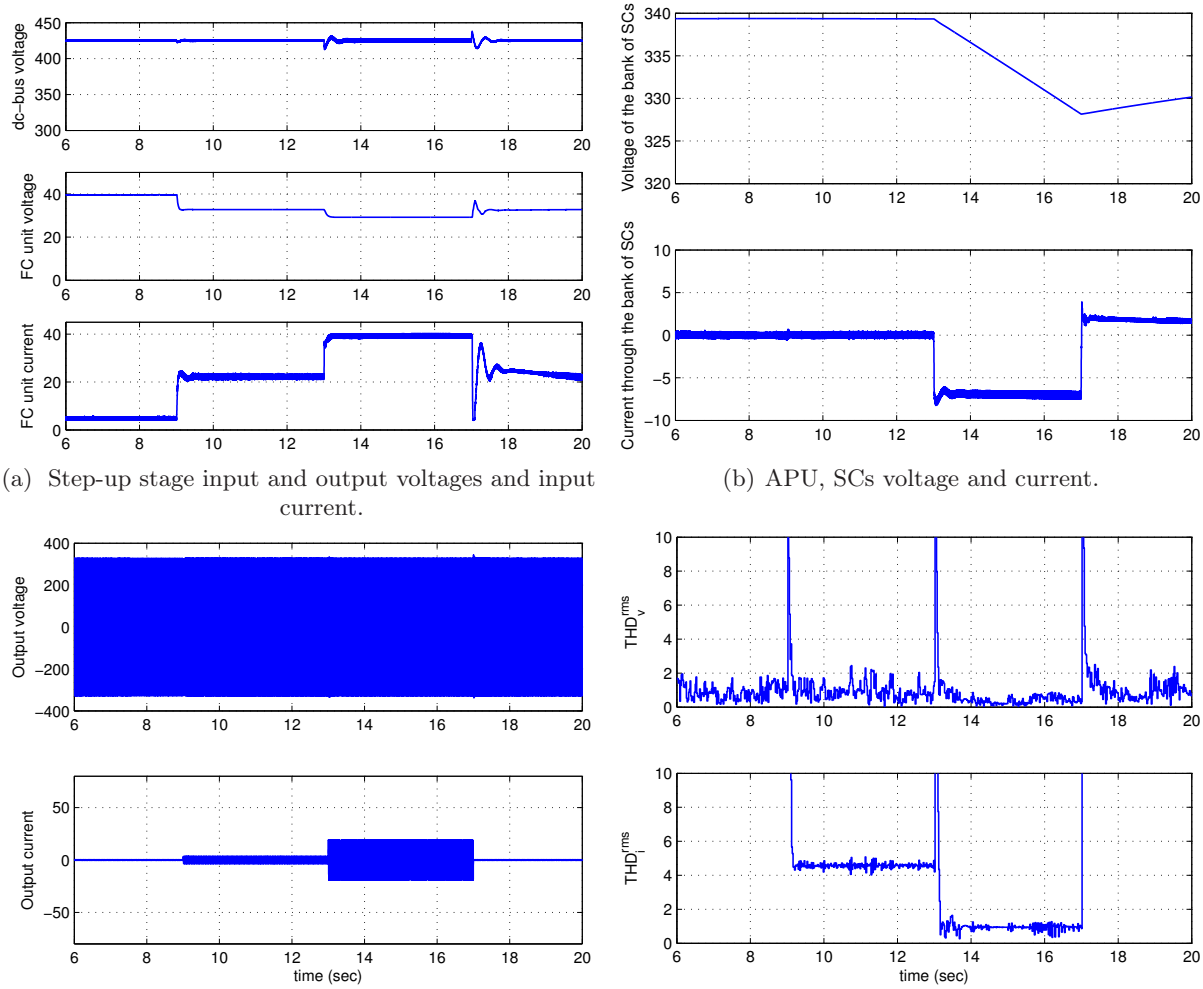
Two sets of simulation tests have been performed. In the first, the response of the energy conditioning system has been evaluated in front of linear load changes. Load changes from empty to loaded, loaded to overload and from overload to empty conditions are performed. In the second set of tests, the system has been used to feed nonlinear loads. These tests follow the same load changes scheme explained before. In all cases, the active power component of the loads used lie within the nominal and overload active power specifications given in Section I.2.1.

VI.3.1 Linear loads

For the linear load changes test, resistive loads have been used. The system has been driven to steady state while not feeding any load. At $t = 9$ s a load change is performed, a 520 W resistive load is connected. This load level is held until $t = 13$ s when a total resistive load of 3100 W is connected, driving the energy conditioning system to work under overload condition, and therefore, some energy is extracted from the bank of SCs. The overload is removed from the system at $t = 17$ s, making the system work again under no-load condition.

Fig. VI.11 shows the energy conditioning system response under the linear load changes test. The output voltage as well as the input current and voltage of the step-up stage are presented in Fig. VI.11(a). Fig. VI.11(b) shows the current and voltage levels present at the bank of SCs. The output voltage and current present at the dc-ac inverter is presented in Fig. VI.11(c). Fig. VI.11(d) shows the $\mathrm{THD_i^{rms}}$ and $\mathrm{THD_v^{rms}}$ levels achieved during the test.

The energy conditioning system starts to work with no load connected at the output of the dc-ac inverter. Fig. VI.11(a) shows that from $t = 6$ to $t = 9$ s, the step-up stage has an average input voltage of 39.58 V dc and an average input current of 4.88 A dc. This fact implies that about $p_{fc} = v_{fc}\, i_{fc} = 190$ W are demanded from the FC unit in order to supply the parasitic losses of the energy conditioning system under no-load condition. At $t = 9$ s the resistive load of 520 W is connected to the terminals of the dc-ac inverter. No over/undershoot is noticeable in the voltage of the dc-bus. The voltage provided by the FC drops down to 32.76 V dc and the input current increases its average value up to 22.44 A dc. A total power of $p_{fc} = v_{fc}\, i_{fc} = 735$ W is extracted from the FC in order to be able to supply the load. This load level is held until $t = 13$ s when a total load of 3100 W is connected to the output. At this point, the voltage at the dc-bus falls down to 412.46 V dc. This voltage drop can be translated into a 2.93 % undershoot below the steady-state value of the dc-bus voltage. Under these conditions, the input voltage drops down to 29.19 V dc and the input current grows up to 39.40 A dc. This fact means that the power being extracted from the FC is about $p_{fc} = v_{fc}\, i_{fc} = 1150$ W. This value coincides with the PWR_STP_MAX= 1150 W value used for the simulations, this value accounts for the almost 200 W losses, taking into account the absolute maximum power rating of the MAN5100078,



(a) Step-up stage input and output voltages and input current.

(b) APU, SCs voltage and current.

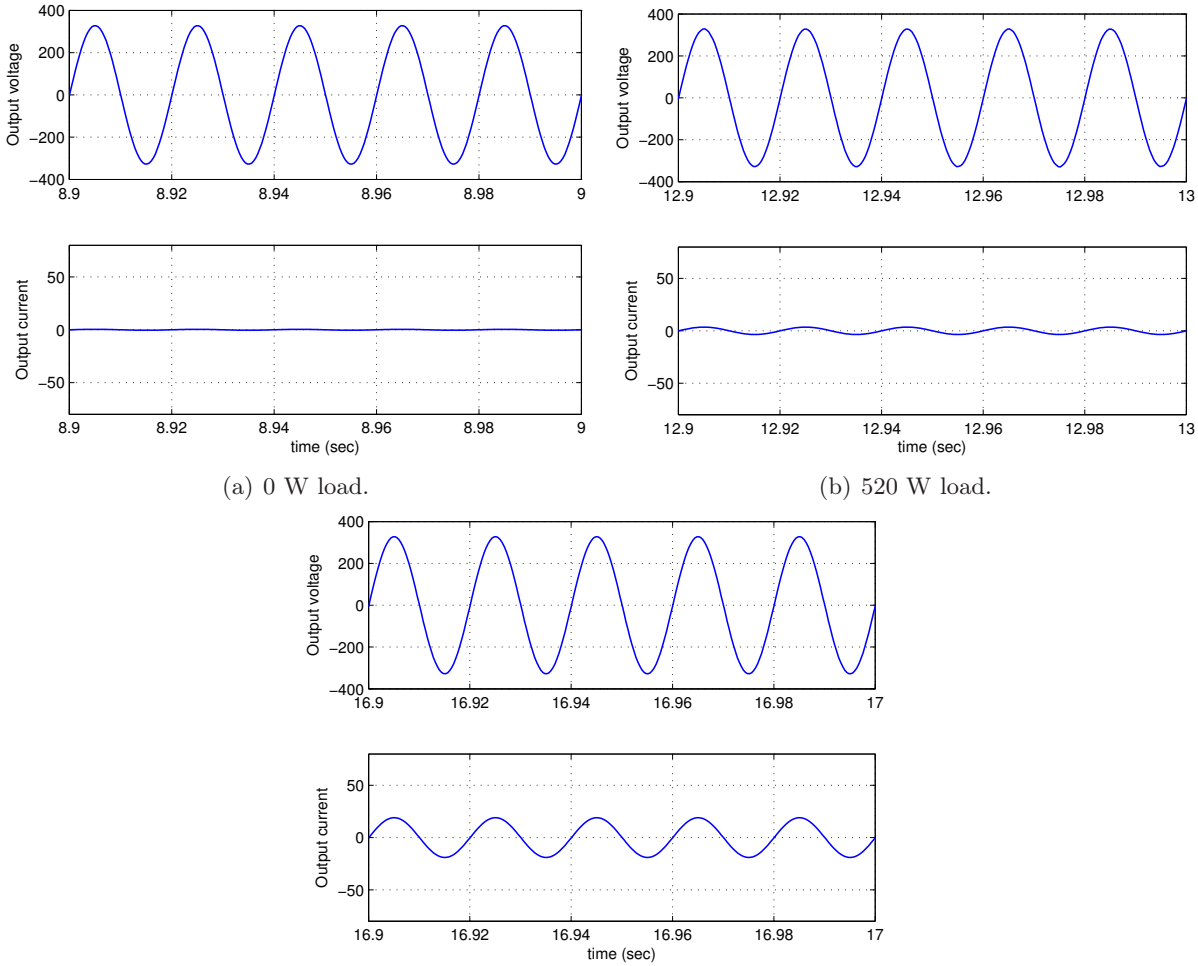
(c) Dc-ac inversion stage, output voltage and current.

(d) Dc-ac inversion stage, output voltage and current THD_i^{rms} and THD_v^{rms}.

Figure VI.11: Energy conditioning system feeding linear loads.

which is 1200 W. The overload condition is held until $t = 17$ s when the load is removed, making the system return to its initial condition. At this point, the voltage at the dc-bus grows up to 438.11 V dc, in other words, a 3.1 % voltage overshoot presents at the dc-bus.

The extra energy that the FC is not able to provide is extracted from the bank of SCs from $t = 13$ s until $t = 17$ s. As it can be seen in Fig. VI.11(a) after the overload condition is removed, an undershoot is present in the input current demand, reaching a steady-state value of about 22.37 A dc. The input voltage reaches a steady-state value of 32.76 A dc. Under this circumstances about 730 W are demanded from the FC unit to recharge the bank of SCs after the overload has been removed.



(a) 0 W load.

(b) 520 W load.

(c) 3100 W load.

Figure VI.12: Steady-state simulation results of the behavior of the full-bridge dc-ac inverter under the different (linear) load conditions present on the test.

Fig. VI.11(b) shows the voltage and current behavior of the SCs during the simulation test. From $t = 6$ to $t = 13$ s, the voltage of the SCs is 340 V dc and a 0 average current flows through the bank of SCs, meaning that the FC unit is able to provide all the energy needed by the load and therefore no energy extraction from the bank of SCs is needed. At $t = 13$, a SCs current reference is generated in order to supply the extra energy that the FC is not able to provide. From $t = 13$ to $t = 18$ s about 2300 W are extracted from the bank of SCs to complement the power being extracted from the FC unit, delivering at the output a total of 3100 W. From $t = 17$ s on, a current of about 1.63 A dc is injected to the bank of SCs in order to recover the full-charge state of the bank.

Fig. VI.11(c) shows the response of the energy conditioning system at the dc-ac inverter. The load changes are evident by the change in the output current levels. There are no noticeable voltage undershoots or overshoots in the output voltage shapes. Fig. VI.11(d) shows the $\text{THD}_{\text{i}}^{\text{rms}}$ and $\text{THD}_{\text{v}}^{\text{rms}}$ levels achieved. As it can be observed, the steady-state $\text{THD}_{\text{v}}^{\text{rms}}$ lies below 2 %

which complies with the maximum $\text{THD}_\text{v}^\text{rms} = 3$ % given in the specifications of the system in Section I.2.1.

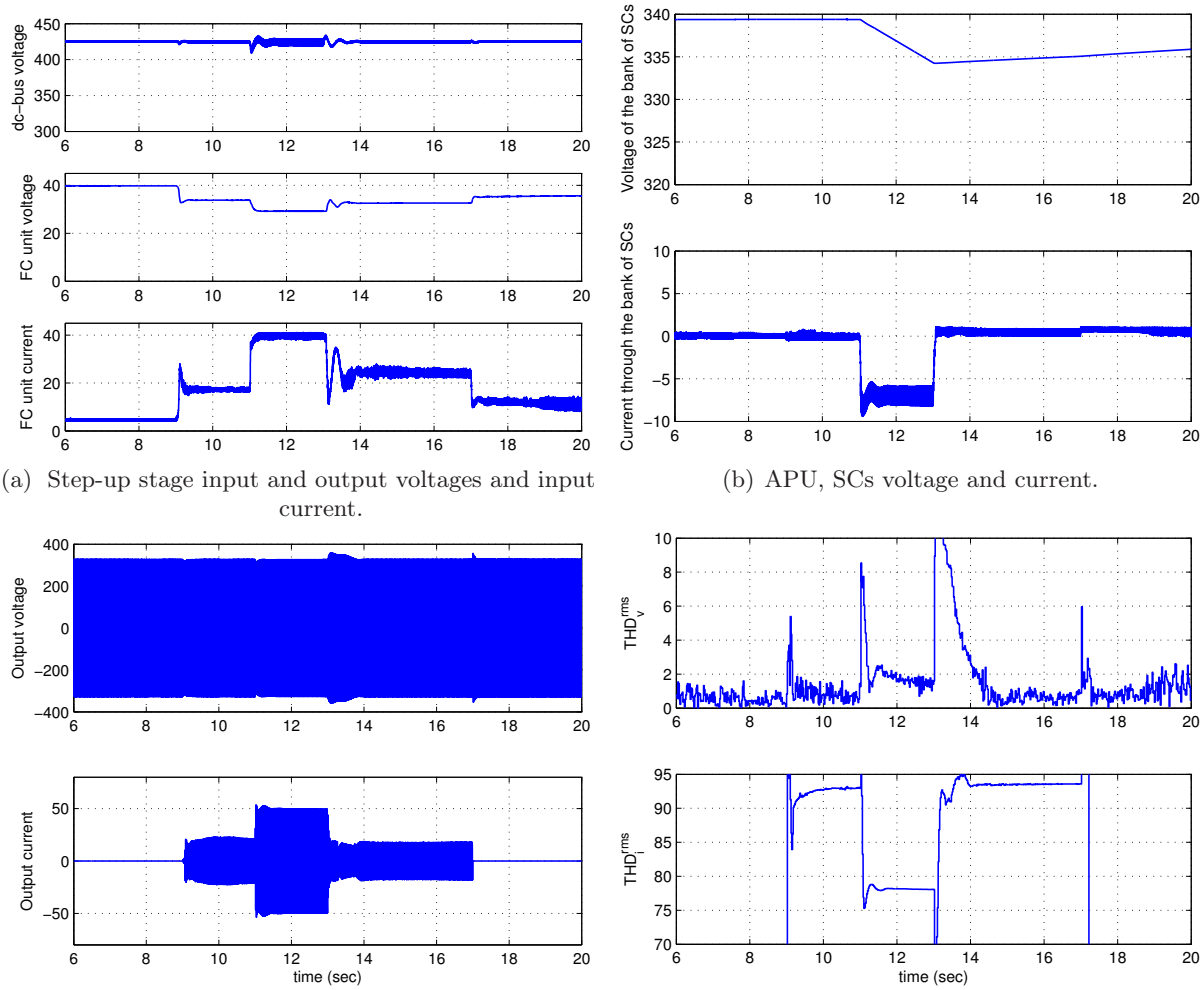
Fig. VI.12 shows the steady-stage output voltage shapes under the three different output power conditions used on the test. The good reference tracking capabilities of the AFC control used on the dc-ac inverter is confirmed by the good sinusoidal output voltage shapes under the no-load condition (see Fig. VI.12(a)), the 520 W load condition (see Fig. VI.12(b)) and the 3100 W overload condition (see Fig. VI.12(c)).

VI.3.2 Nonlinear loads

For the nonlinear load changes test, a full-bridge diode rectifier with a RC load has been used. The system has been driven to steady state while not feeding any load. At $t = 9$ s a load change is performed, a 1032 VA (with an active power component of 366 W) rectified load is connected. This load level is held until $t = 11$ s when a total rectified load of 4425 VA (with an active power component of 2765 W) is connected, driving the energy conditioning system to work under overload condition, and therefore, some energy is extracted from the bank of SCs. The overload is removed from the system at $t = 13$ s, making the system work again under the 1032 VA load condition. At $t = 17$ s the load is removed, making the system return to its no-load condition.

Fig. VI.13 shows the energy conditioning system response under the nonlinear load changes test. The output voltage as well as the input current and voltage of the step-up stage are presented in Fig. VI.13(a). Fig. VI.13(b) shows the current and voltage levels present at the bank of SCs. The output voltage and current present at the dc-ac inverter is presented in Fig. VI.13(c). Finally, Fig. VI.13(d) shows the $\text{THD}_\text{i}^\text{rms}$ and $\text{THD}_\text{v}^\text{rms}$ levels achieved during the test.

The energy conditioning system starts to work with no load connected at the output of the dc-ac inverter. Fig. VI.13(a) shows that from $t = 6$ to $t = 9$ s, the step-up stage has an average input voltage of 39.78 V dc and an average input current of 4.6 A dc. This fact implies that about $p_{fc} = v_{fc}\, i_{fc} = 180$ W are demanded from the FC unit in order to supply the parasitic losses of the energy conditioning system under no-load condition. At $t = 9$ s the rectified load of 1032 VA (366 W) is connected to the terminals of the dc-ac inverter. No noticeable under/overshoot in the voltage of the dc bus is observed. The voltage provided by the FC drops down to 33.80 V dc and the input current increases its average value up to 17.34 A dc. A total power of $p_{fc} = v_{fc}\, i_{fc} = 586$ W is extracted from the FC in order to be able to supply the load. This load level is held until $t = 11$ s when a total of 4425 W (2765 W) is connected to the output. At this point, the voltage at the dc-bus falls down to 409.22 V dc, being translated into a 3.68 % undershoot below the steady-state value of the dc-bus voltage. Under these new load conditions, the input voltage drops down to 29.19 V dc and the input current grows up to 39.40 A dc. This state is held until $t = 13$ s when the overload is removed, returning the system to its previous 1032 VA load condition. At the moment that the overload is removed, the voltage at the dc bus grows up to 433.65 V dc, in other words, a 2.02 % voltage overshoot presents at the dc bus. In this case, the steady-state value of the input voltage grows up to 32.64 V dc with the input current dropping down to a 23.61 A dc, meaning that about 770 W are demanded from the FC unit in order to feed the 1032 VA load and the parasitic losses, the rest of the energy is routed to charge the bank of SCs.



(a) Step-up stage input and output voltages and input current.

(b) APU, SCs voltage and current.

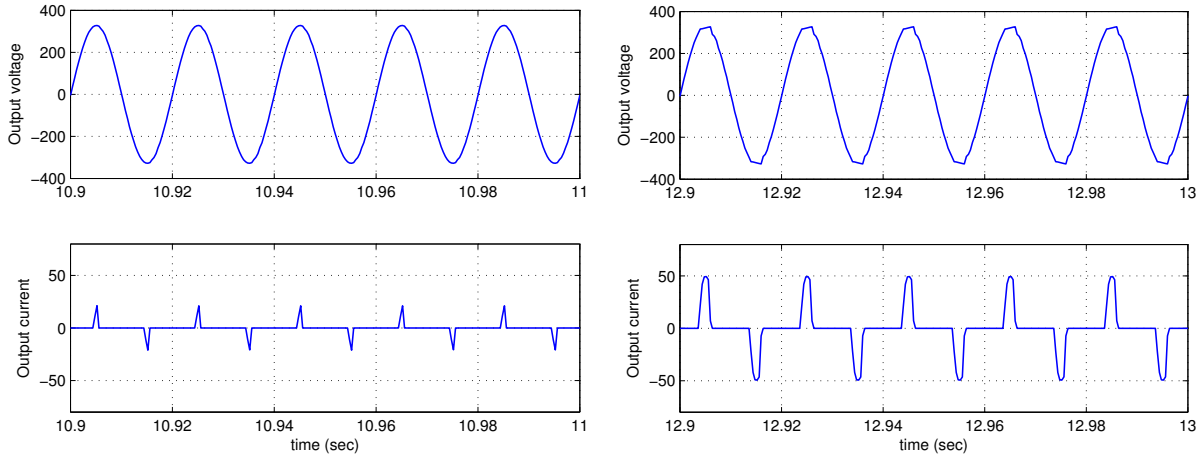
(c) Dc-ac inversion stage, output voltage and current.

(d) Dc-ac inversion stage, output voltage and current THD$_i^{rms}$ and THD$_v^{rms}$.

Figure VI.13: Energy conditioning system feeding nonlinear loads.

At $t = 17$ s the load is removed making the system return to its no-load condition. No noticeable under/overshoot is present in the voltage of the dc bus. Under this new load condition, the input voltage grows up to 36.65 V dc and the input current falls down to 11.14 A dc. This fact implies that about $p_{fc} = 408$ W are demanded from the FC unit to allow the charge of the bank of SCs.

Fig. VI.13(b) shows the voltage and current behavior of the SCs during the simulation test. From $t = 6$ to $t = 11$ s, the voltage of the SCs is 340 V dc and a 0 average current flows through the bank of SCs, meaning that the FC unit is able to provide all the energy needed by the load and therefore no energy extraction from the APU is needed. At $t = 11$ the energy conditioning system starts to operate under overload condition. A SCs current reference is generated in order to supply the extra energy that the FC is not able to provide. From $t = 11$ to $t = 13$ s about 2150 W are extracted from the bank of SCs to complement the power being extracted from the FC unit, delivering at the output a total of 2765 W. From $t = 13$ s to $t = 17$ s, a charge current



(a) 1032 VA (366 W active power) load.

(b) 4425 VA (2765 W active power) load.

Figure VI.14: Steady-state simulation results of the behavior of the full-bridge dc-ac inverter under the different (nonlinear) load conditions present on the test.

of about 0.5 A dc is injected to the bank of SCs. From $t = 17$ s on, when the system is returned to work under the no-load condition, a current of about 0.75 A dc is injected to the bank of SCs in order to recover the full-charge state of the bank.

Fig. VI.13(c) shows the voltage and current delivered at the output of the full-bridge dc-ac inverter. A more detailed view of the output voltage and current shapes is given in Fig. VI.14 for the different load levels used in the test. At $t = 9$ s the 1032 VA load is connected. An almost negligible undershoot occurs in the output voltage amplitude when the load is connected, but the system recovers the desired output voltage amplitude in about 10 cycles. Fig. VI.14(a) shows the steady-state output voltage and current shapes under this load condition. The output current shape has a value of 4.49 A rms, with peaks reaching 17.67 A implying a crest factor of 3.94. A $\text{THD}_{\text{v}}^{\text{rms}} < 2$ % can be observed for this load condition in Fig. VI.13(d) just before the next load change takes place. The periodic output disturbance capabilities of the AFC control loop are evidenced by the rich odd harmonic content of the output current shape. A $\text{THD}_{\text{i}}^{\text{rms}} > 90$ % can be noticed, evidencing the highly disturbed shape of the current.

At $t = 11$ s a total 4425 VA rectified load is connected to the output of the dc-ac inverter. At this point an undershoot on the amplitude of the output voltage shape shows up. This undershoot is only about a 1 % of the steady-state amplitude value of the sinusoidal output voltage shape. Fig. VI.14(b) shows the steady-state output voltage and current shapes delivered by the inverter. The output current has a value of 19.24 A rms, with peaks reaching 49 A implying a crest factor of 2.55 under the overload condition. The output voltage shape presents some distortion, but the periodic disturbance capabilities of the AFC control loop are confirmed by the low $\text{THD}_{\text{v}}^{\text{rms}} < 2$ % observed in Fig. VI.13(d).

At $t = 13$ s the output power condition of the system is changed from 4425 VA down to 1032 VA. At this point an overshoot occurs at the output voltage amplitude of the dc-ac inverter. The amplitude of the overshoot is about a 10 % above the steady-state value of the nominal output voltage value. The AFC control loop is able to recover the amplitude and shape of the output voltage signal in approximately 0.8 s. At $t = 17$ s, all load is removed from the output of the dc-ac inverter. In this case, again an overshoot occurs on the amplitude of the output voltage shape. The overshoot reaches a 9.3 % above the steady-state value of the desired output voltage amplitude. The AFC control loop is able to recover the desired amplitude and shape of the output voltage in about 5 cycles.

Part 3

– Implementation Issues and Experimental Results –

chapter VII

Implementation Issues

No man's knowledge here can go beyond his experience.
John Locke

In this Chapter some details are given regarding the hardware/software implementation of the energy conditioning system. Some considerations have been taken regarding the signal acquisition and processing. The methodologies followed to implement the controllers designed and to generate the references used by these are explained.

When performing the hardware/software implementation of the energy conditioning some considerations have to be taken. Most of these considerations were considered before the construction of the experimental setup and some appeared by the time that the first experimentations were performed.

This Chapter is structured as follows: Section VII.1 gives a brief introduction of the hardware issues and considerations found during the implementation of the energy conditioning system. Section VII.1.1 explains the PWM scheme used, the signals involved in the modulation scheme and their implementation over the experimental setup. Section VII.1.2 presents the procedure followed to implement a rate of rise snubber on the main switch of the step-up converter due to the presence of unexpected high-frequency ringing between the drain and source terminals of the MOSFET. Section VII.1.3 describes a security module implemented to allow the safe use and storage of the bank of SCs. The procedure followed to implement a FC emulation system is described in Section VII.1.4. Section VII.2 gives an introduction to the software implementation issues solved. A general description of general implementation of the controllers and the periodic reference generation for the DT-AFC control scheme is presented in Section VII.2.1. The considerations to take in order to provide a good start-up sequence of the energy conditioning system is presented in Section VII.3. Finally, some images of the FC energy conditioning system are presented in Section VII.4

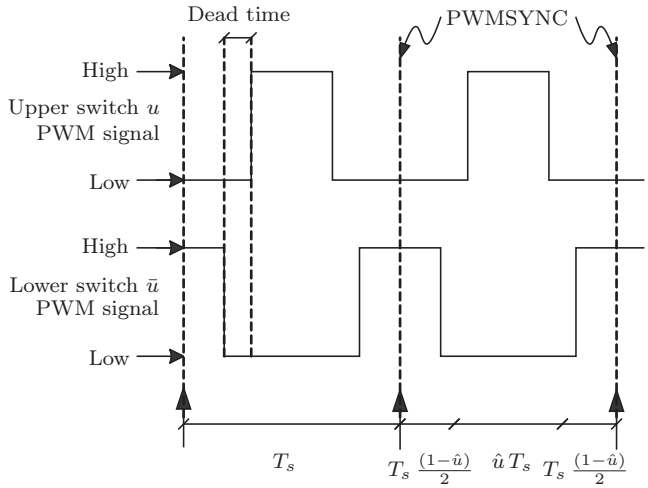


Figure VII.1: Complementary centered-pulse PWM signals.

VII.1 Hardware implementation issues

In this section a brief description of the general hardware considerations taken during the implementation of the energy conditioning system is given. These considerations include: the PWM scheme used, which is directly related to the software implementation; the implementation of a snubber circuit, which is connected in parallel to the switch of the step-up converter, necessary due to the coupling of parasitic capacitances/inductances in the physical system; a security module added to the bank of SCs used, this module protects the bank and the system connected to it in front of various hazardous situations; finally the implementation of the fuel-cell emulator used on the experimental tests is explained.

VII.1.1 Pulse-width modulation (PWM) scheme

As mentioned in previous chapters, all the power converters in this work operate by applying PWM over the controlled switches. A unified PWM scheme has been used on all the modules, this is the centered-pulse, single-update mode PWM. A switching frequency of $f_{sw} = 20$ kHz has been used. The PWM duty cycles, are fed to the PWM module provided by the digital signal processor used as computation device (ADSP21364 from Analog Devices). The use of this modulation scheme introduces a one switching cycle delay between the reception of the duty cycle command and its execution by the PWM module.

A general scheme of the PWM signals used is presented in Fig. VII.1. In this case two complementary PWM signals are presented. This scheme reflects the PWM configuration when driving a half-bridge switch module, as the ones used in the dc-ac inverter and for the APU dc-dc interfacing converter. In this case the duty cycle is denoted by $\hat{u}$ in Fig. VII.1, with $\hat{u} \in [0, 1]$. The value taken by $\hat{u}$ denotes the proportion of the switching period T_{sw} where the PWM signal of the upper switch is on its high level. In this work it is assumed that a high level on the PWM signal means that the switch driven by this signal is under conduction state and viceversa.

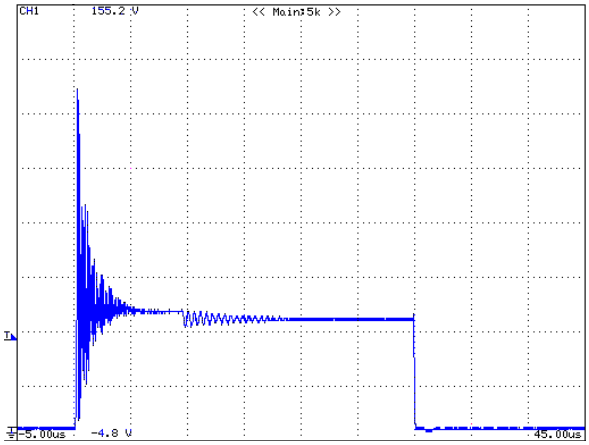


Figure VII.2: MOSFET V_{DS} High-frequency ringing.

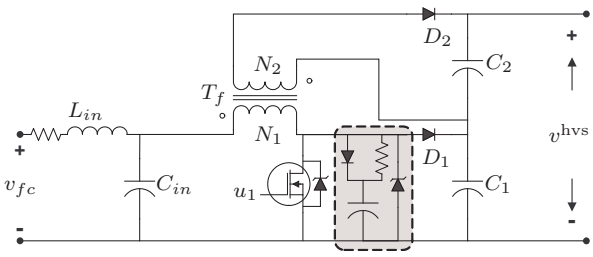


Figure VII.3: Step-up stage with the snubber circuit.

The PWM signals are complementary in order to avoid the simultaneous conduction of the upper and lower switches of the half-bridge module being driven. Simultaneous conduction of these two switches would mean a short circuit in the system. It has also to be taken into account that the the PWM signals drive physical switches, which present non ideal/instantaneous switching capabilities. In order to avoid the simultaneous conduction that could be caused by the response time of the switching devices, a dead time must be introduced between the two complementary PWM signals. A dead time of 2.5 μs has been used in the PWM signals driving the dc-ac inverter[1] and the APU dc-dc interfacing converter.

All the PWM signals are internally synchronized by the PWM module of the ADSP21464 microprocessor. An internal signal is generated in order to know the start/finish of the PWM periods. This signal is denoted by the PWMSYNC label in Fig. VII.1. This signal can be used to synchronize different events during the operation of the system as will be shown latter.

VII.1.2 Step-up converter RDC snubber

As mentioned in Section II.1.2, the switch used in the step-up stage is implemented by means of MOSFET devices. MOSFET switches usually have relatively large parasitic capacitance values between the drain and source terminals. This capacitance can resonate at turn off if connected to an unclamped inductance as pointed out by Mohan in [61] and Todd in [91]. Fig. VII.2 shows the drain to source (V_{DS}) voltage shape observed during the first experimentations over the step-up stage implementation. As it can be observed, the voltage present between the terminals of the switch resembles, somehow, the expected shape presented in Section II.1.2 (Figs. II.7, II.8, II.9 and II.10), but with a superimposed high-frequency ringing.

By making the converter to provide the desired output voltage level at full-load condition, the current flowing through the primary winding of the high-frequency transformer and the switch is about 60 A. At the turn off of the switch, the drain-to-source voltage grows quickly reaching a

[1]The negative effects of the inclusion of the dead time on the PWM scheme used to drive the full-bridge dc-ac inverter are compensated in part by the DT-AFC control scheme as pointed out in Section IV.3.3.

peak of about 300 V dc with a rise time of about 50 ns. After this first peak, the drain-to-source voltage starts to oscillate at a frequency near 6 MHz. The amplitude of the oscillation has a damped behavior reaching its steady-state value in about 10 μs.

For eliminating the high-frequency ringing present between the drain and source terminals of the switch, a rate of rise voltage snubber has been used. By following the procedure given by Todd in [91] a RCD turn-off snubber has been added in parallel to the switch, its purpose is to reduce the voltage ringing between the drain and source terminals of the MOSFET array. A 60EPU02 ultrafast soft recovery diode from IRF, a 16 Ω 20 W resistor and a 33 pF capacitor are used in the RCD snubber.

After adding the RCD rate of rise voltage snubber, the high-frequency ringing has been eliminated, but the first peak remains, mainly due to the response time of the diode used on the snubber. Once the voltage ringing has been eliminated, the second problem to solve is the peak drain to source voltage present when the switch turns off. As mentioned in Section II.1.2, the switch u_1 is implemented by using four IRFPS40N50L MOSFETs. These devices have a drain to source breakdown voltage of 500 V dc, and therefore, the peak drain to source voltage must be kept below this value.

For solving this, a 1.5KE250A Transil from STMicroelectronics has been used to avoid the existence of peak voltages above the 250 V dc. The transil is a voltage clamping device, acting as a high-power, high-voltage zener diode. Fig. VII.3 shows the final configuration of the step-up stage converter including the RCD snubber and the transil, which are inside the shaded part of the figure.

VII.1.3 Supercapacitor bank protection module

An additional circuitry has been added to the bank of SCs mainly due to safety concerns. The aim of the use of this additional circuitry is, in the first place, to protect the bank of SCs against over voltages, as SCs become easily damaged because of this reason. In the second place, as SCs can store a relatively large amount energy, the system connected to the bank must be somehow protected in order to avoid damage in case of unintended high-current situations. Additionally, a self-discharge mechanism has been implemented in order to deplete the energy stored in the bank of SCs if it is not in use.

The circuitry implemented monitors the voltage and current between the terminals of the bank of SCs. If the bank is in use, its voltage must remain lower than the absolute maximum voltage rating of 345 V dc, if for any reason the voltage goes above this level, the terminals of the bank of SCs are disconnected from the rest of the circuit, and the self-discharge process is started. Also, the operative range for the voltage of the SCs has been considered. As per the design considerations, the voltage in the bank moves within a range, which guarantees that a maximum of 85 % of the energy can be extracted from the bank when departing from full-charge condition. If the bank of SCs is providing energy to the system and the voltage at its terminals falls below a security level, it would imply an abnormal functioning of the circuit and then the bank of SCs is disconnected from the rest of the circuit.

An over current protection has been also implemented. As the bank of SCs can receive either positive or negative currents, the over current protection considers the absolute value of the current flowing from/towards the SCs. If the magnitude of the current through the SCs overpass the security level, also the bank is separated from the rest of the system and self discharged.

The self discharge is achieved by connecting a high-power resistor in parallel to the bank of SCs. This system is activated by either an abnormal situation or by switching off the box that contains the bank of SCs. In this way, the bank can be safely stored.

VII.1.4 Fuel-cell emulator

As mentioned in Section II.1.1, a Ballard MAN5100078 PEM type FC stack has been chosen as the nominal power source. The MAN5100078 has internal temperature, humidity, oxygen and hydrogen flux controls allowing the consideration of the device as a black-box power supply with some particular voltage/current characteristics. As the MAN5100078 FC unit takes care of all the non-electrical variables only the electrical characteristics of the MAN5100078 have been considered during the development of this work.

By the time that the tests over the experimental setup were performed, there was not available FC unit to be used, making it also necessary to implement a FC emulator in order to test the system under the characteristic voltage/current variations present when using these devices.

Analog programming implementation

The implementation of the FC emulator has been carried out by using a 6 kW SM 120-50 dc power source from Delta Elektronika and an ADuC812QS fixed-point microcontroller board from Analog Devices. The Delta STM-50 power supply can be controlled through an analog programming port. Also, the output current/voltage levels can be known by using the analog input/output port of the supply. The ADuC812QS board has built-in ADCs and DACs that allow the interfacing of the microcontroller with external devices.

The voltage vs current polarization curve of the MAN5100078 FC unit (see Fig. II.2) have been programmed in the microcontroller, the output current provided by the power supply is measured and according to the current demand, the output voltage command is set by programming a DAC which is connected to the analog programming port of the power supply. In order to take into account the response speed of the FC, the measured signals are filtered by using a discrete-time, low-pass filter with static a gain of 1 and with a cut-off frequency of 5 Hz.

A frequency of 100 Hz has been used for sampling the output current of the power supply and to deliver the output voltage command through the appropriate DAC channel.

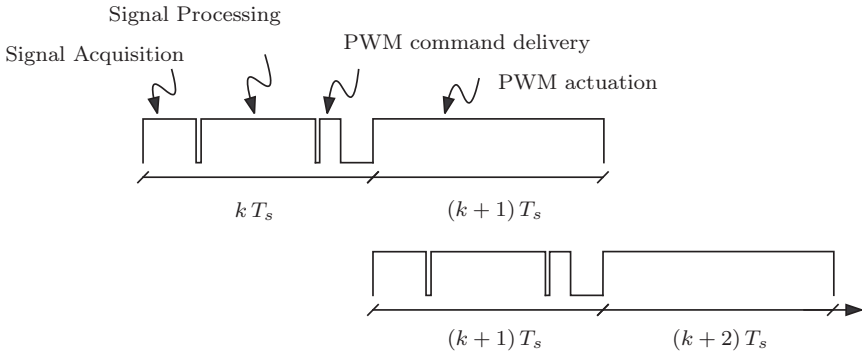


Figure VII.4: Acquisition, processing and delivery sequence of the measured and control signals.

VII.2 Software implementation issues

Regarding the software implementation there are various aspects to consider. In this work the PWMSYNC signal has been used to start the acquisition of the measured signals, and therefore the switching and the sampling frequency coincide having then $f_s = f_{sw} = 20$ kHz. Due to the hardware structure of the ADSP21364 and the PWM scheme used, a sequence of operation is defined. The main requirement is to deliver the kth PWM command before the $(k+1)$th switching cycle starts. As mentioned before, this sequence introduces a one switching cycle delay between the delivery of the PWM command and its execution by the PWM module of the microprocessor.

Fig. VII.4 shows a general diagram of the sequence to be followed for the computation of the control algorithm. At the beginning of the kth switching cycle, the PWMSYNC signal starts the acquisition process of the measured signals. This process lasts for some time, until all the measured variables have been acquired and stored in the memory of the microprocessor. Once the measurements are available, the computation of the controller can be started. In this case, all the control outputs are PWM duty cycles, which will drive the PWM module during the next switching cycle. Then, the obtained PWM duty cycles are fed to the PWM module of the ADSP21364. The execution of the desired PWM outputs take place in the $(k+1)$th switching cycle.

In parallel, the signal acquisition and computation of the control outputs for the $(k+1)$th switching period takes place. As it can be seen, there is a hard limitation on the time available for the delivery of the control outputs to the PWM module. All the signal acquisition and processing must be performed within the time frame of a switching period T_{sw}. In order so save processing time from the microprocessor, Direct Memory Access (DMA) has been used to obtain the measured signals from the ADCs. In this way, the processor can still be used for making calculations, while the ADCs fill up their data at the desired memory locations. Once all the data has been transferred to the memory, the completion of the task is notified to the processor by means of a software interruption.

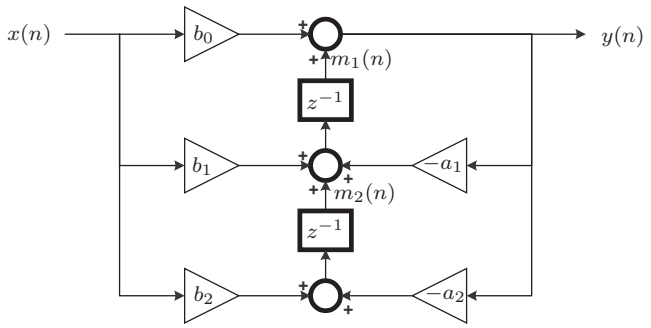


Figure VII.5: Second-order transposed direct form II implementation.

VII.2.1 Controllers implementation and periodic reference generation

Special care must be taken during the software implementation in order to provide of realizations of the controller and reference generation that allow the execution of the whole control algorithm within the time frame of a single switching cycle T_{sw}. It is well known that special functions like the trigonometric ones take a much longer processing time to provide a result than simpler operations like products and additions. It is also possible to achieve controller implementations which can be split in different parts, each these parts can be executed at convenient times by locating the appropriate sections of the code at the desired position within the overall code. In this section some of the considerations taken during the coding of the energy conditioning system are commented.

Transposed direct form II

The obtained discrete-time transfer functions of the controllers can be implemented in many different ways. In this work these have been implemented by using cascaded second-order modules of the form

$$\frac{Y(z)}{X(z)} = \frac{b_0 + b_1\, z^{-1} + b_2\, z^{-2}}{1 + a_1\, z^{-1} + a_2\, z^{-2}},$$

whose transposed direct form II implementation is depicted in Fig. VII.5. The dynamic behavior described by this transfer function can be rewritten by the difference equations set

$$\begin{aligned} y(n) &= b_0\, x(n) + m_1(n), \\ m_1(n) &= b_1\, x(n-1) - a_1\, y(n-1) + m_2(n-1), \\ m_2(n) &= b_2\, x(n-1) - a_2\, y(n-1). \end{aligned}$$

The different equations set described before, can be rewritten in an efficient programming C language code of the form presented in Listing VII.1

```
yn      =   b0*xn + m1n;
m1n     =   b1*xn - a1*yn + m2n;
m2n     =   b2*xn - a2*yn;
```

Listing VII.1: Sample C code for the implementation of a transposed direct form II second-order transfer function.

where the sequence given must be kept. This code can be split in two parts, the first one for the obtention of the control output yn, and the second one for the computation of the auxiliary variables m1n and m2n. As it can be seen, the control output is obtained by just performing one product and one addition while the computation of the auxiliary variables involves four products and three additions.

If the discrete-time transfer function to be implemented has an order $j > 2$, it can be rewritten to an equivalent second-order section representation in the form

$$\frac{Y(z)}{X(z)} = \frac{b_0 + b_1\, z^{-1} + ... + b_i\, z^{-i}}{1 + a_1\, z^{-1} + ... + a_j\, z^{-j}} = g \prod_{k=1}^{L} \frac{b_{0k} + b_{1k}\, z^{-1} + b_{2k}\, z^{-2}}{1 + a_{1k}\, z^{-1} + a_{2k}\, z^{-2}}.$$

If the transfer function has been split in three second-order sections, for example, the transposed direct form II code for such implementation takes the form presented in Listing VII.2

```
y1n     =   b01*xn  + m11n;
y2n     =   b02*y1n + m12n;
y3n     =   b03*y2n + m13n;
m11n    =   b11*xn  - a11*y1n + m21n;
m21n    =   b21*xn  - a21*y1n;
m12n    =   b12*y1n - a12*y2n + m22n;
m22n    =   b22*y1n - a22*y2n;
m13n    =   b13*y2n - a13*y3n + m23n;
m23n    =   b23*y2n - a23*y3n;
```

Listing VII.2: Sample C code for the implementation of three cascade transposed direct form II second-order sections.

In this case, three second-order blocks are cascaded. The input variable is xn, which is used to compute the output of the first second-order block y1n. The output of the first block is used as input for the second block and the same relationship is held between the second and the third blocks. The final output of this transfer function is y3n. The output of the total transfer function y3n is quickly obtained due to the low number and type of operations involved. As the output of the controller has been obtained rapidly, it can be fed to the PWM module before the next switching cycle starts. The computation of the auxiliary variables m11n, m12n, ..., m23n

can be carried out latter, with the only condition that these values must be available when the next iteration of the control algorithm occurs. The time dependency of the delayed terms is held by the order of the operations involved during the computation of the auxiliary variables, and therefore, it is important to maintain the computation sequence presented.

DT-AFC reference signals

The use of complex mathematical functions penalizes the execution time of the control algorithm. This is the reason why, it is necessary to use instructions as simple as possible in the software realization of the controllers. This fact has become evident during the implementation of the dc-ac inverter control. In this case, 120 different sinusoidal references need to be generated to be used by the DT-AFC control scheme. All these references share a common characteristic, they are all phase-shifted harmonics of the fundamental 50 Hz frequency. The first problem to be tackled is the generation of the fundamental 50 Hz reference to be used in output voltage reference of the dc-ac inversion stage. The second problem to be boarded is the generation of the remaining 29 harmonic frequencies in an efficient way. With this first 30 sinusoidal references in hand, various phase shifts must be implemented in order to feed the 4 carriers needed by each of the 30 $R_k(z)$ resonators (see Fig. IV.3). The online use of the trigonometric functions included in the mathematical library of the ADSP21364 is not feasible, as the computation time would increase beyond the allowed time frame of one switching cycle T_{sw}. Also, the use of a table stored in memory for each of the carriers is not viable, as the memory of the ADSP21364 module is limited.

Output voltage reference generation

The generation of the output voltage reference to be delivered to the controller of the dc-ac inverter, and the generation of the fundamental frequency to be used as carrier in the first resonator $R_1(z)$ is the same problem, the only difference is the amplitude of the signals, being 1 for the fundamental and $230\sqrt{2}$ for the output voltage reference. In this case a flexible enough system must be designed. The reference generation system must allow changes in the reference frequency in a relatively simple way. As will be seen in the Experimental Results Chapter, the system has been used to feed loads using ac voltages with frequencies different than 50 Hz, and therefore, online changes of the fundamental frequency and its harmonics must be allowed.

The fundamental frequency reference generation system has been implemented as follows: First, a 720 points vector (SinT[0..719]) has been filled up during the initialization of the energy conditioning control algorithm. This vector contains a complete cycle of the sinus function ($\sin(\theta)$ with $\theta = 0..2\,\pi$ rad) sampled with a $8.73 \cdot 10^{-3}$ rad (0.5 °) resolution. This vector has been filled up using the sinus function included in the mathematical library of the ADSP21364. The execution time of the control algorithm is not compromised during the initialization stage, as at this time the controllers are not running yet.

```
////////////////////////////////////////////////////////
// Reference angle generation functions
////////////////////////////////////////////////////////

static double   ykint       =   0.0;
static double   ukint       =   0.0;
static double   Angle_REF   =   0.0;
static int      REF_idx     =   0;

double Sinus_Int_Y(LongDub uk)
{
        ukint=uk;
        return(ykint);
}

void Sinus_Int_M(void)
{
        ykint+= ukint*Ts;

        if (ykint >= 2*3.14159265359) {
                    ykint -= 2*3.14159265359;
        }
}

////////////////////////////////////////////////////////
// Index generation (to be called every sampling period Ts)
////////////////////////////////////////////////////////

void sin_idx(void)
{
        Angle_REF       =   Sinus_Int_Y(2*3.14159265359*FREQ_REF);

        REF_idx         =   (int) (720*(Angle_REF/(2*3.14159265359))+0.5);

        if (REF_idx >= 720)
            {
                REF_idx = 0;
            };

        Sinus_Int_M(void);
}
```

Listing VII.3: Sample C code for the generation of a sinus function at the desired fundamental frequency.

After the initialization stage has been completed, and the control algorithm starts to work, the nth sample of the fundamental sinus signal, $\sin(\omega_1 T_s n)$ with $\omega_1 = 2\pi\,\text{FREQ\_REF}$, must be generated at the beginning of the nth switching cycle. As it has been mentioned before, the PWMSYNC signal has been used to start the acquisition of the measured signals, and therefore the sampling frequency coincides with the switching frequency $f_s = f_{sw} = 20$ kHz. For a desired fundamental frequency FREQ_REF, (f_s/FREQ_REF) points must be generated for each cycle of the output of the dc-ac inverter. For example, with the sampling frequency of $f_s = 20$ kHz, and a desired dc-ac inverter frequency of FREQ_REF = 50 Hz, then f_s/FREQ_REF = 20000/50 = 400 samples must be generated, and each sample must be generated every $T_s = 1/f_s$ seconds.

The sample C code for the generation of the fundamental frequency reference is presented in Listing VII.3. The desired fundamental frequency reference is obtained by reading the SinT

vector with the appropriate index increment every sampling period T_s. The index increment generated is based on the required angle increment of the $\sin(\theta)$ at the desired sampling frequency FREQ_REF. In order to go through $\theta = 0...2\,\pi$ rad at the desired FREQ_REF frequency, a $\Delta\theta$ increment of $2\,\pi * \text{FREQ\_REF} * T_s$ is required every sampling period T_s. The reference angle obtained after adding the increment is translated into an index to go through the SinT vector.

Carrier signals generation

By calling the `Sin_idx()` function presented in Listing VII.3 at the beginning of the nth switching period, the nth sample of the reference fundamental sinus can be obtained by retrieving the value `SinT[REF_idx]`. The nth sample of the $\cos(\omega_1\,T_s\,n)$ carrier can be obtained by reading the `SinT` vector with an index increment of a fourth of the length of the vector module the length of the vector. Therefore, $\cos(\omega_1\,T_s\,n)$=`SinT[(REF_idx+720/4)%720]`. Having now the $\sin(\omega_1\,T_s\,n)$ and $\cos(\omega_1\,T_s\,n)$ values, the nth sample of each of the higher harmonics can be computed in the form

$$\sin(\omega_k\,T_s\,n) = \sin(\omega_1\,T_s\,n)\,\cos(\omega_{k-1}\,T_s\,n) + \cos(\omega_1\,T_s\,n)\,\sin(\omega_{k-1}\,T_s\,n),$$
$$\cos(\omega_k\,T_s\,n) = \cos(\omega_1\,T_s\,n)\,\cos(\omega_{k-1}\,T_s\,n) - \sin(\omega_1\,T_s\,n)\,\sin(\omega_{k-1}\,T_s\,n),$$

with $\omega_k = k\,\omega_1$, $\omega_1 = 2\,\pi\,\text{FREQ\_REF}$ and $k = 2..30$. The values of $\sin(\omega_k\,T_s\,n)$ and $\cos(\omega_k\,T_s\,n)$ are stored then in a vector, which will be used latter to perform the appropriate phase shifts needed to obtain the remaining carrier signals.

The resonator structure $R_k(z)$ (see Fig. IV.3), includes the parameter φ_k, which is translated into a phase shift of the last two carriers used in the resonator structure. The nth sample of the shifted carriers for each of the resonators R_k can be obtained in the form

$$\sin(\omega_k\,T_s\,n + \varphi_k) = \sin(\omega_k\,T_s\,n)\,\cos(\varphi_k) + \cos(\omega_k\,T_s\,n)\,\sin(\varphi_k),$$
$$\cos(\omega_k\,T_s\,n + \varphi_k) = \cos(\omega_k\,T_s\,n)\,\cos(\varphi_k) - \sin(\omega_k\,T_s\,n)\,\sin(\varphi_k),$$

where the values of $\sin(\varphi_k)$ and $\cos(\varphi_k)$ have been also obtained and stored in vectors during the initialization stage of the energy conditioning control algorithm. With all the nth samples of the carriers in hand, the contribution of each resonator and the global contribution of the bank of resonators can be obtained. A sample C code of the implementation of the bank of resonators is presented in the Listing VII.4. It is assumed that the vector `PhiK` stores the phase shift parameters of the resonators φ_k, `ResGainK` the gains of the resonators g_k and u_k is the input signal to the bank of resonators, the error between the reference and the measured dc-ac inverter voltage. `REF_idx` is the index used to read the nth sample of the sinusoidal reference at the fundamental frequency.

```
static double  SinT         [720];

static double  SinPhiK      [30];
static double  CosPhiK      [30];

static double  ykSinCarr    [30];
static double  ykCosCarr    [30];

double  SinHarmKN           [30];
double  CosHarmKN           [30];
double  SinHarmKNPhiK       [30];
double  CosHarmKNPhiK       [30];

////////////////////////////////////////////////////////
// Initialization of the bank of resonators variables
////////////////////////////////////////////////////////
void Resn_Ini(void)
{   int i;
        for (i=0; i<30; i++) {
                SinPhiK[i]    =   sin(PhiK[i]);
                CosPhiK[i]    =   cos(PhiK[i]);

                ykSinCarr[i]  =   0.0;
                ykCosCarr[i]  =   0.0;
        }

        for (i=0; i<720; i++) {
                SinT[i]       =   sin((2*3.14159265359/720)*i);
        }
}

////////////////////////////////////////////////////////
// Bank of resonators response
// (to be called every sampling period Ts)
////////////////////////////////////////////////////////
double Resn_Cont(double uk)
{
  int i;
  double SinFundN;
  double CosFundN;
  double sum=0.0;

  SinFundN=sinT[REF_idx];
  CosFundN=sinT[(int)((REF_idx + 720/4))%720];

  SinHarmKN[0] = SinFundN;
  CosHarmKN[0] = CosFundN;

  for (i=1; i<30; i++) {
     SinHarmKN[i]= SinFundN*CosHarmKN[i-1] + CosFundN*SinHarmKN[i-1];
     CosHarmKN[i]= CosFundN*CosHarmKN[i-1] - SinFundN*SinHarmKN[i-1];
  }

  for (i=0; i<30; i++) {
     SinHarmKNPhiK[i] = SinHarmKN[i]*CosPhiK[i] + CosHarmKN[i]*SinPhiK[i];
     CosHarmKNPhiK[i] = CosHarmKN[i]*CosPhiK[i] - SinHarmKN[i]*SinPhiK[i];
  }

  for (i=0; i<30; i++) {
     ykSinCarr[i] +=  uk * SinHarmKNPhiK[i];
     ykCosCarr[i] +=  uk * CosHarmKNPhiK[i];
     sum+=(ykSinCarr[i]*SinHarmKN[i] + ykCosCarr[i]*CosHarmKN[i])*ResGainK[i];
  }

   return(sum);
}
```

Listing VII.4: Sample C code for the implementation of the bank of resonators for the DT-AFC control scheme.

The sample C code implementation shown in Listing VII.4 presents an efficient methodology to perform the realization of the bank of resonators to be used in the DT-AFC control loop. The nth sample of each of the 140 references needed are generated in real-time operation of the control algorithm. The avoidance on the direct use of the trigonometric function implementations included in the mathematical libraries of the ADSP21364 processor saves execution time, allowing the control algorithm of the energy conditioning system to run within the one switching cycle time frame T_s. The online dynamic generation of the carrier samples, saves memory evading the need of the use of large tables stored in memory.

VII.3 Conditioning system start-up sequence

Care must be taken in the way used to start the operation of the system. Many things must be considered in order to obtain an adequate system start-up process, among them are: the initial switch positions, initial voltage and current levels of the power supply and/or the energy storing devices connected to the system, the appropriate sequence in which the conversion modules must be started, the references delivered to the different control loops, etc.

The first consideration that can be made is the order in which the operation of the different conversion modules is started. It is clear that for this system, first, the dc-bus voltage v_{bus} must have reached its steady-state value before the rest of the systems begin to operate. It is important to consider the initial conditions and switch position of the step-up converter at the time that the system is about to start to work. When in idle state, the switch of the step-up converter must not be under conduction state. This initial non-conduction state is forced by adequately adjusting the initial positions of the PWM pins at the processor. The PWM module must start to provide a valid output only at the time that the control algorithm is providing a valid output.

Regarding the software implementation, the references given to the controllers of the different conversion stages must be coherent with the desired and allowed initial operational stages of the energy conversion system. In the case of the step-up control, the dc-bus voltage must gradually grow from the initial output voltage of the converter in idle state to the desired voltage at the dc bus. Once this state has been achieved, the start-up of the following conversion modules can be started. In this case, the next module to be started is the dc-dc interfacing converter used on the APU.

At the time the APU is started to work, the bank of SCs must be discharged. The presence of a non-zero voltage at the SCs could lead to undesired peak currents, putting in risk the integrity of the physical components. As the bank of SCs is depleted at this time, the initial configuration of the switches for this conversion stage is to have the lower switch of the half-bridge module under conduction state, in parallel to the bank of SCs and the inductance of the converter L_{apu}, having then, the higher switch open. The inverse initial positions of the switches (higher switch under conduction state and the lower switch open) would directly connect the dc bus with the bank of SCs, making it appear as a short circuit to the step-up stage. The natural conduction of the anti-parallel diode of the higher switch of the half-bridge module would cause the direct connection between the dc bus and the bank of SCs if a non-zero voltage is present at the SCs.

With the initial switch positions for the APU and the SCs discharged, the initial charge of the bank of SCs can be started. A small current is commanded to the SCs current control loop in order to start the charge process. This current command is gradually increased until the maximum allowed charge current is obtained. The charge current command must be held until the bank of SCs is completely charged, and then, the next stage on the start-up process of the system can be started.

After the full charge of the SCs has been achieved, the energy conditioning system is fully operative at the dc side. The only remaining task is to start the functioning of the dc-ac inverter. Up to now, the switches of the full-bridge dc-ac inverter have been kept with the lower switches of each leg under conduction state. This fact implies that the higher switches of the full-bridge inverter are open. With this configuration of the switches, even under the presence of a load connected to the output of the dc-ac inverter, the dc side of the system sees no load, and then the start-up process is performed as if the system were under no load condition. At the time that the inverter must start to work, a null dc-ac inverter output voltage reference delivered. The amplitude of the output voltage reference is gradually increased until it reaches the desired $230\sqrt{2}$ level. At this point the start-up process finishes and the energy conditioning system is fully operative.

VII.4 Implementation images

Fig. VII.6 shows a general view of the setup used in the experimentations of the energy conditioning system. A DL9040 and two DL1640 oscilloscopes from Yokogawa have been used as the data acquisition devices. A Fluke 43 power quality analyzer has been used to evaluate the quality of service of the output of the dc-ac inversion module. Various Fluke 179 multimeters have been used to monitor de dc-bus voltage, temperature of the semiconductor devices, voltage at the SCs, etc.

At the left of Fig. VII.6 the SM 120-50 power supply from Delta Elektronika and the ADuC812QS microcontroller module used to implement the fuel-cell emulator are displayed. At the center up, the module which contains the bank of SCs is presented. At its right, the oscilloscopes used to acquire the voltage and current shapes of the converters. The power converters are shown at the center down of Fig. VII.6. Finally, at the right, the computing and sensing units are highlighted.

A more detailed view of each of the modules used on the implementation of the energy conditioning system is presented in Fig. VII.7. Fig. VII.7(a) shows a closer look of the implementation of the power converters. The high-frequency transformer, switch, output diodes and capacitors of the step-up stage are identifiable. Fig. VII.7(b) shows a different angle of the power converters view. In this case, the dc-bus and step-up stage capacitors can be seen. The switch drivers board and the computing and sensing units appear at the right of the image.

An upper view of the SCs module with the case open can be seen in Fig. VII.7(c). The upper half of the image contains the bank of SCs implemented by means of a series connection of 23, 58 F 15 V dc, BPAK0350-15EA SC packs from Maxwell. The lower half of the image shows the security circuitry implemented and described in Section VII.1.3.

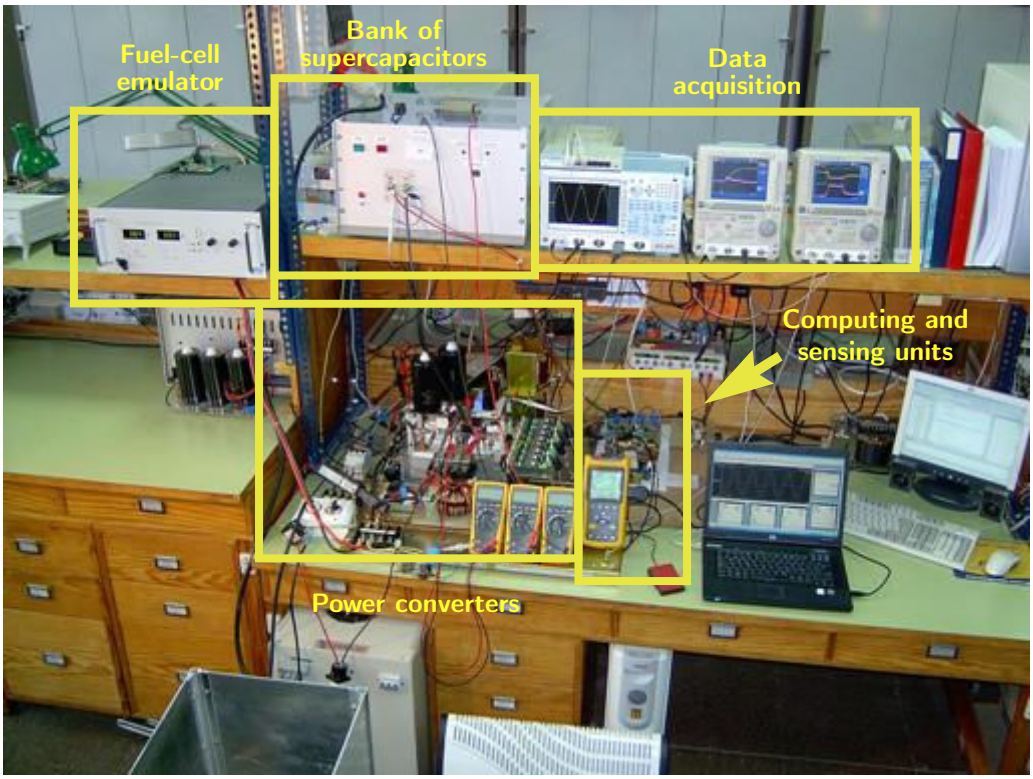
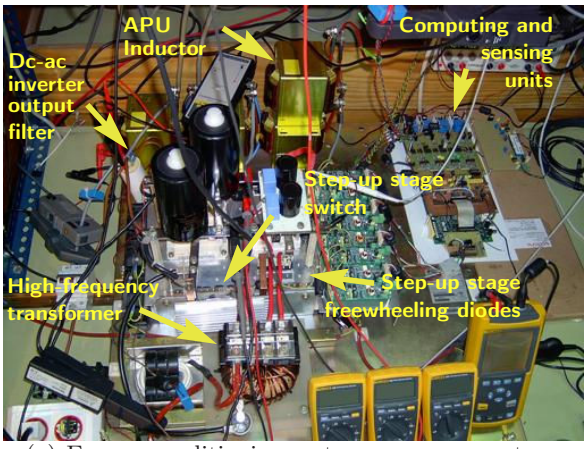


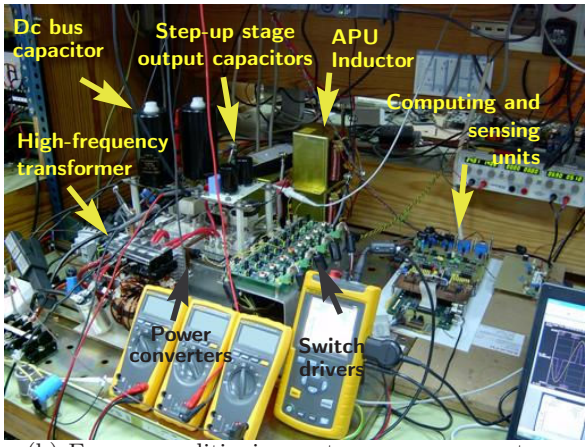
Figure VII.6: Experimental setup general view.

Fig. VII.7(d) shows a closer look of the computing and sensing units used. These are composed by four modules, identified by the (1), (2), (3) and (4) labels. The label (1) denotes the Analog Devices ADSP21364 EZ kit lite starter kit module used as computing device. Label (2) identifies the ADCs module built by using two MAX1324ECM, 8 channel simultaneous sampling analog to digital converters from Maxim used to interface the analog signals obtained from the sensors with the ADSP21364. An analog filters module has been implemented and shown by the (3) label in the figure. This module has been implemented using differential low-pass filters used to remove the high frequency noise of the acquired signals. Finally, the label (4) identifies the main sensors module, an auxiliary module is also used and seen at the right of Fig. VII.7(b).

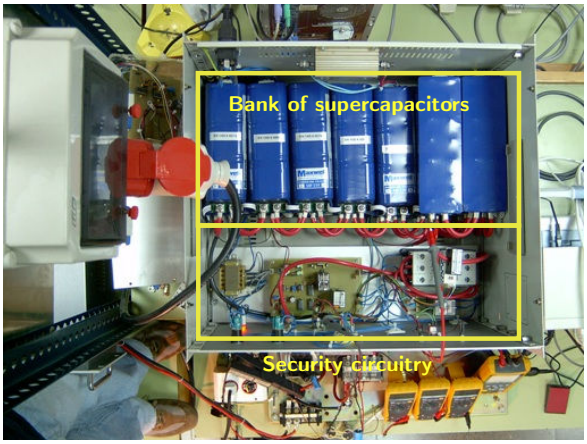
Some images regarding the constructive process of the high-frequency transformer, which has been designed and built for the project, are presented in Fig. VII.7(e). The transformer is formed by two 20 turns coils connected in parallel for the primary winding and one 136 turns coil for the secondary winding. A T400-60D iron powder core from Micrometals has been used. This core has an inner diameter of 102 mm and an external diameter of 57.2 mm. The final configuration of the transformer, including the coils, has an external diameter of 132 mm. Finally Fig. VII.7(f) shows a closer look of the fuel-cell emulator. The ADuC812QS microcontroller module can be seen at the top of the SM 120-50 power supply.



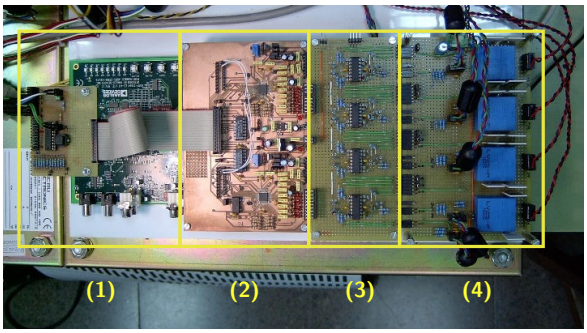
(a) Energy conditioning system power converters.



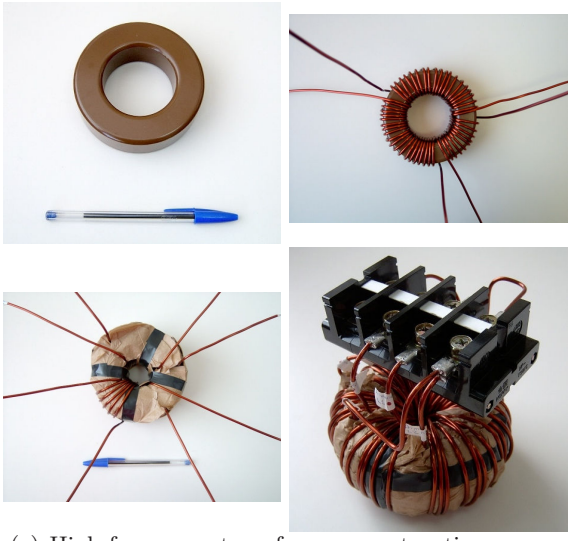
(b) Energy conditioning system power converters.



(c) Bank of supercapacitors.



(d) Computing and sensing devices.



(e) High-frequency transformer constructive process.

(f) Fuel-cell emulator.

Figure VII.7: Energy conditioning system hardware implementation.

chapter VIII

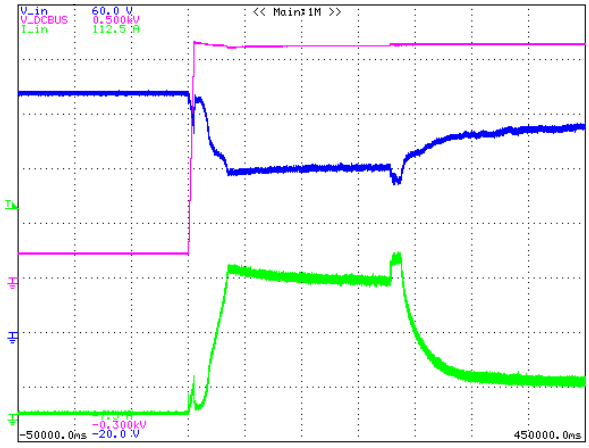
Experimental Results

La paciencia es la madre de la ciencia
(patience is the mother of science)
–unknown

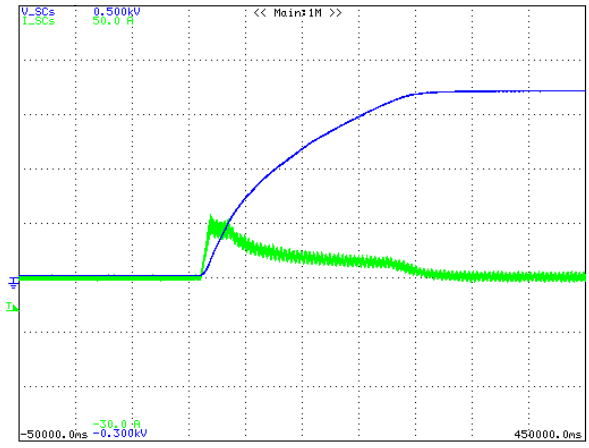
This Chapter presents the results obtained from the tests performed over the experimental setup. The performance and functioning of each of the modules that compose the energy conditioning system is analyzed under each test. The response of the energy conditioning system has been evaluated under nominal and overload conditions by performing step load changes using linear and/or nonlinear loads.

A set of tests has been performed over the experimental setup. The main power source used is a FC emulator implemented as described in Section VII.1.4. As mentioned before, the FC emulator provides a current/voltage behavior that resembles the behavior that can be found in the electrical variables of a FC unit. This fact emphasizes the black-box consideration of the FC unit mentioned in Section II.1.1. The tests comprise the linear and nonlinear loads cases connected at the output of the dc-ac inversion stage. For the linear load case, resistive loads have been used. For the nonlinear load case a full-bridge diode rectifier, with a C filter and a resistive load (see Fig. IV.1) has been used. Additionally, a set of tests has been performed using ac induction machines. These last have been performed to test the motor start-up capabilities of the energy conditioning system.

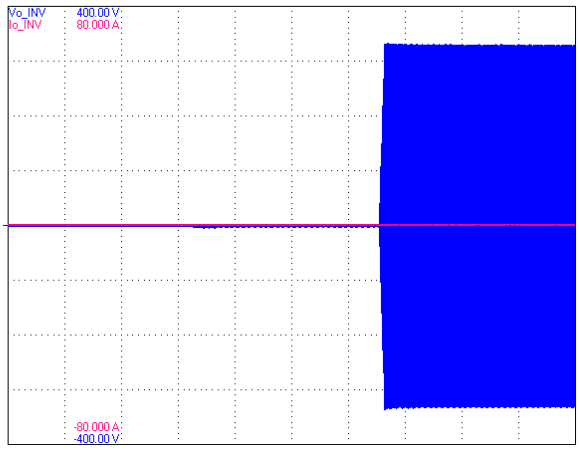
The start-up process of the energy conditioning system is presented in Section VIII.1. Various sets of tests have been performed over the experimental setup. The steady-state behavior and the system response in front of resistive load changes is presented in Section VIII.2. The experimental results when feeding nonlinear loads are presented in Section VIII.3. The response of the system while feeding dynamic loads has been also evaluated and presented in Section VIII.4. The dc-ac inversion stage along with the DT-AFC control has been used to feed a load that presents complex dynamic behavior while generating ac output voltages at 48, 50 and 52 Hz. The experimental results obtained during these tests are presented in Section VIII.5.



(a) Step-up stage input and output voltages and input current. (Scales: $v_{fc} = 10$ V/div, $v_{bus} = 100$ V/div, $i_{fc} = 15$ A/div).



(b) APU, SCs voltage and current. (Scales: $v_{sc} = 100$ V/div, $i_{sc} = 10$ A/div).



(c) Dc-ac inversion stage, output voltage and current. (Scales: $v_o = 100$ V/div, $i_o = 20$ A/div).

Figure VIII.1: Energy conditioning system start-up. (Time scale: 50 s/div).

VIII.1 System start-up

As described in Section VII.3, care must be taken in order to assure a correct start-up process of the energy conditioning system. Fig. VIII.1 shows the start-up sequence followed to bring of the energy conditioning system to the operative condition. Fig. VIII.1(a) shows the behavior of the step-up stage. The blue trace shows the voltage and the green trace shows the current present at the input terminals of the step-up conversion stage (provided by the FC emulator); the pink trace shows the output voltage present at the high-voltage side of the converter ($v^{\text{hvs}} = v_{bus}$). Fig. VIII.1(b) shows the behavior of the APU stage. The green and blue traces show the current and voltage present at the terminals of the bank of SCs, respectively. Fig. VIII.1(c) shows the behavior of the dc-ac inversion stage. The blue and pink traces show the output voltage and current, respectively. The process shown in Fig. VIII.1 occurs with no load connected at the output of the dc-ac inversion stage.

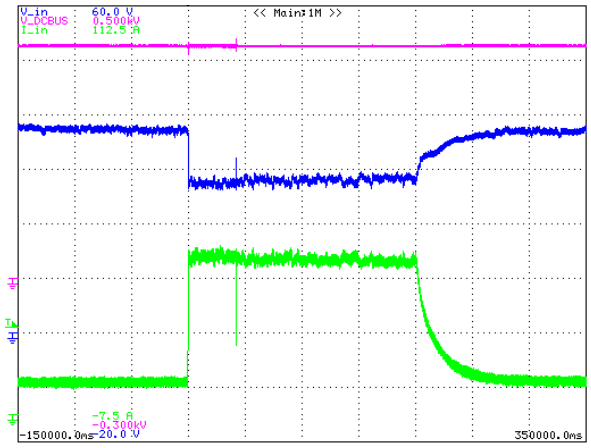
The sequence of Fig. VIII.1 is completed in about 3.5 min from idle to full-operative condition. All the inner control schemes are initialized with zero references (zero current reference for the step-up control, zero output voltage reference for the dc-ac inversion control and zero current reference for the SCs current control). These zero current references for the APU and the step-up stages are generated by the global power balance control (GPC) loop.

As mentioned in Section VII.3, some considerations must be taken to account for the initial conditions of the system in order to allow the GPC loop to provide the appropriate current references under these circumstances. When departing from idle state, due to the natural conduction of diode D_1 of the step-up converter (Fig.II.6) the voltage at the high voltage side is equal to the input voltage v_{fc}. The global power balance control receives a v_{bus}^{ref} ramp reference, departing from $v_{bus}^{\text{ref}} = v_{fc} + 5$ to start the boosting of the input voltage, up to $v_{bus}^{\text{ref}} = 425$. This fact can be observed in Fig. VIII.1(a), by the sharp slope shown by the pink trace from 150 s to 155 s when the output voltage reaches its maximum level. After this point, the value of the voltage reference given to the GPC loop is held constant at $v_{bus}^{\text{ref}} = 425$.

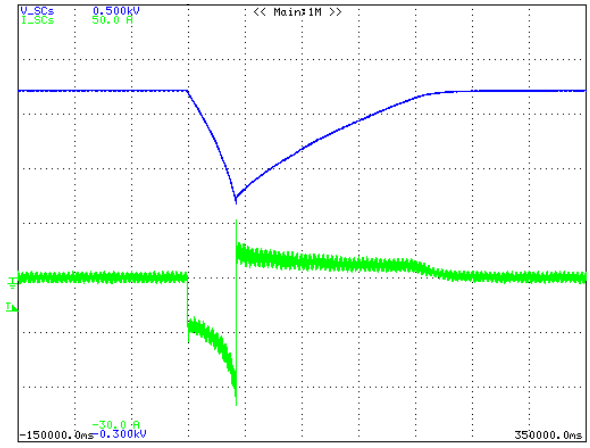
With the step-up stage working and providing the desired $v_{bus} = 425$ V dc level, now the functioning of the other modules can be started. At the beginning, as it can be observed in Fig. VIII.1(b), the bank of SCs is completely depleted, and therefore a $v_{sc} \approx 0$ V dc voltage measurement is expected. As the APU current reference is obtained by dividing the APU power reference by the SCs voltage measurement (as shown in Fig. VI.10), this can lead to very high current references for the SCs current control loop. In order to avoid this situation, a *dummy* measurement is forced, and an initial $v_{sc} = 30$ V dc measurement is seen by the GPC loop. The GPC loop generates then an input current reference i_{sc}^{ref} according to the available power that can be extracted from the FC and the *dummy* v_{sc} measurement. The reference value delivered to the SCs current control loop is set to $i_{sc}^{\text{ref}} = 0$ by using a scaling factor. Then, this scaling factor is increased in a linear way, from 0 to 1 in 25 s, in order to allow the SCs control loop to receive the whole current reference generated by the GPC loop. The *dummy* measurement value is replaced by the actual v_{sc} measurement once $v_{sc} \geq 30$.

The influence of the *dummy* measurement can be observed in Fig. VIII.1(b). A delay of 5 s has been left after the step-up stage has reached its desired output voltage value before the charging process of the bank of SCs starts. The current injected to the SCs grows rapidly for some seconds, until $v_{sc} \geq 30$. After this point, the SCs are charged using the allocated power level, in this case PWR_APU_CHRG_MAX= 850 W and the voltage present at the bank of SCs v_{sc} along with the scaling factor.

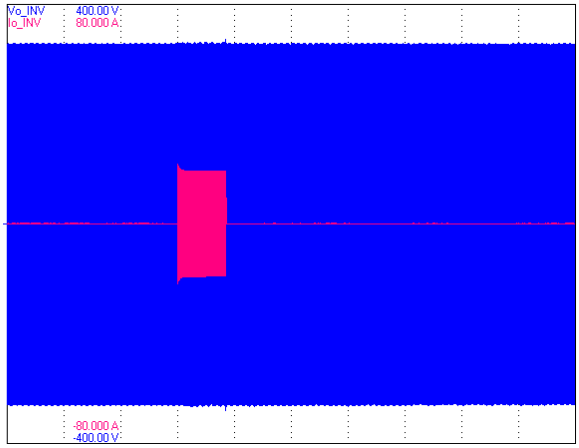
The bank of SCs is fully charged in about 3 min. After the maximum allowed value for v_{sc} voltage has been reached, the current reference to the SCs current control is set to $i_{sc}^{\text{ref}} \approx 0$, having only a dc component in order to compensate the self discharge of the bank of SCs. Once the bank of SCs is fully charged, the operation of the dc-ac inverter is started. During the whole start-up process, the dc-ac inverter controller has been working with a $v_o^{\text{ref}} = 0$ reference. In fact, the sinusoidal reference for the output voltage is generated during the process, but again, a scaling factor is used to set the reference value to zero. The scaling factor for the amplitude of the sinusoidal output voltage reference is increased from 0 to 1 in 5 s. After this, the energy conditioning system has reached the fully operative state.



(a) Step-up stage input and output voltages and input current. (Scales: $v_{fc} = 10$ V/div, $v_{bus} = 100$ V/div, $i_{fc} = 15$ A/div).



(b) APU, SCs voltage and current. (Scales: $v_{sc} = 100$ V/div, $i_{sc} = 10$ A/div).



(c) Dc-ac inversion stage, output voltage and current. (Scales: $v_o = 100$ V/div, $i_o = 20$ A/div).

Figure VIII.2: Linear load changes. From no load to overload condition to no load. (Time scale: 50 s/div).

VIII.2 Linear load change tests

In order to test the functioning of the energy conditioning system, load change tests have been performed. Two set of tests have been carried out for the case of linear loads. In the first, a change has been performed from the system working with no load to overload condition and then back to empty load. In the second test, the system is initially feeding a resistive load within the 1 kW nominal limit, then a load change to full-overload condition is performed and after the system is returned to its initial load condition. The tests performed show complete discharge/charge cycles of the bank of SCs to supply the power demanded by the overload. The performance of all the modules can then be analyzed during the transients caused by the load level variations, and also after the steady-state regime has been reached by the system.

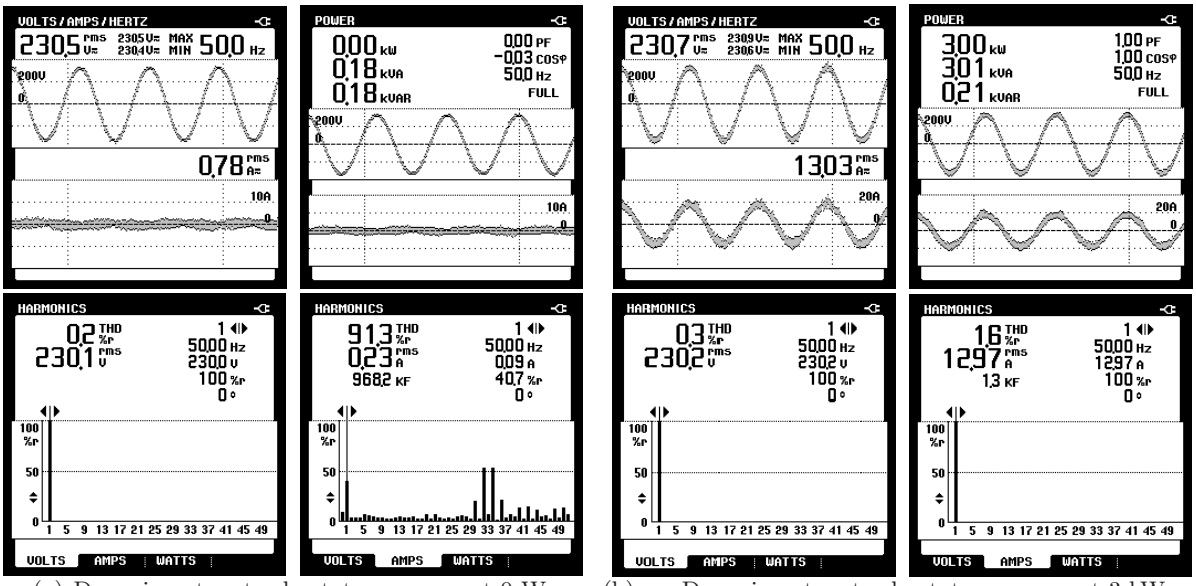
VIII.2.1 No load to overload condition to no load

In this test, the system has been brought to steady state while having no load connected at the output terminals of the dc-ac inverter. At $t = 150$ s a 3 kW resistive load is connected to the dc-ac inverter. In terms of linear load change, this test constitutes the worst case scenario because the system is suddenly forced to work at maximum power, departing from an empty-load condition.

Fig. VIII.2 shows the energy conditioning system response to the resistive load change. Fig. VIII.2(a) shows the response of the step-up stage. From $t = 0$ s to $t = 150$ s, the system is not feeding any ac load, and the input voltage (blue trace) is $v_{fc} = 37.3$ V dc, with an input current (green trace) of $i_{fc} = 8.95$ A dc. From this values it can be determined that $p_{fc} = v_{fc}\, i_{fc} \approx 334$ W are demanded to the FC in idle state to supply the switching and parasitic losses of the system. At $t = 150$ s a 3 kW resistive load is connected to the conditioning system. As it can be seen in Fig. VIII.2(a) an abrupt change in the input current and voltage appears in order to supply the output at full-load condition. The input voltage falls down to $v_{fc} = 27.41$ V dc and the input current grows up to $i_{fc} = 43.4$ A dc implying that about $p_{fc} = 1189$ W are being demanded from the FC unit. This maximum power coincides with the parameter PWR_STP_MAX of the global power control presented in Fig VI.10, that in this case has been set to PWR_STP_MAX= 1200 W. The difference between the PWR_STP_MAX limit and the experimental 1189 W level observed, is explained by the error in the sensing of the signals, which could be caused aliasing of the measured signals, thermal drift of the components, calibration, etc.

At $t = 150$ s a v_{bus} voltage undershoot occurs. The voltage decreases to $v_{bus} = 410.8$ V dc, being quickly recovered by the combined action of the step-up and APU stages. This voltage drop can be translated into a 3.64 % undershoot below the steady-state dc-bus voltage value. The overload condition is hold for about 43 s. After this time, the system is returned to its initial no-load condition. At the moment that the overload is removed an overshoot presents in the voltage of the dc bus. The voltage grows up to 438.6 V dc which means a 2.88 % overshoot over the steady-state voltage value of v_{bus}. After the 3 kW load has been removed, the step-up stage maintains the full-load condition power demand from the FC in order to be able to recharge the bank of SCs which has been depleted. After the SCs reach their maximum allowed operative voltage the GPC removes the SCs charge current command, making the step-up stage return to its initial condition.

Fig. VIII.2(b) shows the voltage (blue trace) and current (green trace) present at the bank of SCs during the test. From $t = 0$ s to $t = 150$ s, a small average current of $i_{sc} \approx 50$ mA is injected to the SCs in order to maintain the full-charge condition of the bank. During this period, the bank of SCs has a voltage of $v_{sc} = 343.88$ V dc. The small current being injected means that $p_{sc} = v_{sc}\, i_{sc} \approx 17$ W are demanded from the system in order to compensate the self discharge of the bank of SCs. At $t = 150$ s the 3 kW load is connected. At this point, around 2.8 kW are extracted from the bank of SCs during the presence of the overload condition. By considering the efficiencies of the conversion stages in the path, only about 2 kW to 2.1 kW reach the load, allowing the functioning of the energy conditioning system. After the load is removed, the voltage of the SCs starts to increase, recovering its full charge state in approximately 2.5 min.



(a) Dc-ac inverter steady-state response at 0 W. (b) Dc-ac inverter steady-state response at 3 kW feeding a resistive load.

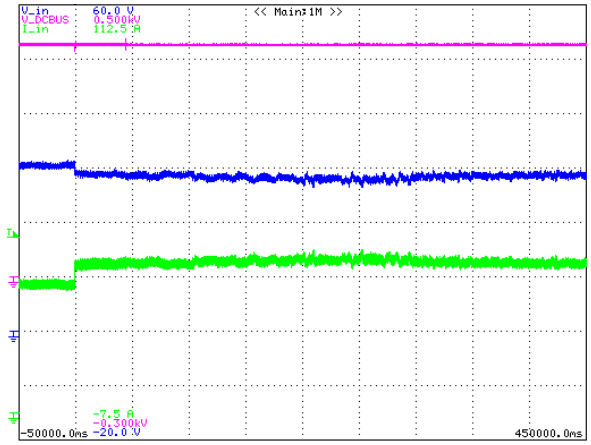
Figure VIII.3: Linear load changes. Dc-ac inverter steady-state responses.

After this point the APU returns to its initial state, and only a small current is injected in order to maintain the state of charge of the bank of SCs.

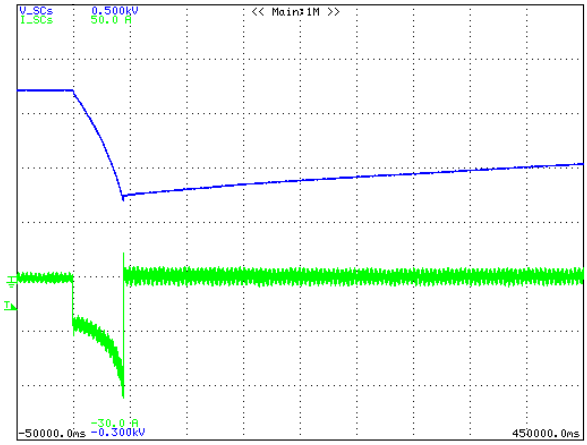
Fig. VIII.2(b) shows that a total voltage drop of $\Delta\, v_{sc} \approx 209$ V dc presents at the bank of SCs during the overload condition. Before the overload condition, the bank presents a voltage of $v_{sc} = 343.88$ V dc, value that falls down to $v_{sc} = 135.35$ V dc just before the overload is removed. This fact implies that an 84.5 % of the initial energy has been extracted from the bank of SCs to supply the energy needed by the overload. Therefore, the dc-dc APU interfacing converter is forced to provide a maximum conversion ratio of 3.14 when the minimum voltage is present at the bank of SCs.

Fig. VIII.2(c) shows the voltage and current delivered at the output of the full-bridge dc-ac inverter. No overshoot is noticeable in the shape of the output voltage when the load is connected or disconnected. The high quality of the ac voltage under, either, the empty load or the overload cases can be observed in Fig. VIII.3. Fig. VIII.3(a) shows the steady-state behavior of the full-bridge dc-ac inverter while no load is connected at its terminals. The low $\mathrm{THD}_{\mathrm{v}}^{\mathrm{rms}} = 0.2$ % achieved is a good indicator of the performance of the DT-AFC control scheme (presented in Chapter IV) used on the dc-ac inversion stage.

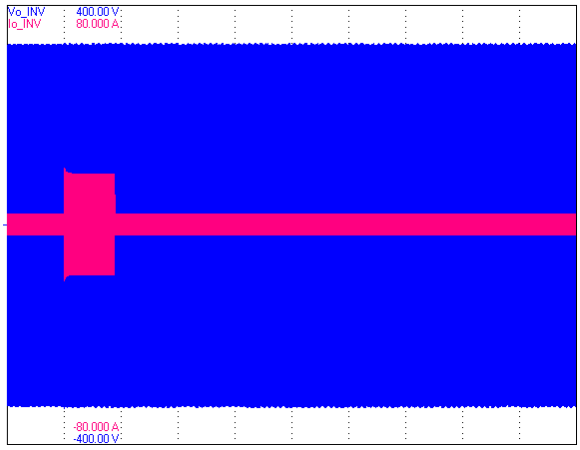
Fig. VIII.3(b) shows the steady-state response of the dc-ac inversion stage under the full-overload condition while feeding the 3 kW resistive load. As it can be noticed, in this case a $\mathrm{THD}_{\mathrm{v}}^{\mathrm{rms}} = 0.3$ % is achieved, confirming the good sinusoidal shape of the output voltage. As this test has been performed using a resistive load, only the 50 Hz component of the output voltage and current is noticeable, with no evident contribution of the higher harmonics in both cases.



(a) Step-up stage input and output voltages and input current. (Scales: $v_{fc} = 10$ V/div, $v_{bus} = 100$ V/div, $i_{fc} = 15$ A/div).



(b) APU, SCs voltage and current. (Scales: $v_{sc} = 100$ V/div, $i_{sc} = 10$ A/div).



(c) Dc-ac inversion stage, output voltage and current. (Scales: $v_o = 100$ V/div, $i_o = 20$ A/div).

Figure VIII.4: Linear load changes. From 570 W to overload condition and back to 570 W. (Time scale: 50 s/div)

VIII.2.2 Small load to overload condition to small load

In this case the system has been driven to steady state while feeding a resistive load of 570 W. At $t = 50$ s a total resistive load of 2.89 kW is connected to the terminals of the dc-ac inverter. The overload condition is hold until the bank of SCs is depleted, and after, the system is returned to feed the 570 W resistive load.

Fig. VIII.4 shows the response of the energy conditioning system during the test. Fig. VIII.4(a) shows the response of the step-up stage. From $t = 0$ s to $t = 50$ s, the system is feeding the resistive 570 W load at the output of the dc-ac inverter. The input voltage (blue trace) is

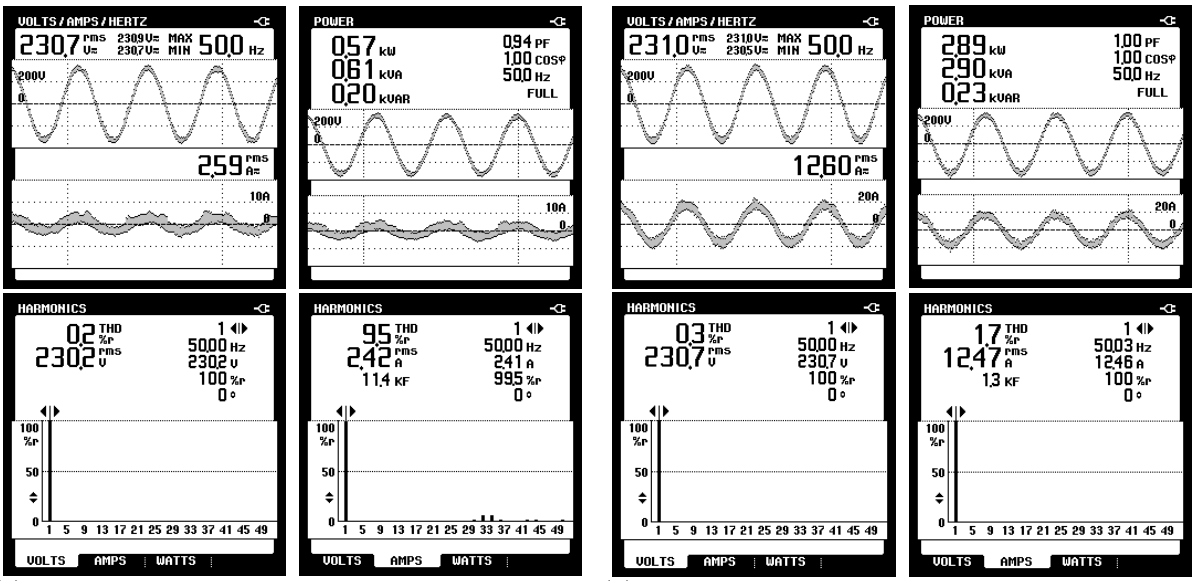
$v_{fc} = 30.46$ V dc, with an input current (green trace) of $i_{fc} = 35.41$ A dc. From this values it can be determined that $p_{fc} = v_{fc}\, i_{fc} \approx 1079$ W are demanded to the FC. At $t = 50$ s the 2.89 kW resistive load is connected to the conditioning system. As it can be seen in Fig. VIII.4(a) a change in the input current and voltage appears in order to supply the output at full-load condition. The input voltage decreases to $v_{fc} = 28.83$ V dc and the input current grows up to $i_{fc} = 40.91$ A dc implying that about $p_{fc} = 1179$ W are being demanded from the FC unit. This maximum power limit is set by the parameter PWR_STP_MAX of the global power control presented in Fig VI.10.

At $t = 50$ s a v_{bus} voltage undershoot occurs. The v_{bus} voltage drops down to 413.31 V dc, being quickly recovered by the combined action of the step-up and APU stages. This voltage drop can be translated into a 3.12 % undershoot below the steady-state dc-bus voltage value. The overload condition is hold for about 44.5 s. After this time, the system is returned to its initial 570 W load condition. At this point, an overshoot presents in the voltage of the dc bus. The voltage grows up to 437 V dc which means a 2.44 % overshoot over the steady-state voltage value of v_{bus}. After the 2.89 kW load has been removed, the step-up stage maintains the full-load condition power demand from the FC in order to be able to feed the 570 W load, and use the remaining power that can be extracted from the FC to recharge the bank of SCs which has been depleted. After the SCs reach their maximum allowed operative voltage the GPC removes the SCs charge current command, making the step-up stage return to its initial condition.

Fig. VIII.4(b) shows the voltage (blue trace) and current (green trace) present at the bank of SCs during the test. From $t = 0$ s to $t = 50$ s, only a small current is injected to the SCs in order to maintain the full-charge condition of the bank. During this period, the bank of SCs has a voltage of $v_{sc} = 343.88$ V dc. At $t = 50$ s the 3 kW load is connected. At this point, around 2.76 kW are extracted from the bank of SCs during the presence of the overload condition. By considering the efficiencies of the conversion stages in the path, only about 2 kW reach the load, allowing the functioning of the energy conditioning system. After the load is removed, the system keeps feeding the 570 W load, and the rest of the energy of the FC is used to recharge the bank of SCs. The voltage of the SCs starts to increase, recovering its full charge state in approximately 25 min. After this point the APU returns to its initial state, and only a small current is injected in order to maintain the state of charge of the bank of SCs.

Fig. VIII.4(b) shows that a total voltage drop of $\Delta\, v_{sc} \approx 205$ V dc presents at the bank of SCs during the overload condition. Before the overload condition, the bank presents a voltage of $v_{sc} = 343.75$ V dc, value that falls down to $v_{sc} = 138.48$ V dc just before the overload is removed. This fact implies that an 83.8 % of the initial energy has been extracted from the bank of SCs to supply the energy needed by the overload. Therefore, the dc-dc APU interfacing converter is forced to provide a maximum conversion ratio of 3.07 when the minimum voltage is present at the bank of SCs.

Fig. VIII.4(c) shows the voltage and current delivered at the output of the full-bridge dc-ac inverter. Again, no overshoot is noticeable in the shape of the output voltage when the load is either connected or disconnected. The high quality of the ac voltage under the 570 W or 2.89 kW load cases can be observed in Fig. VIII.5. Fig. VIII.5(a) shows the steady-state behavior of the full-bridge dc-ac inverter while feeding the 570 W load. The low $\mathrm{THD}_{\mathrm{v}}^{\mathrm{rms}} = 0.2$ % achieved is



(a) Dc-ac inverter steady-state response at 570 W feeding a resistive load.

(b) Dc-ac inverter steady-state response at 2.89 kW feeding a resistive load.

Figure VIII.5: Experimental results: Linear load changes. Dc-ac inverter steady-state responses.

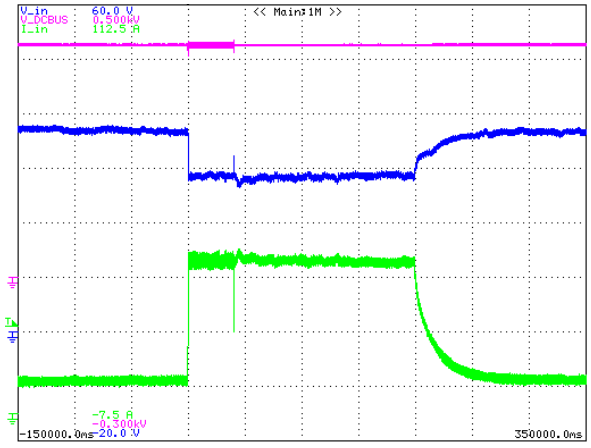
a good indicator of the quality of the sinusoidal output voltage. The contribution of the 50 Hz component dominates the shape of the output voltage.

Fig. VIII.5(b) shows the steady-state response of the dc-ac inversion stage under the full-overload condition while feeding the 2.89 kW resistive load. As it can be noticed, in this case a $\mathrm{THD}_{\mathrm{v}}^{\mathrm{rms}} = 0.3\ \%$ is achieved, confirming the good sinusoidal shape of the output voltage. In this case only the 50 Hz component of the output voltage and current is noticeable, with no evident contribution of the higher harmonics.

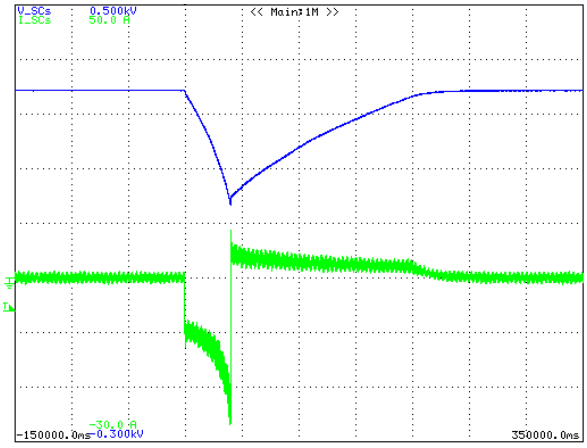
VIII.3 Nonlinear load change tests

The functioning of the energy conditioning system has been evaluated under the influence of nonlinear loads. A full-bridge diode rectifier with a RC load has been used. This load has been dimensioned following the guidelines given by the IEC in the IEC62040-3 especification [41], for the test of uninterruptible power systems (UPS). This nonlinear load has been designed to demand about 3 kW active power from the conditioning system when working under overload condition.

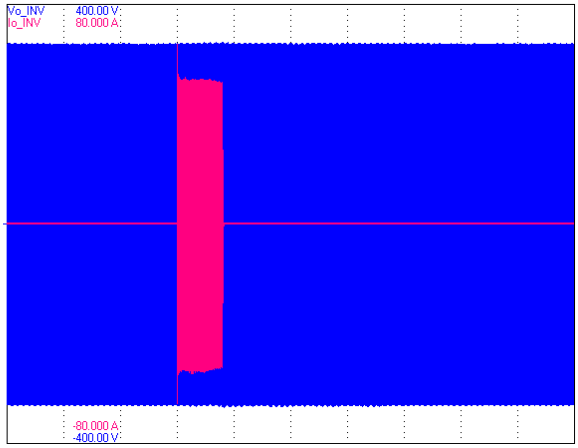
Again, two sets of tests have been carried out for the case of nonlinear loads. In the first, a change has been performed from the system working with no load to overload condition, demanding up to 4.71 kVA (with an active power component of 3.24 kW) from the system, and then back to empty load. In the second test, the system is initially feeding a rectified load of 930 VA (470 W active power), then a load change to full-overload condition is performed, de-



(a) Step-up stage input and output voltages and input current. (Scales: $v_{fc} = 10$ V/div, $v_{bus} = 100$ V/div, $i_{fc} = 15$ A/div).



(b) APU, SCs voltage and current. (Scales: $v_{sc} = 100$ V/div, $i_{sc} = 10$ A/div).



(c) Dc-ac inversion stage, output voltage and current. (Scales: $v_o = 100$ V/div, $i_o = 20$ A/div).

Figure VIII.6: Nonlinear load changes. From no load to overload condition to no load. (Time scale: 50 s/div).

manding 4.74 kVA (with 3.25 kW active power) and after the system is returned to its initial load condition. The tests performed show complete discharge/charge cycles of the bank of SCs to supply the power demanded by the overload.

VIII.3.1 No load to overload condition to no load

In this test, the system has been brought to steady state while having no load connected at the output terminals of the dc-ac inverter. At $t = 150$ s a 4.71 kVA (3.24 kW active power) rectified load is connected to the dc-ac inverter. In terms of nonlinear load change, this test constitutes the worst case scenario because the system is suddenly forced to work at maximum overload power, departing from an empty-load condition.

Fig. VIII.6 shows the energy conditioning system response to the resistive load change. Fig. VIII.6(a) shows the response of the step-up stage. From $t = 0$ s to $t = 150$ s, the system is not feeding any ac load, and the input voltage (blue trace) is $v_{fc} = 36.96$ V dc, with an input current (green trace) of $i_{fc} = 9.03$ A dc. From this values it can be determined that $p_{fc} = v_{fc}\, i_{fc} \approx 333$ W are demanded to the FC in idle state to supply the switching and parasitic losses of the system. At $t = 150$ s a 4.71 kVA nonlinear load is connected to the conditioning system. As it can be seen in Fig. VIII.6(a) an abrupt change in the input current and voltage appears in order to supply the output at full-load condition. The input voltage falls down to $v_{fc} = 28.61$ V dc and the input current grows up to $i_{fc} = 41.66$ A dc implying that about $p_{fc} = 1192$ W are being demanded from the FC unit.

At $t = 150$ s a v_{bus} voltage undershoot occurs. The voltage decreases to $v_{bus} = 406.3$ V dc, being quickly recovered by the combined action of the step-up and APU stages. This voltage drop can be translated into a 4.73 % undershoot below the steady-state dc-bus voltage value. In this case, the overload condition is hold for about 40 s. After this time, the system is returned to its initial no-load condition. At the moment that the overload is removed an overshoot presents in the voltage of the dc bus. The voltage grows up to 434.7 V dc which means a 2.02 % overshoot over the steady-state voltage value of v_{bus}. After the 4.71 kVA load has been removed, the step-up stage maintains the full-load condition power demand from the FC in order to be able to recharge the bank of SCs which has been depleted. After the SCs reach their maximum allowed operative voltage the GPC removes the SCs charge current command, making the step-up stage return to its initial condition.

Fig. VIII.6(b) shows the voltage (blue trace) and current (green trace) present at the bank of SCs during the test. From $t = 0$ s to $t = 150$ s, a small average current of $i_{sc} \approx 25.4$ mA is injected to the SCs in order to maintain the full-charge condition of the bank. During this period, the bank of SCs has a voltage of $v_{sc} = 344.1$ V dc. The small current being injected means that $p_{sc} = v_{sc}\, i_{sc} \approx 8.4$ W are demanded from the system in order to compensate the self discharge of the bank of SCs. At $t = 150$ s the 4.71 kVA load is connected. At this point, about 3 kW are extracted from the bank of SCs during the presence of the overload condition. By considering the efficiencies of the conversion stages in the path, only about 2.25 kW can reach the load, allowing the functioning of the energy conditioning system. After the load is removed, the voltage of the SCs starts to increase, recovering its full charge state in approximately 3.5 min. After this point the APU returns to its initial state, and only a small current is injected in order to maintain the state of charge of the bank of SCs.

Fig. VIII.6(b) shows that a total voltage drop of $\Delta\, v_{sc} \approx 210$ V dc presents at the bank of SCs during the overload condition. Before the overload condition, the bank presents a voltage of $v_{sc} = 344.1$ V dc, value that falls down to $v_{sc} = 134$ V dc just before the removal of the overload. This fact implies that an 84.84 % of the initial energy has been extracted from the bank of SCs to supply the energy needed by the overload during the test. Therefore, the dc-dc APU interfacing converter is forced to provide a maximum conversion ratio of 3.17 when the minimum voltage is present at the bank of SCs.

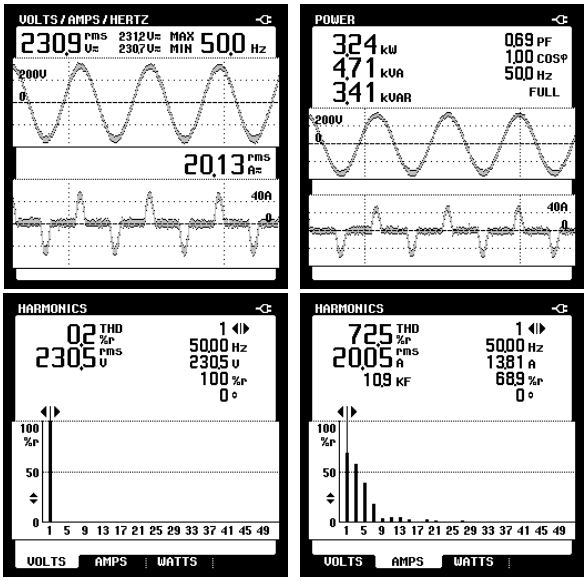
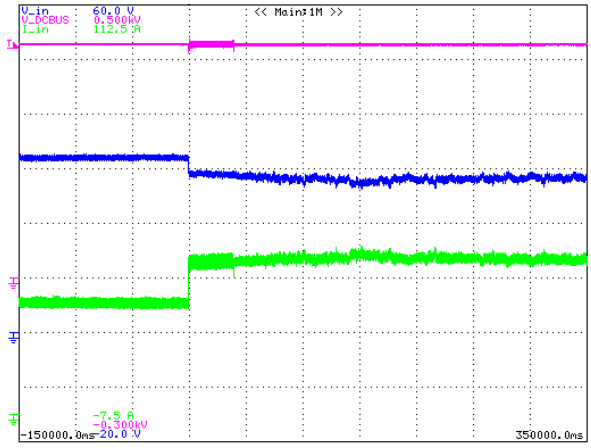


Figure VIII.7: Nonlinear load changes. Dc-ac inverter steady-state response at 4.71 kVA feeding a full-bridge diode rectifier with a RC load.

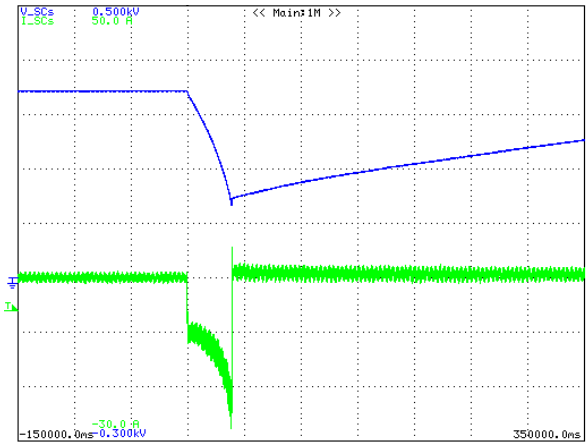
Fig. VIII.6(c) shows the voltage and current delivered at the output of the full-bridge dc-ac inverter. No overshoot is noticeable in the shape of the output voltage when the full-bridge diode rectifier is either connected or disconnected. Starting at $t = 150$ s the shape of the output voltage becomes a little distorted, but the DT-AFC control loop is able to reject the disturbing harmonic content in less than 20 cycles. A peak transient current of 65.5 A shows up when the 4.71 kVA load is connected. The steady-state responses of the output voltage and current can be observed in Fig. VIII.7. The $\text{THD}_{\text{v}}^{\text{rms}} = 0.2$ % achieved is a good indicator of the performance of the DT-AFC control scheme in the presence of periodic disturbances that are harmonics of the fundamental 50 Hz frequency. As noticed by Pileggi *et al.* [68], when this kind of loads (full-bridge diode rectifiers) is used, odd harmonics of the fundamental sinusoidal frequency are introduced into the shape of the output voltage of the dc-ac inverter. This fact can be also observed in Fig. VIII.7 by looking at the harmonic content of the output current. A rich harmonic content is present, specially in the harmonics 3, 5 and 7. A crest factor (CF) of approximately 2.5 is present when the dc-ac inverter is feeding the 4.71 kVA load.

VIII.3.2 Small load to overload condition to small load

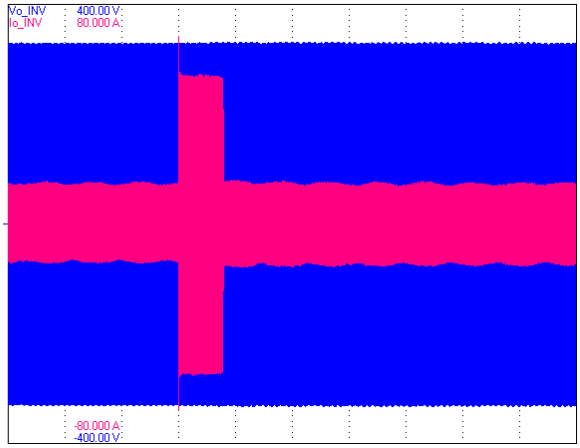
In this case the system has been driven to steady state while feeding a load within the 1 kW nominal limit. A full-bridge diode rectifier with a RC load has been connected to the system, demanding about 930 VA (with 470 W active power). At $t = 150$ s, a 4.74 kVA (with 3.25 kW active power) is connected to the dc-ac inverter, making the system work under overload condition. The system is kept feeding the overload for some seconds, depleting the energy stored in the bank of SCs, and then the initial 930 VA load condition is restored.



(a) Step-up stage input and output voltages and input current. (Scales: $v_{fc} = 10$ V/div, $v_{bus} = 100$ V/div, $i_{fc} = 15$ A/div).



(b) APU, SCs voltage and current. (Scales: $v_{sc} = 100$ V/div, $i_{sc} = 10$ A/div).



(c) Dc-ac inversion stage, output voltage and current. (Scales: $v_o = 100$ V/div, $i_o = 20$ A/div).

Figure VIII.8: Nonlinear load changes. From 470 W to overload condition and back to 470 W. (Time scale: 50 s/div)

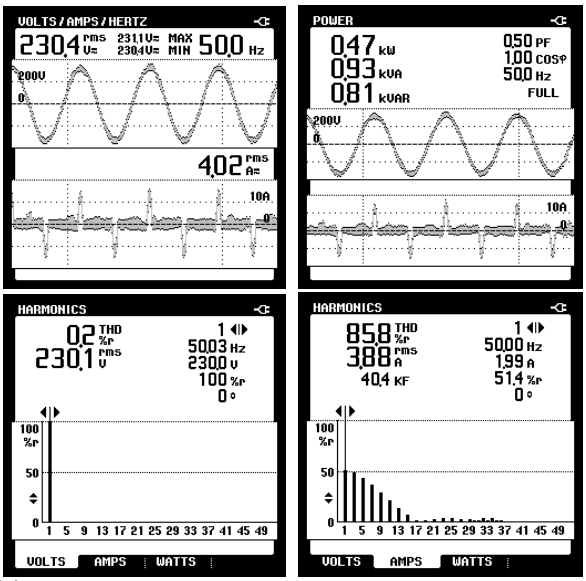
Fig. VIII.8 shows the response of the energy conditioning system during the test. Fig. VIII.8(a) shows the response of the step-up stage. From $t = 0$ s to $t = 150$ s, the system is feeding the nonlinear 930 VA load at the output of the dc-ac inverter. The input voltage (blue trace) is $v_{fc} = 32.01$ V dc, with an input current (green trace) of $i_{fc} = 30.57$ A dc. From this values it can be determined that $p_{fc} = v_{fc}\, i_{fc} \approx 979$ W are demanded to the FC. At $t = 150$ s the 4.74 kVA nonlinear load is connected to the conditioning system. As it can be seen in Fig. VIII.8(a) a change in the input current and voltage appears in order to supply the output at full-load condition. The input voltage decreases to $v_{fc} = 28.99$ V dc and the input current grows up to $i_{fc} = 41.65$ A dc implying that about $p_{fc} = 1207$ W are being demanded from the FC unit.

At $t = 150$ s a v_{bus} voltage undershoot occurs. The v_{bus} voltage falls down to 411.49 V dc, being quickly recovered by the combined action of the step-up and APU stages. This voltage drop can be translated into a 3.86 % undershoot below the steady-state dc-bus voltage value. The overload condition is hold for about 39 s. After this time, the system is returned to its initial 930 VA load condition. At this point, an overshoot presents in the voltage of the dc bus. The voltage grows up to 435.35 V dc which means a 1.79 % overshoot over the steady-state voltage value of v_{bus}. After the 4.74 kVA load has been removed, the step-up stage maintains the full-load condition power demand from the FC in order to be able to feed the 930 VA load, and use the remaining power that can be extracted from the FC to recharge the bank of SCs which has been depleted.

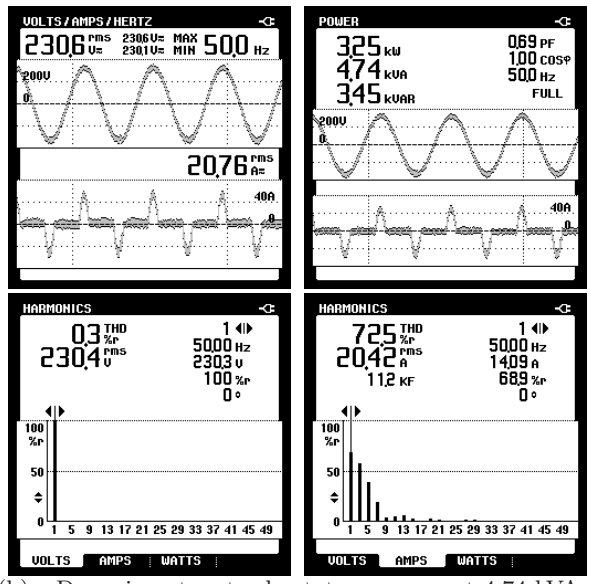
Fig. VIII.8(b) shows the voltage (blue trace) and current (green trace) present at the bank of SCs during the test. From $t = 0$ s to $t = 150$ s, only a small current is injected to the SCs in order to maintain the full-charge condition of the bank. During this period, the bank of SCs has a voltage of $v_{sc} = 342.95$ V dc. At $t = 150$ s the 4.74 kVA load is connected. At this point, around 3 kW are extracted from the bank of SCs during the presence of the overload condition. By considering the efficiencies of the conversion stages in the path, only about 2.25 kW can reach the load, allowing the functioning of the energy conditioning system. After the load is removed, the system keeps feeding the 930 VA load, and the rest of the energy of the FC is used to recharge the bank of SCs. The voltage of the SCs starts to increase, recovering its full charge state in approximately 25 min. After this point the APU returns to its initial state, and only a small current is injected in order to maintain the state of charge of the bank of SCs.

Fig. VIII.8(b) shows that a total voltage drop of $\Delta v_{sc} \approx 211$ V dc presents at the bank of SCs during the overload condition. Before the overload condition, the bank presents a voltage of $v_{sc} = 343$ V dc, value that falls down to $v_{sc} = 133.27$ V dc just before the overload is removed. This fact implies that an 84.9 % of the initial energy has been extracted from the bank of SCs to supply the energy needed by the overload. Therefore, the dc-dc APU interfacing converter is forced to provide a maximum conversion ratio of 3.19 when the minimum voltage is present at the bank of SCs.

Fig. VIII.8(c) shows the voltage and current delivered at the output of the full-bridge dc-ac inverter. No overshoot is noticeable in the shape of the output voltage when the full-bridge diode rectifier is either connected or disconnected. Starting at $t = 150$ s the shape of the output voltage becomes a little distorted, but the DT-AFC control loop is able to reject the disturbing harmonic content in less than 20 cycles. A peak transient current of 68.44 A shows up when the 4.71 kVA load is connected. The steady-state responses of the output voltage and current can be observed in Fig. VIII.9. The steady-state behavior of the dc-ac inverter while feeding the 930 VA can be observed in Fig. VIII.9(a). The $\text{THD}_{\text{v}}^{\text{rms}} = 0.2$ % achieved is a good indicator of the performance of the DT-AFC control scheme in the presence of periodic disturbances that are harmonics of the fundamental 50 Hz frequency. This fact can be also observed in Fig. VIII.9(a) by looking at the harmonic content of the output current, where a rich odd harmonic content is present, specially in the harmonics 3, 5, 7, 9, 11, 13 and 15. A crest factor (CF) of approximately 3.6 is present when the dc-ac inverter is feeding the 930 VA load.



(a) Dc-ac inverter steady-state response at 930 VA feeding a nonlinear load.



(b) Dc-ac inverter steady-state response at 4.74 kVA feeding a nonlinear load.

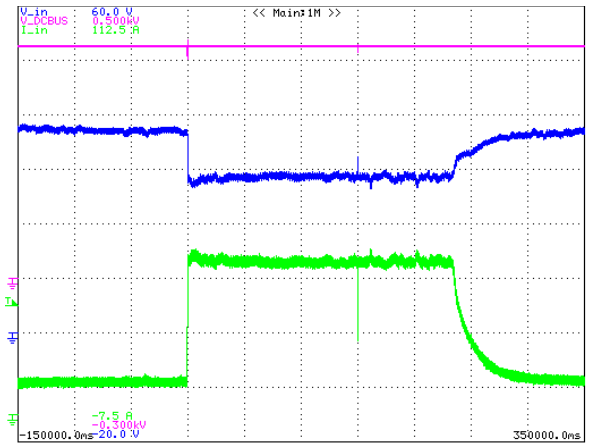
Figure VIII.9: Nonlinear load changes. From 930 VA to overload condition and back to 930 VA.

Fig. VIII.9(b) shows the steady-state behavior of the dc-ac inverter while feeding the 4.74 kVA. Again, the $\mathrm{THD}_{\mathrm{v}}^{\mathrm{rms}} = 0.3$ % achieved is an evidence of the good sinusoidal voltage shape delivered by the full-bridge dc-ac inverter at full-load condition. The DT-AFC control scheme rejects the odd harmonic disturbances induced especially by the high contribution of harmonics 3, 4 and 7 on the shape of the output current. A CF of 2.54 is present under these circumstances.

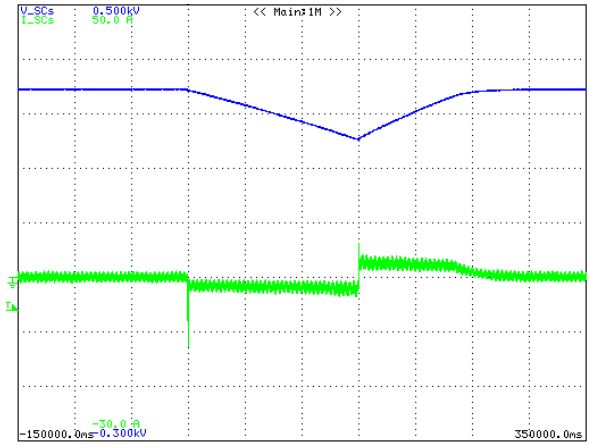
VIII.4 Dynamic load change tests

In this case, dynamic loads have been used to test the functioning of the energy conditioning system. Two sets of tests have been performed to evaluate the response of the energy conditioning system. In the first, load changes have been performed from the system feeding no load to feed a 1.15 kVA dynamic load composed of an industrial vacuum debris capturer and a jigsaw connected in parallel and simultaneously activated by the action of a single switch. The system feeds this load for some time and then the system is returned to its initial condition.

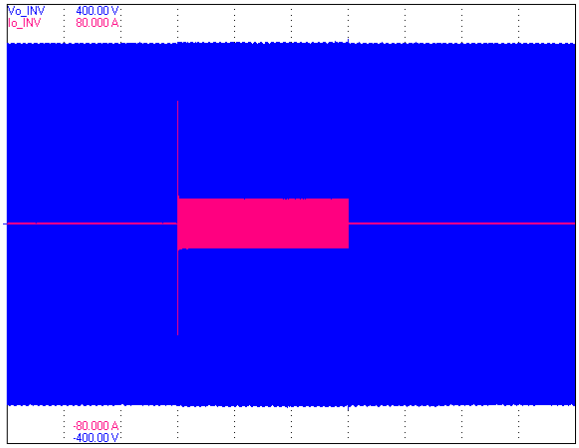
For the second test, the system has been brought to steady state feeding a resistive load. After, the dynamic load is connected in parallel to the resistive load, achieving a 1.72 kVA total load. The system is hold feeding this load for some seconds and then the system is returned to its initial condition.



(a) Step-up stage input and output voltages and input current. (Scales: $v_{fc} = 10$ V/div, $v_{bus} = 100$ V/div, $i_{fc} = 15$ A/div).



(b) APU, SCs voltage and current. (Scales: $v_{sc} = 100$ V/div, $i_{sc} = 10$ A/div).



(c) Dc-ac inversion stage, output voltage and current. (Scales: $v_o = 100$ V/div, $i_o = 20$ A/div).

Figure VIII.10: Dynamic load changes. From no load to loaded condition to no load. (Time scale: 50 s/div)

VIII.4.1 No load to loaded condition to no load

In this test, the system has been driven to steady state while feeding no load at the output of the dc-ac inverter. At $t = 150$ s a total load of 1.15 kVA (with 1.08 kW active power) is connected to the output of the dc-ac inverter. The dc-ac inverter feeds the load which consists of a LPKF 750 W vacuum debris capturer and a 400 W Black & Decker jigsaw connected in parallel.

Fig. VIII.10 shows the energy conditioning system response to the resistive load change. Fig. VIII.10(a) shows the response of the step-up stage. From $t = 0$ s to $t = 150$ s, the system is not feeding any ac load, and the input voltage (blue trace) is $v_{fc} = 37.14$ V dc, with

an input current (green trace) of $i_{fc} = 9.98$ A dc. From this values it can be determined that $p_{fc} = v_{fc}\, i_{fc} \approx 333$ W are demanded to the FC in idle state to supply the switching and parasitic losses of the system. At $t = 150$ s the 1.15 kVA dynamic load is connected to the conditioning system. As it can be seen in Fig. VIII.10(a) an abrupt change in the input current and voltage appears in order to supply the output at full-load condition. The input voltage falls down to $v_{fc} = 28.53$ V dc and the input current grows up to $i_{fc} = 42$ A dc implying that about $p_{fc} = 1198$ W are being demanded from the FC unit.

At $t = 150$ s a v_{bus} voltage undershoot occurs. The voltage falls down to $v_{bus} = 402.77$ V dc, after recovered by the combined action of the step-up and APU stages. This voltage drop can be translated into a 5.42 % undershoot below the steady-state dc-bus voltage value. In this case, the loaded condition is hold for about 2.5 min. After this time, the system is returned to its initial no-load condition. At the moment that the load is removed an overshoot presents in the voltage of the dc bus. The voltage grows up to 439.72 V dc which means a 1.03 % overshoot over the steady-state voltage value of v_{bus}. After the 1.15 kVA load has been removed, the step-up stage maintains the full-load condition power demand from the FC in order to be able to return the bank of SCs to its full-charge condition. After the SCs reach their maximum allowed operative voltage the GPC removes the SCs charge current command, making the step-up stage return to its initial no-load condition.

Fig. VIII.10(b) shows the voltage (blue trace) and current (green trace) present at the bank of SCs during the test. At $t = 150$ s the 1.15 kVA load is connected. Although the load is around the 1 kW nominal limit, some extra watts (about 490 W) are extracted from the bank of SCs during the presence of the load. This energy is mainly used to compensate the parasitic and switching losses of the system. By considering the efficiencies of the conversion stages in the path, only about 368 W from the original 490 W can reach the load. After the load is removed, the voltage of the SCs starts to increase, recovering its full charge state in approximately 2 min. After this point the APU returns to its initial state, and only a small current is injected in order to maintain the state of charge of the bank of SCs.

Fig. VIII.10(b) shows that a total voltage drop of $\Delta\, v_{sc} \approx 93.85$ V dc presents at the bank of SCs during the presence of the load. Before the connection of the load, the bank presents a voltage of $v_{sc} = 344.86$ V dc, value that falls down to $v_{sc} = 251.79$ V dc just before the removal of the load. This fact implies that an 46.93 % of the initial energy has been extracted from the bank of SCs during the 2.5 min that the load has been connected. Therefore, the dc-dc APU interfacing converter is forced to provide a maximum conversion ratio of 1.68 when the minimum voltage is present at the bank of SCs. Fig. VIII.10(c) shows the voltage and current delivered at the output of the full-bridge dc-ac inverter. No overshoot is noticeable in the shape of the output voltage when the dynamic loads are either connected or disconnected. Starting at $t = 150$ s the shape of the output voltage becomes a little distorted, but the DT-AFC control loop is able to reject the disturbing harmonic content in less than 8 cycles. A peak transient current of 44.61 A shows up when the 1.15 kVA dynamic load is connected. The steady-state responses of the output voltage and current can be observed in Fig. VIII.11. The $\mathrm{THD}_{\mathrm{v}}^{\mathrm{rms}} = 0.3$ % achieved is a good indicator of the performance of the DT-AFC control scheme in the presence of periodic disturbances that are harmonics of the fundamental 50 Hz frequency.

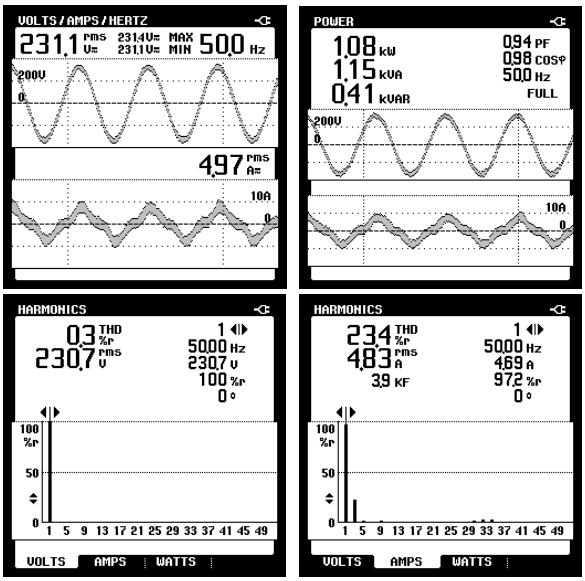


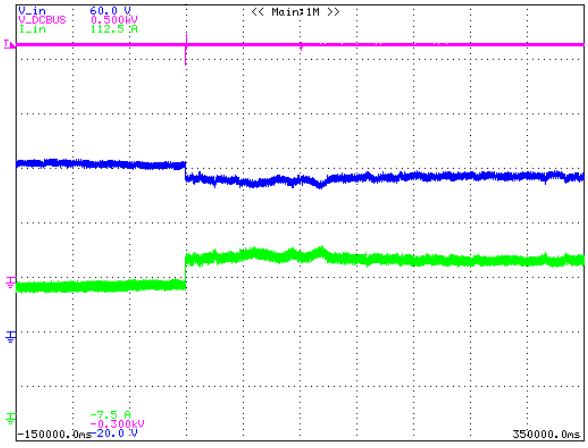
Figure VIII.11: Dynamic load changes. Dc-ac inverter steady-state response at 1.15 kVA.

The output current has a noticeable contribution of the 3rd harmonic of the fundamental 50 Hz frequency. This fact can be also observed in Fig. VIII.11 by looking at the harmonic content of the output current. The output current has an almost triangular waveform. A crest factor (CF) of approximately 1.74 is present when the dc-ac inverter is feeding the 1.15 kVA load.

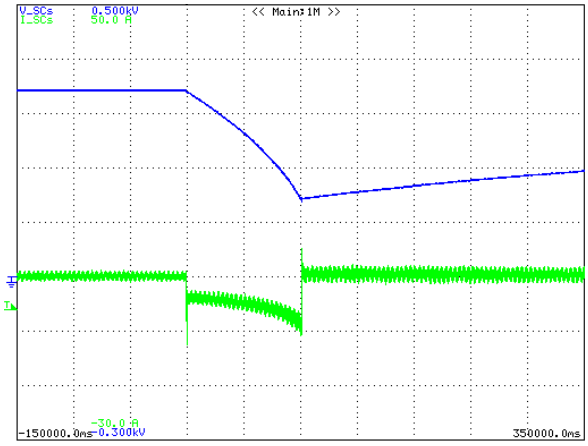
VIII.4.2 Small load to loaded condition to small load

In this case the system has been driven to steady state while feeding a resistive load of 560 W. At $t = 150$ s, a total load of 1.72 kVA (with 1.69 kW active power) is connected to the dc-ac inverter. This load is composed by the 560 W resistive load in parallel with a LPKF 750 W vacuum debris capturer and a 400 W Black & Decker jigsaw. The system is kept feeding this load for some seconds, and then the initial 560 W resistive-load condition is restored.

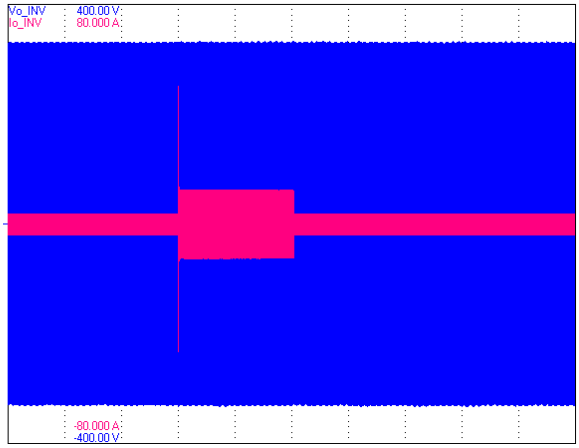
Fig. VIII.12 shows the response of the energy conditioning system during the test. Fig. VIII.12(a) shows the response of the step-up stage. From $t = 0$ s to $t = 150$ s, the system is feeding the resistive 560 W load at the output of the dc-ac inverter. The input voltage (blue trace) is $v_{fc} = 30.74$ V dc, with an input current (green trace) of $i_{fc} = 35.08$ A dc. From this values it can be determined that $p_{fc} = v_{fc}\, i_{fc} \approx 1078$ W are demanded to the FC. At $t = 150$ s the 1.72 kVA dynamic load is connected to the conditioning system. As it can be seen in Fig. VIII.12(a) a change in the input current and voltage appears in order to supply the output at full-load condition. The input voltage falls down to $v_{fc} = 27.67$ V dc and the input current grows up to $i_{fc} = 43.22$ A dc implying that about $p_{fc} = 1196$ W are being demanded from the FC unit.



(a) Step-up stage input and output voltages and input current. (Scales: $v_{fc} = 10$ V/div, $v_{bus} = 100$ V/div, $i_{fc} = 15$ A/div).



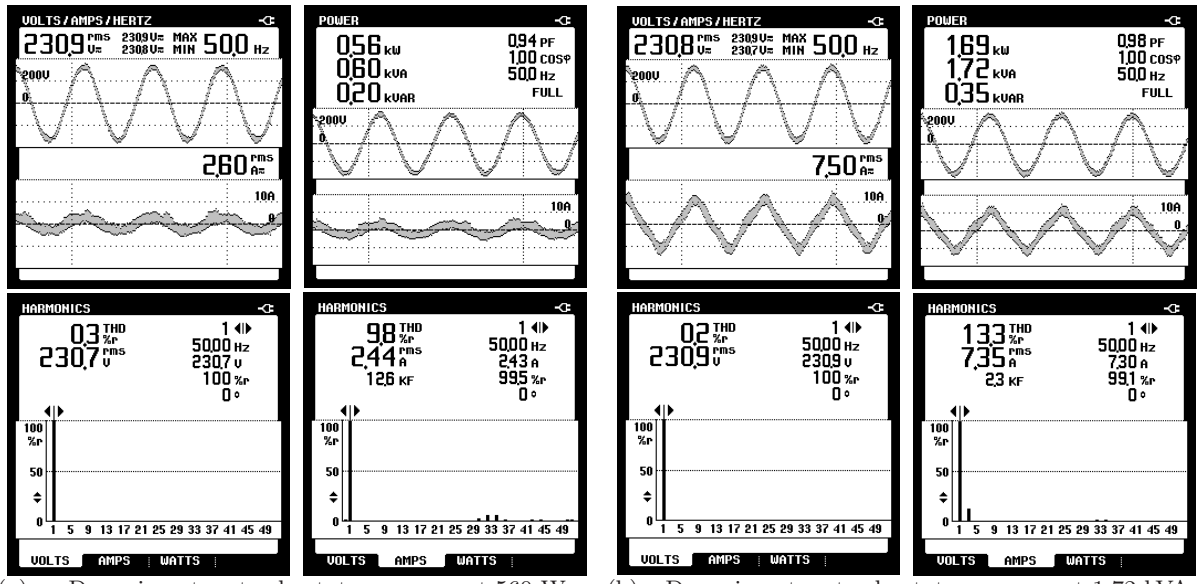
(b) APU, SCs voltage and current. (Scales: $v_{sc} = 100$ V/div, $i_{sc} = 10$ A/div).



(c) Dc-ac inversion stage, output voltage and current. (Scales: $v_o = 100$ V/div, $i_o = 20$ A/div).

Figure VIII.12: Dynamic load changes. From 560 W to overload condition and back to 560 W. (Time scale: 50 s/div)

At $t = 150$ s a v_{bus} voltage undershoot occurs. The v_{bus} voltage drops down to 390.33 V dc, being quickly recovered by the combined action of the step-up and APU stages. This voltage drop can be translated into a 8.55 % undershoot below the steady-state dc-bus voltage value. The load condition is hold for about 1.75 min. After this time, the system is returned to its initial 560 W resistive-load condition. At this point, an overshoot presents in the voltage of the dc bus. The voltage grows up to 431.45 V dc which means a 1.19 % overshoot over the steady-state voltage value of v_{bus}. After the 1.72 kVA load has been removed, the step-up stage maintains the full-load condition power demand from the FC in order to be able to feed the 560 W load, and use the remaining power that can be extracted from the FC to recharge the bank of SCs which has been depleted.



(a) Dc-ac inverter steady-state response at 560 W feeding a linear load.

(b) Dc-ac inverter steady-state response at 1.72 kVA feeding a dynamic load.

Figure VIII.13: Dynamic load changes. From 560 W to overload condition and back to 560 W.

Fig. VIII.12(b) shows the voltage (blue trace) and current (green trace) present at the bank of SCs during the test. From $t = 0$ s to $t = 150$ s, only a small current is injected to the SCs in order to maintain the full-charge condition of the bank. At $t = 150$ s the 1.72 kVA load is connected. At this point, around 1.25 kW are extracted from the bank of SCs during the presence of the 1.72 kVA load. By considering the efficiencies of the conversion stages in the path, only about 940 W can reach the load, allowing the functioning of the energy conditioning system. After the load is removed, the system keeps feeding the 560 W load, and the rest of the energy of the FC is used to recharge the bank of SCs. The voltage of the SCs starts to increase, recovering its full charge state in approximately 30 min. After this point the APU returns to its initial state, and only a small current is injected in order to maintain the state of charge of the bank of SCs.

Fig. VIII.12(b) shows that a total voltage drop of $\Delta\, v_{sc} \approx 205$ V dc presents at the bank of SCs during the loaded condition. Before the 1.72 kVA load is connected, the bank presents a voltage of $v_{sc} = 343.29$ V dc, value that decreases to $v_{sc} = 138.15$ V dc just before the overload is removed. This fact implies that an 83.8 % of the initial energy has been extracted from the bank of SCs to supply the energy needed by the dynamic load. Therefore, the dc-dc APU interfacing converter is forced to provide a maximum conversion ratio of 3.08 when the minimum voltage is present at the bank of SCs.

Fig. VIII.12(c) shows the voltage and current delivered at the output of the full-bridge dc-ac inverter. No overshoot is noticeable in the shape of the output voltage when the dynamic load is either connected or disconnected. Starting at $t = 150$ s the shape of the output voltage becomes

a little distorted, but the DT-AFC control loop is able to reject the disturbing harmonic content in less than 20 cycles. A peak transient current of 50.11 A shows up when the 1.72 kVA load is connected. The steady-state responses of the output voltage and current can be observed in Fig. VIII.13. The steady-state behavior of the dc-ac inverter while feeding the 560 W can be observed in Fig. VIII.13(a). The $\text{THD}_{\text{v}}^{\text{rms}} = 0.3$ % achieved is a good indicator of the quality of the sinusoidal voltage shape. Being this a linear load, as expected, only the 50 Hz fundamental frequency has a noticeable contribution in the harmonic content of both, the shapes of the output voltage and current.

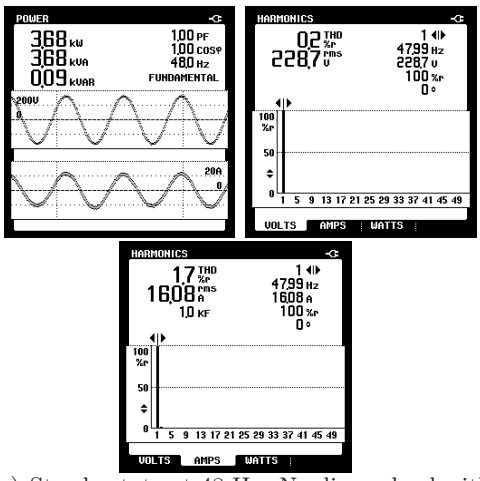
Fig. VIII.13(b) shows the steady-state behavior of the dc-ac inverter while feeding the 1.72 kVA dynamic load. Again, the $\text{THD}_{\text{v}}^{\text{rms}} = 0.2$ % achieved is an evidence of the good sinusoidal voltage shape delivered by the full-bridge dc-ac inverter. The DT-AFC control scheme rejects the odd harmonic disturbances induced especially by the high contribution of the 3rd harmonic on the shape of the output current. A CF of 1.57 is present under these circumstances.

VIII.5 Full-bridge dc-ac inverter feeding an active filter

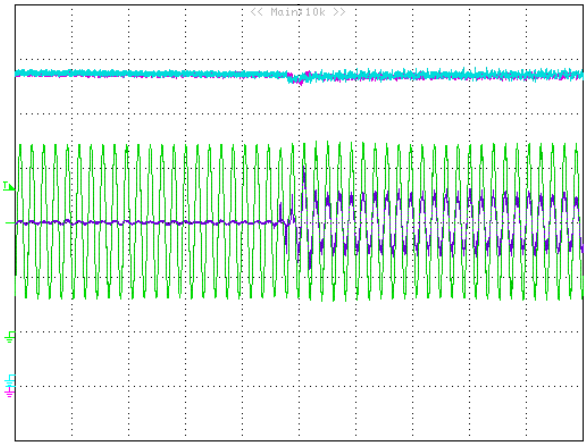
The purpose of this set of experiments is to show the robustness of the DT-AFC controller used on the dc-ac inversion stage. In this case the dc-ac inverter, which is a switching power device, is used to feed another switching power system. The load to be fed is an active filter connected in a shunt manner between the inverter and a full-bridge diode rectifier with a RC load as presented by Costa-Castelló *et al.* in [23]. The active filter is a switching power electronics device, and therefore it has a complex dynamic behavior. Under this scenario, the DT-AFC controller would be considered robust if the dc-ac inverter is able to feed the switching load avoiding the excitation of any mutual resonant mode between the devices. The tests have been performed including variations in the fundamental frequency of output voltage provided by the dc-ac inverter, showing the capability of the dc-ac inversion stage to act as a variable frequency ac voltage source.

The dc-ac inverter has been fed in this case by using a three-phase, full-bridge diode rectifier and an autotransformer, in order to be able to provide the output power level demanded by the load. The set has been adjusted in order to get a dc-bus voltage of around $v_{bus} = 425$ V dc in idle state. Therefore, the voltage at the dc bus is not regulated and important variations can occur depending on the power level to be supplied. These voltage variations are seen as external disturbances by the DT-AFC control scheme.

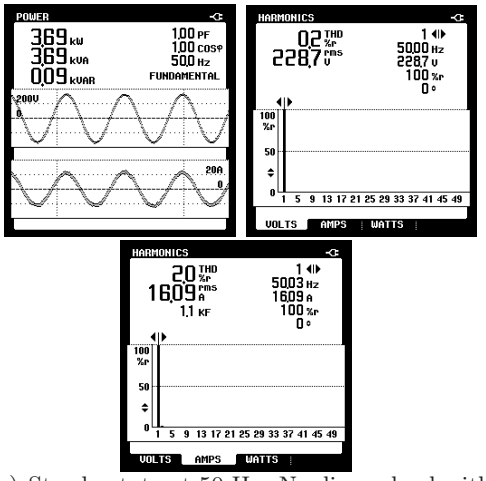
The frequency of the reference signal to be followed by the dc-ac inverter has been varied from 48 Hz up to 52 Hz. The output voltage feeds the pair load/active filter, being seen from the dc-ac inverter as an ac load with certain complex dynamic behavior. Care must be taken when connecting switching power converters in this way, in this case one switching converter is used as the power supply and the other as part of the load. Mutual resonant modes could be excited, and it is not recommended to connect them directly, in this way the integrity of the converters can be protected. In this case a 1 to 1 transformer has been used as interface between the power supply and the load. The dynamic response of the transformer has been considered in the fine tuning of the DT-AFC control.



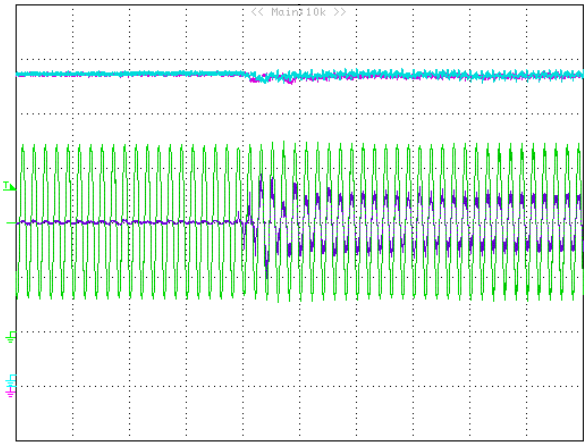
(a) Steady state at 48 Hz. Nonlinear load with the active filter.



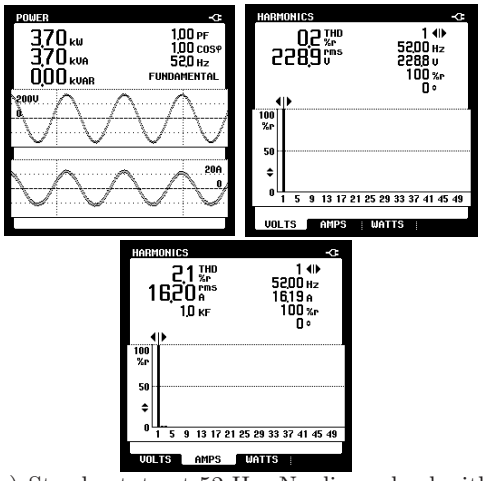
(b) Nonlinear load change at 48 Hz. From empty to full-load with the active filter.



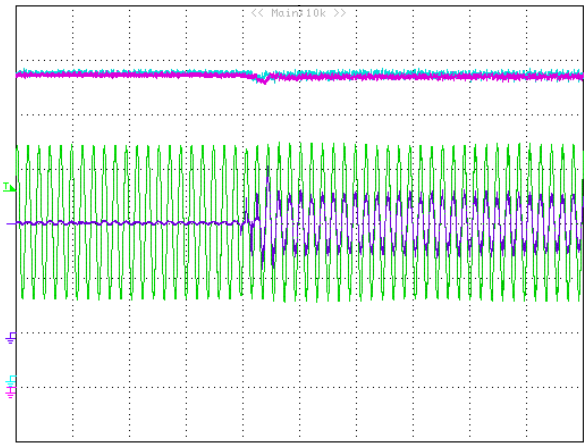
(c) Steady state at 50 Hz. Nonlinear load with the active filter.



(d) Nonlinear load change at 50 Hz. From empty to full-load with the active filter.



(e) Steady state at 52 Hz. Nonlinear load with the active filter.



(f) Nonlinear load change at 52 Hz. From empty to full-load with the active filter.

Figure VIII.14: Dc-ac inverter, steady-state behavior and load change response while feeding a nonlinear load connected in a shunt manner with a power factor correction active filter at 48, 50 and 52 Hz. (Oscilloscope scales: (green) $v_o = 225$ V/div, (pink and lightblue) $\pm\, v_{bus} = 75$ V/div, (purple) $i_o = 43$ A/div, Time scale: 100 ms/div).

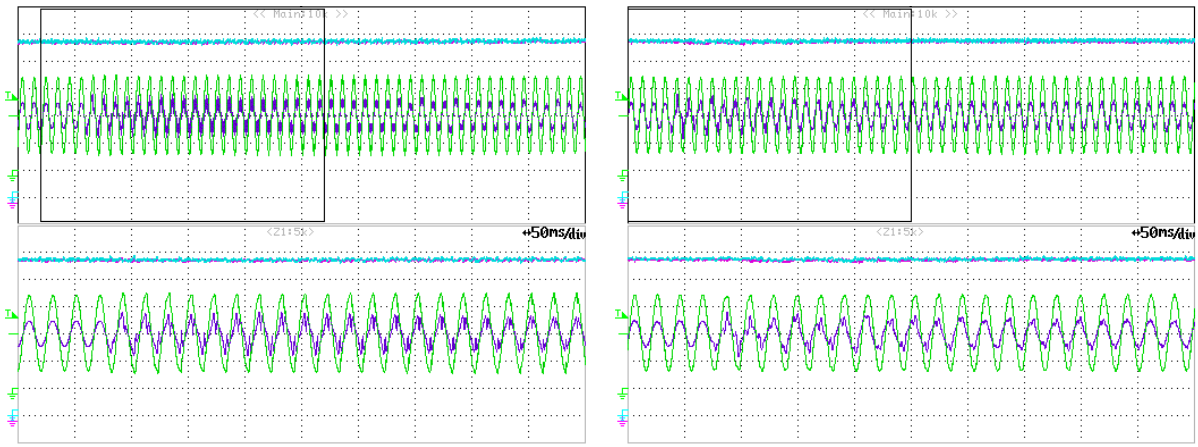
Two sets of tests have been carried out. In the first, the dc-ac inverter has been driven to steady state while feeding the active filter working with no load connected to it. Suddenly, the rectified load is connected to the system, achieving a load level of about 3.3 kW seen at the inverter side. This load change has been done while generating ac output voltages of 48, 50 and 52 Hz. In the second set of tests, the system has been driven to steady state while feeding the 3.3 kW load. Suddenly, the frequency of the reference signal is changed from 48 to 50 Hz in the first case, and from 50 to 48 Hz in the second.

VIII.5.1 Steady-state behavior under different frequency references and load changes

Fig. VIII.14 shows the steady-state behavior of the dc-ac inverter and the system response to load changes while the inverter is generating 48, 50 and 52 Hz ac output voltages. Figs. VIII.14(a) and VIII.14(b) show the response of the system under the 48 Hz case. The steady-state behavior of the output of the dc-ac inverter when the converter if feeding the full-bridge diode rectifier with the active filter is presented in Fig. VIII.14(a). As it can be observed, the dc-ac inverter is able to feed this load, achieving a very good 48 Hz sinusoidal shape with $\mathrm{THD}_{\mathrm{v}}^{\mathrm{rms}} = 0.2$ %. The low $\mathrm{THD}_{\mathrm{i}}^{\mathrm{rms}} = 1.7$ % present at the shape of the output current confirms the good operation of the active filter, making the load appear as a resistive one at the dc-ac inverter side. Fig. VIII.14(b) shows the inverter response to a load change from the active filter point of view. First, the dc-ac inverter is only feeding the shunt active filter with no load. At approximately 475 ms, the nonlinear load is connected, making the inverter to deliver a total power of around 3.7 kW. The dc-ac inverter current (purple trace) has a disturbed shape of the output current that slowly, after some seconds, takes an almost sinusoidal form. The shape of the output voltage (green trace) achieves the $\mathrm{THD}_{\mathrm{v}}^{\mathrm{rms}} = 0.2$ % condition after some seconds as well.

The steady-state response of the inverter in the 50 Hz case can be observed in Fig. VIII.14(c). Again a $\mathrm{THD}_{\mathrm{v}}^{\mathrm{rms}} = 0.2$ % is achieved. It is clear that the inverter is able to feed this complex load with no resonant interactions. Fig. VIII.14(d) shows the load change for the inverter feeding the load at 50 Hz. Again, at the beginning, the shapes of the output voltage and current become a little bit disturbed, but the DT-AFC control loop is able to overcome the situation, making the output voltage to recover an almost sinusoidal shape after some seconds.

When the inverter is providing the 52 Hz output voltage, the behavior of the system is very similar to the previous cases. The steady-state behavior under the full-load condition observed in Fig. VIII.14(e) achieves also a $\mathrm{THD}_{\mathrm{v}}^{\mathrm{rms}} = 0.2$ %. When observing at the voltage and current harmonic content, it is evident that no contribution of any higher harmonic is noticeable. Regarding the system response under the load change presented in Fig. VIII.14(f), the system is able to hold a good enough voltage shape at the beginning in order to feed the load. The DT-AFC controller is able to reject the undesired harmonic content from the shape of the output voltage. The speed at which the harmonics are removed, is mainly due to the initial interactions that occur among the dc-ac inverter, nonlinear load and the active filter, but after some time the set is able to reach an acceptable steady-state behavior.



(a) From 48 Hz to 50 Hz.

(b) From 50 Hz to 48 Hz.

Figure VIII.15: Experimental results: Step frequency changes. (Oscilloscope scales: (green) $v_o = 225$ V/div, (pink and lightblue) $\pm\, v_{bus} = 75$ V/div, (purple) $i_o = 43$ A/div, Main time scale: 100 ms/div, Zoom time scale: 50 ms/div)

VIII.5.2 Step frequency variations

For these tests, the system has been driven to steady state while feeding the 3.7 kW load composed by the full-bridge diode rectifier along the active filter. Step load changes have been performed. The amplitude of the changes is ±2 Hz. For the first test, the system is feeding the load at 48 Hz, at approximately $t = 120$ ms, the frequency of the voltage provided by the dc-ac inverter is changed from 48 Hz to 50 Hz. Fig. VIII.15(a) shows the response of the system to this change. The output voltage (green trace) gets some distortion but the 50 Hz component is dominant. The effects of the distortion can be observed by the shape of the output current (purple trace). The system is able to eliminate the undesired harmonic content after some seconds, achieving the steady-state behavior shown in Fig. VIII.14(c).

For the second test, the output voltage reference frequency is changed from 50 Hz down to 48 Hz at approximately $t = 75$ ms. The response of the system can be seen in Fig. VIII.15(b). The output voltage distortion is lower in this case than in the previous one, allowing the system to have a faster recovery. The shape of the output voltage recovers acceptable quality levels after about 3 s. The dc-ac inverter is therefore able to feed the load with the frequency change. The relatively long recovery time is caused mainly by the mutual interactions between the switching systems.

Part 4

– Conclusions and Future Work –

CHAPTER IX

Conclusions and Future Work

IX.1 Conclusions

The development of this thesis has achieved the objectives stated in Section I.2, contributing with a new design of an energy conditioning system for PEM type FCs.

Among the contributions of this thesis are:

- After an analysis of various energy conditioning system topologies, finally a conditioning architecture based on multiple-stage dc-ac power inverter configuration has been chosen. After the general modular architecture was determined, an analysis of the different conversion requirements for each of the modules has been performed. Having established the conversion requirements and constraints present on the system, appropriate converter topologies have been chosen in order to accomplish the desired energy conversion objectives of each of the modules as presented in Chapter II.
- The energy conditioning system has been designed considering the FC unit as a black-box power supply, this assumption allows the separated and specialized control of the electrochemical variables on one side, and the control of the electrical variables handled in this work. The energy conditioning system developed in this work allows then the use of the FC unit as an independent device, without any interference in its control or operation, other than the power being demanded from it.
- The use of a modular hardware architecture has allowed the development of different control schemes for each of the modules in order to achieve the local control objectives, and a global controller in charge of coordinating the functioning and contribution of each of the power conversion modules in order to assure the power balance of the whole energy conditioning system. The developed controllers are:
  - Global power balance control stage. This is the highest level control loop. This control stage takes care that the power levels demanded/injected from/towards the main power source (FC unit), the auxiliary power source (bank of SCs), and the load are coherent with the input/output power conditions and the specifications of each of the modules that compose the energy conditioning system as presented in Chapter VI.
  - Input current control for the step-up stage. This control loop is in charge of controlling the current that is demanded from the FC unit by the step-up stage as presented in Chapter III.

  - Dc-ac inverter control - output voltage reference tracking. This control stage is in charge of allowing the dc-ac inverter to produce a good 230V ac and 50Hz voltage with the purpose of feeding broad variety of loads as presented in Chapter IV.
  - APU control - current control of the bank of supercapacitors. This control stage is in charge of controlling the current that is injected/extracted from/towards the bank of SCs used in the auxiliary power unit as presented in Chapter V.

- An experimental setup has been successfully built in order to test the chosen power converters and the controllers designed. The hardware implementation has been achieved using regular industry grade commercial components, obtaining a realistic experimentation platform regarding the state of the art of the technology.

- Although the converter used in the step-up stage presents a very complex load-dependent behavior as presented in Section II.1.2 the use of the empiric approach presented in Section III.1 used to determine the plant to be controlled by the input current control loop of the step-up stage has demonstrated its effectiveness for the solution of this problem. The addition of the current filter (L_{in} and C_{in}), the selection of the input current as the variable to be controlled, and the selection of $\hat{u}_1$ as control variable in the inner-control loop have made easier to find a good continuous-time approximation of the inner-loop nominal plant.

- A deep analysis has been carried out in Section IV.3.1 regarding the properties of the DT-AFC control scheme. The validity of the criteria used for the selection of the design parameters is confirmed by the DT-AFC properties studied.

- A high-quality ac output voltage shape has been obtained by using the DT-AFC control scheme as can be observed in the simulation results presented in Section IV.3.3 and the experimental results presented in Chapter VIII. The steady-state $\mathrm{THD}_{\mathrm{v}}^{\mathrm{rms}}$ obtained is about 10 times lower than the maximum allowed steady-state total harmonic distortion stated in the specifications of the system given in Section I.2.

- The global power balance control scheme has been developed and tested over the experimental platform, even though the lack of a model of the step-up power converter used. The use of the empiric approach presented in Section VI.1 used to develop the models needed has proven its feasibility for this application.

- The global power balance approach developed has allowed the separation and distribution of the slow and the fast power requirements to the appropriate conversion modules. Only the slow power requirements are routed to step-up stage which is the only module that directly extracts the energy from the FC unit. The auxiliary power unit supplies the fast power demands that the FC unit is not able to satisfy. By doing this, the fast power requirements do not reach the FC unit, and therefore the lifespan and/or integrity of this device is not compromised in front of energy requirements beyond its bandwidth limitation.

IX.2 Future work

The development of this work has allowed us to identify some areas of interest that could lead to future research lines derived from this thesis.

Among the possible future works that can be performed are:

- To perform experiments with the system being fed by a real FC unit instead of the FC emulator used. Although the FC emulator built reflects in a very good manner the electrical behavior of the device, as given in the specifications of the target FC stack [5], these tests would help to gain a more deep insight regarding other aspects such as the stress level applied over the FC unit, and the response of the energy conditioning system in front of the changes on the voltage and current of the FC due to its operation.

- To perform a deeper analysis over the selection and tuning of the g_k gains used on the $R_k(z)$ resonators of the DT-AFC control scheme, evaluating the use of optimization techniques to maximize/minimize the appropriate objective function. This objective function can be build attending to different design concerns, such as desired performance, robustness, etc., which will be determined by the conditions of the problem.

- To explore the development of complementarity models of the converter. One starting point could be to apply the results obtained by Pérez-Rivas in [66] and [67]. Another interesting option would be to explore the applicability of the complementarity modeling framework for power converters presented by Vasca *et al.* in [94]. After a complementarity model has been obtained it would be worthy to explore the different linear/nonlinear control techniques that could be applied over the system.

- To continue the research line started during the three month internship performed from January/05/2009 to April/07/2009 at the *Division systèmes* of the *Laboratoire des signaux et systèmes* (L2S), located at Gif-Sur-Yvette, France. The L2S is a common facility to *L'École Supérieure d'Électricité* (SUPÉLEC), the French *Centre National de la Recherche Scientifique* (CNRS), and the *Université Paris-Sud 11*. The analysis of the dynamic behavior of the converter used on the step-up stage started under the guidance of Prof. Romeo Ortega can lead to a better understanding on the functioning and control of the converter. Also, this analysis can lead on the development of nonlinear controllers which can be implemented and tested over the experimental setup.

- To analyze the modifications needed over the energy conditioning system to support the presence of regenerative loads. Stand-alone energy conversion systems can be used in a broad variety of applications, some loads are known to momentarily reverse the power flow of the system, such as induction machines in braking mode. These momentary reverse power flows could be stored and latter used.

- To analyze the use of complementary energy storing devices such as flywheels/batteries/SCs, evaluating different energy sharing policies in order to achieve different objectives, such as expanding the lifespan of the batteries, providing fast/slow/long-duration overload supply characteristics to the system, absorbtion and reuse of reverse energy flows, etc.

- To perform experimental tests feeding other types of loads, for example lighting systems using sodium-vapor lamps, which have a very capacitive behavior at start-up but change their dynamic behavior as the temperature on the lamp grows.

- To perform the conversion of the dc-ac inversion stage from single phase to three phase plus neutral. The use of a three-phase plus neutral dc-ac inversion stage would induce disturbances in the voltage at the dc bus due to unbalanced loads. This change would imply a modification in the structure of the control algorithms used and the inclusion of some kind of disturbance rejection block at dc-bus control stage.

- To evaluate the selection of other switching components and/or modulation techniques to improve the efficiency of the full-bridge dc-ac inverter.

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