Optimal Inductor Current in Boost DC/DC Converters Operating in Burst Mode under Light-Load Conditions

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***Abstract*— This letter analyses how the efficiency of boost DC/DC converters operating in burst mode under light-load conditions can be improved by an appropriate selection of the inductor current that transfers energy from the input to the output. A theoretical analysis evaluates the main power losses (fixed, conduction and switching losses) involved in such converters and how do they depend on the inductor current. This analysis shows that there is an optimal value of this current that causes minimum losses and, hence, maximum efficiency. These theoretical predictions are then compared with experimental data resulting from a commercial boost DC/DC converter (TPS61252) whose average inductor current is adjustable. Experimental results show that the use of the optimal inductor current, which was around 340 mA for an output voltage of 5 V, provides an efficiency increase of 7%.**

***Index Terms*— Boost converter, burst mode, DC/DC converter, efficiency, light-load conditions.**

I. Introduction

MANY portable devices operate in low-power standby modes for most of the time and, therefore, increasing the efficiency of voltage regulators under light-load conditions (i.e. for load currents of a few milliamperes) is crucial for extending the battery lifetime. Regrettably, switching DC/DC converters with a pulse-width modulation (PWM), which involves a fixed switching frequency, have a low efficiency (say, lower than 60 % [1]) at light loads mainly due to switching losses. To cope with this limitation, the efficiency of PWM converters can be improved by dynamically adjusting: (i) the gate driving voltage [2,3], (ii) the size of the switching transistors [4,5], and (iii) the number of active phases (i.e. phase shedding) in multiphase DC/DC converters [6]. Soft-switching techniques, such as zero-voltage switching and zero-current switching, have also been proposed to reduce switching losses due to the voltage-current overlap in low-power [7] and medium-power [8] DC/DC converters

Another way to tackle the light-load efficiency is the use of a hybrid control whereby the converter operates in PWM at heavy loads, but it switches to a variable-frequency mode, such as pulse-frequency modulation (PFM) or burst mode (BM), at light loads. In PFM, the switching frequency is scaled down with the load current, thus reducing the switching losses at light loads. Two PFM-based approaches operating in discontinuous conduction mode (DCM) have been proposed [9]: (i) constant on-time [10], which can also be dynamically adapted [11], and (ii) constant peak inductor current [12]. In both cases, there is an optimal value of on-time and peak current that leads to maximum efficiency [9].

In BM (also known as pulse-skip mode), the transistors of the switching DC/DC converter are cyclically switched on and off at a fixed frequency (the same as in PWM) during an active period thus resulting in a burst of energy pulses transferred to the output, but they are permanently in off-state during an inactive period [13]. The lower the load current, the longer the inactive period and, hence, the lower the equivalent switching frequency. This principle has also been applied to improve the light-load efficiency of resonant DC/DC converters [14]. Two techniques have been proposed to control the burst in active period [15]: (i) constant duty cycle [13]; and (ii) constant average (or peak) inductor current [16], which has been applied in many commercial DC/DC converters such as TPS6120x, LT1303, L6920 and STBB1-AXX. Experimental results using the latter technique showed that the efficiency in continuous conduction mode (CCM) was higher than in DCM [16]. However, unlike what happens in PFM, the optimal value of inductor current that provides maximum efficiency in BM-CCM has not been analyzed so far. This is evaluated herein for a boost DC/DC converter showing that an appropriate selection of that current can provide an efficiency increase of 7%.

II. Operating Principle

A schematic of a synchronous boost DC/DC converter is shown in Fig. 1. It relies on an inductor (L) and two power MOSFET transistors (MN and MP) with the corresponding gate control signals (v_{c1} and v_{c2}) generated by a control circuit. This control circuit has two feedback loops: (i) a voltage loop that monitors the output voltage (v_{out}) by a voltage divider R_1-R_2 and a comparator (with a hysteresis of $\pm V_{hys}$) whose non-inverting input is connected to a reference voltage (V_{ref}), and (ii) a current loop that monitors the inductor current (i_L) by either a shunt resistance in series with L or the voltage drop

This work was supported by the Spanish Ministry of Science under project TEC2011-27397.

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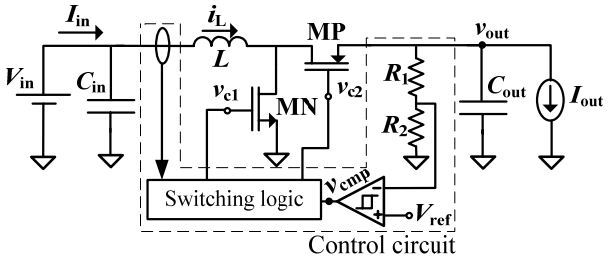


Fig. 1. Schematic of a synchronous boost DC/DC converter.

across MN or MP. Current information has also been obtained by measuring the output voltage ripple, as suggested in V^2-controlled converters, but its application to boost converters has some limitations [17] that have been solved, for instance, by (a) an improved version of the V^2 control called V^2C control [18], and (b) a differentiator-based analog processing of the output voltage ripple [19]. The input of the converter is connected to a DC voltage source (V_{in}), which models the voltage supplied by batteries, in parallel with a high-value input capacitor (C_{in}). On the other hand, the output of the converter is connected to a DC current source (I_{out}), which models the current consumed by the load, in parallel with a high-value output capacitor (C_{out}).

The circuit in Fig. 1 regulates v_{out} around a desired DC voltage (V_{out}) by operating in BM. Its overall operating principle is represented in Figs. 2a, 2b and 2c with two stages that respectively last $t_{inactive}$ and t_{active}, and an overall duty cycle $D_T = t_{active}/T_T$, where $T_T = t_{inactive} + t_{active}$. In the first stage, the converter is deactivated (i.e. both transistors are in off-state) and C_{out} supplies the DC current to the load, thus decreasing v_{out}. When $v_{out} = V_{out} - V_{hys}$, the state of the comparator output (v_{cmp}) changes and the second stage starts. Then, input energy (mostly coming from C_{in}, but also from V_{in}) is transferred to the output through a burst of energy pulses, thus increasing v_{out}. To do so, a burst of on/off pulses is applied to the gate of the transistors, as shown in Fig. 2c and with more details in Fig. 2d. When $v_{out} = V_{out} + V_{hys}$, the converter is deactivated and the process starts again. Note that the current coming from V_{in} increases during t_{active} providing part of the energy required, but it decreases towards zero during $t_{inactive}$ with the recharge of C_{in}. The average value of that current is $I_{in} = I_{out}V_{out}/V_{in}$ if losses are neglected.

During the active period, the converter has two operating phases that respectively last t_{on} and t_{off}, with a switching period $T_s = t_{on} + t_{off}$. In steady state, the duty cycle (i.e. $D = t_{on}/T_s$) depends on the operating conditions as $1-V_{in}/V_{out}$, assuming CCM and no losses. The switching frequency (i.e. $f_s = 1/T_s$) is fixed and equal to that employed in PWM. In the first phase (MN on, MP off), input energy is stored in L and i_L increases, whereas in the second phase (MN off, MP on), the energy accumulated in L is transferred to the output and i_L decreases. A current-programmed mode control in CCM is assumed so that i_L has an average of I_{L0} (whose value is analyzed herein so as to maximize the efficiency) and a ripple of ΔI_L. The resulting waveforms of v_{c1} and i_L are shown in Figs. 2d and 2e, respectively; v_{c2} is the same as v_{c1} but with

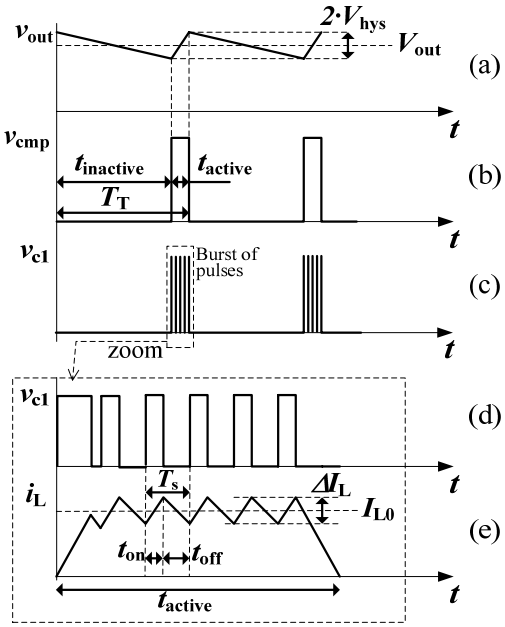


Fig. 2. Waveforms of interest from the circuit in Fig. 1 operating in BM-CCM.

some dead time between them to prevent cross conduction. Using this operating principle, the lower the load current, the lower the equivalent switching frequency (i.e. $f_s{\cdot}D_T$) and, hence, the lower the effects of the switching losses on the efficiency.

III. Theoretical Analysis

Power losses in the DC/DC converter shown in Fig. 1 are analyzed using the equivalent circuit model represented in Fig. 3, where R_S is a shunt resistance to sense i_L, R_L is the equivalent series resistance (ESR) of L, R_{Ci} and R_{Co} are the ESR of C_{in} and C_{out}, respectively, R_N and R_P are the on-resistances of MN and MP, respectively, C_A is the parasitic capacitance at node A (for example, due to the drain-bulk junction capacitance of MN), and C_{G1} and C_{G2} are the parasitic capacitances at the gate of MN and MP, respectively. The control circuit is assumed to be powered from the output, as usually happens in boost converters, and has a current consumption of $I_{Q,a}$ in active mode and $I_{Q,i}$ in inactive mode, where $I_{Q,i}$ is expected to be much lower than $I_{Q,a}$.

The circuit in Fig. 3 has three types of power losses [9]: (i) fixed losses, which are mainly due to the quiescent current of the control circuit; (ii) conduction losses, which are generated by the Joule effect involved in the parasitic resistances; and (iii) switching losses, which are mostly caused by the charge-discharge process of the parasitic capacitances and the voltage-current overlap in MN during the transitions (with an average transition time of t_c) from on to off and vice versa [20]. The expression of such losses in both active and inactive modes is summarized in Table I, where $R_{eq,a} = R_{Ci}+R_S+R_L+R_ND+(R_P+R_{Co})(1-D)$, $R_{eq,i} = R_{Ci}(V_{out}/V_{in})^2+R_{Co}$ and $C_{eq} = C_{G1}+C_{G2}+C_A$. As for $R_{eq,a}$ it is assumed that, in active mode, i_L is mostly provided by C_{in} and that the current through MP is

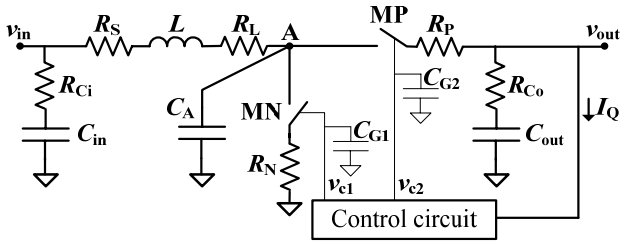


Fig. 3. Equivalent circuit model for the analysis of power losses in the circuit shown in Fig. 1.

TABLE I
POWER LOSS COMPONENTS OF THE CIRCUIT IN FIG. 3 IN BOTH ACTIVE AND INACTIVE MODES

Power losses	Active mode	Inactive mode
Fixed	$V_{out}I_{Q,a}$	$V_{out}I_{Q,i}$
Conduction	$R_{eq,a}I_{L0}^2$ [a]	$R_{eq,i}I_{out}^2$
Switching	$C_{eq}V_{out}^2 f_s + V_{out}I_{L0}t_c f_s$	0

[a] The RMS value of i_L is approximated to I_{L0} since $\Delta I_L < I_{L0}$ [21].

much higher than I_{out}, whereas for $R_{eq,i}$ it is considered that the current that charges C_{in} in inactive mode is $I_{out}V_{out}/V_{in}$. Furthermore, C_{G1}, C_{G2} and C_A have been lumped in one equivalent capacitance (C_{eq}) since they have the same charging voltage (i.e. V_{out}); note that the control circuit is powered from the output and, hence, the gate driving voltage of MN and MP equals V_{out}. Fixed losses due to leakage current of transistors and capacitors, and switching losses due to the body diode of MP during the dead time and to the inductor core have been considered negligible.

The average value of power losses over a whole period (i.e. T_T) can be expressed and approximated (assuming $P_{L,active} >> P_{L,inactive}$) as

$$P_L = P_{L,active}D_T + P_{L,inactive}(1-D_T) = \left(P_{L,active} - P_{L,inactive}\right)D_T + P_{L,inactive} \approx P_{L,active}D_T + P_{L,inactive} \quad (1)$$

where $P_{L,active}$ and $P_{L,inactive}$ are the overall power losses in active and inactive modes, respectively, obtained from Table I. Since the charge extracted from C_{out} in inactive mode (i.e. $I_{out}t_{inactive}$) equals that accumulated in C_{out} in active mode (i.e. $[I_{L0}(1-D)-I_{out}]t_{active}$), D_T can also be written as $I_{out}V_{out}/I_{L0}V_{in}$. Using this relation in (1), the efficiency in BM can be calculated as

$$\eta = \frac{1}{1+\frac{P_L}{P_{out}}} \approx 1-\frac{P_L}{P_{out}} = 1-\frac{1}{V_{in}}\left[R_{eq,a}I_{L0} + \frac{V_{out}I_{Q,a}+C_{eq}V_{out}^2 f_s}{I_{L0}} + V_{out}t_c f_s\right] - \frac{I_{Q,i}}{I_{out}} - \frac{I_{out}R_{eq,i}}{V_{out}} \quad (2)$$

where P_{out} is the output power (i.e. $V_{out}I_{out}$). According to (2), η increases with increasing V_{in}, decreases with increasing V_{out},

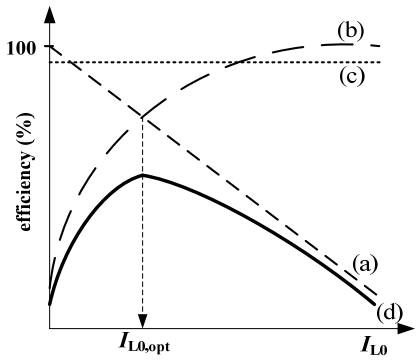


Fig. 4. Efficiency versus I_{L0} considering the effects of different power loss components.

but slightly depends on I_{out} because the last two terms on the right-hand side in (2) are the least significant factors; this performance will be verified later in Section IV. If we compare converters operating in BM with those that continuously operate in PWM [22], we realize that the effects of V_{in} and V_{out} on η are similar, but not those of I_{out} since the light-load efficiency of PWM converters significantly decreases with decreasing I_{out}.

Equation (2) also shows that η clearly depends on I_{L0}, but each power loss component has its own effects on such dependence. This is represented in Fig. 4 as follows: case (a) corresponds to conduction losses in active mode, where η decreases with increasing I_{L0}; case (b) corresponds to fixed losses and switching losses due to C_{eq} in active mode, where η increases with increasing I_{L0}; case (c) corresponds to switching losses due to the voltage-current overlap in active mode together with losses in inactive mode, where η is independent of I_{L0}; and case (d) shows the overall effects with a maximum of efficiency at an optimal value of I_{L0} ($I_{L0,opt}$). Taking the derivative of (2) with respect to I_{L0} and then making the result of the derivative equal zero, we can find the value of I_{L0} that causes the maximum:

$$I_{L0,opt} = \sqrt{\frac{V_{out}I_{Q,a}+C_{eq}V_{out}^2 f_s}{R_{eq,a}}} \quad (3)$$

which is independent of both I_{out} and V_{in}, but it increases with increasing V_{out}.

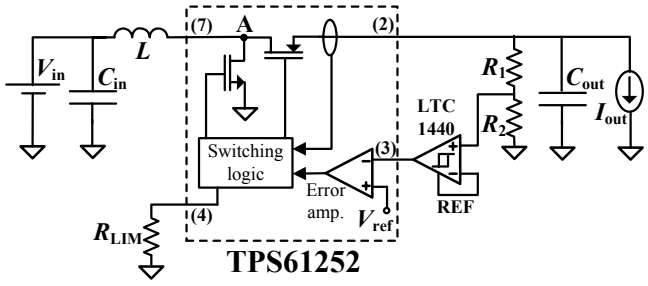


Fig. 5. Application circuit based on the TPS61252 employed to prove the concept of optimal inductor current; the numbers given in brackets are the pin numbers of the TPS61252.

IV. Experimental Results

The concept of optimal inductor current has been tested experimentally using a commercial boost DC/DC converter (TPS61252 from Texas Instruments [23]) that enables adjusting I_{L0} from 100 mA to 1500 mA by an external resistor (R_{LIM}); such a current is measured on-chip through the voltage drop across MP and, hence, $R_S = 0$ in this particular case. In order to have the BM-CCM operation shown in Fig. 2, it was necessary to place an external comparator (LTC1440 from Linear Technology) between the voltage divider R_1-R_2 and the feedback (FB) input of the converter, as shown in Fig. 5. Using this circuit, if v_{out} is lower than the desired voltage, then the comparator output is low, which brings the converter to active mode and, consequently, i_L is regulated around I_{L0}. Otherwise, if v_{out} is higher than the desired voltage, then the comparator output is high and the converter enters into inactive mode. The comparator LTC1440 is an ultralow-power model with a built-in reference (REF in Fig. 5) and a programmable hysteresis that was adjusted to have $V_{hys} =$ 5 mV.

The circuit in Fig. 5 was subjected to different test conditions: (i) different values of I_{out} (5, 10 and 20 mA) sunk by a DC current source (Agilent B2901), (ii) different values of V_{out} (4, 5 and 6 V) set by an appropriate voltage divider R_1-R_2 and measured by a digital multimeter (Agilent 34410), and (iii) different values of V_{in} (2.4, 2.7 and 3.0 V) supplied by a DC voltage source (Agilent E3631A); this range of V_{in} emulates, for instance, that supplied by two cylindrical alkaline primary batteries in series. In all cases, a power analyzer (Yokogawa WT310) measured the average input power with a sampling frequency of 100 kSa/s and an update rate of 5 s. C_{in} and C_{out} were low-ESR tantalum capacitors of 2×1 mF and 4×2.2 mF, respectively, and $L = 2.2$ µH.

The operating principle of the circuit in Fig. 5 was first verified by monitoring the voltage waveform at the main nodes using a digital oscilloscope. Fig. 6 shows, for example, the resulting waveforms for $V_{in} = 3.0$ V, $V_{out} = 5.0$ V, $I_{out} = 10$ mA and $I_{L0} \approx 370$ mA. The output voltage and the comparator output (i.e. pins #2 and #3 of the TPS61252, respectively) are represented in Fig. 6a for several active and inactive periods. Note that the signal at the comparator output is the complementary of that represented in Fig. 2b because this signal is then inverted by the on-chip error amplifier. In Fig. 6a we measured $V_{hys} \approx$ 6-7 mV and $D_T = 5\%$, which agrees with that estimated from $I_{out}V_{out}/I_{L0}V_{in}$. On the other hand, Fig. 6b shows the voltage at the switching node A (i.e. pin #7) within one active period; this signal is also the complementary of that represented in Fig. 2d since it is inverted through MN. In Fig. 6b we measured $f_s = 3.7$ MHz, instead of the nominal value of 3.25 MHz, and $D = 44\%$, which agrees with that estimated from $1-\eta V_{in}/V_{out}$ assuming $\eta = 91\%$ (reported later in Fig. 7). Moreover, the value of D was very stable during the active period, which means that the inductor current was well regulated around I_{L0}.

The experimental results of efficiency versus I_{L0} are shown in Fig. 7 for different values of (a) I_{out}, (b) V_{out}, and (c) V_{in}, using $V_{in} = 3.0$ V, $V_{out} = 5.0$ V and $I_{out} = 10$ mA as default values. The optimal value of I_{L0} was independent of both I_{out} (Fig. 7a) and V_{in} (Fig. 7c), but it increased with increasing V_{out} (Fig. 7b), which agrees with (3). To be precise, $I_{L0,opt} \approx 340$ mA in Figs. 7a and 7c, and it increased from 255 to 455 mA in Fig. 7b. Moreover, the efficiency was almost constant with I_{out} (Fig. 7a), decreased with increasing V_{out} (Fig. 7b), and increased with increasing V_{in} (Fig. 7c), as predicted by (2). With respect to the case with minimum efficiency (which was found at either the minimum or the maximum value of I_{L0}), the efficiency increased by 6%, 8% and 7% in Figs. 7a, 7b and 7c, respectively, when $I_{L0,opt}$ was applied.

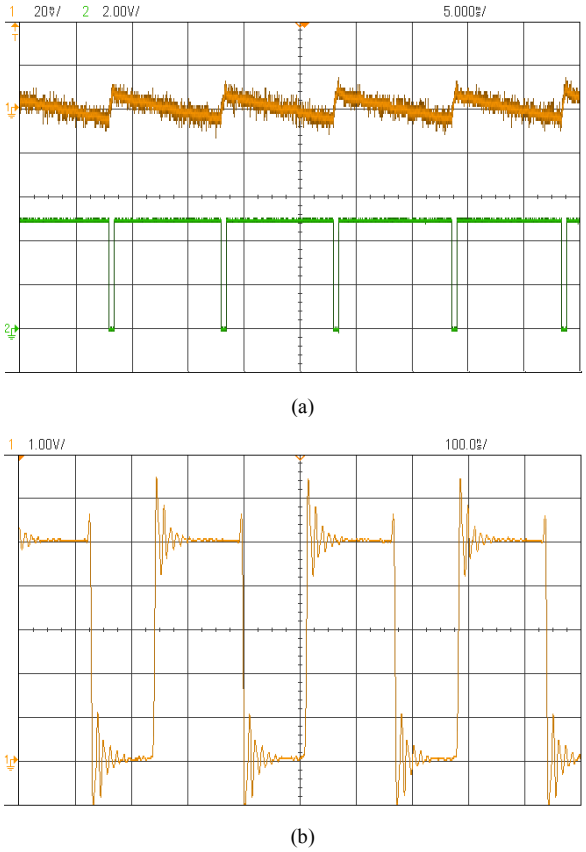
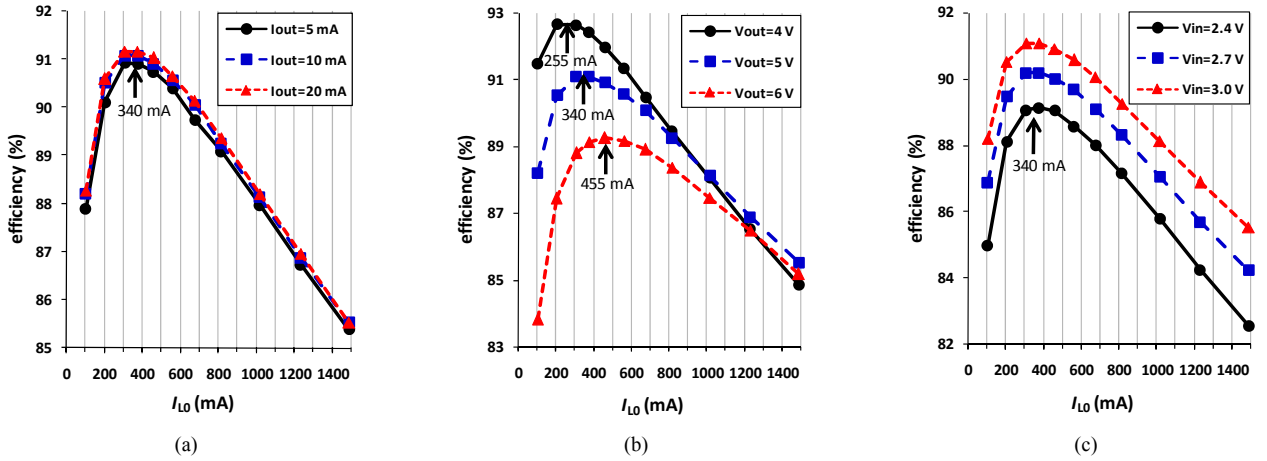


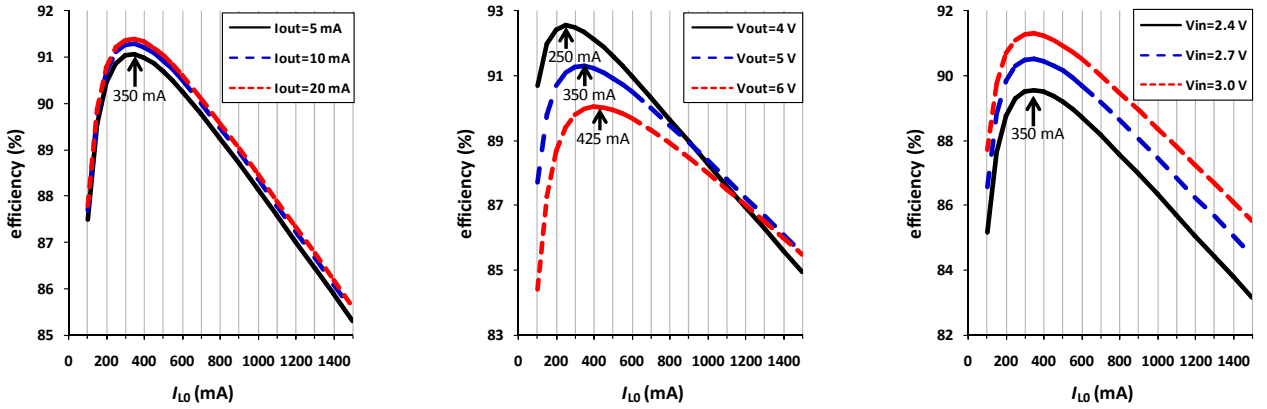
Fig. 6. From the circuit in Fig. 5, experimental waveforms of (a) the output voltage (channel 1 in AC coupling) and the comparator output (channel 2) for several active and inactive periods, and (b) the voltage at the switching node A within one active period.

For the same test conditions represented in Fig. 7, Fig. 8 shows the efficiency predicted by (2) using the data available in datasheets; two remarks about Fig. 8: (i) C_{eq} and t_c were unknown and were initially extracted by fitting (2) to a set of experimental results, and (ii) R_N and R_P were assumed to be dependent on the gate driving voltage of the transistors (i.e. V_{out}) in Fig. 8b [2,4]. Figs. 7 and 8 show a very similar response both qualitatively and quantitatively (see, for example, the values of $I_{L0,opt}$ and η). Therefore, we can conclude that the model proposed in Section 3 properly predicts the efficiency of DC/DC converters in BM-CCM at different operating conditions.



(a) (b) (c)

Fig. 7. Experimental efficiency versus I_{L0} for different values of (a) I_{out}, (b) V_{out}, and (c) V_{in}. The default values are V_{in} = 3.0 V, V_{out} = 5.0 V and I_{out} = 10 mA.



(a) (b) (c)

Fig. 8. Efficiency predicted by (2) versus I_{L0} for different values of (a) I_{out}, (b) V_{out}, and (c) V_{in}. The default values are V_{in} = 3.0 V, V_{out} = 5.0 V and I_{out} = 10 mA.

V. Conclusion

A theoretical analysis and a set of experimental results have demonstrated that DC/DC converters operating in BM-CCM under light-load conditions have an optimal value of inductor current in terms of efficiency. This optimal current is independent of both (i) the input voltage and, hence, of the state (fresh or spent) of the input batteries, and (ii) the load current and, hence, of the variability of the current consumption of the electronics to be powered. However, such an optimal current does depend on the desired output voltage. Experimental tests with a commercial boost DC/DC converter operating in BM have shown that the use of the optimal inductor current (of 340 mA at V_{out} = 5 V) provides up to 7% increase in efficiency. DC/DC converters with a hybrid control (i.e. PWM and BM) can make good use of the results presented herein to increase their efficiency under light-load conditions.

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