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# Analysis and Application of FLL based on the Processing of the Input and Output Periods

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**Original scientific paper**

This paper describes development, analysis, implementation and application of one recursive Frequency Locked Loop (FLL) based on the measurement and processing of the periods of the input and output signals. FLL is the linear discrete system of the first order, which regulates its output once per the input period. The FLL parameters are defined by the frequencies of three clocks. These frequencies have to be mutually in defined relationship for the stable FLL. FLL provides a wide range of properties useful for different applications. The stability and the other conditions, under which the described system can have the properties of a FLL, are investigated using the Z transform analyses. Using mathematical analyses and the simulations of this FLL it is shown that, for the corresponding system parameters, FLL possesses the power noise rejection ability. This FLL can also be used for the different predicting and tracking applications, for the measurements of the frequency of the input signal in the noise environments and for the other applications. The oscilloscope picture of the characterized input and output signals, recorded on the realized FLL, is presented.

**Key words:** Digital circuit, Frequency Locked Loop, Phase Locked Loop, Recursive feedback algorithm

**Analiza i primjena frekvencijske petlje zasnovane na obradbi ulazne i izlazne periode.** Ovaj rad opisuje razvoj, analizu, realizaciju i primjenu jedne rekurzivne frekvencijske petlje zasnovane na obradbi perioda ulaznog i izlaznog signala. Petlja predstavlja linearni diskretni sustav prvog reda koji korigira svoj izlaz jednom po ulaznoj periodi. Parametri petlje su definirani s tri frekvencije takta. Za stabilnu petlju ove frekvencije moraju biti u međusobno definiranom odnosu. Petlja posjeduje širok spektar karakteristika za različite primjene. Stabilnost i drugi uvjeti pod kojima opisan sustav ima osobine frekvencijske petlje, su analizirani korištenjem Z transformacije. Matematičkom analizom i simulacijom rada petlje je pokazano da za određene vrijednosti parametara, petlja osigurava jako potiskivanje šuma. Petlja se također može koristiti za različite potrebe predikcije i praćenja signala, za mjerenja frekvencije ulaznog signala u prisustvu šuma i za druge primjene. Prikazan je osciloskopski snimak karakterističnih ulaznih i izlaznih signala, snimljenih na realiziranom modelu petlje.

**Ključne riječi:** Digitalni sklop, Frekventna petlja, Fazna petlja, Rekurzivni algoritam s povratnom vezom

## 1 INTRODUCTION

It is of the interest to emphasize that the feedback systems Phase Locked Loop (PLL) and Frequency Locked Loop (FLL) are closely related systems, but they are not the same. Any PLL, if it is in the stable state, reduces both the phase and the frequency difference between the input and output signals to zero. Generally, the phase difference in PLL is not to be obviously zero, but it must not depend on the initial conditions. FLL, known in the literature as the Frequency Lock Generators as well, reduces only the frequency difference to zero if it is in the stable state. The output frequency of FLL can also be, when FLL is in the stable state, in certain pre-defined relation to the input frequency. Its phase difference depends on the initial conditions. There are many applications in frequency-based system, where the frequency is the only signal parameter which carries or represents the information. In such applications the phase difference is not of interest and FLL are either more suitable for usage than PLL or represent the only possible solutions.

Generally, the error as the difference between the input and output signals of FLL and PLL can be generated by measurement of the phase, the amplitude, the frequency and the time. The PLL based on the measurement of phase are mostly used today. They are well known as classical PLL. The PLL based on the measurement of the amplitude of the input sinusoidal signal make the correction of the output signals once per input period and they were called the discrete PLL. These PLL, besides the other parts, include the digital filter, sampling and different signal con-

versions. Because of that they are complex and not suitable for applications. PLL or FLL which are based on the measurement of time are very rare in the literature. Many years ago appeared FLL based on the measurement and comparison of the input and output periods. According to the result of comparison, this FLL, either increases or decreases the output period only for one period of clock. This approach of FLL requires a lot of hardware and it does not offer the real processing of the input and output periods. Therefore this FFL does not possess the functional abilities for a wider range of applications. Because of that this approach has not been appearing in the literature in the meantime. But it is worth mentioning it to provide continuity and better insight into the contributions described in this paper.

Unlike the previous measurement of errors, the measurement of the time is the easiest and the most precise today. It is necessary to develop the corresponding algorithms for the processing of time error. They have to be simple for realizations and they should enable, at the same time, wide range of applications of FLL and PLL based on this principle. Providing that the corresponding algorithms are explored, FLL and PLL based on time errors would appear as more powerful and more applicable than the others.

One new approach to FLL of the first order is described in this paper. FLL is based on the measurement and on the recursive processing of the input and output periods. The recursive algorithm executes, at the same time, the function of digital filtering. Except in [1-2] similar approach to FLL is not described in the literature. FLL described in [1] functions as software predictor and another one described in [2] functions as phase shifter. FLL described in [3-5] are based on the measurement of frequency difference between the input and output signals. Nevertheless they are closely related to FLL described in this article because of the similarity of some hardware parts used in their realizations. The articles [6-14] represent in the field of FLL and PLL the wider base of literature. The books [15-19] are used for electronics implementation and as mathematical and theoretical base in the development and analyses.

## 2 MATHEMATICAL DESCRIPTION OF FLL

### 2.1 Recursive equation of FLL

General equation describing the discrete system of the first order, which processes the periods of the input and output signals, can be presented as:

$$TO_{k+1} = a \cdot TI_k + b \cdot TO_k \tag{1}$$

where $TO_{k+1}$ and $TO_k$ are the periods of the output signal $S_{op}$ which occur at discrete times respectively $t_{k+1}$ and $t_k$, $TI_k$ is the period of the input signal $S_{in}$ which occur at discrete time $t_k$, and "a" and "b" are the system parameters. Note that (1) can be transformed in another form, which is more convenient for the realization as well as for the analyses. If the system parameters are changed by $a = f_2/f_c$ and $b = f_1/f_c$, (1) will change to:

$$f_c \cdot TO_{k+1} = f_1 \cdot TI_k + f_2 \cdot TO_k \tag{2}$$

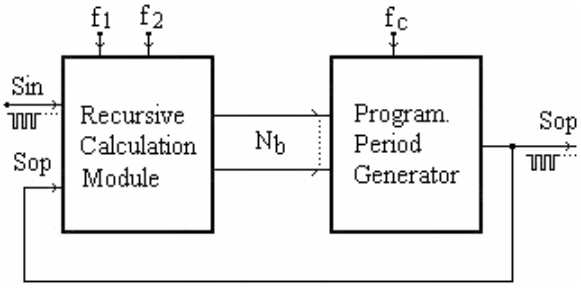


*Fig. 1. Organization of FLL according to* (2)

Providing the variables $f_c$, $f_1$ and $f_2$ represent the frequencies of three clock signals respectively $S_c$, $S_1$ and $S_2$, (2) discovers the way of realization of this system using electronic circuits. Since $f_c = 1/t_c$, $f_1 = 1/t_1$ and $f_2 = 1/t_2$, where $t_c$, $t_1$ and $t_2$ represent the corresponding periods of the clock signals, all members in (2) are the ordinary numbers. Equation (2) suggests that the input and output periods $TI_k$ and $TO_k$ are measured by the clock frequencies respectively $f_1$ and $f_2$, and, at the same time, that the next output period $TO_{k+1}$ is generated using clock frequency $f_c$. Following the given explanation, the principal scheme of electronic circuit, which corresponds to (2), is represented in Fig. 1. The Recursive Calculation Module (RCM) measures and makes addition of the periods TI and TO in binary form using clocks $f_1$ and $f_2$ at each discrete time. In other words, clock pulses with frequency $f_1$ are counted during period $TI_k$, and clock pulses with frequency $f_2$ are counted during period $TO_k$. Their sum, as binary number $N_b$, is applied to Programmable Period Generator (PPG) being used for the generation of the output period $TO_{k+1}$ at the next discrete time $t_{k+1}$. The functioning of PPG is described in details in [2,3,5]. Let us remember that PPG generates the output period $TO = N_d \cdot t_c$, where $N_d$ is the decimal value of binary number $N_b$, shown in Fig. 1. Binary word $N_b$ represents the sum of $TI_k/t_1$, and $TO_k/t_2$. $Sin$ and $Sop$ represent pulse rates with periods respectively $TI_k$ and $TO_k$ in Fig. 1. Clock signals $S_1$, $S_2$ and $S_c$ are preferably presented by their frequencies respectively $f_1$, $f_2$ and $f_c$ in Fig. 1.

### 2.2 Analyses of the output period for the step input

Before the description of the precise realization of (2) by the electronic circuit, it is necessary to analyze under

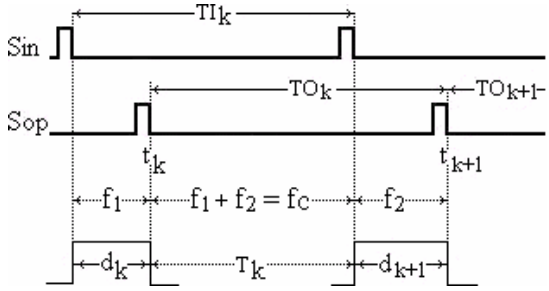


*Fig. 2. Time relation between the variables of FLL*

which condition the described system can own the properties of FLL. To do that, it is necessary to find the Z transform of (2):

$$f_c \cdot z \cdot [TO(z) - TO_0] = f_1 \cdot TI(z) + f_2 \cdot TO(z) \quad (3)$$

where $TO_0$ is the initial value of $TO_k$. $TO(z)$ can be calculated from (3) as:

$$TO(z) = TI(z) \cdot \frac{f_1/f_c}{z - f_2/f_c} + TO_0 \cdot \frac{z}{z - f_2/f_c} \quad (4)$$

In case that the step $Tl(k) = TI$ is applied to the input, $Tl(z)$ in (4) should be substituted by $TI \cdot z/(z-1)$ and using the inverse Z transform, the transient behavior of the output period in the function of "$k$" can be found out:

$$TO(k) = TI \cdot \frac{f_1/f_c}{1 - f_2/f_c} \cdot [1 - (\frac{f_2}{f_c})^k] + TO_0 \cdot (\frac{f_2}{f_c})^k \quad (5)$$

It yields from (5) that the proposed system has the properties of FLL if $\lim TO(k) = TI$, when $k \to \infty$. Equation (5) can satisfy the previous condition only if the system is stable, i.e. if the pole of the system $f_2/f_c < 1$, and if:

$$f_1 + f_2 = f_c \quad (6)$$

If condition given by (6) is met, the condition $f_2/f_c < 1$ is also satisfied.

### 2.3 Analyses of the time difference for the step input

Instead of the phase difference between the input and output signals, which is usually analyzed in classical PLL, it is more convenient to use the time difference $d_k$ between the input and output periods at discrete time $t_k$. The time relations between all variables describing FLL are shown in Fig. 2. The periods $TI_k$ and $TO_k$, as well as $d_k$, occur at discrete times $t_0$, $t_1$, $\ldots t_k$, $t_{k+1}$, which are defined by the falling edges of the pulses of $Sop$. The natural relation between the variables yields from Fig. 2:

$$d_{k+1} = d_k + TO_k - TI_k \quad (7)$$

To analyze the behavior of time difference "$d$" it is necessary to find the Z transform of (7):

$$z \cdot d(z) - z \cdot d_0 = d(z) + TO(z) - TI(z) \quad (8)$$

Changing $TO(z)$ from (4) to (8), it can be found:

$$d(z) = -\frac{TI(z)}{z - f_2/f_c} + \frac{1}{z-1}(TO_0 \cdot \frac{z}{z - f_2/f_c} + z \cdot d_0) \quad (9)$$

Providing that the step function $TI(k) = T$ is applied to the input, $Tl(z)$ in (9) should be substituted by $TI \cdot z/(z-1)$. Using the final value theorem, it is possible to find $d_\infty = \lim d(k)$ if $k \to \infty$, using $d(z)$:

$$d_\infty = \lim[(z-1) \cdot d(z)]_{z \to 1} \quad (10)$$

Applying (10), it yields:

$$d_\infty = \lim[d(k)]_{k \to \infty} = \frac{TO_0 - TI}{f_1/f_c} + d_0 \quad (11)$$

Note that, in addition to the input $TI$ and the FLL parameters $f_1$ and $f_c$, the final value $d_\infty$ depends on the initial conditions $TO_0$ and $d_0$. This fact means that the system cannot hold the properties of PLL. It operates only as FLL. It is of interest to find out the transient behavior of the time difference in the function of "$k$" in case that the step $Tl(k) = TI$ is applied to the input. If $Tl(z)$ in (9) is substituted by $TI \cdot z/(z-1)$ and using the inverse Z transform, the transient behavior of the time difference may be found out:

$$d(k) = \frac{TO_0 - TI}{f_1/f_c}[1 - (\frac{f_2}{f_c})^k] + d_0 \quad (12)$$

Note that the final value $d_\infty$, given by (11), can also be found out from (12). The final value $d_\infty = \lim d(k)$ if $k \to \infty$. It can be seen from (5) and (12) that the transient time of FLL is shorter for the smaller ratio $f_2/f_c$.

## 3 REALIZATION OF FLL

According to Fig. 2, it can be noticed that $TI_k = d_k + T_k$ and $TO_k = d_{k+1} + T_k$. Taking in account expressions for $TI_k$, $TO_k$ and relation $f_1 + f_2 = f_c$, (2) can be transformed into the next form:

$$f_c \cdot TO_{k+1} = f_1 \cdot d_k + f_c \cdot T_k + f_2 \cdot d_{k+1} \quad (13)$$

Note that, according to (13), it is possible to avoid the simultaneous measurement of $TI_k$ and $TO_k$. Instead of that, only one continues measurement of time i.e. first $d_k$ by frequency $f_1$, then $T_k$ by $f_c$ and at last the measurement of $d_{k+1}$ by $f_2$, will give the same result as the measurement

according to (2). These three time intervals are adjacent in Fig. 2. Obviously, it is necessary to generate each of them as separate interval, because every one of them is measured by the different clock frequency. The second important conclusion is that all intervals are to be summed before their total sum is entered into PPG. During interval $TO_k$, the total sum must be prepared for the next generation of $TO_{k+1}$. However, the interval $d_k$ does not belong to the period $TO_k$. It occurred before the discrete time $t_k$, when generation of $TO_k$ started. This suggests that the measured $d_k$ by $f_1$, must be memorized, and taken in account during the interval $TO_k$.

Generally, it is possible to measure and calculate the sum of $TO_{k+1}$ exactly according to (2), but the suggested approach with three adjacent intervals, enables the considerable saving in hardware realization of FLL. Following the described concept, the functional scheme of FLL is made and shown in Fig. 3. It consists of two Up-down counters, PPG and the additional logic. When addition of $d_k$, $T_k$ and $d_{k+1}$ is performed, the sum is from counter 2 preset to PPG using control pulse $P_1$. Up-down counter 1 is devoted to the measuring of the time difference $d_k$ at the discrete time $t_k$, but the Up-down counter 2 measures continuously, one after the other, time $T_k$ and time difference $d_{k+1}$, according to Fig. 2, at the next discrete time $t_{k+1}$. Before the measuring of $T_k$ and $d_{k+1}$, control pulse $P_2$ presets the previous measured $d_k$ from counter 1 to counter 2, so that the measurement of $T_k$ and $d_{k+1}$ makes, at the same, time addition of $d_k$, $T_k$ and $d_{k+1}$ in counter 2. Immediately after the presetting of $d_k$ is made, control pulse R is used to reset counter 1 and to prepare it for the measurement of the next "$d$". It can be seen from Fig. 3 that the measurement of $d_k$, using logic circuits, is performed by the clock of frequency $f_1$, the measurement of $T_k$ and $d_{k+1}$ are performed by the clocks of frequencies respectively $f_c$ and $f_2$, exactly according to the previous analyses. Note that every time difference "$d$" is measured instantaneously twice, by the clock of the frequency $f_1$ and at the same time by the clock of frequency $f_2$.

The control pulses P1, P2 and R are differentiated pulses which occur one after the other on the falling edge of the output pulses, shown in Fig. 3. The widths of the control pulses must be very small, so that they do not effect to the accuracy of the measurement of "$d$" and "$T$".

For the realization of Up-down counters number 1 and 2 and PPG, 4-Bits Binary Up-down counter CD 40193 are used. Each of these eight bits modules consists of two 4-Bits CD 40193 circuits connected in cascade. All functional inputs and outputs shown in Fig. 3 are defined according to the functional properties of digital circuit CD 40193. Logical one is signed by "1" in Fig. 3. The control pulses P1, P2 and R are generated by the mono-stable

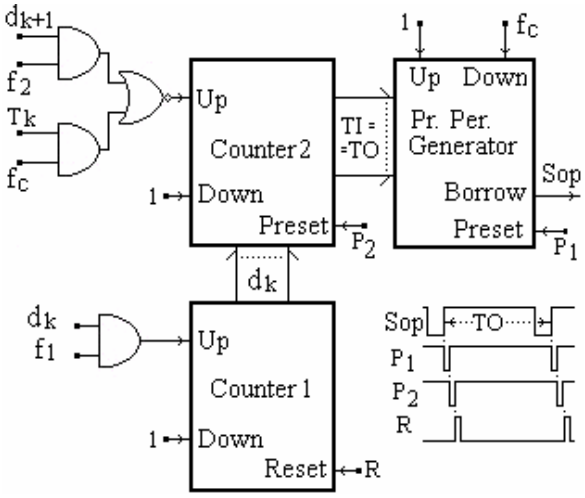


*Fig. 3. The functional scheme of FLL*

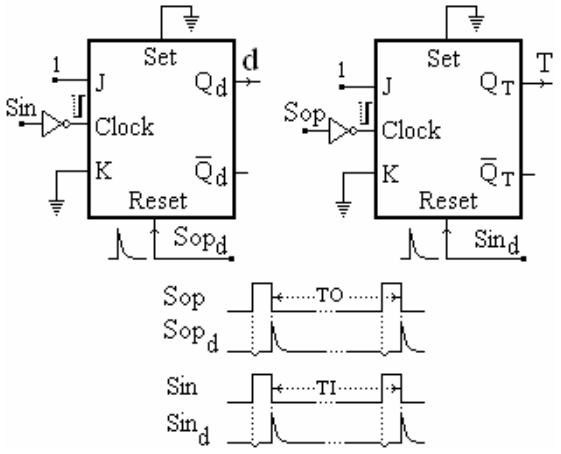


*Fig. 4. The generation of d and time interval T*

multivibrators. They can also be generated by RC differentiators.

The generation of time difference "$d$" and time interval "$T$" is represented in Fig. 4. For this realization JK Flip-flops CD 4027 are used. The inputs JK of the Flip-flops are chosen so that arising edge on the clock input sets Flip-flops. The falling edges of $Sin$ and $Sop$ pulses are differentiated by RC differentiators. The differentiated pulses $Sin_d$ and $Sop_d$ reset Flip-flops, generating in that way the time difference "$d$" and the time interval "$T$" at theirs outputs. All functions of trigger edges are adopted in Fig. 4 according to the properties of the Flip-flop CD 4027.

The described hardware organization will enable the locking of the output period to the input period in the way shown in Fig. 2, where the output signal $S_{op}$ is delayed


*Fig. 5. Sin, Sop and Sc recorded on the stable FLL*

in comparison to the input signal $S_{in}$. Note that, according to (7), the time difference "$d$" can change sign during the locking procedure. To take care about the sign of "$d$", it is necessary to add sign generator. The sign generator will have two states. One state corresponds to the case when two pulses or more pulses of $S_{in}$ occur during one period of $S_{op}$. The second state corresponds to the case when two or more pulses of $S_{op}$ occur during one period of $S_{in}$. These two states are easy to detect electronically. The sign of the time difference "$d$" will take opposite value in these two situations. The output of the sign generator will be consequently used in the locking procedure. FLL can reach the stable state without the sign generator, but in some application the sign generator might be required, if the locking procedure is to be controlled in every step.

One eight-bit model of the proposed FLL is realized for the parameters $f_1 = f_2 = f_c/2$. The oscilloscope picture recorded on the realized model is shown in Fig. 5. The picture shows that the output period is locked to the input period, but the phase difference between $Sin$ and $Sop$ is not equal to zero. This property is consistent with the previous description of FLL. The pole for the realized FLL $f_2/f_c = 0.5$. Digital control of $f_2/f_c$ can be easily implemented in various ways, so that FLL may be adaptable for use in the different real time applications.

## 4 SIMULATION OF FLL LOCKING PROCEDURE

The simulation of FLL functioning has two important aims. The first one is to discover additional properties of FLL and its possible efficient applications. The second one is to enable better insight into the procedure and physical meaning of the variables described, as well as to prove the mathematical analyses described. All discrete values in simulations are merged to form continuous curves. All simulations are made using technical computing language Matlab.

### 4.1 Simulation of output period and time difference

The simulation of the output period $TO(k)$, and the time difference $d(k)$, according to (2) and (7), for different value of the FLL parameters are shown respectively in Fig. 6 and Fig. 7. The initial conditions for the locking procedure are shown in Figs. It can be seen in Fig. 6 that the input period $TI(k)$ is the step consisting of 10 time-units (t.u.). Note that time-unit can be, $\mu$sec, msec or any other, assuming the same time-units for $TI(k)$ and $TO(k)$. The output period $TO(k)$ tends to $TI(k)$, but the speed of the locking procedure depends on the relation $f_2/f_c$. The lower $f_2/f_c$ performs the faster locking procedure. The simulated results agree with (5). The locking procedure of the time difference $d(k)$ in Fig. 7, is also faster for the lower value of $f_2/f_c$. (or higher value of $f_1/f_c$). Note that the simulation of $d(k)$ is identical to the calculations of (12) and $d_\infty$ agree in all cases with calculation according to (11). The shown simulations prove the correctness of the mathematical analyses.

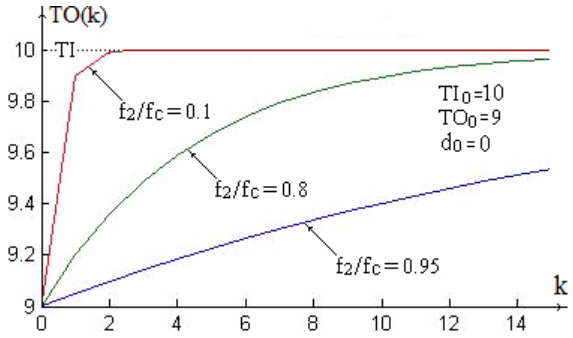


*Fig. 6. The lower $f_2/f_c$ enables the faster locking*

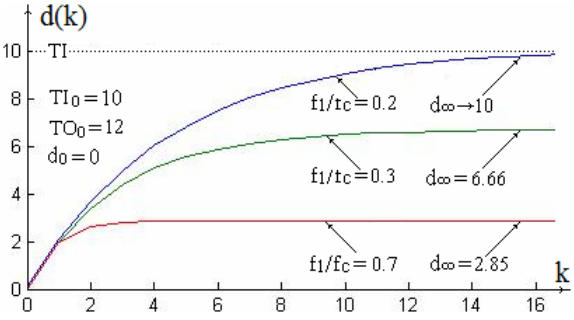


*Fig. 7. The simulated $d_\infty$ agree with $d_\infty$ given by* (11)

The simulation of $TO(k)$ and $d(k)$ for the same locking procedure, for $TI = 10$ t.u. is shown respectively in Fig. 8a and 8b. The initial conditions are presented in Fig. 8. For better understanding of this physical process, the real time locking procedure of pulse rates $Sin(k)$, $Sop(k)$ and $d(k)$ and relations between them are presented in every step in Fig. 8c. All calculated values agree with shown curves for $TO(k)$ and $d(k)$. In the locking procedure $TO(k)$ tends to $TI = 10$ t.u., and $d(k)$ tends to 5 t.u. The results shown in Fig. 8 agree with (5), (11) and (12).

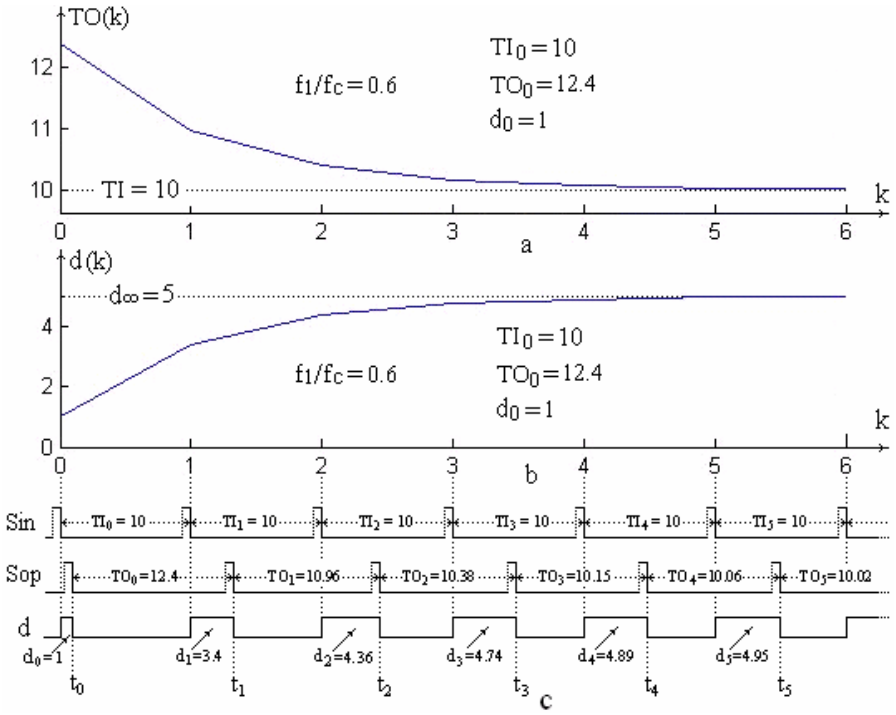


*Fig. 8. Simulation of $TO(k)$; b. Simulation of $d(k)$; c. Locking procedure of $TO(k)$ and $d(k)$ in real time*

### 4.2 Noise rejection ability of FLL

The noise rejection ability of FLL is presented in Fig. 9. The input period $TI(k)$ is the step consisting of 10 time-units, which is strongly corrupted by uniform distributed noise. The amplitude of noise is 10 time-units peak to peak. The rejection of noise at the output period $TO$ is very powerful for the parameter $f_2/f_c = 0.95$. For the value $f_2/f_c = 0.9$, effect of noise suppression is weaker. For the value $f_2/f_c = 0.85$, the suppressed noise in the output period is about 60% of the noise in the input period. The lower value $f_2/f_c$ provides the lower noise rejection effect.

It is very simple, but useful for the practice, to explain how FLL rejects noise physically. Looking the main recursive algorithm given by (2), it can be noticed that the number $f_c \cdot TO_{k+1}$, which represent the next period $TO_{k+1}$, consist of two parts. The first one $f_1 \cdot TI_k$ is strongly corrupted by noise. The second one $f_2 \cdot TO_k$ is pure. If $f_2$ is much greater than $f_1$, the noise is suppressed. But, for this case, $TO_{k+1}$ takes a large number of steps to reach $TI$.

### 4.3 Tracking ability of FLL

The tracking ability of FLL is presented in Fig. 10. The input period $TI(k)$ is the ramp function given by $TI(k) = 2 + 0,3 \cdot k$ [time units]. The first conclusion is that the output period of FLL can track the ramp function at the input, but with the constant error. This error is consistent with the properties of FLL of the first order. The second conclusion is that the constant error and the tracking transient time are lower if $f_1/f_c$ is greater. In other word, since $f_1/f_c + f_2/f_c = 1$, the constant error and the tracking transient time are lower for lower value of $f_2/f_c$.

If one takes in account the previous results that the lower value $f_2/f_c$ provides the lower noise rejection effect, it means that it is impossible to realize FLL which would own the maximum abilities for the noise rejection, tracking and short transient speed, at the same time. For instance, let us consider the applications where the measurement of the input period is required in the tracking mode of FLL and in the presence of noise. Note that the higher $f_1/f_c$ provides the lower tracking error and the faster measurement of TI, but it also contributes to the lower noise rejection effects. In these applications one has to make the trade of the parameters $f_1$ and $f_2$, in order to adopt FLL to the specific requirements.

## 5 CONCLUSION

The description and illustrations of the realized FLL of the first order represent a new approach to design and construction of FLL in both theoretical and practical sense. It discovers the way of the development, implementation,

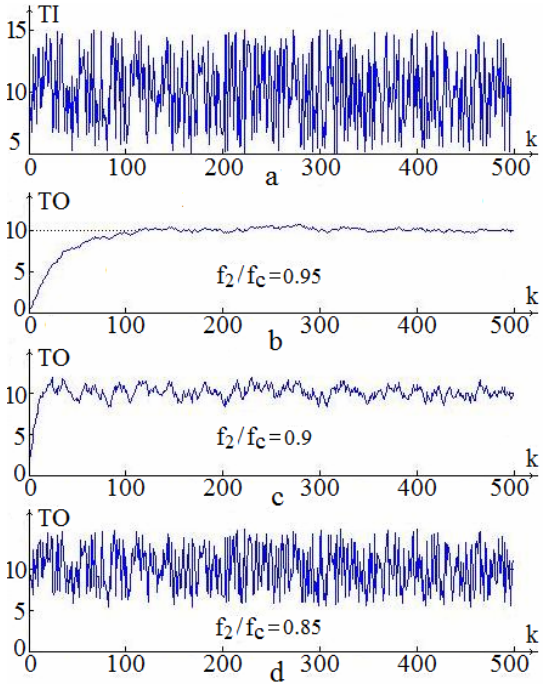


*Fig. 9. The noise rejection performance of FLL; a) The input step is strongly corrupted by noise; b, c and d) The rejection of noise is very powerful for $f_2/f_c = 0.95$. The lower value $f_2/f_c$ provides the lower noise rejection effect*

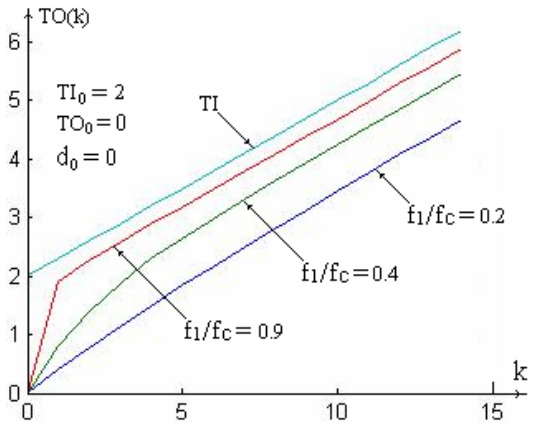


*Fig. 10. The higher $f_1/f_c$ provides the lower tracking error and the faster locking procedure*

analysis and application of the recursive FLL based on measurement and processing of the input and output periods.

In comparison with the existing approaches of FLL and PLL in the literature, the approach described in this paper represents one fundamentally different approach to theory, design, methods of description, processing and analysis. It also represents a novelty in the way of measurement of error and in the way of functioning and realization of FLL components. For instance the error and the output of FLL or PLL, which are usually respectively phase and frequency, are changed by the time difference and the output period. The input frequency is changed by the input period. All the measurement of the phase, the amplitude and the frequency difference in the existing approaches of FLL and PLL are changed by the measurement of time. Note that the time measurement is more convenient, easier and the most precise in the comparison with the measurement of the phase, the frequency or the amplitude, which are used in the existing approaches of FLL and PLL.

The parameters of FLL represent the frequencies of three clock pulse rates. These frequencies have to be in defined relation for the stable FLL. If these frequencies are changeable, they provide a wide range of properties of FLL.

The analyses and simulations showed that FLL is suitable for the noise suppression, for the different predicting and tracking applications and for the measurements of the frequency of the input signal in the noise environments. It can be also used for the other usual applications of FLL and PLL.

The recursive processing is realized without the classical digital filters, enabling the simple realization of all FLL components. The described recursive model enables the tracking and the controlling of the transient flow in each step of FLL. This makes FLL compatible with the different digital system. This also makes FLL suitable for some applications where FLL is to be adaptive and controlled by the other system.

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