A 0.5V Time-Domain Instrumentation Circuit with Clocked and Unclocked $\Delta\Sigma$ Operation

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***Abstract*— This paper presents a time-domain instrumentation circuit with exceptional noise efficiency directed at using nano metre CMOS for next generation neural interfaces. Current efforts to realize closed loop neuromodulation and high fidelity BMI prosthetics rely extensively on digital processing which is not well integrated with conventional analogue instrumentation. The proposed time-domain topology employs a differential ring oscillator that is put into feedback using a chopper stabilized low noise transconductor and capacitive feedback. This realization promises better digital integration by extensively using time encoded digital signals and seamlessly allows both clocked & unclocked $\Delta\Sigma$ behavior which is useful on-chip characterization and interfacing with synchronous systems. A 0.5 V instrumentation system is implemented using a 65 nm TSMC technology to realize a highly compact footprint that is 0.006 mm^2 in size. Simulation results demonstrate an excess of 55 dB dynamic range with 3.5 μV$_{\text{rms}}$ input referred noise for the given 810 nW total system power budget corresponding to an NEF of 1.64.**

***Index Terms*—Neural recording, Instrumentation, VCO, Time-domain, Asynchronous logic, Low noise, Delta-Sigma.**

I. Introduction

Recent efforts to realize brain machine interfaces (BMI) target fully integrated neural recording systems that use advanced CMOS technologies to enable real time diagnostics for hundreds of channels simultaneously. This emerging trend is predominately motivated by the extensive use of digital techniques applied to robust therapeutic feedback for closed-loop neuromodulation and signal compression/feature extraction in high channel count BMIs for prosthetic motor control [1]. However there are a growing number of challenges associated with integrating analogue instrumentation for these digital systems due to the loss in analogue transistor characteristics which has motivated the use of time domain (TD) analogue [2]. TD systems encode information with respect to the timing intervals of asynchronous digital signals to perform mixed signal processing while extensively using standard logic and oscillators that do not suffer from analogue complications. Many recent publications will indicate the potential for exceptional dynamic range like in the recording system of [3] or highly compact instrumentation like the potentiostat in [4]. We argue that a key advantage for these systems is that supply voltage is utilized more effectively from a fundamental aspect without being impeded by linearity. This allows an aggressive reduction in power dissipation. Furthermore realizing band limiting filters outside the instrumentation loop prevents KT/C relations from limiting the compactness of the system. This work presents a TD instrumentation topology for neural recording applications that targets ultra-low power operation and a highly compact implementation for miniaturized multichannel systems. Based on previous work in [5], which uses a third order feedback loop to digitize the signal asynchronously, this realization exhibits only one dominant pole and thus reduces the resources spent on achieving stability. While [5] can achieve a smaller footprint than the topology presented here the feed-forward structure cannot achieve high dynamic range as the high frequency quantization noise and out of band distortion from the counter cannot be suppressed without additional filtering. Our current efforts aim to realize the system architecture illustrated in Fig. 1. This approach aims to use the efficiency of TD processing techniques to extract features from neural recordings which promise an order of magnitude improvement over conventional implementations [6]. In fact such a TD approach has already been applied to acquire wireless radio signals with a versatile activity dependent power dissipation [7]. However there will be numerous scenarios where these asynchronous structures must interface with clocked systems to effectively perform calibration or other discrete time analysis. For this reason we specifically consider how the class of circuits presented here and in [6] can seamlessly realize a more traditional clocked $\Delta\Sigma$ oversampling loops. This is relevant because time encoded signals have a very broad bandwidth of several GHz making it unreasonable to characterize or communicate a large number of them off chip. Finding effective means to convert such time-encoded signals to a clocked and quantized equivalent is crucial for fully integrated systems. This paper is organized as follows; First the basic structure of the proposed circuit

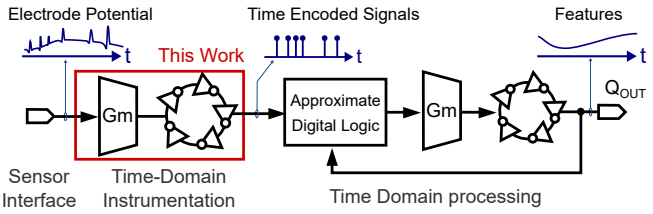

Fig. 1. TD system architecture for BMI systems where both the instrumentation and processing sub-blocks manipulate time-encoded signals to perform feature extraction from bio-signal recordings. This paper will present the instrumentation sub-system.

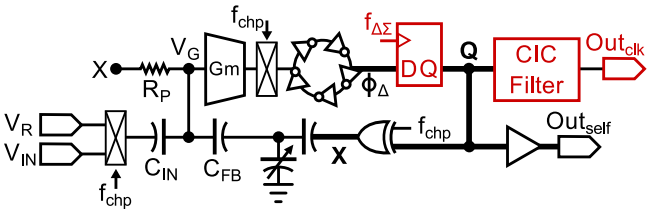

Fig. 2. The proposed chopper stabilized instrumentation system that uses a ring oscillator to realize TD based first order integration with respect to the output phase difference which is then quantized in time and decimated using a CIC filter.

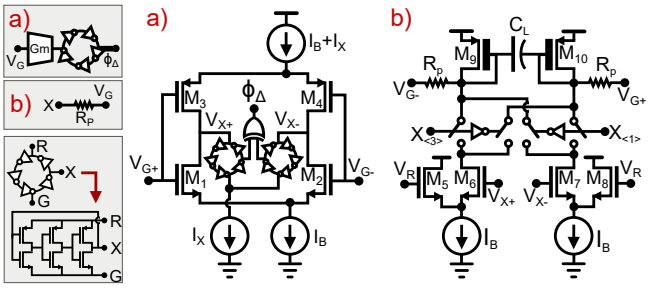

Fig. 3. Transistor level implementation of a) the low noise amplifier and b) high pass filter circuit that removes flicker noise and off-set. A legend is presented in gray showing how a) & b) relate to Fig. 2 and the chopper in a) is omitted for clarity.

is introduced in Sec. II which motivates the general topology chosen here. Then in Sec. III we shall detail the circuit level implementation and identify important design considerations. Finally Sec. IV presents the preliminary simulation results which leads to the conclusions in Sec. V.

II. Time-Domain Instrumentation Architecture

The proposed configuration is shown in Fig. 2 as a single ended equivalent of the fully differential system implemented here. The neural signals picked up on V_{IN} include local field potentials of several millivolt and extracellular action potential from nearby neural tissue with 100 microvolt amplitudes where the total bandwidth of interest here is from near DC to 6 kHz [1]. Using a reference electrode these components are first chopped to a higher frequency f_{chp} at 100 kHz. This is then passed into a capacitive network that allows the digital output signal Q to be directly feedback onto the input after using a XOR gate realize chopper modulation. The intermediate node V_G is tapped off to a transconductive cell which advances/recedes the phase of a multi stage ring oscillator structure after the signal is chopped back to the base band. By referencing the phase of this oscillator to another oscillator we can realize the time-encoded digital signal that encodes the phase difference ϕ_{Δ} as pulse width modulated information. Then we may either quantize this signal with a register in the time domain or simply buffer it onto Q to provide asynchronous feedback without time quantization. Now the near-DC aggressors such as off-set and flicker noise from the transconductor are neutralized using the feedback loop through R_p which presents a high pass response for signals below the chopper frequency on node V_G. If we simply take the transconductor, oscillator, and digital logic to represent some kind of integrator then the high level instrumentation topology reduces to a relatively simple chopper stabilized circuit. Finally in the synchronous case where time is quantized, the output Q is passed into a second order cascaded integratorcomb (CIC) filter that decimates oversampled signals into discrete samples. Otherwise ϕ_{Δ} is simply passed onto other TD processing structures which is outside the scope of this paper. We highlight the fact that the high pass feedback uses the output referred signal. This has a profound effect on how the noise profile of R_p appears at the chopper frequency when referred to the input. In fact if R_p was tied to a biasing voltage to set V_G then resistor's noise will have a rms power of $\sqrt{kT/C_{IN}}$ at the input that is up modulated and will corrupt the linearity of the integrator. This can be very substantial because C_{IN} is reduced to 100 fF in order to boost the input impedance that depends on the chopping frequency as $R_{IN}=1/(f_{chp}C_{IN})$. This feedback configuration reduces this noise component as a function of closed loop gain A_{cl} which is maximized as we realize all the necessary signal gain in a single analogue processing stage. Moreover the chopper stabilization allows an aggressive reduction on input transistor size which is important for reducing parasitics on the node V_G. Any parasitic loading here can prevent further reduction in C_{IN} because it would degrade the noise performance. The PWM signals ϕ_{Δ}, Q, and X in Fig. 2 are illustrated in bold because they represent multiphase time-encoded signals by simultaneously taping off multiple phases inside the oscillator and using them in parallel. The capacitive feedback network sums these signals to acquire an analogue equivalent where the number of amplitude quantization levels is 1+N for N phases used in parallel. This is an important point because the error signal on V_G is a function of the supply voltage as $V_{DD}/(N\ A_{cl})$ which must lie well within the linear range of the transconductor. Adding to the fact that supply noise is also inversely proportional to A_{cl} reveals that although we can reduce power by reducing V_{DD}, this parameter is tightly coupled to other performance requirements. In fact using the definition of noise efficiency factor NEF from [8] one can derive the following expression to predict the system power P_{sys} for noise limited systems:

$$P_{sys} = V_{DD}\,\omega_{3dB}\frac{kT\,U_T}{e_{in}^2}NEF^2 \qquad (1)$$

Eq. 1 uses ω_{3dB}, kT, U_T, and e^2_{in} as the signal bandwidth in radians, Boltzmann energy, thermal voltage, and input referred noise power. This expression ignores any constraints due to sampling noise or capacitor sizing that could suffer as the supply voltage decreases. However it clearly illustrates our motivation for reducing power through V_{DD} which is allowed in this fashion only if no band limiting behavior is required from the instrumentation loop. In fact an important contribution here is that a near ideal NEF is achieved for the TD structure using the proposed implementation.

III. Circuit Implementation

The fully differential analogue part of this system is shown in Fig. 3. Here two analogue structures are shown, one for signal amplification that integrates on the differential phase ϕ_{Δ} which we shall consider the amplifier. The second structure presents the pseudo resistor that rejects the low frequency aggressors that are being up modulated onto the output Q which we will refer to as the high pass filter. The amplifier is composed of a complementary transcondutor to boost the noise efficiency and is loaded by two ring oscillators that are biased with a current I_X that is 16x smaller than I_B such that the input referred noise from the oscillator to V_G is greatly reduced. A XOR gate is used to compute the phase difference of the two oscillators because it does not have a discontinuity in its phase to PWM characteristic. The floating ground of both oscillators is tied together to reject common mode noise and minimize any coupling to the analogue power supplies. Actually, the high pass filter not only performs feedback but also determines the common mode input voltage on V_G. This mechanism is used to set the common mode on V_X to V_{CM} using the transistors M5-M8. This is important because the oscillator needs to run in the middle of the rail to allow more efficient conversion from the small internal voltage oscillation of 300 mV to a digital signal with full swing. The reason a current DAC is used to drive the pseudo resistors is because the linearity of these devices is important and R_p can only handle $\pm$100 mV if simple diode connected devices are used. This is why C_L is introduced to provide some filtering and minimize distortion from the high frequency PWM feedback. Note that because all transistors will use subthreshold operation the threshold voltage V_{TH} difference between the input PMOS pair M3-M4 and the high V_{TH} devices M9-M10 will represent voltage headroom of the PMOS current bias which should at least be 100 mV. Now there is quite a significant impact from using an oscillator as load for the amplifier structure in this particular fashion. It may be obvious that there are no high impedance analogue nodes in this configuration that could introduce undesirable poles. But more importantly we do not need to provide extra voltage headroom or a second gain stage to let our output signal vary with maximum amplitude. This proposed implementation allows both simplicity and high power efficiency. In this case the oscillator mostly reuses the V_{TH} voltage headroom needed by the NMOS input transistors. This raises an interesting question; what limits the required voltage headroom for this circuit? Typically the complementary structure necessitates that the source drain voltage of the current bias transistors and differential pairs is sufficient to provide good channel resistance. However there is another component with regard to the noise generated by the oscillator that should be considered in terms of the oscillator voltage overhead V_{RO}. Consider the noisy charge induced as sampling noise from one of the oscillators on each inverter gate capacitance C_{gate} before the up/down transition as residue from the previous cycle. This can be represented by an equivalent noisy current source $\mathbf{i}^2_{smp}$ using the oscillator frequency f_{osc} as formulated in Eq 2.

$$i^2_{smp} = 2N\, f^2_{osc}\, kT\, C_{gate} \tag{2}$$

Referring this component to V_G as input referred voltage noise equivalent $\mathbf{v}^2_{smp}$ requires f_{osc} to be represented in terms of total charge dissipated each cycle f_{osc}=I_X/(2N V_{RO} C_{gate}). Taking the transconductance of the amplifier approximately as Gm$\approx$2I_B/(η U_T) will resolve the expression as in Eq 3 using η and U_T as slope factor and thermal voltage.

$$v^2_{smp} = \frac{i^2_{smp}}{Gm^2} = \frac{2\,kT}{P_{osc}} \left(\eta\, U_T \frac{I_X}{2\, I_B}\right)^2 \tag{3}$$

This result may be surprising in some sense because indicates the oscillator should dissipate a strict amount of energy to avoid this noise component from being significant. The only way to do this is by increasing the V_{RO} because increasing its bias current I_X will in fact degrade the input referred noise. Also notice that the actual capacitive load of the oscillator does not impact the thermal noise floor although it is directly related to the bandwidth of operation. In this particular case we configured the oscillation frequency to be around 300 kHz after optimization which implies that the effective frequency is around 1.5 MHz given the 5 phases. For this reason when the CIC filter is enabled we use a 3 MHz system clock for time quantization and an over sampling ratio of 128. This implies that the instrumentation bandwidth will be limited to 11 kHz sampled at exactly 22 kS/s.

IV. Simulation Results

The presented implementation was fabricated using the commercially available TSMC 65 nm CMOS LP MS RF technology (1P9M 6X1Z1U RDL). This system can operate at 0.5 V by extensively using the different V_{TH} process options for the standard transistor. Fig. 4 shows the floor plan and final fabricated device and the MIM capacitors covering the active area. A compact configuration was achieved with a 0.006mm^2 footprint where future work could potentially share the biasing and digital filter resources. Our preliminary results consist of post layout noise simulations that should have a good degree of precision for predicting the expected bench top measurements. Fig 5 shows the ring oscillator output with 200 mV amplitude in the middle of the rail that is fed to the XOR gate to produce the full swing digital signal ϕ_{Δ}. Fig 6 shows the output of the circuit in the frequency domain before & after decimation by the CIC filter. We can observe that linearity is quite easily achieved due to the exceptional loop gain from the TD integrator and because all analogue nodes exhibit a small signal swing. The performance summary in Table I compares this work to recently published instrumentation systems using the 65nm or 90nm technology node. Notice that a comparable noise performance is achieved for a similar if not better input dynamic range while the NEF & area characteristics are respectable given the extra capability that signal quantization is also performed. The input resistance due to chopping for this configuration is estimated to be 57 MΩ

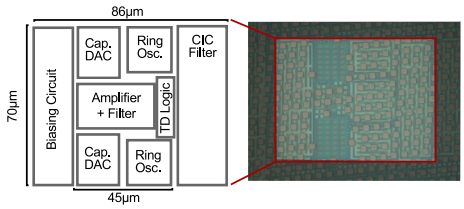

Fig. 4. The floor plan and micro photograph of the fabricated TD instrumentation prototype.

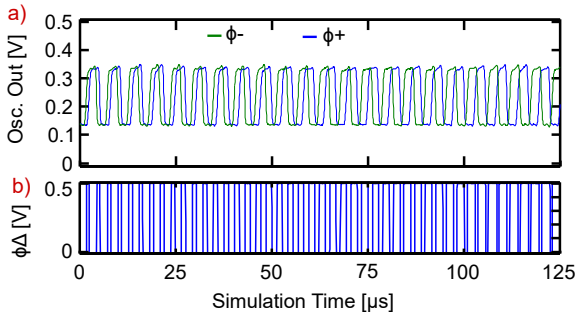

Fig. 5. Simulation results showing a) the two ring oscillator outputs & b) the respective phase difference signal due to a 5 mVpp sinusoidal signal at 2 kHz at the input of the instrumentation system.

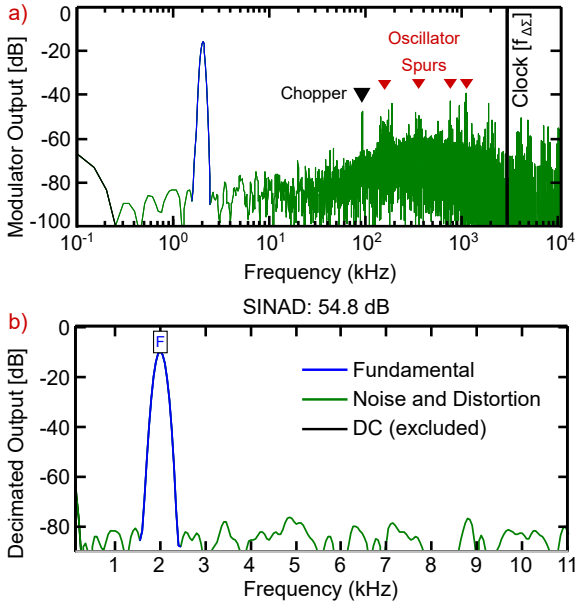

Fig. 6. Spectral characteristics of a) the $\Delta\Sigma$ modulator and b) the CIC filter output due to a 2 kHz 5 mVpp sinusoidal input showing a precision of 54.8 dB SINAD and no visible harmonics due to distortion.

which will be sufficient for most integrated neural recording electrodes.

V. Conclusion

This work realizes a chopper stabilized $\Sigma\Delta$ modulator right at the sensor interface using a time-domain topology for ultra low voltage operation. The proposed oscillator based instrumentation circuit addresses a number of the challenges associated with instrumentation using nano metre CMOS technologies. This system has a power budget of 810 nW and a compact silicon foot print of 0.006 mm^2. Moreover this system can achieve a NEF of 1.64 while including the power dissipation due to quantizing the signal with 8.8 effective number of bits at 22 kS/s.

TABLE I
Performance summary and comparison with state of the art.

Specification	This Work∗	[9]	[10]	[11]
Modality	Time	Volt.	Volt.	Volt.
Technology	65nm	90nm	65nm	65nm
Supply [V]	0.5	1	1	1
Supply [A]	1.62μ	2.85μ	1**n**	3.28μ
Gain [dB]	45	59	32	52
Bandwidth [Hz]	11 **k**	10.5 **k**	370	8.2 **k**
SINAD [dB]	55	>40	57	>40
IRN [V_{rms}]	3.5μ	3.04μ	26μ	4.13μ
NEF	1.64†	1.93	2.1	3.19
Area [mm^2]	0.006⋆	0.137	0.168⋆	0.042

⋆ Includes ADC area. † Includes power for quantization.
∗ Based on preliminary simulation results.

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