A Low Hardware Complexity Time Domain Quantizer for Wideband Multibit $\Sigma\Delta$ ADCs

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***Abstract*—This paper presents proof of concept of a low hardware complexity time domain quantizer (TDQ) for wideband multibit countinuous time (CT) $\Sigma\Delta$ ADCs. Besides rendering multi-level quantization of the input signal, the proposed scheme generates a two-level loop feedback signal for the modulator. The two-level feedback eliminates the errors emanating from component mismatches in the feedback digital-to-analog converter (DAC) due to process variations. The complete scheme is modeled using Simulink (MATLAB) and is validated through simulation. A 2^{nd} order $\Sigma\Delta$ modulator incorporating the proposed TDQ achieves a dynamic range of 45.7 dB for a bandwidth of 10 MHz and an input sine-wave of -5.78 dBFS amplitude.**

I. Introduction

Oversampling compounded with the noise-shaping capability, makes $\Sigma\Delta$ ADCs the most hankered choice in high-resolution applications [1]. These two characteristic features endow them with superior linearity, reduced anti-aliasing filtering requirements and straightforward analog implementation. Small feature size, low parasitic capacitances, lower power supply levels and high clock rates characterize contemporary and future VLSI technologies. Also, Pelgrom's mismatch model relates the local fluctuations of any device parameter under scaling to an area term, i.e., mismatch $\sim \frac{1}{\sqrt{WL}}$ [2] [3]. It implies that narrow devices show more mismatch and scaled VLSI technologies are more likely to be afflicted by poor component matching. In this regard a $\Sigma\Delta$ modulator, which offers greater immunity to circuit nonidealities and component mismatches, due to oversampling and their noise shaping behavior, becomes the most apt candidate for the implementation of high resolution ($\geq$ 16 bits) ADCs in scaled VLSI technologies. The modulator has proved its superiority specially for applications where the motive is digitization of overall signal, or "*signal acquisition*", rather than "*sample-by-sample data acquisition* "[4]. Moreover, $\Sigma\Delta$ ADCs offer more degrees of freedom for design (viz. order of the loop filter, oversampling ratio and the resolution of the internal quantizer) compared to other ADC architectures, hence easing the design procedure involving different trade-offs.

Depending upon whether the sampling is done before or within the loop, $\Sigma\Delta$ modulators can be categorized into discrete-time (DT) and countinuous-time modulators (CT). DT modulators sample the signal just before the modulator loop and are implemented using switched capacitor circuits. For a continuous-time modulator, sampling is done just before the internal quantizer and is implemented using RC filters. The CT modulators have an edge over DT modulators in the following terms : (i) relaxed settling requirement for the integrators, making them more suitable for high frequency applications [6] (ii) the CT loop renders additional anti-aliasing for the input signal [5](iii) lower thermal-noise contribution of the integrator stages [6] (iv) avoids the use of switches, hence reducing the burden of implementing efficient switches in low-end technologies [7] (v) exhibit lower figure of merit (FOM) and are more area efficient [9].

Based on the resolution of the internal quantizer the $\Sigma\Delta$ modulators can be categorized into single bit (the internal quantizer is a comparator generally) and multibit (the internal quantizer is a multibit ADC e.g. flash, SAR, etc.) modulators. Single bit quantizers (only two levels of quantization) are inherently linear and exhibit insensitivity to process and component variations, achieve better figure of merit (FOM) and are more area efficient compared to their multibit counterparts [8][9]. Advantages of a multibit topology over the single bit counterparts are as follows: (i) increment in overall dynamic range (DR) by roughly 6dB per bit of the internal quantizer (ii) alleviates the effect of idle tone and noise pattern (iii) increased randomness of the quantization noise makes the analysis using white noise approximation more valid (iv) better stability, hence higher order NTFs can be utilized (v) works with a smaller OSR (for a target SNDR) leading to a lower complexity decimation filter, reduces power consumption of both the modulator and corresponding decimation filter, and hence apt for wideband applications [4] [10].

Taking cue from the above discussion, CT modulators have been employed to design effcient multibit wideband converters to bring together the individual advantages of the CT and multibit topologies [11]. However, multibit designs are limited by the strict accuracy requirements on the feedback DAC, emnating from the process and component mismatches. To explicate the effect of DAC errors on the output of the modulator, a linearized model of a $\Sigma\Delta$ modulator is shown in Fig. 1. The loop filters, $H_1(z)$ and $H_2(z)$ are defined as

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$$H_1 = \frac{0.5 * z^{-1}}{(1 - z^{-1})}; \quad H_2 = \frac{2 * z^{-1}}{(1 - z^{-1})} \tag{1}$$

All the error/noise sources viz. $N_1(z), N_2(z), N_3(z)$ and $N_4(z)$, depending on the where they appear within the loop, are included as independent inputs, similar to the desired signal $P(z)$. The transfer function of the modulator's output, $Q(z)$, with respect to each of the mutually independent inputs are

$$STF(z) = \frac{Q(z)}{P(z)} = \frac{H_1 H_2}{1 + H_1 H_2 + H_2} = z^{-2} \tag{2}$$

$$NTF_1(z) = \frac{Q(z)}{N_1(z)} = \frac{H_1 H_2}{1 + H_1 H_2 + H_2} = z^{-2} \tag{3}$$

$$NTF_2(z) = \frac{Q(z)}{N_2(z)} = \frac{H_2}{1 + H_1 H_2 + H_2} = 2z^{-1}(1 - z^{-1}) \tag{4}$$

$$NTF_3(z) = \frac{Q(z)}{N_3(z)} = \frac{1}{1 + H_1 H_2 + H_2} = (1 - z^{-1})^2 \tag{5}$$

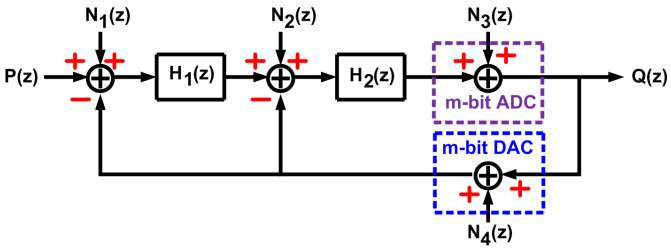
$$NTF_4(z) = \frac{Q(z)}{N_4(z)} = -\frac{H_1 H_2 + H_2}{1 + H_1 H_2 + H_2} = -z^{-1}(2 - z^{-1}) \tag{6}$$

where, STF is the signal transfer function and NTFs are the noise transfer functions. Magnitude plots for all the NTFs are shown in Fig. 1. The plots clearly show that noise-shaping increases from $NTF_1(z)$ to $NTF_2(z)$ to $NTF_3(z)$, which implies that the in-band power of a source of error in the forward path of the loop will decrease with an increase in the proximity of the source and quantizer. Moreover, since the error in the feedback path $NTF_4(z)$ is added directly to the input, it passes on to the output of the modulator without any shaping. The error due to component mismatch in the DAC corresponds to $NTF_4(z)$ here. Therefore the overall accuracy of the modulator is no better than than that of the feedback DAC. Also, assuming a Gaussian distribution for variation of the actual value of each unit element (capacitors, resistors, current sources, etc.), the worst-case relative error in a *B*-bit DAC output can be estimated as

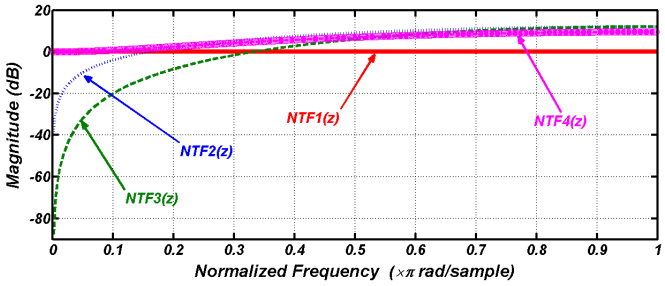
$$\sigma\left\{\frac{\Delta y}{y}\right\} = \frac{1}{2 * \sqrt{2^B}} * \sigma\left\{\frac{\Delta U_e}{U_e}\right\} \tag{7}$$

where, $\frac{\Delta U_e}{U_e}$ is the relative error in the unit element used to reconstruct the analog feedback signal [12][19].

A typical lithographical renders a component matching of 0.1-0.5% ($\sim$ 8-10 bit resolution) [14]. To achieve a higher resolution, Flash ADC, if used as the internal quantizer in the modulator, necessitates trimming of the intermediate reference levels [15]. But trimming requires additional circuitry. Also the comparators require additional offset correction [16]. [17] replaces flash ADC with SAR ADC as the internal quantizer of the modulator. Important techinques to correct the DAC error are as follows : (i) external trimming [18] [19] (ii) utilizing two different DACs, one single bit and other multibit [20] (iii) multibit quantization



(a) Linearized model of a $2^{nd} order \Sigma\Delta$ modulator.



(b) Magnitude plots for all NTFs.

Fig. 1. A simple model of a $\Sigma\Delta$ modulator to understand the effect of relevant noise sources on the modulator's output.

but single bit feedback [21] (iv) digital error correction [14][4][22][23][24] (v) various data element matching techniques (DEM), like randomization algorithms [25], clocked averaging [26], individual level averaging (ILA) [27], data weighted averaging (DWA) [28], data directed scrambling (DDS) [29], vector-quantizer structures [30]. Lately to circumvent the problem of DAC non-linearity, there has been an inclination to shifting the voltage-domain signal processing to time-domain processing. This scheme exploits the usage of arbiters (i.e., flip-flops) in place of comparators making it suitable for advanced CMOS technologies with low supply voltage and fast switching speed[31]. Numerous works involving time-domain signal processing employ voltage-controlled oscillators and gated-ring oscillators [31][32][33][34][35][36][37][38]. A time encoding quantizer was presented in [39][40][41][42][43]. Modulators with time-domain quantizers (TDQ) utilizing pulse wave modulation (PWM) and pulse position modulation (PPM) have been introduced in [44][45][46][47].

In this paper, a 2^{nd} order $\Sigma\Delta$ modulator with a new TDQ is demonstrated. The scheme utilizes a pulse wave modulator to convert the voltage-domain information to time-domain by modulating the width of the pulse proportional to the input voltage. This time-domain information, or width of the pulse, is then quantized in terms smaller time steps using a counter. The signal which needs to be fed back to the loop is also derived from the output of the counter. The obtained feedback is fit for 1-bit DAC, eliminating the problem of feedback DAC linearity. It is better scheme than [44] in terms of utilizing lesser hardware, and hence is more area efficient.

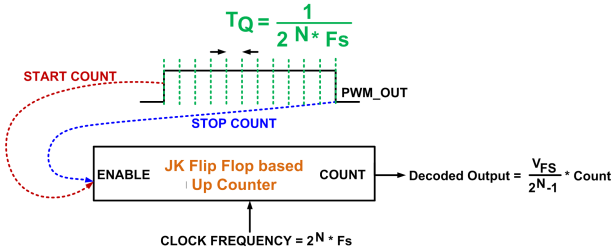


Fig. 2. Basic scheme of the proposed TDQ.

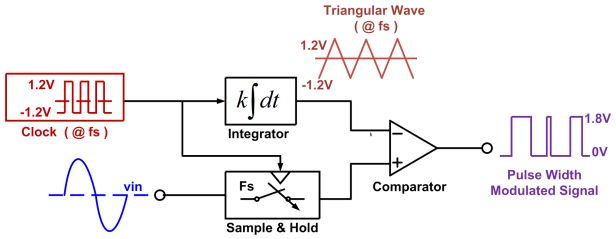


Fig. 3. Block diagram of the PWM generator.

The organization of this paper is as follows. Section II introduces the proposed TDQ and mentions the design parameters used for modeling the TDQ and $\Sigma\Delta$ modulator. The experimental results and conclusions are given in Section III and Section IV, respectively.

II. Modified Time-Domain Quantizer

Fig. 2 illustrates the basic scheme of the proposed time domain quantizer. The PWM generator outputs pulses, PWM_OUT, whose widths are proportional to the input voltage. The PWM_OUT signal acts as the *enable* signal for a counter, working as a time to digital converter (TDC). The counter operating at a high frequency (multiples of the sampling frequency of the modulator) counts the number of time steps, T_Q, within the width of the pulse generated by the PWM. A *N-bit* voltage-domain quantizer divides the full scale voltage range into 2^N levels. Emulating the same concept, the *N-bit* TDC requires a *N-bit* counter so that the pulse with maximum width can be divided into 2^N time steps T_Q. Therefore, the counter needs to be operating at a frequency of $2^N * F_S$, where F_S is the sampling frequency of the modulator. The feedback signal is derived by *ORing* the outputs (Q_0 - Q_5) of the counter and it emulates the 1-bit feedback signal in the case of single bit modulators. Hence this scheme does away with the stringent requirements of DAC accuracy in multibit topology.

A. PWM Generator

The block diagram of the PWM generator is depicted in Fig. 3. A clock pulse signal of frequency of F_S, where F_S is the sampling frequency of the modulator, is integrated to obtain a triangular wave with same frequency. This triangular wave along with the input sampled at F_S are fed to a comparator. The comparator outputs a PWM signal whose pulse width is proportional to the input voltage. Hence, the voltage-domain information is encapsulated into width of the pulse in time-domain. It is worth mentioning here that compared to that in [44], double sampling is not required in the proposed scheme. Thus a single comparator is enough vis-a-vis two comparators necessary in [44]. Also the proposed scheme samples the input at a rate half that of [44], so the proposed scheme is comparatively less effected by errors emanating from clock jitter.

The simulation parameters used for the PWM generator for the proposed TDQ are given in Table I.

TABLE I
Simulation Parameters for PWM Generator

Parameter	Value
Modulator sampling frequency	250MHz
Input signal sampling frequency	250MHz
Clock frequency	250MHz
Triangular wave frequency	250MHz
Triangular wave peak-to-peak voltage range	$\pm 1.2V$

B. TDC with loop feedback signal generation

The PWM_OUT signal acts as an enable signal for the TDC. The TDC consists of a JK flip flop based up-counter. The counter essentially counts the number of smaller time steps, T_Q, hence emulating a conventional qunatizer with its quantization error (see Fig. 2). In order to obtain $N-bit$ resolution the counter is operated at a frequency of $2^N * F_S$, where F_S is the sampling frequency of the modulator. At the same time it is noticeable that only $M = \log_2(N)$ flip-flops is enough to achieve the same resolution. The counter starts to count at positive edge of the PWM_OUT and is reset at its negative edge. The count corresponding to each pulse is also latched at same negative edge. A normal JK flip-flop in the Simulink (MATLAB) library is modified to include the reset functionality as shown in Fig. 4. A synchronous up-counter is built using the modified JK flip-flop as shown Fig. 5.

Finally taking clue from the fact a 1-bit $\Sigma\Delta$ ADC outputs more number of logic ones for a higher input amplitude, it is contemplated that the loop feedback signal needs to be held at logic high for a period proportional to the input signal amplitude. Hence the feedback signal is generated by $ORing$ each of the M bits of the counter.

The simulation parameters used for the TDC for the proposed TDQ are given in Table II.

TABLE II
Simulation Parameters for TDC

Parameter	Value
Desired qunatizer resolution	6 bits
Counter operating frequency	$(2^6 * 250MHz =) 16GHz$
Number of flip-flops used	6

The complete TDQ is shown in Fig. 6.

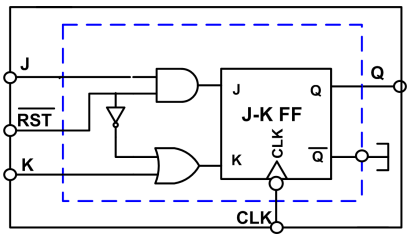


Fig. 4. JK flip-flop from the Simulink library modified to include reset facility.

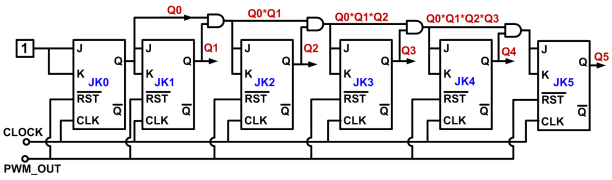


Fig. 5. Block diagram of the up-counter implemented using the modified JK flip-flop shown in the previous figure.

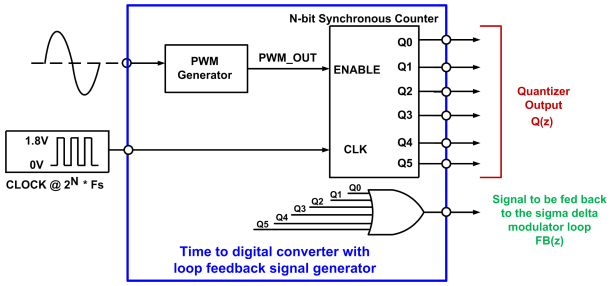


Fig. 6. Block diagram of the proposed TDQ.

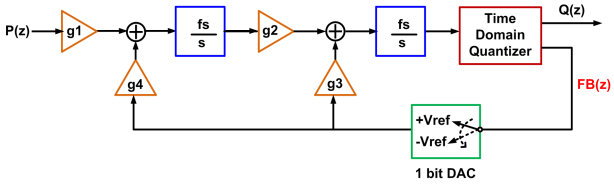


Fig. 7. Block diagram of the 2^{nd} order CT $\Sigma\Delta$ modulator loop incorporating the proposed TDQ.

C. Continuous-time $\Sigma\Delta$ modulator incorporating the proposed TDQ

The 2^{nd} order CT $\Sigma\Delta$ modulator loop incorporating the proposed TDQ is shown in Fig. 6. Here the coefficients, $g1, g2, g3$ and $g4$, are fixed (using the concept of dynamic loop scaling) such that the output of the second integrator does not exceed the peak-to-peak volatge range of the triangular wave obtained from the PWM generator (see Fig. 3). The loop coefficients and simulation parameters are given in Table III.

III. Simulation Results

To validate the proposal the complete scheme described above is modeled using Simulimk (Matlab). The Fig. 8 shows the output of each of the integrator in the modulator, and the

TABLE III
SIMULATION PARAMETERS FOR $\Sigma\Delta$ MODULATOR

Parameter	Value
g_1	0.2
g_2	0.7
g_3	0.6
g_4	0.3
F_S	250MHz
V_{REF}	1.225V
Input amplitude	-5.78dB
Input frequency	1 MHz

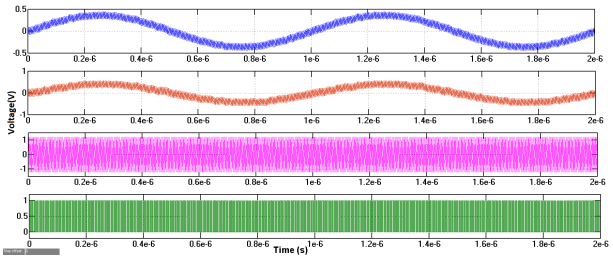


Fig. 8. Output waveform of each of the integrator in the modulator, and the PWM generator. The plots are arranged as - output of first integrator, output of the second integrator, triangular wave and PWM wave (in sequence from top to bottom).

PWM generator. As is clear from the figure, the peak-to-peak output of the second integrator never exceeds the peak-to-peak voltage range of the triangular wave. The outputs of the TDC along with the feedback signal for the loop for one of the pulses generated by the PWM generator is shown in Fig. 9. It is evident from the figure that counter starts to count at arrival of the first clock pulse after positive edge of the PWM_OUT and is reset at its negative edge. Also the feedback signal, hence generated, closely matches the input pulse with some quantization error. The power spectral density of the output of the $\Sigma\Delta$ modulator, described in the previous section, is shown in Fig. 10. The $\Sigma\Delta$ modulator achieves 45.7dB signal to noise distortion ratio (SNDR) for a input sine-wave of 1MHz frequency and -5.78dB amplitude. Therefore, the proposed scheme for a TDQ works as desired and is compatible with a $\Sigma\Delta$ modulator. More importantly, it is worth noticing that the proposed quantizer renders the same functionality of [44], but with a significantly lower hardware requirement. The proposed PWM generator requires only one comparator vis-a-vis two comparators necessary in [44]). Additionally, the proposed N-bit TDC uses only N flip-flops compared to 2^N used in [44].

IV. Conclusion

$\Sigma\Delta$ modulator with a new scheme for TDQ has been proposed. All the required modules have been modeled using Simulink (MATLAB) library blocks and the proposed scheme is validated through simulations. The proposed TDQ works as desired, and more importantly, with considerably lesser hardware requirements. This system is intended for wideband applications.

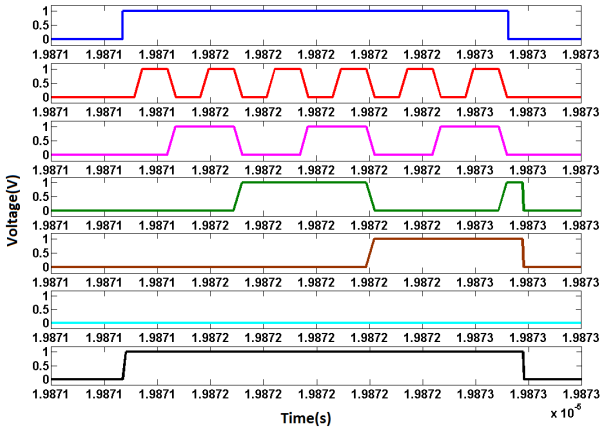


Fig. 9. The output of the TDC along with the feedback signal for the loop for a specimen pulse generated by the PWM generator is shown in Fig. 9. The outputs are arranged as - the pulse from PWM generator, $Q0$ (LSB), $Q1$, $Q2$, $Q3$, $Q4$, $Q5$ (MSB) and the feedback signal (in sequence from top to bottom).

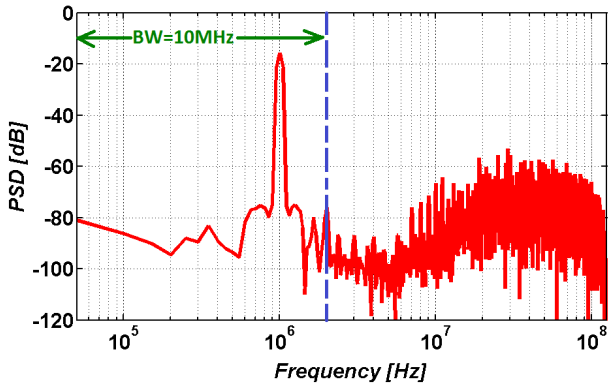


Fig. 10. The power spectral density of the output of the $\Sigma\Delta$ modulator shown in Fig.7 .

TABLE IV
PERFORMANCE OF $\Sigma\Delta$ ADC WITH TDQ

Parameter	Value	
	This work	[44]
Order	2^{nd}	3^{rd}
Bandwidth (MHz)	10	20k
Fs (MHz)	250	250
V_{REF} (V)	1.225	1.2
Input amplitude (dB)	-5.78	-5
SNDR (dB)	45.7	60

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