

A Compact and Low-Power CMOS Circuit for Fully-Integrated NEMS Resonators

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Abstract—This paper presents a fully-integrated NEMS resonator, operable at frequencies in the MHz range, together with a compact built-in CMOS interfacing circuitry. The proposed low-power CCII circuit allows detailed read-out of the nanocantilever structure for either extraction of equivalent circuit models or comparative studies at different pressure and DC biasing conditions. In this sense, extensive experimental results are presented for a real mixed electro-mechanical system integrated through a combination of in-house standard CMOS technology and nanodevice post-processing by nanostencil lithography. The proposed read-out scheme can be easily adapted to operate the nanocantilever in closed loop operation as a stand alone NEMS oscillator.

Index Terms—Low-power, current-conveyor, CMOS, NEMS, resonator, read-out.

I. INTRODUCTION

IT is well known that the semiconductor market exhibits an increasing demand on products for mobile applications, requiring in general very low-power and compact integrated circuits. In this sense, nanotechnologies seem a suitable partner for CMOS circuits, since mechanical implementations may achieve larger power savings and size reductions than their electronic counterparts. In particular, micro and nanoelectromechanical systems (M/NEMS) are good candidates to replace the costly and bulky quartz crystal devices in integrated oscillators [1], [2] or to operate as integrated sensors [3], [4]. Hence, there is a real need not only for CMOS compatible NEMS resonators but also for specific MOS circuits required for their test and operation in future mixed electro-mechanical systems-on-chip.

This paper presents a fully-integrated nanocantilever, operable at frequencies in the MHz range, together with a specific built-in low-power CMOS read-out circuit for its experimental characterization and interfacing (e.g. closed loop operation as stand alone oscillator). The NEMS fabrication is based on nanostencil lithography [5], while a new low-power CMOS topology is introduced for the interface circuit in terms of second generation current conveyors (CCII) [6]. The mixed electro-mechanical system is finally integrated through a combination of in-house standard CMOS technology and nanodevice post-processing [7].

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Next section makes a short introduction to the overall mixed NEMS/CMOS system to be integrated. Then, an equivalent circuit is explained in Section III for modeling the nanoresonator itself. The novel low-power CCII CMOS topology for the interfacing circuit is proposed in Section IV, while Section V presents a mixed integrated example and its experimental results. Finally, conclusions are summarized in Section VI.

II. RESONATOR READ-OUT

In general, NEMS resonators based on nanocantilevers include the main parts shown in Figure 1(a), where its ideal read-out scheme is also illustrated. The device consists of a driver, mechanically fixed, and a cantilever placed in parallel very close to the driver and anchored only at one end, so it can freely bend around the static position at a given oscillation frequency.

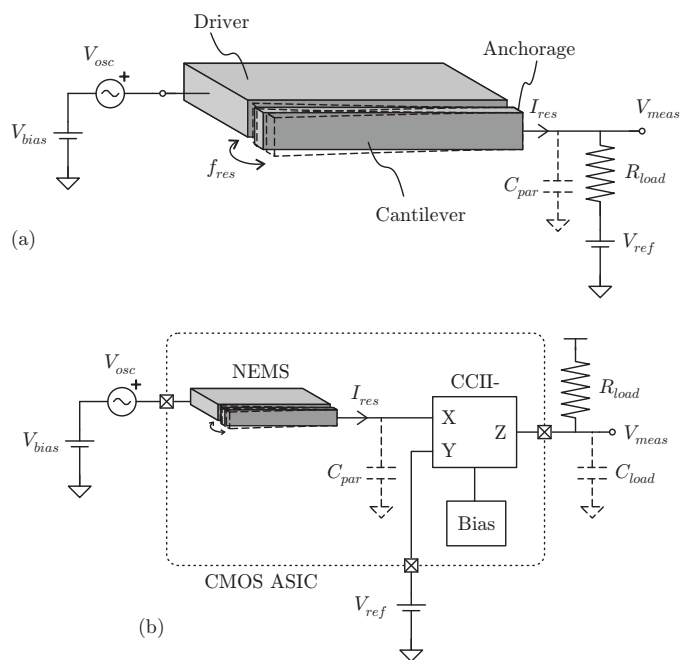


Fig. 1. NEMS ideal read-out scheme (a) and proposed monolithic CMOS solution (b).

Under read-out operation, the fixed driver is devoted to bias the required DC voltage $V_{bias} - V_{ref}$ (typ. 1V to 20V) and to act as the input terminal for the frequency stimulation V_{osc} (typ. -30dBm to 0dBm). On the other hand, the cantilever plays the role of the output terminal, allowing the read-out of the NEMS resonator current I_{res} (typ. in the range of nA)

and the corresponding voltage signal V_{meas} at the load resistor R_{load} . The resonance frequency f_{res} (typ. 1MHz to 10MHz) depends on the cantilever material and dimensions, as detailed in Section III.

Unfortunately, the ideal read-out scheme of Figure 1(a) is not feasible in practice due to the $M\Omega$ range values of the NEMS resonator impedance around f_{res} , which limits the allowed parasitic capacitance at the output port C_{par} far below the pF range. Hence, a built-in interface circuit is required. Several implementations based on the passive integration of I_{res} through C_{par} have been reported in the literature [2], [8], [9]. However, the resulting integration gain is still strongly dependent on the layout parasitics. In order to overcome this issue, the alternative approach of Figure 1(b) is proposed, where a built-in CMOS CCII is inserted at the output electrode. This new scenario is not only suitable to ensure parasitic capacitance values for C_{par} in the sub-pF range, but it also minimizes C_{par} effects by keeping a constant voltage bias at this electrode. Furthermore, the proposed CCII interface supplies flat spectral amplification of I_{res} for either external measurement at V_{meas} or internal feedback to V_{osc} (e.g. stand alone oscillator), as analyzed in Section IV.

III. NEMS TECHNOLOGY AND DEVICE MODEL

The basis of the fabrication process is described in [8] and consists of post-processing standard CMOS wafers. Only a required area of poly-silicon for the nanodevice must be reserved during CMOS integration. However, the novelty here is the lithography process itself, from which an enhanced resolution down to 200nm and a higher fabrication throughput are obtained [7] by applying a full-wafer and parallel nanopatterning technique named nanostencil lithography (nSL) [5]. In this new process, after concluding the fabrication of the CMOS circuits, the integration area is selectively patterned with a 80nm thick aluminum layer by nSL. Subsequent process steps consist on reactive ion etching of silicon to transfer the aluminum pattern to the poly-silicon structural layer, wafer dicing and silicon oxide wet etching to release the mechanical structure. Following this procedure, lateral resolutions of 200nm can be routinely achieved, while surrounding CMOS circuits show no degradation of their analog performance. Further details about this specific NEMS technology can be found in a recent work reported by these authors [7]. As a result of the above CMOS post-processing, the poly-silicon structure of Figure 2(a) is obtained, where W , L , H and D stand for the cantilever width, length, height and gap to driver, respectively. In our case, the typical dimensions for the NEMS device are listed in Table I.

TABLE I
PHYSICAL DIMENSIONS OF THE NEMS RESONATOR OF FIGURE 2.

| Parameter | Value | Units |
|-----------|-------|---------------|
| W | 265 | nm |
| L | 14.5 | μm |
| H | 580 | nm |
| D | 650 | nm |

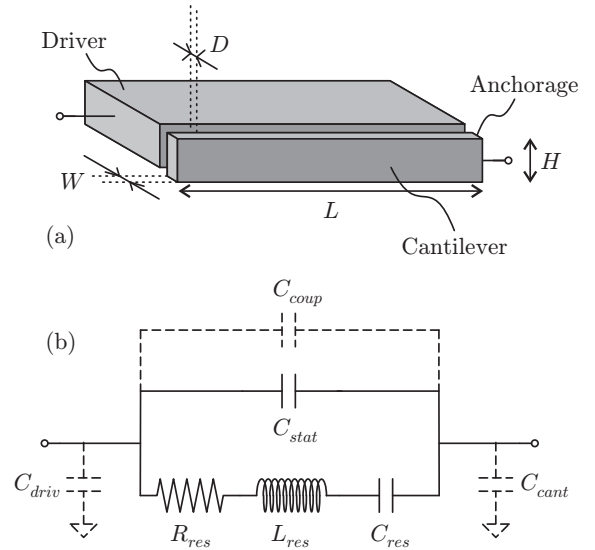


Fig. 2. Physical (a) and equivalent circuit model (b) of the NEMS resonator. Top drawing not in scale.

In general, the resonance frequency for a given oscillation mode i of a mechanical resonator is given by:

$$f_i = \frac{1}{2\pi} \sqrt{\frac{k_i}{m_{eff}}} \quad (1)$$

where k_i and m_{eff} are the spring constant and the effective mass, both depend on the oscillation mode and on the force loading distribution and point of application (air damping is neglected). In our case, we consider the fundamental mode that corresponds to a lateral flexion. Supposing undamped (i.e. ideal vacuum) operation, the analytical expression of the natural (i.e. without any electrostatic force) resonance frequency of this mode is found to be [10]:

$$f_{res} = \frac{1.015}{2\pi} \sqrt{\frac{E W}{\rho L^2}} \quad (2)$$

where E and ρ stand for the Young's modulus and the mass density of the nanocantilever material, respectively.

The signal transduction is based on capacitive detection. Around the resonance frequency of the considered mode, the nanocantilever moves laterally and its mechanical motion is translated into an electrical signal, subsequently collected and processed by the read-out circuit. In fact, the capacitive current generated by a two-electrodes configuration can be described as:

$$\begin{aligned} I_{res} &= \frac{dQ_{res}}{dt} \\ &= (C_{stat} + C_{mot}) \frac{dV_{osc}}{dt} + (V_{bias} - V_{ref} + V_{osc}) \frac{dC_{mot}}{dt} \\ &\simeq C_{stat} \frac{dV_{osc}}{dt} + (V_{bias} - V_{ref}) \frac{dC_{mot}}{dt} \end{aligned} \quad (3)$$

where C_{stat} and C_{mot} are the static plate and the motion capacitances, respectively. Thus, the NEMS current can be understood as a sum of two contributions: one arising from the

static structure (i.e. $C_{stat} \frac{dV_{osc}}{dt}$) and the other coming from the nanocantilever motion itself (i.e. $(V_{bias} - V_{ref}) \frac{dC_{mot}}{dt}$). This second part allows the measure of the frequency response of the mechanical resonator.

In practice, either due to air environment or other second order effects, the NEMS resonator can exhibit important losses that translate into a decrease of its quality factor Q . In these cases, the nanomechanical resonator can be described through a small signal equivalent RLC model [1], as depicted in Figure 2(b). The main physical parameters of this model are the cantilever dissipation, mass and elasticity, which are electrically equivalent to R_{res} , L_{res} and C_{res} respectively:

$$\begin{aligned} R_{res} &= \frac{\sqrt{k_0 m_{eff}}}{Q \eta^2} & C_{stat} &= \epsilon_0 \frac{HL}{D} \\ L_{res} &= \frac{m_{eff}}{\eta^2} \\ C_{res} &= \frac{\eta^2}{k_0} & \eta &= \epsilon_0 \frac{HL(V_{bias} - V_{ref})}{D^2} \end{aligned} \quad (4)$$

where η and ϵ_0 stand for the electromechanical coupling coefficient and the vacuum dielectric constant, respectively. In addition, the cantilever output capacitance C_{cant} and the fringing coupling to the driver C_{coup} are included here, while the driver own capacitance C_{driv} can be neglected according to the read-out scheme of Figure 1. Unfortunately, analytical expressions for R_{res} are difficult to obtain, so Q is usually extracted from experimental data, as illustrated in Section V.

IV. CMOS CURRENT CONVEYOR CIRCUIT

As stated in Section II, the aim of the CMOS interfacing circuit in Figure 1 is both to ensure a constant bias at the output of the NEMS resonator and to read-out its current. For this purpose, the compact CMOS circuit shown in Figure 3 is proposed. Basically, this block consists of an input low-impedance stage (M1-M4) and an output current scaler (M5-M12).

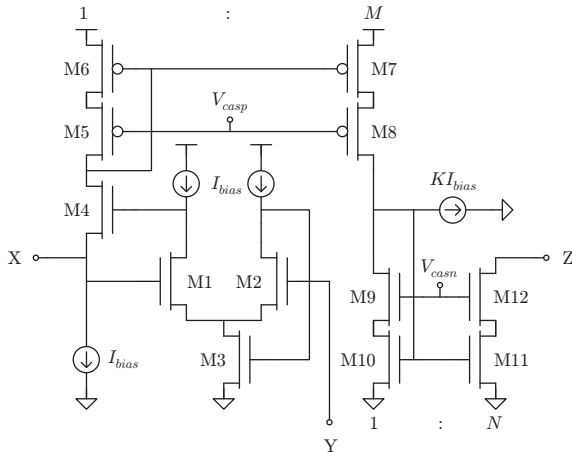


Fig. 3. Simplified schematic of the CMOS CCII- circuit.

On one hand, the input low-impedance is achieved by the cascode transistor M4. Its gate is continuously regulated by

the telescopic differential amplifier M1-M3, whose negative feedback tends to compensate any difference between V_X and V_Y . As a result, this input stage behaves like a voltage source V_X controlled by V_Y , sinking or sourcing the I_{res} current demanded by the NEMS resonator. In this sense, the I_{res} full scale that can drive the CCII- circuit from X is defined by its Class-A bias level I_{bias} . According to the advanced EKV MOSFET model [11], the small-signal input resistance of this controlled voltage source is found to be:

$$r_{in} = \left(\frac{1}{n + \frac{gm_{g1}}{gm_{d1}}} \right) \frac{1}{gm_{g4}} \quad (5)$$

where n stands for the subthreshold slope factor. Hence, the error amplifier M1 scales down r_{in} by its gain factor $\frac{gm_{g1}}{gm_{d1}}$ compared to the impedance of the single M4 transistor $\frac{1}{gm_{g4}}$.

On the other hand, the NEMS current sensed by M4 is amplified by the geometry scaling factors M and N of the two-stage cascode current mirrors M5-M8 and M9-M12 biased at V_{casp} and V_{casn} , respectively. In order to reduce the overall power consumption, a K/M fraction of the biasing is subtracted before the second amplification stage.

In conclusion, the proposed circuit qualitatively behaves like a classic CCII- [6], but with an extra gain from the I_X to I_Z signals:

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & -MN & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \quad (6)$$

In fact, the new CCII- topology introduced in Figure 3 is an improvement of the input stage [12] in order to allow a wider voltage range for both V_X and V_Y thanks to the symmetry of the M1 and M2 drain connections. Also, compared to other similar CCII- evolutions like [13], [14], the proposed circuit saves power consumption by minimizing the transistor count of the input stage.

Applying the circuit model (6) to the general read-out scheme of Figure 1, we obtain the final design equations:

$$\Delta V_{meas} = R_{load} MN \Delta I_{res} \quad (7)$$

$$V_{cant} \equiv V_{ref} \quad (8)$$

where V_{cant} stands for the voltage biasing at the NEMS resonator output. The MOS device dimensions for the proposed CCII- are listed in Table II, while the resulting electrical specifications are summarized in Table III for a typical set of design values.

V. INTEGRATION AND RESULTS

Following the proposals of Sections III and IV, a compact 1.5MHz NEMS resonator together with the CMOS interfacing circuit has been integrated through the in-house standard CMOS double poly-silicon technology and the full-wafer post-processing steps based on nanostencil lithography described in [7]. The resulting size of the mixed electro-mechanical system without pads is about $800\mu\text{m} \times 400\mu\text{m}$ (0.32mm^2), as

TABLE II
DEVICE DIMENSIONS FOR THE CCII- OF FIGURE 3

| Transistor | $\frac{W}{L}$ [$\frac{\mu\text{m}}{\mu\text{m}}$] |
|------------|---|
| M1-2 | $4 \times 30/5$ |
| M3 | $2 \times 15/10$ |
| M4 | $30/3$ |
| M5-6 | $10/5$ |
| M7-8 | $M \times 10/5$ |
| M9-10 | $50/5$ |
| M11-12 | $N \times 50/5$ |

TABLE III

OVERALL SPECIFICATIONS OF THE READ-OUT CIRCUIT FOR $I_{bias}=10\mu\text{A}$,
 $M=N=10$, $K=9$ AND $R_{load}=700\Omega$

| Parameter | Value | Units |
|-----------------------------|-------|------------------------------|
| Transimpedance | 70 | $\text{k}\Omega$ |
| Bandwidth | 7.5 | MHz |
| In-band input impedance | <3 | $\text{k}\Omega$ |
| In-band input current noise | 0.5 | $\text{pA}/\sqrt{\text{Hz}}$ |
| Supply voltage | 5 | V |
| Current consumption | 230 | μA |
| Load capacitance | 30 | pF |

shown in Figure 4. Since the in-house CMOS technology is a $2.5\mu\text{m}$ lithography process, a considerably smaller implementation can be obtained using modern submicron CMOS technologies.

Taking advantage of the built-in interfacing circuit, the NEMS resonator has been tested. In this sense, the typical transfer function of the nanoresonator is depicted in Figure 5. As it can be easily seen, the NEMS device exhibits a clear and narrow mechanical resonance around $f_{res}=1.5\text{MHz}$, showing important magnitude losses outside this band. All magnitude transfer functions in this section are normalized to $R_{load}MN/R_{res}\simeq-55\text{dB}$. In case of fully integrated closed loop operation (e.g. stand alone oscillator), this attenuation factor can be easily compensated to 0dB by choosing larger M , N and R_{load} design values, as the CCII- load capacitance is then $C_{driv} \ll C_{load}$. From the Q factor and the $V_{bias}-V_{ref}$ DC biasing of Figure 5, the model parameters of Table IV are deduced. The same nanocantilever has been measured for different environment pressure conditions in Figure 6, returning very good results at vacuum levels below 10Pa. Finally, a comparison between vacuum and air environments for different biasing levels has been also tested in Figure 7. These results verify the dependence of the resonance frequency on the square of the DC biasing for electrostatically actuated NEMS resonators, and the decrease of its resonance quality factor due to air damping losses.

VI. CONCLUSIONS

A compact NEMS resonator with built-in CMOS interfacing circuitry has been successfully integrated and experimentally tested. The new low-power CCII read-out circuit allows detailed measurements of the nanocantilever structure in the

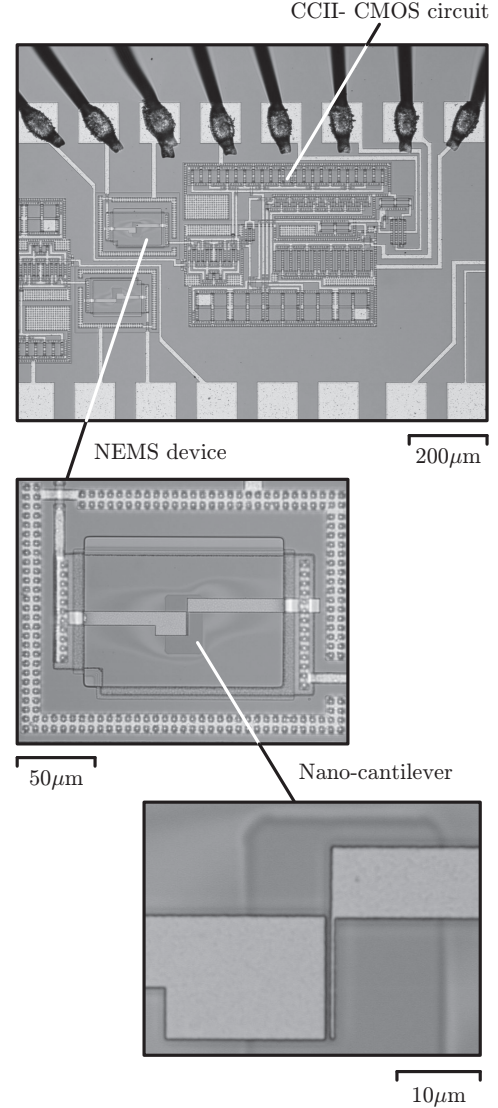


Fig. 4. Microscope photographs of the mixed NEMS and CMOS circuit.

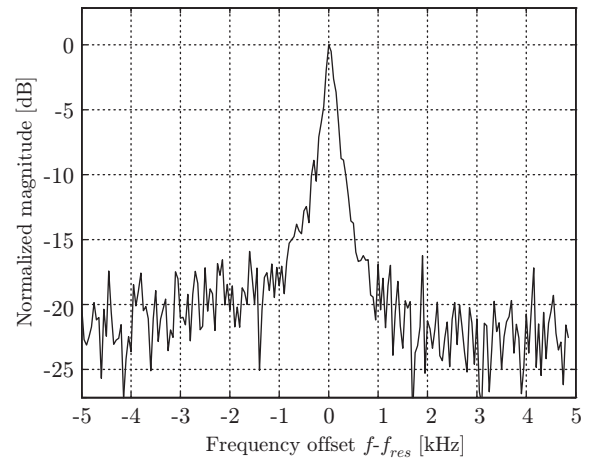
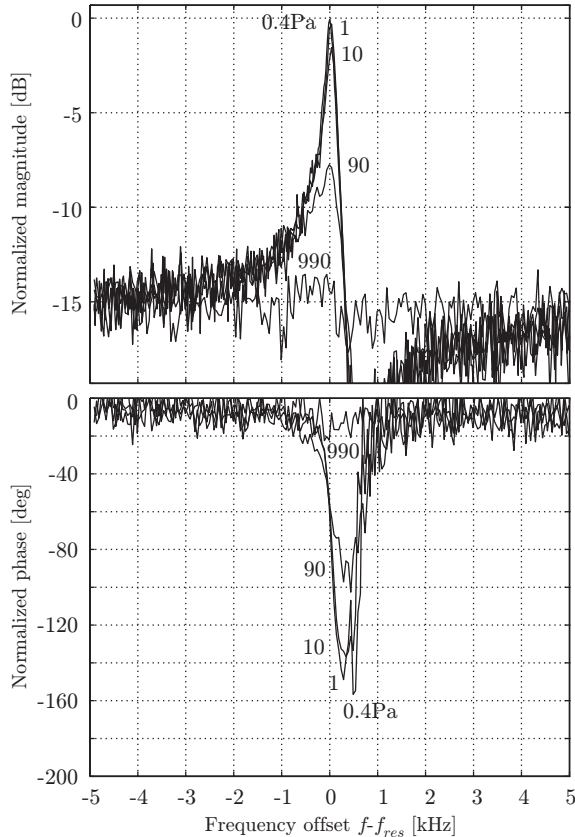


Fig. 5. Experimental NEMS transfer function in vacuum (0.9Pa) for $V_{bias}-V_{ref}=2\text{V}$, $V_{osc}=-26\text{dBm}$, resulting in $f_{res}\simeq 1.5\text{MHz}$ and $Q\simeq 8000$.

TABLE IV

TYPICAL MODEL PARAMETERS FOR THE NEMS RESONATOR OF FIGURE 2.

| Parameter | Value | Units |
|-----------------------|-------|------------|
| R_{res} | 40 | M Ω |
| L_{res} | 33 | kH |
| C_{res} | 0.34 | aF |
| $C_{stat} + C_{coup}$ | 275 | aF |
| C_{cant} | <50 | fF |

Fig. 6. Experimental NEMS transfer function for different vacuum levels and $V_{bias}-V_{ref}=1V$, $V_{osc}=-17dBm$ and $f_{res}\simeq 1.5MHz$.

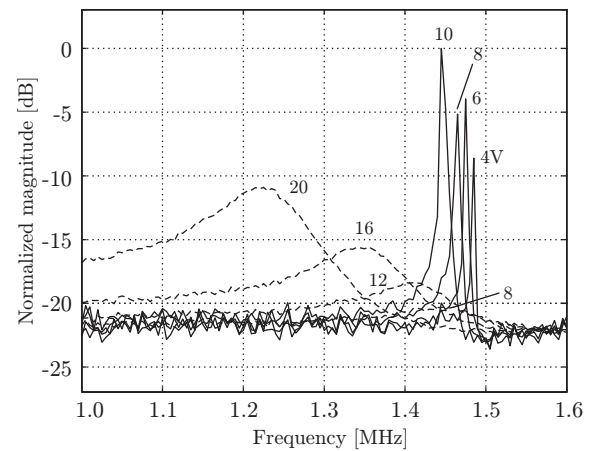
MHz range for either extraction of equivalent circuit models or comparative studies at different pressure and DC biasing conditions. In this sense, the proposed interfacing circuit can be easily adapted (e.g. choosing a larger value for R_{load}) to operate the nanocantilever in closed loop operation as a mixed electro-mechanical stand alone oscillator.

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Fig. 7. Experimental NEMS transfer function comparison between vacuum (solid, $<5Pa$, $V_{osc}=-10dBm$) and air pressure (dashed, $V_{osc}=0dBm$) for different $V_{bias}-V_{ref}$ levels. Due to limited frequency resolution, peak values are approximative.

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