Low-Power and Compact CMOS APS Circuits for Hybrid Cryogenic Infrared Fast Imaging

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***Abstract*— This paper presents a complete set of CMOS basic building blocks for low-cost scanning infrared cryogenic imagers. Low-power and compact novel circuits are proposed for single-capacitor integration and correlated double sampling, embedded pixel test, pixel charge-multiplexing and video composition and buffering. In order to validate the new basic building blocks, experimental results are reported in standard 0.35μm CMOS technology for a 50μm×100μm active pixel cell operating at 77K. Based on the proposed circuits, infrared imagers capable of capturing up to 256×2560 pixels at 25fps can be implemented.**

***Index Terms*— Low-power, CMOS, APS, infrared, photon sensors, QWIP, cryogenic, imagers.**

I. Introduction

Today imaging applications in fields like medicine, astronomy and strategic equipments demand read out integrated circuits (ROICs) capable of capturing high resolution and real time infrared (IR) images. In general, IR sensing is primary supported in these systems by either cryogenic photon or room temperature thermal devices. The advantages of the former are higher sensitivity and shorter response times, while the latter avoids the auxiliary cooling system and it can be CMOS compatible. Anyway, these IR devices are usually arranged in a fixed focal plane array (FPA) and attached one-by-one to the corresponding active pixel sensor (APS) of the ROIC through hybrid packaging (e.g. bump bonding), or building the IR sensor monolithically on top of the CMOS read-out circuit by specific technology postprocessing. Unfortunately, the resulting large Si area of such a FPA tends to increase the prototyping costs and decrease the production yield of the ROIC. An alternative approach consists of building the IR image from a linear ROIC scanner, so reducing the physical size of the FPA. However, scanners require high speed APS cells for the real time multiplexing of high definition images, together with very low-power operation to prevent from inducing thermal noise at the IR sensor, specially for cryogenic devices. This paper presents a complete set of CMOS circuits from pixel to system levels in order to build fast scanning imagers for infrared cryogenic photon sensors. Using these novel basic building blocks, a compact and low-power APS is obtained, which is compatible with high speed and low temperature operation. In this sense, experimental results operating at cryogenic temperatures are reported for a standard 0.35μm CMOS technology.

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II. Imager Architecture

The target system architecture is based on a linear imager [1], which builds the full frame by rotative scanning, as depicted in Fig.1(a). The imager itself includes an array of IR sensors vertically attached to the ROIC through a grid of sensor-to-APS bumps, as shown in Fig.1(b). In our case, the IR plane is made of quantum-well infrared photon sensors (QWIP) operating at cryogenic (77K) temperature [2], which generate a sensor-to-APS current proportional to the IR power according to their optical responsivity. The serial output signal is generated by iterative scanning along the full column of pixels. Although the system structure behaves as a single-column effective imager, in practice several columns of identical APS cells are included to process tri-color and 4-times oversampling images for time-delay integration (TDI). Hence, apart from the pixel scanning along each column, the video signal also requires multiplexing across several columns.

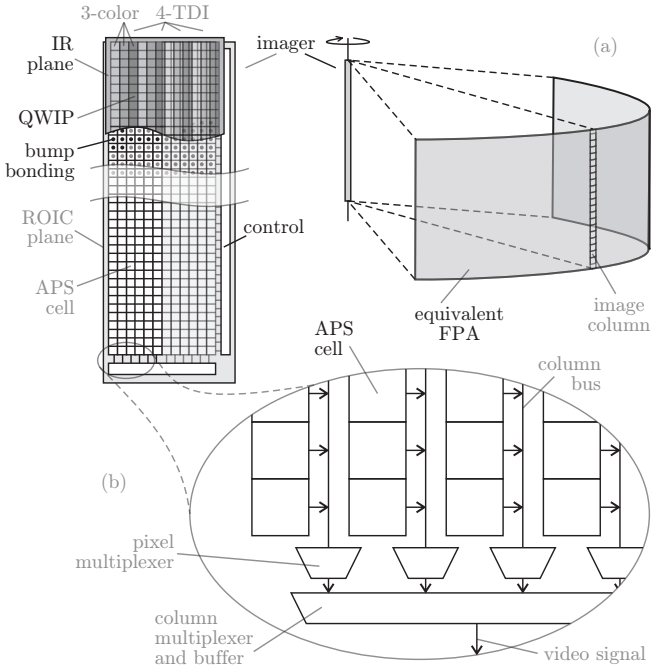

Fig. 1. Basic operation (a) and internal architecture (b) of the target IR scanning imager.

The main advantage of the scanning architecture of Fig.1 over the equivalent fixed FPA solution is the reduced silicon area requirements for the final ROIC, resulting in a low-cost and yield-improved CMOS integration. Furthermore, an optimum trade-off can be achieved between horizontal frame size and refresh time for each particular imaging application

(e.g. halving the width of the frame in pixels allows to double its image rate). In fact, the product of these two variables defines the true specification, which is the column rate.

On the contrary, the APS cell of Fig.1(b) must be now fast enough in terms of integration and multiplexing times to meet the requested high column rate. Concerning the short integration time, a correlated double sampling (CDS) mechanism is mandatory for the reduction of the KTC noise [3], but its implementation should not increase the overall size of the APS cell. On the other hand, short pixel multiplexing times along the image column usually require higher power consumption levels, which should be optimized to be compatible with the cryogenic operation of the system.

III. Basic Building Blocks

A. Single-Capacitor CTIA and CDS

In the case of hybrid imagers, pre-amplification of the sensor current signal (I_{qwip}) is usually implemented inside each APS cell through a capacitive transimpedance amplifier (CTIA), in order to minimize the effects of the input parasitic capacitance of the packaging (C_{par}). Due to the short integration times required by the scanning system, small integration capacitances (C_{int}) are needed. As a result, an extra CDS stage is added to eliminate the low-frequency components of the KTC_{int} noise. A classical circuit implementation [3] for the CDS function is shown in Fig.2(a).

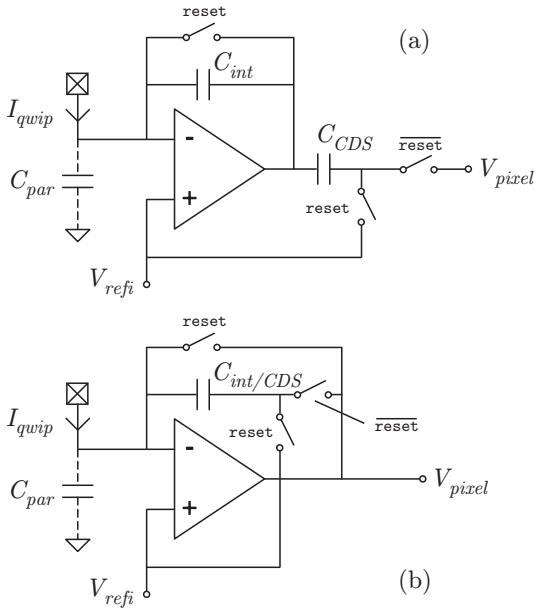

Fig. 2. Classic integration and CDS scheme (a) and proposed single-capacitor solution (b) for the APS cell.

In this scheme, C_{CDS}, V_{refi} and V_{pixel} stand for the CDS capacitance, the input bias voltage of the IR sensor and the output signal voltage, respectively. The principle of operation is a follows: during the initial reset of the integration capacitor (`reset`=1), C_{CDS} samples the output noise of the CTIA; once in the integration time (`reset`=0), the same C_{CDS} is connected in series to cancel the offset and low-frequency noise components at V_{pixel}. In practice, this series capacitor is one of the main contributors to the pixel size. In order to save silicon area, a new single-capacitor implementation is proposed in Fig.2(b). Instead of resetting C_{int} to zero before each integration period, the basic idea here is to pre-charge it to the offset and the output noise of the CTIA. For this purpose, $C_{int/CDS}$ is connected between the CTIA output and the reference input when resetting (`reset`=1), while it is reversed during the integration phase to cause proper cancellation (`reset`=0). Hence, the same capacitor $C_{int/CDS}$ is devoted to perform both the integration and the CDS tasks. As a result, the replaced capacitor C_{CDS} of Fig.2(a) can be used then for other functions inside the same APS, as proposed in next subsections. For short integration times (T_{int}) compared to signal bandwidth, the resulting signal at the output of Fig.2(b) is:

$$\begin{aligned} V_{pixel} &= V_{refi} - \frac{1}{C_{int/CDS}} \int_{nT_{int}}^{(n+1)T_{int}} I_{qwip} dt \\ &\simeq V_{refi} - \frac{T_{int}}{C_{int/CDS}} I_{qwip} \end{aligned} \tag{1}$$

B. Embedded Pixel-Test

Due to yield issues, most imaging applications require in practice built-in test capabilities to check individual APS cells of the ROIC, specially before the expensive hybrid packaging of Fig.1. For this purpose, the embedded pixel-test circuit of Fig.3(a) is presented, where C_{test} is the test capacitor.

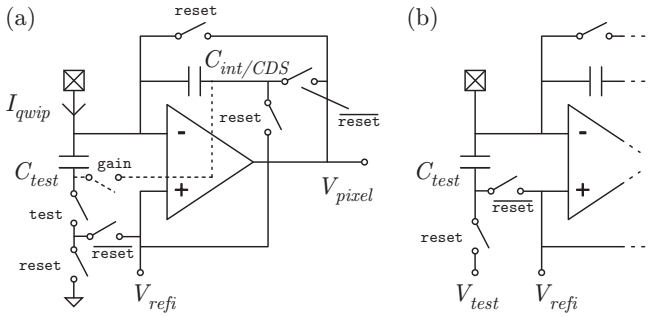

Fig. 3. Proposed embedded test for each individual APS cell (a) and analog direct port modification for the IC verification of Section IV.

If test is selected (`test`=1), the principle of operation is as follows: every reset phase before integration (`reset`=1) causes C_{test} to be pre-charged to V_{refi}; during T_{int} (`reset`=0), the charge stored in C_{test} is transferred to $C_{int/CDS}$ by means of the input virtual short circuit supplied by the CTIA. Hence, under test mode and before packaging (i.e. $I_{qwip} \equiv 0$), the output voltage of the APS cell results in the following technology-independent expression:

$$V_{pixel} = \left(1 - \frac{C_{test}}{C_{int/CDS}}\right) V_{refi} \tag{2}$$

Furthermore, the embedded pixel-test proposal of Fig.3(a) can be combined with several `test` control signals to activate different pixel groups, so cross-talk between adjacent APS cells can be easily investigated. After packaging, C_{test} may be

also reused by operating in parallel with $C_{int/CDS}$ (gain=1) in order to supply some programmability of the CTIA gain:

$$V_{pixel} \simeq V_{refi} - \frac{T_{int}}{C_{int/CDS} + \texttt{gain}C_{test}} I_{qwip} \qquad (3)$$

C. Pixel Charge-Multiplexing

The main bottle-neck in most imagers is the signal multiplexing at pixel level, where hundreds of low-power APS cells must share the same long bus, exhibiting high value capacitive parasitics. Classically, signal multiplexing at this stage is performed through followers or simple series switches at the output of each APS, either in the linear voltage domain [4] or using voltage compression [5]. Anyway, analog voltage switching tends to require higher power consumption at pixel level and it dangerously increases the crosstalk between parallel buses or correlative-in-time samples. In order to overcome such inherent problems, an alternative pixel multiplexing strategy in the charge domain is proposed in Fig.4(a), where C_A and C_B are the pixel and column multiplexing capacitances, while V_{refo} and V_{col} stand for the column voltage reference and signal, respectively. The multiplexing sequence is depicted in Fig.4(b) and explained as follows: previously to any column scanning, all C_A are initialized to the pixel reference V_{refi}, while the column amplifier pre-charges the bus line to V_{refo} (init=1); secondly, all C_A are released and kept in high impedance, so C_B can be then released too (init=0); during pixel multiplexing, the selected k-th APS cell captures (releases) a certain amount of charge from (to) the high-impedance bus through its C_A ($\texttt{select}_k$=1), resulting in a voltage change at the column output V_{col} due to the charge redistribution with C_B; during the selection of the next APS cell ($\texttt{select}_{k+1}$=1), the k-th cell is reset ($\texttt{reset}_k$=1), so the charge is released (captured) back to (from) the bus line. The cycle is completed by keeping again C_A floating. Note that the selection signals can be directly reused as resetting signals for the previous pixel, hence the digital control is strongly simplified. As a result, the multiplexed column output is found to be:

$$\begin{aligned} V_{col} &= V_{refo} + \frac{C_A}{C_B}\left(V_{refi} - V_{pixel}\right) \\ &= \begin{cases} V_{refo} + \dfrac{C_A}{C_B}\dfrac{T_{int}}{C_{int/CDS}} I_{qwip} & \text{sensing} \\ V_{refo} + \dfrac{C_A}{C_B}\dfrac{C_{test}}{C_{int/CDS}} V_{refi} & \text{testing} \end{cases} \end{aligned} \qquad (4)$$

Apart from the signal re-scaling and level-shifting possibilities in (4), the advantage of this new charge-based multiplexing approach is double. Firstly, power consumption in each APS cell can be drastically reduced, since the CTIA of Fig.3(a) only has to drive C_A in Fig.4(a). Secondly, crosstalk between pixels is also minimized due to the fact that the bus lines are kept at the constant voltage V_{refo}. Furthermore, using the same switch in C_A for both, initializing the bus (i.e. init) and for reseting each APS cell (i.e. $\texttt{reset}_k$), charge injection and clock-feedthrough can be canceled even for different values

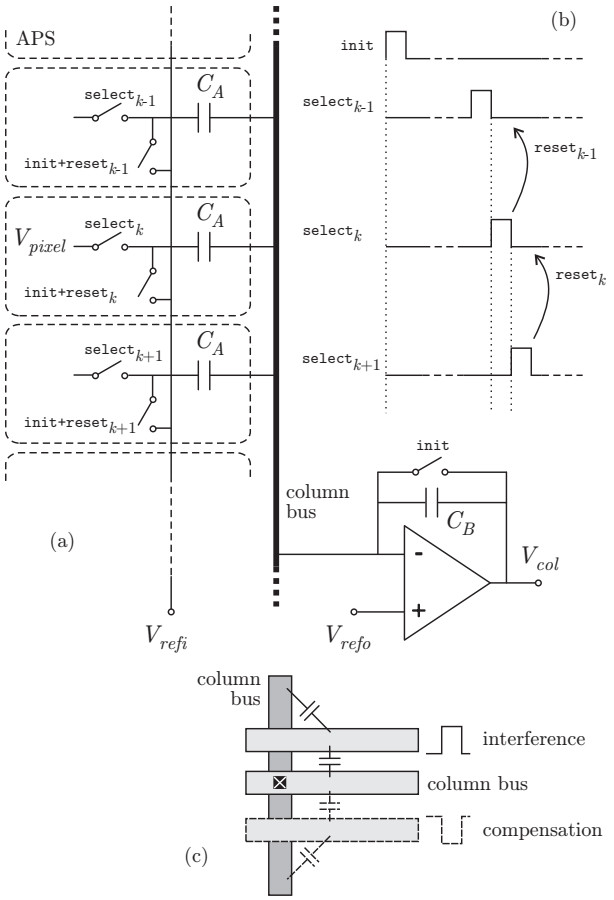

Fig. 4. Simplified schematic (a) and operation principle (b) of the proposed charge-based APS multiplexing, and compensation layout technique against digital coupling to the column bus (c).

in each pixel. In counterpart, the main drawback of this new strategy comes from the possible coupling of digital signals (e.g. $\texttt{select}_k$ or $\texttt{reset}_k$) crossing the high-impedance bus lines. In this sense, the layout technique illustrated in Fig.4(c) based on differential digital signaling is proposed to cancel both overlapping and fringing coupling.

Finally, a dynamic biasing technique is proposed in Fig.5 to optimize consumption during integration and multiplexing phases. Following this topology, the CTIA is fed at a constant and low-value tail-current (I_{bias}) during the slow-swing integration phase, while its biasing is abruptly increased ($+NI_{bias}$) during the selection window in order to drive C_A. The overall power consumption of the ROIC is not affected, as all APS cells are usually consuming I_{bias} except to the single selected pixel. Such dynamic biasing is also active during the APS reset phase in order to store in $C_{int/CDS}$ any possible clock-feedthrough at the input of the CTIA for further cancellation by the CDS itself.

D. Column Multiplexing and Video Buffering

Once individual pixel signals are packed in columns, the imager must still compose the final video stream and supply the suitable output buffering. For this purpose, the low-power and compact circuit topology of Fig. 6 is presented. The

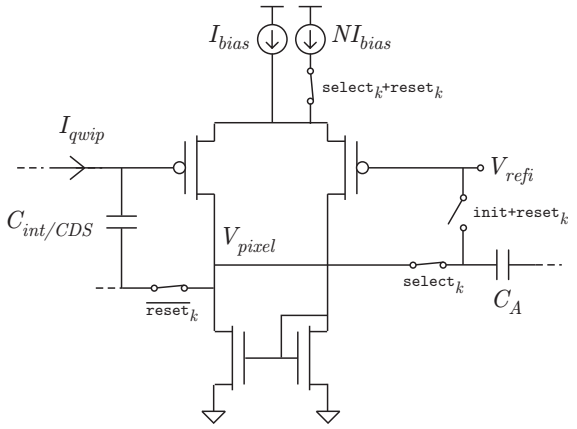

Fig. 5. Proposed low-power dynamic biasing for the CTIA. In this case, the selection window of the multiplexing phase is shown active.

circuit core consists of a cascode pseudo-differential follower which allows Class-AB operation with no extra biasing circuitry. In steady state, M1-M4 devices are biased at I_{bias} by simple matching. Column multiplexing is then implemented by switching the input devices M1 and M3 only through `selectA,B,C...`, so half of the circuitry is shared by several columns. Also, a dummy switch is included in the common part to optimize circuit symmetry. Hence, this strategy combines high-speed capability during signal transients, low-power operation for quiescent outputs, and compact circuit area.

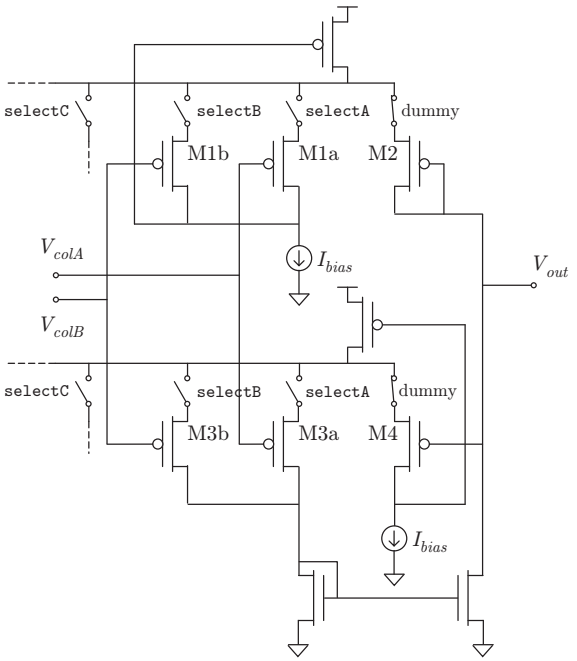

Fig. 6. Proposed column multiplexer and video buffering stage (cascode transistors not shown for simplification).

IV. Experimental Results

In order to validate all the proposed basic building blocks, a test vehicle has been designed and integrated in standard 0.35μm 2-poly 3-metal CMOS technology from Austria Micro Systems (AMS). However, due to the cryogenic operation of the target IR sensors, a re-characterization of the thermal MOSFET model was required before the circuit design, like in [6]. For such a purpose, the custom made test setup of Fig.7(a) was developed, which allows the experimental characterization of the device under test (DUT) down to 77K. Schematically, the dewar is filled with liquid nitrogen, keeping the lower end of the cooler at 77K, while the heater is devoted to increase the temperature of the DUT. In this sense, a pair of thermocouples are placed on top and at the bottom of the DUT in order to monitor the thermal operating point and control the heater accordingly. Based on this lab setup, exhaustive measurements were performed on the MOSFET test structures supplied by the foundry. The comparison of these measurements with the cryogenic simulation of the standard BSIM3 parameters (extracted from 25°C to 125°C) showed unacceptable results, as in Fig.7(b). Since stable cryogenic operation is mandatory to keep the sensitivity of the QWIP plane in the system of Fig. 1(a), the measured data was used to extract specific BSIM3 parameters [7] valid only for the cryogenic range (<-140°C), as illustrated in Fig.7(b). Basically, thermal coefficients related to mobility (`UTE`) and drain/source resistance (`PRT`) were adjusted.

Based on the new MOSFET model values, the design parameters for the proposed circuits have been chosen to be: I_{bias}=5μA, N=5, $C_{int/CDS}$=120fF, C_{test}=60fF, C_A=0.96pF, C_B=0.55pF, and a maximum load capacitance of 10pF. The resulting integrated test vehicle is shown in Fig.8(a). This prototype includes an active matrix built from 3 columns of 8 APS cells (8×3). The two lateral columns are used to evaluate the crosstalk between adjacent APS cells, while a long dummy serpent is attached to the central column to emulate the load of a full 256-pixel length column. Each active column has its own pixel multiplexing circuit according to Fig.4, and all three columns are connected to the column multiplexer and output buffer of Fig.6. Hence, a single video signal of 24-pixel length is generated. Additionally, a custom-made low-voltage differential signaling (LVDS) input driver has been implemented for the external digital clock to minimize crosstalk with the analog video output. A detailed view of the 50μm×100μm APS cell is shown in Fig.8(b). As it can be seen, the APS cell is also supplying the common

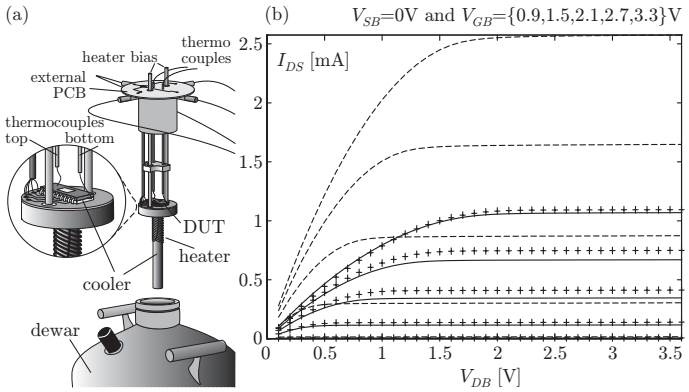

Fig. 7. Custom made lab setup for measurements at cryogenic temperatures (a), and 10μm/10μm MOSFET output curve comparison (b) between experimental (cross), standard room-temperature (dashed) and new cryogenic (solid) extracted BSIM3 models.

biasing pads of the sensor array in order to compensate for possible breaks in the hybrid packaging of Fig.1. Using a lab setup similar to Fig.7(a) combined with the direct test input port introduced in Fig.3(b), the performance of the APS cells has been experimentally measured at cryogenic temperature, as shown in the example of Fig.9 and summarized in Table I. According to this data, the proposed basic building blocks are able to read out >64k columns per second of 256-pixel each. Hence, cryogenic IR video at 25fps is feasible to be obtained in the target system of Fig.1 with frame sizes up to 256×2560-pixel for monochrome, resulting in theoretical FPA power and area figures of about 5.1mW and 1.3mm^2, respectively. In contrast, a fixed 256×2560 FPA would require an equivalent silicon area of more than 30cm^2, which is not practical in terms of production yield and integration costs, and an overall power consumption >10W. Compared to [4], [5], [8], the proposed basic building blocks allow faster multiplexing (more than 10 times) with a similar power consumption.

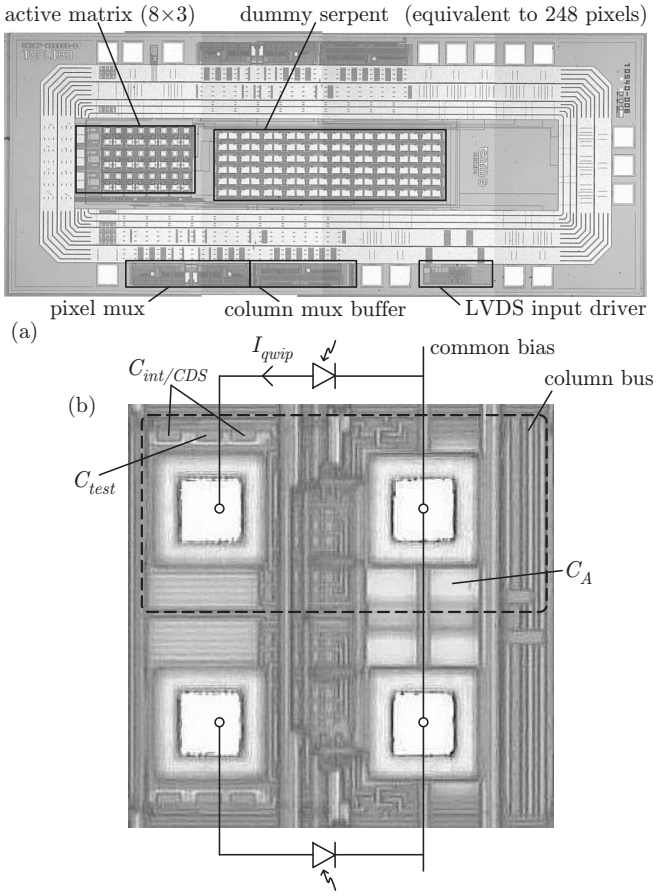

Fig. 8. Microscope photography of the test vehicle (a, 1.1mm×2.7mm) and the APS cell (b, boxed 50μm×100μm) including sensor bumping pads for the common voltage biasing (right) and the individual current sensing (left).

V. Conclusions

A complete set of CMOS basic building blocks has been proposed for low-cost scanning infrared cryogenic imagers. The low-power and compact novel circuits implement single-capacitor integration and correlated double sampling, embedded test at pixel level, pixel charge-multiplexing and video

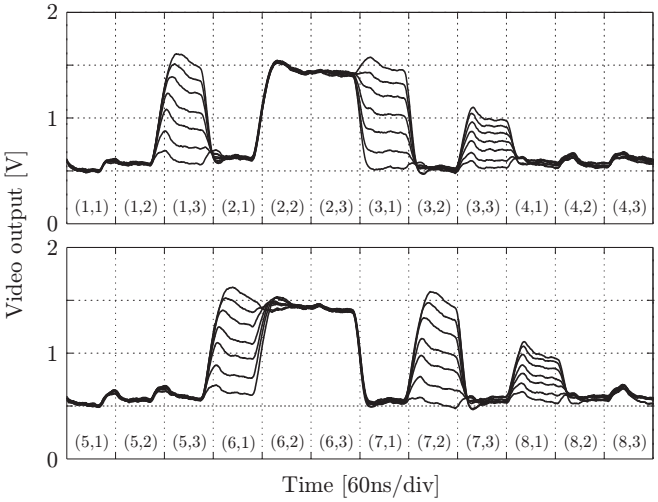

Fig. 9. Experimental video output at 77K for different V_{test} DC values applied to some selected APS cells following Fig.3(b). Pair numbers in brackets indicate pixel position in the 8×3 FPA of Fig.8(a).

TABLE I
Experimental results of the proposed APS cell at 77K.

Parameter	Value	Units
I_{qwip} full scale	5	nA
T_{int}	15.6	μs
V_{out} full scale	1	V_{pp}
Supply voltage	3.3	V
Static consumption	< 20	μW
Read-out consumption	< 30	μW
Read out time	60	ns

composition. Also, experimental results are reported in standard 0.35μm CMOS technology for a 50μm×100μm APS cell operating at 77K and capable of capturing high resolution and real time IR images. Based on these basic building blocks, a low-cost and low-power IR imager capable of capturing up to 256×2560 pixels at 25fps can be implemented.

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