# A 0.3mW/Ch 1.25V Piezo-Resistance Digital ROIC for Liquid Dispensing MEMS

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***Abstract*—A low-power multi-channel CMOS digital read-out IC (ROIC) for differential piezo-resistive sensing is presented as part of the positioning system of a liquid dispensing MEMS. New very low-voltage and single-battery compatible CMOS circuits are proposed for digital gain tuning, pre-amplification and integrating A/D conversion. Overall low-power consumption is achieved by operating the key devices in subthreshold in order to prevent from heating the fluidic MEMS. A complete quad-channel ROIC has been integrated in 0.35$\mu$m CMOS 2-polySi 4-metal technology. The reported experimental results agree with the electrical simulations.**

***Index Terms*—Piezo-resistive sensors, CMOS interface circuits, analog-to-digital (A/D) conversion, pulse density modulation (PDM), micro-electro-mechanical systems (MEMS).**

## I. Introduction

THE interest in patterning surfaces with micrometer resolution droplets has been growing fast in recent years, specially for photonics, molecular electronics, and biosensors. In particular, the accurate registry of small amounts of molecules or particles in well-defined areas along with their specific properties is of great significance for high sensitivity and fast screening applications. For such purposes, the combination of micro-electro-mechanical systems (MEMS) and CMOS circuits is very promising, as it has been proven in other fields when integrating sensors [1]–[4], actuators [5] and RF devices [6]. From the technological viewpoint, microcantilevers are preferred for liquid dispensing, since they allow a direct patterning of the surface with different kinds of materials without any need for prefabricated patterns [7]. Furthermore, alignment of the tips with respect to specific regions on the surface is straightforward, since the cantilevers themselves can be used as displacement sensors if piezo-resistors are integrated in the same MEMS structure [8]. A dummy piezo-resistor is also introduced as a reference to cancel thermal, mechanical and electrical noise and disturbing spurious from the weak stress signal. However, positioning problems arise in practice from the technological mismatching between these integrated piezo-resistive sensors.

This paper presents a low-power multi-channel CMOS digital read-out IC (ROIC) for differential piezo-resistive sensing, as part of the positioning system of a liquid dispensing MEMS. Parallel channel processing, including integrating A/D conversion, is implemented in this ROIC to narrow the equivalent noise bandwidth and minimize inter channel crosstalk. In order to overcome possible issues from the mismatching of the integrated piezo-resistive sensors, a digital gain tuning mechanism is introduced for each individual reading channel. Moreover, very low-voltage circuit CMOS techniques compatible with single battery operation are proposed to isolate ground and to obtain a compact packaging. The reported designs are also optimized for low-power consumption to prevent from heating and drying the fluidic MEMS in future monolithic solutions. Next section introduces the MEMS scenario, while Section III proposes a suitable ROIC architecture. Then, very low-voltage and low-power CMOS circuit proposals for input gain tuning, differential pre-amplification and integrating A/D conversion are described in Sections IV, V and VI, respectively. The overall ROIC design is detailed in Section VII, together with the experimental results of Section VIII. Finally, conclusions are summarized in Section IX.

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## II. MEMS Description

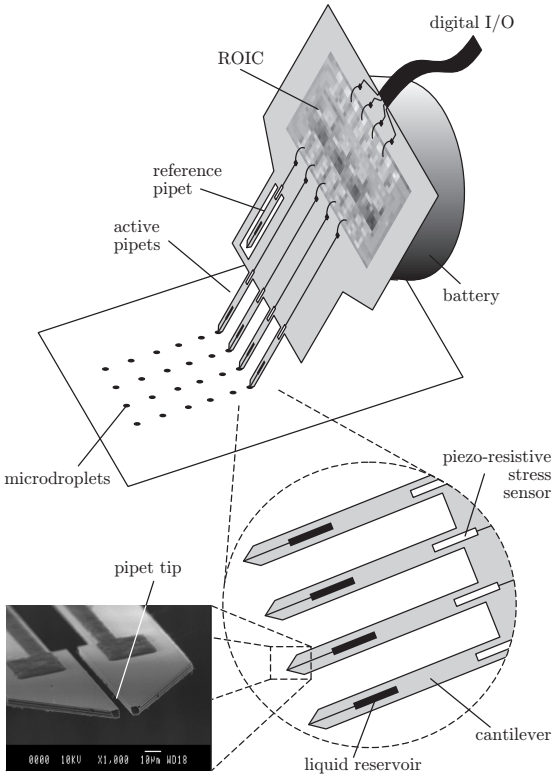


Figure 1. Exploded view of the liquid dispensing MEMS based on [7] to be monitored by the ROIC. Drawing not in scale.

The general concept of the liquid dispensing MEMS is illustrated in Figure 1: a set of cantilever-based micropipets equipped with their corresponding liquid reservoirs are operated in parallel to pattern arrays of microdoplets in a given surface. Piezo-resistors are also integrated in the same cantilevers to sense the stress of the micropipet when its tip is in touch with the surface. In practice, the mismatch of these piezoresistors causes tilt errors when positioning the MEMS head respect to the patterned surface. As a consequence, both droplet diameter and shape created by each micropipet are non-uniform [8]. In order to compensate for such an issue, a dedicated ROIC is placed close to the fluidic MEMS.

In practice, a dummy micropipet is also included to cancel thermal, mechanical and electrical piezo-resistance deviations. However, these integrated sensors exhibit very poor technological matching, as depicted in Figure 2, where $R_{sens}$ and $R_{ref}$ stand for the active and reference piezo-resistive sensors, respectively, while $R_{sens} - R_{ref}$ is the effective stress signal to be measured. From the same figure, it is clear that the main design bottleneck comes from the combination of both, the sensor mismatching and the amplitude of the dynamic disturbing signals. Such unwanted variations coming from the environment, even in pure common mode, are partly seen as an input differential residual due to the unbalancing between $R_{sens}$ and $R_{ref}$, so they can not be completely rejected just by differential reading.

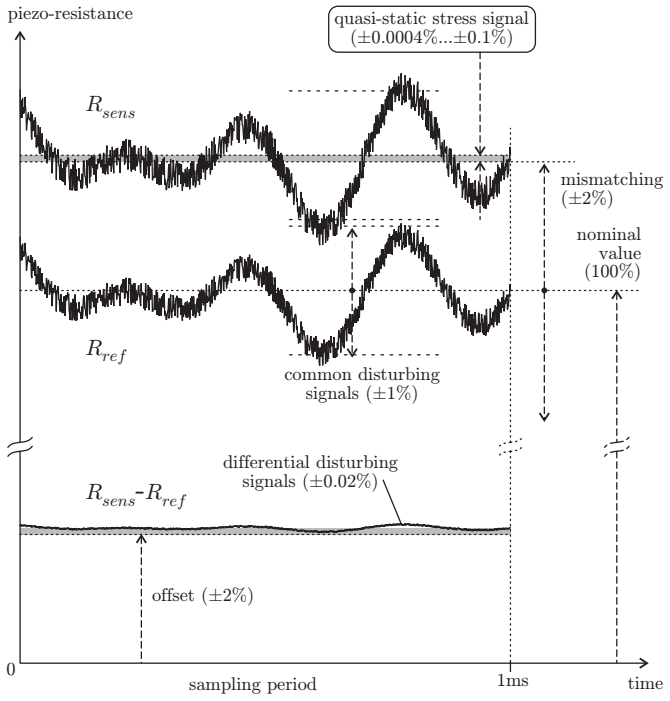


Figure 2. Integrated piezo-resistor specifications and differential sensor read-out scenario without gain calibration. Drawing not in scale.

Following Figure 2, the resulting disturbing residual after differential reading is about $\pm 1\% \times 2\% = \pm 0.02\%$, which is $\pm$50LSB for 1LSB=$\pm 0.0004\%$, and it can not be compensated by digital postprocessing due to its dynamic nature. Hence, a calibration method for the gain of each read-out channel is required in the ROIC. This mechanism must compensate a maximum individual gain adjustment of up to $\pm 2\%$, while ensuring a gain accuracy of $\pm$0.5LSB/2%=$\pm 0.01\%$, resulting in a gain dynamic range of 8+1 bit. In that case, the residual offset can still be up to $\pm 0.01\%$ ($\pm$25LSB), but this static component is easily compensable by digital post-processing. Anyway, even if exact balancing is obtained between $R_{sens}$ and $R_{ref}$ after this gain calibration, the ROIC must exhibit a common mode rejection ratio ($CMRR$) as large as 1%/0.5LSB$\simeq$75dB against the truely common disturbing signals.

## III. ROIC Architecture

Taking into account all the specifications of Section II, the ROIC architecture of Figure 3 is proposed, where $V_{bias}$ stands for the sensors common bias voltage. Basically, the system behaves as four independent digital read-out channels, operating in parallel in order to reduce the equivalent noise bandwidth.

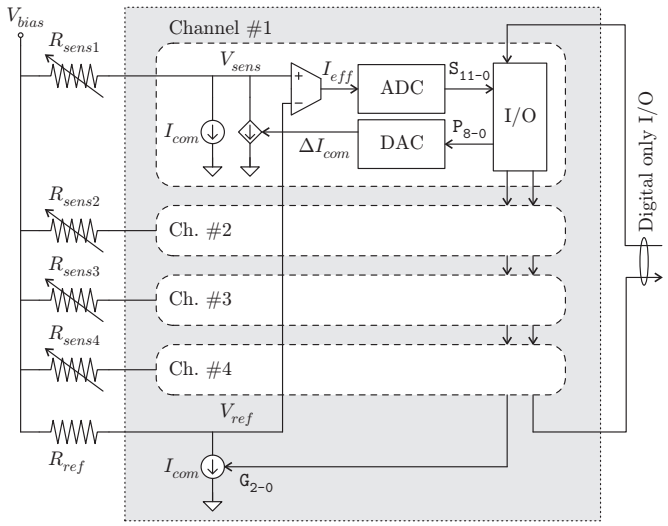


Figure 3. Architecture at block level of the proposed ROIC.

Signal processing starts by calibrating the individual sensor current bias around the common level $I_{com}$ with the current D/A converter (DAC), which allows the gain adjustment at each input according to $V_{sens} = (I_{com} \pm \Delta I_{com}) R_{sens}$. Then, pre-amplification and differential to single-ended conversion is performed through the operational trans-conductance amplifier (OTA), generating an stress effective current $I_{eff}$ to be quantified during $T_{int}$ by the integrating A/D converter (ADC). Finally, the serial digital interface (I/O) is in charge of the sensor read-out ($S_{11-0}$), and also of the programming-in ($P_{8-0}$) for the individual channel gain calibration. Apart from the fine tuning of $\Delta I_{com}$, the system also allows to change the common $I_{com}$ value for all channels as a coarse gain digital configuration ($G_{2-0}$).

## IV. Input Gain Tuning

The first step of the signal processing chain in Figure 3 is to convert the piezo-resistance change of $R_{sens}$ coming from the stress sensor into the voltage-domain signal $V_{sens}$ by means of

a constant current biasing $I_{com}$. In order to cancel unwanted components not related with the stress measurement itself, the dummy sensor $R_{ref}$ is included for the differential reading:

$$V_{sens} - V_{ref} = I_{com}\left(R_{sens} - R_{ref}\right) \tag{1}$$

As already explained, a fine balancing of the differential gain is required for the compensation of the technology mismatching between $R_{sens}$ and $R_{ref}$, and between their $I_{com}$ sources as well. For such a purpose, the calibration of $\Delta I_{com}$ for each channel is proposed:

$$V_{sens} - V_{ref} = I_{com}\left[R_{sens}\left(1 \pm \frac{\Delta I_{com}}{I_{com}}\right) - R_{ref}\right] \tag{2}$$

In fact, this strategy also allows the compensation of any unbalance coming from circuit asymmetries in the differential OTA of Section V. The current-mode DAC of Figure 4(upper) is proposed to control the value of $\Delta I_{com}$ through $\mathtt{P}_{8\text{-}0}$.

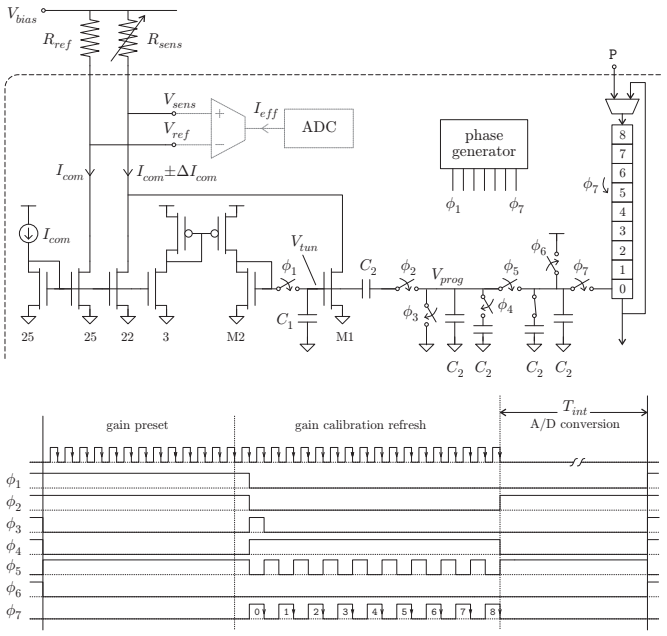


Figure 4. CMOS implementation (upper) and operation (lower) of the proposed current-mode DAC.

Basically, M1 acts as a voltage controlled current source capable of adding $12\%I_{com} \pm \Delta I_{com}$ to the $88\%I_{com}$ biasing of $R_{sens}$ according to the $C_2$-based switched-capacitor DAC [9] and the chronogram of Figure 4(lower). This mixed DAC architecture is proposed to limit the technological matching requirements to a few passive components only. The basic operation of this equivalent current-mode DAC is as follows. Firstly, the two capacitors $C_1$ and $C_2$ connected to the gate of M2 are precharged by setting $V_{tun}$=$V_{GB2}$, so $I_{D2}$=$I_{D1}\equiv 12\%I_{com}$, and $V_{prog}\simeq V_{DD}/2$, as $C_1 \gg C_2$, being $V_{DD}$ the supply voltage. Secondly, $V_{tun}$ is disconnected from $V_{prog}$, which in turn is serially programmed through the $C_2$-based switched capacitor network:

$$V_{prog} = V_{DD}\sum_{i=0}^{8}\frac{\mathtt{P}_{8-i}}{2^{i+1}} \tag{3}$$

Once generated, the value of $V_{prog}$ is dumped into the gate of M2 using the capacitive divider $C_1$ and $C_2$, and kept constant during the A/D conversion phase, typically around 1ms:

$$V_{tun} = V_{GB2} + \underbrace{\frac{C_2}{C_1 + C_2}\left(V_{prog} - \frac{V_{DD}}{2}\right)}_{\Delta V_{tun}} \tag{4}$$

Choosing $C_1 \gg C_2$ and $(W/L)_{1,2} \ll 1$ in order to operate M1 and M2 in deep strong inversion, the resulting calibrating current can be expressed as:

$$\begin{aligned}\Delta I_{com} &\simeq gm_{g1}\Delta V_{tun} \\ &\simeq \sqrt{\frac{2\beta_1 12\%I_{com}}{n}}\frac{C_2}{C_1}\left(\sum_{i=0}^{8}\frac{\mathtt{P}_{8-i}}{2^{i+1}} - \frac{1}{2}\right)V_{DD}\end{aligned} \tag{5}$$

where $\beta$ and $n$ stand for the current factor and subthreshold slope, respectively, of the EKV MOSFET model [10]. This routine is repeated before every acquisition period in order to regenerate and avoid degradation of the internal analog memories $V_{prog}$ and $V_{tun}$. Moreover, each channel includes its own DAC to allow fast gain calibration without crosstalk.

## V. Differential Pre-Amplification

Following the general block scheme of Figure 3, this stage is devoted to translate the differential stress voltage into a single ended effective current for its subsequent integrating A/D conversion:

$$I_{eff} = G_m\left(V_{sens} - V_{ref}\right) \tag{6}$$

where $G_m$ stands for the differential transconductance gain. Typically, for a given $R_{sens}\sim$5k$\Omega$ and $I_{com}\sim$200$\mu$A, the dynamic range of the differential stress signal is around $DR(V_{sens}-V_{ref})\sim$1mV/4$\mu$V. Hence, the OTA block implementing this differential pre-amplification must provide in practice both a large $G_m$ to protect stress signal against circuit noise, together with a good $CMRR$ to attenuate dynamic disturbing signals.

Based on the above requirements, the low-voltage OTA implementation of Figure 5 is proposed. The circuit core consists of a differential input pair (M1-M2) followed by a folded cascode output stage (M3-M8). In this sense, M1-M2 are operated in weak inversion to optimize transconductance versus power consumption, while M3-M8 are biased in strong inversion for a lower technology mismatching.

The full non-linear expression for the transconductance of the OTA presented in Figure 5 is found to be:

$$\begin{aligned}I_{eff} &= 2I_{biasn}\frac{e^{\frac{V_{sens}-V_{ref}}{nU_t}} - 1}{e^{\frac{V_{sens}-V_{ref}}{nU_t}} + 1} \\ &= 2I_{biasn}\tanh\left(\frac{V_{sens} - V_{ref}}{2nU_t}\right)\end{aligned} \tag{7}$$

being $U_t$ the thermal potential. Due to the limited range of the differential input signal $\left|\frac{V_{sens}-V_{ref}}{2nU_t}\right|$<0.04, the maximum

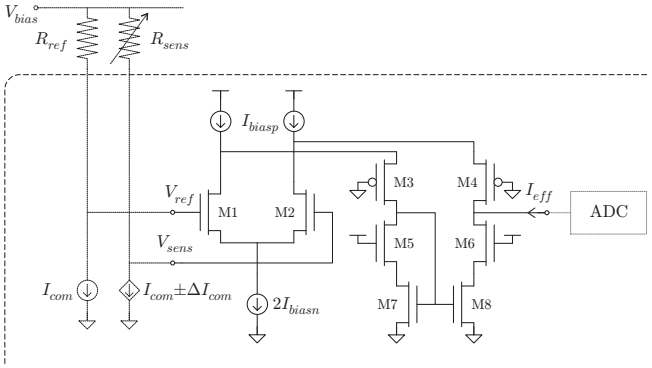


Figure 5. Low-voltage CMOS implementation of the OTA block.

linearity errors at full-scale are below ±LSB/100, so the equivalent transconductance of the OTA stage can be simplified to:

$$G_m = \frac{I_{biasn}}{nU_t} \quad \text{for} \quad |V_{sens} - V_{ref}| \ll 2nU_t \tag{8}$$

For our purposes, a transconductance gain of $G_m \geq 0.8$mS is chosen in order to obtain an equivalent input integrated noise up to 1kHz of $V_{neq} \leq 2\mu V_{rms}$ (including $I_{com}$ sources). Hence, the resulting dynamic range of the single ended effective current becomes $DR(I_{eff}) \sim 1\mu$A/4nA.

Concerning the $CMRR$ performance of Figure 5, circuit differential asymmetries and common biasing sensitivities limit its final value to:

$$\frac{1}{CMRR} = \frac{\Delta G_m}{G_m}\left(1 - \frac{1}{1 + \frac{1}{2nG_m R_{tail}}}\right) \tag{9}$$

where $\Delta G_m$ stands for the unbalancing of $G_m$ between $V_{sens}$ and $V_{ref}$, mainly due to the mismatching between M1 and M2 from technology, geometry, temperature or biasing asymmetries, while $R_{tail}$ is the output impedance of $I_{biasn}$. Either due to a perfect matching between the differential parts ($\Delta G_m \to 0$) or due to a very high output impedance of the common biasing ($R_{tail} \to \infty$), rejection should tend to be ideal ($CMRR \to \infty$). Unfortunately, none of these scenarios are really feasible. In practice, large device areas must be selected for M1-M2 and long aspect ratios for the MOS devices of $I_{biasn}$ to meet the $CMRR$ specifications of Section II. Also, due to the low-voltage operation of the ROIC, this rejection ratio can only be achieved for a limited range of the common mode input voltage:

$$V_{com} \doteq \frac{V_{sens} + V_{ref}}{2} \tag{10}$$

Hence, the biasing level of the piezo-resistive sensors of Figure 3 must be adjusted to ensure a suitable $V_{com}$ according to the characteristics of the sensor ($R_{sens}$) and the $I_{com}$ bias level programmed from the ROIC:

$$V_{bias} = V_{com} + I_{com} R_{sens} \tag{11}$$

## VI. Integrating A/D Conversion

For the digital quantization of the quasi-static stress signal $I_{eff}$ in Figure 3, the predictive ADC architecture of Figure 6 is chosen, which is inspired in spike-counting A/D techniques applied in neural networks [11], [12] and digital imagers [13]–[15]. Basically, the pulse density modulation (PDM) stage is in charge of integrating the current-mode signal and pushing the quantization noise to higher frequencies. Then, the counter stage can filter such unwanted frequency components in the digital domain.

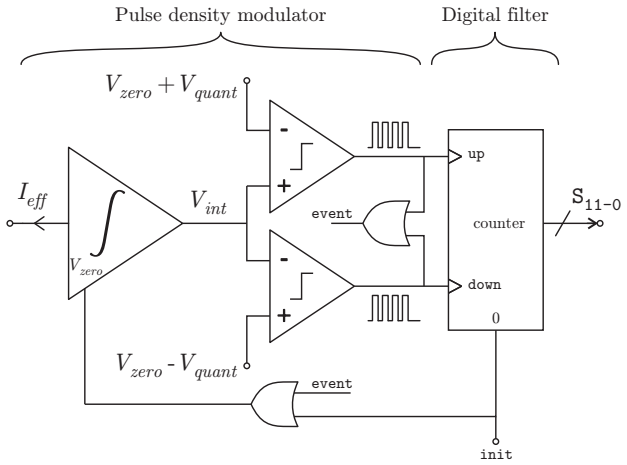


Figure 6. Architecture of the predictive ADC at block level.

Its principle of operation is as follows: during initialization (`init`=1), both the analog integrator of the PDM stage and the digital counter are reset; once in conversion (`init`=0), the stress quasi-static current $I_{eff}$ is integrated into $V_{int}$; when $V_{int}$ reaches the quantizer threshold $\pm V_{quant}$ (depending on the polarity of the stress signal $I_{eff}$), the window comparator generates the corresponding pulse, which is sent to the digital counter and also fed back to the first stage as the reset signal (`event`=1), making $V_{int}$ to return to its zero signal level ($V_{zero}$). The ideal waveforms of this operation cycle are illustrated in Figure 8(a). Due to the nature of the MEMS application of Figure 1, the scheme of Figure 6 will be only operated in practice for a single $I_{eff}$ phase, either positive or negative but not simultaneous. Hence, this predictive ADC behaves as having a single bit quantizer inside the PDM loop, with all the advantages in terms of inner linearity and mismatching insensitivity.

At the end of the acquisition time $T_{int}$, the integrating A/D conversion is completed and the state of the digital counter should be:

$$\begin{aligned} \mathtt{S}_{11\text{-}0} &= \pm\frac{T_{int}}{C_{int}V_{quant}} I_{eff} \\ &= \pm\frac{G_m T_{int}}{C_{int}V_{quant}} I_{com}\left[R_{sens}\left(1 \pm \frac{\Delta I_{com}}{I_{com}}\right) - R_{ref}\right] \end{aligned} \tag{12}$$

where $C_{int}$ is the analog integrator capacitance. Hence, the overall gain of the ROIC for a relative piezo-resistance deviation ($\pm\Delta R_{sens}/R_{sens}$) is:

$$\left|\frac{\mathtt{S_{11\text{-}0}}}{\Delta R_{sens}/R_{sens}}\right| = \frac{G_m T_{int}}{C_{int} V_{quant}} I_{com} R_{sens} \qquad (13)$$

Typically, the integration of $I_{eff}$ in the PDM stage of Figure 6 is implemented using the circuit classical topology [16], [17] of Figure 7(a): during initialization (init=1), the integration capacitor $C_{int}$ is reset, while the correlated double sampling (CDS) capacitor $C_{CDS}$ samples the output noise of the analog integrator; once in conversion (init=0), $I_{eff}$ is integrated in $C_{int}$ and the series $C_{CDS}$ performs cancellation of the integrator offset and low frequency noise at $V_{int}$.

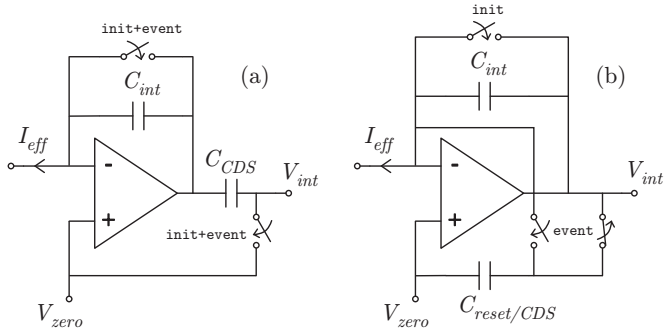


Figure 7. Classical (a) and novel (b) reset scheme proposal for the analog integrator of the PDM stage of Figure 6.

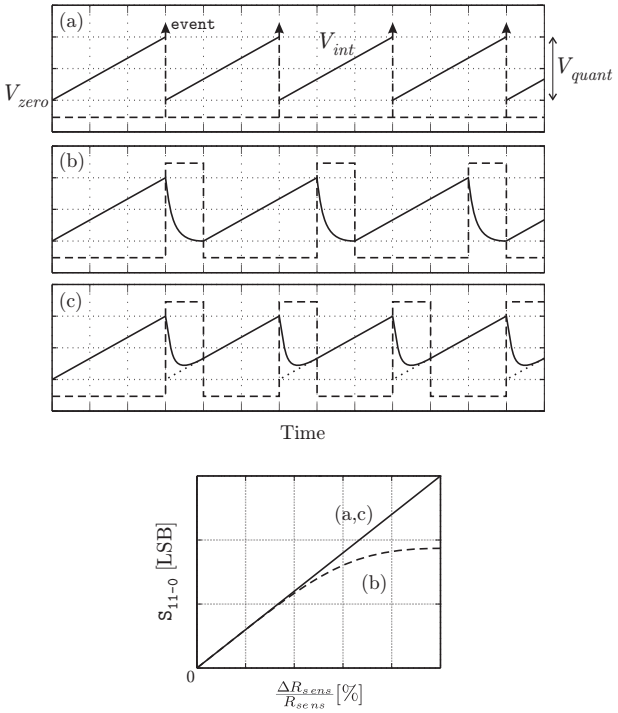


Figure 8. ADC transient operation (upper) and equivalent transfer curve (bottom) for positive $I_{eff}$ values according to the ideal (a), classical (b) and proposed (c) PDM schemes. Drawings not in scale.

However, due to the low-voltage supply operation of the switching devices, the event duration in Figure 8(a) can not be null in practice. Hence, some time is lost at each pulse generation in order to reset the analog integrator, as depicted in Figure 8(b). According to Figure 7(a), no integration in $C_{int}$ is possible during this event time, so the resulting pulse frequency in Figure 8(b) is decreased compared to the ideal case of Figure 8(a). This effect is specially important at full-scale of $|I_{eff}|$, where the pulse period is small and comparable to the reset time, so causing saturation of the ADC curve, as shown in the same Figure 8. Hence, reset time forces in general to waste more power in the analog blocks of the ADC for minimizing these non-linearity problems.

In order to overcome this issue, the alternative analog integrator scheme of Figure 7(b) is proposed, which does not use a hard short circuit but a novel switched-capacitor technique to reset $C_{int}$. In this case, the principle of operation is as follows: during initialization (init=1), $C_{int}$ is reset, while $C_{reset/CDS}$ remains connected to $V_{int}$; once in conversion (init=0), the stress quasi-static current $I_{eff}$ is integrated in $C_{int}$ while $C_{reset/CDS}$ is tracking the offset, the low frequency noise and the output signal itself of the amplfier; when the fixed threshold $\pm V_{quant}$ is reached, the window comparator generates the corresponding pulse, which is again sent to the digital counter, but in this case it also causes $C_{reset/CDS}$ to be connected to the input of the analog integrator (event=1). As a result, the charge stored in $C_{int}$ is compensated by $C_{reset/CDS}$ and the reset is performed. However and unlike in the classical implementation of Figure 7(a), this novel strategy does not block the integration in $C_{int}$ during the event time, combining both the charge coming from $I_{eff}$ and from $C_{reset/CDS}$ as illustrated in Figure 8(c). In consequence, the pulse frequency is no longer dependent on the reset time and matches (12). Furthermore, since $C_{reset/CDS}$ is continuously sampling the offset and the low frequency noise of the analog integrator, it already implements the CDS function.

Based on the new PDM scheme, low-voltage CMOS circuits are proposed in Figure 9 for the analog integrator and the window comparator. The first stage is based on the single-transistor capacitive transimpedance amplifier (CTIA) built around M1. A second matched device M2 configured as active load is used to obtain the appropriate $V_{zero}$ level together with a low enough output impedance for the new reset scheme of Figure 7(b). In fact, by choosing the same ratio between $\frac{I_{biasi}}{(W/L)_{1,2}}$ of Figure 9(a) and $\frac{I_{biasp}-I_{biasn}}{(W/L)_{7,8}}$ of Figure 5, the input of the CTIA is biased at the same potential as the gate of M7 in Figure 5. As a result, the node voltages of the OTA of Figure 5 are fully balanced, and the $CMRR$ is enhanced thanks to the corresponding decrease of $\Delta G_m$ in (9).

Concerning the window comparator, the dual N/PMOS structure of Figure 9(b) is proposed. Apart from its low-voltage compatibility, the dynamic current biasing supplied by M3 due to the positive feedback from M4 allows both a static low-power consumption ($I_{biasc}$) together with short transient times.

Finally, the required threshold levels for the window comparator of Figure 6 are obtained from the modular and floating generator of Figure 10. This CMOS circuit consists of two parts: a low-voltage stacked structure MA-MB, in charge of generating the relative threshold $V_{quant}$, and a switched-capacitor network to derive the absolute levels $V_{zero} \pm V_{quant}$. Concerning the generation of $V_{quant}$, and supposing weak

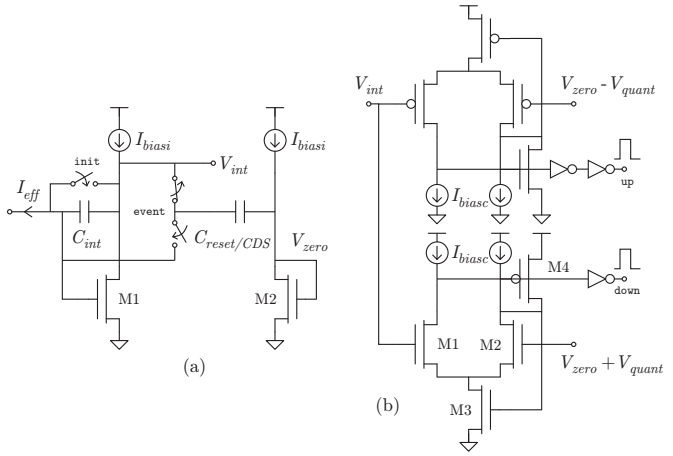


Figure 9. Low-voltage CMOS integrator (a) and window comparator (b) for the PDM blocks of Figure 6.

inversion conduction for MA$i$ devices and saturation for MB$i$ devices, each stacked block contributes to the total threshold with:

$$\Delta V_{quanti} = U_t \ln\left[\frac{(W/L)_{Bi}}{(W/L)_{Ai}}\left(1+\frac{I_{Bi}}{I_{Ai}}\right)+1\right] \qquad (14)$$

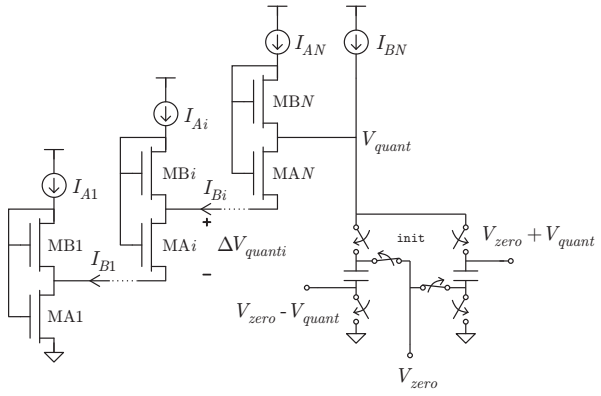


Figure 10. Low-voltage CMOS modular $V_{quant}$ generator proposal for the window comparator of Figure 6.

It is interesting to note that the $U_t$ dependencies here and in (8) require a proportional to absolute temperature (PTAT) current reference like [18] for the biasing of the piezo-resistor sensor ($I_{com}$) and the OTA block ($I_{biasn,p}$) in order to cancel thermal dependencies on the final expression (12).

## VII. System Design

Based on all the low-voltage and low-power CMOS circuits proposed in Sections IV to VI, a complete quad-channel ROIC has been developed following Figure 3. The main design parameters for all the ROIC blocks are summarized in Table I.

According to (8), the transconductance of the pre-amplifier is chosen to be $G_m \simeq 0.8$mS, while the Montecarlo simulation in Figure 11 reports a large enough $CMRR$ for $V_{com} \sim 1$V. Concerning the predictive A/D converter, the fixed threshold voltage of the PDM stage is designed through (14), resulting in $V_{quant} \simeq 300$mV at room temperature. The rest of performance results from simulation are listed in Table II for their comparison with the experimental data of Section VIII. In this sense, the theoretical relative gain from (13) for $R_{sens}=5\text{k}\Omega$, $I_{com} \simeq 189\mu$A and $T_{int}=1$ms returns an estimated $\left|\frac{\text{S}_{11\text{-}0}}{\Delta R_{sens}/R_{sens}}\right| \simeq 6$kLSB/%, which agrees with the full-chip simulations of Figure 12.

Finally, the complete ROIC has been integrated in 0.35$\mu$m CMOS 2-polySi 4-metal technology from AMS, as depicted in Figure 13.

Table I
ROIC main design parameters.

| Parameter | Value | Units |
|---|---|---|
| $C_1$ | 9 | pF |
| $C_2$ | 0.5 | pF |
| $I_{biasp}$ | 56 | $\mu$A |
| $I_{biasn}$ | 44 | $\mu$A |
| $I_{biasi}$ | 36 | $\mu$A |
| $I_{biasc}$ | 4 | $\mu$A |
| $C_{int,reset/CDS}$ | 4 | pF |
| $N$ | 3 | - |
| $\frac{(W/L)_{Bi}}{(W/L)_{Ai}}$ | 3 | - |
| $I_{B3}=10I_{A1-3}$ | 1.5 | $\mu$A |

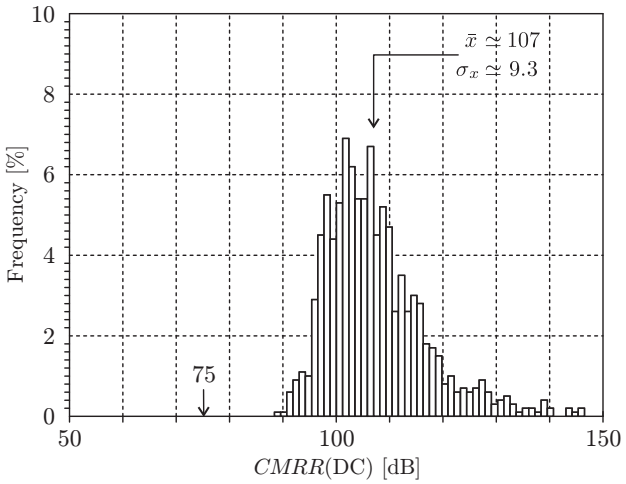


Figure 11. Simulated common mode rejection ratio of the pre-amplifier stage versus technology mismatching for $V_{com}=1$V.

## VIII. Experimental Results

Since the real scenario of Figure 1 does not allow the separated characterization of the ROIC part, the specific setup of Figure 14 has been developed for the detailed test of the integrated circuit of Figure 13. Firstly, the sensor bias and calibration capabilities of the ROIC are verified using the low-noise current pre-amplifier SRS SR570, together with a standard oscilloscope Tektronix TDS2024. Secondly, the full signal processing chain, including the pre-amplification and integrating A/D conversion stages, is characterized using the ultra low-noise function generator SRS DS360, together with the multifunction synthesizer HP 8904A. In both cases, all the digital I/O communications for programming $\text{G}_{2\text{-}0}$ and $\text{P}_{8\text{-}0}$

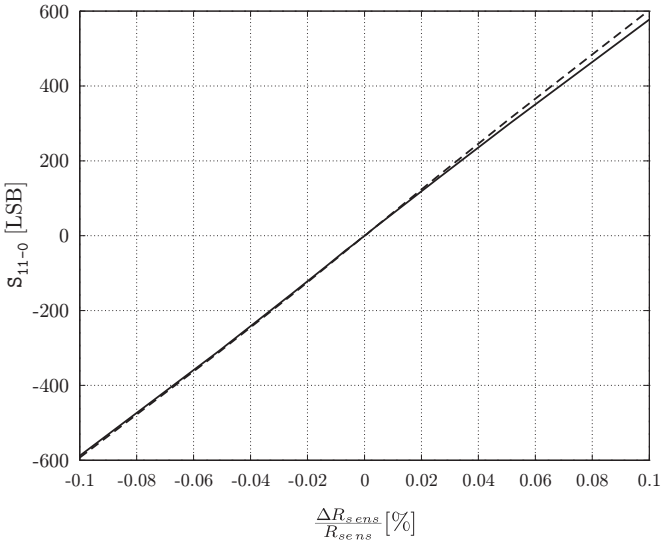


Figure 12. Pre (dashed) and post (solid) layout simulation of the ROIC relative transfer function after calibration for $R_{sens}$=5kΩ, $I_{com}$=189$\mu$A and $T_{int}$=1ms.

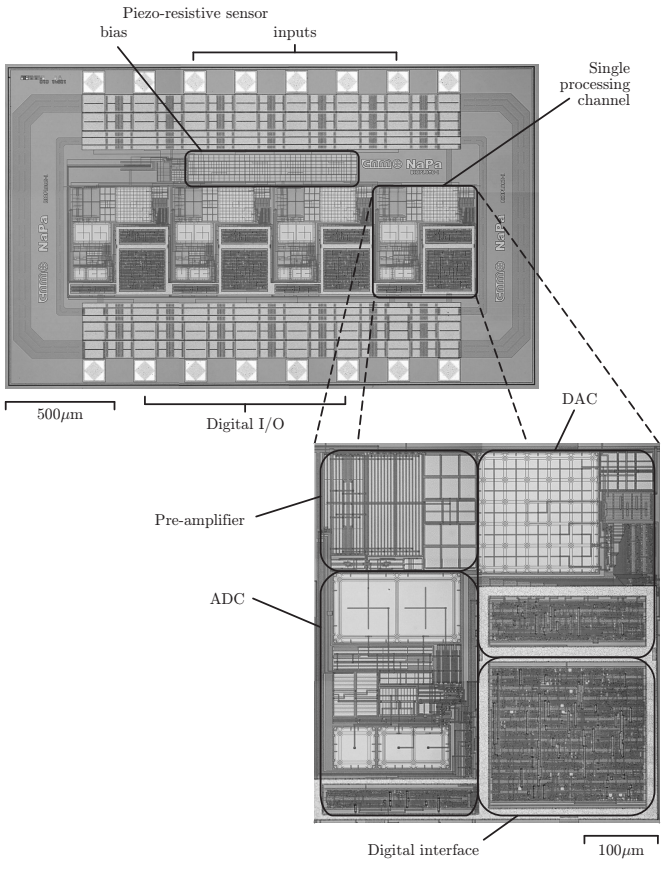


Figure 13. Microscope photography of the ROIC (top) and a single processing channel (bottom). The overall size is 2.4mm×1.3mm=3.1mm$^2$.

and reading $S_{11\text{-}0}$ are controlled through the logic analyzer Tektronix TLA 721.

The complete set of experimental results is reported in Table II and Figures 14 to 17. Concerning the differential transfer curve of the ROIC, an equivalent gain of 0.5LSB/$\mu$V is obtained from Figure 15. The -2dB error between the

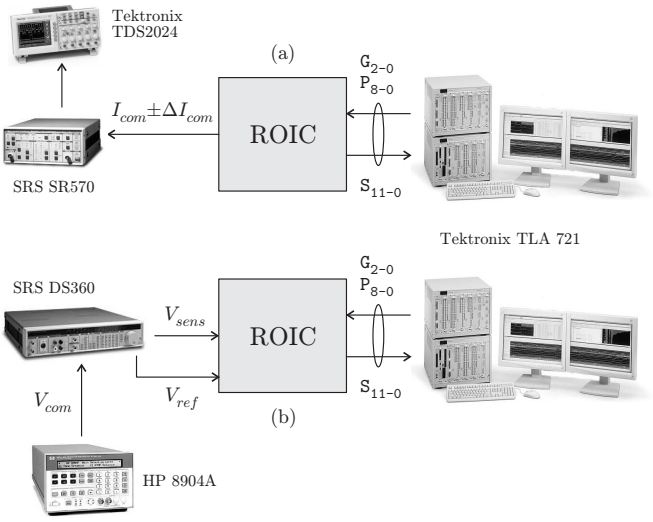


Figure 14. Experimental ROIC test setup for the sensor calibration (a) and transfer function (b) measurements.

simulated and the experimental gain is probably due to $C_{int}$ deviations in (13) caused by process spread. The ADC transfer function is affected by a gain asymmetry between the positive and negative input range caused by the technology mismatching of $\pm V_{quant}$ in the generator of Figure 10. However, this gain error can be neglected here since the liquid dispensing MEMS system of Figure 1 does not require simultaneous reading of positive and negative input signals. Actually, the ROIC exhibits a remarkable linearity for each of the signal polarities, even well above the full-scale. Since just a single polarity is required in each acquisition, the gain balancing can be obtained by simple scaling during post-processing. The ROIC resolution is extracted from averaging several plots like Figure 16, but the value given in Table II is limited by the noise of the test setup. For the characterization of the $CMRR$, a common input voltage sweep ($\Delta V_{com}$) is performed in Figure 17, measuring a sensitivity of less than 0.5LSB for more than 100mV of change in $V_{com}$ for all the tested samples. Hence, the equivalent $CMRR$ is $>\frac{0.5\text{LSB}/\mu\text{V}}{0.5\text{LSB}/100\text{mV}}$=100dB, as expected from the statistical simulation of Figure 11.

## IX. Conclusions

A CMOS digital ROIC is presented for multi-channel and differential piezo-resistive sensing, as part of the positioning system of a liquid dispensing MEMS. Very low-voltage circuits, combined with low-power subthreshold operation, have been proposed for the digital gain tuning, pre-amplification and integrating A/D conversion required inside the ROIC. The complete system has been integrated in 0.35$\mu$m CMOS 2-polySi 4-metal technology, showing good agreement between simulation and experimental results.

## Acknowledgment

The partial financial supports of the EC-funded project NaPa (Contract no. NMP4-CT-2003-500120) is gratefully acknowledged.

Table II
ROIC COMPARATIVE RESULTS.

| Parameter | Simulation | Experimental | Units |
|---|---|---|---|
| Supply voltage $V_{DD}$ | 1.25 | | V |
| Common input $V_{com}$ | 1 | | V |
| Sensor bias levels $I_{com}$ | | | |
| $G_{2\text{-}0} = 000$ | 76 | 73 | $\mu$A |
| 001 | 95 | 91 | |
| 010 | 114 | 111 | |
| 011 | 133 | 129 | |
| 100 | 151 | 146 | |
| 101 | 170 | 164 | |
| 110 | 189 | 184 | |
| 111 | 208 | 202 | |
| Sensor calibration range $\pm\Delta I_{com}/I_{com}(P_{8\text{-}0})$ | $\pm$2 | $\pm$1.8 to $\pm$2 | % |
| Acquisition time $T_{int}$ | 1 | | ms |
| Diff. gain $\left\lvert\frac{S_{11\text{-}0}}{V_{sens}-V_{ref}}\right\rvert$ | 0.63 | 0.50 | LSB/$\mu$V |
| Equivalent input noise | 2 | <4 | $\mu V_{rms}$ |
| $CMRR$ | 107$\pm$9 | >100 | dB |
| Power consumption | 350 | 300 | $\mu$W/Ch |
| Si area | 0.47×0.53=0.25 | | mm$^2$/Ch |

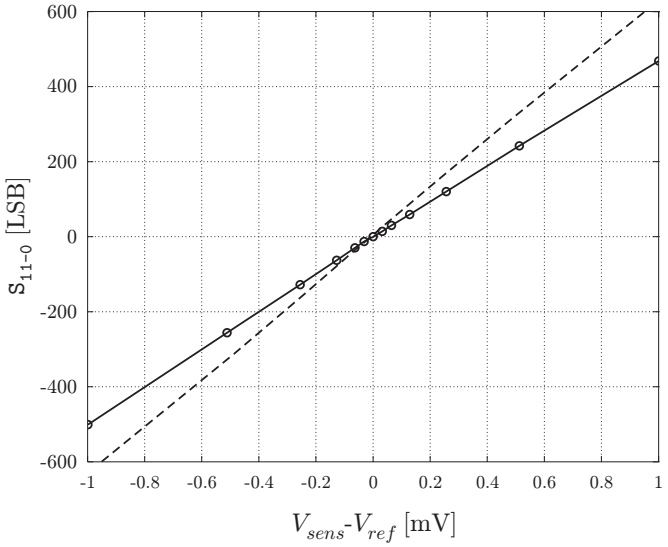


Figure 15. Full-scale experimental (solid) and simulated (dashed) differential transfer curve of the ROIC under the test setup of Figure 14(b).

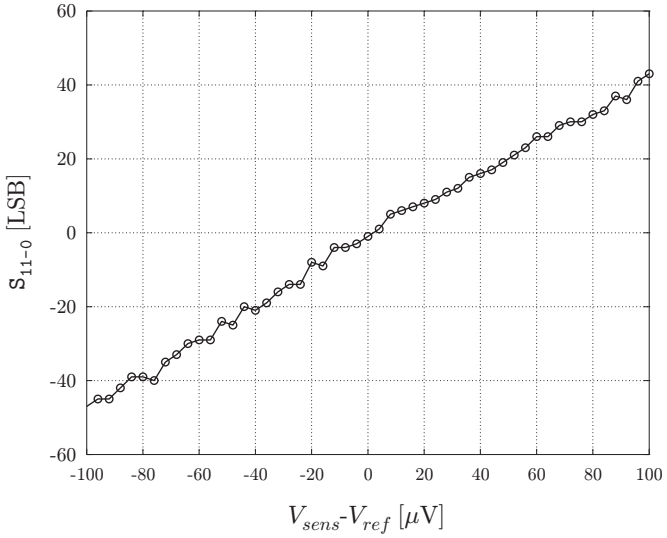


Figure 16. Experimental resolution of the ROIC differential transfer function.

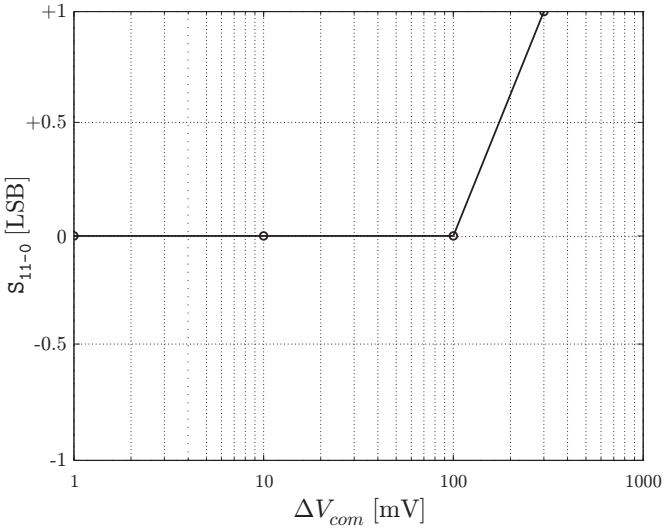


Figure 17. Experimental common transfer function of the ROIC under the test setup of Figure 14(b).

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