J. Sabadell, R. Figueras, J.M. Margarit, E. Martín, L. Terés and F. Serra-Graells,
A 70umx70um CMOS Digital Active Pixel Sensor for Digital Mammography and X-ray Imaging
IOP Journal of Instrumentation, 6:3(C03002), Mar 2011, ISSN 1748-0221
http://dx.doi.org/10.1088/1748-0221/6/03/C0300

A 70µm× 70µm CMOS Digital Active Pixel Sensor for Digital Mammography and X-Ray Imaging

Justo Sabadell[1], Roger Figueras, Josep Maria Margarit, Elena Martín, Lluís Terès and Francisco Serra-Graells

Instituto de Microelectrónica de Barcelona-Centro Nacional de Microelectrónic, IMB-CNM(CSIC), Bellaterra (Barcelona), Spain

E-mail: justo.sabadell@imb-cnm.csic.es

ABSTRACT: This work presents an architecture for CMOS active pixel sensors (APS) based on a novel lossless charge integration method, proposed for X-ray imagers in general but specifically optimized for full-field digital mammography. The objective is to provide all the required functionality inside the pixel, so to use full digital control and read-out signals only, therefore avoiding crosstalk between analog lines over large pixel arrays. It includes a novel lossless A/D conversion scheme besides a self-calibrating dark current cancellation circuit, a self-biasing circuitry, biphasic current sensing for the collection of electrons (e-) or holes (h+) and built-in test. Furthermore, FPN compensation is available by individually addressing the pixel's internal DAC controlling the gain. Implemented in a 0.18 μm 1P6M CMOS technology with MiM capacitors, everything fits into a 70 μm by 70 μm due to the extensive reuse of available blocks and aggressive layout techniques. Also, thanks to the MOSFET subthreshold operation, the average power consumption is as low as 8 μW/pixel.

KEYWORDS: Front-end electronics for detector readout, Pixelated detectors and associated VLSI electronics, X-ray mammography and scinto- and MRI-mammography, X-ray detectors

[1] Corresponding author.

Contents

1. Introduction

It is well acknowledged that screening is likely to reduce breast cancer mortality, which is the second leading cause of death by cancer among women in the United States. Mass screening using mammography can improve early detection by as much as 15–35%. Therefore, it is currently one of the recommended cost-effectiveness screening methods for its early detection, even if its convenience is discussed due to increase on overdiagnosis and overtreatment [1]-[2]. Be that as it may, during last decade, full-field digital mammography is replacing the classic screen-film technology as it has been proved to be more efficient for early detection [3].

An X-ray sensing array of active pixels has a practical pitch requirement in the range of 50μm to 100μm. In the case of direct conversion digital mammography, each digital pixel sensor (DPS) is likely built from the hybrid combination of the X-ray detector (materials ranging from low-cost Si to high-efficient CdTe compounds) and the CMOS read-out circuit cell. The former converts each absorbed photon into electric charge and the latter collects it (being it either electrons or holes) and pre-processes the resulting electrical signal. [4].

This paper deals with the CMOS design techniques for a DPS based on the well known charge integration system. The total charge coming from the detector is simply integrated during the time of exposure and the accumulated total charge is measured at its completion [5].

The specific DPS circuits that may be suitable for X-ray imaging (pulsed currents) are usually based on photon-counting A/D conversion [6]-[9], so they tend to suffer from signal losses due to pile-up and charge-sharing between neighboring pixels. Besides, it can be discussed if a photon counting system might be the best solution on every given application involving radiation detection, as its inherent advantages wanes when large rates and signal currents or particles are expected [10]-[11]. Truly enough, a charge integrating system meets its match there where photon counting excels, when measuring small signals or when requiring spectral information.

This paper presents a description and operation of a novel CMOS DPS circuit specifically conceived for digital mammography with self-bias capability, dark current autocalibration, built-in test, selectable e^-/h^+ collection, lossless charge-integration A/D conversion suitable for X-ray current patterns and an individual pixel gain programming mechanism for fixed pattern noise cancellation. The CMOS circuits proposed here exploit subthreshold operation of the MOS transistor together with exhaustive circuit reuse inside the pixel in order to achieve a very low-power and compact DPS cell, respectively. Worth to mention, this work is based on a preliminary proposal from the same authors [12], but with improved pitch, power consumption and experimental results based on a test chip for electrical characterization.

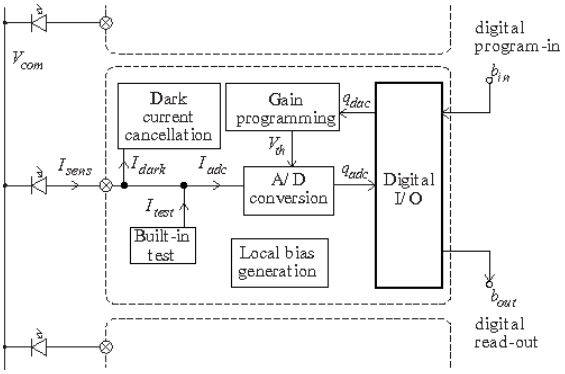

Figure 1. Functional description of the proposed architecture for the active pixel.

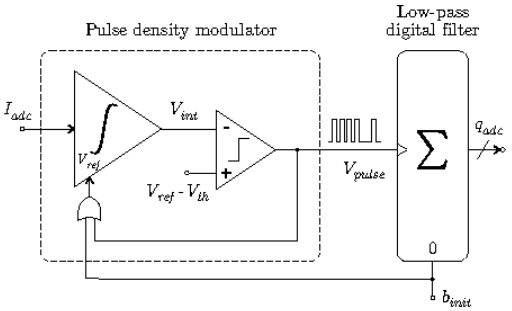

Figure 2. Scheme of a pulse density modulation (PDM) architecture.

2. Principles of operation

Figure 1 shows the functional description of the proposed DPS. V_{com} and I_{sens} are –respectively– the common voltage of the semiconductor X-Ray detector and the individual signal coming to a single pixel (a package of charge seen as a current). b_{in} and b_{out} are the digital input and output serial ports of the pixel.

The DPS has two main operation modes: signal acquisition and communication/ programming. In the first one, the pixel performs first a calibration of the dark current coming from the not yet irradiated detector (so that afterwards it can be cancelled) followed by the integration of the charge arriving during the acquisition time (T_{frame}), when it is possible to add a desired test pattern to the input. The total signal is digitally quantified by the charge-integrating A/D converter and stored in a digital register. In the second mode, the digitally stored data (q_{adc}) is serially read-out through b_{out}. At the same time, a new set of programming data (q_{dac}) is fed into the register in order to control the gain of each pixel (via V_{th}) individually, so any present fixed pattern noise of the detector can be compensated.

Besides, all the required analog references and biasing levels are generated locally within each pixel. Thus, the crosstalk among different pixels coupling through these analog signals is essentially eliminated.

2.1 Lossless integrating A/D conversion

Concerning A/D converter (ADC) architectures, we have selected a predictive one. Thanks to the internal feedback of these ADCs, the performance of their analog parts can be strongly relaxed, so area and power savings may be obtained, which are our main concern.

The preferred architecture is shown in figure 2, comprising a pulse density modulation (PDM) followed by a digital low-pass filter (implemented by a simple digital counter), which can be seen as an equivalent to an asynchronous continuous-time first-order single-bit sigma-delta converter. The incoming signal I_{adc} is integrated into V_{int} and then quantified at 1 bit by the comparator according with a given threshold and reference voltages (V_{th} and V_{ref}). The resulting asynchronous pulses (V_{pulse}) are fed back to perform the integrator's reset, acting as the D/A converter of a sigma-delta loop.

At the end of the acquisition time (T_{frame}), the counter's digital output is $q_{adc} = \lfloor n_{adc} \rfloor$ with $n_{adc} = \frac{T_{fram}}{T_{pdm}}$, where $\lfloor x \rfloor$ stands for the floor integer approximation of x and T_{pdm} is the obtained PDM average period. As the integrator is built around an integrating capacitor C_{int}, ideally we found that, being I_{adc} the average input signal,

$$n_{adc\text{-}ideal} = \frac{T_{frame}}{C_{int} V_{th}} I_{adc} \tag{1}$$

Thus, the desired linear conversion is accomplished. However, in a real situation, the finite power available gives V_{pulse} a width instead of being a delta-shaped pulse. Therefore, there exists a certain non-zero time (T_{res}) throughout the integrator is reset, which causes a certain reduction of the PDM frequency according to:

$$n_{adc\text{-}real} = \frac{n_{adc\text{-}ideal}}{1 + \frac{T_{res}}{T_{frame}} n_{adc\text{-}ideal}} \tag{2}$$

These cases can be compared at figure 3, where a DC I_{adc} is used for illustrative purposes. A non-null T_{res} means that the ADC's actual transfer curve exhibits a strong compression, especially obvious at full scale of I_{adc} where T_{res} is not negligible compared to T_{frame} and where the maximum error will appear. It can be demonstrated that to ensure a peak deviation below half a significant bit, T_{res} should be that $T_{res} < \frac{T_{fram}}{2^{2N+1}}$ for $2^N >> 1$. This translates in an unaffordable waste of power in the PDM blocks and statistical noise well below the full scale limit due to the pulsed nature of the current coming from the X-ray detector. In order to overcome these problems a specific PDM solution was proposed [12], as can be seen at figure 4. The design proposal does not use a hard short circuit but a novel switched-capacitor technique to reset C_{int}. In this case, the principle of operation is as follows: during frame initialization (b_{init} high), the analog integrator is "hard" reset, while $C_{reset/CDS}$ remains connected to V_{int}. Once in acquisition mode (b_{init} low), the sensor quasi-static current I_{adc} is integrated in C_{int} while $C_{reset/CDS}$ is now tracking the offset, the low frequency noise and the output signal itself of the first stage. Finally, when the fixed threshold voltage is reached, the comparator generates a spike (V_{pulse} high), which is sent again to the digital counter/low-pass filter of figure 2 and it also causes $C_{reset/CDS}$ to be connected to the input of the analog integrator.

As a result, the charge stored in C_{int} is compensated by that on the matched $C_{reset/CDS}$ and the reset is so performed. However -and unlike the results for a classical implementation of figure 3(b)-, this novel strategy does not block the integration of I_{adc} in C_{int} during the reset time and the integrator is operating in continuous-time during the whole full frame. Hence, integration of both the charges coming from I_{adc} and from $C_{reset/CDS}$ are linearly combined in C_{int}

during the reset phase. This fact can be easily seen in figure 3(c), where V_{int} does not return to the reference level V_{ref} after each reset. In consequence, the spike frequency is no longer dependent on the reset time and matches the ideal target of figure 3(a). In fact, just a minimum reset time is required to ensure complete charge redistribution between $C_{reset/CDS}$ and C_{int}, but its particular value is not relevant. Since $C_{reset/CDS}$ is continuously sampling the offset and the low frequency noise of the analog integrator, it innately implements the CDS function.

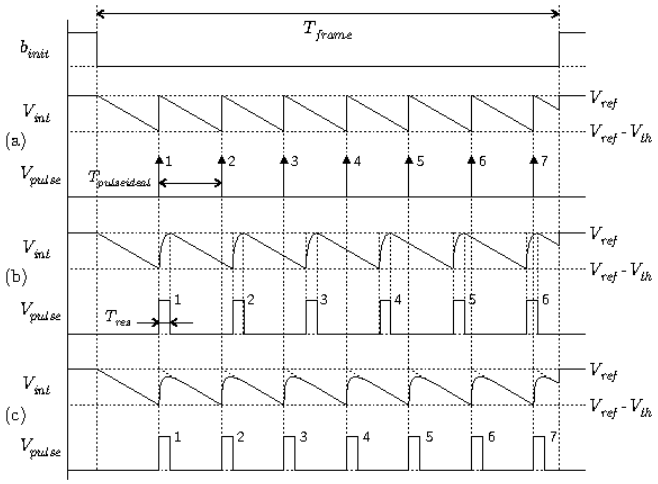

Figure 3. Operation for the ideal (a), classical (b) and proposed (c) PDM architectures.

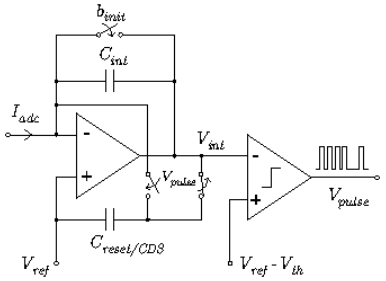

Figure 4. Proposal topology for the PDM stage at figure 2.

The above reasoning still holds if a pulsed I_{adc} is used instead of a DC current, as will be shown later.

In practice, technology mismatching between C_{int} and $C_{reset/CDS}$ causes an equivalent small offset in the threshold voltage, but this is negligible compared to the absolute process deviations of C_{int}. Furthermore, it can be fully compensated by the DPS gain programming capabilities explained in Section 2.3.

This operation resembles a modification of that of the charge-balancing integrator [13].

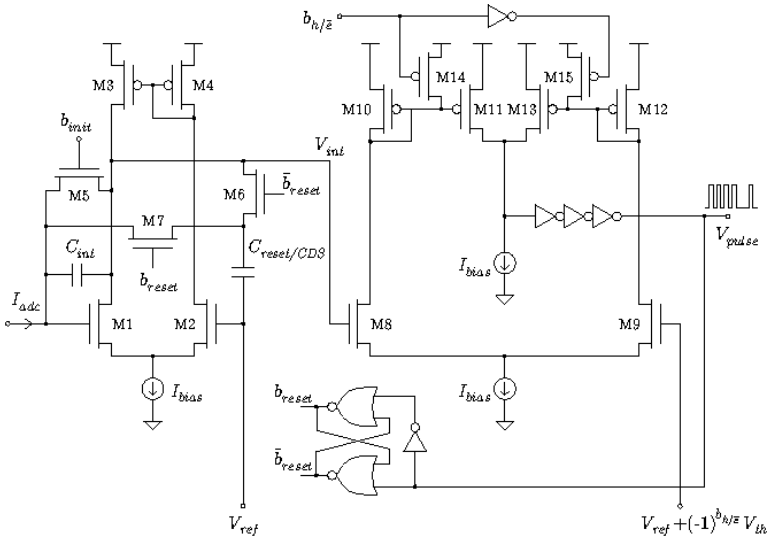

Figure 5. Proposal of a CMOS implementation of the PDM scheme at figure 4.

Based on the lossless PDM topology explained above, the compact CMOS circuit of figure 5 is proposed as an implementation. The pulse modulator is mainly composed of a compact capacitive transimpedance amplifier (CTIA) M1-M4 and C_{int}, the new reset scheme (M5-M7 and $C_{reset/CDS}$), a comparator (M8-M15) and a latch for generating the non-overlapping reset signals of the CTIA (b_{reset} and $\overline{b}_{reset}$). Long channel lengths and very low current biasing levels are chosen for the main amplifier devices of the CTIA in order to optimize gain and power consumption. As the detector material and biasing can be changed, it is convenient that the DPS may deal with positive (if collecting holes) or negative (if electrons) I_{adc} values. This is accomplished by selecting an external and global digital signal ($b_{h/e}$). This programmability is implemented by the two switches M14-M15, which changes the sign of the comparison appropriately. Obviously, the comparison level $V_{ref}+(-1)^{b_{h/e}}V_{th}$ must be programmed accordingly, as explained in Section 2.3.

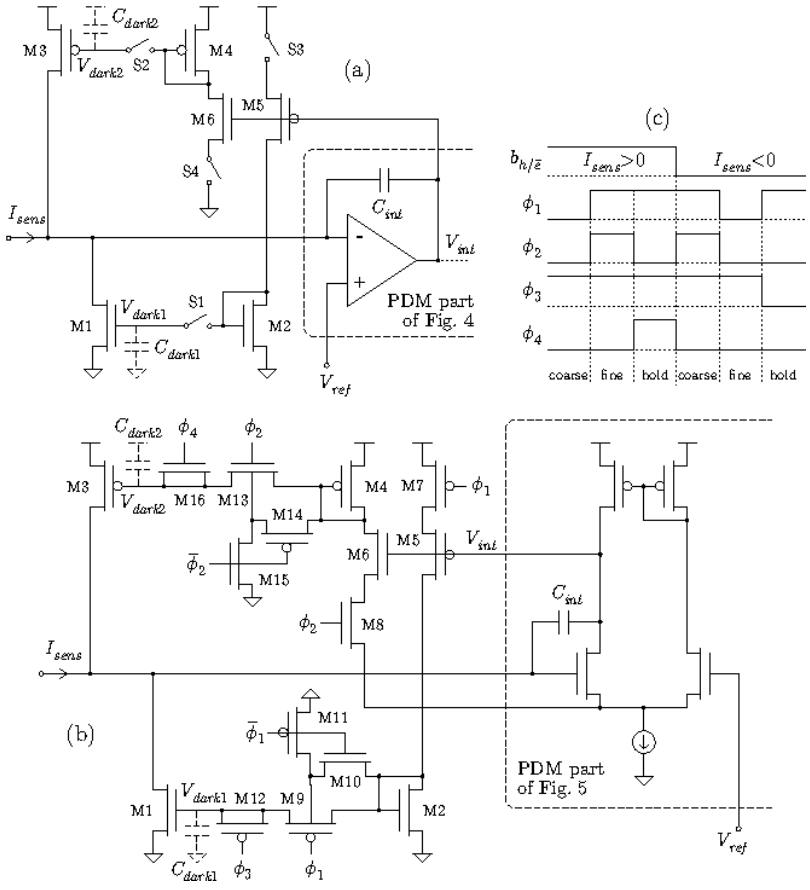

Figure 6. A scheme of the proposed automatic dark current cancellation circuit (a) is shown, along its CMOS implementation (b) and its control signals' operation (c).

2.2 Dark current cancellation

As previously discussed, just before an acquisition window is open, a calibration of the dark current of the detector (I_{dark}) is performed by the cancellation circuit shown in figure 6. As it can

be inferred from it, the dual dynamic current mirrors M1-M2 (NMOS) and M3-M4 (PMOS) can compensate -following the selection of switches S1 to S4- for positive and negative I_{dark} values respectively. The dark current value is stored by the translated equivalent voltage $V_{dark1,2}$ at the gates of M1 and M3, using the CTIA of the A/D converter through M5 and M6. Reusing the amplifier, we get a more reduced and power efficient DPS, besides compensating for the input offset voltage during the A/D conversion.

There two main concerns regarding this implementation, pertaining mainly to switches S1 and S2. First, the degradation of the cancellation of the dark current due to the drift in the analog memories $V_{dark1,2}$ for long acquisition times (e.g. 1 second) as a result of the leaking through them. And, second, the cancellation error due mainly to charge injection of these switches. To deal with these problems, we proposed the solution shown in figure 6(b).

The first problem is addressed by using the composite switching networks M9-M12 and M13-M16 instead of regular switches. In this way, we obtain dynamic biasing of the bulk of the main switching transistor, so achieving a low leakage current while in the off state and a fast settling time while conducting.

The second issue is dealt with by performing a two step calibration procedure. Its principle of operation can be easily explained following the chronogram of figure 6(c). In the case of holes collection ($b_{h/e}$ high), M1 performs first the coarse estimation of I_{dark}, but the dummy transistor M12 -devoted to cancel charge injection error of M9-, is not activated when holding. In fact, the positive error in M1 current due to the charge injection from M9 is then calibrated in the fine phase by its dual M3. Finally, and unlike for the coarse period, the dummy M16 is activated when holding. For electrons collection ($b_{h/e}$ low), the procedure is completely equivalent but interchanging the coarse and fine roles between M1 and M3, and the corresponding switches. As a result, even if the final charge cancellation is not perfect, the absolute residual is not directly depending on the value of I_{dark}, but on a fraction of the coarse charge injection offset, which is significantly smaller.

2.3 Pixel's gain programmability

As mentioned in the Introduction, each DPS has inherently a programming mechanism, shown in figure 7, to compensate for pixel gain FPN. Basically, it comprises a switched-capacitor D/A converter attached to the amplifier in order to set the threshold voltage V_{th}. This is equivalent to select different gain values. At the same time as q_{adc} is read-out through the b_{out} output of figure 1, the individual threshold code q_{dac} is serially entered through b_{in} using the same daisy chain pixel connectivity. The charge redistribution between C_{samp} and C_{mem} controlled by the chronogram in figure 7, the threshold voltage is generated according to $V_{prog} = V_{DD} \sum_{i=0}^{B-1} q_{dac}(i) 2^{-B+i}$ for $C_{samp} = C_{mem}$ where B and V_{DD} are the number of programming bits and the supply voltage, respectively. V_{prog} is then transferred to C_{int} from C_{mem} using the same CTIA of figure 4 and figure 6 obtaining the final threshold voltage

$$V_{th} = \frac{C_{mem}}{C_{int}} V_{DD} \sum_{i=0}^{B-1} q_{dac}(i) 2^{-B+i} \qquad (5)$$

which is stored in the MOS capacitor as the absolute voltage level according to the charge selected by the $b_{h/e}$ bit $V_{ref} + (-1)^{b_{h/e}} V_{th}$.

The re-use of the CTIA allows a fast driving of the large MOS capacitor and avoids charge redistribution errors to the passive DAC.

2.4 Built-in test

Obviously, a built-in test feature is mandatory in order to electrically test the pixel performance before and after the flip-chip process. A procedure to do this is to re-use C_{mem} in figure 7 as a charge pump test-capacitor during acquisition. In fact, most of the circuitry used is the same as in the previous section, as programming and injection of the test signal functions do not overlap in time. The injected charge at every test pulse is $Q_{test} = C_{int}(V_{test} - V_{reset})/C_{mem}$ if $C_{int} \equiv C_{mem}$.

2.5 Local bias generation

As mentioned in the Introduction, both current biasing I_{bias} and voltage reference V_{ref} are generated locally inside every DPS by the circuit shown in figure 8. It provides the proportional to absolute temperature (PTAT) voltage $V_{bias}=U_t \cdot \ln P$, where U_t is the thermal voltage and P the geometrical aspect ratio of transistors M1 (M3) to M2 (M4). I_{bias} is obtained afterwards from the non-linear load M8-M9. If they work at strong inversion saturation and conduction, respectively, the resulting current is proportional to the specific current I_S as $I_{bias} = \beta Q^2 U_t^2 / n$, where β and n are the current factor and subthreshold slope, respectively, while Q is a function of the geometrical factors M, N and P [14].

Driving I_{bias} into the active load M12 the reference voltage is thus obtained, $V_{ref} = n U_t \ln(QX/Y) + V_{TO}$. As V_{TO} is the MOSFET threshold voltage and displays a negative temperature coefficient, V_{ref} can be thermally compensated by a suitable scaling of the geometrical factors Q, X and Y.

3. CMOS integration

Following the architecture and circuits proposed above, we have implemented a 70μm-pitch DPS CMOS cell for its use as a detection pixel for sensing arrays. The main design parameters are summarized in table I and the resulting layout is shown in figure 9. The technology used is a 0.18 μm 1polySi 6-metal triple-well bulk standard CMOS.

A test chip has been integrated in order to verify experimentally the developed CMOS pixel (see figure 10). This test IC comprises four DPS replicas and additional circuitry (as current D/A converter, analog and digital buffers and so on) to perform several electrical analog characterization of the inner pixel performance (as all external signals are digital, apart from V_{test}).

The value of the integrating capacitor C_{int} (80fF) and the typical programmed threshold voltage from equation (5) have been chosen as to produce one event (reset) every 2 to 5 arriving photons of the energy of interest. Each event is then equivalent of a charge counting bin of around 75Ke$^-$, used as a typical value in our application. Obviously, this bin can be enlarged or reduced as needed by programming V_{TH} accordingly, so as to avoid overflow in the counter.

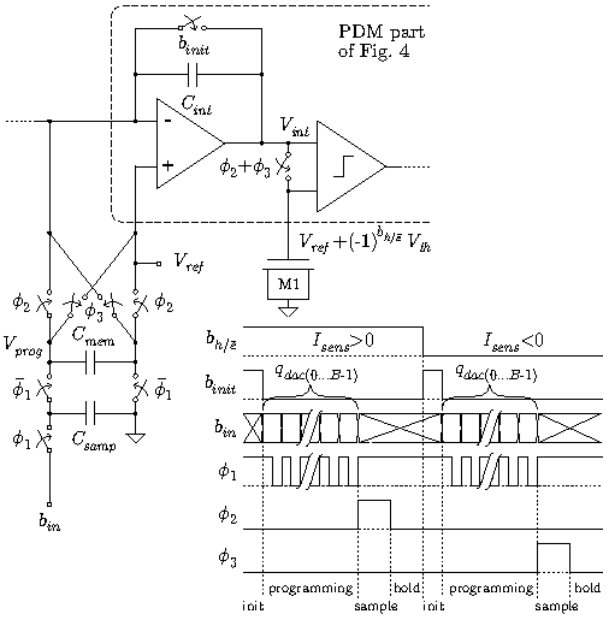

Figure 7. Individual in-pixel gain programmability scheme and operation for both polarities.

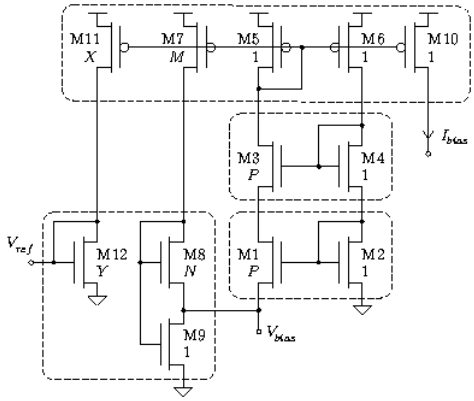

Figure 8. CMOS circuit for the in-pixel generation of bias.

Parameter	Value	Unit
I_{bias}	450	nA
V_{DD}	1.8	V
V_{ref}	760	mV
C_{int}	85	fF
$C_{reset/CDS}$	85	fF
C_{mem}	85	fF
C_{samp}	85	fF
V_{th}	40-400	mV
N	10	bit

Table I. Main design parameters

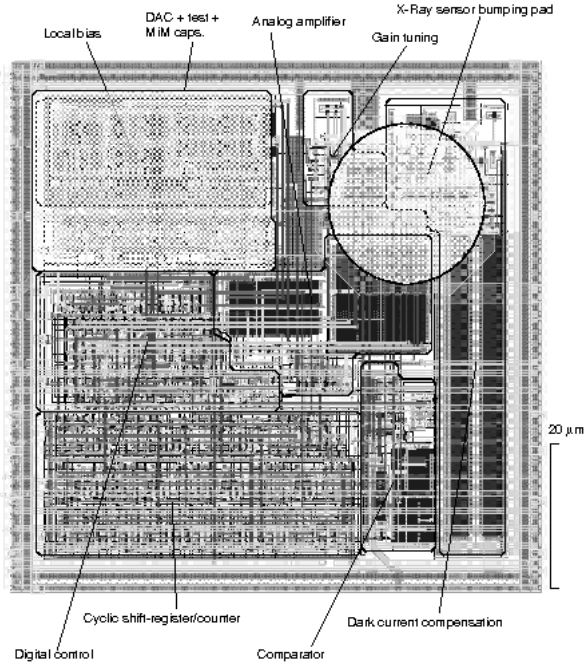

Figure 9. Layout of the DPS CMOS cell, showing the main functional blocks

4. Experimental results

So far, we have performed extensive electrical characterization to the test IC of figure 10. The results are shown in table II and figures 11 to 15.

Parameter	Value	Unit
Supply voltage, V_{DD}	1.8	V
Dark cur. cancel. range	<15	nA
Conversion gain	1/250 to 1/25	LSB/ke$^-$
Equivalent Noise Charge	(1.5 to 18)	ke$^-_{rms}$
Integ./acq. time	1 to 1000	ms
Output dynamic range	10+1	bit
Max. freq. of events	500	kHz
Inter-pixel crosstalk	<0.5	LSB
I/O speed	>50	Mbps
Static power consump.	8	μW
Bias mismatching	<10	%
Pixel size	70 x 70	μm^2

Table II. Experimental (simulated) results for the presented DPS circuit.

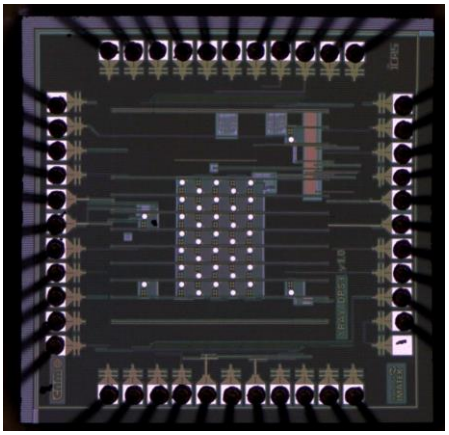

Figure 10. A microscope photography of the presented DPS test chip.

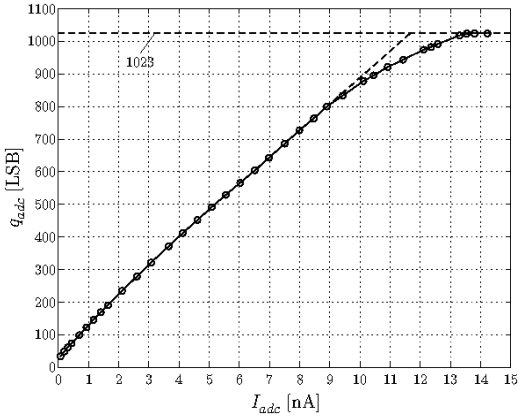

Figure 11. Experimental transfer curve for V_{th}=314mV and 1.88ms acquisition time.

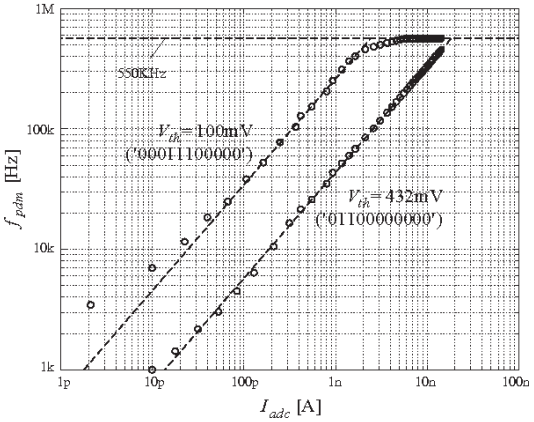

Figure 12. Experimental ADC transfer curve for two gain (V_{th}) settings (q_{dac} shown, too).

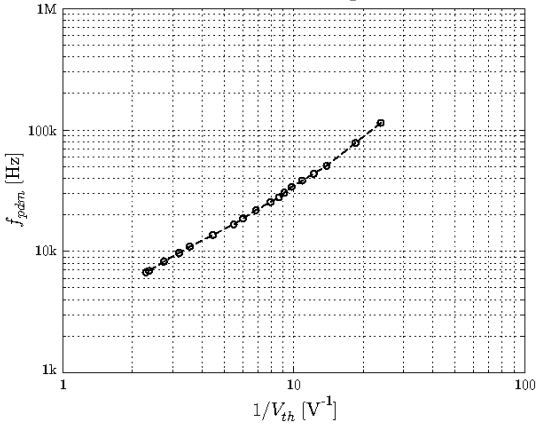

Figure 13. Experimental in-pixel gain programming range (DC input I_{sens}=300pA).

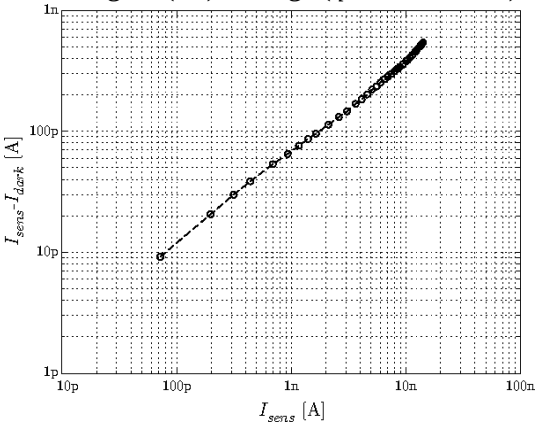

Figure 14. Experimental in-pixel dark current cancellation error (I_{sens} as dark current only).

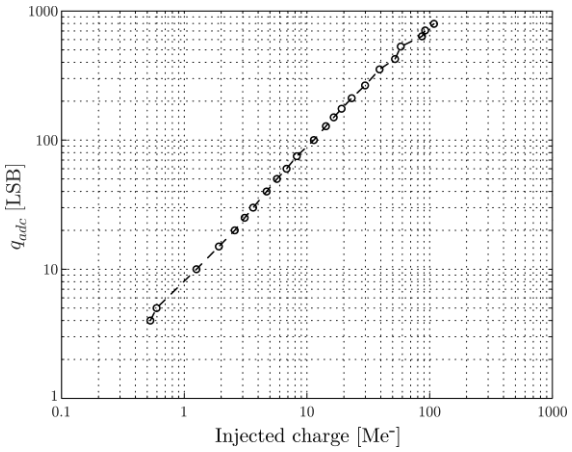

Figure 15. Experimental event-to-injected charge curve using the built-in charge injection circuitry mimicking incoming absorbed photons (period 7 μs).

5. Conclusions

The new low-power compact CMOS active pixel presented in this work fulfills the objective performances given in the introduction. The 70 μm pitch, 8 μW DPS cell has been integrated and carefully tested returning very good results on terms of linearity, noise, crosstalk immunity and speed, so being suitable for its use in X-ray imagers for digital mammography. Future work will bring results based on a working pixel matrix bump-bonded to an actual radiation detector.

Acknowledgments

This work has been partially funded by the Spanish Ministry of Science and Innovation (research project TSI-020302-2009-82.).

References

[1] *Screening for Breast Cancer: U.S. Preventive Services Task Force Recommendation Statement*, Annals of Internal Medicine, vol. 151, no. 10, pp. 716–726, Nov 2009.

[2] P.C. Gøtzsche, M. Nielsen, *Screening for breast cancer with mammography (review)*, Cochrane Database of Systematic Reviews 2009, Issue 4. Art. No.: CD001877.

[3] E. D. Pisano et al., *Diagnostic Performance of Digital versus Film Mammography for Breast-Cancer Screening*, The New England Jour. of Medicine, vol. 353, no. 17, pp. 1773–1783, Oct 2005.

[4] K. Iniewski, *Medical imaging: Principles, detectors and electronics*, John Wiley & Sons, Inc, 2009.

[5] S. Kasap and J. Rowlands, *Direct-conversion panel X-ray image sensors for digital radiography*, Proceedings of the IEEE, vol. 90, pp. 591-604, April 2002.

[6] R. Ballabriga et al., *Medipix3: A 64-k Pixel Detector Readout Chip Working in Single Photon Counting Mode with Improved Spectrometric Performance*, Nuclear Instrum. and Meth. in Physics Research Section A, vol. In Press, Corrected Proof, 2010.

[7] M. Locker et al., *Single photon counting X-ray imaging with Si and CdTe single chip pixel detectors and multichip pixel modules*, IEEE Trans. on Nuclear Science, vol. 51, pp. 1717-1723, Aug. 2004.

[8] B. Schmitt et al., *Development of single photon counting detectors at the Swiss Light Source*, Nucl. Instr. Meth. A, vol. 518, pp. 436-439, Feb. 2004.

[9] S. Basolo et al., *XPAD: pixel detector for material sciences*, IEEE Transactions on Nuclear Science, vol. 52, pp. 1994-1998, Oct. 2005.

[10] Edgar Kraft, *Counting and Integrating Microelectronics Development for Direct Conversion X-ray Imaging*, PhD Thesis Fakultät at the Rheinischen Friedrich-Wilhelms-Universität, Bonn, 2007.

[11] A. Mozzanica et al., *A single photon resolution integrating chip for microestrip detectors*, Nuclear Intruments and Methods in Physics Reaerch A, 2010.

[12] R. Figueras et al., *A 0.18μm CMOS Low-Power Charge-Integration DPS for XRay Imaging*, in Proceedings of the Biomedical Circuits and Systems Conference. IEEE, Nov 2009, pp. 209 –212.

[13] B. Gottschalk, *Charge-balancing current integrator with large dynamic range*, Nucl.Instr. And Meth., A 207, pp. 417-421, 1983.

[14] F. Serra-Graells and J. L. Huertas, *Sub-1V CMOS Proportional-to-Absolute-Temperature References*, IEEE Journal of Solid State Circuits, vol. 38, no. 1, pp. 84–88, Jan 2003.