Experimental Characterization of a 10μW 55μm-pitch FPN-Compensated CMOS Digital Pixel Sensor for X-Ray Imagers

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Abstract

This paper presents experimental results obtained from both electrical and radiation tests of a new room-temperature digital pixel sensor (DPS) circuit specifically optimized for digital direct X-ray imaging. The 10μW 55μm-pitch CMOS active pixel circuit under test includes self-bias capability, built-in test, selectable e^-/h^+ collection, 10-bit charge-integration A/D conversion, individual gain tuning for fixed pattern noise (FPN) cancellation, and digital-only I/O interface, which make it suitable for 2D modular chip assemblies in large and seamless sensing areas. Experimental results for this DPS architecture in 0.18μm 1P6M CMOS technology are reported, returning good performance in terms of linearity, $2ke^-_{rms}$ of ENC, inter-pixel crosstalk below 0.5LSB, 50Mbps of I/O speed, and good radiation response for its use in digital X-ray imaging.

Keywords: CMOS, low-power, digital pixel sensor (DPS), FPN, imaging, X-ray.

1. Introduction

X-ray imaging is a key technology in many application fields such as medicine, industry, security, chemistry and high-energy physics. Hybrid digital direct detectors are the state-of-the-art technology for X-ray imaging (1; 2). These systems are composed of a direct X-ray detector bump-bonded

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to a readout integrated circuit (ROIC). Direct detectors convert X-ray photons to electronic charge, which is sent to the bonded circuitry for further signal processing. The main advantages of hybrid systems over more traditional technologies such as charge-coupled devices (CCD) or flat panel detectors (FPD) are: 100% fill factors, improved detection efficiency and spatial resolution, and the possibility of combining independent technologies for the detector and its readout circuit. The latter allows the use of the same readout chip for a wide range of detector materials to meet the requirements of several applications. Fig. 1 illustrates a direct detector pixel hybridized with its complementary metal-oxide-semiconductor (CMOS) readout circuitry using bump-bonding and flip-chip techniques. In this figure, I_{sens} and V_{com} stand for the detector readout current and high-voltage biasing, respectively.

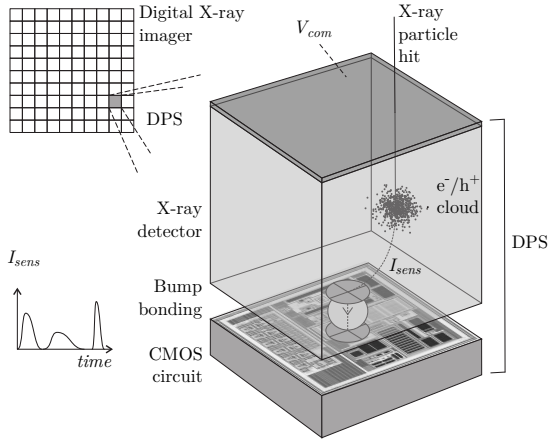

Figure 1: General parts of a hybrid digital pixel sensor for direct X-ray imaging with a representation of a generic X-ray particle hit. Not at scale.

Regarding the readout circuitry, the reading method can be classified into two widely studied categories: charge-integration (3; 4; 5; 6), and photon-counting (7; 8; 9; 10). Most charge-integration approaches present limited functionality, either requiring external analog references or lacking test capability or in-pixel A/D conversion. Active pixel circuits combining these two readout methods have also been studied (11). Charge-integration signal processing accumulates all the charge generated by X-ray particles and the noise. On the other hand, photon-counting pixels compare the charge generated by a single X-ray photon with a given energy threshold to determine if this photon contributes to the output image or it is discarded.

Thus, each counted photon contributes with the same weight, and the lowest measurable signal is a single X-ray photon. Since the energy threshold is set above circuit noise, background is eliminated and large acquisition times are allowed. Furthermore, using multiple threshold levels, at the expense of a more complex circuitry, or sweeping this threshold in consecutive acquisitions, information of incoming X-ray photons spectrum can be obtained. However, photon counting pixel detectors with small pitch have also some drawbacks due to a process known as charge-sharing, which degrades detector performance (12; 13). The charge-sharing effect occurs when the charge cloud generated by the X-ray photon in Fig. 1 expands and some fraction is captured by neighboring readout pixels. As a consequence, the charge captured may not exceed the threshold in any of the involved pixels, causing the loss of this photon count. The opposite effect, when the threshold is exceeded in more than one pixel, results in multiple events. Moreover, photon counting pixels can suffer also from pile-up issues at high X-ray photon fluxes, when photons arrive closer than the temporal resolution of the readout circuitry and they can not be resolved as a single particle (14).

Concerning ROIC complexity, it can range from simple charge-integrating pixels with analog output to commonly more complex photon-counting circuits with in-pixel digital counters.

Hybrid digital direct detectors in general present another drawback for certain applications since large and seamless sensing areas can only be obtained at high costs due to restrictions in technology yield (15).

To avoid information losses due to charge-sharing and pile-up effects in photon-counting, the authors previously designed a room-temperature CMOS readout pixel circuit based on charge-integration readout. The main features of this novel fully functional pixel design are: lossless charge integration readout, individual gain programming for fixed pattern noise (FPN) compensation and system flexibility, local bias generation and digital-only communications for reduced crosstalk, built-in test capabilities to lower screening costs, biphasic current sensing capability for flexibility, compact design for high spatial resolution and low-power operation to avoid detector heating. Three generations of this design have been fabricated with 100μm, 70μm and 55μm-pitch (16; 17; 18).

This paper presents the results of a deep characterization, at electrical and radiation levels, of the advanced 55μm-pitch digital pixel sensor (DPS). Section 2 reviews a summary of the DPS architecture for completeness, while Section 3 presents the integration of the DPS together with the description

of the test setups. Finally, Sections 4 and 5 report the results obtained from electrical and radiation tests.

2. X-Ray Digital Pixel Architecture

This section reviews the architecture of the proposed DPS, described in detail in (16; 17; 18). Fig. 2(a) shows the functional model of the pixel ROIC. As illustrated, the X-ray imager is built by arranging the DPS cells in daisy chains at column or row levels with b_{in} and b_{out} for the digital serial input and output connections between chained pixels, while V_{com} stands for the common polarization voltage of the X-ray direct sensor.

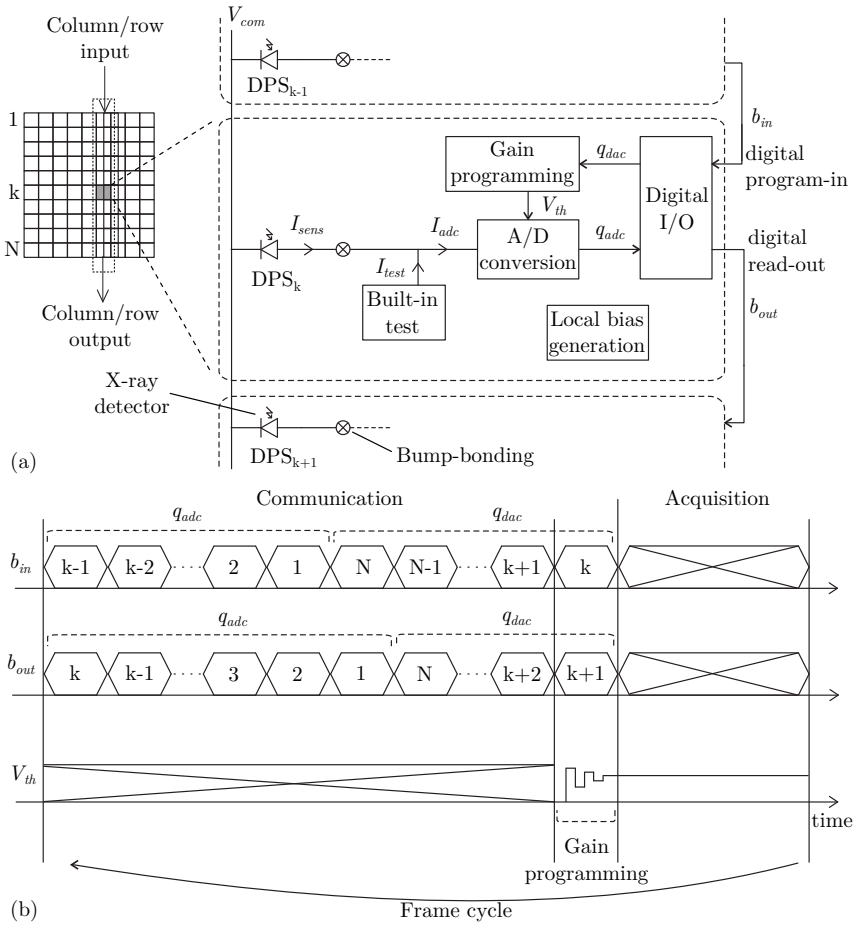

Figure 2: Architecture (a) and operation (b) of the proposed DPS for digital X-ray imaging.

The operation of the DPS is explained in Fig. 2(b), where communication and acquisition modes can be distinguished. During acquisition, input signal I_{adc} is digitally quantified by the in-pixel charge-integration analog-to-digital converter (ADC). In addition, self-test can be performed during acquisition by injecting controlled charge packets through I_{test}. The acquired digital word q_{adc} is finally readout serially through b_{out} during communications phase while, at the same time and without any extra speed cost, the individual gain V_{th} of the pixel ADC is programmed-in to all the daisy chained pixels using b_{in} to compensate for any FPN during the following frame.

2.1. Lossless A/D Conversion

In order to reduce the equivalent noise bandwidth and crosstalk, the A/D conversion is implemented at pixel level. The novel scheme of Fig. 3, based on a pulse density modulator (PDM) and implemented by a C_{int}-based capacitive transimpedance amplifier (CTIA) stage, satisfies the requirements for a compact and low-power pixel while presenting a lossless charge integration operation and implementing the correlated doubled sampling (CDS).

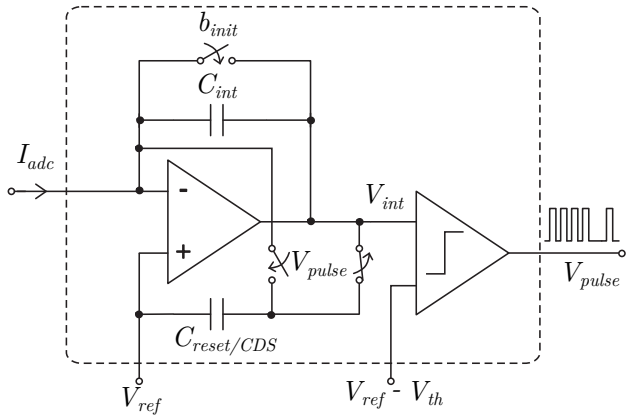

Figure 3: Proposed novel scheme for the PDM of the in-pixel predictive ADC ($I_{adc} > 0$ case).

During acquisition (b_{init} low), the proposed ADC integrates the input signal I_{adc} in C_{int} while $C_{reset/CDS}$ tracks the offset, the low frequency noise and the output signal itself of the first stage. When the fixed threshold $V_{ref} - V_{th}$ is reached, the comparator generates a spike (V_{pulse} high), connecting $C_{reset/CDS}$ to the input of the analog integrator (not shown in Fig. 3).

Thus, the charge stored in C_{int} is compensated by $C_{reset/CDS}$ and the reset is accomplished.

The main difference in comparison with classical reset schemes for charge-integration (19) is that in the proposed PDM, integration of I_{adc} in C_{int} during reset time (T_{res}) is not blocked, allowing the extension of the pixel dynamic range to high photon fluxes. The resulting waveforms are illustrated in Fig. 4 showing the matching of the proposed scheme operation with ideal behavior that the classical scheme can not achieve. Hence, the pulse frequency at the output of the proposed PDM can therefore be written as:

$$f_{pulse} = \frac{I_{adc}}{C_{int} V_{th}} \tag{1}$$

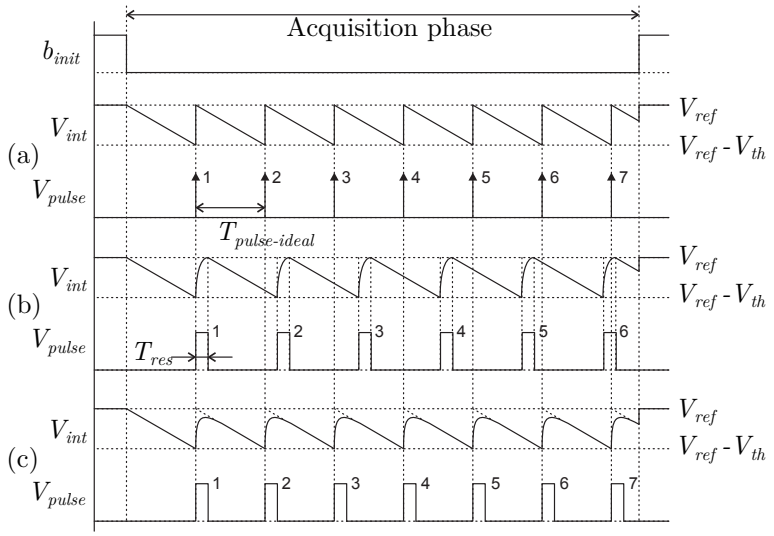

Figure 4: Qualitative waveforms of the operation of ideal (a), classical (b) and proposed (c) PDM ($I_{adc} > 0$ case). Not in scale.

2.2. Gain Programmability and Built-in Test

According to Eq. (1), the gain of the pixel ADC can be tuned by changing the threshold voltage (V_{th}) of its PDM stage. For this purpose, the switched-capacitor digital-to-analog-converter (DAC) of Fig. 5 is introduced inside each DPS cell. Despite increasing circuit complexity, this DAC brings flexibility to the system, and it allows the independent programming of each

pixel gain in order to compensate for any FPN due to pixel mismatching at both detector and circuit levels.

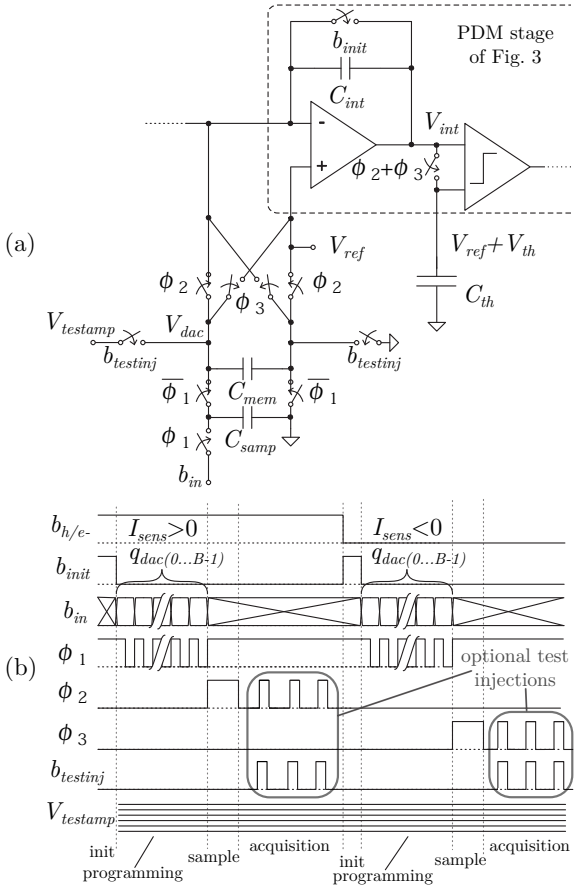

Figure 5: Simplified scheme (a) and operation (b) for in-pixel gain programming and built-in test.

During communications phase, the individual digital word q_{dac} is entered in each DPS through b_{in} using the daisy-chained connections between pixels. Following the chronogram of Fig. 5, the desired threshold voltage is sequentially generated in V_{dac} using the code q_{dac} to control the charge redistribution between C_{samp} and C_{mem}. Finally, the same CTIA of the PDM stage of Fig. 3 is used to transfer the charge stored in C_{mem} to C_{int}, with the polarity defined by b_{h/e^-} (ϕ_2 or ϕ_3) to deal with positive (holes) or negative (electrons) charge integration. The reuse of the CTIA block means important silicon area and power consumption savings per DPS, but even more important, the

low output impedance of this block allows the resulting V_{int} to be copied into C_{th} for further storage during acquisition. Assuming $C_{samp} \equiv C_{mem} \equiv C_{int}$ the expression of the programmed gain value can be found to be:

$$V_{th} = (-1)^{b_{h/e^-}} V_{DD} \sum_{i=0}^{B-1} \frac{q_{dac}(i)}{2^{B-i}} \tag{2}$$

where B stands for the length of the programming word q_{dac}, and V_{DD} for the supply voltage.

The same circuitry is reused for the DPS built-in test mechanism, since both functions are not overlapped in time. The aim of this block is to generate the I_{test} pulses of Fig. 2 during acquisition phase in order to emulate external signals without requiring any X-ray source or even before hybridization. Thus, defective ROIC chips can be screened before the expensive hybridization step. The principle of operation is similar to that used for gain programming: during acquisition, C_{mem} is biased to the common test amplitude $V_{testamp}$; when a test stimulus is requested ($b_{testinj}$ high), the charge stored in C_{mem} is injected directly to the ADC input according to the polarity again specified by b_{h/e^-} flag to test the biphasic current sensing capability of the proposed pixel. The resulting change on the integrated signal due to I_{test} is:

$$\Delta V_{int} = (-1)^{b_{h/e^-}} \frac{C_{mem}}{C_{int}} V_{testamp} \tag{3}$$

Typically $C_{mem} \equiv C_{int}$, so $|\Delta V_{int}| \equiv V_{testamp}$. The separate control of amplitude and timing signals of the test pattern is of special interest to simplify external components and reduce noise in test mode. In fact, $V_{testamp}$ is the only external analog signal of the DPS which can inject noise , but it has no contribution during regular acquisition ($b_{testinj}$ low). Even in test mode, the external control of a constant DC voltage reference is simpler than distributing dynamic analog signals inside the pixel array.

2.3. Local Bias Generation

As already illustrated in Fig. 2(a), the connectivity between pixels is limited to digital signal only in order to reduce crosstalk between pixels and relax layout requirements. For this purpose, a local analog generator is incorporated inside each DPS. Basically, this block is in charge of generating both current biasing sources I_{bias} and voltage reference V_{ref} required by all

CMOS circuits presented in previous sections. The main advantages of including a local generator in each pixel are: low crosstalk thanks to the lack of common analog signals between active pixels, and low interconnectivity to relax technology requirements. In (18) and (20) a detailed description of this circuit block is published. As an additional advantage, the locally generated V_{ref} is thermally compensated, that is, temperature independent.

3. CMOS Integration

Based on the circuits proposed in previous sections, a 55μm-pitch DPS cell is developed in UMC 0.18μm 1P6M triple-well bulk CMOS technology, following the layout of Fig. 6, which is an improved version of the pixel presented in (18). As it can be seen, half of the pixel area is occupied by digital blocks (ADC counters and control logic), while analog circuitry is placed beneath the bumping pad and the metal-in-metal (MIM) capacitors for compacting silicon area. The same 11-bit reconfigurable digital I/O block is used for both acquisition and communication phases. For the former, it is configured as a 10-bit ripple counter with overflow flag, while for the latter it operates as a shift register for the serial read-out and program-in of signal ans gain data respectively.

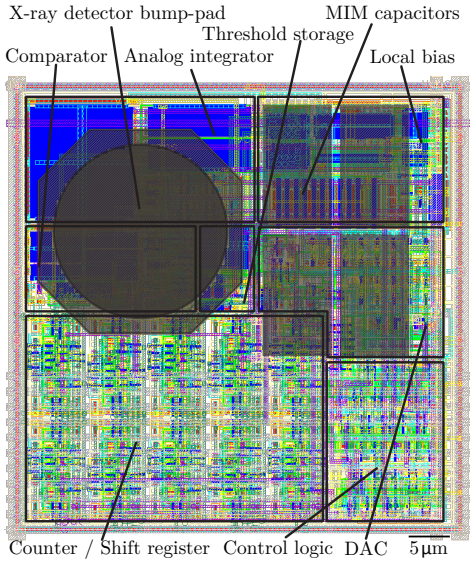

Figure 6: Layout of the proposed DPS CMOS cell and main blocks.

Test chips have been designed and integrated containing DPS cells of Fig. 6, as shown in Fig. 7. The integrated circuit of Fig. 7(a), includes individual DPS experiments for in lab electrical characterization (without detector hybridization) of the internal blocks of Fig. 2, together with a tiny array of DPS cells to study inter-pixel crosstalk. Some signals such as V_{int}, V_{ref}, V_{pulse} or V_{th} of Fig. 3 are made externally accessible on those standalone pixels. Fig. 7(b) shows an integrated small array of 20×24 pixels, covering an area of 1.10×1.32 mm^2, for its hybridization with direct X-ray detectors and its test under X-ray radiation. This pixels array can be also used to study the effect of CMOS design for manufacturing (DFM) metal filling on the final image. In this sense, four different metal dummy patterns can be easily identified for each quadrant of the array.

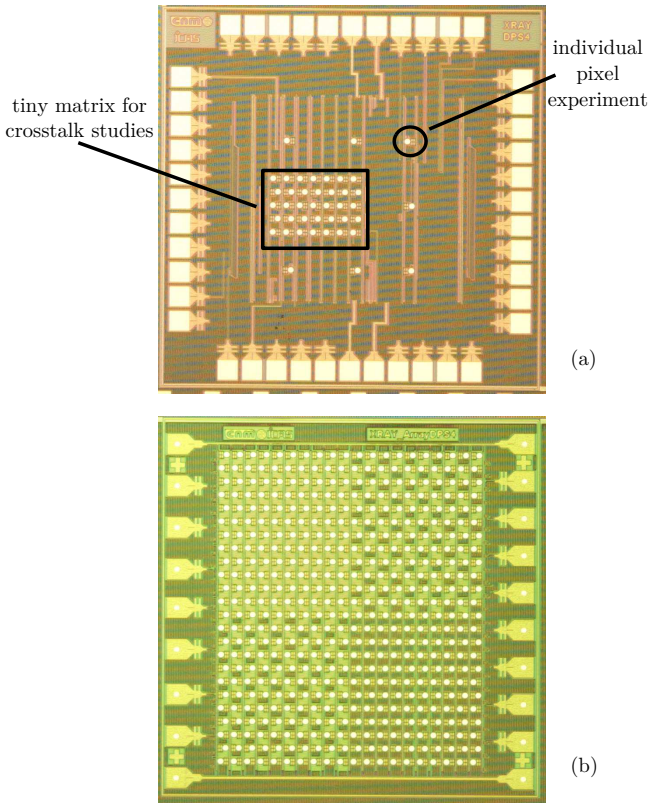

Figure 7: Microscope photography of the test chips for electrical characterization (a) and for hybridization with direct X-ray detectors and tests under radiation (b). Chip sizes are 1.5mm×1.5mm.

The corresponding array of 55μm-pitch Silicon direct X-ray detector has been integrated through a customization of the low-cost 2.5μm 1P1M CMOS technology from IMB-CNM(CSIC) based on detector designs used in (21). As shown in Fig. 8, the back side of the detector array includes the pixelated p-n junctions and the ROIC fan-in, together with the bumps grown at Fraunhofer IZM. Three sides of the array include the wire-bonding pads for the connectivity to external circuitry. The detector front side, not shown in Fig. 8, is fully metalized to apply the high-voltage bias, chosen for hole collection in this case.

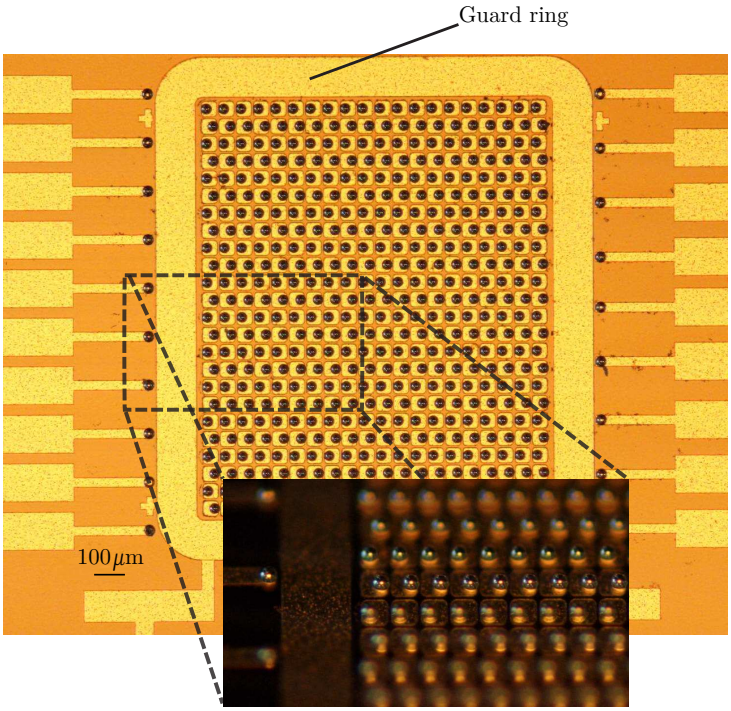

Figure 8: Microscope photography of the 300μm-thick Si direct X-ray detector back side with bumps.

Finally, the test imager of Fig. 9 is obtained after performing the flip-chip hybridization of the ROIC array of Fig. 7(b) with the X-ray detector of Fig. 8 and wire-bonding packaging at IMB-CNM(CSIC) facilities. As illustrated in the figure cross-section, the hybrid device is attached to a windowed printed circuit board (PCB) substrate for further connectivity to the field programmable gate array (FPGA) based lab setup.

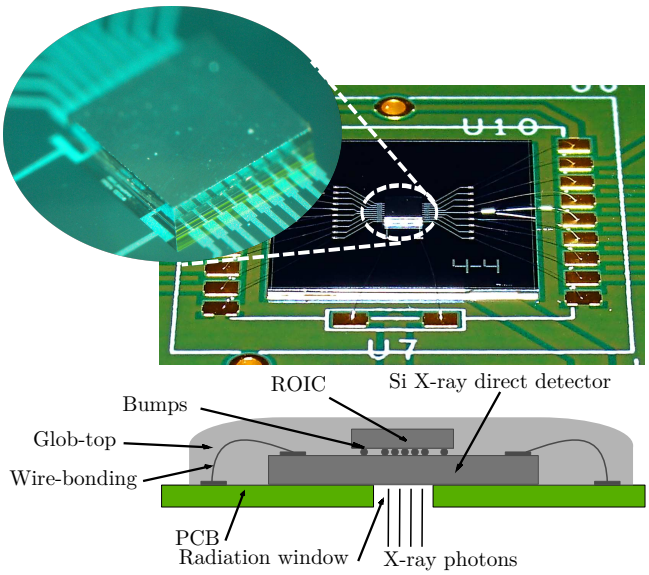

Figure 9: Photograph after flip-chip (a) and cross-section scheme of the terminated hybrid imager (b).

4. Electrical Tests

Standalone DPS cells of the test chip of Fig. 7(a) are used for individual pixel block verification by performing electrical measurements at room-temperature as in (18). The obtained results are summarized in Table 1. Taking advantage of the extra circuitry added to the test vehicle chip, the expected behavior of the meaningful signal waveforms can be verified. The low measured power consumption helps obtaining a good performance of the system at room-temperature since it does not cause relevant heating of the X-ray detector, which would degrade its behavior especially regarding the dark current. The robustness of the proposed design and layout implementation is verified from the low mismatching of both V_{ref} and I_{bias} obtained from measurements on all fabricated samples. Besides, the analog input circuit is not saturated for input DC currents up to 10nA or higher, depending on the programmed conversion gain.

The conversion gain can be digitally programmed using all 11-bits of the digital I/O interface. In this sense, the weight of a single count, also known as least significant bit (LSB) can be programmed from 25ke$^-$ to 250ke$^-$. Since the most significant bit (MSB) of the 11-bit counter is reserved as an overflow flag, the digital output dynamic range is given by the remaining 10-bits of

the ripple-counter, leading to a full scale charge up to 250Me$^-$. On the other hand, the ENC is calculated using:

$$ENC = \frac{1}{q} C_{int} \sqrt{\int_{1/T_{acq}}^{\infty} V^2_{n\_CTIA-out} df} \tag{4}$$

which is under 2ke$^-_{rms}$ for a practical lower integration limit ($T_{acq} \leq 1$s). That is a reasonable value for a charge-integration system, which uses higher integrating capacitors when compared to their photon-counting counterparts. Furthermore, since it is much lower than the minimum LSB, it is not the limiting factor to the output dynamic range.

Table 1: DPS experimental electrical performance.

Parameter	Value	Units
Supply voltage	1.8	V
Reference voltage (V_{ref})	830	mV
Biasing current (I_{bias})	620	nA
Bias mismatching ($\pm\sigma$)	< 10	%
Conversion gain	1/250 to 1/25	LSB/ke$^-$
Input full scale	> 10	nA
Reset pulse width (T_{res})	0.5	μs
Max. PDM frequency	900	kHz
Equivalent noise charge	< 2	ke$^-_{rms}$
Threshold programming word	11	bit
Integration time	1 to 1000	ms
Output dynamic range	10	bit
Inter-pixel crosstalk	< 0.5	LSB
Max. program-in/read-out speed	> 50	Mbps
Static power consumption	10	μW
Integrating capacitor	100	fF
Pixel pitch	55	μm

The tiny pixel matrix of Fig. 7(a) is used to study the inter-pixel crosstalk, since single pixels can be stimulated at full-scale input signal while their neighboring pixels receive no input signal. Thanks to the local generation of the references and the digital-only communications between pixels, no crosstalk effects have been observed even working at low threshold levels, which leads to an improvement of the final image sharpness and contrast.

As pointed in Section 2.1, the novel lossless charge integration circuit proposed in Fig. 3 does not block the integration of the input signal during the reset time. This aspect improves the linearity at high radiation fluxes as demonstrated in Fig. 10, where the PDM output pulses frequency presents a notorious linear response following the behavior of Eq. (1) even for frequency values close to $1/T_{res}$, which reduces the brightness distortion from the imaging point of view. The high linearity observed through all the input signal range combined with practical integration times reported in Table 1, make the proposed DPS suitable for a wide range of applications, from synchrotron applications, using high photon fluxes, to medical imaging requiring lower fluxes.

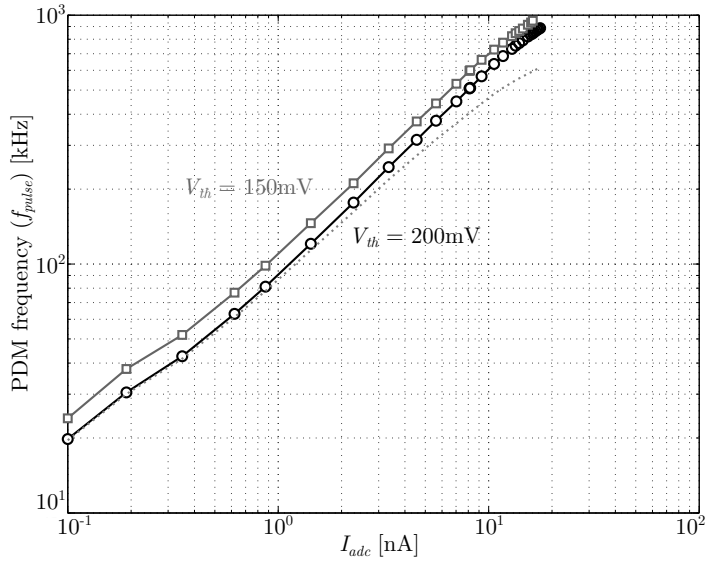

Figure 10: Experimental PDM transfer function of the in-pixel ADC for two different gain programming levels. Dashed line represents the transfer function using classic charge integration for $T_{res} = 0.5\mu$s. Non-linearities are reduced from 5% of classic schemes to around 1%. Results obtained using DC current as input to standalone pixels of Fig. 7(a).

Concerning the compensation of FPN through the tunable gain of the ADC, V_{th} in Eq. (1), Fig. 11 demonstrates the proper behavior described in Section 2.2. Since programmability range extends over more than one decade, this feature is useful not only for practical FPN compensation but also brings flexibility to the system, allowing image preprocessing and adjustment of imager sensitivity to each particular X-ray application and detector type.

Since CdTe detectors absorb more high energy X-ray photons when compared to Si detectors, the latter then may require higher pixel sensitivity.

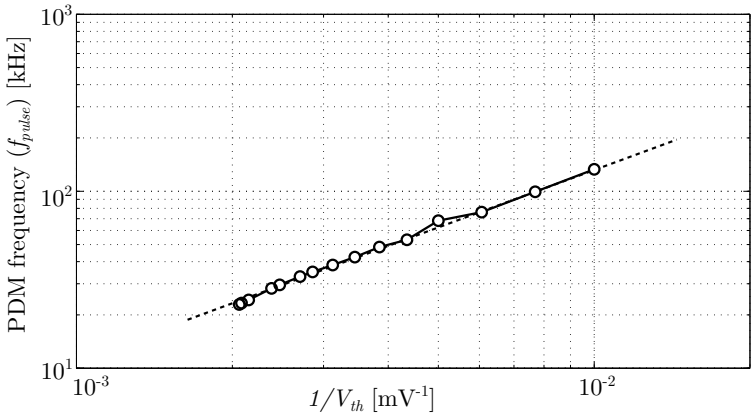

Figure 11: Experimental in-pixel ADC gain programming range for a constant input of $I_{adc} = 600$pA. Full range non-linearity is under 0.22%.

5. Radiation Test Results

All reported results in this section have been obtained using the test setup presented in Fig. 9. The direct X-ray detector is biased at $V_{com} = 80$V under uncooled operation, to ensure detector is fully depleted. Radiation is produced in an X-ray tube with Tungsten anode and adjustable applied voltage and current intensity. The latter is directly related with the number of emitted photons, while the applied voltage is associated with photon energy.

Flat radiated captures confirm that the guard ring is mandatory. When disabled, the outer pixels of the array collect a large amount of charge from the array surrounding area. High repeatability is observed for read-out values when comparing a large number of measurements, obtaining deviations of about 0.5%, basically due to variations in dark current between acquisition runs.

Fig. 12 presents the average digital output code of all pixels of the array for flat radiation images applying different X-ray tube voltage levels (V_{tube}). The expected exponential behavior of Lambert-Beer law at the detector is obtained. Regarding the photon flux, Fig. 13 reports the digital output lectures for flat images captured under different X-ray tube intensities (I_{tube}), obtaining the expected linear behavior. The linear response with respect

to the number of photons is further verified by changing the acquisition time for a given X-ray intensity as in Fig. 14. These results also proof that the proposed DPS is useful in a wide range of applications, since the good performance is maintained through wide ranges of acquisition times, photon energies and radiation intensities.

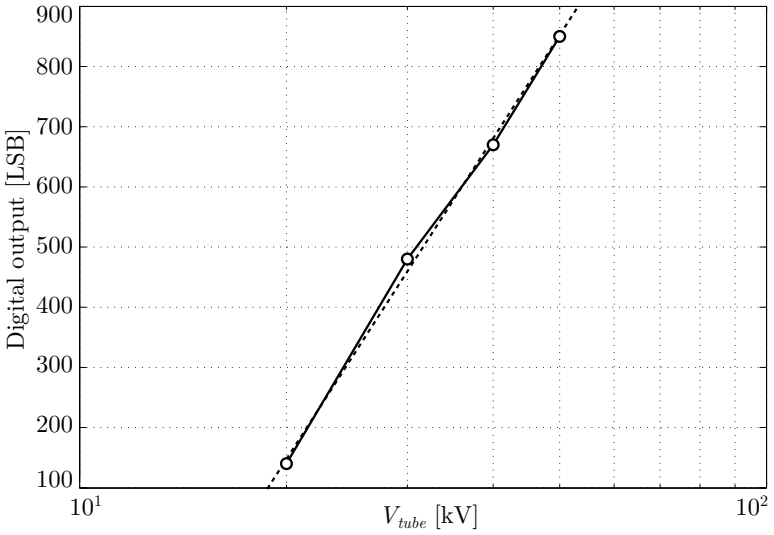

Figure 12: Experimental pixel digital output as a function of the X-ray tube high voltage bias for T_{acq}=1000ms, q_{dac}=2047LSB and I_{tube} = 1000mA. Logarithmic deviation is under 0.2%.

Threshold voltage programmability of the PDM stage is shown in Fig. 15, illustrating the average digital output of flat irradiated captures under same conditions, but modifying only the programming digital word q_{dac}. As proved with the experiment of Fig. 11, the programmability range is adequate both for practical FPN compensation and for adapting the system to the requirements of a wide range of applications. FPN compensation feature can be verified in Fig. 16, where the distribution of digital outputs for all pixels under flat radiation acquisition before and after equalization are shown. This in-situ equalization results are obtained after adapting each individual pixel threshold over few iterations. As the number of iterations grows, more uniform digital outputs are obtained. The presented example corresponds to a case with only 10 iterations to adjust the individual pixel gains. Even though the low number of iterations, a significant reduction of the deviation in the measured digital output is achieved.

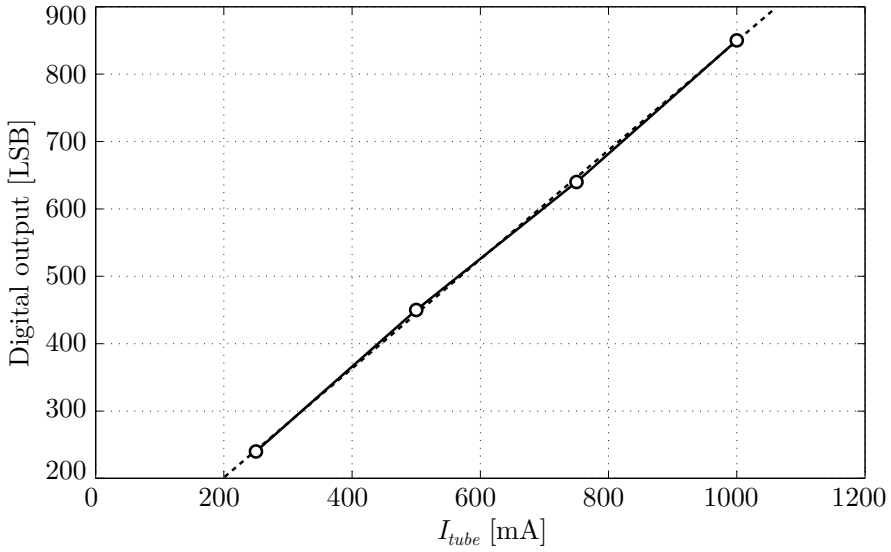

Figure 13: Experimental pixel digital output versus X-ray tube intensity for T_{acq}=1000ms, q_{dac}=2047LSB, and V_{tube} = 50kV. Measured non-linearity is under 0.04%.

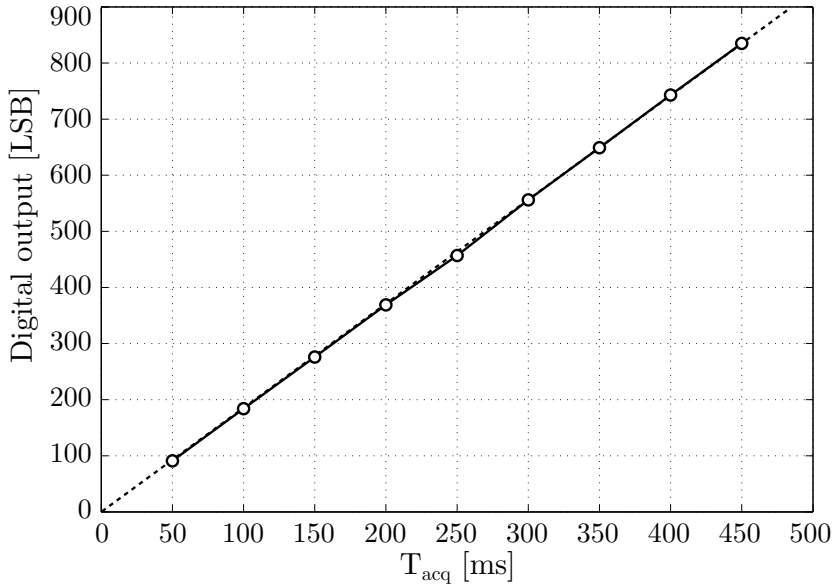

Figure 14: Experimental digital output as a function of acquisition time for q_{dac}=500LSB, V_{tube}=50kV and I_{tube}=1000mA. Measured non-linearity is under 0.001%.

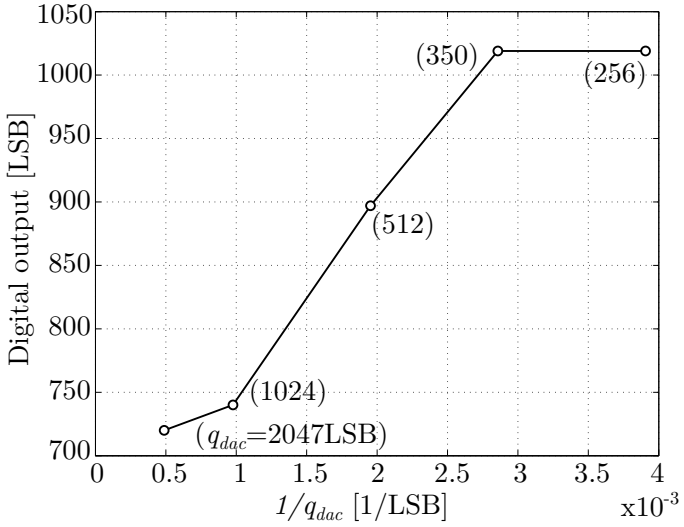

Figure 15: Experimental digital output versus threshold programming for T_{acq}=400ms, V_{tube}=50kV and I_{tube}=1000mA.

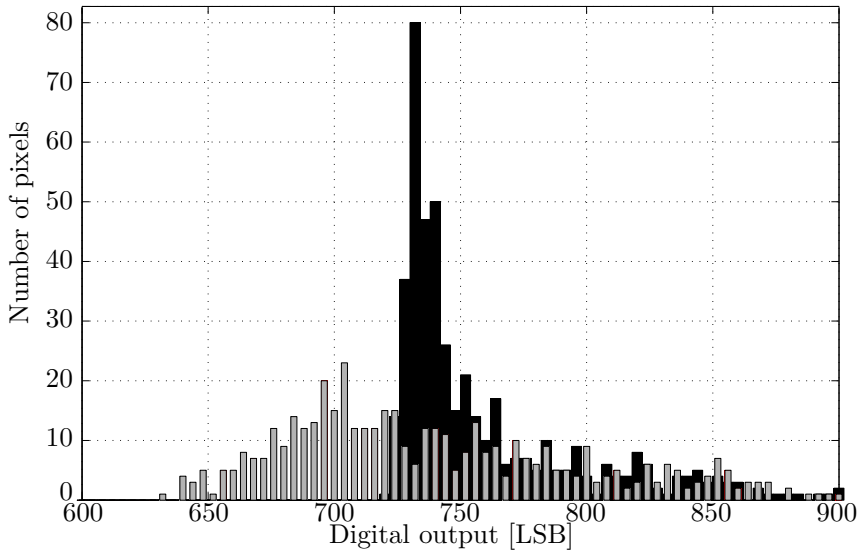

Figure 16: Experimental distribution of all pixel readout digital outputs of the 20 × 24 array of Fig. 7(b) under flat radiation before (gray, and narrower for easy visualization) and after (black) in-pixel threshold equalization. Initial q_{dac} = 1000dec code is adapted for equalization in the course of 10 iterated captures. In this case: T_{acq}=1000ms, V_{tube}=50kV and I_{tube}=1000mA.

The modulation transfer function (MTF) describes the spatial frequency response of an imaging system. In other words, it quantifies how contrast is transmitted. In practice, it can be measured by imaging a precision edge slightly tilted to the pixels column or row. Fig. 17 shows the MTF obtained with the proposed DPS compared to that obtained with the Timepix (22) chip used by the commercial product XRI-UNO (23) operating in counting mode and using the same slanted edge MTF extraction algorithm (24). This algorithm performs system MTF calculations up to twice the Nyquist frequency over slanted edge images. Due to the small size of the test array of this work, a single image has been replicated to obtain the minimum needed area for computation. As seen in Fig. 17, results from this work and Timepix pixels are comparable, since both pixels exhibit the same pitch (55μm) and MTF is extracted in both cases using the same algorithm on almost identical images.

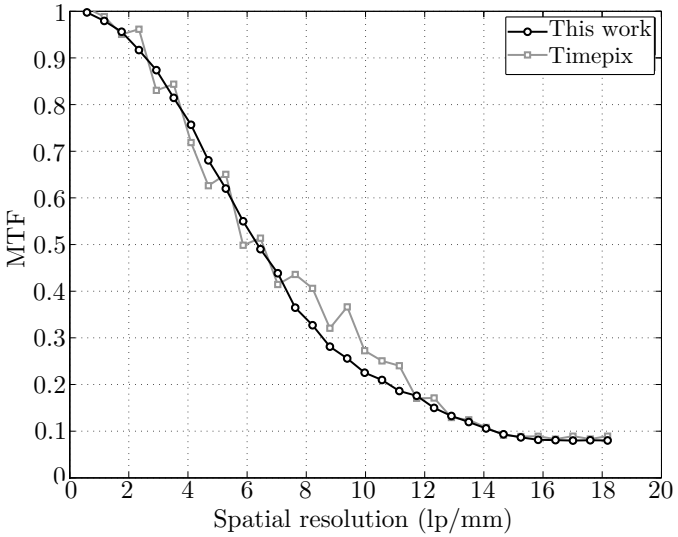

Figure 17: Experimental MTF of this work compared to Timepix (22) extracted from slanted edge images for T_{acq}=1000ms, V_{tube}=50kV and I_{tube}=1000mA.

Regarding the response to attenuated radiation, several materials and thickness have been used to mitigate the incoming X-ray flux in Fig. 18. Again, the exponential behavior of the Lambert-Beer law referred to the detector X-ray absorption can be observed, meaning that the ROIC pixels do not degrade image contrast.

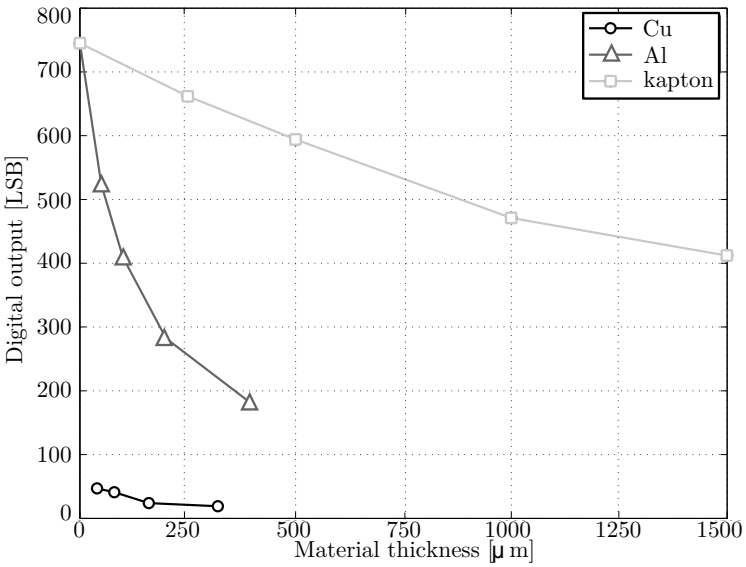

Figure 18: Experimental pixel digital output obtained attenuating radiation with different materials and thickness for T_{acq}=400ms, q_{dac}=1024dec, V_{tube}=50kV and I_{tube}=1000mA.

As a qualitative example, Fig. 19 shows a composition of few single shots to obtain a larger image (about 7.040mm length) of an encapsulated chip, where the pads inside the packaging and even the internal wire-bonds (typ. 25μm in diameter) are visible. Some single small equalized images are supplied in the same figure. Since the detector area is small (1.10×1.32 mm^2), the images are magnified for visual accommodation. As appreciated in the provided images, one pixel presents a defective behavior probably due to a bad bump bonding connection, since it does not block the daisy chain communications. However, it does not affect the neighboring pixels thanks to the low crosstalk architecture of the imager.

Finally, the test setup of Fig. 9 has also been mounted in a synchrotron facility (25) for a limited time. Taking advantage of the microfocus capabilities of this facility, a 15μm×15μm monochromatic beam of 10keV X-ray photons is pointed to the pixel array. Fig. 20 shows a section of the captured images, at room temperature and without any calibration, for four positions of the X-ray beam in the array. For these experiments, the initial beam intensity was attenuated using 0.35mm thickness of Aluminum. As appreciated in the figure, no crosstalk is observed. Moreover, these measurements confirm that the proposed DPS is suitable for high photon fluxes applications, since the

DPS response is not saturated despite synchrotron beam intensity is much higher (30 times approx.) than the X-ray tube used in previous experiments.

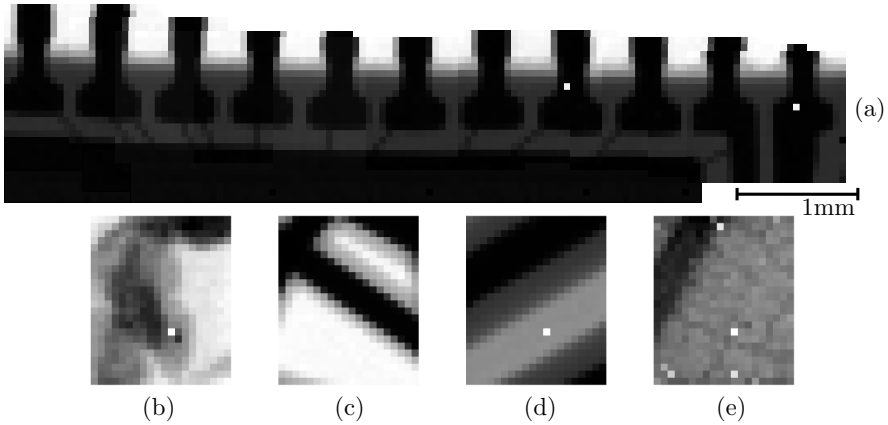

Figure 19: Composition of few single equalized shots to obtain a larger area image of an encapsulated chip (a), and small single images of part of an ant (b), metal wires covered with plastic (c), small region of a flat cable (d) and a low contrast leaf (e) where the stem can be distinguished. For all cases, T_{acq}=400ms, V_{tube}=50kV and I_{tube}=1000mA.

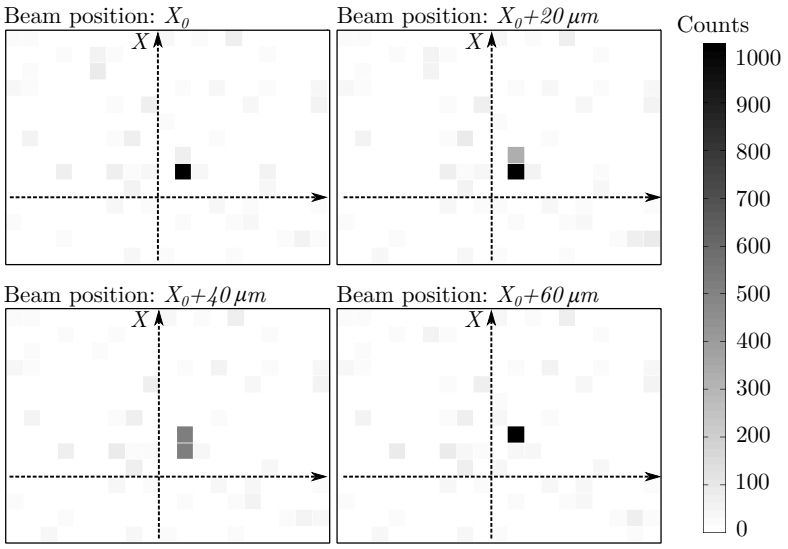

Figure 20: Images captured moving a 15μm×15μm focused X-ray beam through X axis direction in 20μm steps (smaller than the 55μm pixel pitch). For all cases, T_{acq}=17ms, q_{dac}=2047.

No radiation hardening has been observed neither during X-ray tube experiments nor during synchrotron measurements.

6. Conclusions

Experimental results of a new 55μm-pitch low-power and compact fully functional CMOS active pixel circuit are presented. First, the DPS design proposed by authors is reviewed, together with the description of the integrated test chips and setup. Then, analysis of both electrical and radiation tests are supplied.

Most of the charge-integrating X-ray DPS found in the literature present a lack of functionality while their photon-counting counterparts may suffer from information looses due to charge-sharing and pile-up effects. Therefore, a direct comparison of the proposed DPS with other works can not be made. However, it can be concluded that the proposed DPS shows state-of-the-art performance in terms of dynamic range, calibration, crosstalk, linearity and speed for its use in large-scale 2D-modular X-ray imagers.

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