Variable-Mirror Amplifier: A New Family of Process-Independent Class-AB Single-Stage OTAs for Low-Power SC Circuits

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***Abstract*—This paper presents a new family of Class-AB operational transconductance amplifier (OTA) circuits based on single-stage topologies with non-linear current amplifiers. The proposed variable-mirror amplifier (VMA) architecture is mainly characterized by generating all Class-AB current in the output transistors only, by exhibiting very low sensitivity to both technology and temperature deviations, and by avoiding the need for any internal frequency-compensation mechanism. Hence, this family of OTAs is well-suited for low-power switched-capacitor circuits and specifically optimized for switched-OpAmp fast on-off operation and multi-decade load-capacitance specifications. Analytical expressions valid in all regions of operation are presented to minimize VMA settling time in discrete-time circuits. Also, a complete OTA design example integrated in 0.18μm 1P6M MiM 1.8V CMOS technology is supplied with detailed simulation and experimental results. Compared to resistor-free state-of-art Class-AB OpAmp and OTA literature, the proposed architecture returns the highest measured figure-of-merit value.**

***Index Terms*—Analog, CMOS, operational amplifiers, OpAmp, OTA, Class-AB, low-power, switched-capacitor, slew-rate.**

I. Introduction

THE market demand of true ubiquitous and autonomous smart sensors is boosting the research of low-power switched-capacitor (SC) design techniques for their analog front-end circuits, like charge amplifiers, tunable filters and data converters. In this context, both operational voltage amplifiers (OpAmps) and operational transconductance amplifiers (OTAs) are clearly key contributors in terms of power consumption of the resulting SC circuit.

In general, low-power SC design techniques can be classified into two different strategies: low-voltage and low-current circuits. In the first approach, power savings are obtained by scaling down the nominal supply voltage of the overall circuit. The consequent reduction of available voltage room between power rails is then compensated by specific circuit techniques, which try to optimize internal signal headroom allocation against device non-linearities. Examples of low-voltage SC design strategies are: rail-to-rail operation [1], bulk-driven inputs [2], [3], internal supply multipliers to drive critical switches [4], [5], inverter-based amplifiers [6], [7], and switched-OpAmps (SOAs) for replacing critical switches [8]. In practice, low-voltage SC techniques usually can only achieve moderate power-saving ratios, in the order of a single octave, due to technology limitations (e.g. MOSFET threshold voltage) or even to the increase of current consumption caused by the extra biasing circuits. Hence, the above circuit techniques are usually reserved for specific constraints of supply-voltage downscaling (e.g. single-cell batteries).

When stronger power reduction is needed, low-current SC circuit techniques are mandatory. In this sense, the low-current OpAmp and OTA designs reported in literature exploit Class-AB operation by means of several circuit techniques. Telescopic pairs or flipped voltage followers [9]–[12] overcome the current limitation of classic differential pairs by changing tail current on demand at the cost of requiring more pair structures. Hybrid Class-A/AB operation [13] can be obtained by combining folded cascode circuits as the first stage and active current mirrors as the second one at the expense of increasing the number of current branches. Other solutions come from cascading inverters with self-biasing capabilities [6] to control its quiescent consumption, but with intrinsic limitations in terms of PSRR due to their pseudo-differential architectures. Adaptive biasing of classic fully differential topologies can be achieved in general by the use of dedicated slew-rate monitoring circuits [14], which dynamically control the bias current of the main amplifier, with the corresponding area and power overheads associated with these auxiliary blocks.

In the particular case of push-pull output stages, the introduction of RC bias tees [15] helps to set the quiescent bias point while maintaining its Class-AB capabilities, although some penalties may need to be paid in terms of area or noise to ensure that the low cut-off frequency does not affect the signal bandwidth. Dual input stages with dedicated CMFB [16] or floating voltage sources [17] are also employed to control the NMOS and PMOS biasing of these push-pull stages, not without the corresponding drawbacks in terms of power and area. Even the use of multiple-input floating-gate transistors have been proposed for this purpose [18].

Other interesting strategies to trigger Class-AB operation relay on negative resistance loads [19], typically implemented through cross-coupled transistor pairs. Special care must be paid then to tune the amount of partial positive feedback in order to avoid latching issues. Finally, there are some Class-AB techniques focused on introducing additional signal paths for a more effective reuse of current modulation, like in the case of recycling topologies [20], [21] and multi-paths with current starving [22], but also incrementing at the same time the number of internal current branches of the amplifier circuit.

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Unfortunately, some of the above circuit techniques rely on multi-stage architectures [6], [13]–[18], with the consequent extra power and area penalties imposed by their closed-loop frequency compensation. Regarding those strategies based on single-stage amplifiers [9]–[12], [19]–[22], they expend the effective Class-AB peak currents not only at output transistors but also at internal circuit branches due to intermediate current-mirroring stages, causing an important reduction of their dynamic-power efficiency. Furthermore, in most of the above low-current OpAmp and OTA design techniques, Class-AB performance tends to suffer from technology or temperature sensitivity.

This work introduces a new family of Class-AB OTA circuits called variable-mirror amplifiers (VMAs), which are based on single-stage topologies with non-linear current mirrors. The initial idea was first presented by these authors in [23], but this paper further improves the concept by adding: extension to weak inversion operation, a new auxiliary biasing circuit for a better control of peak currents, analytical expressions of the maximum slew rate, a complete set of parametrized curves to show the design flexibility of the VMA topology and a settling time analysis to optimize its power consumption when used in SC circuits. Thanks to the proposed VMA architecture, Class-AB dynamic peak currents are fully invested in the output transistors only. Apart from the inherent power savings, this single-stage design approach avoids the current and area overheads associated with frequency compensation mechanisms, while it features multi-decade load-capacitance capability and compatibility with SOA fast on-off operation in SC circuits. Last but not least, the proposed VMA family exhibits very low technology and temperature sensitivity, which is of special interest when targeting deep-submicron CMOS technologies, and its Class-AB principle can be extended to a wide range of device operating conditions.

The presented paper is organized as follows: Section II introduces the general architecture of the VMA and its principle of operation. Then, two process-independent CMOS circuit implementations are proposed in Section III for the Class-AB parts of the VMA. Section IV presents a settling-time analysis to help with the design optimization of this amplifier family. Based on the proposed circuits, a practical VMA design example is given in Section V, while its experimental results together with a comparative analysis with state-of-art Class-AB OpAmps and OTAs are reported in Section VI. Finally, conclusions are summarized in Section VII.

II. Variable-Mirror Amplifier Architecture

The main idea behind the proposed VMA topology is illustrated in Figure 1. In what follows, all MOSFET bulk terminals are connected to their respective supply rail. Starting with a classic fully-differential current-mirror OTA architecture, two complementary differential pairs are introduced here as input transconductors in order to split input signal into two paths for the separate Class-AB control of NMOS and PMOS output transistors. Please note dual input stages have no significant impact on the input swing when used in fully differential SC circuits since OTA input common-mode level

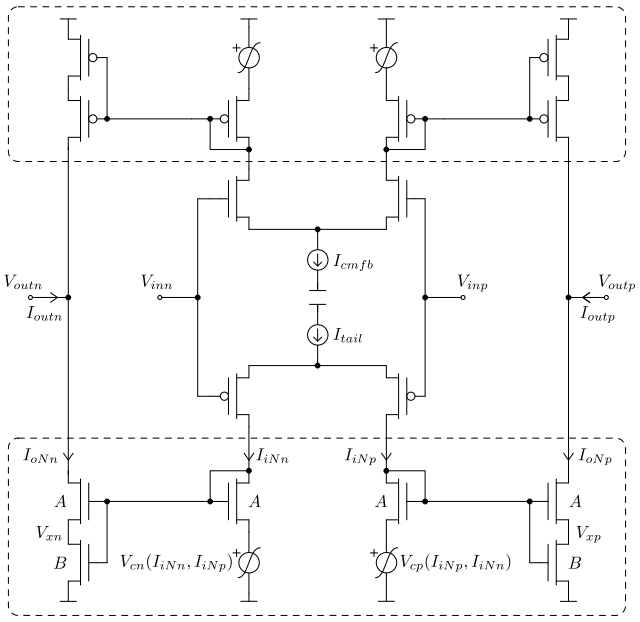

Figure 1. General architecture of the proposed VMA.

is already kept at a constant value (typ. half of the supply voltage) by the common-mode feedback (CMFB) control. The core of the novel OTA architecture are the dynamic current mirrors enclosed in the dashed boxes of the same figure. They can be understood as fully-differential voltage-controlled (V_{cp} and V_{cn} for the NMOS path) non-linear current amplifiers (I_{oNp}/I_{iNp} and I_{oNn}/I_{iNn} for the NMOS path), whose gain is dynamically and symmetrically changed by cross-coupled partial positive local feedback. Finally, the output CMFB control required for this fully differential OTA is introduced through the tail bias current of NMOS input transconductor (I_{cmfb}).

Two important advantages can be already noted in the VMA architecture of Figure 1. First, there is no need for Miller compensation capacitors as in the classic Class-A current-mirror OTA, thus silicon area and bandwidth performance are both improved at the same time as SOA speed capabilities. Second, only output transistors are actually draining Class-AB high-peak currents, since the rest of OTA devices are in fact operated in Class A, with the consequent benefits in terms of dynamic-to-static power consumption ratios. From the large-signal Class-AB viewpoint, the wanted functionality for the variable-gain current mirrors boxed in Figure 1 is (NMOS positive-path case):

$$\begin{cases} I_{outp} > 0 & V_{cp} > V_{xp} & I_{oNp} \gg I_{iNp} & \text{Class-AB} \\ I_{outp} \equiv 0 & V_{cp} \equiv V_{xp} & I_{oNp} \equiv I_{iNp} \equiv \frac{I_{tail}}{2} & \text{Bias point} \\ I_{outp} < 0 & V_{cp} < V_{xp} & I_{oNp} \ll I_{iNp} & \text{Class-AB} \end{cases} \quad (1)$$

In other words, the voltage-controlled gain must supply both the required current boosting or attenuation in Class-AB operation together with the control of the biasing point under no output driving requirements, as illustrated in Figure 2.

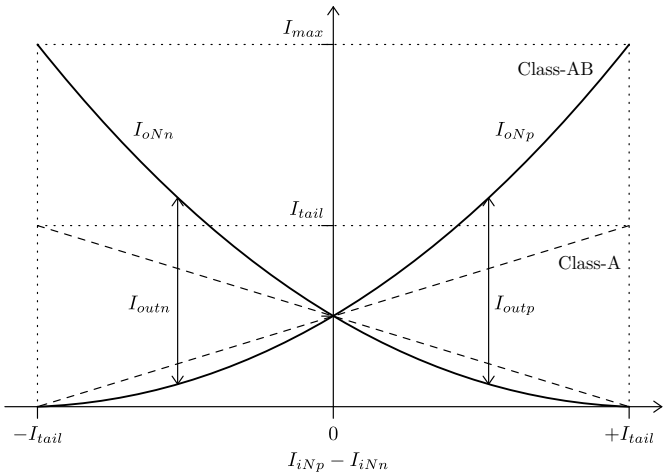

Figure 2. Qualitative large-signal Class-AB DC operation for the variable-mirror blocks boxed in Figure 1. Drawing not in scale.

Supposing saturation operation for the A-sized transistors of Figure 1 and linear mode for their B-sized counterparts, the EKV MOSFET model [24] returns the following non-linear current mirror transfer function (NMOS-path case):

$$I_{oNp,n} = \begin{cases} \dfrac{B}{A+B} e^{\frac{V_{cp,n}}{U_t}} I_{iNp,n} & \text{weak inv.} \\ \dfrac{B}{A+B}\left(\sqrt{A\dfrac{n\beta}{2}} V_{cp,n} + \sqrt{I_{iNp,n}}\right)^2 & \text{strong inv.} \end{cases} \tag{2}$$

where U_t, n and β stand for the thermal potential, sub-threshold slope and current factor, respectively. As expected, $V_{cp,n}$ can be effectively used to supply the requested large-signal Class-AB current amplification, and attenuation at some extent, as well as the setting of output bias points. In this sense, the circuit implementations presented in next section for the control of $V_{cp,n}$ can be classified as source-degeneration techniques [25], [26], but with the novelty of being dynamic and specifically designed to cancel the process and temperature dependencies still present in (2).

When Class-AB operation is not activated, the small-signal behavior at the symmetrical bias point of the architecture proposed in Figure 1 mimics those from the classic current-mirror OTAs. In particular, VMA input stage follows the same equivalent input noise and gain non-linearity design equations as the Class-A amplifier counterpart.

III. Process-Independent Class-AB Circuits

A. Type-I

The first Class-AB circuit proposal for the VMA architecture of Figure 1 is presented in Figure 3(a). As it can be seen, a B-sized cross-coupled matched pair is introduced here to supply the local positive feedback responsible for emphasizing the Class-AB behavior. However, in order to prevent from an excess of positive feedback gain which would otherwise latch the entire OTA circuit, an additional C-sized crossed transistor is also incorporated in Figure 3(a) providing some

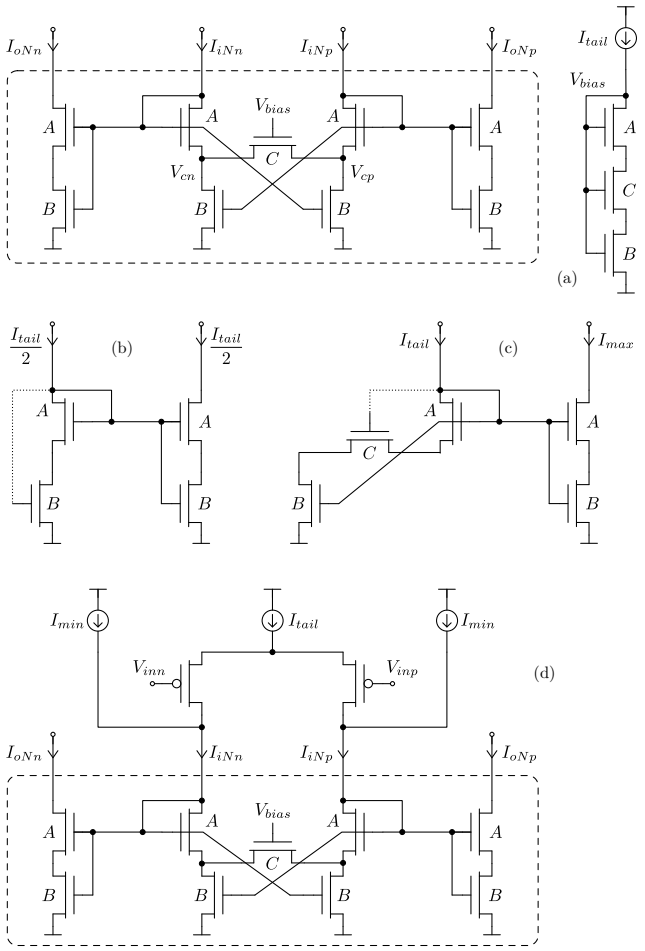

Figure 3. Type-I Class-AB current amplifier (a) proposed for the boxed sections of Figure 1 (NMOS path), equivalent right-half circuits for Class-A operating point $I_{iNp} \equiv I_{iNn} \equiv \frac{I_{tail}}{2}$ (b) and maximum Class-AB positive output $I_{iNp} \simeq I_{tail}$ $I_{iNn} \simeq 0$ (c), and Class-AB smoothing mechanism (d). Dotted lines indicate virtual short circuits.

amount of local negative feedback. In practice, the optimum balance between positive and negative feedback can be simply achieved by the design of the device matching ratios B and C. Finally, the required gate voltage of the C-sized transistor (V_{bias}) is directly obtained from the matched composite active load biased at I_{tail}.

Supposing weak-inversion operation for all devices, the EKV-based analysis of Figure 3(a) returns:

$$D \doteq \frac{AB}{A+B} \qquad E \doteq \frac{ABC}{A+B+C} \tag{3}$$

$$\begin{aligned} I_{iNp} &= \tfrac{B}{D} I_{oNn}\left(1 - \tfrac{D}{A}\tfrac{I_{iNp}}{I_{oNp}}\right) + \tfrac{CD}{AE} I_{tail}\left(\tfrac{I_{iNp}}{I_{oNp}} - \tfrac{I_{iNn}}{I_{oNn}}\right) \\ I_{iNn} &= \tfrac{B}{D} I_{oNp}\left(1 - \tfrac{D}{A}\tfrac{I_{iNn}}{I_{oNn}}\right) + \tfrac{CD}{AE} I_{tail}\left(\tfrac{I_{iNn}}{I_{oNn}} - \tfrac{I_{iNp}}{I_{oNp}}\right) \end{aligned} \tag{4}$$

while for strong-inversion operation, the following expressions can be found:

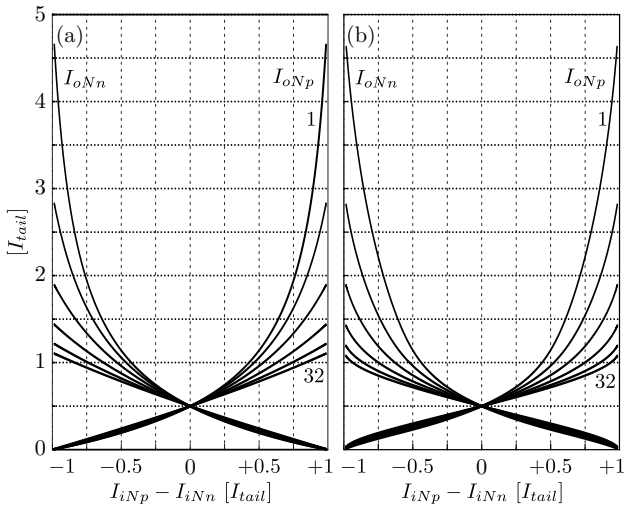

Figure 4. Simulated DC transfer functions for the type-I Class-AB current amplifier of Figure 3(a) under weak (a) and strong (b) inversion operation. Curves are parameterized for $C = \{1, 2, 4, 8, 16, 32\}$ and $A \equiv B = 8$ (i.e. $D = 4$).

$$
\begin{aligned}
I_{iNp} =& B\left(2\sqrt{\tfrac{I_{oNn}}{D}} - \sqrt{\tfrac{I_{oNp}}{D}} + \sqrt{\tfrac{I_{iNp}}{A}}\right)\left(\sqrt{\tfrac{I_{oNp}}{D}} - \sqrt{\tfrac{I_{iNp}}{A}}\right) \\
&+ C\left(2\sqrt{\tfrac{I_{tail}}{E}} - \sqrt{\tfrac{I_{oNp}}{D}} - \sqrt{\tfrac{I_{oNn}}{D}} + \sqrt{\tfrac{I_{iNp}}{A}} + \sqrt{\tfrac{I_{iNn}}{A}}\right) \\
&\left(\sqrt{\tfrac{I_{oNp}}{D}} - \sqrt{\tfrac{I_{oNn}}{D}} - \sqrt{\tfrac{I_{iNp}}{A}} + \sqrt{\tfrac{I_{iNn}}{A}}\right) \\
I_{iNn} =& B\left(2\sqrt{\tfrac{I_{oNp}}{D}} - \sqrt{\tfrac{I_{oNn}}{D}} + \sqrt{\tfrac{I_{iNn}}{A}}\right)\left(\sqrt{\tfrac{I_{oNn}}{D}} - \sqrt{\tfrac{I_{iNn}}{A}}\right) \\
&+ C\left(2\sqrt{\tfrac{I_{tail}}{E}} - \sqrt{\tfrac{I_{oNp}}{D}} - \sqrt{\tfrac{I_{oNn}}{D}} + \sqrt{\tfrac{I_{iNp}}{A}} + \sqrt{\tfrac{I_{iNn}}{A}}\right) \\
&\left(\sqrt{\tfrac{I_{oNn}}{D}} - \sqrt{\tfrac{I_{oNp}}{D}} - \sqrt{\tfrac{I_{iNn}}{A}} + \sqrt{\tfrac{I_{iNp}}{A}}\right)
\end{aligned}
\tag{5}
$$

Although (4) and (5) are non explicit equations, the absence of any process parameter demonstrates that Class-AB current transfer functions between $I_{iNp,n}$ and $I_{oNp,n}$ are virtually independent from technology and temperature in both regions of operation under ideal matching conditions. Furthermore, if type-I circuits are used in the VMA architecture of Figure 1, the bias current at the output branches of the OTA is automatically set to $I_{tail}/2$. The variable-mirror nature of the Class-AB proposed stage can be seen in the equivalent right-half circuits of Figure 3(b,c), where the non-linear current amplifier behaves in practice as a current mirror with variable geometrical ratios.

Figure 4 illustrates the flexibility of the proposed type-I current mirror when designing a particular Class-AB modulation index for the overall VMA. In practice, a wide range of OTA responses can be chosen, from strong Class-AB to almost Class-A, by changing the relative weights between A, B and C parameters. Moreover, this variety of responses is also extended to all regions of transistor operation, from weak to strong inversion. In general, the maximum Class-AB output current capability of the type-I VMA can be approximated by:

$$I_{max} \simeq \left(1 + \frac{D}{C}\right) I_{tail} \tag{6}$$

The above expression is actually the unified design equation

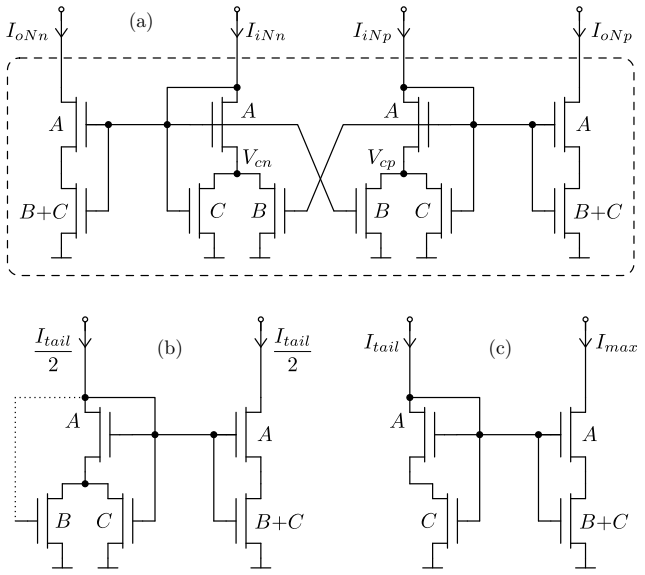

Figure 5. Type-II Class-AB current amplifier (a) proposed for the boxed sections of Figure 1 (NMOS path), and equivalent right-half circuits for Class-A operating point $I_{iNp} \equiv I_{iNn} \equiv \frac{I_{tail}}{2}$ (b) and maximum Class-AB positive output $I_{iNp} \simeq I_{tail}$ $I_{iNn} \simeq 0$ (c). Dotted line indicates virtual short circuit.

for the practical optimization of the OTA slew-rate in all regions of operation, and it is in agreement with the maximum output current values reached in Figure 4. However, if high D/C ratios are selected, deviations caused by technological mismatching can turn into amplifier instability due to excessive positive local feedback, or even the latch of the entire VMA if enough differential input amplitude is applied. In order to prevent this unwanted behavior when working with high Class-AB modulation indexes, the built-in smoother of Figure 3(d) is proposed. This mechanism injects a low-level common-mode input (I_{min}) into the type-I Class-AB current amplifier. Thanks to this minimum biasing level ($I_{iNp,n} \geq I_{min}$), cut-off state is avoided in both sides of the differential structure and VMA transient operation can be smoothed for extreme slew-rate design cases.

B. Type-II

The second Class-AB circuit proposal for the boxed parts of Figure 1 is presented in Figure 5(a). Basically, it replaces the C-sized crossed transistor of Figure 3(a), which is in charge of generating the negative feedback contribution, by two split counterparts. Intuitively, type-I and type-II topologies can be understood as the serial ($B + C$) and parallel ($B||C$) circuit implementation of $V_{cp,n}$, respectively. The aim of the type-II proposal is to bypass the circuit overhead caused by the V_{bias} reference generator of Figure 3(a), and to avoid the possibility of VMA latching under extreme Class-AB modulation indexes.

Supposing weak-inversion operation for all devices, the EKV-based analysis of Figure 5 returns:

$$D \doteq \frac{A(B + C)}{A + B + C} \tag{7}$$

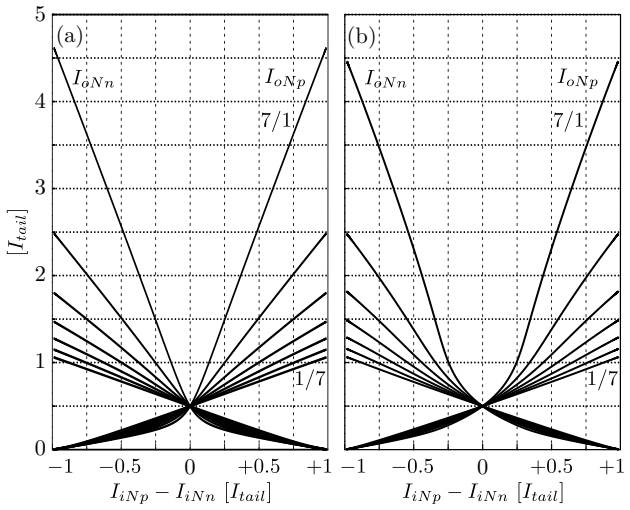

Figure 6. Simulated DC transfer functions for the type-II Class-AB current amplifier of Figure 5(a) under weak (a) and strong (b) inversion operation. Curves are parameterized for $B/C = \{1/7, 2/6, 3/4, 4/4, 5/3, 6/2, 7/1\}$ and $A = 8$.

$$I_{iNp} = \left(\tfrac{B}{D} I_{oNn} + \tfrac{C}{D} I_{oNp}\right)\left(1 - \tfrac{D}{A}\tfrac{I_{iNp}}{I_{oNp}}\right)$$
$$I_{iNn} = \left(\tfrac{B}{D} I_{oNp} + \tfrac{C}{D} I_{oNn}\right)\left(1 - \tfrac{D}{A}\tfrac{I_{iNn}}{I_{oNn}}\right) \tag{8}$$

while the following expression can be obtained in case of strong-inversion operation:

$$\begin{aligned} I_{iNp} =& \Big[2\Big(B\sqrt{\tfrac{I_{oNn}}{D}} + C\sqrt{\tfrac{I_{oNp}}{D}}\Big) \\ & -(B+C)\Big(\sqrt{\tfrac{I_{oNp}}{D}} - \sqrt{\tfrac{I_{iNp}}{A}}\Big)\Big]\Big(\sqrt{\tfrac{I_{oNp}}{D}} - \sqrt{\tfrac{I_{iNp}}{A}}\Big) \\ I_{iNn} =& \Big[2\Big(B\sqrt{\tfrac{I_{oNp}}{D}} + C\sqrt{\tfrac{I_{oNn}}{D}}\Big) \\ & -(B+C)\Big(\sqrt{\tfrac{I_{oNn}}{D}} - \sqrt{\tfrac{I_{iNn}}{A}}\Big)\Big]\Big(\sqrt{\tfrac{I_{oNn}}{D}} - \sqrt{\tfrac{I_{iNn}}{A}}\Big) \end{aligned} \tag{9}$$

Analytical expressions (8) and (9) are again non explicit, but they still show no technological parameters nor temperature dependencies. Like in the type-I circuit proposal, the current bias point at the output branches of Figure 1 is automatically fixed to $I_{tail}/2$ by simple device matching. The variable-mirror nature of this Class-AB stage can be also seen in the equivalent right-half circuits of Figure 5(b,c), where the non-linear current amplifier behaves as a current mirror with variable geometrical ratios.

Similarly to Section III-A, Figure 6 demonstrates the possibility of choosing a wide range of Class-AB modulation indexes in all regiosn of operation by the proper selection of A, B and C values. In the particular case of type-II, the maximum output current of the VMA under Class-AB regime can be approximated as:

$$I_{max} \simeq \frac{1 + \frac{A}{C}}{1 + \frac{A}{B+C}} I_{tail} \tag{10}$$

Again, the above unified expression for both weak and strong inversion operation is in agreement with the maximum current levels returned by Figure 6.

Comparatively speaking, the type-II VMA proposal not only avoids the extra biasing and anti-latching circuits of the type-I counterpart, but it also exhibits a higher current capability in the intermediate slewing, as concluded when comparing Figures 4 and 6. On the other hand, the type-I VMA topology opens the possibility of on-the-fly tuning of Class-AB modulation indexes through the dynamic control of V_{bias} level.

IV. Settling Time Analysis

As already introduced in Section I, the proposed VMA family is well suited for their use in low-power SC circuits. In this context, there is a typical design trade-off between the supply power consumption and the maximum sampling rate for a given dynamic range specification. OTA slew-rate plays a critical role in this design trade-off, thus both (6) and (10) are key equations when optimizing VMAs for low-power SC circuits. In this sense, they can be unified under the Class-AB peak modulation index:

$$k_{AB} \doteq \frac{I_{max}}{I_{tail}} = \begin{cases} 1 + \dfrac{1}{C}\dfrac{AB}{A+B} & \text{type I} \\ 1 + \dfrac{1}{C}\dfrac{AB}{A+B+C} & \text{type II} \end{cases} \tag{11}$$

However, the maximum sampling rate is not only limited by slew-rate performance but also by amplifier settling time. Consider the full-scale case scenario illustrated in Figure 7, where the VMA is operated in a typical SC integrator. The displayed waveforms correspond to the the second half of the sampling period (T_S), when the charge stored in the sampling capacitor need to be transfered to the feedback counterpart for its integration. The VMA used as a charge pump for this purpose will show two qualitatively different transient parts: the slewing time (t_{slew}), or Class-AB large-signal operation dominated by the VMA slew-rate performance (SR), and the settling time (t_{sett}), when the VMA progressively tends to its Class-A bias point driven by the small-signal time constant (τ) of the single-stage topology.

Applying the first-derivative continuity condition at the boundary between the slewing and settling times of Figure 7, the overall sampling period is found to be:

$$\frac{T_S}{2} = \underbrace{\frac{V_{FS}}{SR} - \tau}_{t_{slew}} + \underbrace{\tau \ln \frac{\tau SR}{\epsilon V_{FS}}}_{t_{sett}} \tag{12}$$

where V_{FS} and ϵ stand for the differential full-scale voltage and the residual error referred to the former. Interestingly, static power consumption in Figure 7(b) is minimized for:

$$t_{slew} \equiv 0 \qquad SR \equiv \frac{V_{FS}}{\tau} \qquad \frac{T_S}{2} \equiv t_{sett} = \tau \ln \frac{1}{\epsilon} \tag{13}$$

While this design strategy effectively allows the maximum time constant, so the lowest power consumption at the Class-A bias point of the VMA, it also imposes the maximum peak modulation index during its Class-AB operation according to:

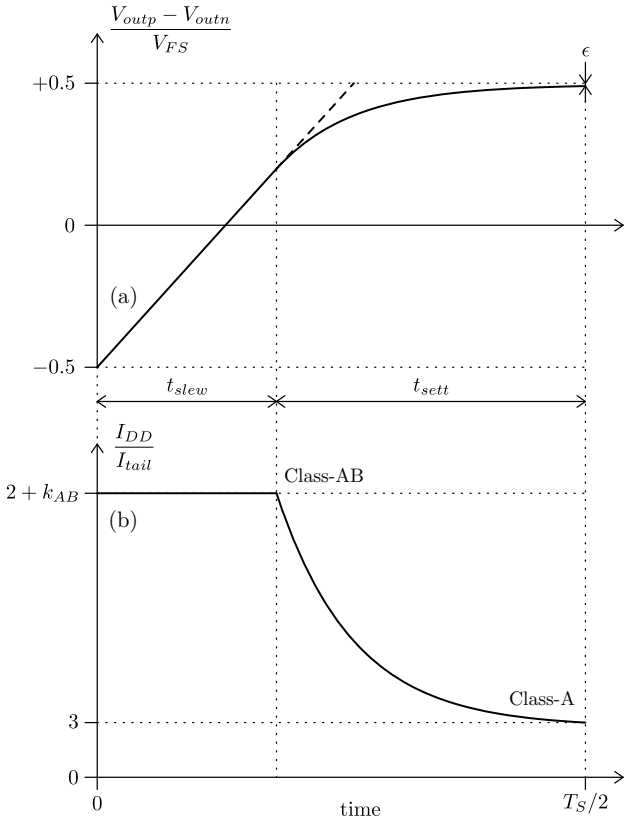

Figure 7. Qualitative transient response of the VMA differential output voltage (a) and supply current (b) during the integrating phase of a SC integrator for positive full-scale input. Drawing not in scale.

$$SR = \frac{I_{max}}{C_{load}} = \frac{k_{AB} I_{tail}}{C_{load}} \tag{14}$$

In our context, C_{load} is the equivalent load capacitance derived from the combined output and feedback capacitor networks of the corresponding SC integrator. Concerning the Class-A time constant, its expression can be directly obtained from the gain-bandwidth product (GBW) of the VMA single-stage topology. In the most optimistic case of weak inversion operation for the input transconductance (G_m) of Figure 1:

$$\frac{1}{\tau} = 2\pi GBW = \frac{G_m}{C_{load}} = \frac{I_{tail}/2}{nU_t C_{load}} \tag{15}$$

Hence, by substituting (14) and (15) in (13), the maximum VMA Class-AB modulation index required to minimize static power consumption is:

$$k_{ABmax} = \frac{V_{FS}}{2nU_t} \tag{16}$$

In practice, optimum k_{AB} values are usually found well below this upper limit due to the effect of: moderate or strong inversion operation of the VMA input transconductors, which return larger time constant values for the same tail-current bias level; step amplitudes lower than the worst-case condition of $\pm V_{FS}$ in Figure 7(a); and the parasitic pole at the gate of the A-sized transistors of Figure 1, which may introduce ringing during settling time.

This latter effect can be studied through the equivalent single-ended input resistance ($1/g_{par}$) of the Class-AB current amplifiers of Figure 3(a) and 5(a). The EKV MOSFET small-signal model returns the following g_{par} expressions normalized to the transconductance of an A-sized active load (g_{mgA}):

$$\frac{g_{par}}{g_{mgA}} = \begin{cases} \dfrac{-ng_{mgB} + g_{mdB} + 2g_{mdC}}{ng_{mgA} + g_{mdB} + 2g_{mdC}} & \text{type I} \\ \dfrac{n(-g_{mgB} + g_{mgC}) + g_{mdB} + g_{mdC}}{ng_{mgA} + g_{mdB} + 2g_{mdC}} & \text{type II} \end{cases} \tag{17}$$

As expected, the negative terms shown above come from the local positive feedback supplied by the cross-coupled B-sized MOS pairs, which is compensated by the C-sized transistors. In general, the resistance of this parasitic pole is very low compared to the dominant pole located at the VMA output, specially if cascode transistors are introduced to improve open-loop voltage gain, like in the design example of Section V. However, if large enough Class-AB modulation indexes are selected, g_{par} can become virtually null in (17) and move the parasitic pole to low frequency, with the corresponding VMA stability issues in closed-loop operation. Hence, special attention must be paid to not increase the capacitance of this parasitic pole when sizing A, B and C transistors. In this sense, it is a good practice to choose minimum channel length for these devices. Also, by inspecting (11), the total gate area of the parasitic node can be minimized with the following unified rule of thumb:

$$\left.\begin{array}{ll} \text{type I} & A \equiv B \\ \text{type II} & A \equiv B + C \end{array}\right\} \quad k_{ABopt} \equiv 1 + \frac{B/C}{2} \tag{18}$$

V. Practical Design in 0.18μm CMOS Technology

This section presents a practical example of type-II VMA design in 0.18μm 1.8V CMOS technology for its use in the first SC stage of a high-resolution $\Delta\Sigma$ ADC. In this particular case study, the main circuit specifications are sampling, feedback and output capacitances of 64pF, 212pF and 5pF values, respectively (i.e. $C_{load} \simeq 54$pF), and target sampling period $T_S/2 < 35$ns for a residual error $\epsilon = 0.035\%$ referred to the differential full-scale voltage $V_{FS} = 2.4\text{V}_{\text{pp}}$.

Figure 8 details the VMA schematic sizing obtained from the settling time analysis described in previous section. The equivalent design parameters for the type-II Class-AB current amplifiers are $A = 4$, $B = 3$ and $C = 1$ with extra geometrical scaling at the output transistors. The optimized $k_{AB} = 2.5$ verifies (18) and it is well below the theoretical maximum value of 32 returned by (16) for $n = 1.5$ and room temperature. Compared to Figure 1, cascode transistors are added to the OTA output branches for the purpose of improving open-loop voltage gain. The optimum biasing of these stacked devices for a maximum output full-scale voltage can be obtained from [27]. As a positive side effect, minimum channel-length devices can be selected to minimize parasitic capacitance.

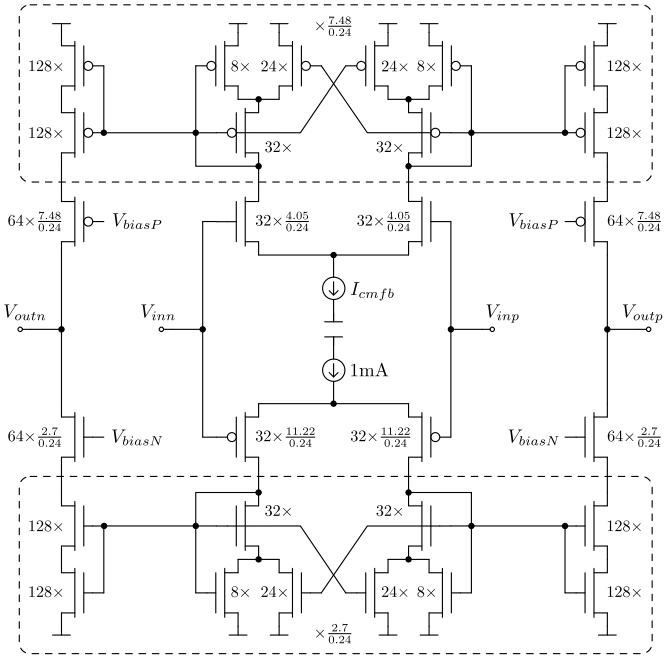

Figure 8. Type-II VMA design example in 0.18μm 1.8V CMOS technology. All device dimensions are given in μm.

Simulation results for this OTA circuit example are reported in Figures 9, 10 and 11. The VMA Class-AB behavior is as expected from the analytical model of Section III-B, with the slight reduction in the current peak value observed in Figure 9 due to the cascode biasing scheme adopted to maximize output full-scale voltage. Furthermore, the VMA Class-AB operation shows a remarkable low sensitivity to both technology and temperature deviations, as demonstrated in the corner study of Figure 9(b).

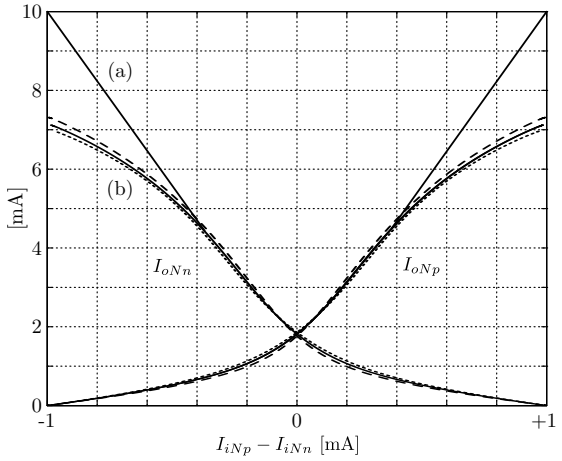

Figure 9. Analytical (a) and simulated (b) Class-AB DC current transfer curve for the type-II VMA of Figure 8 (NMOS path), and typ/27°C (solid), fast/-40°C (dashed) and slow/80°C (dotted) simulation corners.

Concerning the open-loop dynamic performance of Figure 10(a), the single-stage VMA circuit can achieve high-gain values while maintaining the parasitic pole frequencies well above GBW. In fact, it is worth to highlight the robustness of VMA stability under closed-loop operation for multi-decade range of capacitive load conditions, as studied in Figure 10(b).

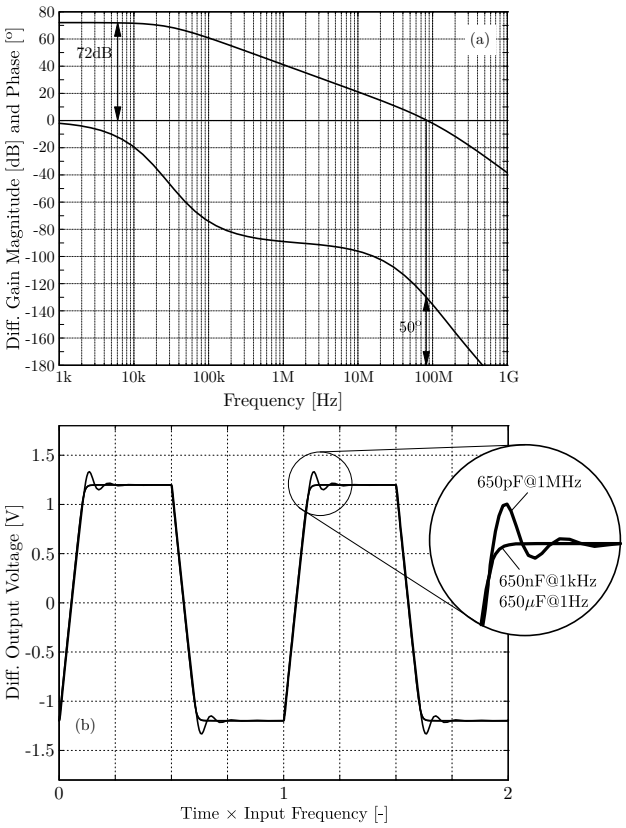

Figure 10. Simulated open-loop frequency response for 200pF load (a) and step response under scaled load and frequency conditions (b) for the type-II VMA of Figure 8.

Finally, Figure 11 presents a comparative analysis in terms of static CMRR and PSRR$_+$ between the proposed Class-AB VMA design example of Figure 8 and its equivalent Class-A current-mirror OTA counterpart (i.e. same device sizing and bias levels). As it can be seen, no degradation can be noticed due to the proposed Class-AB mechanism. In fact, the variable-mirror symmetry allows to keep almost the same performance, showing average rejection ratios exceeding 100dB and standard-deviation values below 10dB.

VI. Experimental Results

The type-II VMA circuit example of Figure 8, together with its own SC network for CMFB control, has been integrated in 0.18μm 1P6M MiM 1.8V CMOS technology, as depicted in Figure 12. Characterization results under unity gain resistive inverter configuration are reported in Figures 13 and 14 together with Table I. In all cases, good agreement is observed between simulated and experimental data, like in the dynamic Class-AB measurements of Figure 14.

Table I includes a comparative study between the tested type-II VMA example and previous Class-AB OpAmp and OTA literature according to the following well-accepted figure-of-merit:

$$\text{FOM} = \frac{\text{SR} \times C_{load}}{P_D} \tag{19}$$

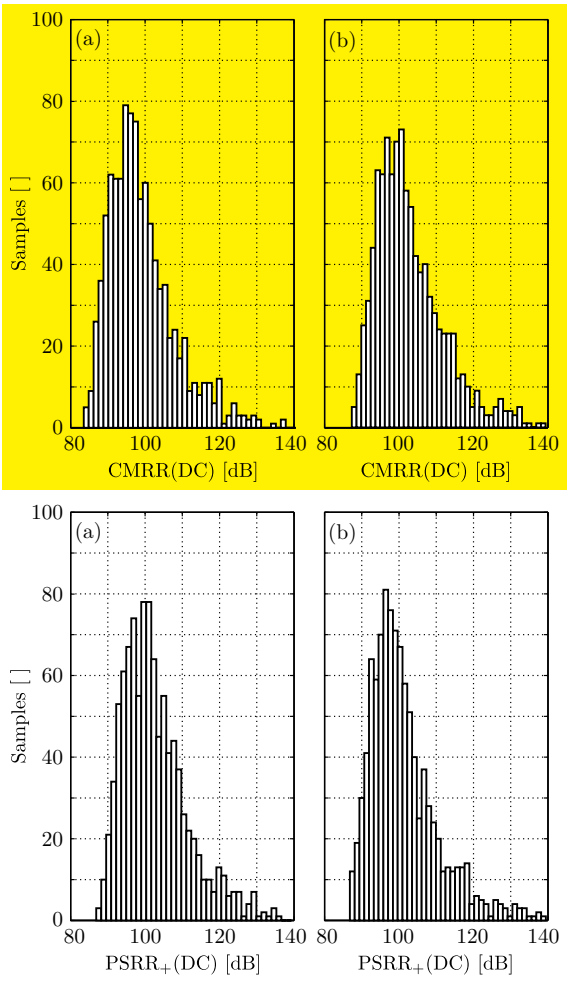

Figure 11. Simulated CMRR and PSRR deviations due to technology mismatching for (a) the type-II Class-AB VMA of Figure 8 and (b) its equivalent Class-A current-mirror OTA counterpart (i.e. same device sizing and bias levels).

where P_D stands for the static power consumption. In terms of Class-AB capabilities, references [11], [15] report extremely high FOM values but at the cost of poorer gain performance figures (below 50dB), of requiring resistors for their CMOS integration and of a higher sensitivity to technology. Considering the rest of state-of-art proposals, the presented work returns the highest FOM with an improve of at least 25% of its value.

VII. Conclusions

A new family of Class-AB OTA circuits based on single-stage topologies with non-linear current amplifiers has been presented. The novel VMA architecture, when appropriately applied, avoids the need for any internal frequency compensation mechanism, and it is characterized by investing the whole Class-AB current in the output transistors only. Furthermore, thanks to their matched-based design, both type-I and type-II VMA Class-AB behavior exhibits very low sensitivity to both technology and temperature deviations. Analytical expressions valid in all regions of operation are presented for the proposed circuits to minimize VMA settling time under discrete-time operation. The resulting OTAs are suitable for low-power SC

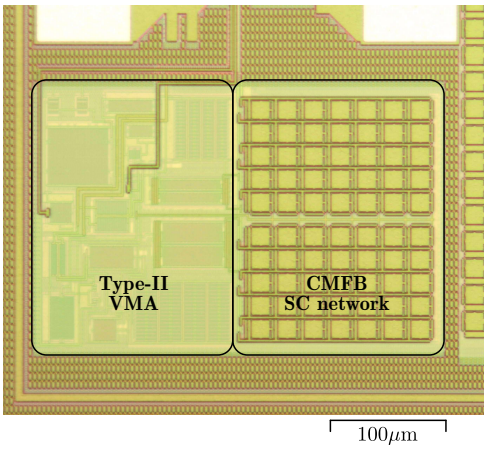

Figure 12. Micrograph of the type-II VMA of Figure 8 and its CMFB capacitive network integrated in 0.18μm 1P6M 1.8V CMOS technology. Overall circuit size is 335μm $\times$ 210μm (0.07mm^2).

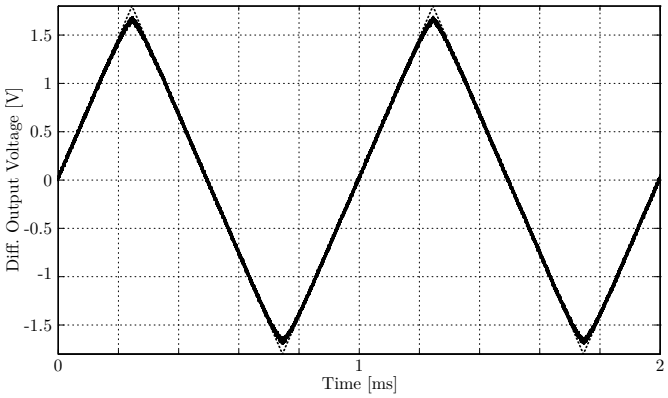

Figure 13. Experimental (solid) an ideal (dotted) transient response of the type-II VMA of Figure 12 at 3.6V$_{pp}$ differential input and 650nF load.

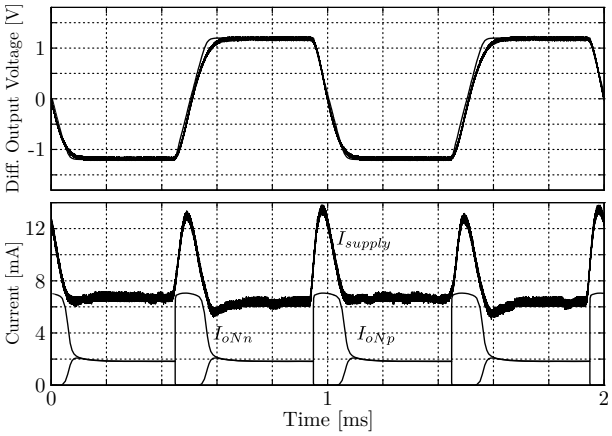

Figure 14. Experimental (thick) and simulated (thin) step response of the type-II VMA of Figure 12 at 2.4V$_{pp}$ differential input and 650nF load.

Table I
CLASS-AB OPAMP AND OTA CIRCUIT COMPARISON.

Parameter	[16]	[10]	[13]	[17]	[18]	[11]	[19]	[15]	[21]	[14]	[6]	[22]	This work
CMOS technology [μm]	0.5	1.2	0.25	0.8	0.8	0.5	0.18	0.5	0.18	0.18	0.13	0.09	0.18
Supply voltage [V]	1.8	3	1.2	1.5	1.5	2	1	2	1.8	1.8	1.2	1.2	1.8
DC Gain [dB]	94	63	69	67	60	43	58.25	45	53.6	74	70	59.8	72
Eq. noise [$\frac{\text{nV}_{\text{rms}}}{\sqrt{\text{Hz}}}$@100kHz]	7.9	19	21.2	17	21						14.1	34.9	0.8
Load capacitance [pF]	4	35	4	10	10	80	5	25	5.6	1.75	5.5	5	200
GBW [MHz]	26	8	165	15	15	0.725	79.53	11	134.2	160	35	348.1	86.5
Phase margin [deg]	64		65	80	75	89.5	61		70.6		45	62.2	50
Slew rate [V/μs]	104	10.2	329	10	10	89	2.3	20	94.1	26.6	19.5	173	74.1
Power [mW]	0.6	0.534	5.8	0.3	0.39	0.12	0.067	0.04	1.44	0.362	0.11	0.852	11.9
Area [mm^2]		0.061				0.024		0.012	0.005		0.012		0.070
FOM [$\frac{\text{V}}{\mu\text{s}}\frac{\text{pF}}{\mu\text{W}}$]	0.69	0.67	0.28	0.33	0.26	59.33	0.17	12.5	0.366	0.129	0.98	1.015	1.25
Resistor-free	No	Yes	Yes	No	No	No	Yes	No	Yes	No	Yes	Yes	Yes

circuits and specifically optimized for SOA fast power on-off operation and multi-decade load capacitance specifications. A complete design example integrated in standard 0.18μm 1P6M MiM 1.8V CMOS technology is presented with detailed simulation and experimental results to proof the validity of the proposed VMA architecture. Compared to resistor-less state-of-art Class-AB OpAmp and OTA literature, the proposed VMA family returns the highest FOM value.

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