Interdigitated design of a thermoelectric microgenerator based on silicon nanowire arrays

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ABSTRACT

Silicon nanowires thermoelectric properties are much better than those of silicon bulk. Taking advantage of silicon microfabrication techniques and compatibilizing the device fabrication with the CVD-VLS silicon nanowire growth, we present a thermoelectric microgenerator based on silicon nanowire arrays with interdigitated structures which enhance the power density compared to previous designs presented by the authors. The proposed design features a thermally isolated silicon platform on the silicon device layer of an SOI silicon wafer. This silicon platform has vertical walls exposing <111> planes where gold nanoparticles are deposited by galvanic displacement. These gold nanoparticles act as seeds for the silicon nanowires. The growth takes place in a CVD with silane precursor, and uses the Vapor-Solid-Liquid synthesis. Once the silicon nanowires are grown, they connect the silicon platform with the silicon bulk. The proposed thermoelectric generator is unileg, which means that only one type of semiconductor is used, and the second connection is made through a metal. In addition, to improve the thermal isolation of the silicon platform, multiple trenches of silicon nanowire arrays are used, up to a maximum of nine. After packaging the device with nanowires, we are able to measure the Seebeck voltage and the power obtained with different operation modes: harvesting mode, where the bottom device is heated up, and the silicon platform is cooled down by natural or forced convection, and test mode, where a heater integrated on the silicon platform is used to produce a thermal gradient.

Keywords: Silicon nanowires, thermoelectric, energy harvesting, microgenerator, nanowire arrays, interdigitated structures.

1. INTRODUCTION

Micro and nanotechnologies have already made possible the fabrication of small, low cost and good performance sensors that are called to be protagonists of continuous monitoring scenarios and distributed intelligence paradigms (Internet of Things, Trillion Sensors). Energy autonomy keeps being one of the most desired enabling functionalities in the context of off-grid applications, such as wireless sensor networks. In many such applications, wired power is not feasible and batteries are normally used. However, battery replacement will eventually become impractical (economically, environmentally, and logistically) not only for sensor networks in remote places or harsh environments, but also for more standard applications if the number of nodes explodes exponentially.

Harvesting energy, tapping into environmentally available sources such as heat and vibrations, may be a good solution in man-made scenarios applications. Energy densities of $100\mu W/cm^2$ seem appropriate for many such applications. Furthermore, coupling those harvester devices to secondary batteries to buffer enough energy to account for the power demand peaks required by the communication unit of wireless nodes could be a quite enabling energy autonomy solution. Silicon technologies provide an enabling path to miniaturization, 3D architectures (improved energy densities), mass production with economy of scale, and the ability of power intelligence integration. Being silicon technologies the ones used for the fabrication of the sensors themselves, they are the prime candidate for building microenergy solutions of similar robustness able to power such sensors during their whole lifetime.

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2. DESIGN

Thermoelectric materials efficiency is measured by the dimensionless figure of merit *ZT*, defined as:

$$ZT = \frac{S^2 \cdot \sigma \cdot T}{\kappa} \tag{1}$$

Where S is the Seebeck coefficient [V/K], σ is the electrical conductivity [$\Omega^{-1} \cdot m^{-1}$], T is the temperature [K] and κ is the thermal conductivity [W/(m·K)]. Only materials with $ZT \geq 1$ are regarded as good thermoelectric materials [1]. Traditional thermoelectric modules are mainly based on Bi_2Te_3 or PbTe and use alternating p-type and n-type pellets (see figure 1).

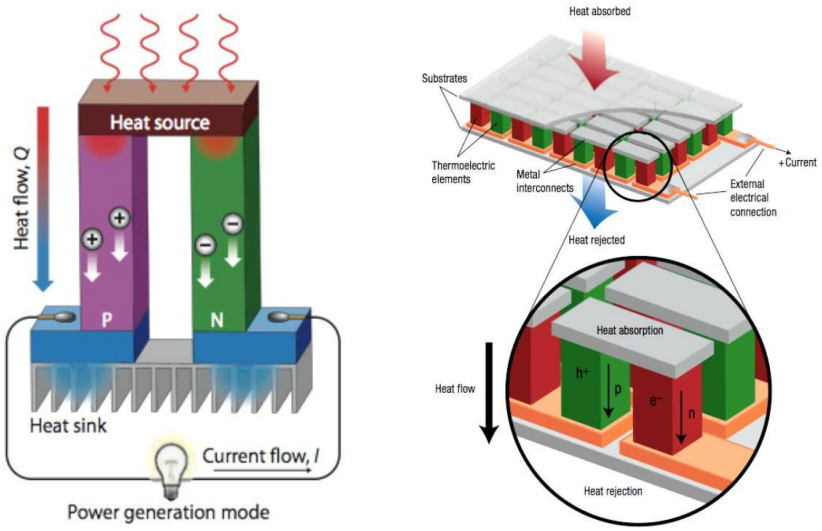

Figure 1: (left) Schematic representation of a thermoelectric generator working between a heat source and a heat sink formed by p-type and n-type elements [2]. (right) Thermoelectric module showing charge and heat flow [3].

Materials nanostructuring can dramatically enhance the thermoelectric properties of materials which in bulk form have moderate or low ZT values [4-5]. Moreover, it has been reported [6-7] that silicon nanowire thermoelectric properties surpass those of silicon in bulk form. From this information, the authors have been working on overcoming the issue of integrating the device microfabrication and the silicon nanowire growth [8-9]. The device geometry to make the silicon nanowire growth process compatible with the platform microfabrication is based on a suspended silicon platform (*S1*) connected to another silicon mass (*S2*) through multiple arrays of silicon nanowires (figure 2).

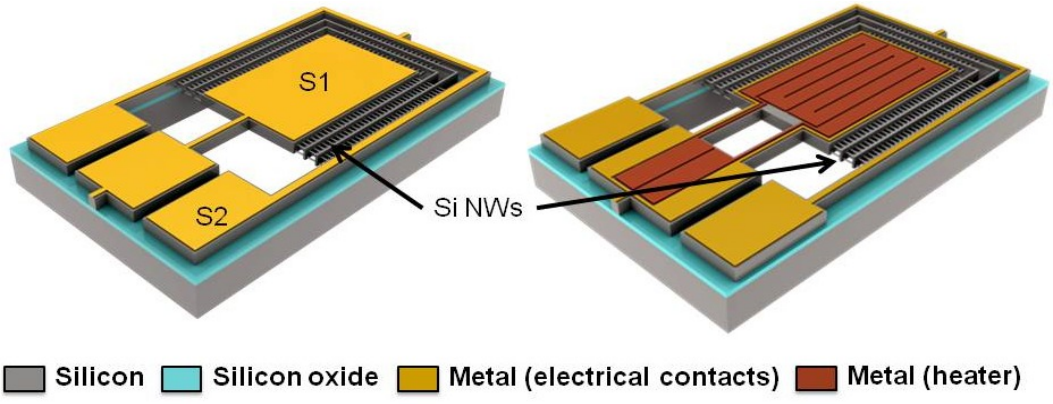

Figure 2: Schematic representation of the proposed design for the micro thermoelectric generator (μTEG). The device on the right doesn't have a heater while the device on the right includes an internal heater. Both images correspond to a device with three trenches, where the silicon nanowires are grown.

Comparing figure 2 with figure 1 (left), our device has only one type of semiconductor and the second element is a metal. These thermoelectric devices are called unileg. The parallel connection of the p-type silicon nanowires represents an equivalent single semiconductor element, while the second element in our device corresponds to the metal leads in the *S1* platform.

The proposed device in this work is an improvement of the previously presented design featuring an interdigitated platform which increases the number of nanowires while preserving the device area.

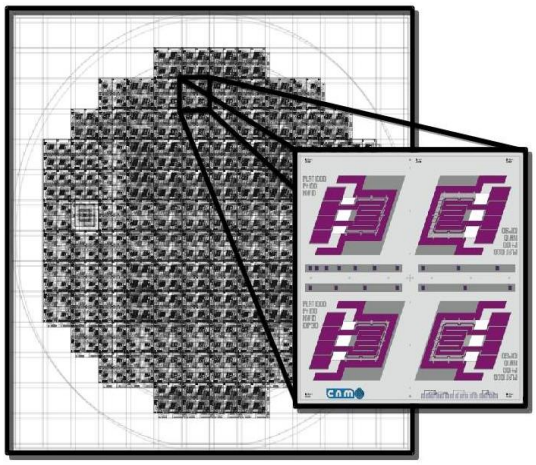

Figure 3: Mask set used on photolithographic processes to pattern the different layers involved in the fabrication of the complete device. Each chip is 7x7mm2, and contains four different devices, as seen on the inset.

3. FABRICATION

The fabrication starts from a SOI wafer, with 15µm thick Si device layer, and 0.5µm thick buried oxide layer, on top of a 500µm thick Si bulk. The particularity of the silicon nanowire growth, which only takes place along the <111> direction, forces the orientation of the silicon device layer to be (110) so that we are able to vertically etch trenches in the silicon with exposed planes corresponding to <111> planes. Therefore, the Si device layer of the SOI wafer must have a (110) orientation which is not standard. However this does not apply for the SOI silicon bulk which has the standard orientation of (100).

Initially a 400nm thick thermal oxide layer is grown on both layers. This layer is used as an insulator of the heater, to avoid any electrical path from the heater to the internal or external collectors. Once deposited, it is patterned using photolithography (see figure 3) and a wet etch process, after which the photoresist is stripped. After that, an adhesion layer of 30nm Ti/W (10%/90%) and a 200nm thick tungsten layer are deposited by sputtering. Another photolithography and a wet etch step pattern the metal leads which define the heater, and the internal and external collectors. Once the metal is patterned, it is passivated with a 1µm thick SiO_2 deposited by PECVD. The last step on the device layer is to define the silicon platform and the trenches. This is done with another photolithographic step and a dry etch process, which removes sequentially the silicon oxide layer and the silicon device layer, until it reaches the buried oxide layer. Finally, the last process is a DRIE of the bulk silicon from the bottom, using a patterned 1µm thick aluminum layer as a hard mask. This last step completely defines the thermoelectric generator with all the metals and silicon passivated, except the silicon vertical walls which expose the <111> planes for the silicon nanowire growth.

Different device designs have been fabricated, including different platform sizes (500µm and 1000µm), two different heater lead widths (50µm and 100µm), different number of trenches (1,3,6 and 9) and squared platform structures as well as interdigitated structures (see figure 4). In this paper we show the results of an interdigitated structure with different number of trenches, namely 1, 3 and 9. Each trench is 10µm wide and the silicon bars defining the trenches are 3 µm wide. Therefore the total distance from the silicon platform to the silicon bulk is $9 \cdot 10\mu m + 8 \cdot 3\mu m = 114\mu m$. The perpendicular silicon bars (like the horizontal one shown in the detail of figure 4) are used to keep the platform and the silicon bulk aligned, and facing each other. Without these structures the silicon platform tends to bend upwards due to thermomechanical stresses induced by the different layers present, which prevents the silicon nanowires to connect

effectively both structures as they would not be fully aligned. These perpendicular silicon bars can be cut with FIB once the silicon nanowires have been grown, as is shown in the Results section of this paper.

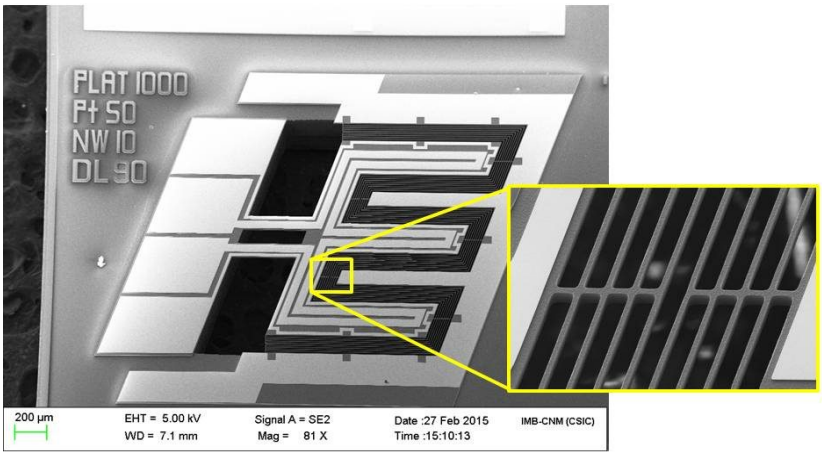

Figure 4: SEM image shown one of the devices in a chip. This corresponds to an interdigitated structure with 9 trenches, a silicon platform of 1000µm and a metal lead width of 50µm. A detail of the 9 trenches is shown on the right inset.

Figure 5: CVD equipment from First Nano, model EasyTube® 3000, located at IREC facilities and used to grow the silicon nanowires by VLS.

VLS-CVD silicon nanowires

Once the device is completed the silicon nanowires need to be grown on the vertical walls defining the trenches which separate the silicon platform from the silicon bulk. A CVD process is used to grow them perpendicularly from <111> walls following a Vapor-Liquid-Solid synthesis mechanism. This process is carried out at IREC facilities where a First Nano's CVD EasyTube® 3000 is located (see figure 5). The galvanic displacement method is used to control the deposition of gold catalyst nanoparticles, which act as seeds for the silicon nanowires, only at exposed silicon surfaces (see figure 6 left). It does not deposit gold nanoparticles on the silicon oxide passivation covering the rest of the device. Once the gold nanoparticles are deposited, the device goes through the CVD process where the silicon nanowires grow (see figure 6 right). The conditions used include a pressure between 2.5 and 20 Torr, temperatures ranging from 520ºC to 725ºC, and growth times from 15 to 60 minutes. The gases used during the growth are hydrogen (1000 sccm), hydrochloric acid (15 sccm) and diluted silane (10% in hydrogen, with a flow rate of 150 sccm) [10]. Once the process is completed the silicon nanowires can be seen on any silicon exposed area which is not covered by silicon oxide (see figure 7).

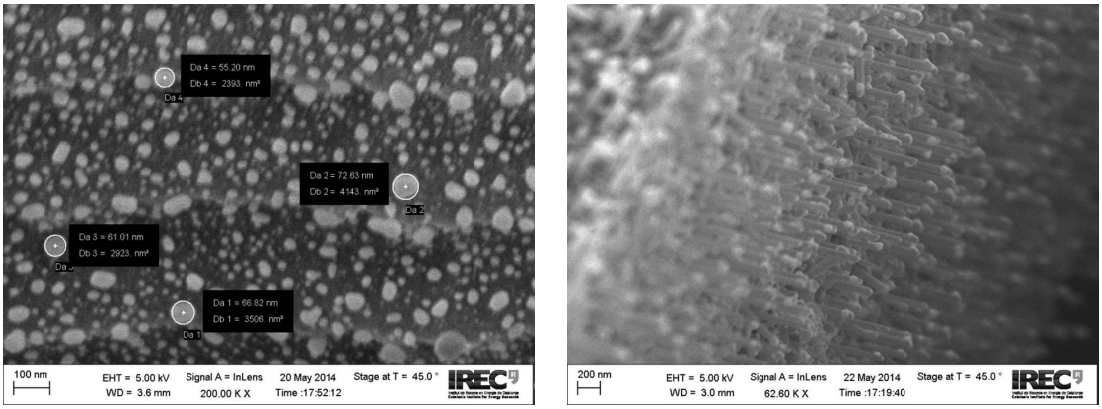

Figure 6: (left) SEM image of a vertical wall after the gold nanoparticles have been deposited by galvanic displacement. Diameter values measured on selected nanoparticles ranging from 50nm to 80nm. (right) SEM image of a tilted vertical wall after a few minutes of growth where the gold nanoparticles can be seen on the tip of the silicon nanowires.

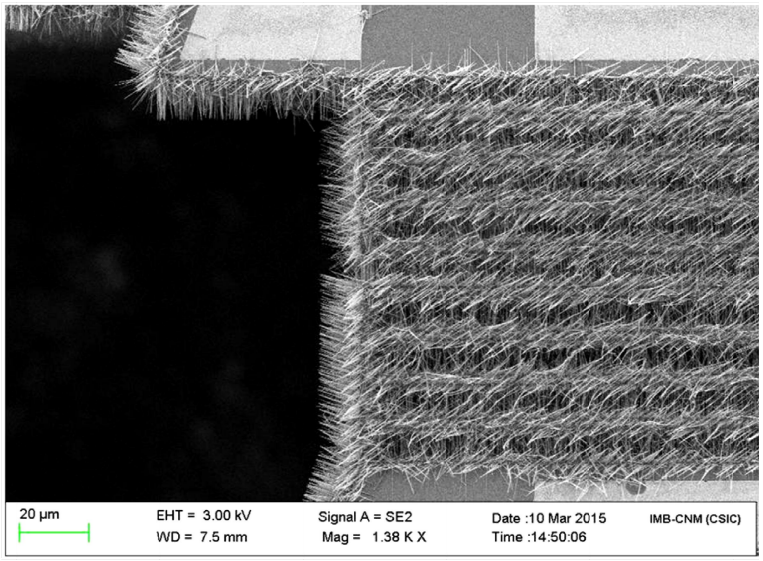

Figure 7: SEM image of a nine trench device with silicon nanowires grown covering the 10µm distance on each trench.

4. EXPERIMENTAL SETUP

The first characterization made on the packaged device is the measurement of the Temperature Coefficient of Resistance (TCR) of the heater. This allows us to have an estimation of the temperature platform. The value we obtain corresponds to the average resistance of the whole heater, but as most part of it lies on the platform we have an idea of the platform average temperature. To measure it we place the packaged device inside an oven together with a thermocouple. The oven is heated up to 250ºC and once that temperature is reached it's turned off, and measurements are taken while the oven is cooling down. The cooling ramp is slow enough to ensure that the whole device is at the same temperature when the measurements are taken (see figure 8). The heater resistance temperature dependence can be written as follows:

$$R = R_0 \cdot \left(1 + \alpha \cdot \Delta T\right) \tag{2}$$

Where R is the measured resistance in Ω, R_0 is the resistance at $T=T_0$, α is the TCR in $ºC^{-1}$, and $\Delta T=T-T_0$ measured in ºC. The value obtained after characterizing the four devices on the packaged chip is $\alpha=1920\cdot10^{-6}$ $ºC^{-1}$. The process is automated with a program using LabVIEW, and takes about 4-6 hours to complete the TCR characterization.

Once the TCR is obtained, we can use the heater as a temperature sensor, correlating its resistance value with the average temperature using equation (2). The next step in characterizing the devices is measuring the actual Seebeck voltage from the silicon nanowires (see figure 9). To do so, as we said before, we can use the heater to generate a thermal gradient between the platform and the silicon bulk. In such a case, we are characterizing the test mode of the device, and the thermal gradients produced can reach 200ºC. On the other hand, when the heater is only used as a temperature sensor, we are characterizing the harvesting mode of the device. To do so, we use an Examina (Linkam) stage (see figure 10) which has a thermal chuck capable of reaching temperatures up to 350ºC.

Figure 8. Experimental setup to measure TCR from a packaged device using an oven. Kapton tape is used to avoid short-circuit between contiguous leads of the package. A thermocouple is used to get the temperature measurements while 4-wire resistance measurements of the heater resistance are taken.

The packaged device is left on top of the thermal chuck using a silver paste to enhance the thermal contact between both surfaces. While the bottom part of the device is at high temperatures the top of the device is left at ambient temperature so that it cools either by natural convection or by forced convection. In the former case, no air is applied directly to the device, but the lid is left open on the Linkam station. In the latter case, a silicone tube with approximately 4mm in diameter is positioned vertically 5cm above the device, pointing downwards, and a pressure of 0.2 bar is applied to let the air flow (not shown in figure 9). In such a case the heat exchange between the platform and the ambient is enhanced, and therefore lower platform temperatures are expected, which correspond to larger thermal gradients seen by the nanowires. Once the thermal setup is settled, the electrical connections are done for each device at a time. We cannot characterize the four devices on each chip at once, because the maximum number of electrical connections to the exterior of the Linkam is 8. Therefore, once a device has been completely characterized, the next device needs to be connected.

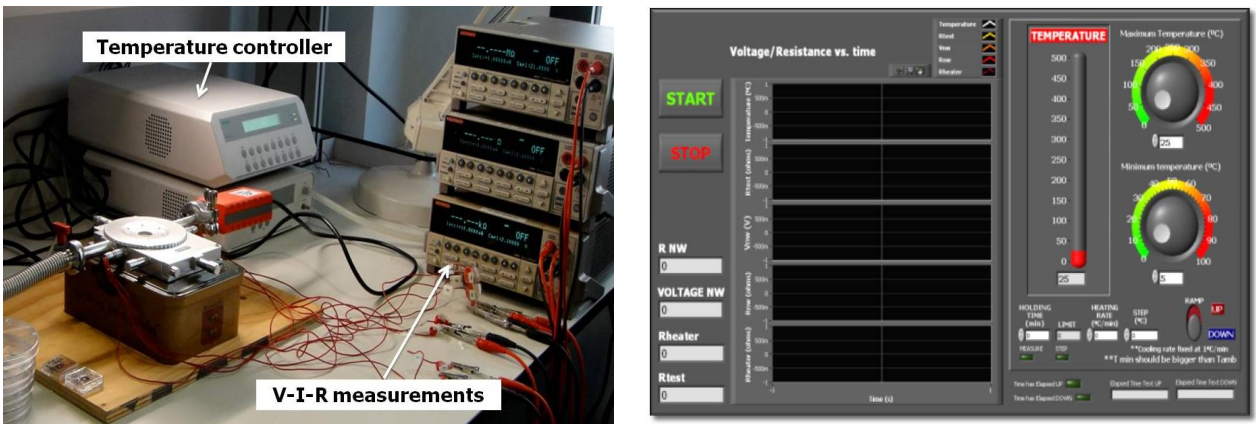

Figure 9: Experimental setup to characterize the device thermally and electrically, including an Examina stage from Linkam®, the associated temperature controller, and three source-meters from Keithley®. On the right the user interface from the LabVIEW program used to setup a measurement process.

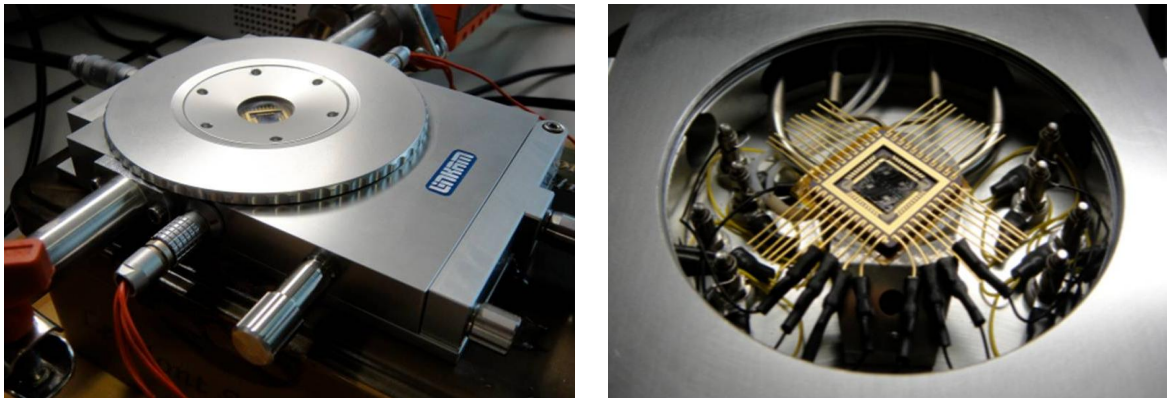

Figure 10: Examina stage THMS350EV from Linkam Scientific Instruments. Apart from having the capability to reach temperatures up to 350ºC, it has 8 electrical connections to extract signals from the stage.

The parameters measured in a measurement sequence include the voltage and resistance between the internal and the external collector, V_{NW} and R_{NW}, and the heater resistance, R_{heater},

5. RESULTS

The first type of measurements made is the nanowire resistance, measuring from the internal collector to the external collector. The result for devices N1, N3 and N9 is shown in table 1:

Table 1. Nanowire resistance measured in devices N1, N3 and N9.

	R_{NW} [Ω]
N1	46
N3	93
N9	700

As it can be seen the difference of the nanowire resistance for the three devices is quite significant. This difference is aligned but not linearly dependent on the effective length of the nanowires ensemble (i.e. number of trenches). Other factors contributing may be overall nanowire density variations among the devices, or particular geometrical aspects of the different structures which also feature supporting silicon bars in parallel with the silicon nanowires. To get rid of the silicon bars contribution to the thermal and electrical response , they were cut with FIB (see figure 11).

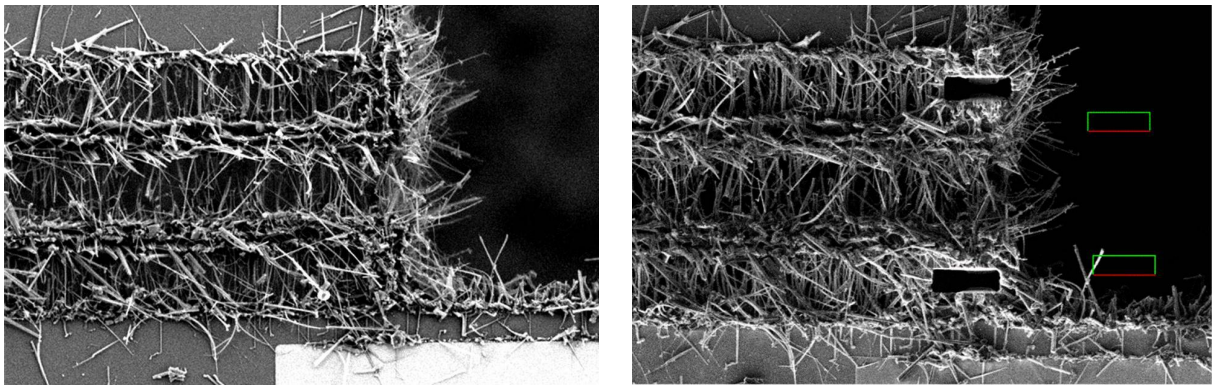

Figure 11: SEM images showing a close-up view of the trenches in a N3 device, before (left) and after (right) FIB to cut the silicon bars connecting the structures.

The effect of cutting the silicon bars with FIB is shown in figure 12. As it can be seen, for any device, when the hotplate is set at a given temperature, the Seebeck voltage (between the internal and external collectors) increases after the FIB. Therefore, once the silicon bars are cut, a larger thermal gradient develops and thus a larger voltage is generated. That means that the silicon bars contribution to the thermal conductivity is significant.

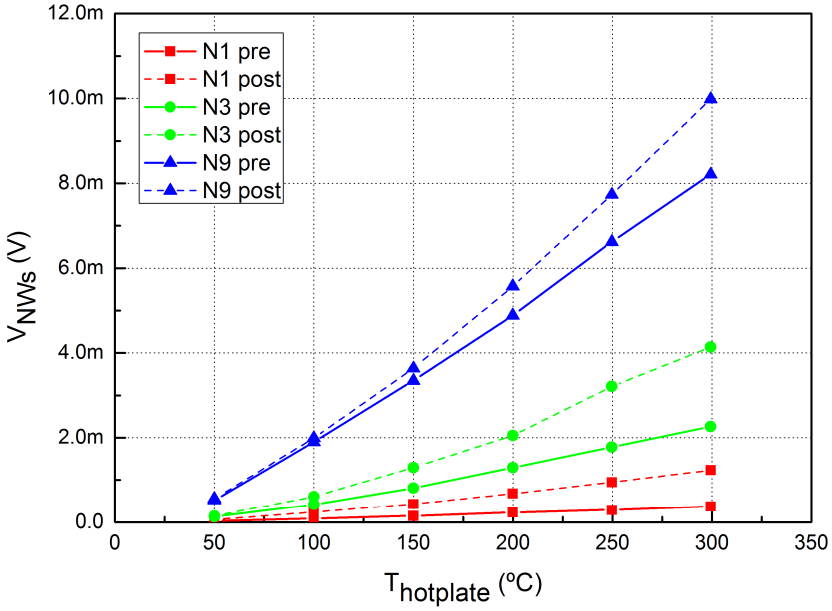

Figure 12: Voltage between internal and external collectors for different hotplate temperatures in harvesting mode. Devices N1, N3 and N9 are compared before and after cutting the silicon bars connecting the silicon platform and silicon bulk.

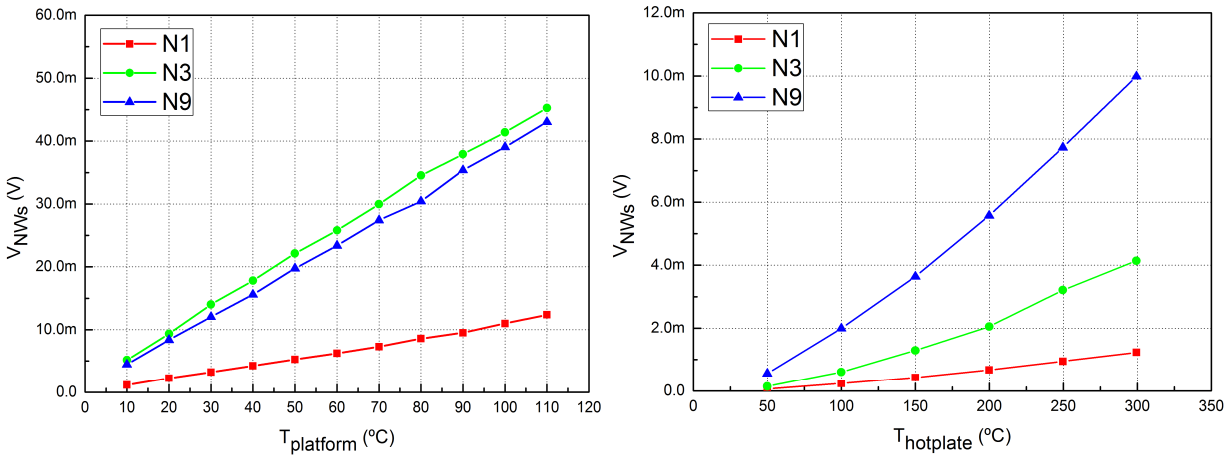

Figure 13: Seebeck voltage for N1, N3 and N9. Comparison between test mode (left) and harvesting mode (right). Test mode results are obtained before FIB while harvesting mode results are obtained after FIB.

In figure 13, we can see the Seebeck voltages obtained in harvesting mode or in test mode. It's worth mentioning that test mode measurements are taken with natural convection, while harvesting measurements are taken with forced convection. In the test mode, we generate the thermal gradient using the heater on the platform. Using the heater itself as a temperature sensor we can obtain the average platform temperature and plot the corresponding Seebeck voltage versus it. In harvesting mode, on the other hand, although the temperatures involved are much larger, the thermal gradients seen by the nanowires are lower. Comparing the Seebeck voltages obtained in each operation mode, we can estimate the thermal gradient seen by the nanowires in harvesting mode when the hotplate is at 300ºC. For example, if we look at the right

plot in figure 13, we can see that the Seebeck voltage for the N9 device in harvesting mode with the hotplate at 300ºC is 10mV. Then, we can find in the right plot of figure 13 that N9 device generates roughly 10mV when the platform is at 20ºC above ambient. Therefore, the thermal gradient seen by the silicon nanowires is the same in both cases, which means that setting the hotplate at 300ºC generates a thermal gradient on the nanowires of approximately 20ºC.

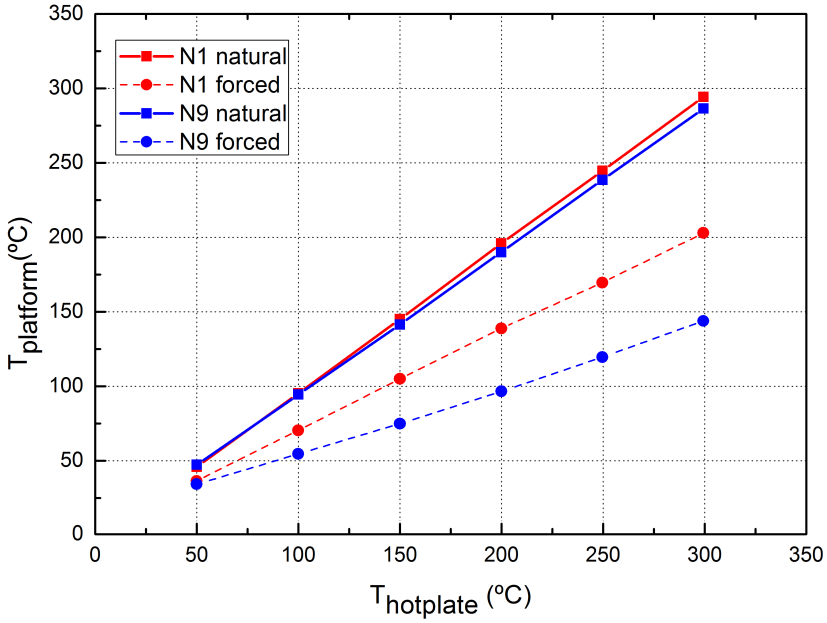

Figure 14: Comparison of platform temperature vs hotplate temperature for N1 and N9 devices, with natural convection and forced convection.

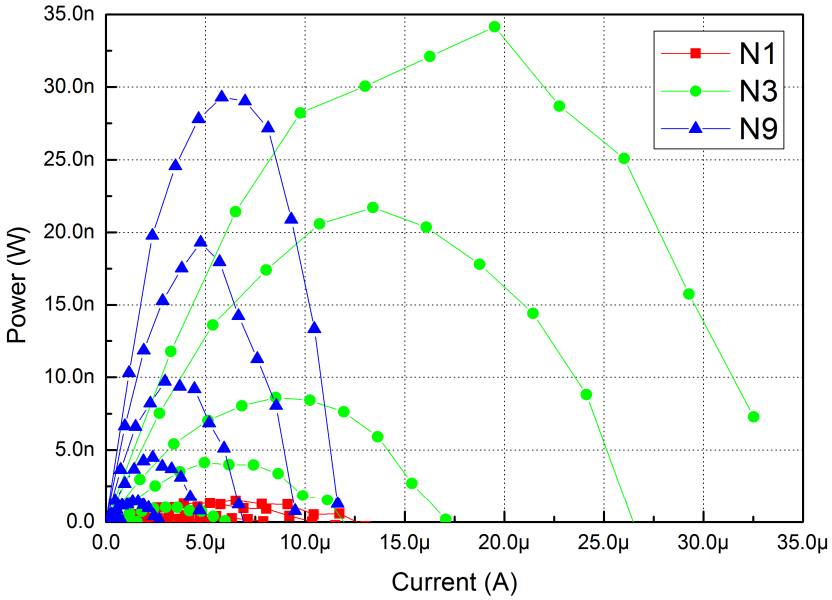

Figure 15: Power versus current plot for different devices (N1, N3 and N9) in harvesting mode and forced convection for different hotplate temperatures from 50ºC to 300ºC in 50ºC steps. The larger power corresponds to a hotplate temperature of 300ºC.

The effect of forced convection is shown in figure 14. The plot shows the platform temperature, measured through the heater resistance and its TCR, versus the hotplate temperature in harvesting mode. We are comparing the results for N1 and N9 devices with natural convection and forced convection. If the hotplate is at 300ºC the silicon bulk is at the same

temperature because silicon is a good thermal conductor. On the other hand, the silicon platform, which is designed to be thermally isolated from the silicon bulk, should be at a lower temperature. If we look at the solid lines in figure 15, which correspond to the natural convection cases, we can see that the platform temperature is slightly lower than the temperature of the hotplate. This means that the thermal gradient produced by natural convection is quite low. It can even be seen that N1 device has a lower thermal gradient than N9 device, which has a significantly better thermal isolation (larger effective silicon nanowire ensemble). But if we compare these results with the dashed lines, which correspond to a forced convection (described in the previous section), we can see that the thermal gradients obtained are much larger. Therefore the platforms have lower temperatures than the hotplate, especially for the N9 device which increases from a thermal gradient of roughly 10ºC in natural convection, to slightly more than 150ºC with forced convection. It is worth mentioning that, this thermal gradient is not the one seen by the nanowires. It is important to note that the temperature measured with the heater corresponds to an average temperature of the heater. Therefore, the thermal gradient seen by the nanowires will be smaller.

The power obtained from the micro thermoelectric generator, depends greatly on the internal resistance of the generator ($P=V^2/R$), which in our case corresponds to the nanowire resistance measured between the internal and external collectors. Therefore, if we look at figure 15, which plot the obtained power in harvesting mode with forced convection, we can see that N9 device does not scale properly when compared to N3 device. But if we look at table 1, we can see that the internal resistance of N9 is much larger than that of N3 or N1 devices. On the other hand we can see that the maximum power obtained for the current device being tested is approximately 35nW when the hotplate is at 300ºC.

On the other hand, in test mode (see figure 16), the maximum power output for N3 is 6.5µW, which corresponds to roughly a 200 fold increase from the harvesting mode. And it's worth mentioning that if N9 internal resistance were comparable to that of N1 or N3, the maximum power output would be even larger.

Moreover, these prototype devices can be connected in series or in parallel if we need larger voltages or current respectively. In addition, currently each chip measures 7x7mm^2 while the device itself only involves an area slightly larger than 1x1mm^2. Therefore, a higher integration can be achieved with the same design if needed. Additional improvements on this design imply the addition of a heat exchanger on the platform to enhance the heat transfer with ambient, and obtain larger thermal gradients in harvesting mode than the ones obtained with the current packaging so that they could come closer to the response obtained in test mode.

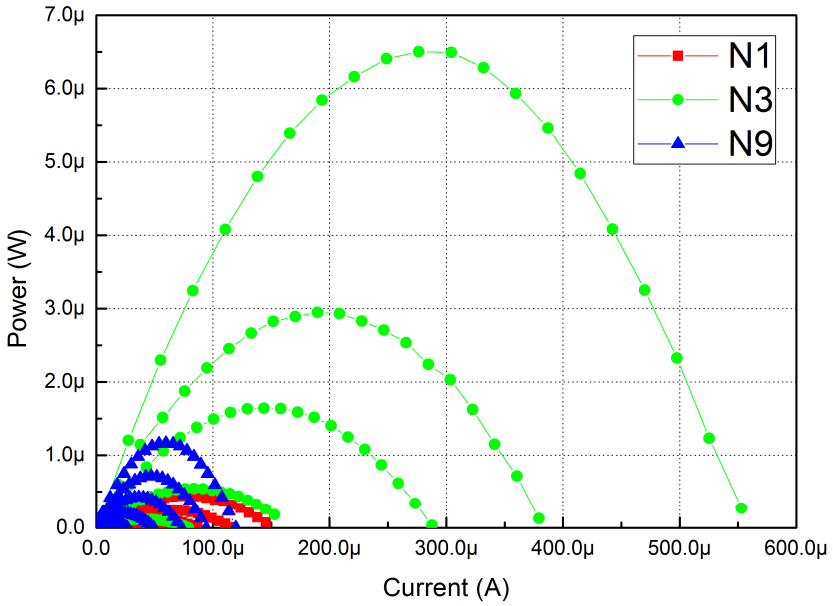

Figure 16: Power versus current plot for different devices (N1, N3 and N9) in test mode and natural convection for different platform temperatures from 20ºC to 100ºC with 20ºC steps. The larger power corresponds to a platform temperature of 100ºC.

ACKNOWLEDGEMENTS

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REFERENCES

[1] Snyder, G. J., [Thermoelectrics Handbook: Macro to Nano], CRC/Taylor&Francis, Boca Raton, (2005).
[2] Li, J., Liu, W., Zhao, L. and Zhou, M., "High-performance nanostructured thermoelectric materials." NPG Asia Materials 2, 152-158 (2010).
[3] Snyder, G. J. and Toberer, E. S., "Complex thermoelectric materials," Nature Materials 7(2), 105-114 (2008).
[4] Hicks, L. D., Dresselhaus, M. S., "Effect of quantum-well structures on the thermoelectric figure of merit," Phys. Rev. B 47(19), 12727 (1993).
[5] Hicks, L. D., Dresselhaus, M. S., "Thermoelectric figure of merit of a one-dimensional conductor," Phys. Rev. B 47(24), 16631 (1993).
[6] Boukai, A. I., Bunimovich, Y., Tahir-Kheli, J., Yu, J., Goddard, W. A. and Heath, J. R., "Silicon nanowires as efficient thermoelectric materials," Nature 451, 168-171 (2008).
[7] Hochbaum, A. I., Chen, R., Delgado, R. D., Liang, W., Garnett, E. C., Najarian, M., Majumdar, A. and Yang, P., "Enhanced thermoelectric performance of rough silicon nanowires," Nature 451, 163-167 (2008).
[8] Davila, D., Tarancón, A., Kendig, D., Fernández-Regúlez, M., Sabaté, N., Salleras, M., Calaza, C., Cané, C., Grácia, I., Figueras, E., Santander, J., San Paulo, A., Shakouri, A. and Fonseca, L., "Planar thermoelectric microgenerators based on silicon nanowires," Journal Eletron. Mater. 40(5), 851-855 (2011).
[9] Dávila, D., Tarancón, A., Fernández-Regúlez, M., Calaza, C., Salleras, M., San Paulo, A. and Fonseca, L., "Silicon nanowire arrays as thermoelectric material for a power microgenerator," Journal Micromech. Microeng., 21(10), 104007 (2011).
[10] Gadea, G., Morata, Á., Santos, J., Dávila, D., Calaza, C., Salleras, M., Fonseca, L., "Towards a full integration of vertically aligned silicon nanowires in MEMS using silane as a precursor," Nanotechnology, Accepted.