

High ferroelectric polarization in *c*-oriented BaTiO₃ epitaxial thin films on SrTiO₃/Si(001)

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The integration on silicon of epitaxial BaTiO₃ films, combining *c*-orientation, surface flatness and high ferroelectric polarization, is of main interest towards its use in memory devices. This combination of properties has been only achieved so far by using yttria-stabilized zirconia (YSZ) buffer layers. Here, the all-perovskite BaTiO₃/LaNiO₃/SrTiO₃ heterostructure is grown monolithically on Si(001). The BaTiO₃ films are epitaxial and *c*-oriented, and present low surface roughness and high remnant ferroelectric polarization around 6 μ C/cm². This result paves the way towards the fabrication of lead-free BaTiO₃ ferroelectric memories on silicon platforms.

Keywords: Ferroelectric films, Oxides on silicon, BaTiO₃

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BaTiO₃ (BTO), a ferroelectric oxide with high polarization, piezoelectric and electrooptic coefficients, is a major candidate for lead-free devices based on piezoelectric or ferroelectric thin films.¹⁻⁴ For example, *a*-oriented BTO on silicon has permitted integrating optical devices with improved properties respect the commonly used LiNbO₃.^{5,6} On the other hand, c-oriented BTO has been used to fabricate memory devices on silicon as ferroelectric tunnel junctions.^{7,8} In memory devices high switchable ferroelectric polarization along the outof-plane direction is desired. It requires *c*-orientation, which is challenging for BTO films on Si due to the thermal expansion mismatch between BTO and Si that causes in-plane tensile stress.^{9,10} Moreover, the growth of epitaxial BTO on Si(001) requires a buffer layer, being used either yttria-stabilized zirconia (YSZ) and/or LaNiO₃ (LNO),¹¹⁻¹⁵ or SrTiO₃ (STO).^{5-8,16-21} The YSZ buffer layer is combined with other layers to accommodate progressively the high lattice mismatch of around 9% with BTO. The high mismatch causes in-plane compressive epitaxial stress, favoring growth of *c*-oriented BTO with high ferroelectric polarization for a broad range of BTO thickness.¹³ In the case of the STO buffer layer, its lattice parameter is much closer to that of BTO permitting epitaxial growth without additional layers. The functional characterization of BTO film on STO/Si(001) has been usually based on piezoresponse force microscopy measurements,^{16,18,19,21} which is known that can not be taken as an unambiguously demonstration of ferroelectricity.²²⁻²⁴ Recently, the hysteretic dependence of the resistance with the writing voltage expected for a ferroelectric tunnel junction was observed for BTO tunnel junctions on La_{2/3}Sr_{1/3}MnO₃/STO/Si(001).⁸ However, the direct evidence of ferroelectricity in BTO films on STO/Si(001) remains pending. The absence of reported results contrasts with the ferroelectric loops with high remnant polarization reported for BTO integrated with Si(001) using buffer layer heterostructures based on YSZ.^{13,15} It suggests that the used buffer layer could be critical to compensate the stress due to the thermal expansion mismatch. The integration of coriented BTO on Si(001) in an all-perovskite oxides heterostructure could be challenging, thus limiting the progress towards the fabrication of Pb-free ferroelectric memories on silicon wafers. Thus it is of major relevance to determine the ferroelectric properties of high quality epitaxial BTO films on Si(001) buffered with STO.

Here, we report on the growth and properties of BTO films on Si(001) buffered with STO. High quality STO layers were deposited by molecular beam epitaxy (MBE) on Si(001),²⁵ and they were used to grow by pulsed laser deposition (PLD) bilayers with bottom conducting LNO and top ferroelectric BTO. Deposition conditions permitting to obtain high ferroelectric polarization of BTO when deposited on LNO/CeO₂/YSZ/Si(001) were used.¹³ We will show that BTO films on LNO/STO/Si(001) are *c*-oriented with expanded *c*-axis parameter, and present high ferroelectric polarization and low leakage. The results constitute a direct and

unambiguous prove of ferroelectricity of BTO integrated with Si(001) using STO as buffer layer.

Epitaxial STO buffer layers, 10 nm thick, were deposited by MBE on Si(001) wafers at a temperature of around 400 °C. The crystalline quality and morphology of the STO buffer layer were monitored during growth by using in-situ reflection high-energy electron diffraction (RHEED). Detailed growth conditions are presented in Supplementary Material. STO/Si(001) pieces were used as substrates to grow top-BTO/bottom-LNO by PLD in a single process. Thickness (t) was around 30 nm and 200 nm for LNO and BTO, respectively. Epitaxial relationships and out-of-plane lattice parameters were determined by X-ray diffraction (XRD) using CuK_{α} radiation. The surface morphology was studied by atomic force microscopy (AFM). The study of the microstructure was performed using an aberration corrected Nion UltraSTEM 200 microscope operating at 200 kV. Cross-section specimens were prepared using the standard mechanical polishing and ion-milling techniques. Platinum top contacts, 20 nm thick, were deposited by dc magnetron sputtering through stencil masks (squares around $60x60 \ \mu m^2$). Electrical measurements were performed at room temperature using a TFAnalyser2000 platform (aixACCT Systems GmbH) with a configuration of two BTO vertical capacitors in series, with the bottom LNO layer as a common electrode.²⁶ Polarization loops were obtained from current versus electric field measurements at 5 kHz using the dynamic hysteresis mode technique.²⁷ Leakage current at each voltage point was measured with an integration time of 3 s.

Figures 1a and 1b show RHEED patterns recorded *in situ* during the growth of the STO buffer layer. Figure 1a shows the 2x1 reconstructed Si(001) surface passivated by 1/2 monolayer of Sr, and the corresponding RHEED patterns taken at the end of the STO deposition along Si[1<u>1</u>0] and Si[100] are in Figure 1b. The patterns are streaky, signaling an atomically flat surface. The patterns indicate that STO has grown epitaxially with an in-plane rotation of 45° of the STO unit cell respect Si, as expected considering the lattice parameters ($a_{Si} = 5.431$ Å and $a_{STO} = 3.905$ Å). In agreement with the RHEED patterns, high resolution $\theta/2\theta$ XRD scans along symmetrical reflections show only (001) reflections from the substrate and the STO layer (Figure 1c). Laue fringes can be appreciated around the STO(002) reflection signaling high crystalline STO quality and sharp interfaces. The corresponding rocking curve around the STO(002) reflection (Figure 1d) presents a full width at half maximum of 0.54°. The surface morphology of the STO layers, measured by topographic AFM, was confirmed to be atomically flat on which surface atomic steps can be observed (Figure 1e), with rms roughness below 0.3 nm, and the height profile (Figure 1f) along the marked line shows height variations in a range of less than two unit cells of STO.

AFM topographic images of the BTO/LNO/STO/Si(001) sample, $5x5 \mu m^2$ and $1x1 \mu m^2$ in area, are presented in Figures 2a and 2b, respectively. The BTO films are flat in spite of its large thickness (200 nm), with a low surface roughness of around 0.7 nm. The XRD $\theta/2\theta$ scan along symmetrical reflections (Figure 2c) confirms the oriented crystalline growth of the BTO/LNO/STO trilayer on Si(001). The diffraction peaks correspond to (001) reflections of the silicon substrate and the STO, LNO and BTO layers. Diffraction peaks from other crystal orientations or other phases are not detected. A zoom of the scan around the (002) reflections of the layers is in Figure 2d. The STO(002) reflection at 2 θ around 46.5° is appreciated despite the low thickness of the buffer layer (10 nm). In the case of the electrode, the LNO(002) peak at 2θ = 47.82° indicates a compressed out-of-plane parameter of 3.804 Å, in agreement with the tensile epitaxial stress caused by the bottom STO layer. The BTO peak is of high intensity, and it is narrow and symmetric thus signaling uniform strain. It occurs at $2\theta = 44.65^{\circ}$, whereas the (002) reflection for bulk BTO is at higher angle (marked by the vertical line in Figure 2d. Thus the BTO film is c-oriented and presents an expanded out-of-plane lattice parameter of c = 4.059Å, which is similar to that of BTO films of comparable thickness on LNO/CeO₂/YSZ/Si(001).¹³ The rocking curve of the BTO(002) reflection (Figure 2e), with full width at high maximum of 0.84° , indicates low mosaicity considering that the substrate is silicon. Indeed, the rocking curve of the (002) reflection of the STO buffer layer (Figure 1d) is only slightly narrower (0.54°) .

Epitaxial growth of the BTO and LNO layers was confirmed by XRD ϕ -scans around asymmetrical reflections (Figure 3a). The ϕ -scans around LNO{101} and BTO{101} show four peaks, located at the same ϕ angles and 45° apart from the four Si{202} peaks. ϕ -scans around STO reflections are not presented due to the low thickness of the buffer layer. RHEED pattens (Figures 1a and 1b) indicated epitaxial growth with the STO unit cell rotated 45° in-plane respect the Si cell. Therefore, the epitaxial relationship of the heterostructure, sketched in Figure 3b, is [110]BTO(001) / [110]LNO(001) / [110]STO(001) // [100]Si(001).

The detailed microstructure of the multilayer was studied by means of scanning transmission electron microscopy (STEM), as shown in Figure 4. All STEM images were acquired using a high-angle annular detector. In this image mode the contrast ensues from a high angle scattering strength, giving rise to the so-called Z-contrast imaging (Z being the atomic number).²⁸ This allows for the easy identification of the BTO, LNO and STO layers in the low-magnification STEM image shown in Figure 4a. Concomitantly, in atomic resolution images the heavier atomic columns can be easily distinguished from lighter ones, as seen in the Z-contrast images of the interfaces, Figures 4b and 4c. These images confirm the high quality and the epitaxial relationship of the heterostructures, and reveal atomically flat interfaces between the BTO, LNO and STO layers, with absence of intermixing or nanoprecipitates. In fact, except for the amorphous SiO_x interfacial layer between Si and STO, which originates

during LNO and BTO deposition, all the interfaces show a coherent matching of the crystal lattices. In addition, a closer look to the LNO layer reveals the presence of vertically and horizontally antiphase boundaries (marked with yellow arrows in the image), in which a Ni-O plane is missing. Regarding the BTO layer, a detailed analysis of the in-plane and out-of-plane spacing using Fourier Transform (not shown here) reasserts the tetragonality and the *c*-axis orientation of the BTO layer.

Figure 5a shows a set of polarization loops measured with increasing maximum applied electric field. Minor loops are obtained at low maximum applied fields, whereas the loops are saturated from maximum fields of around 500 kV/cm. The corresponding current-field curves (see an example in the inset of Figure 5a) display clear switching peaks. The remnant polarization is around 6 μ C/cm². The ferroelectric polarization, and the coercive field of around 60 kV/cm, are similar to the values of BTO films of equivalent thickness deposited on LNO/CeO₂/YSZ/Si(001) using same growth conditions.¹³ Besides, the leakage curve (Figure 5b) indicates that BTO on STO/Si(001) presents a low leakage (around 10⁻⁵ A/cm² at 50 kV/cm), again similar to equivalent films on YSZ-based buffer layers.

In conclusion, the ferroelectricity of BTO films integrated on STO buffered Si(001) has been confirmed by the measurement of polarization loops. The films present *c*-orientation with similar strain and ferroelectric properties that state of the art BTO films on $LNO/CeO_2/YSZ/Si(001)$. Thus the BTO properties are mainly dictated by the deposition conditions of BTO, being similar the eventual role of the buffer layer on the reduction of the tensile stress due to the thermal expansion mismatch between BTO and Si. This is an important step towards the desired integration of *c*-oriented BTO on silicon using materials and processing conditions compatible with CMOS technology. A similar demonstration of ferroelectricity in BTO films deposited on Si(001) by techniques as atomic layer deposition or MBE at reduced growth temperature would pave the way towards its use in memory devices.

Supplementary Material

See Supplementary Material for detailed growth conditions of the SrTiO₃ buffer layers.

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FIG. 1. RHEED patterns after passivation of the Si(001) surface with 1/2 monolayers of Sr (a) and at the end of the STO deposition (b). (c) High resolution XRD $\theta/2\theta$ scan of the STO/Si(001) sample and (d) rocking curve around the STO(002) reflection. (e) 1x1 μ m² AFM topographic image of the STO buffer layer. The image in the inset corresponds to a 5x5 μ m² scanned region. (f) Height profile along the line marked in (e).



FIG. 2. AFM topographic images corresponding to scanned areas of (a) $5x5 \ \mu\text{m}^2$ and (b) $1x1 \ \mu\text{m}^2$. (c) XRD $\theta/2\theta$ scan along symmetrical reflections and (d) zoomed region. The vertical dotted lines mark the (001) reflections for bulk BTO. (e) Rocking curve around the BTO(002) reflection.



FIG. 3. (a) XRD ϕ -scans around BTO{101}, LNO{101}, and Si{202} reflections (b) Sketch of the heterostructure illustrating the epitaxial relationships.



FIG. 4. (a) Low magnification Z-contrast image of the BTO/LNO/STO/Si multilayer along the Si[110] zone axis. The horizontal contrast variation observed in the BTO layer is an artifact stemming from the interaction of the atom-size scanning probe and the crystal lattice spacing. (b) High-resolution Z-contrast image of the STO/Si, and LNO/STO interfaces. While there is a sharp interface between LNO and STO, there is an amorphous SiO_x interfacial layer between STO and the Si substrate. The yellow arrows in the LNO layer mark the position of two antiphase boundaries. (c) High-resolution Z-contrast image of the LNO/STO interface.



FIG. 5. (a) Ferroelectric polarization loops measured with increasing maximum applied electric field. The ferroelectric loops were obtained from current versus electric field measurements (an example is in the inset). (b) Leakage current versus voltage.

