Bidirectional DC-DC Converter for Aircraft Electric Energy Storage Systems

A THESIS SUBMITTED TO THE UNIVERSITY OF MANCHESTER
FOR THE DEGREE OF DOCTOR OF PHILOSOPHY
IN THE FACULTY OF ENGINEERING AND PHYSICAL SCIENCES

2010

By

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School of Electrical and Electronic Engineering

Contents

Word Count – 65,065

List of Tables

List of Figures

List of Symbols

C_d	Damping capacitor
$C_{S\text{-}HV}$	HV side snubber capacitor
$C_{S\text{-}LV}$	LV side snubber capacitor
C_S	Snubber capacitor
d	Duty ratio
di/dt	Rate of change of IGBT current during switching transient
dV	Total change in ultracapacitor voltage
dv/dt	Rate of change of IGBT voltage during switching transient
δ	Dead-time
δ_i	Dead-time introduced on the primary
δ_0	Dead-time introduced on the secondary
EC_S	Energy delivered to the snubber capacitor
E_{OFF}	Turn-off energy loss of IGBT
E_{ON}	Turn-on energy loss of IGBT
f_s	Switching frequency
i_{A1}	Current flow through the transistor A_1
$i_{AD1\text{-}A1}$	Current flow through the anti-parallel diode A_{D1} and transistor A_1 pair
i_{AD1}	Current flow through the anti-parallel diode A_{D1}
i_{avg}	Average ultracapacitor current
i_{C1}	Current flow through the transistor C_1
$i_{CD1\text{-}C1}$	Current flow through the anti-parallel diode C_{D1} and transistor C_1 pair
i_{CD1}	Current flow through the anti-parallel diode C_{D1}
I_{CRMS}	Filter capacitor RMS current
I_D	Diode current
I_{inavg}	Input side average current
i_{in}	HV side terminal current
I_{inRMS}	Input side RMS current
i_L	Current flow through the coupling inductor
I_{Lrms}	RMS current of the inductor

$I_{L1,}$ $I_{L2,}$ $I_{L3,}$ I_{L4}	Successive peaks of the inductor current
i_{max}	Maximum ultracapacitor current
i_{min}	Minimum ultracapacitor current
$I_{(n)}$	nth sample of inductor current
$I_{(n-1)}$	(n-1)th sample of inductor current
$I_{(n+1)}$	(n+1)th sample of inductor current
i_0	LV side terminal current
I_0	Average output current
$I_0^{'}$	Normalised average output current
I_{OFF}	Turn-off current of transistor
I_P	Peak inductor current
I_{PP}	Peak-to-peak inductor current
I_{ref}	Reference current
I_T	Transistor current
l	Length of air core coil
$L/L_{coupling}$	Coupling inductance
L'	Primary referred coupling inductance
N	Number of turns
n	Transformer turns ratio
P_C	Total conductor loss
P_{CondD}	Conduction loss of diode
P_{CondT}	Conduction loss of transistor
P_{in}	Input power
P_0	Output power
P_{OFF}	Turn-off power loss of IGBT
P_{ON}	Turn-on power loss of IGBT
P_{SW}	Total switching power loss
P_T	Total power loss
Φ	Phase shift between the AC link voltage and current
R	Load resistance
r	Radius of air core coil

r_{CE}	On-state slope resistance of IGBT
R_d	Damping resistor
R_G	Gate resistance of IGBT
$R_{th(c-s)}$	Case to sink temperature
$R_{th(j-c)}$	Junction to case temperature
$R_{th(s-a)}$	Sink to ambient temperature
S_{A1}	Gate drive signal of transistor A_1
S_{A2}	Gate drive signal of transistor A_2
S_{B1}	Gate drive signal of transistor B_1
S_{B2}	Gate drive signal of transistor B_2
S_{C1}	Gate drive signal of transistor C_1
S_{C2}	Gate drive signal of transistor C_2
S_{D1}	Gate drive signal of transistor D_1
S_{D2}	Gate drive signal of transistor D_2
T_a	Ambient temperature
t_B	time taken for i_L to fall to zero after HV/LV switching instant
T_{case}	Case temperature of IGBT module
t_f	Fall-time of transistor current
T_{jDiode}	Junction temperature of diode
T_{jIGBT}	Junction temperature of IGBT
t_r	Rise-time of transistor current
T_S	Switching period for a cycle
T_s	Heat sink temperature
Δt	sampling interval
θ	corresponding angle marked in i_L current waveform
V_{CE}	Collector to emitter voltage of IGBT
V_{CEO}	On-state threshold voltage of IGBT
$V_{CE(sat)}$	On-state voltage drop of IGBT
V_F	Forward voltage drop of diode
V_{HV}	Square-wave voltage generated by HV bridge
V_{in}	Aircraft DC bus voltage

V_L	Voltage across the coupling inductor
V_{Lrms}	RMS voltage of the inductor
V_{LV}	Square-wave voltage generated by LV bridge
V_{min}	Minimum voltage of ultracapacitor
V_0	Ultracapacitor voltage
$V_0^{'}$	Normalised ultracapacitor/output voltage
V_P	Primary referred transformer voltage
V_S	Voltage across the transformer secondary
V_W	Working voltage of the ultracapacitor
ω	Resonant frequency of snubber capacitor and inductor circuit
Z	Impedance of snubber capacitor and inductor circuit

List of Abbreviations

A/D	Analog to Digital
ADC	Analog to Digital Converter
ASIC	Application-Specific Integrated Circuit
CCS	Code Composer Studio
CMC	Common Mode Choke
DAB	Dual Active Bridge
D/A	Digital to Analog
DCM	Discontinuous Current Mode
DSP	Digital Signal Processor
EMC	Electromagnetic Compatibility
ESR	Equivalent Series Resistance
ESL	Equivalent Series Inductance
EVA	Event Manager A
EVB	Event Manager B
FBW	Fly-By-Wire
GHG	Green House Gas
HBCS	Half-Bridge Current Source
HV	High Voltage
IDE	Integrated Development Environment
IEPNEF	Intelligent Electrical Power Networks Evaluation Facility
IGBT	Insulated Gate Bipolar Transistor
LV	Low Voltage
MEA	More Electric Aircraft
MOSFET	Metal Oxide Field Effect Transistor
PBW	Power-By-Wire
PI	Proportional plus Integral
PPS	Phase shift plus Pulse width modulation
PWM	Pulse Width Modulation
RAT	Ram Air Turbine

SOA	Safe Operating Area
TAB	Triple Active Bridge
TI	Texas Instruments
UAV	Unmanned Aerial Vehicle
UTC	University Technology Centre
ZCS	Zero-Current Switching
ZVS	Zero-Voltage Switching
ZVZCS	Zero-Voltage and Zero-Current Switching

Abstract

Future aircraft are likely to employ electrically powered actuators for adjusting flight control surfaces, and other high power transient loads. To meet the peak power demands of aircraft electric loads and to absorb regenerated power, an ultracapacitor-based energy storage system is examined in which a bidirectional dual active bridge DC-DC converter is used. This Thesis deals with the analysis, design, development and performance evaluation of the dual active bridge (DAB) converter, which can act as an interface between the ultracapacitor energy storage bank and the aircraft electrical power network.

A steady-state analysis is performed for the DAB converter producing equations for the device RMS and average currents and the peak and RMS currents in the coupling inductor. This analysis focuses on understanding converter current shapes and identifying the zero-voltage switching (ZVS) boundary condition. A converter prototype was designed and built and its operation verified through SABER simulations confirming the accuracy of the analysis. Experimental results are included to support the analysis for 7kW, 20 kHz operating conditions giving a measured efficiency of 90%.

To enhance the performance of the converter under light-loads, a quasi-square-wave mode of operation is proposed in which a dead-time is introduced either on the transformer primary voltage, or on the transformer secondary voltage, or simultaneously on both transformer primary and secondary. A similar detailed analysis as that for square-wave operation has been undertaken for all three cases and the converter performance was analysed focusing on ZVS operating range, impact of the RMS/peak inductor currents and converter efficiency. The theoretical work was validated through SABER simulations and proof of concept experimental measurements at 1kW, 20 kHz, which resulted in converter efficiency well above 91%. A 9%-17% improvement in efficiency and a 12%-17% improvement in ZVS operating range over square-wave operation are observed for similar operating conditions.

Furthermore, a novel bidirectional current control technique for the DAB converter is presented. A SABER simulation has been performed and the converter operation is validated for square-wave and quasi-square-wave modes under steady-state and transient conditions.

Declaration

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Dedicated to my dearest parents

Mr. N.S.R. Samy & Mrs. RM. Lakshmi

Acknowledgements

"Ya Devi Survabhudeshu Shaktirupena Samshita; Namastasyai Namastasyai Namastasyai Namonamah!; Ya Devi Survabhudeshu Bhddhirupena Samshita; Namastasyai Namastasyai Namastasyai Namonamah!; Ya Devi Survabhudeshu Smritirupena Samshita; Namastasyai Namastasyai Namastasyai Namonamah!" *- Devi Mahatmyam*

I Thank Goddess "The Divine Mother of the Universe" for blessing me to achieve success in various stages in my life with good health, education, confidence, enthusiasm & perseverance.

I express my gratitude to my supervisors Prof. Andrew J. Forsyth and Dr. Roger Shuttleworth for their valuable suggestions, support and encouragement during my PhD. I am grateful to Prof. Andrew for his valuable comments on my conference paper. I am indebted to Dr. Roger for his help, valuable comments and support especially during my Thesis revisions.

I thank my sponsors Rolls-Royce plc and EPSRC, UK for their financial support through the DHPA for my PhD programme. I thank the University of Manchester for the opportunity to pursue my PhD study.

I thank Dr. Nigel Schofield for providing me an opportunity to attend the TMS320C2000 DSP Workshop at Texas Instruments, Northampton. I thank Dr. Ian Hawkins for proof reading my Thesis and for his inputs in the driver circuit design. I thank the staff and students of the Power Conversion Group for their support during my PhD. I also thank Mr. Robert Stephens for his appreciation and encouragement during my experimental work.

I thank all the staff members of the Mechanical and Electronic workshop, especially Mr. Vincent James for his help at the initial stages.

I thank Ms. Patricia Campbell for her compassion, general advice and encouragement during my study.

I thank my dearest parents whose sacrifice, love, care and great concern, prayers, continuous encouragement and support have been invaluable and have brought me thus far. I thank my better half for his care, concern, understanding and encouragement. I thank my brothers Mr. R. Abiraman and Mr. R. Bhaarathi and my sister Ms. R. Kayathri for their encouragement and affection.

Publications

- R.T. Naayagi, A.J. Forsyth, "Bidirectional DC-DC Converter for Aircraft Electric Energy Storage Systems," *Proceedings of the 5th IET Power Electronics, Machines and Drives Conference (PEMD)*, pp. 1-6, 2010, Brighton, UK.

- R.T. Naayagi, A. J. Forsyth, R. Shuttleworth, "Analysis of Quasi-Square-Wave Operation of the Dual Active Bridge DC-DC Converter", *Under preparation for submission for review to IEEE Transactions on Power Electronics.*

- R.T. Naayagi, A. J. Forsyth, R. Shuttleworth, "Simulation study of a novel bidirectional control of Dual Active Bridge DC-DC Converter", *Under preparation for submission for review to IET Power Electronics.*

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Thaiyal Naayagi Ramasamy completed her Bachelor's degree in Electrical and Electronics Engineering from *Bharathidasan University, India* by securing University I Rank. She was honoured with a Gold Medal by the Governor of Tamilnadu state in 2001. She was conferred the *T.R. Rajagopalan Award* for being the Best Outgoing Female Graduate of her batch (1996-2000). She worked in academia for few years. She gained interest in Power Electronics and pursued her Master's degree in Power Electronics and Drives at *Anna University, India* from 2003-2005. She secured the University II Rank in her Master's degree programme. She also received the Outstanding Master's Student Award in 2005 from her institution. Meanwhile, she also completed her M.Sc in Information Technology from *Alagappa University, India* in part-time. She has received several scholarships and merit certificates for her outstanding academic performance. She decided to do her PhD abroad to specialise in the area of Power Electronics and also to gain international exposure and practical expertise. In 2006, she secured the *Rolls-Royce badged Dorothy Hodgkin Postgraduate Award* from the School of Electrical and Electronic Engineering of *The University of Manchester, UK* to pursue her PhD programme. Her research interests are in power electronic circuits and systems for aerospace and electric vehicle applications.

Chapter 1

Introduction

Global climate change may be one of the greatest challenges faced by the world today. To reduce its impact on mankind, governments are encouraging technological innovation towards reducing heat-trapping gases and preventing further deterioration of the environment and safeguarding the health and well being of current and future. Transport contributes a significant proportion of green house gas emissions responsible for global climatic change [1]. According to the UK department of transport statistics, the level of green house gas (GHG) emissions from UK transport industries was 47% higher in 2002 than 1990. Between 1990 and 2002, GHG emissions from the UK air transport industry rose from 20.2 million tonnes to 37.5 million tonnes and contributed to 85% of increase in UK air transport emissions [1, 2]. Currently, air transport is the main focus of attention with respect to reducing future gas emissions in the transport sector. This creates the necessity for environmentally-friendly flights to facilitate local and global transport. To address this issue, several initiatives are being taken by the aircraft industry, to promote the use of electrical power to drive most of the aircraft systems and subsystems that were previously driven by hydraulic, pneumatic and mechanical systems. A study completed by NASA demonstrated that using more electrical technologies for a typical 200 seat aircraft could result in a 10% reduction in aircraft empty weight, a 13% reduction in required engine thrust and a 9% reduction in aircraft fuel burn; these are significant improvements both economically and environmentally [3]. The development of aircraft designs with improved environmental performance e.g. reduced noise, emissions and fuel burn, to make more efficient and environmentally-friendly aircraft is the motivation underlying the concept of More Electric Aircraft (MEA).

1.1 Background – More Electric Aircraft

In the 1980's, the first commercial aeroplane "Fly-By-Wire" (FBW) system was introduced by Airbus in the A320 series, shortly followed by Boeing with its B777 model. In the FBW system, electrical control systems incorporating computers are used for controlling flight control surface actuators (aileron, elevator, rudder and spoiler). These surfaces were previously manually controlled using mechanical and hydro-mechanical control systems.

FBW technology reduces aeroplane weight and improves reliability while the use of computers makes control easier and safer [4-5]. In those first FBW systems the control surface actuators were powered hydraulically and in conventional aircraft, electrical systems were mainly used for avionics, powering energy storage systems and auxiliary loads. These electrical systems typically used 115V, 400Hz AC for high power loads and 28V DC for avionics and battery driven vital services [6]. Essential systems such as flight control actuation, landing gear, wing anti-icing protection and engine starter/generator were driven by a combination of hydraulic, pneumatic and mechanical systems. These systems tended to be heavy, inefficient and require frequent maintenance. To overcome these drawbacks, initiatives were taken to develop aircraft electrical power systems and power electronic components to enhance reliability, fault tolerance, power density and performance. The resulting new system topologies form the basis for the More Electric Aircraft [7-12]. Key benefits of employing more electrical systems are reduced operating cost, lower fuel burn and less environmental impact.

In the late 1990's, "Power-By-Wire" (PBW) technology was introduced to revolutionise FBW technology. In this technology, bulky and heavy hydraulic circuits are eliminated and replaced by electrical equivalents in addition to retaining all the benefits of digital FBW technology [13]. Replacement of existing systems with electrical equivalents will significantly increase the electric power requirements [14]. This is providing a spur for advances in power electronics, fault tolerant power distribution systems and electrically driven actuators. Variable frequency generation is reported to be the key for higher output power management [15], as it can increase power generation without significantly increasing weight. The power generation capacity of the more electric Boeing B787 and Airbus A380 aeroplanes is about 1.4MW and 850kW respectively [16]. In order to reduce weight, electrical power should be transmitted around the aircraft at a high voltage resulting in low current and low conduction losses. An investigation [17] showed that a ±270V DC power distribution system architecture is the most reliable configuration for sustaining operation even under severe supply transients. This is because large DC link capacitors would aid in maintaining the system voltage during transients. Moreover, AC systems require larger cables than DC systems because of reactive power flows, and at high frequencies the problem of skin effect

occurs. Therefore, the generation and distribution voltage in these advanced aircraft is mainly ±270V DC with 230V variable frequency AC and 28V DC distribution for low power loads [18-21]. Hence, the electric source not only supplies the energy storage system, avionics and auxiliary loads, but also the actuators for flight control surface, landing gear, de-icing systems and the engines' starter/generator [22, 23].

Four core areas have been identified as necessary developments in order to push forward the MEA initiative [24]. These areas are internal engine starter/generator, primary flight control actuation, integrated (auxiliary and emergency) power unit, and a fault tolerant power management, distribution and motor drive system [25]. The use of an embedded generator as a motor provides the benefit of being able to start the engine electrically allowing the removal of a conventional air starter. Variable frequency AC systems with simpler and lighter generators are now being considered by the industry [26] to replace integrated drive generators, which need complex hydraulic systems to generate constant frequency AC voltage from variable speed engine shaft power inputs [27-28]. This enables the direct coupling of generators to engine shafts and eliminates gearboxes and associated drive shafts, lubrication systems, hydraulic systems and pneumatic engine starting systems.

Subsequently, electro hydraulic and electromechanical actuators were developed to replace traditional hydraulic actuators. The major advantages of electrical actuation include increased reliability, elimination of the central hydraulic system and reduced maintenance [29-33]. New flight control subsystem packages include a power-on-demand electrical system and electric actuation of flight control surfaces (rather than the traditional, large, heavy and difficult-to-maintain hydraulic actuation). However, the actuator's power profile is highly dynamic – this could lead to over sizing of the generators and may raise power quality issues [34]. Presently, batteries are used to maintain the system voltage during transients and to supply power for short-term heavy loads. Environmentally friendly energy storage technologies are required to meet the demands in MEA designs. Another important issue surrounding power generation involves the ability to generate aircraft power during emergency situations. Fan-driven generators could be used to replace conventional ram air turbine (RAT) designs [35]. In the event of engine shutdown, the windmilling of the main

engine fan drives the LP shaft, and is sufficient for the generator to provide emergency power. In addition to providing adequate emergency power, the new design gives the generator the capability of supplementing the main generating system by operating as a main generator over the whole engine speed range. This capability creates the opportunity to reduce the size and weight of the other main generators [36-37].

Next, the need for power electronic energy conditioning systems in the MEA has been identified. Power electronic systems are needed to interface the generator and the distribution bus in order to combine power from multiple generators operating at different frequency and voltage levels [38]. The other essential tasks are controlling bidirectional power flow to allow engine start, regulating the distribution bus voltage in response to load changes and ensuring efficient operation of the power system over a wide speed and power flow range within an aircraft [39-40]. In addition to satisfying these requirements, power electronic devices must be small and light weight [41-42]. Power electronic converters constitute the heart of motor drives, which are essential for electro mechanical/electro hydraulic actuators [43-44]. Therefore, there is a continuous demand for high performance and efficient power electronic converters to meet today's challenges in MEA designs.

1.2 Motivation

More electric technology revolution in aerospace applications has put forward several challenges to design engineers to ensure that aircraft systems and subsystems are ultra reliable, compact, easy to maintain, low cost and of high performance. To ensure high availability of electric power in aircraft, the power network architecture should allow for potential redundancy of the power supply [45]. The generation and distribution architecture must be flexible so that power backup can occur. These needs create a significant demand for light weight and highly efficient power electronics for conversion and control of power. Hence, research in this area is vital.

1.2.1 Intelligent Electrical Power Networks Evaluation Facility (IEPNEF)

A 100kVA aircraft electrical power system rig has been installed in the Intelligent Electrical Power Networks Evaluation Facility (IEPNEF) at the Manchester University Technology Centre (UTC) with support from Rolls-Royce plc, with the aim of devising and developing more electric technologies for future aircraft and land-based vehicles. This facility is to be used to investigate flexible, reconfigurable and fault tolerant intelligent electric power networks for an Unmanned Aerial Vehicle (UAV). The electrical power system in the facility has a 30kW switched reluctance generator and a 70kW permanent magnet brushless AC generator, separately driven by motor drives, which emulate the high and low pressure shafts of a gas turbine engine. The electrical power is distributed around a ± 270V DC bus, to various power electronic load emulators, which imitate the behaviour of real aircraft loads such as actuators, environmental control systems, fuel and oil pumps, and avionics.

The facility has high power resistive load banks, unidirectional active programmable load banks and bidirectional active programmable load banks. The bidirectional active load bank is used to address energy management issues associated with the power regeneration capability of real-time loads such as flight control surface actuators. Electrically powered actuators draw transient power for a brief period of time. Design of generators to provide such dynamic power will increase the system weight and cost. Moreover, peak power demands from the electrical network must be maintained at an absolute minimum for safety reasons. Energy storage systems can provide a wide array of solutions to such key issues by providing clean and stable power in an affordable manner so as to improve power quality and electric power system stability.

Performance benefits of the latest energy storage devices are described in [46] and comparison of the various characteristics of different static energy storage devices is presented in [47]. For aircraft applications, weight is the primary concern with no sacrifice of performance. Lithium-ion batteries and bipolar metal hydride batteries are proposed in [48-52] for aerospace applications. Though aircraft battery technology has made significant advances in the recent past, batteries still suffer from low reliability, limited power density and necessitate maintenance. Environmentally-friendly ultracapacitors have much higher specific

power, higher charge/discharge efficiency and a long life cycle, despite their lower energy density [53-54]. Recent literatures point to the utility of ultracapacitor based energy storage system in automotives [55], large vehicle propulsion [56], and transportation networks [57]. Ultracapacitors are designed to meet pulsed power demands. Ultracapacitors exhibit a response time (half a second is the response time of a typical 125V ultracapacitor module from Maxwell Technologies), which cannot be achieved practically with any other energy storage system [58]. The problem is not regarding how much energy can be stored, but how fast it can be delivered. Ultracapacitors are a new energy storage technology, ideally suited for applications requiring repeated bursts of power for fractions of a second to several minutes. The ultracapacitor also has an operating temperature range between -40ºC and +65ºC and is also shock and vibration resistant [59]. With these attributes, the ultracapacitor can find use as a highly effective energy storage device. Hence, an investigation into ultracapacitor based energy management, for the dynamic power demands of bidirectional real-time aircraft loads, tested on the aircraft power system in IEPNEF would be a useful new area of research. This facility serves as the main motivation, which offers opportunities for researchers to devise, examine, explore and validate design ideas from paper to platform.

1.3 Review of DC-DC converter topologies

Though the conventional aircraft is primarily AC based in concept, DC is required to power avionics and battery systems. Modern aircraft use more open electrical technologies that employ DC as well as AC power systems. Therefore, DC-DC power conversion is often required to meet the necessary voltage level of various loads in an aircraft. Isolated DC-DC converters are required for sensitive and safety-critical avionics loads since galvanic isolation helps to reduce the supply noise by providing a floating ground on the secondary side of the converter. Moreover, the main purpose of isolation is to protect personnel from exposure to dangerous voltage levels. Non-isolated converters are generally used where voltage needs to be stepped-up or stepped-down in relatively low power applications. Several configurations have been introduced in recent years to realise DC-DC power conversion.

Unidirectional converters typically include buck, boost, forward, push-pull and half bridge converters and cater to various onboard loads such as sensors, controls, entertainment,

utility and safety equipments. For safety reasons, in order to provide DC isolation, isolation of non-linear loads and also to isolate supply noise, both unidirectional and bidirectional DC-DC converters should incorporate isolation. However, there is an increased need for a bidirectional DC-DC power converter with galvanic isolation due to the provision of electrical energy storage. In order to reduce the number of power electronic components, charging and discharging capability should be implemented within the same circuit topology. In the following sections, prior work in the area of bidirectional DC-DC converters is reviewed and various topologies are compared. A suitable topology for a high power bidirectional DC-DC converter for energy storage systems is then identified.

1.3.1 Low power bidirectional converter topologies

A bidirectional DC-DC converter topology for low power applications is proposed in [60]. The power circuit topology is shown in Figure 1.1 and is a combination of half bridge and current fed push-pull topologies. During forward/charging mode energy from DC mains charges the battery, switches S_1 and S_2 are gated and the body diodes of S_3 and S_4 provide battery side rectification. In the backup/current-fed mode, reversal of power flow occurs and the switches S_3 and S_4 are gated and the body diodes of the switches S_1 and S_2 provide load side rectification. In order to enable simultaneous and equal charging of capacitors C_1 and C_2, the balancing winding N_{P1} and the diodes D_1 and D_2 were used. The circuit has the following advantages: low stresses on the transistors, galvanic isolation, a low number of devices and low current ripple. However if the converter starts operating in the backup mode when the hold-up capacitors C_1 and C_2 are not charged, the duty cycle of S_3 and S_4 is increased to build up the load (dc bus) voltage. Therefore current in the inductor continues to rise with the switches operating at maximum duty cycle. This continuous increase of inductor (L_0) current results in a switch current that exceeds the rated value and can damage the switch. To avoid this, a parallel combination of a relay and a resistor is necessary. The series resistor limits the previously increasing inductor current. Once the output capacitors are charged, the resistor is bypassed by the relay. Moreover, diodes D_1 and D_2 reverse recovery results in current spikes on the transformer primary during forward and backup modes.

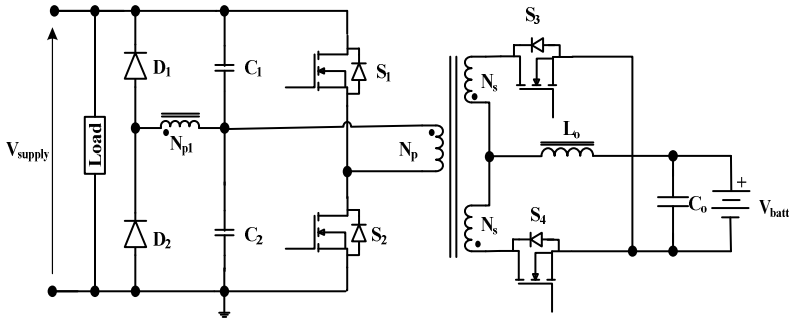


Figure 1.1 Low power bidirectional DC-DC converter, [60]

Another low cost, low power versatile bidirectional DC-DC converter for a battery charger application was proposed in [61]. The synchronously rectified current fed push-pull topology has a low number of switches and magnetic components, as shown in Figure 1.2. The center-tap on the transformer introduces difficulties in design as the primary and secondary windings must be tightly coupled in order to avoid voltage spikes when each transistor is turning-off. Soft switching techniques such as Zero Current Switching (ZCS – turn-on/off of the devices at zero current) may be integrated into the operation if the active devices of the converter work as rectifiers, by sensing the current flow through the devices and timing the driving of the MOSFETs so that they function as zero current switches. This work is representative of an initial effort in the general direction of DSP based bidirectional DC-DC converters.

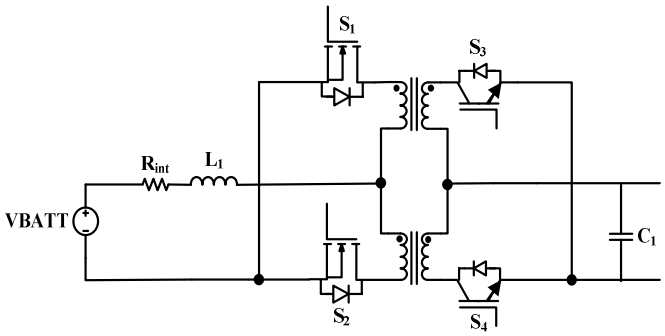
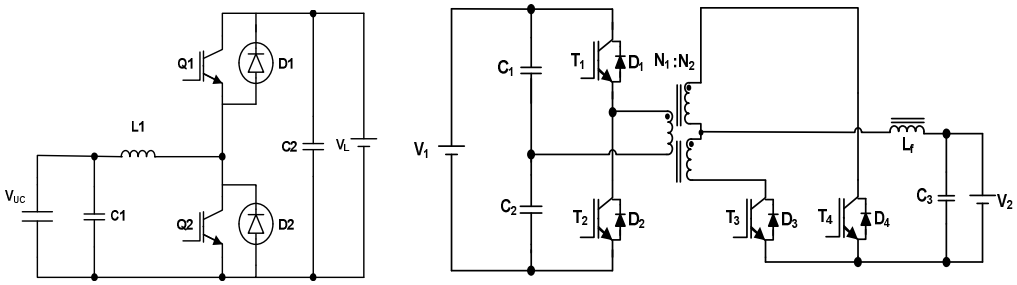


Figure 1.2 Synchronously rectified current fed bidirectional DC-DC converter, [61]

A non-isolated bidirectional converter topology uses only two devices to achieve bidirectional operation [62], as shown in Figure 1.3(a). Owing to its simplicity, it is preferred for electric vehicle applications [63]. Three such stages have been combined in one circuit to

form a multi-input dc-dc converter [64]. The converter is used to combine battery and ultracapacitor energy storage with the electric generator to improve system dynamic performance. The same converter topology has been used as an active damping device [65] across a constant power load in a distributed DC power system to prevent instability. Although the topology is very simple and effective, it requires a large inductor to limit the input ripple current, and high current capacitors to filter the output current. Also, it possesses limited power handling capability and has a low voltage conversion ratio due to its non-isolated structure. Based on comparative studies [66], new configurations were investigated in [67]. In order to achieve a higher voltage conversion ratio between the supercapacitor and the DC link, a Half Bridge Current Source (HBCS) converter shown in Figure 1.3(b) was proposed in [68].



(a) (b)

Figure 1.3 (a) Non-isolated bidirectional converter [62] (b) HBCS converter [68]

In [69-70], Mishima and Hiraki presented a new bidirectional dc-dc converter topology for dual voltage power systems, in which ultra low voltage operation of a supercapacitor is made possible by transformer isolation. A MOSFET full bridge topology was used on the high voltage side, and a current fed, push-pull topology was used on the low voltage side, as depicted in Figure 1.4. Despite synchronous rectification, to reduce the overall power loss, a soft-switching technique is essential, which increases the converter complexity.

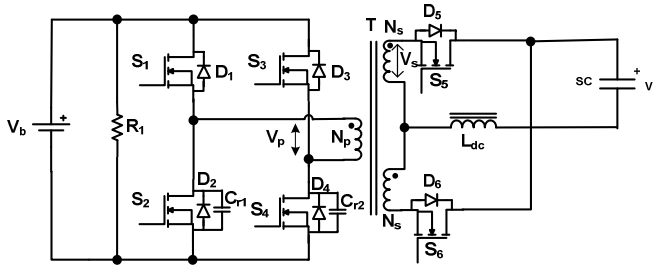
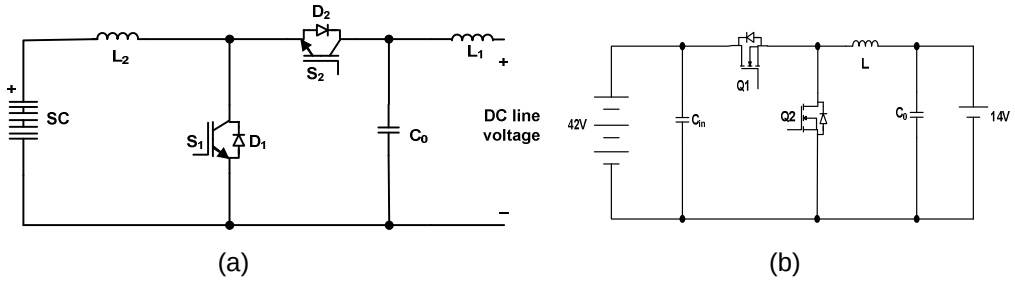


Figure 1.4 Full bridge/push-pull based bidirectional DC-DC converter [70]

To absorb regenerative energy and to improve system efficiency in an electric railway system, a single stage bidirectional DC-DC converter as shown in Figure 1.5(a) has been proposed [71]. However an initial charging circuit is necessary for the supercapacitor to raise the voltage at the time of starting the motors. Also, excessive regenerative energy, beyond the capacity of the supercapacitors used, had to be dissipated as heat using additional resistors. A bidirectional dc-dc converter was proposed for a dual voltage 42/14V system in automobiles [72], as given in Figure 1.5(b). The converter is designed to suppress transient currents during converter start-up and change of mode between buck and boost operation. Transistor gate signals are blocked for a definite time, to suppress transients during start-up and mode change. The blocking time is chosen from stored reference data according to operating conditions, and this limits the versatility of the circuit's operation.



(a) (b)

Figure 1.5 Single stage bidirectional DC-DC converter
(a) for electric railways [71] (b) for automobiles [72]

The behaviour of several low power DC-DC converter modules with different ratings at cryogenic temperatures was investigated in [73] for space applications. Test results revealed that the converters exhibit improved efficiency and enhanced dynamic performance in comparison to operation at room temperature.

1.3.2 High power bidirectional converter topologies

Targeting space applications, a bidirectional non-isolated DC-DC converter was presented in [74-75]. This topology, shown in Figure 1.6, provides input and output current filtering through coupled inductors with reduced noise and no requirement for additional filters. However, it has a limited voltage conversion ratio, due to no transformer isolation, and needs the complexity of a floating gate drive for transistor M_2.

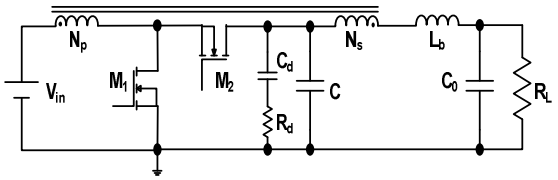


Figure 1.6 Bidirectional coupled inductor boost converter [74]

Reference [76] dealt with a cascaded bidirectional buck-boost converter, shown in Figure 1.7, as a candidate for electric vehicle applications. Despite low electric and thermal stresses experienced by the active and passive components, it requires twice the number of active components in comparison to the topology of Figure 1.6. The circuit was not analysed by the authors. Several non-isolated DC-DC converters, to address power management in hybrid electric vehicles when using an ultracapacitor as an energy storage medium, were compared in [77]. Even though the work gave a detailed analysis of active and passive component current stresses, the converter topologies investigated, restricted the ultracapacitor voltage to be equal to or less than the DC bus voltage.

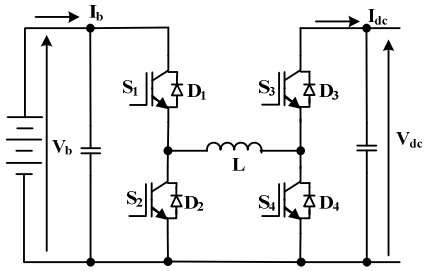


Figure 1.7 Cascade buck-boost converter [76]

A dual half bridge topology was introduced, to achieve a high power rating with a low number of devices in [78-81]. It has a voltage fed inverter at the high voltage side and a current fed inverter at the low voltage side, as portrayed by Figure 1.8. Zero-voltage-switching

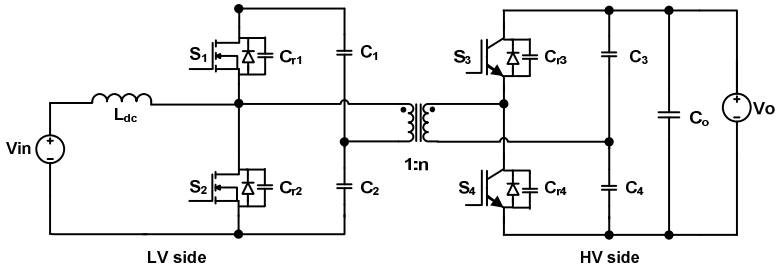


Figure 1.8 Bidirectional half bridge DC-DC converter [78]

(ZVS) is achieved in either direction of power flow without a voltage-clamping circuit or extra switching devices and resonant components. However, the split capacitors have to handle full load current and a voltage sharing imbalance might exist in the two sets of capacitors due to variations in initial conditions and/or DC offsets in the controller analog components. Thus an additional control circuit is required to eliminate capacitor voltage imbalances.

In order to overcome the drawbacks of the topology in Figure 1.8, a new bidirectional isolated DC-DC converter, shown in Figure 1.9, was proposed in [82] for a fuel cell powered electric vehicle driving system. It has the advantages of high efficiency, simple circuit configuration and cost-effectiveness. The inductors L_1 and L_2 offer ripple cancellation on the battery current. But, the penalty for achieving bidirectional operation is that the circuit requires two additional inductors and one series blocking capacitor.

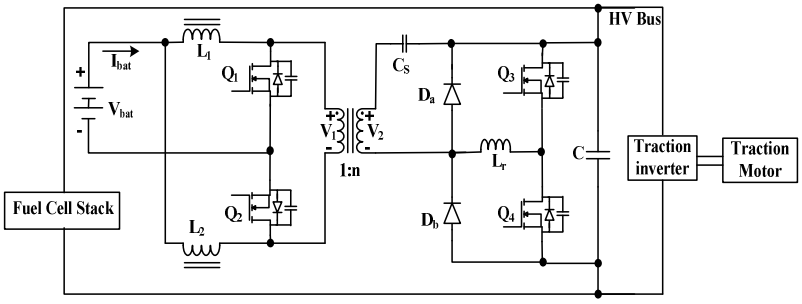


Figure 1.9 Isolated bidirectional power converter, [82]

The converter proposed in [83] and discussed in [84] is for a power conversion system comprising two H-bridge converters, shown in Figure 1.10. The H-bridge converter on the left is implemented with bidirectional switches and connected to its supply with an inductor. Because of the absence of fast forward and reverse blocking devices [83], the switches on the left-hand-side are realized by an antiparallel series connection of an IGBT and a diode in the medium power range. Although the converter exhibits low switching losses, the high on-state loss of the bidirectional switches is a drawback.

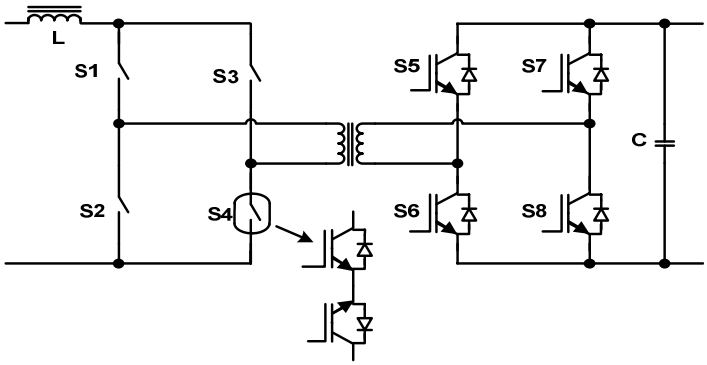
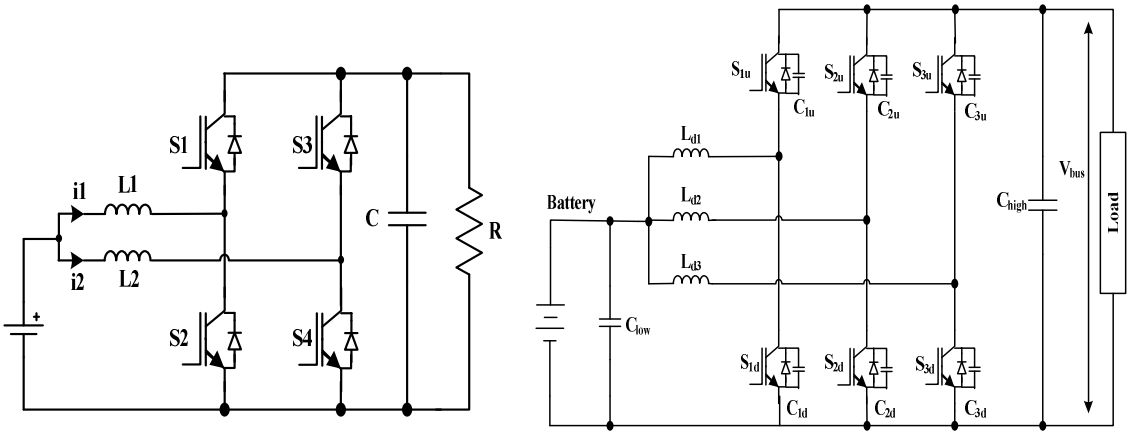


Figure 1.10 Two bridge bidirectional DC-DC converter [84]

Dual and three phase interleaved bidirectional DC-DC converters, shown in Figure 1.11(a) and 1.11(b), were proposed as suitable for high power density design and soft switching operation of the converter transistors in [85-86]. In order to increase the power density, the converter could be designed to operate in discontinuous current mode (DCM) so that the passive inductor size can be reduced. But DCM operation introduces a high current ripple, so it is necessary to interleave multiple phases to reduce the ripple. This topology may be beneficial when voltage conversion ratios are not high.



(a) (b)

Figure 1.11 Interleaved bidirectional DC-DC converters (a) Dual phase [85] (b) Three phase [86]

An interesting topology is the dual active bridge (DAB) configuration, in which two H-bridges are coupled through a high frequency transformer as shown in Figure 1.12. Many papers have been published on this topology over the past two decades [87-120], particularly

aimed at its bidirectional feature for energy storage systems. The topology is popular for its low device and component stresses, small filter components, low switching losses (by virtue of zero voltage switching), high power density and high efficiency, bidirectional power flow capability, buck-boost operation and low sensitivity to system parasitics. However, zero voltage switching is lost under light load conditions [87]. Nevertheless, high performance and high efficiency along with the other advantages listed above are notable. Hence, a number of researchers have pursued research on DAB converters. Their achievements are summarised in the following paragraphs.

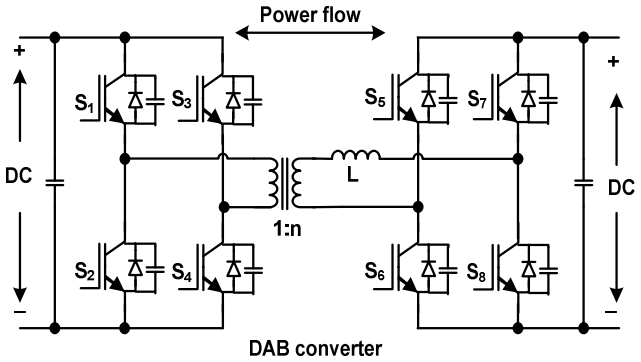


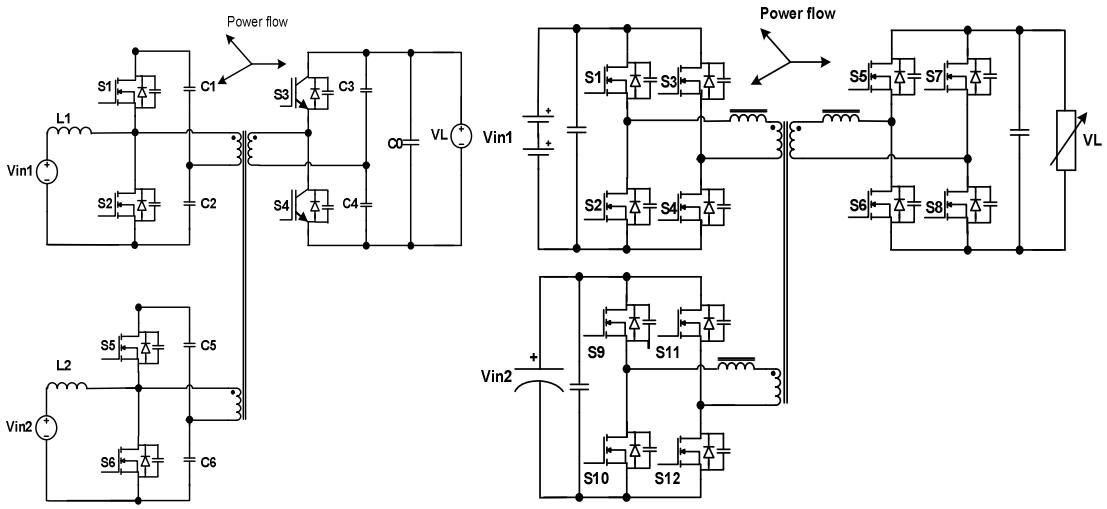
Figure 1.12 Dual Active bridge bidirectional DC-DC converter [87]

The first article on a DAB converter [87], published 17 years ago, highlighted its performance for high power applications. Subsequently, several papers were published [88-91] on the converter performance, accompanied by comprehensive analysis. Design considerations for high frequency transformers used in DAB converters were concerned with core material selection, loss minimisation and realisation of controlled leakage inductances as discussed in [92-93]. Dynamic performance of the DAB converter analysed through a small signal model was presented in [94-95], and a converter loss model was introduced for performance evaluation and design optimisation, as described in [96].

A comparative evaluation of the DAB topology with other isolated converter topologies was reported in [97-100] and soft switching techniques to enhance the performance were presented in [101-106]. Various modulation techniques and control strategies to minimise the losses were investigated in [107-111]. The authors of [107-108] introduced trapezoidal and triangular modulation methods to achieve triangular and trapezoidal currents

in the AC link. This was achieved by modulating the duty ratio of the converter bridges as an alternative method to reducing losses over a wide operating voltage range. These modulation methods are applicable for certain voltage conversion ratios and dead-time, but increase the RMS and peak currents of the devices. Reference [112] studied the performance of the DAB converter incorporating the latest switching devices and the use of this topology for automobile applications was investigated in [113-114]. References [115-120] validated the performance of the DAB topology for next generation power conversion systems and energy storage systems using supercapacitor based technologies.

Recently, a triple active bridge (TAB) topology has been introduced [121-127] as an advancement of the DAB topology, as shown in Figure 1.13(a) and 1.13(b). This topology has three active half/full bridges to combine a slow primary source with fast energy storage to power a common load. In [121-122], a three-port converter having two current fed ports was used as an interface with multiple energy storage elements; however, the converter cannot operate with zero voltage switching when port voltages vary widely.



(a) (b)

Figure 1.13 Triple Active Bridge bidirectional converters (a) Half bridge [121] (b) Full bridge [127]

In [123], a tri-modal half-bridge converter is presented, based on an isolated half-bridge converter topology. It has only one bidirectional port and thus does not support a

regenerative load. The three-port TAB topology reported in [124-127] has the property of bidirectional power flow due to the presence of active bridges at all ports. The power flow between the three-ports can be managed by phase shifting the gate drives to the bridges. Nevertheless, it is not possible to maintain soft-switching in the case of wide operating voltages at the ports, for example, when using supercapacitors and weak primary sources such as fuel cells.

1.4 Review of control methods for DC-DC conversion

This section investigates the various control techniques proposed so far for DC-DC power conversion. This covers soft switching techniques; analog approaches and newly developed digital techniques along with their merits and demerits. The use of high frequencies in high power conversion has created a demand for improved dynamic performance in controlling power flow in the target applications. Depending on the application, the control may have different functions. For example, in energy storage system, charging and discharging would be the two main functions during periods of regeneration and peak power demand. Hence, the controller should be designed to achieve these objectives, by choosing appropriate control parameters so as to operate the power conversion system effectively and efficiently in different scenarios. Hence, control strategies to achieve high-level operational performance constitute an important research area in the realm of power electronics.

1.4.1 Soft-switching control techniques

There has been an increasing demand for raising the switching frequency of power devices to allow the use of small filters and energy storage elements, thereby facilitating higher power density and improved dynamic performance. With hard switching a higher switching frequency leads to increased switching losses, switching noise and switching stresses [128]. However, the DAB converter can operate all its power switches in zero voltage switching (ZVS) keeping the switching loss low. The modulation scheme presented in [129] can only achieve ZVS within a limited region, as it reverts to hard switching whilst operating under very light load conditions. Efforts have been undertaken to extend the soft switching region, but the full load range remains to be covered [130].

Many methods have been proposed to extend the ZVS range of operation, and they are based on two main approaches. The first technique is to use additional circuit components such as an inductor, a saturable inductor in series with the primary transformer and a snubber circuit [131-132]. These approaches, while extending the load range for ZVS, results in significant conduction losses or increase the design cost. Another approach [133] is to employ zero current switching (ZCS) at, say, the left-leg transition and ZVS at the right-leg transition without additional hardware components by phase shifting the two half-bridge legs of a full-bridge. Therefore, the converter operates in discontinuous current mode under light loads, where the transformer currents feature a triangular shape. Thereby, the left-leg switches of the half bridge operate in ZCS and the right-leg switches operate in ZVS. This approach also extends the load range for soft switching, but there is a region between the minimum load for ZVS and the maximum load for ZCS at left-leg, where the switches of the left-leg neither work under ZCS nor ZVS [133]. In that region, the peak primary current is not zero prior to turn-on of left-leg and this peak current is too small for the left-leg to achieve ZVS.

Active-clamp type isolated boost dc/dc converters, shown in Figure 1.14(a), (b) and (c), achieve soft switching while minimising the circulation current [134-136], and achieve relatively high efficiency power conversion. However, an active snubber consisting of a switch and capacitor has to switch at twice the switching frequency and at the full power of the main dc/dc converter. The fly back start-up winding shown in Figure 1.14(a) on the main choke is only used in the start-up stage in boost mode operation, while it remains dormant in other operation modes. Reference [136] compared the performance of the L-type half-bridge converter, shown in Figure 1.14(b), with the current fed full-bridge as shown in Figure 1.14(c) for the low voltage side whilst retaining voltage-fed full-bridge converter on the high voltage side. The L-type half-bridge has less active component count than the current-fed full-bridge, but it has more passive components. The current-fed full bridge as shown in Figure 1.14(c) employed in [136] has an active clamping circuit, consisting of clamping switch S_c and clamping capacitor C_c. The body diode of S_c naturally conducts whenever the LV side voltage exceeds the voltage across the clamping capacitor C_c. The clamping switch S_c can be turned on during the energy transfer period. During battery discharge mode operation, the active clamp circuit also allows zero-voltage zero-current switching (ZVZCS) because the primary

side current is reset to zero when Sc is turned on. Although the L-type half-bridge has less active components, experimental results presented in [136] revealed that it is inefficient during bidirectional operation due to the passive clamp circuit. The burden of high current stress and associated thermal issues of the active switch and the capacitor, add limitations to active-clamped snubber methods in bidirectional high power applications. In [137], the full bridge current fed converter was used, which also requires voltage clamping to avoid excessive voltage stress across the LV side switches.

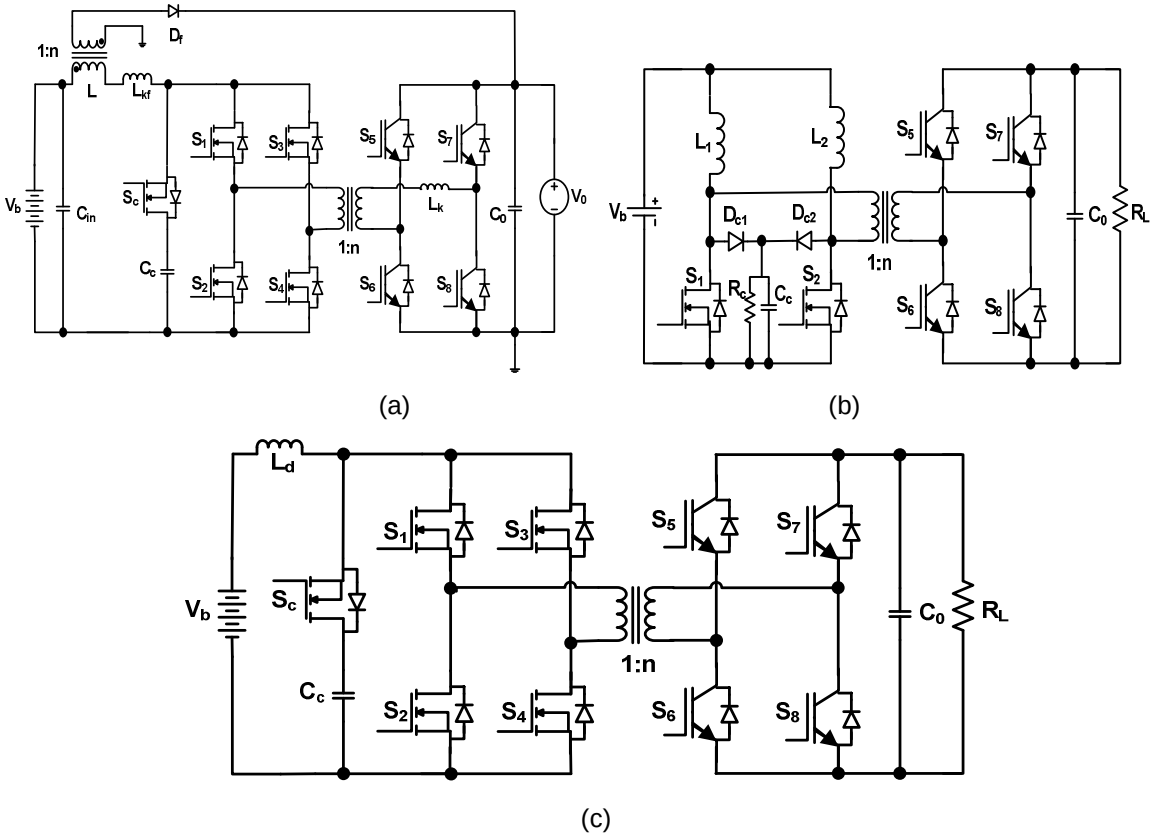


Figure 1.14 Active-clamp isolated bidirectional converters
(a) with soft-start capability [134] (b) using L-type half-bridge [136]
(c) using current-fed full-bridge [136]

Unique commutation logic, to minimise the mismatch between current in the current-fed inductor and that in the leakage inductance of the transformer at the time of switch commutations, was proposed in [138], using the topology shown in Figure 1.15. The control scheme utilizes the resonant tank (consists of device output capacitance and leakage inductance) and freewheeling path in the full bridge inverter at the voltage-fed side to preset

the current in the leakage inductance of the transformer in a resonant manner. This reduces the difference between the current fed inductor and leakage inductor thereby the voltage spike

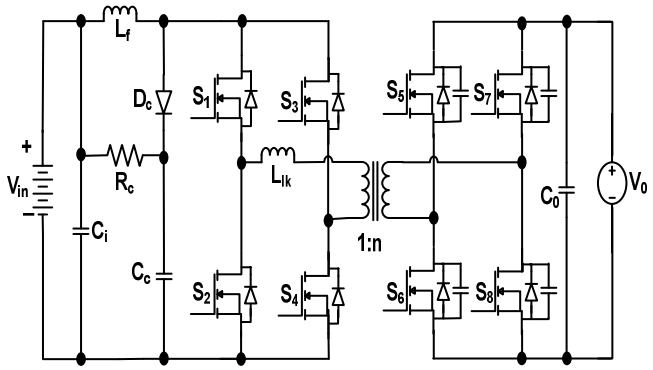


Figure 1.15 Soft commutating isolated full bridge bidirectional DC-DC converter [138]

across the switches in the current fed side. Therefore, low current flows through the clamping snubber thus significantly reducing its power rating and enabling the use of a passive snubber. However, an additional voltage clamping circuit is still required to clamp the voltage spike although the energy that is dumped into the clamped snubber C_C is minimized.

To reduce the switch count and improve the performance, a half-bridge-based topology was proposed and studied extensively in [80, 139]. Although the devices of the half-bridge on the low voltage side are subject to twice the dc input voltage in the topology shown in Figure 1.8, this is an advantage for electric vehicles and fuel cell applications because the dc input voltage is very low (12 V batteries) so that the extra voltage is easily managed. The major drawback of the half bridge is that the split dc capacitors have to handle the full load current. Consequently, high current electrolytic capacitors in conjunction with high frequency polypropylene capacitors are used. Chiu and Lin [82] proposed a bidirectional converter that consists of a current doubler at the low voltage side to further reduce the battery ripple current, and a soft switching asymmetrical half bridge at the high-voltage side.

In [140], a ZVZCS bidirectional DC/DC converter was proposed. The input stage switches are turned-on in a ZVS condition, and those in the output stage are turned-off in a ZCS condition. Nevertheless, the circuit has a high passive component count, which in turn

affects the efficiency and power density. To extend the soft-switching operating range, a phase-shift and pulse-width-modulation control (PPS) scheme was proposed in [141-144] and the PPS converter is shown in Figure 1.16. Compared with phase shift control alone, PPS control can reduce current stresses and the RMS currents in the converter, decreasing the converter losses. However, the performance of the converter in terms of the ZVS operating region, converter stress and conductor loss parameters was examined and discussed only for low voltage conversion ratios (between the range of 0.8 to 1.25).

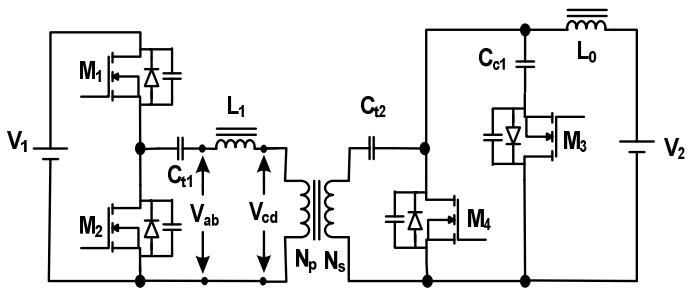


Figure 1.16 Phase-shift plus PWM control bidirectional DC-DC converter [141]

1.4.2 Analogue control techniques

In general, voltage mode control and current mode control of the converter were initially realized through analogue means. Voltage mode control is a single-loop control in which the output voltage is measured and compared with a reference voltage. The amplified difference between the two is compared with a fixed frequency saw tooth waveform to produce the switching duty ratio. The switching duty ratio via the switching devices, adjusts the voltage across the inductor and hence the inductor current. This eventually brings the output voltage close to its reference value. However, this technique usually results in a slow response [145]. Compared with voltage-mode control, current-mode control provides an additional inner loop for controlling current. Comparing output voltage with reference voltage generates an error signal. This error signal is used to generate the control signal. The inductor current is then sensed and compared with the control signal to generate the duty cycle of the switch of the converter [145].

Analogue current programmed control can be classified as peak or valley current control, depending on whether the maximum or minimum point of the sensed current is compared to a reference. In such a control scheme, transistor is controlled on a cycle-by-cycle basis. This helps to improve the dynamic performance of the system. In addition, peak current control offers fast over-current switch protection. However, peak or valley control results in some line current distortion, which can be reduced by biasing the reference current waveform [146, 147]. Moreover, in peak current control, to minimise the error between peak and average currents, a compensating ramp with a slope equal to the inductor current down-slope is usually applied to the comparator input to eliminate instability. This technique is called slope compensation, and is required for peak current control when the transistor duty ratio exceeds 50% during continuous conduction mode. Another technique is to operate the converter at the boundary of continuous and discontinuous conduction modes, such that the average inductor current follows one half of the peak current reference. However, the switching frequency is variable, and additional circuitry is required to detect the zero crossing of the inductor current [148-150].

For a number of years, Proportional plus Integral (PI) controllers have been prevalent in power electronic systems because of their flexibility, ease of implementation and simple structure [151]. However, the limitations of a PI controller are also obvious. The parameter selection of a PI controller is a tradeoff between robustness and transient response, and is very empirical. In general, a large overshoot occurs in the output when the rise time of the response is reduced. Anti-windup protection when incorporated into PI controllers can help to mitigate such problems [152].

The analogue controller for a bidirectional DC-DC converter is often realized using general purpose PWM ICs [101,141,153]. In [141], a phase shift plus pulse-width-modulation (PPS) control was applied to the bidirectional DC-DC converter shown in Figure 1.16, where the converter uses two half-bridges to generate asymmetrical waveforms in order to deal with the voltage variation. Firing signals are derived using two PWM controllers. Similarly, [154-155] describe a bidirectional DC-DC converter control using two PWM ICs. When the converter operates in either forward/reverse operation modes, one of the PWM ICs is enabled

and the other is disabled. The output of the error amplifier of the disabled IC may therefore saturate. Hence, during mode transition, a circuit that can suspend switching operation for a certain time interval is required. A seamless change of direction is not possible because the switching operation needs to be blocked for a certain time until the controller is able to output nominal duty and suppress any transient currents occurring during start-up and mode transitions.

Although, analogue control has been dominant owing to its simplicity and low implementation cost, it has several drawbacks, such as high part count, low flexibility, low reliability, and sensitivity to environmental influences such as thermal ageing, and tolerance [156]. In addition, the dynamic behaviour of power converters is complicated due to the nonlinear and time varying nature of switches, variation of parameters, and fluctuations of input voltage and load current, and analogue controllers cannot easily cope with such variations.

1.4.3 Digital control techniques

Advanced algorithms that are computationally intensive, programmed into digital controllers, can provide improved performance with reduced cost. The potential advantages of digital control over analog control are higher immunity to component variations, increased flexibility through programming and the possibility to improve performance using more advanced control algorithms and a reduced number of components [157]. Digital control for DC-DC converters can be implemented using digital signal processors (DSPs), microcontrollers and application-specific digital integrated circuits (ASICs). Generally, DSPs feature more computational power than microcontrollers. Therefore, more advanced control algorithms can be implemented using a DSP. On the other hand, microcontrollers tend to be less expensive than DSPs, therefore providing digital control solutions at lower cost and ASICs are designed specifically for a special purpose application. However, digital current mode control is not easy to achieve [158], because the transistor/inductor current is a fast switching waveform and its switching frequency is very high.

The problems associated with digital current mode control were investigated and a way to improve the performance of digital current control was dealt with in [158]. The proposed peak, valley and average digital current programmed control schemes were validated to a maximum frequency of 400Hz, suitable for avionic requirements. High performance data converters are required for a DSP-based controller. The performance of the converter in terms of its speed, conversion precision and noise greatly influences the fidelity of the controller. Hence, many have not attempted digital current mode control using high frequency current sampling; instead existing literatures deal with output/load voltage control and output/source DC current control of DC-DC converters [159-161]. Many advanced modulating strategies, such as fuzzy-neural control or sliding-mode control [162-163], have been proposed recently and shown to be feasible in simple-structured circuits, such as buck, boost, and half-bridge circuits [164-165].

A review of different digital current control techniques is given in [166]. The predictive digital current programmed control algorithm works on the principle of predicting the duty cycle of the next switching cycle based on the values obtained from the previous cycles. This requires samples of the input and output voltage values for calculating the next duty cycle [167-168]. Using this method, predictive valley current control, predictive peak current control and predictive average current control are achievable.

Digital control of power electronics has been investigated considering three different generations of control [169]. They can be classified as follows: the first generation used digital processing on the control loop periphery to perform a supervisory role, the second generation applied digital processing inside the control loop to achieve real-time control processes and finally the present third generation uses digital processing for moment-by-moment direct action of active switching devices in a converter. [169] also discussed the sampling issues involved in using A/D and D/A converters for achieving high frequency current control.

Two PI controllers with anti-windup protection were employed to regulate the dc link voltage and fuel cell power in [170]. The controller was based on the digital approximation of an analog backward Euler scheme. The sampling frequency was chosen as 100 kHz, and 50%

of the DSP computational power was consumed by the dc-dc stage interrupt routine. Other articles [171-172] highlighted digital control based on referencing look-up tables. In [172], a digital signal processor and a programmable logic device were used for controlling the bidirectional DC-DC converter, with the DSP operating at a sampling frequency of 50 kHz. Due to the computational complexity, the control parameters were calculated numerically in advance and stored in the form of look-up tables with the current reference signals as the index parameters.

1.5 Summary of literature review

From the literature review, the present scenario and development trends in More Electric Aircraft systems shows there is a growing demand for high performance power electronic systems. In particular, DC systems are found to be robust for modern and future aircraft systems due to their continuous operation during severe supply transients. The electro hydraulic and electro mechanical actuators draw transient power during their operation and are capable of returning power to the source during regeneration. Hence, in order to maintain the DC system voltage during transients and to provide clean and stable power to those bidirectional active loads, efficient power electronic interfaces for environment friendly, fast responding aircraft energy storage systems are mandatory. A literature review of existing DC-DC converter topologies and control methods for bidirectional power transfer shows there is still scope for improving the converter performance. The review suggests that considering various factors such as power density requirements, operating voltage conversion ratio, soft switching range, efficiency and safety needs etc., an appropriate topology has to be carefully identified for each application, and there is no universally suitable converter topology. Review of the control methods for DC-DC power conversion gave a broad overview of control techniques in both analog and digital domains in addition to soft switching techniques.

The interest in DAB converter topology for high power density applications such as aerospace applications is increasing rapidly due to its attractive features. However, most of the soft switching techniques employed for DAB converters improve performance at the expense of introducing additional active and passive components. Hence, it was decided to enhance the performance of the converter without any additional components. Moreover, a comprehensive

review reveals that control of the DAB converter topology is mainly limited to PI based phase shift control. The traditional PI based phase-shift control is simple and easy to implement, but lacks flexibility. In this method of control, either the output DC voltage or the average of the output current of the converter is considered as the control parameter to achieve the desired phase shift between the two bridges. In some cases, input power and output dc voltage have been regulated to achieve the desired phase shifts, thereby effecting power transfer. During transient operation, the phase shift might fluctuate which may cause current oscillation and voltage over-modulation. In addition, any change in line or load parameters must first be sensed as an output change and then corrected by the feedback loop – this results in a slow response. Hence, controlling these parameters that are slowly varying in nature affects the dynamic response of the system. Currently, there is a need to improve the dynamic response of systems during bidirectional operation when the main power source is not designed to meet the peak power demand.

1.6 Objectives

This Thesis describes the research work underpinning one of the developments in the Rolls-Royce UTC facility dealing with intelligent electrical networks for future autonomous vehicles. In particular, the design, implementation and testing of a power electronic interface, to connect a ultracapacitor energy storage system with the 100kW aircraft electric power system in the IEPNEF, has been undertaken. The aim of this Thesis is to analyse, design, construct and evaluate the performance of the DAB DC-DC converter topology for an aircraft electric energy storage system. In addition, it discusses a new operating mode that is found to enhance the performance of the DAB converter without resorting to the use of any extra active or passive elements. Furthermore, this Thesis also presents a new bidirectional control strategy that could possibly enhance the dynamic performance of the DAB converter for future aircraft systems. The simulation results obtained using SABER software underline its robustness in the presence of transients.

There are three main contributions in this Thesis. Firstly, the Thesis introduces a new steady-state analysis for the DAB converter which derives equations for the average and RMS device currents and the peak and RMS inductor/transformer currents for the square-wave

mode. These equations are useful for the design of the converter prototype. The analysis focuses on understanding converter current shapes and identifying the zero-voltage switching (ZVS) boundary condition. Secondly, the steady-state analysis of quasi-square-wave mode of the DAB converter is proposed by introducing dead-time in the transformer primary, secondary and simultaneously on primary and secondary voltages. The key findings from the analysis show that the performance of the converter improves under light-loads with reduced dead-time, and ZVS enhancement is achieved at the expense of increased conduction losses. The novelty of the analysis is in the derivation of equations for the average and RMS device currents and the peak and RMS inductor/transformer currents. The analysis can be extended to other converters of the same family. Also, it can be extended to address other operating modes of the DAB converter such as discontinuous current mode. A 20kW DAB converter prototype is designed and built to evaluate the proposed steady-state analysis. The experimental testing validated the design, the steady-state analysis proposed and theoretical predictions. Finally, a novel controller is presented and some preliminary investigations have been undertaken to show its operation for bidirectional power transfer. However, further investigations are needed to examine the controller performance in a real-time scenario.

1.7 Organisation of the Thesis

This chapter gives background information relating to the research area, objectives of the research, survey of existing literature and describes the Thesis structure.

The second Chapter makes a contribution to the steady-state analysis of the DAB converter by presenting equations for the RMS and average device currents and the RMS and peak inductor/transformer currents. This Chapter explains the operating principle of the DAB converter and the SABER simulation results validate the proposed analysis.

Chapter 3 focuses on the design, construction and development of the DAB converter prototype. It includes the selection information of power semiconductor devices, input and output filter capacitors, snubber capacitors, heat sink, planar busbar designs, design of driver circuits and interfacing and conditioning circuits for DSP control.

Experimental verification of the DAB converter prototype is presented in Chapter 4. It includes the individual testing of high voltage and low voltage side bridges and the DAB converter, loss estimation of devices and study of the effect of snubber capacitors. This chapter also mentions the electromagnetic noise issues and their minimisation.

The fifth Chapter proposes a new mode of operation for the DAB DC-DC converter accompanied by a detailed analysis of complex converter waveforms. It covers the performance evaluation of the DAB converter by means of introducing dead-time on the transformer primary, secondary and simultaneously on both the primary and secondary windings. This leads to quasi-square-wave mode of operation of the DAB converter. Analysis is performed for the quasi-square-wave modes producing equations for the device RMS and average currents and the peak and RMS currents in the coupling inductor. The operation of the DAB DC-DC converter is verified through extensive simulations, confirming the accuracy of the analysis. Experimental results are included to support the theoretical analysis.

In Chapter 6, a new bidirectional current control for the DAB DC-DC converter is described and some preliminary investigations are undertaken to show its operation. It covers the SABER simulation models for bidirectional control under square-wave and quasi-square-wave modes of operation of the converter, extensive simulation results corresponding to steady-state and transient performance analysis for both the operating modes and confirmation of simulation and analytical results. Also, the DSP performance related issues are discussed.

Finally, the conclusions are drawn in Chapter 7. The original contributions in this research are summarised and directions for further research are highlighted in good detail. Following this, the appendices that contain supplementary information for Chapters 2 to 6 are provided.

Chapter 2

Bidirectional DAB DC-DC Converter for Aircraft Electric Energy Storage Systems

2.1 Introduction

The DAB converter topology has been chosen as it features high power density, high efficiency, bidirectional power flow capability, inherent soft switching, galvanic isolation and low number of passive components. Hence, the converter is a candidate for high-power-density aerospace applications [87]. This chapter makes a contribution to the steady-state analysis of the DAB converter by producing equations for the RMS and average device currents and the RMS and peak inductor/transformer currents. These equations are useful in predicting the losses that occur in the devices and passive components and for the design of the converter prototype. The SABER simulations verified the theoretical results of the analysis.

Future aircraft will employ high power transient loads such as electrically powered actuators for adjusting flight control surfaces [173]. Ultracapacitors are one possible form of energy storage device that may be used to meet these high transient power demands and smooth the load on the generators. Ultracapacitors could conceivably be beneficial in aircraft energy storage applications due to their fast response time and high current/power handling capability over a wide range of operating temperatures. A Maxwell Technologies 125V ultracapacitor module specification has been used in SABER simulations to evaluate the converters performance. The input supply voltage for the converter was chosen as 540V. These two voltage levels are likely to be used in future aerospace systems [173]. As the switching frequency is increased, the transformer and inductor size decreases. But, if the switching frequency is high, the switching losses increase. Therefore, based on the current handling capability and power dissipation capability of available devices for the specified voltage levels on the HV and the LV sides of the DAB converter, the device switching frequency was chosen as 20 kHz.

The analysis of the DAB converter was performed for both charging and discharging modes of operation, and the conditions to achieve ZVS have been derived. The effect of the

snubber capacitor during device turn-off has been analysed, from which the turn-off equivalent circuit has been obtained. The minimum load current requirement to achieve ZVS has been determined by analysing the action of turn-off snubbers.

2.2 Principle of operation of DAB DC-DC converter

The DAB converter shown in Figure 2.1(a) consists of two full-bridge circuits whose AC connections, ab and cd are connected through an isolation transformer and a coupling inductor L, which may be provided partly or entirely by transformer leakage inductance. The full

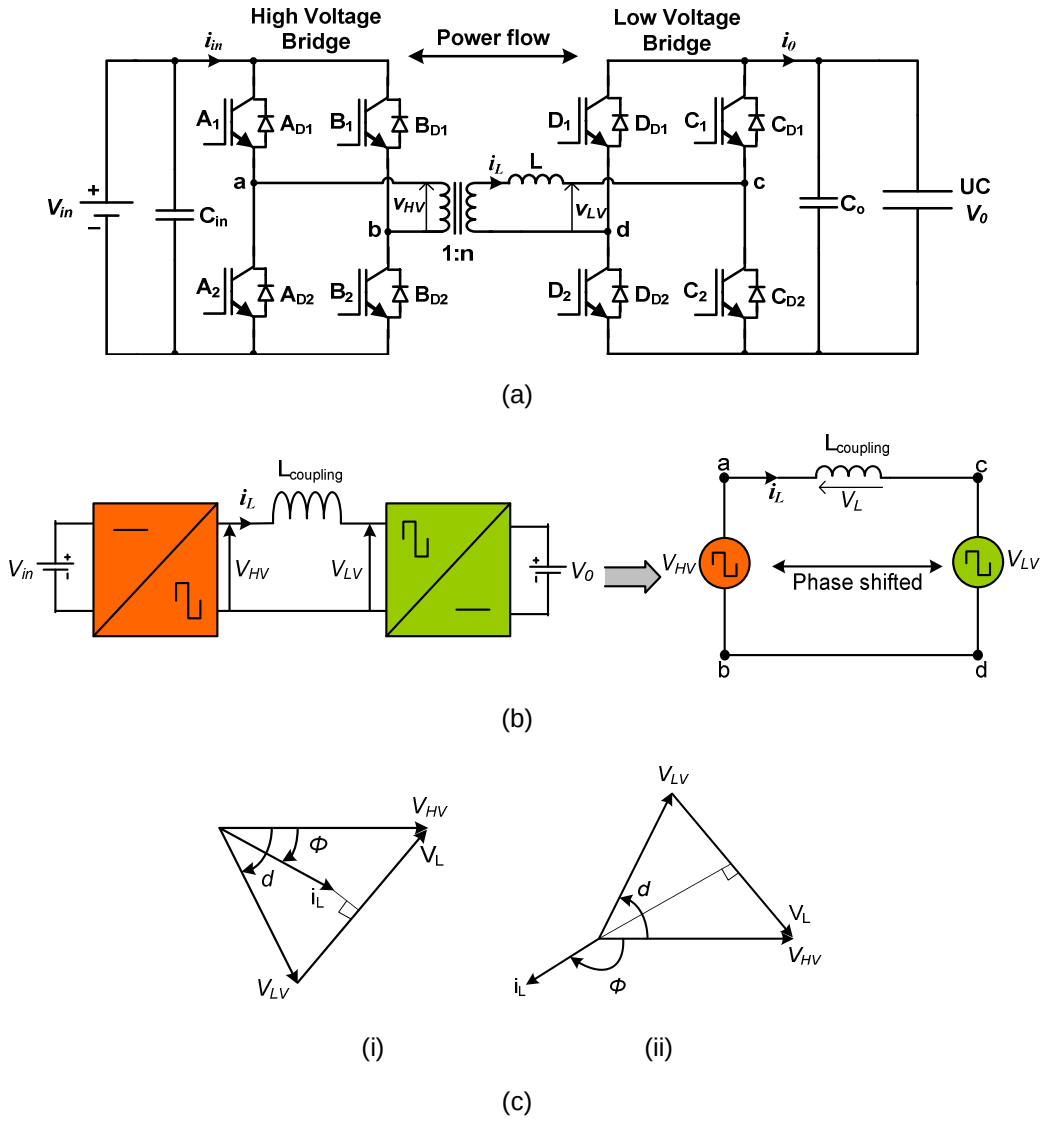


Figure 2.1 (a) Schematic of the DAB DC-DC converter (b) Simplified equivalent circuit (c) Phasor diagram for (i) lagging (V_{LV} lags V_{HV}) and (ii) leading phase (V_{LV} leads V_{HV}) shifts

bridge on the left-hand-side of Figure 2.1(a) is connected to the high voltage (HV) DC bus and the full-bridge on the right-hand-side is connected to a low voltage (LV) ultracapacitor. Each bridge is controlled to generate a high-frequency square-wave voltage at its transformer terminals of the same frequency. The two square-waves can be phase-shifted with respect to each other to control the power flow through the transformer and inductor. Thus power can be made to flow from V_{in} to V_0 or vice versa. Power always flows from the bridge generating the leading square-wave to the other bridge [87].

For illustration purposes, the switching devices on the HV side are labelled 'A' and 'B' and those on the LV side are 'C' and 'D'. In order to differentiate the devices located in the top and bottom portions of each leg, the devices located in the top of each leg are provided with the subscript '1' and the devices in the bottom of each leg are identified by the subscript '2'. The anti-parallel diode across each device is named in the same manner with an additional subscript 'D'.

To elucidate the operation and power flow in the converter, simplified equivalent circuit and phasor diagrams are shown in Figures 2.1 (b) and (c). The voltages generated by the two full-bridges, V_{HV} on the HV side and V_{LV} on the LV side are square-wave voltages with a fixed 50% duty cycle. i_L denotes the current flowing through the coupling inductance L, and V_L is the voltage across the coupling inductance. i_{in} denotes the HV side terminal (input) current and i_0 denotes the LV side terminal (output) current. The phase shift between V_{HV} and V_{LV} is $\frac{dT_S}{2}$, where T_S is the switching period and d is the controlled duty ratio. Phase displacement between V_{HV} and current i_L is denoted as Φ. Phasor diagrams (i) and (ii) depicted in Figure 2.1 (c) show that when V_{LV} lags V_{HV}, power flows from the HV bridge to the LV bridge and reverses when V_{LV} leads V_{HV}.

2.2.1 Charging mode

During this mode, the HV bridge leads the LV bridge by $dT_s/2$, where 'd' is the duty ratio and 'T_s' is the time period for one cycle. Thereby power flows from the HV side to the LV ultracapacitor side, to charge the ultracapacitor. The primary, HV bridge performs inverter

operation and the secondary, LV bridge performs rectification. During description of the states, it is assumed that the energy stored in the coupling inductance is sufficient to realise zero-voltage switching, ZVS, of all the transistors. The key operating waveforms of the converter during the charging mode, when power flows from the HV side to the LV ultracapacitor side, are shown in Figure 2.2.

The waveforms depict the gate voltages of transistors S_{A1} to S_{D2}, the voltages generated by the bridges V_{HV} on the HV side and V_{LV} on the LV side, i_L denotes the current flowing through the coupling inductance, $i_{AD1\text{-}A1}$ and $i_{CD1\text{-}C1}$ are the device currents on the HV and LV sides respectively and i_0 is the LV side terminal current. All transistors in the HV bridge exhibit similar waveforms, though A_2 and B_1 are displaced by half a cycle from transistors A_1 and B_2. Similarly, on the LV bridge, although transistors C_1, C_2, D_1 and D_2 have similar current waveforms, C_2 and D_1 are displaced in time by a half cycle with respect to C_1 and D_2. The transistor A_1 current waveform and transistor C_1 current waveform are drawn with their anti-parallel diode currents. Based on the assumption of loss-less components, the sequence of steady-state modes over one half of a switching cycle is described below. The various time instants are indicated in Figure 2.2.

- **$t_0 \rightarrow t_1$**

The cycle starts at t_0 when transistors A_1 and B_2 are turned on while their anti-parallel diodes A_{D1} and B_{D2} are conducting. This develops the supply voltage, V_{in}, across the transformer primary winding. Transistors C_2 and D_1 are conducting on the LV bridge side; thereby the transformer secondary voltage is clamped to $-V_0$ and this result in a gradual increase of inductor current.

- **$t_1 \rightarrow t_2$**

The transistors A_1 and B_2 continue to be on. At time t_1, transistors C_2 and D_1 are turned-off with ZVS. However, the current during turn-off is high and therefore to benefit from soft-switching, a turn-off snubber is needed. The current from transistor C_2 is transferred to diode C_{D1}. Similarly, transistor D_1 current is transferred to D_{D2} under ZVS. Now D_{D2} and C_{D1} are conducting; therefore the transformer secondary voltage is clamped to V_0. As a result, the inductor current increases to its peak value.

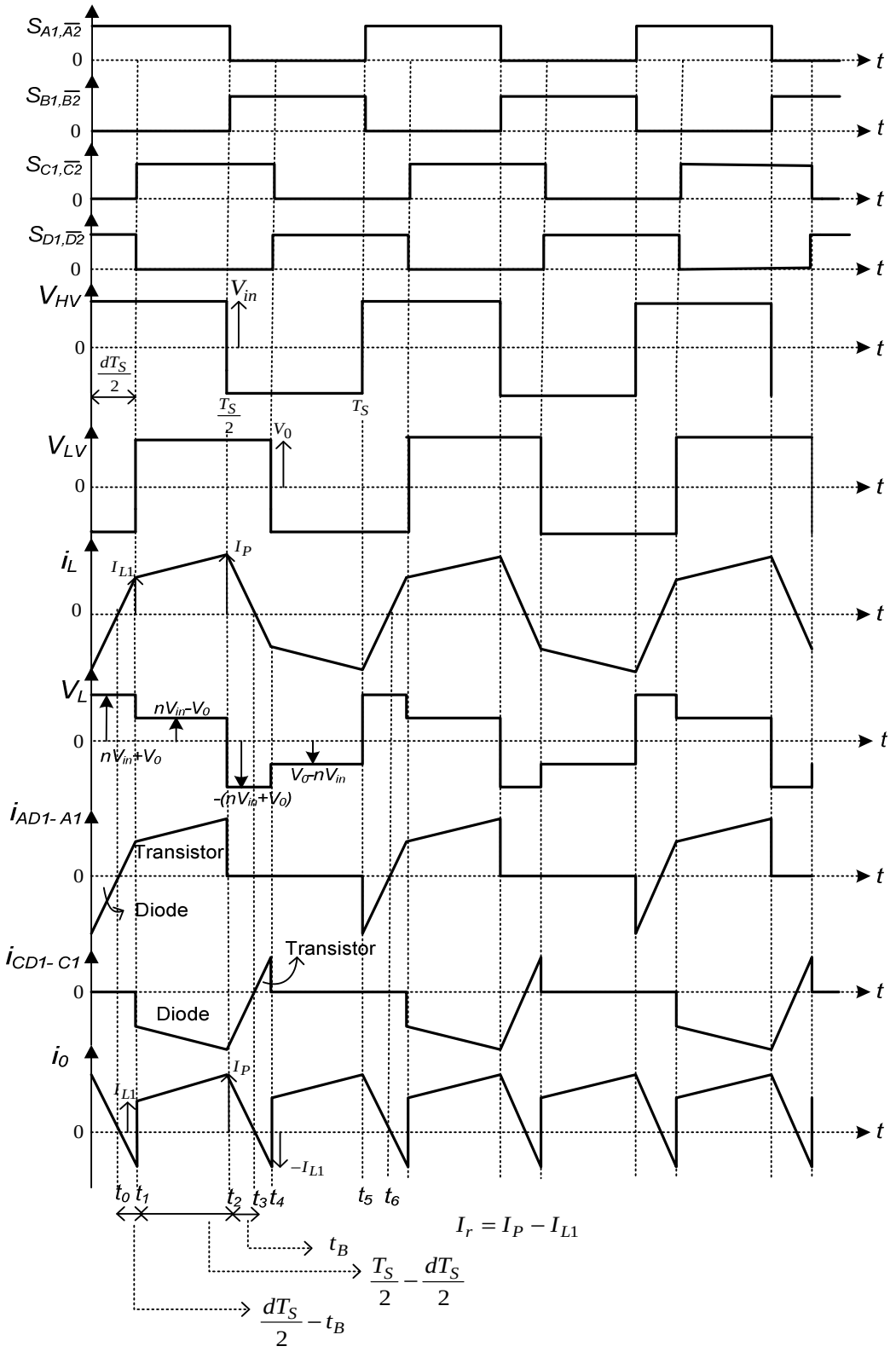


Figure 2.2 Idealised waveforms of the DAB converter during charging mode

- **$t_2 \rightarrow t_3$**

At t_2, transistors A_1 and B_2 are turned off under ZVS. The current from transistor A_1 transfers to diode A_{D2} under ZVS and current from transistor B_2 transfers to diode B_{D1}, hence A_{D2} and B_{D1} are conducting. Thereby the primary voltage is clamped to V_{in} in the opposite direction, whereas on the LV bridge side, diodes D_{D2} and C_{D1} continue to conduct and the transformer secondary voltage is retained at V_0. As a result, inductor current falls to zero and charges in the opposite direction gradually. This completes one half cycle. At t_3, the cycle is repeated, except with the corresponding opposite set of bridge transistors and diodes.

An important feature of converter operation is that losses due to diode reverse recovery are eliminated because the diodes have zero current at the turn-on instants of all transistors. Moreover, the turn-on of transistors is under ZCVS conditions due to the resonance of the coupling inductance and device capacitances. Table 2.1 summarises device switching conditions during the ultracapacitor charging mode. Though the table shows the switching conditions for all devices as ZVS on/off, under light load conditions the devices will be subjected to hard switching. This is due to insufficient energy being stored in the coupling inductance.

Table 2.1 Summary of switching conditions of devices during charging mode

Half cycle	Time instant	Conducting devices		ZVS Turn-on	ZVS Turn-off
		Input bridge	Output bridge		
First	t_0-t_1	A_1, B_2	C_2, D_1	A_1, B_2, C_2, D_1	
	t_1-t_2	A_1, B_2	C_{D1}, D_{D2}		C_2, D_1
	t_2-t_3	A_{D2}, B_{D1}	C_{D1}, D_{D2}		A_1, B_2
Second	t_3-t_4	A_2, B_1	C_1, D_2	A_2, B_1, C_1, D_2	
	t_4-t_5	A_2, B_1	C_{D2}, D_{D1}		C_1, D_2
	t_5-t_6	A_{D1}, B_{D2}	C_{D2}, D_{D1}		A_2, B_1

2.2.2 Discharging mode

In this mode, the LV bridge leads the HV bridge by $dT_s/2$, thereby power flows from the LV side to the HV side, assuming the source is capable of accepting the stored energy. Such a situation arises in an aircraft when peak power demand occurs in electric loads. Compared to the previous mode, the circuit operation is reversed. As a result, the secondary LV bridge performs an inverter operation and the primary HV bridge performs rectification, to discharge

the ultracapacitor. The various switching instants during discharging mode are marked in Figure 2.3. The waveforms in Figure 2.3 depict the gate voltages of transistors S_{A1} to S_{D2}, voltages generated by the bridges V_{HV} and V_{LV}, the current i_L flowing through the coupling inductance, the device currents $i_{AD1\text{-}A1}$ and $i_{CD1\text{-}C1}$ on the HV and LV sides respectively and the LV side terminal current i_0. Table 2.2 summarises the device switching conditions for a cycle during this mode.

- **$t_0 \rightarrow t_1$**

Just before t_0, the anti-parallel diodes C_{D1} and D_{D2} are conducting. At time t_0, transistors C_1 and D_2 are turned-on. The ultracapacitor voltage is applied across the transformer secondary. On the primary (HV side), transistors A_2 and B_1 are conducting; thereby the transformer primary is clamped to V_{in} in the reverse direction. Since the resultant voltage impressed across the inductor is negative, a gradual increase of inductor current in the reverse direction occurs until it attains its peak value at time t_1.

- **$t_1 \rightarrow t_2$**

At t_1, transistors A_2 and B_1 are turned-off under ZVS. Therefore, current is transferred from transistors A_2, B_1 to diodes A_{D1} and B_{D2} respectively. This clamps the transformer primary to the supply, V_{in}. Transistors C_1 and D_2 remain in conduction during this mode. The resultant voltage across the inductor is positive during this interval, which makes the inductor current fall from its negative peak.

- **$t_2 \rightarrow t_3$**

During this interval, current flowing in C_1 and D_2 transfers to diodes C_{D2} and D_{D1} respectively under ZVS, and transistors C_1 and D_2 turn-off. Now C_{D2} and D_{D1} are conducting, thereby the secondary of the transformer is kept at $-V_0$. Switches AD1 and BD2 continue to conduct during this interval. As a result, inductor current falls to zero and charges in the forward direction gradually. This completes one half cycle in discharging mode. The next half cycle repeats at t_3, except with the corresponding opposite set of bridge transistors and diodes.

Table 2.2 Summary of device switching conditions during discharging mode

Half cycle	Time instant	Conducting devices		ZVS Turn-on	ZVS Turn-off
		Input bridge	Output bridge		
First	t_0-t_1	A_2, B_1	C_1, D_2	A_2, B_1, C_1, D_2	
	t_1-t_2	A_{D1}, B_{D2}	C_1, D_2		A_2, B_1
	t_2-t_3	A_{D1}, B_{D2}	C_{D2}, D_{D1}		C_1, D_2
Second	t_3-t_4	A_1, B_2	C_2, D_1	A_1, B_2, C_2, D_1	
	t_4-t_5	A_{D2}, B_{D1}	C_2, D_1		A_1, B_2
	t_5-t_6	A_{D2}, B_{D1}	C_{D1}, D_{D2}		C_2, D_1

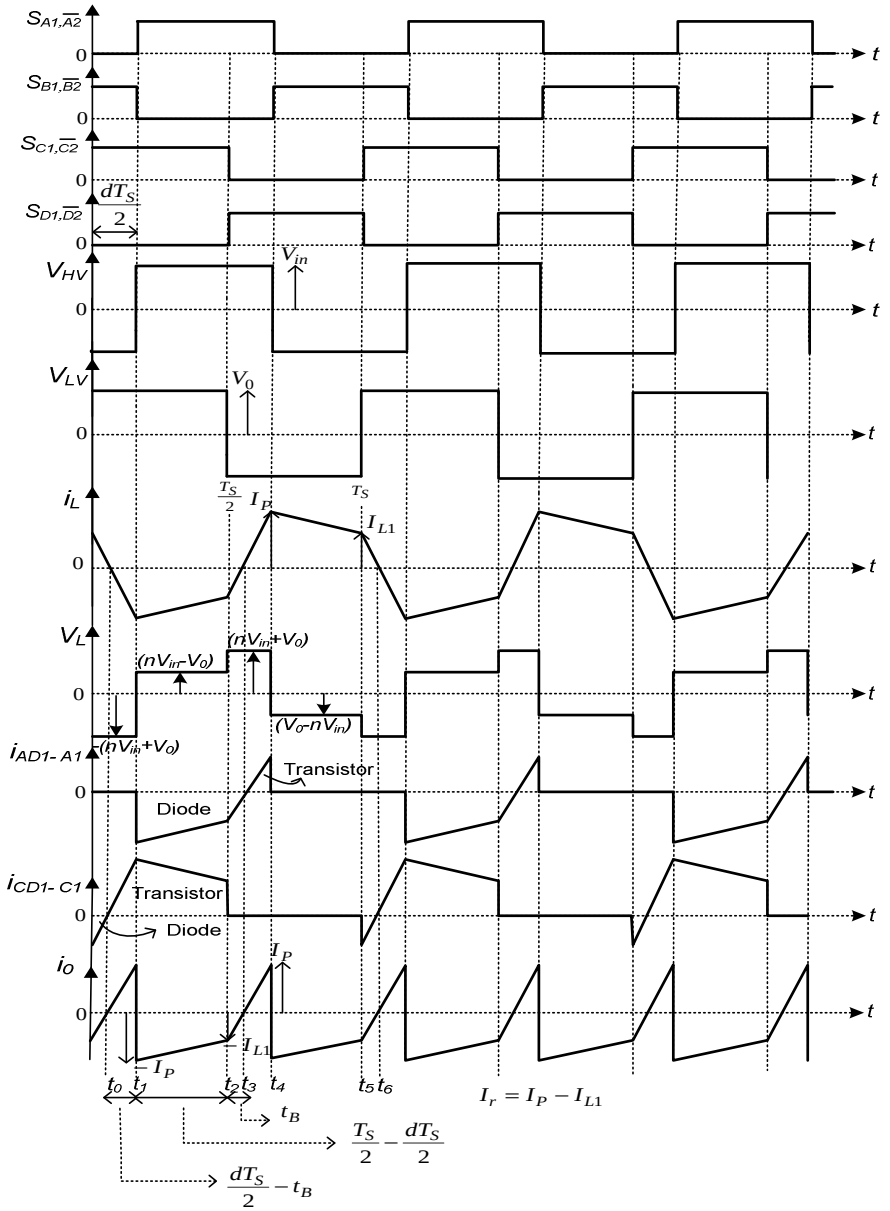


Figure 2.3 Ideal steady-state waveforms of the DAB converter during discharging mode

Maximum power transfer is achieved at a phase-shift of 90°, where the duty ratio is *d = 0.5*. High efficiency is obtained, since all devices operate under ZVS conditions over much of the load range. The circuit can achieve either step-up or step down voltage conversion depending upon the phase shift. During charging mode, the converter operates in buck mode to step down the aircraft power system voltage. On the contrary, the discharging mode steps up the voltage and the converter works in boost mode.

2.3 Steady-state analysis

This section presents a new waveform (steady-state) analysis of the DAB converter for charging and discharging modes. Equations for the device RMS and average currents, and the peak and RMS currents of the coupling inductor are derived, based on the assumption of lossless components and a piece-wise linear waveform for i_L. These equations are useful in predicting the losses that occur in the devices and passive components and allow a study of the converter characteristics. The difference between voltages of the two bridges appears across the coupling inductor and the inductor current changes with an essentially constant slope; this enables determination of the expressions for peaks of the inductor current at different switching instants.

2.3.1 Charging mode

During the charging mode, the peak-to-peak change in inductor current can be found by analysing the voltage across inductor L over a half cycle. Expressions are derived for the inductor current at the switching instants I_P and I_{L1} as follows. The notation used in the following analysis is indicated in Figure 2.4. Let V_L be the voltage across, and i_L the current flowing through, the inductor, L. The integral of voltage across the inductor over the first half cycle of Figure 2.4 is expressed as,

$$\int V_L dt = \left(nV_{in} + V_o\right)\frac{dT_S}{2} + \left(nV_{in} - V_o\right)\frac{\left[T_S - dT_S\right]}{2}$$

$$= \frac{nV_{in}T_S}{2} + V_oT_S\left(d - \frac{1}{2}\right)$$

where n is the transformer turns ratio. During this first half cycle, the inductor current changes from negative peak I_P to positive peak I_P.

Hence, the peak to peak change in inductor current is given by $I_{PP} = \frac{\int V_L dt}{L}$

$$\text{Hence,} \quad I_{PP} = \frac{T_S\left[V_0\left(2d-1\right)+nV_{in}\right]}{2L}$$

Therefore, peak inductor current which is the current at the HV switching instant is expressed as,

$$I_P = \frac{T_S}{4L}\left[V_0\left(2d-1\right)+nV_{in}\right] \tag{2.1}$$

In a similar manner I_{L1} is found to be:

$$I_{L1} = \left(\frac{nV_{in}+V_0}{L}\right)\left(\frac{dT_S}{2}\right) - I_P \tag{2.2}$$

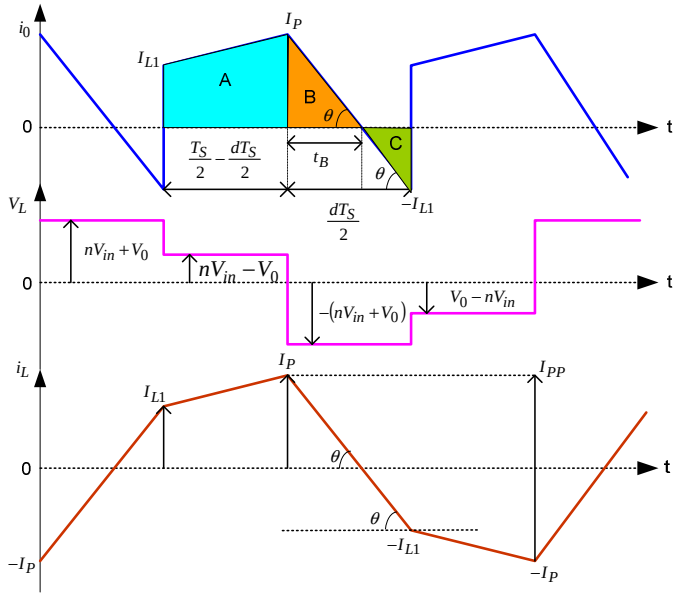


Figure 2.4 Voltage and current waveforms of the inductor during charging mode

Substituting (2.1) in (2.2) and simplifying further, the expression for the inductor current I_{L1}, which is the LV switching instant current is given by,

$$I_{L1} = \frac{T_S}{4L}\left[nV_{in}\left(2d-1\right)+V_0\right] \tag{2.3}$$

In order to find the average ultracapacitor current, an expression is required for the interval t_B; the time taken for i_L to fall from I_P to zero following the HV switching instant. Since the output current waveform is piece-wise linear, this can be calculated from the following,

$$\frac{I_P + I_{L1}}{\frac{dT_S}{2}} = \frac{I_P}{t_B} = \tan\theta \tag{2.4}$$

where θ is the angle marked on the i_0 and i_L current waveforms shown in Figure 2.4. The total current change during the interval $\frac{dT_S}{2}$, where the current is increased from -I_P to +I_{L1} can be written as,

$$I_P + I_{L1} = \left(\frac{nV_{in} + V_0}{L}\right)\frac{dT_S}{2} \tag{2.5}$$

Substituting (2.5) and (2.1) in (2.4) and simplifying to get an expression for t_B gives,

$$t_B = \frac{T_S\left[nV_{in} + V_0(2d-1)\right]}{4\left(nV_{in} + V_0\right)} \tag{2.6}$$

Using the above equations, the area under the i_0 current waveform shown as shaded regions *A*, *B* and *C* in Figure 2.4 is obtained. Since the waveform is periodic over half a cycle, dividing the area by the duration, which is $\frac{T_S}{2}$, gives the average output current of the DAB converter, which is given by,

$$I_o = \frac{A + B - C}{\frac{T_S}{2}} \tag{2.7}$$

Where,

$$A = \left(\frac{I_{L1} + I_P}{2}\right)\left(\frac{T_S - dT_S}{2}\right)$$

$$B = \frac{T_S\left[V_o(2d-1) + nV_{in}\right]}{8\left[nV_{in} + V_o\right]}I_P$$

$$C = \frac{1}{2}\times I_{L1}\left(\frac{dT_S}{2} - t_B\right) = \frac{dT_S I_{L1}}{4} - \frac{T_S\left[V_o(2d-1) + nV_{in}\right]}{8\left(nV_{in} + V_o\right)}I_{L1}$$

Substituting for *A*, *B* and *C* in (2.7) and simplifying, the expression for average output current can be derived as follows,

$$I_o = \frac{T_S nV_{in}}{2L}\left(d - d^2\right) \tag{2.8}$$

Normalising the average output current by the base value $\frac{T_S nV_{in}}{2L}$ gives,

$$I_o' = d - d^2 \tag{2.9}$$

Figure 2.5 shows the variation of normalised average output current with duty ratio. It can be observed from Figure 2.5 that the maximum power transfer is achieved at a phase-shift of 90°. Therefore, the maximum average output current occurs at a duty ratio of 0.5. For a particular power transfer there are two operating points, one on the left-hand-side and the other on the right-hand-side of Figure 2.5. The region on the left-hand-side of Figure 2.5 (where *d* varies from 0 to 0.5) has lower converter RMS and peak currents than the right-hand-side for the same amount of power transfer. For this reason it is preferable to operate with a value of d from 0 to 0.5. The RMS component of current is needed to estimate the conduction losses in the transformer/inductor windings and losses in the devices. The RMS value of inductor current and the output current i_0 can be derived using the HV and LV switching instant current expressions and their respective time intervals. Using these it is found that,

$$I_{RMS} = \sqrt{\frac{2}{T_S}\left[\frac{(I_{L1})^2\left(\frac{dT_S}{2}-t_B\right)}{3}+\left(\frac{T_S}{2}-\frac{dT_S}{2}\right)\left(I_{L1}{}^2+\frac{I_r{}^2}{3}+I_{L1}I_r\right)+\frac{I_P{}^2 t_B}{3}\right]} \tag{2.10}$$

Similarly, the RMS and average current equations for the devices on the HV and LV sides of the DAB converter can be derived from the waveforms shown in Figure 2.2 and are listed in Tables 2.3 and 2.4. The detailed step-by-step derivation of device RMS currents, output RMS current and inductor/transformer RMS current is presented in Appendix A.

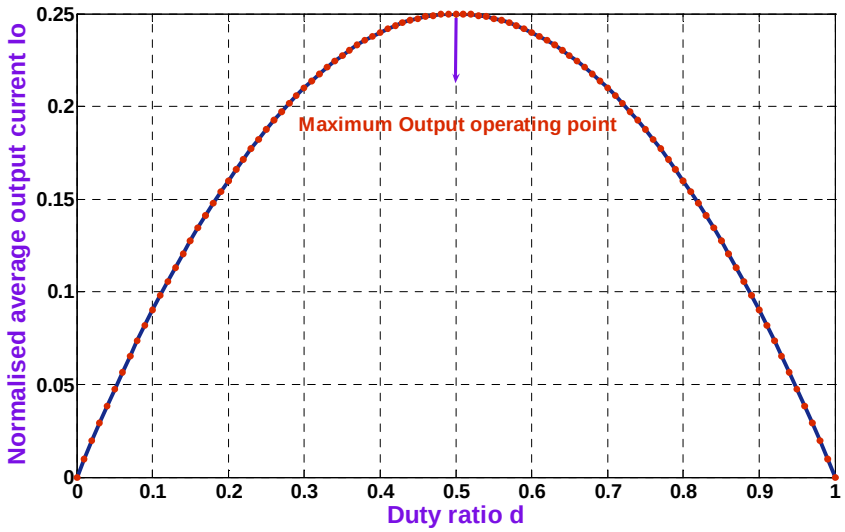


Figure 2.5 Normalised average output current vs Duty ratio

Table 2.3. Average current equations of devices in the DAB converter for charging mode (power transfer from the HV side to the LV side)

Device	Average current expression
HV side Transistor	$I_{avg}=\frac{\frac{1}{2}\times I_{L1}\times\left(\frac{dT_S}{2}-t_B\right)+\frac{1}{2}\times(I_{L1}+I_P)\times\left(\frac{T_S}{2}-\frac{dT_S}{2}\right)}{\frac{T_S}{2}-t_B}$
HV side Diode	$I_{avg}=\frac{\frac{1}{2}\times I_P\times t_B}{t_B}$
LV side Transistor	$I_{avg}=\frac{\frac{1}{2}\times I_{L1}\times\left(\frac{dT_S}{2}-t_B\right)}{\left(\frac{dT_S}{2}-t_B\right)}$
LV side Diode	$I_{avg}=\frac{\frac{1}{2}\times(I_{L1}+I_P)\times\left(\frac{T_S}{2}-\frac{dT_S}{2}\right)+\frac{1}{2}\times I_P\times t_B}{\left(\frac{T_S}{2}-\frac{dT_S}{2}+t_B\right)}$

Table 2.4. RMS current equations of devices in the DAB converter for charging mode (power transfer from the HV side to the LV side)

Device	RMS current equation
HV side Transistor	$I_{RMS}=\sqrt{\frac{1}{T_S}\left[\frac{(I_{L1})^2}{3}\times\left(\frac{dT_S}{2}-t_B\right)+\left(\frac{T_S}{2}-\frac{dT_S}{2}\right)\left({I_{L1}}^2+\frac{{I_r}^2}{3}+I_{L1}I_r\right)\right]}$
HV side Diode	$I_{RMS}=\sqrt{\frac{1}{T_S}\left[\frac{{I_P}^2}{3}\times t_B\right]}$
LV side Transistor	$I_{RMS}=\sqrt{\frac{1}{T_S}\left[\frac{(I_{L1})^2}{3}\times\left(\frac{dT_S}{2}-t_B\right)\right]}$
LV side Diode	$I_{RMS}=\sqrt{\frac{1}{T_S}\left[\left(\frac{T_S}{2}-\frac{dT_S}{2}\right)\left({I_{L1}}^2+\frac{{I_r}^2}{3}+I_{L1}I_r\right)+\frac{(I_P)^2 t_B}{3}\right]}$

2.3.1.1 Condition for ZVS:

The converter operating conditions to achieve virtually loss-less zero-voltage switching conditions are:

- At turn-on of any device, its anti-parallel diode is conducting and
- At turn-off of any device, the minimum current flow through the device is positive

In practice the zero-voltage switching limits will be imperfect since the inductor current must always be large enough to charge/discharge the device output capacitances at the switching instants.

By applying the zero-voltage switching conditions to the device current waveforms shown in Figure 2.2, the current at the LV switching instant must be greater than zero to achieve ZVS in the LV bridge. Therefore using (2.3), the following condition must be satisfied for ZVS in the LV bridge:

$$I_{L1} = \frac{T_S}{4L}\left[nV_{in}\left(2d-1\right)+V_0\right] \geq 0 \tag{2.11}$$

Solving for the inequality given in (2.11), the duty ratio at which ZVS occurs is obtained as,

$$d \geq 0.5 - \frac{V_0^{'}}{2} \tag{2.12}$$

where $V_0^{'} = \frac{V_0}{nV_{in}}$ is the normalised voltage conversion ratio. To achieve ZVS in the HV bridge, the current at the HV switching instant given in (2.1) must be positive. However, this condition is normally achieved and the limiting condition for ZVS is that given in (2.11).

Equation (2.11) is applicable when $V_0^{'} < 1$. If $V_0^{'} > 1$, the shape of the inductor current in Figure 2.2 will change and the effect of this is to interchange the expressions for the currents at the LV and HV switching instants. Therefore with $V_0^{'} > 1$ the expression for the LV switching instant current is given by (2.1) and the expression for the HV switching instant current is given by (2.3). The zero-voltage switching limit still occurs in the LV bridge, but is now given by requiring the current level in equation (2.1) to be greater than zero, which results in the condition:

$$d \geq 0.5 - \frac{1}{2V_0^{'}} \tag{2.13}$$

2.3.2 Discharging mode

When the converter operates in the discharging mode, power flows from the LV side to the HV side. A similar procedure is followed to that of the charging mode to derive the necessary equations. The voltage across the inductor L over a half cycle is analysed to determine the

peak-to-peak change in the inductor current. Then the expressions are derived for the inductor current at the switching instants I_P and I_{L1}. The notation used in the following analysis is indicated in Figure 2.6. The integral of voltage across the inductor over a half cycle is expressed as,

$$\int V_L dt = (nV_{in} + V_0)\frac{dT_S}{2} + (V_0 - nV_{in})\frac{[T_S - dT_S]}{2}$$

$$= \frac{T_S}{2}[V_0 + nV_{in}(2d-1)]$$

During this half cycle, the inductor current changes from negative peak I_{L1} to positive peak I_{L1}. Peak to peak change in the inductor current is $I_{L1PP} = \frac{T_S}{2L}[V_o + nV_{in}(2d-1)]$

The expression for the current at the LV switching instant I_{L1} can be found as,

$$I_{L1} = \frac{T_S}{4L}[V_o + nV_{in}(2d-1)] \tag{2.14}$$

Solving for the HV switching instant current based on the current slope during the interval $\frac{dT_S}{2}$ gives,

$$I_P = \frac{T_S}{4L}[nV_{in} + V_o(2d-1)] \tag{2.15}$$

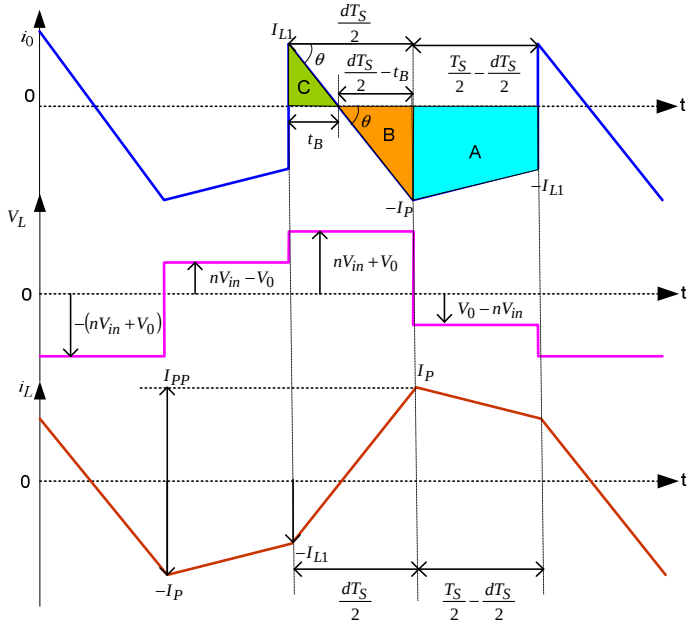


Figure 2.6 Voltage and current waveforms of the inductor during discharging mode

In order to find the average ultracapacitor current, an expression is required for the interval t_B; the time taken for i_L to fall to zero following the LV switching instant. Since the i_0 current waveform is piece-wise linear, this can be calculated from the following,

$$\frac{I_P + I_{L1}}{\frac{dT_S}{2}} = \frac{I_{L1}}{t_B} = \tan\ \theta \tag{2.16}$$

where θ is the angle marked on the i_0 current waveform shown in Figure 2.6. The total current change during the interval $\frac{dT_S}{2}$, where the current is increased from $-I_{L1}$ to $+I_P$ can be written as,

$$I_P + I_{L1} = \left(\frac{nV_{in} + V_0}{L}\right)\frac{dT_S}{2} \tag{2.17}$$

Substituting (2.14) and (2.17) in (2.16), then solving for t_B gives,

$$t_B = \frac{T_S\left[V_o + nV_{in}(2d-1)\right]}{4\left(nV_{in} + V_o\right)} \tag{2.18}$$

Using the above equations, the area under the i_0 current waveform shown as shaded regions *A*, *B* and *C* in Figure 2.6 is obtained. Since the waveform is periodic over half a cycle, dividing the area by the duration, which is $\frac{T_S}{2}$, gives the average output current of the DAB converter, which is given by,

$$I_o = \frac{C - A - B}{\frac{T_S}{2}} \tag{2.19}$$

Where the areas *A*, *B*, and *C* in the above figure are computed as,

$$A = \left(\frac{I_{L1} + I_P}{2}\right)\left(\frac{T_S - dT_S}{2}\right)$$

$$B = \frac{1}{2}I_P\left(\frac{dT_S}{2} - t_B\right)$$

$$C = \frac{t_B I_{L1}}{2}$$

Substituting the expressions for *A*, *B*, and *C* in (2.19) and deducing the equation for average ultracapacitor current, which may be expressed as,

$$I_o = \frac{T_S\, nV_{in}}{2L}\left(d^2 - d\right) \tag{2.20}$$

The normalised average ultracapacitor current, as a ratio of the base value $\frac{nV_{in}T_S}{2L}$ is,

$$I_o' = d^2 - d \tag{2.21}$$

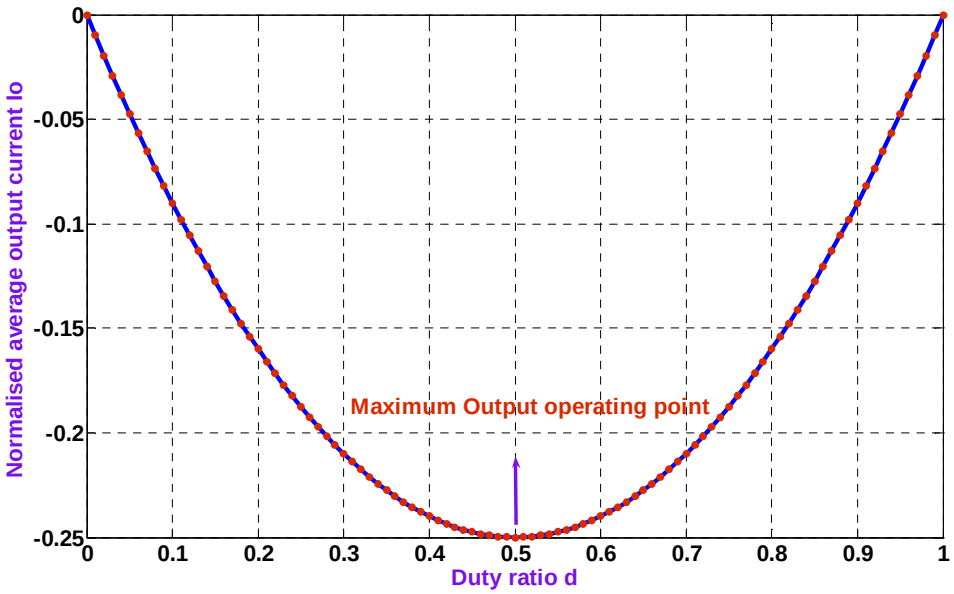


Figure 2.7 Variation of normalised average output current vs duty ratio during discharging mode

From Figure 2.7, it is clear that the maximum power transfer is achieved at a duty ratio of 0.5 during the discharging mode of ultracapacitor. The RMS value of inductor current and output current i_0 can be derived using the HV and LV switching instant current expressions and their respective time intervals, which result in,

$$I_{RMS} = \sqrt{\frac{2}{T_S}\left[\frac{I_P^2}{3}\left(\frac{dT_S}{2} - t_B\right) + \left(\frac{T_S}{2} - \frac{dT_S}{2}\right)\left(I_P^2 + \frac{I_r^2}{3} - I_P I_r\right) + \frac{I_{L1}^2 t_B}{3}\right]} \tag{2.22}$$

A detailed derivation of inductor/transformer RMS current during the discharging mode is given in Appendix A.

From the analysis for the discharging mode, it can be observed that the corresponding expressions for the currents at the HV and LV switching instants, I_P and I_{L1} respectively in (2.1)

and (2.3) are unchanged. However in the expressions for i_0, the LV-side terminal current, given by equations (2.8) and (2.9), the $\left(d-d^2\right)$term is replaced by $\left(d^2-d\right)$. Also, the expressions for the transistor and diode currents will be interchanged in Tables 2.3 and 2.4. For example, the expression for the HV side transistor current becomes the expression for the LV side transistor with I_P, I_{L1} replaced by I_{L1}, I_P respectively.

2.3.2.1 Condition for ZVS:

When the converter operates in the discharging mode and power transfers from the LV side to the HV side, the zero-voltage switching limit is again found to occur in the LV bridge and may again be expressed by (2.11), (2.12) and (2.13).

2.4 Effect of snubber capacitor

Although the turn-on of transistors is achieved at minimum (near-zero) positive diode current, the instantaneous transistor currents that occur during the turn-off process are significant. Hence, minimal transistor currents during the turn-off switching time instant are mandatory in order to achieve low switching losses. To limit switching transients, reduce current/voltage spikes and minimise electromagnetic compatibility (EMC) problems associated with high *dv/dt*, snubbers are placed across the switching devices [174-178]. In order to enhance the converter performance and minimise switching losses, snubber capacitors, C_s, have been introduced across all the switches in the DAB converter circuit, see Figure 2.8. Due to the similarity of the transistor switching instants, only one transistor (A_1) turn-off instant for the HV bridge side and one transistor (C_1) turn-off instant for the LV bridge side will be described.

2.4.1 Device turn-off process

In the absence of a snubber capacitor across the device during turn-off, resonance would naturally occur between device output capacitance and the coupling inductance. The energy stored in the coupling inductance would be sufficient to ensure charge/discharge of device output capacitances at the switching instants. Normally, the device output capacitance is of low value and would not be enough to produce a low *dv/dt*. As a result, there would be a high rate of initial current fall (*di/dt*) with a rapid voltage rise (*dv/dt*) across the device, during turn-

off. This produces turn-off switching loss and device stress. If stray inductance is present in the circuit, this can result in a device over voltage.

Simple snubber capacitors were used to reduce the turn-off switching loss of the devices. These capacitors slow down the rate of voltage rise across the devices so that a lower voltage appears during the current decay time. Figure 2.8 shows the schematic of the DAB converter with snubber capacitors C_s across all the devices. These capacitors are identified with the subscript of their respective parallel devices. The effect of the added snubber capacitors during device turn-off is explained in the following paragraphs, starting with the HV device turn-off and followed by the LV device. Two devices are turned-on or turned-off at any switching instant in each case. Hence, an explanation is provided for one device with the other device details in brackets.

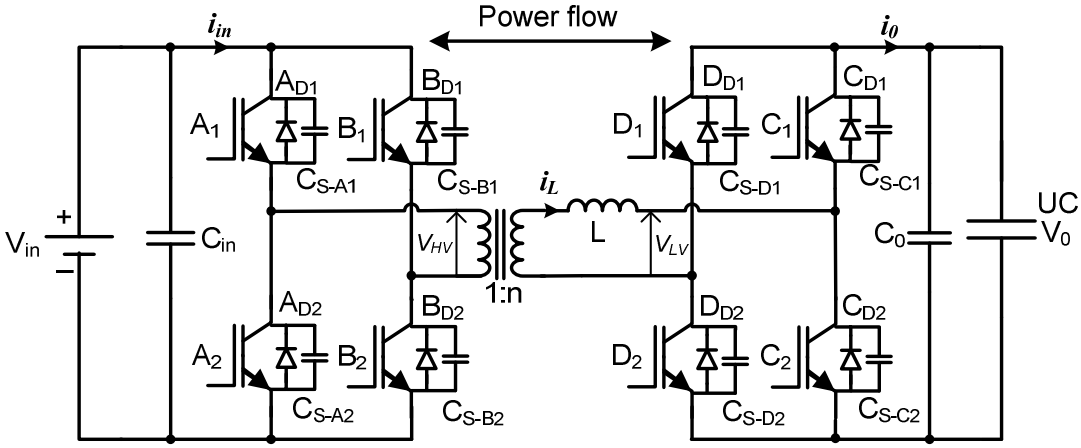


Figure 2.8 Schematic of the DAB DC-DC converter with loss-less snubber

Assuming that initially transistor A_1 (B_2) is on and forward current flows through the device during the on-state. The snubber current is zero and the snubber capacitor $C_{s\text{-}A1}$ ($C_{s\text{-}B2}$) is uncharged. Now transistor A_1 (B_2) stops conducting and all the other devices are not in conduction. The turn-off time of the device is considered to be negligible, and the value of snubber capacitor is sufficiently high to ensure very little change in the voltage across the transistor during its turn-off time. Without the capacitor, the voltage across transistor A_1 (B_2) would rapidly rise to V_{in} with high *dv/dt*. If parasitic inductance is present, this may lead to a device over voltage. The snubber reduces this high *dv/dt* by conducting the device turn-off

current. Therefore, during the device A_1 (B_2) turn-off, the current in coupling inductor *L* discharges $C_{s\text{-}A2}$ ($C_{s\text{-}B1}$) and charges $C_{s\text{-}A1}$ ($C_{s\text{-}B2}$) in a resonant manner until their respective voltages reach the opposite rails, at which point, if the current is still positive, diode A_{D2} (B_{D1}) turns on, clamping the voltage across $C_{s\text{-}A2}$ ($C_{s\text{-}B1}$) to zero and that of $C_{s\text{-}A1}$ ($C_{s\text{-}B2}$) to V_{in}.

The upper devices in each leg are switched in anti-phase with the lower devices of the same leg. However, there is a short period after a transistor in a leg turns off before the other transistor in the leg is turned on. This period is termed as a dead-time. The dead-time should be longer than the snubber charging time to prevent high current pulses. Hence, after the dead time, a gate drive signal is applied to A_2 (B_1); later current is transferred from A_{D2} (B_{D1}) to A_2 (B_1) under ZVS. This is depicted in Figure 2.9 for the turn-off instant of transistors A_1 and B_2. Figure 2.9 depicts simulations of the voltage across and current flowing through all the HV side devices, and the charging/discharging current of HV side snubbers.

Similarly, in the LV bridge, assume that transistor C_1 (D_2) is on, forward current flows through the transistor and the snubber current is zero. Thus the capacitor $C_{s\text{-}C1}$ ($C_{s\text{-}D2}$) is discharged. When transistor C_1 (D_2) stops conducting, the snubber capacitor reduces the high *dv/dt* by conducting the current. Thereby the current in the coupling inductor *L* discharges $C_{s\text{-}C2}$ ($C_{s\text{-}D1}$) and charges $C_{s\text{-}C1}$ ($C_{s\text{-}D2}$) in a resonant manner. As a result, their respective voltages reach the opposite rails. Now, if the current is still positive, diode C_{D2} (D_{D1}) turns on clamping the voltage across $C_{s\text{-}C2}$ ($C_{s\text{-}D1}$) to zero and that of $C_{s\text{-}C1}$ ($C_{s\text{-}D2}$) to V_0. The gate control signal is applied after the dead-time duration to C_2 (D_1); hence, current is transferred from C_{D2} (D_{D1}) to C_2 (D_1) under ZVS. The switching instant of transistors C_1 and D_2 can be observed in the simulation of Figure 2.10.

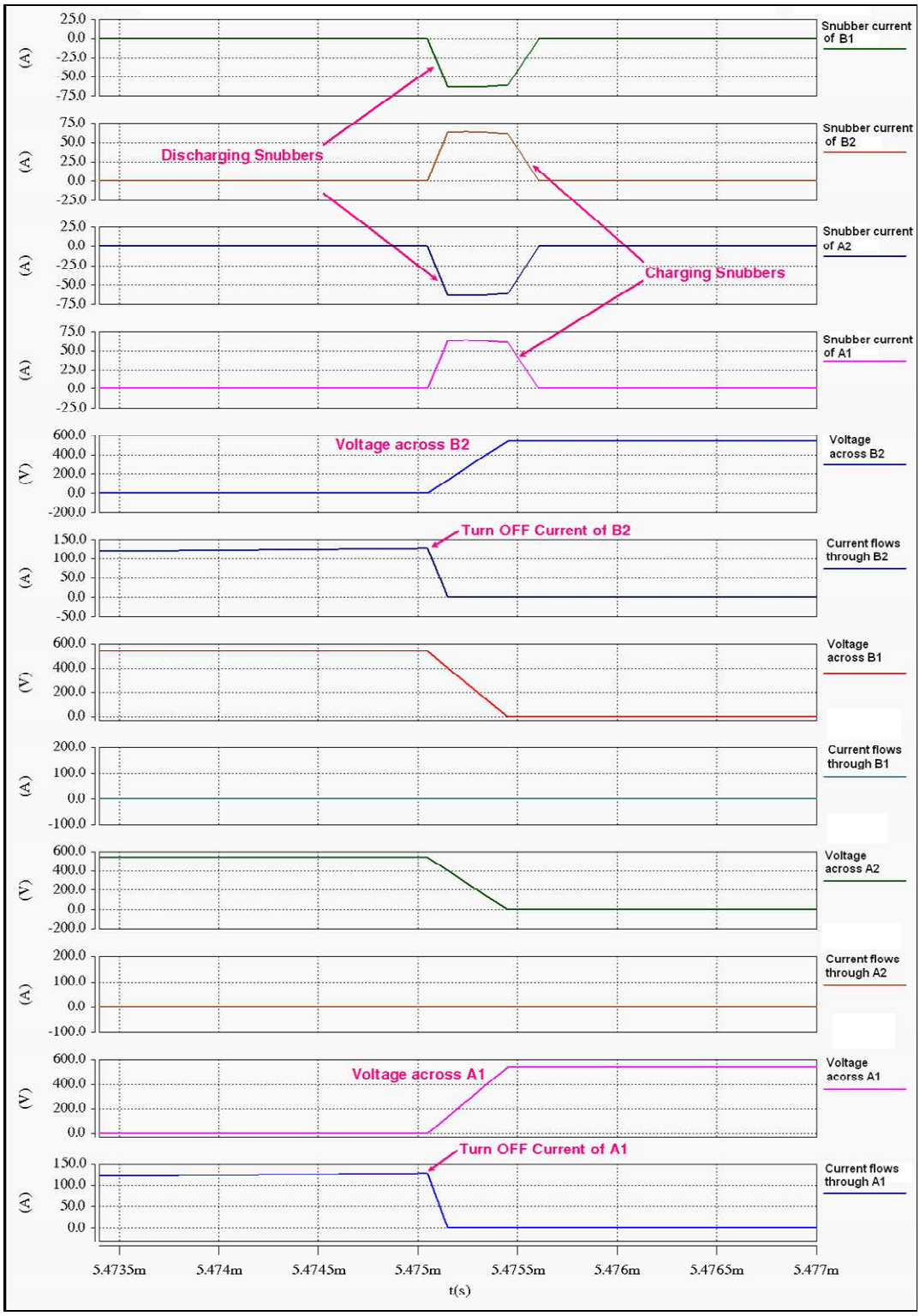


Figure 2.9 Turn-off of transistor A_1 and B_2 at d = 0.5, V_{HV} = 540V, V_{LV} = 62.5V, L = 2.11µH, C_s = 47nF, I_{OFF} = 128A, f_s = 20 kHz

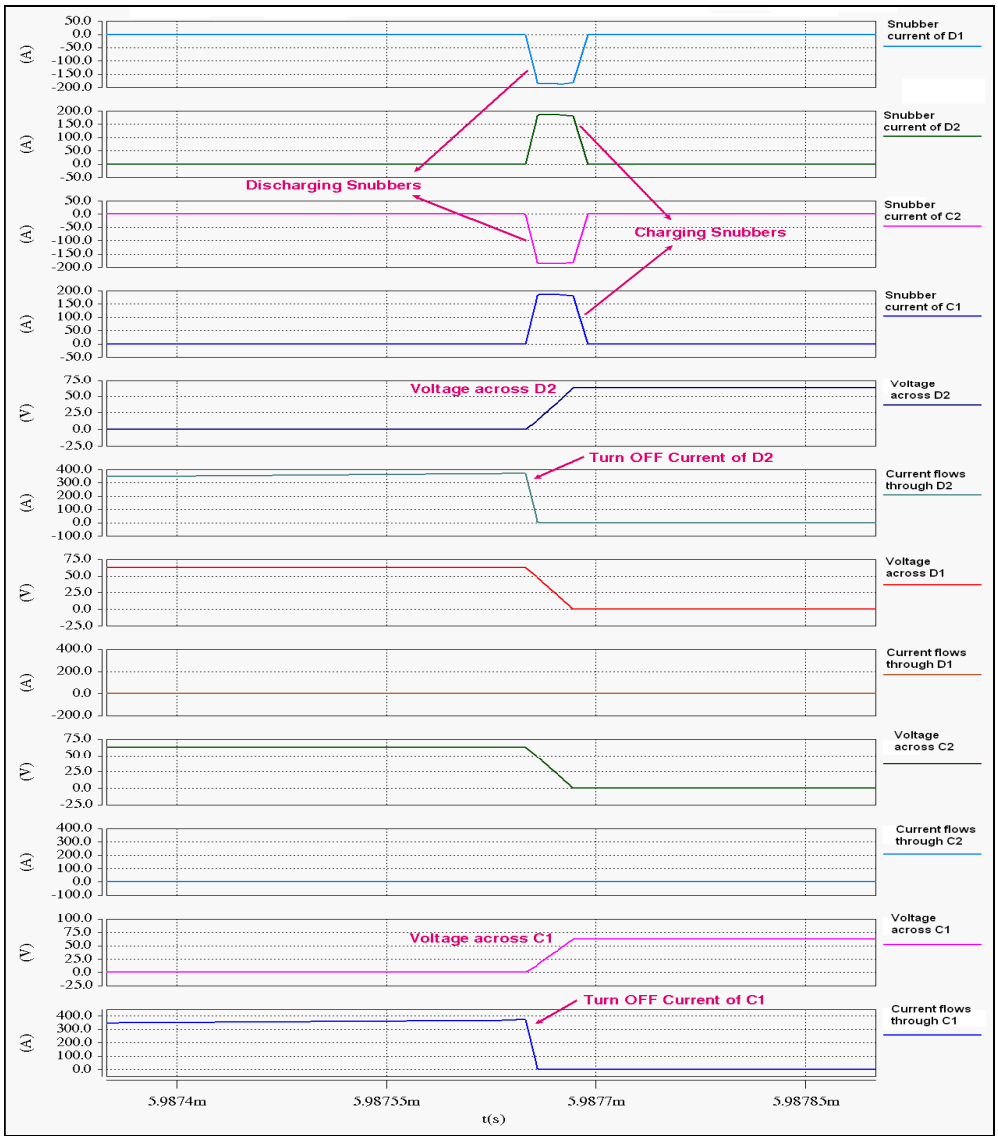


Figure 2.10 Turn-off of transistor C_1 and D_2 at d = 0.5, V_{HV} = 540V, V_{LV} = 125V, L = 2.11µH, C_s = 100nF, I_{OFF} = 371A, f_s = 20 kHz

The snubber capacitor allows device current to fall before the device voltage rises significantly, during the switching period; thereby it minimises the turn-off switching loss. It limits the rise time of voltage across the transistor during turn-off. This limitation of *dv/dt* can be observed on the inclined edges of transistor voltage waveform shown in Figures 2.9 and 2.10. Hence, all the devices turn-on and turn-off under ZVS with reduced stress. Figures 2.11 and 2.12 show the turn-off power and energy losses of transistors A_1 and C_1, with and without snubber capacitors. Waveforms of inductor current i_L, voltages generated by the two full

bridges V_{HV} on the HV side and V_{LV} on the LV side, device voltages V_{A1}, V_{C1} and current flowing through the transistors i_{A1}, i_{C1} along with respective turn-off power and energy loss are displayed.

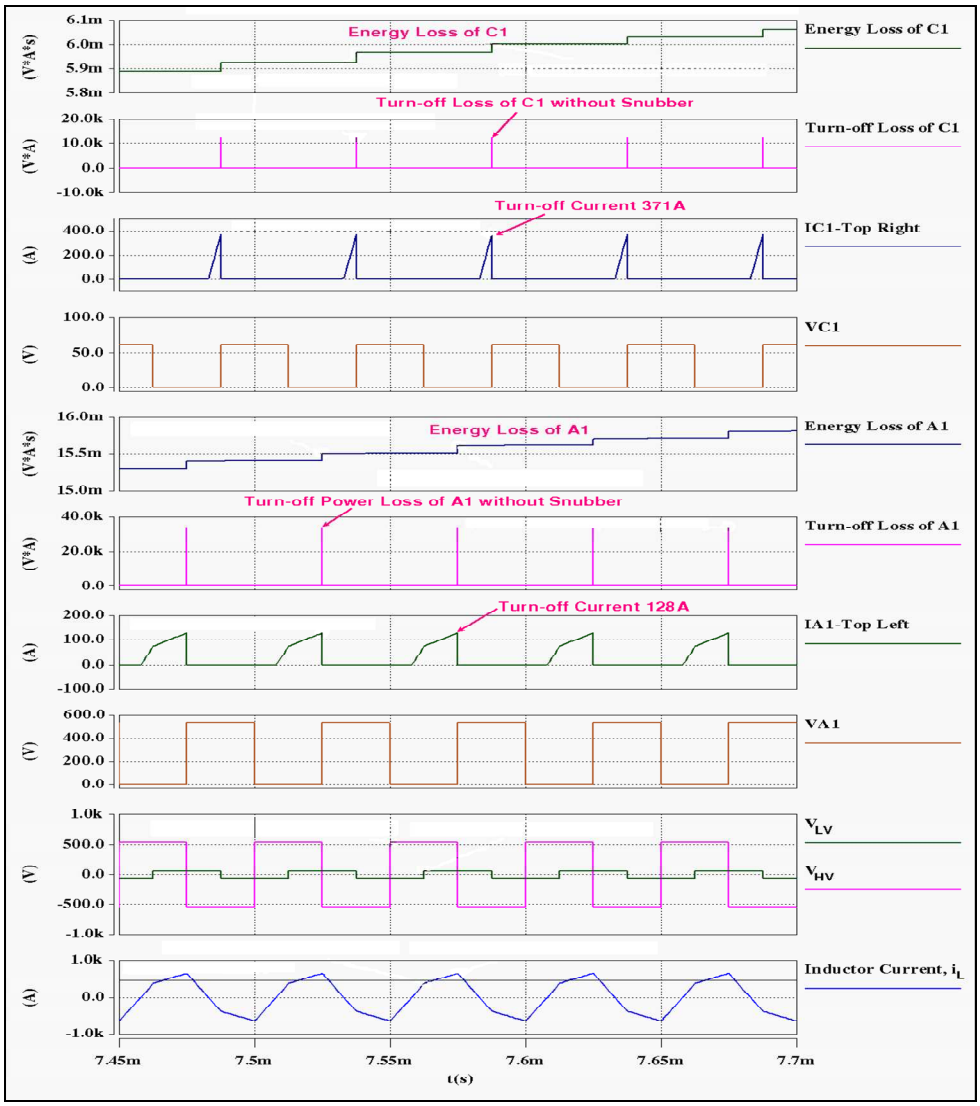


Figure 2.11 Turn-off power and energy loss of A_1 and C_1 without snubber at d=0.5, V_{HV} = 540V, V_{LV} = 62.5V, L=2.11µH, f_s = 20 kHz, P_0 = 20kW, I_0 = 320A

These Figures show that the turn-off power loss across transistors A_1 and C_1 during the switching instant is significantly reduced due to the snubber. The switching energy loss was computed by integrating the instantaneous switching loss per device, and the average power loss was obtained by multiplying the energy loss per cycle with the switching frequency of 20 kHz.

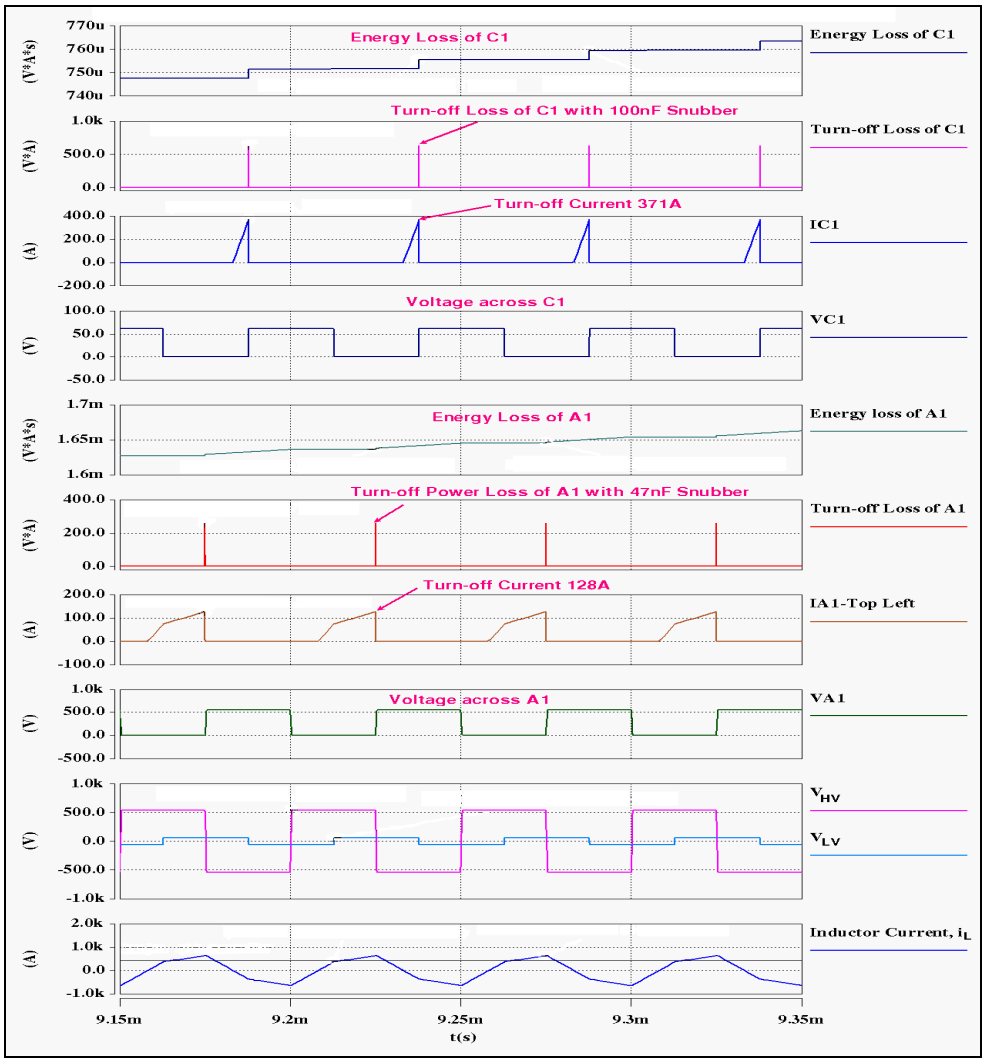


Figure 2.12 Turn-off power and energy loss of A_1 with C_s = 47nF and C_1 with C_s = 100nF snubber at d = 0.5, V_{HV} = 540V, V_{LV} = 62.5V, L = 2.11µH, f_s = 20 kHz, P_0 = 20kW, I_0 = 320A

The simulation component values are typical of likely future aerospace systems [17, 45] at the HV side and the capabilities of ultracapacitor modules at the LV side. The key component values of the converter are determined by applying the worst case operation (i.e. maximum power, minimum voltage operation) to the equations derived from the steady-state analysis. The turns ratio is chosen as 1:1/5, for which the maximum ZVS operating region is obtained. From (2.8), the coupling inductance is calculated as 2.11µH for the worst-case scenario of maximum power and minimum ultracapacitor voltage. At this operating condition *d* was assumed to be 0.5. The SABER simulation circuit along with all parameters is shown in Figure A.3 of Appendix A, page 273.

2.4.2 Minimum current requirement for ZVS

The influence of the snubber capacitor value on the minimum inductor current requirement during turn-off is investigated here. Although snubber capacitors suppress voltage transients during switching, inclusion of a snubber across the switching transistors requires more energy be stored in the coupling inductance to achieve soft switching [87]. An analysis was performed by assuming that the input (HV) and output (LV) voltages are constant during the transistor turn-off instants, to estimate the minimum current necessary during turn-off to achieve ZVS. The transistor turn-off switching instant is shown in the inductor voltage and current waveforms of Figure 2.13. A simplified equivalent circuit of the converter during transistors A_1 and B_2 turn-off is illustrated in Figure 2.14. The LV bridge is replaced by a primary-referred voltage source V_0', with the required polarity shown. The coupling inductor is also referred to the HV side of the transformer as L'.

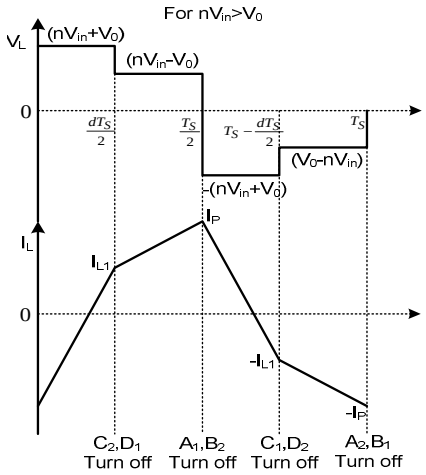


Figure 2.13 Inductor voltage and current waveforms indicating turn-off instants of transistors

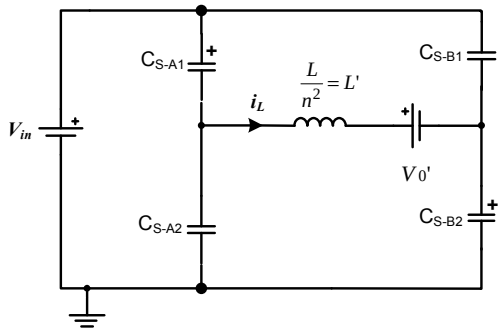


Figure 2.14 Turn-off equivalent circuit of the DAB converter HV bridge during A_1 and B_2 turn-off

From this equivalent circuit, it can be seen that each leg has two identical snubber capacitors ($C_{s\text{-}A1} = C_{s\text{-}A2} = C_s$) in parallel, one capacitor being charged and the other discharged at the time of transistor turn-off. Therefore the effective capacitance per leg is $2C_s$. The capacitors and effective inductor in the circuit resonate during turn-off to achieve ZVS. The current flows in both legs during resonance. Thus, the effective capacitance is C_s. The frequency of resonance should be much higher than the circuit operating frequency to ensure ZVS. The frequency of the snubber capacitor and inductor circuit is given by, $\omega = \frac{1}{\sqrt{L' C_S}}$ (2.23)

where ω is the angular frequency in radians per second. Although the equivalent circuit is drawn for transistors A_1 and B_2, the same circuit is applicable for any transistor turn-off instant under ZVS. During the turn-off instant of transistors A_1 and B_2, the current flow through the inductor charges the snubber capacitors $C_{s\text{-}A1}$ and $C_{s\text{-}B2}$ and discharges snubbers $C_{s\text{-}A2}$ and $C_{s\text{-}B1}$. Therefore, the inductor current $I_L = I_{A1-CS} + I_{A2-CS}$. Assuming the snubber capacitors all have the same value,

$I_{A1-CS} = I_{A2-CS} = I_{CS}$, and hence,

$I_{CS} = \frac{I_L}{2}$, and so $I_L = 2I_{CS}$

Instantaneous current flow through the effective capacitance is given by,

$I_{CS} = C_S \frac{dV_{CS}}{dt}$,

Therefore, the inductor current can be written as,

$$I_L = 2C_S \frac{dV_{CS}}{dt} \quad (2.24)$$

Neglecting losses, the limit of successful ZVS occurs when the inductor energy is just sufficient to charge/discharge the capacitors to the required final voltage. Hence,

$\frac{1}{2} L' {I_L}^2 = EC_S$, where EC_S is the energy delivered to the capacitor. This is given by,

$$EC_S = \int_0^{t_{0ff}} V_0' i_L dt$$

Substituting for $i_{L,}$

$$= \int_0^{t_{0ff}} V_0' \left(2C_S \frac{dV_{CS}}{dt} \right) dt$$

$$= 2C_S V_0' \int_0^{t_{0ff}} \left(\frac{dV_{CS}}{dt} \right) dt$$

$$= 2C_S V_0' \int_0^{t_{0ff}} dV_{CS}$$

Replacing the change in voltage during the switching transition gives,

$$EC_S = 2C_S V_0' V_{in} \tag{2.25}$$

To achieve ZVS, energy stored in the inductor must equal the energy delivered, to charge and discharge the snubber and device output capacitances. Therefore, the condition for ZVS is given as,

$$\frac{1}{2} L' I_L{}^2 = 2C_S V_0' V_{in}$$

Thus,

$$I_L{}^2 = \frac{4C_S V_0' V_{in}}{L'}$$

and $I_L = 2\sqrt{\frac{C_S V_0' V_{in}}{L'}}$

Rearranging to form an expression for the minimum inductor current during turn-off,

$$I_L = 2\sqrt{\frac{V_0' V_{in}}{L' / C_S}} \tag{2.26}$$

$$I_L = 2\frac{\sqrt{V_0' V_{in}}}{Z}, \tag{2.27}$$

Where $Z = \sqrt{L' / C_S}$

Thus the inductor current should be greater than or equal to the value of I_L in equation (2.26) during transistor turn-off to achieve ZVS.

2.4.3 ZVS operating region

From the above analysis, it is clear that in order to achieve soft switching, the minimum inductor current required must equal the value obtained from (2.26) during device turn-off to benefit from ZVS operation. Although inclusion of snubber capacitors decreases the device switching losses, the minimum current required during turn-off restricts the output voltage and output current region available for soft-switching operation. Figure 2.15 illustrates the ZVS operating region of the DAB converter with and without snubber capacitors.

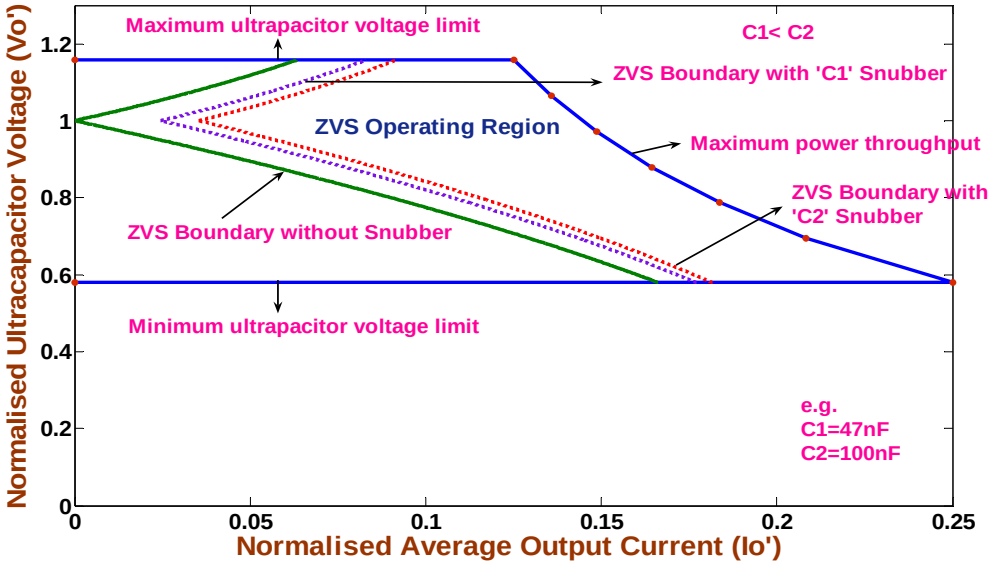


Figure 2.15 ZVS operating region of the DAB converter with and without snubber

The turns ratio is chosen as 1:1/5, for which the maximum ZVS operating region is obtained. The maximum and minimum ultracapacitor voltage limits are obtained by assuming a 2:1 working range for the ultracapacitor voltage. Dividing the ultracapacitor voltage by *nVin* gives the normalised ultracapacitor voltage. Figure 2.15 depicts the range of normalised ultracapacitor voltage over the range of normalised average output current. The region between the blue lines depicts the operating region of the converter, which is set by the ultracapacitor voltage limits and the maximum power throughput. The green line illustrates the ZVS boundary of the converter without snubber capacitors. The region within the green lines and constant power line indicates the soft switching region of the DAB converter. To illustrate the effect of snubber on the ZVS operating region, the effect of C_1 (e.g. 47nF) and C_2 (e.g.

100nF) snubbers are considered, where $C_1 < C_2$. The dotted violet line shows the ZVS boundary for C_1 snubber capacitors across all switching devices and the dotted red line represents the ZVS boundary for C_2 snubber capacitors across all switching devices. It is evident from Figure 2.15 that increasing the value of the snubber capacitors decreases the soft-switching region of the converter. In practice, ZVS boundary limits are slightly different due to the requirement of the inductor current to be sufficient to charge and discharge the device output capacitances at the switching instants.

The ZVS boundaries are obtained from the analysis for the HV and LV side operating voltages. Equations (2.12) and (2.13) were used to obtain the green line boundary. The violet and red line boundaries were obtained by estimating the duty ratio at which the minimum current requirement without snubber (2.11) equals the minimum current requirement with snubber (2.26).

2.5 Simulation results

To validate the equations derived in section 2.3 detailed simulations were carried out using SABER. This section presents simulation results of the DAB converter for charging and discharging modes of the ultracapacitor. The simulation results are for a 20kW DAB converter; the practical design of the converter will be described in the next Chapter. Operating conditions and circuit parameters corresponding to the simulations are given in the Figure captions. Figure 2.16 shows SABER simulation waveforms for the charging mode of the ultracapacitor. Figure 2.16 depicts the voltages generated by the two full-bridges, V_{HV} on the HV side and V_{LV} on the LV side, the current flowing through the coupling inductance $i_{L,}$ the device currents on the HV side i_{A1} ,i_{AD1} and the device currents on the LV side $i_{C1,}$ i_{CD1} , the HV side terminal current i_{in} and the LV side terminal current i_0.

Equations (2.1) and (2.3) corresponding to the steady-state analysis during charging mode are applicable when $V_0^{'} < 1$ for the HV and LV switching instants respectively. For a voltage conversion ratio greater than one ($V_0^{'} > 1$), during the charging mode, the shape of the inductor current in Figure 2.2 will change and the effect of this is to interchange the expressions for the currents at the LV and HV switching instants. Therefore, with $V_0^{'} > 1$ the

expression for the LV switching instant current is given by (2.1) and the expression for the HV switching instant current is given by (2.3). For V_{HV} = 540V, n =1: 0.2, V_{LV} = 125V, the voltage conversion ratio is 1.16. Therefore, from the theoretical analysis, the expected steady-state values are calculated as I_P = 288.13A, I_0 = 159.96A, I_{L1} = 116.15A, I_{RMS} = 196.51A. These values correlate well with the SABER results. Figure 2.17 presents simulation results for the discharging mode of operation. Again, the measurement results from SABER simulation confirm the values obtained through analysis, which are I_P = 640A, I_0 = -320A, I_{L1} = 370.37 and I_{RMS} = 426.92A.

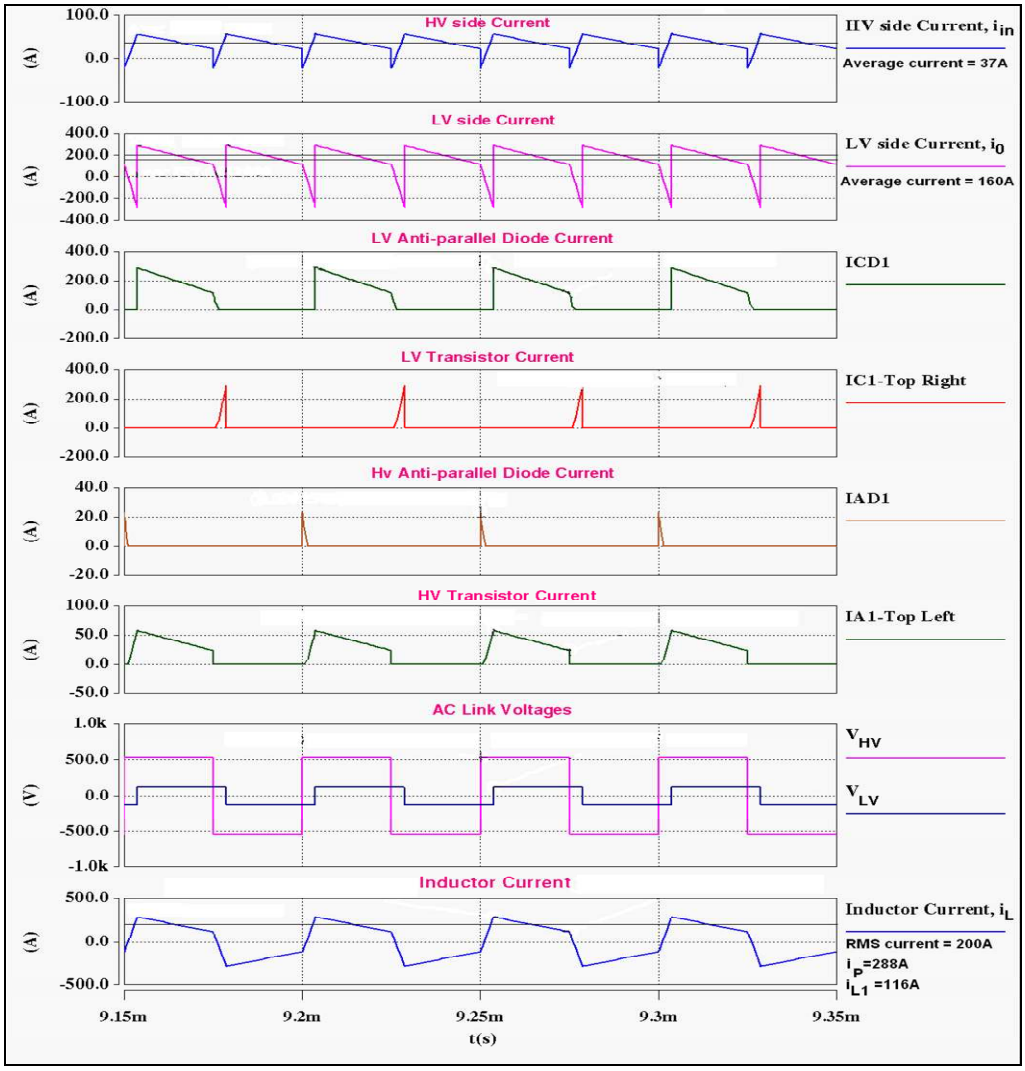


Figure 2.16 Simulation results of the DAB converter during charging mode
V_{HV} = 540V, n =1: 0.2, V_{LV} = 125V, d = 0.146, P_0 = 20kW, I_0 = 160A, f_s = 20kHz, L = 2.11µH

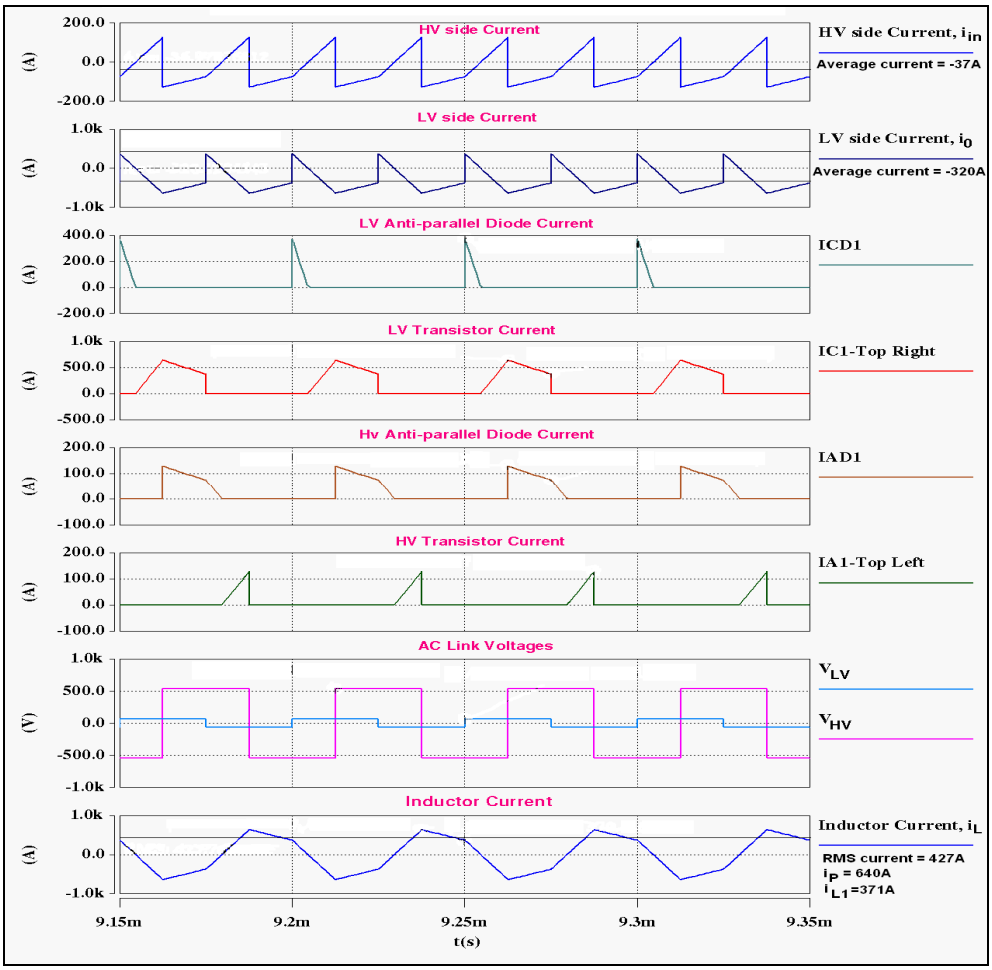


Figure 2.17 Simulation results of the DAB converter during discharging mode
V_{HV} = 540V, n = 1: 0.2, V_{LV} = 62.5V, d = 0.5, P_0 = 20kW, I_0 = 320A, f_s = 20kHz, L = 2.11µH

Figure 2.18 depicts the ZVS boundary waveforms of the converter with 100nF snubber capacitors. Figure 2.18 shows the voltages generated by the two full-bridges V_{HV} and V_{LV}, the current flowing through the coupling inductance i_L, the device currents on the LV side i_{C1}, i_{CD1}, the LV side device voltage V_{C1}, the charging and discharging snubber currents of transistors C_1 and C_2. Based on the theoretical analysis, the expected steady-state values during ZVS boundary operation are, I_0 = 232.54A, I_{L1} = 35.78A, I_P = 446.37A and I_{RMS} = 263.87A. Once again the steady-state analysis values are found to be in close agreement with the simulation results. From Figure 2.18, the instantaneous value of inductor current during device turn-off is found to be 35.78A, which is also the minimum current requirement necessary to achieve ZVS with 100nF snubber as estimated by analysis in section 2.4.2, thus demonstrating the accuracy of the analysis.

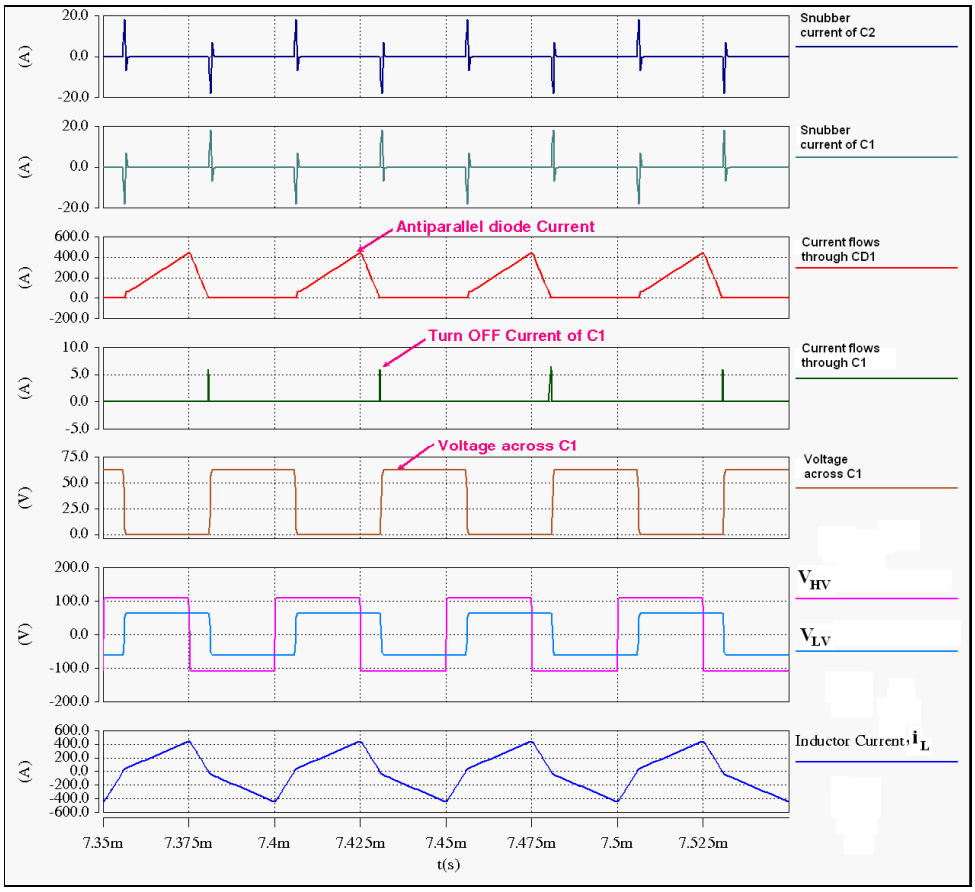


Figure 2.18 Simulation results for ZVS boundary of the DAB converter during charging mode with 100nF snubber
V_{HV} = 540V, n = 1: 0.2, V_{LV} = 62.5V, d = 0.2386, P_0 = 14.5kW, I_0 = 232A, f_s = 20kHz, L = 2.11µH

2.6 Summary

This Chapter has presented a novel steady-state analysis for the DAB converter. The expressions for the average and RMS device currents along with the peak and RMS currents of the coupling inductor were obtained through analysis. These equations are useful during the practical design of the converter prototype. The operation of the DAB DC-DC converter has been verified through extensive simulations, confirming the accuracy of the analysis. The snubber capacitor influence is analysed and the minimum current required to operate the converter in soft-switching region has been derived. ZVS operating region of the converter implies that, although the turn-off snubber is used to suppress the switching transients and reduce the device switching losses, it also reduces the effective region available for soft-switching. The simulation results effectively match that obtained using theoretical analysis.

Chapter 3

Design and Implementation of DAB DC-DC Converter

3.1 Introduction

This chapter presents the design and construction of a DAB converter prototype, to validate the simulation and mathematical analysis presented in this Thesis. The prototype design specifications are followed by a description of the components selection procedure, where the method of selecting power semiconductor devices based on prediction of device losses for the target specification is discussed in detail. Since the converter has two stages viz. DC-AC and AC-DC to perform DC-DC conversion, two sets of appropriate power semiconductor devices must be chosen to achieve power conversion on both HV and LV sides in addition to a careful design and selection of other converter components. The converter layout is then presented describing the design of planar bus bars for HV and LV bridge converters. Next, the selection of a suitable gate driver and its associated circuit design is described followed by a discussion of interfacing/signal conditioning circuit designs.

3.2 Prototype design specifications

The performance specification of the DAB converter prototype is listed in Table 3.1. These figures are typical of likely future aerospace systems [179] at the HV side and the capabilities of ultracapacitor modules at the LV side.

Table 3.1 Design specification of the DAB converter prototype

Performance parameter	Rating
Maximum power output	20kW
Nominal input (HV) voltage	540V
Output (LV) voltage	62.5V – 125V
Switching frequency	20kHz
Maximum input ripple voltage	<2%
Maximum output ripple voltage	<5%

3.3 Components selection

Assuming a 2:1 working range for the ultracapacitor voltage, the worst case operating condition of the converter is V_{HV} = 540V, V_{LV} = 62.5V, inductor RMS current I_{RMS} = 427A, peak inductor current I_P = 640A, average ultracapacitor current I_0 = 320A and power throughput P_0 = 20kW, where d = 0.5. The key component values of the converter are determined by applying the worst case operating condition to the equations derived from the steady-state analysis.

3.3.1 Selection of power semiconductor devices

Selection of power modules for a critical application is subject to consideration of the current carrying capacity under realisable cooling conditions and with reference to the switching frequency and safe operating areas (SOA). Under no circumstances should the maximum ratings of the device blocking voltage, peak current, junction temperature and SOA indicated in the datasheet be exceeded [180, 181, 182]. This section describes the selection of appropriate power semiconductor devices. The emphasis here is on estimation of device conduction and switching power losses. The key parameters and characteristic curves depicted in the datasheets, which are of primary importance, are discussed. In order to select the suitable power devices, a power loss calculation was performed for all devices in the worst case operating condition. A performance comparison of insulated gate bipolar transistors (IGBTs) and MOSFETs from leading manufacturers was made to determine the most suitable devices for the HV side and LV side of the converter [183-189]. In an aerospace application, system voltage transients can occur and these were taken into account in the choice of device voltage ratings on the HV and LV sides by selecting devices of 1200V and 600V rating respectively.

Parameters such as on-state voltage, switching power loss, off-state voltage and power density were considered during the selection procedure. In addition, anti-parallel diode on-state voltage and soft recovery behaviour were considered. The suitability of MOSFETs for the LV side converter was analysed [190]. Due to the high current requirement of the LV side converter at the chosen voltage rating of 600V, a parallel combination of three or more MOSFETs would be required to achieve the desired performance, but this topology would

increase circuit complexity. IGBT power semiconductor technology was also investigated owing to its higher current handling capabilities and higher blocking voltages. Recent technology trends in IGBTs [191, 192, 193] make them attractive for high power converter applications because of their short tail current, capability of operation at frequencies greater than 100 kHz for resonant inverters, and high permissible junction temperatures. Hence, IGBTs were selected for the HV and LV sides of the converter in preference to MOSFETs.

Power modules comprising two series connected IGBTs with anti-parallel diodes were investigated rather than the discrete devices, since such modules have low internal inductances, better heat dissipation capability, and are simple to connect. IGBT conduction and switching power loss calculations for the HV side and LV side of the converter are described in the next section.

3.3.1.1 Power loss prediction

Losses generated by semiconductor devices in the DAB converter for the worst case operating condition are discussed in this section. The loss calculation was carried out for several competitor devices assuming 20 kHz switching frequency. Ideal transistor and anti-parallel diode current and voltage waveforms are shown in Figure 3.1 for one cycle. Assuming piece-wise linear waveforms for the device currents, the average current flow through the transistor in the HV-side during the on-time is,

$$I_T = \frac{\frac{1}{2}\times I_{L1}\times\left(\frac{dT_S}{2}-t_B\right)+\frac{1}{2}\times(I_{L1}+I_P)\times\left(\frac{T_S}{2}-\frac{dT_S}{2}\right)}{\frac{T_S}{2}-t_B} \tag{3.1}$$

Since the IGBT exhibits a constant voltage drop during the on-state, which can be obtained from the data sheet, the conduction losses can be estimated from the average transistor current and duty cycle as,

$$P_{CondT} = V_{CE(sat)} \times I_T \times dutycycle \tag{3.2}$$

Duty cycle is the ratio of on-time interval of transistor to the switching time period. Some manufacturers provide information about on-state slope resistance r_{CE} along with collector to emitter on-state threshold voltage denoted as V_{CEO} (in the data sheet), which can be used to estimate the on-state voltage drop $V_{CE(sat)}$, as

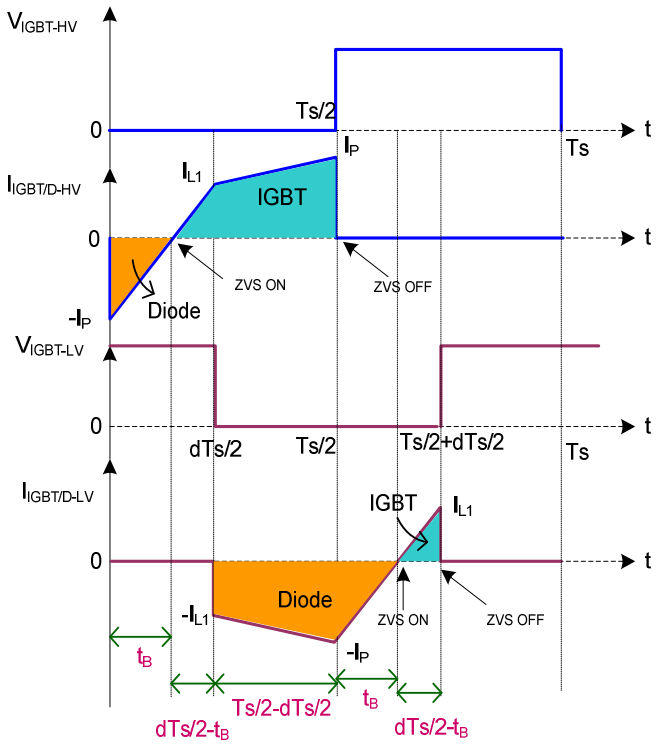


Figure 3.1 Ideal transistor and diode current waveforms on HV and LV side of the DAB converter (Various device switching intervals - indicated in pink letters)

$$V_{CE(sat)} = V_{CEO} + (r_{CE} \times I_T) \tag{3.3}$$

Average HV diode current during the on-state as depicted in Figure 3.1 is given as,

$$I_D = \frac{\frac{1}{2} \times I_P \times t_B}{t_B} \tag{3.4}$$

The diode conduction losses are calculated assuming a constant forward voltage drop V_F, obtained from the diode forward characteristic curve of the manufacturer's datasheet as follows,

$$P_{CondD} = V_F \times I_D \times dutycycle \tag{3.5}$$

Therefore, the total conduction losses (P_C) of the semiconductor devices on the HV side converter is given by,

$$P_C = 4 \times (P_{CondT} + P_{CondD}) \tag{3.6}$$

Switching losses are caused by overlap of the transistor current and voltage waveforms during switching instants [194]. In the DAB converter topology, under ZVS, the diode always turns

off with zero current; this eliminates diode reverse recovery losses. The turn-on (E_{ON}) and turn-off (E_{OFF}) energy loss curves for an IGBT are usually available from the datasheet as a function of collector current at the turn-on and turn-off instants. Therefore, the power loss equations are given by,

$$P_{ON} = E_{ON} \times f \tag{3.7}$$

$$P_{OFF} = E_{OFF} \times f \tag{3.8}$$

Where P_{ON} is the turn-on power loss, P_{OFF} is the turn-off power loss and f is the switching frequency. Some manufacturers do not provide turn-on and turn-off energy loss curves. In such cases, it is necessary to consider the simplified voltage and current waveforms during the switching process. Most of the switching losses occur during the rise-time t_r and fall-time t_f intervals of the IGBT current. The approximated turn-on and turn-off power losses are then calculated based on the following equations:

$$P_{ON} = \frac{1}{2} V_{CE} \times I_C \times t_r \times f \tag{3.9}$$

$$P_{OFF} = \frac{1}{2} V_{CE} \times I_C \times t_f \times f \tag{3.10}$$

In the DAB converter topology, each transistor turns-on with zero voltage across it under a wide range of operating conditions. Since current is transferred from its anti-parallel diode, the IGBTs turn-on losses can be neglected. Hence, the total switching losses (P_{SW}) are approximately,

$$P_{SW} = 4 \times [E_{OFF} \times f] \tag{3.11}$$

The junction temperature of the devices can be calculated [181] as,

$$T_{jIGBT} = T_s + \left(P_T \times R_{th(c-s)}\right) + \left(P_{IGBT} \times R_{th(j-c)}\right) \tag{3.12}$$

$$T_{jDiode} = T_s + \left(P_T \times R_{th(c-s)}\right) + \left(P_{Diode} \times R_{th(j-c)}\right) \tag{3.13}$$

where, T_S is the heat sink temperature (refer section 3.3.2), P_T is the total power loss of the IGBT module. The case to sink $R_{th(c\text{-}s)}$ and junction to case $R_{th(j\text{-}c)}$ thermal resistances were obtained from the manufacturers datasheet.

A comparison of conduction and switching power losses for HV side IGBTs and anti-parallel diodes with ratings close to 1200V, 300A was carried out for five different manufacturers devices: -

- Semikron (SKM300GB125D → 1200V, 300A@ T_{case}=25˚C)
- IXYS (MII300-12A4 → 1200V, 330A@T_{case}=25˚C)
- Dynex semiconductor (DIM200WHS12-A000 → 1200V, 200A@T_{case}=80˚C)
- Fuji semiconductor (2MB1300U4H-120 → 1200V, 400A@T_{case}=25˚C) and
- Powerex (CM300DY-24A → 1200V, 300A@ T_{case}=25˚C)

A table summarising the findings is shown in Figure 3.2. Losses corresponding to an IGBT and anti-parallel diode are depicted for each module for the worst case operating conditions.

Based on this loss comparison, ultra fast 1200V, 300A phase leg IGBT modules (type SKM300GB125D) from Semikron [195] were chosen for the HV side converter due to their low loss. It can be seen from Figure 3.2, that the switching power losses of the IGBTs are significant and are the major contributor to overall power loss. This is due to the high switching frequency and the high turn-off current. To reduce this loss a turn-off snubber is required. Calculations showed that with snubbers, the switching losses would become approximately 20% of the switching losses depicted in Figure 3.2, assuming that the IGBT tail current does not change when the snubber is added.

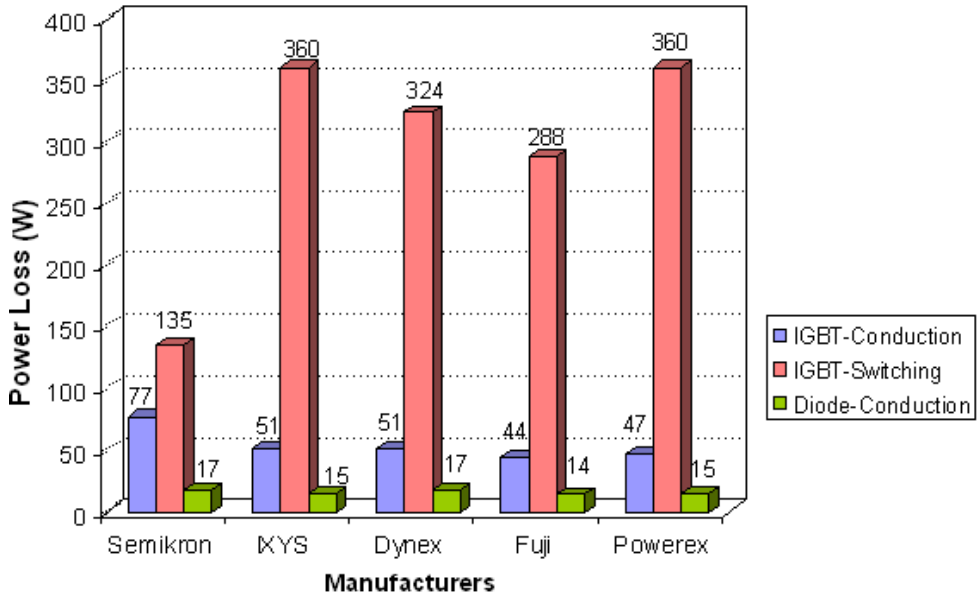


Figure 3.2 Power loss comparisons of HV devices with various manufacturers

A similar procedure was carried out to estimate the LV side devices power loss as well. However, on the LV side the current wave shape differs, since the LV side ac output is shifted from that of the HV side by the duty ratio '*d*'. From Figure 3.1, the current flow during the on-time of a LV side transistor (I_T) and diode (I_D) is given by,

$$I_T = \frac{\frac{1}{2}\times I_{L1}\times\left(\frac{dT_S}{2}-t_B\right)}{\left(\frac{dT_S}{2}-t_B\right)} \tag{3.14}$$

$$I_D = \frac{\frac{1}{2}\times(I_P\times t_B)+\frac{1}{2}\times(I_{L1}+I_P)\times\left(\frac{T_S}{2}-\frac{dT_S}{2}\right)}{\left(\frac{T_S}{2}-\frac{dT_S}{2}+t_B\right)} \tag{3.15}$$

As with the HV side, a comparison of conduction and switching power losses for LV side IGBTs and anti-parallel diodes having ratings close to 600V, 760A at T_{case}=25˚C was carried out for devices offered by four leading manufacturers. The devices' current ratings were chosen based on the average current calculation of device currents on the LV side of the converter. Only four manufacturers had devices close to the required rating. They were

- Semikron (SKM600GB066D → 600V, 760A)
- Mitsubishi (CM600DY-12NF → 600V, 600A)
- Fuji semiconductor (2MB1600U2E-060 → 650V, 600A) and
- Powerex (CM600DY-12NF → 600V, 600A)

A power loss comparison of the LV side devices is shown in Figure 3.3. Losses for a single IGBT and anti-parallel diode are depicted for each module. From Figure 3.3, it can be seen that all the IGBT modules have a similar performance, but that the LV side diode conduction losses are the highest amongst the semiconductor components due to the rectifying function under charging mode. However, during power flow reversal the loss figures are interchanged between the diode and IGBT. It can be seen that the Semikron phase leg IGBT module has slightly lower losses than devices from other manufacturers. Moreover, the maximum junction temperature of the Semikron module is 175˚C while the other modules have a maximum junction temperature of 150˚C. Additionally the Semikron module has a higher current rating. Consequently fourth generation high temperature 600V, 760A phase leg IGBT modules (type SKM600GB066D) from Semikron [196] were chosen as devices for the LV side converter.

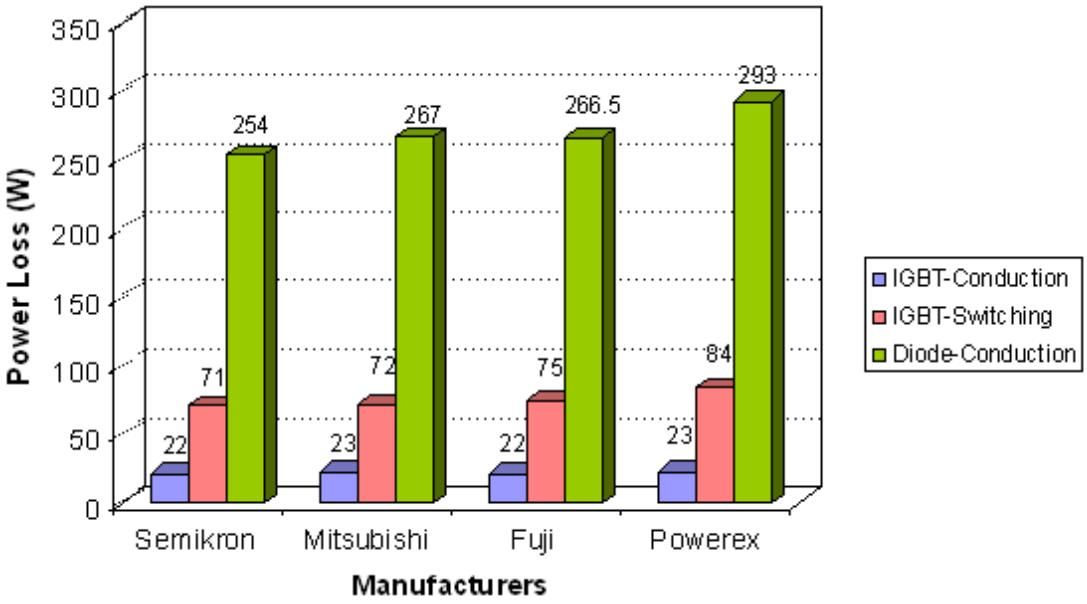


Figure 3.3 Power loss comparisons of LV devices with various manufacturers

3.3.2 Selection of heat sink

It was decided to have one heat sink for both stages (all four modules) of the DAB converter. Hence, the total losses of all the power modules were added together to estimate the correct value of heat sink thermal resistance [197-201]. The calculated value of total power loss for the DAB converter without snubber capacitors was found to be 2304W. Thus a very low heat sink thermal resistance is needed. Consequently, power losses were re-estimated for the case of snubber capacitors across all devices. With snubbers, the switching losses were estimated to be approximately 20% of the switching losses depicted in Figures 3.2 and 3.3, assuming that the IGBT tail current does not change when the snubber is added. Hence, the overall power loss with snubber capacitors was 1645W. The thermal resistance from heat sink to ambient was calculated from,

$$R_{th(s-a)} = \frac{T_s - T_a}{P_T} \tag{3.16}$$

Where, T_s and T_a denote the heat sink and ambient temperature respectively and P_T denote the total power loss of the converter. Assuming a 40˚C rise between heat sink and ambient, $R_{th(s-a)}$ was calculated to be 0.024˚C/W. A double fan bonded-fin forced convection heat sink with a thermal resistance of 0.024˚C/W from Wakefield Thermal Solutions [202] was chosen. 19W

fans, type 4650Z, with 160m^3/h air flow rate, from Papst were chosen to achieve the necessary cooling.

3.3.3 Selection of snubber capacitors

From the power loss comparison graphs shown in Figures 3.2 and 3.3, it can be observed that all the semiconductors considered for comparison exhibit significant switching losses. Although Semikron IGBTs have lower switching losses in comparison with other IGBTs, switching losses tend to dominate conduction losses. Snubber capacitors were therefore selected to reduce the turn-off switching loss of the IGBTs. Knowledge of the current and voltage ratings of the semiconductors and their switching frequency is essential for selection of the snubber capacitors [203-206]. In order to choose the correct snubber capacitor the *dv/dt* requirement for this application must be known. The peak current flowing through the snubbers at the time of turn-off and the corresponding *dv/dt* were estimated for the worst case operating condition. The following paragraphs describe the effect of snubber capacitor on IGBT energy loss, by first dealing with the calculation of IGBT energy loss without snubber capacitors.

Figure 3.4 depicts ideal IGBT voltage and current waveforms during turn-off without a snubber capacitor. The transistor voltage rises rapidly to V_{in} and its current starts to fall. Energy loss can be estimated as follows,

$$\text{Energy Loss} = \int_0^{t_f} V_{in} \times I_{IGBT}\, dt \qquad (3.17)$$

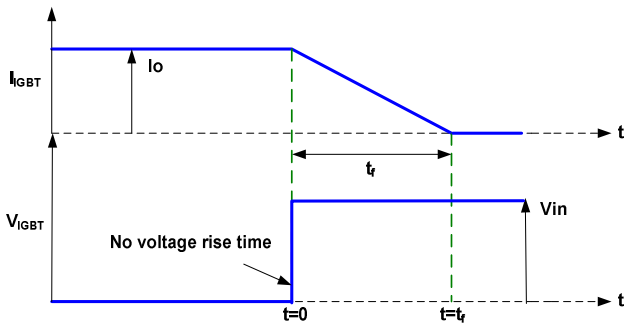


Figure 3.4 IGBT voltage and current waveforms without snubber capacitor

The expression for IGBT current can be written as, $I_{IGBT} = I_0 - \frac{t \times I_0}{t_f}$ (3.18)

Substituting (3.18) in (3.17) gives,

$$\text{Energy loss} = \int_0^{t_f} V_{in} \times \left[I_0 - \frac{t \times I_0}{t_f} \right] dt$$

Simplifying further,

$$= V_{in} I_0 \times \left[t - \frac{t^2}{2t_f} \right]_0^{t_f}$$

$$= V_{in} I_0 \times \left[t_f - \frac{t_f}{2} \right]$$

Therefore, IGBT energy loss without snubber capacitor $= \frac{V_{in} I_0 t_f}{2}$ (3.19)

Figure 3.5 illustrates the IGBT turn-off waveforms with a snubber capacitor under ideal conditions. Since the IGBTs are in the phase leg modules, it was decided to use individual snubber capacitors across every IGBT in the top and bottom of each phase leg. Therefore, the current flowing through the IGBT and snubber capacitor can be written as,

$$I_{IGBT} = I_0 - \frac{t \times I_0}{t_f}$$

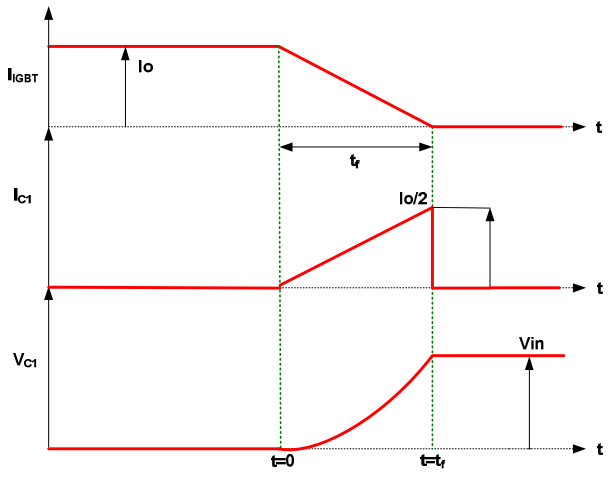


Figure 3.5 Turn-off switching waveforms of IGBT with snubber capacitor

$$I_{C1} = \frac{t \times I_0 / 2}{t_f} \tag{3.20}$$

Charging voltage of the snubber capacitor is given by,

$$V_{C1} = \frac{1}{C}\int I_{C1} dt = \frac{I_0}{2C} \times \left(\frac{t^2}{2t_f} \right) \tag{3.21}$$

Energy loss during turn-off with snubber capacitor is then estimated as,

$$\text{IGBT energy loss} = \int_0^{t_f} P dt = \int_0^{t_f} V_{C1} \times I_{IGBT} dt \tag{3.22}$$

Substituting the equations of capacitor voltage and IGBT current in (3.22),

$$= \int_0^{t_f} \left\{ \frac{I_0}{2C} \times \left(\frac{t^2}{2t_f} \right) \right\} \times \left\{ I_0 - \frac{t \times I_0}{t_f} \right\} dt$$

$$= \frac{I_0^2}{4Ct_f} \int_0^{t_f} \left[t^2 - \frac{t^3}{t_f} \right] dt$$

Simplifying further,

$$= \frac{I_0^2 t_f^2}{4C} \left[\frac{1}{3} - \frac{1}{4} \right]$$

$$\text{Energy loss} = \frac{(I_0 t_f)^2}{48C} \tag{3.23}$$

When $t = t_f, V_{C1} = V_{in}$ substituting in (3.21) gives,

$$V_{C1} = V_{in} = \frac{I_0}{4C} \times \left(\frac{t_f^2}{t_f} \right) = \frac{I_0 t_f}{4C}$$

Therefore, the value of snubber capacitor $C = \frac{I_0 t_f}{4V_{in}}$ (3.24)

Substituting the snubber capacitor equation (3.24) in to the energy loss equation (3.23), the new energy loss equation is given by,

$$\frac{(I_0 t_f)^2}{48C} = \frac{(I_0 t_f)^2}{48 \times (I_0 t_f)} \times 4V_{in} = \frac{V_{in} I_0 t_f}{12}$$

$$\text{IGBT energy loss with snubber capacitor} = \frac{V_{in} I_0 t_f}{12} \tag{3.25}$$

Thus the turn-off switching energy loss with a snubber capacitor is 1/6th of the energy loss without the snubber capacitor. This analysis reveals that the snubber capacitor allows device current to fall before the voltage rises significantly during turn-off, thereby reducing the turn-

off switching loss to 16.67% of its non-snubbered value. It thereby limits the rise time of voltage across the switch during turn-off.

In order to determine a suitable snubber capacitor value, the peak current flowing through the snubbers at the time of turn-off and the corresponding *dv/dt* was estimated for the phase leg, for the worst case operating condition of both HV and LV sides of the DAB converter. Based on the current fall-time value specified in the datasheet for the selected IGBTs, capacitors of value 22nF with a *dv/dt* of 8.455kV/μs and capacitors of 2.2nF with a *dv/dt* of 29kV/μs are needed for the LV side and HV side IGBT snubbers respectively. A radial polypropylene capacitor [207] of 2.2nF, 1600V rating with a *dv/dt* of 34kV/μs from Arcotronics was chosen as the HV side snubber and a polypropylene FKP series direct mount IGBT snubber [208] of 22nF capacitance and voltage rating of 2000V, with a *dv/dt* of 11kV/μs from WIMA was selected as the LV side snubber. Considering the snubber capacitor charging time, a dead-time of 2.2μs between the top and bottom IGBTs of a phase leg was chosen.

3.3.4 Inductor design

The DAB topology can be represented as two phase controlled square-wave voltage sources interconnected by a high frequency AC link inductor. Figure 3.6 (a) – (d) shows the various ways of forming an AC link in the DAB converter. Figure 3.6(a) represents the cost effective manner of interconnection. Figure 3.6(d) uses the transformer with split inductors for interconnecting the two bridges. The topology given in Figure 3.6(d) has been chosen due to its advantage in terms of electromagnetic compatibility (EMC). An air core inductor was designed to form the AC link, as it is relatively easy to construct and cost-effective. Although air core inductors usually require a large number of turns to achieve the desired inductance, they have the advantage of not saturating and can be used at high frequencies without iron loss. The inductance of a single layer air core inductor is given by Wheeler's formula [209, 210],

$$L = \frac{N^2 r^2}{228.6r + 254l}(\mu H) \tag{3.26}$$

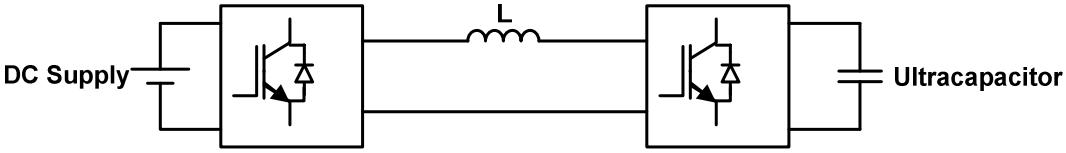
Where,

r is the radius of coil in mm

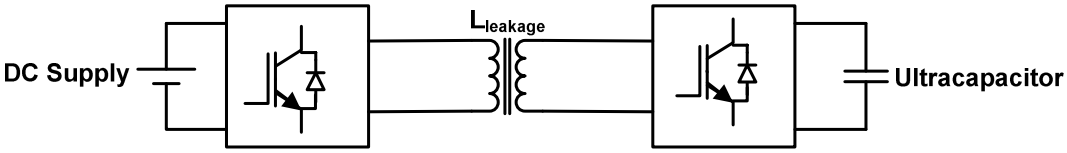
l is the coil length in mm

N is the number of turns

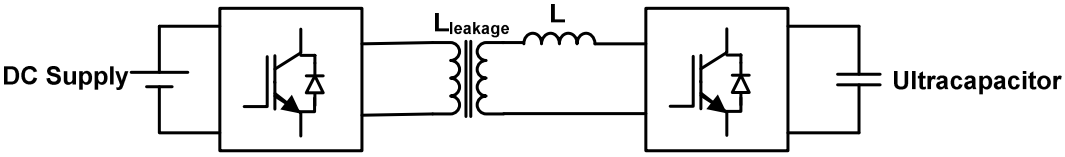
To obtain an accurate value of inductance, $l > 0.8r$ should be maintained in (3.26) and the inductor design values are given in the next Chapter.



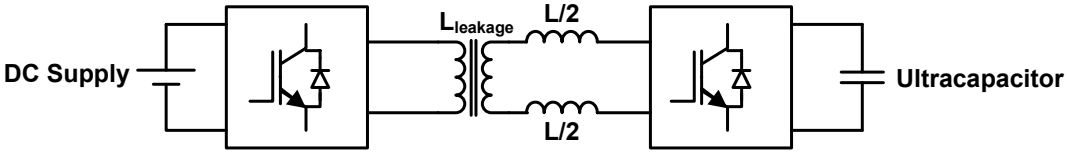
(a) AC link formed through a high frequency inductor



(b) AC link formed through a transformer with desired leakage inductance



(c) AC link formed through a transformer of low leakage inductance with a series inductor



(d) AC link formed through a transformer of low leakage inductance with a split series inductor on each line

Figure 3.6 Various ways of forming an AC link in the DAB converter

3.3.5 Selection of input and output filter capacitors

Filter capacitors were selected based on their current handling capability, rated capacitance and maximum DC operating voltage. RMS current derivations for the waveforms of the DAB converter are given in detail in Appendix A and the average current expressions are given in Chapter 2. The capacitor RMS current can be found using the following expression.

$$I_{CRMS} = \sqrt{I_{inRMS}^2 - I_{inavg}^2} \quad (3.27)$$

Using (3.27), the RMS current flowing through the output and input filter capacitors was estimated as 283A for the output filter and 77A for the input filter. For the worst case, in order to maintain 1% ripple voltage, capacitances of 123μF and 2.91mF are required for the input and output filters respectively. After an extensive search, a choice was made of a single capacitor, type CXP polypropylene [211] having a capacitance of 100μF, a ripple current rating of 90A RMS, a 900V DC rating and an ESR <1.5mΩ from Leclanche capacitors for the HV side filter. This capacitor is capable of maintaining 1.23% ripple voltage. For the HV side, the voltage rating of the input filter capacitor was chosen as 900V, which is 67% greater than the converter's nominal operating voltage of 540V. With this 900V rating the input filter can also protect the converter and its load from transients that appear in the input voltage thereby improving the system reliability [212-214].

For the LV side, twelve UNL metallised polypropylene capacitors [215] of 30μF capacitance, 400V DC rating, 24.2A RMS ripple current rating @ 25˚C and 6mΩ ESR@100kHz from Cornell Dubilier, connected in parallel, were chosen to meet the required RMS current rating. This adds up to a total capacitance of only 360μF, which will result in a ripple voltage between 4% and 8%, depending on the operating voltage of the ultracapacitor module. Considering the system voltage on the LV side, the current rating and appropriate size of the capacitor for the busbar, the voltage rating of the capacitor was chosen to be 2.2 times greater than the converter's nominal output voltage.

3.3.6 Selection of ultracapacitor

An ultracapacitor has been chosen as the energy storage device on the LV side of the DAB converter as it exhibits a fast response time for quick power transfer from/to active loads. It was decided that the ultracapacitor would provide a peak power of 20kW for 30 seconds to supplement the total power generation system capability of the IEPNEF model. In order to choose the right size of ultracapacitor for this application, the procedure given in [216] was followed. The simplified equivalent circuit of the ultracapacitor with equivalent series resistance (ESR) and nominal capacitance is shown in Figure 3.7.

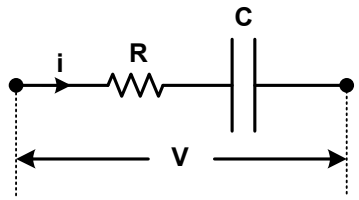


Figure 3.7 Simplified equivalent circuit of the ultracapacitor

From Figure 3.7, the voltage across the ultracapacitor can be written as,

$$V = \frac{1}{C}\int i dt + i \times R$$

The total change in the ultracapacitor voltage can be written as,

$$dV = i \times \frac{dt}{C} + i \times R \tag{3.28}$$

Basic system parameters are,

Working (operating) voltage V_w = 125V

Minimum allowable voltage V_{min} = 62.5V

Power requirement = 20kW

Time = 30 seconds

$$dV = V_W - V_{\min} = 125 - 62.5 = 62.5V$$

The maximum, minimum and average ultracapacitor current can be calculated as,

$$i_{\max} = \frac{P}{V_{\min}} = \frac{20000}{62.5} = 320A$$

$$i_{\min} = \frac{P}{V_{\max}} = \frac{20000}{125} = 160A$$

$$i_{avg} = \frac{i_{\max} + i_{\min}}{2} = \frac{320 + 160}{2} = 240A$$

Maxwell Technologies 125V Power series module [217, 218] is available in the market, which has a response time less than half a second. Hence, the suitability of 125V module for this application has been verified. Maxwell's 125V module [219] has 48 cells of BCAP3000 (2.7V, 3000F, 0.29mΩ) in series and has the following performance figures:

C = 63F

ESR = 18mΩ@25°C

V_{max} = 130V

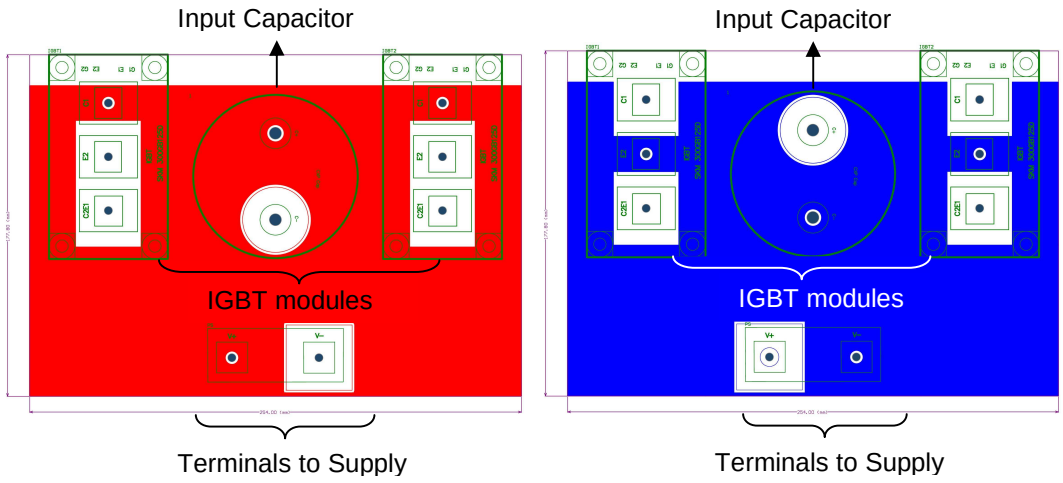
V_{rated} = 125V

Energy = $\frac{\frac{1}{2}\times C\times\left(V_{rated}^2-\frac{1}{2}\times V_{rated}^2\right)}{3600}$ = 101.7Whr

Based on the above figures, by applying the procedure given in [216], it can be observed that a single module will not meet the desired power requirement. Hence, with two modules in parallel, total capacitance would be 126F and resistance would be 9mΩ was chosen for providing 20kW power in 30 seconds time. In the ultracapacitor selection procedure detailed in [216], the loss due to ESR was assumed to be negligible. However, the initial discharge voltage drop due to ESR is an important factor, which was accounted for in the design.

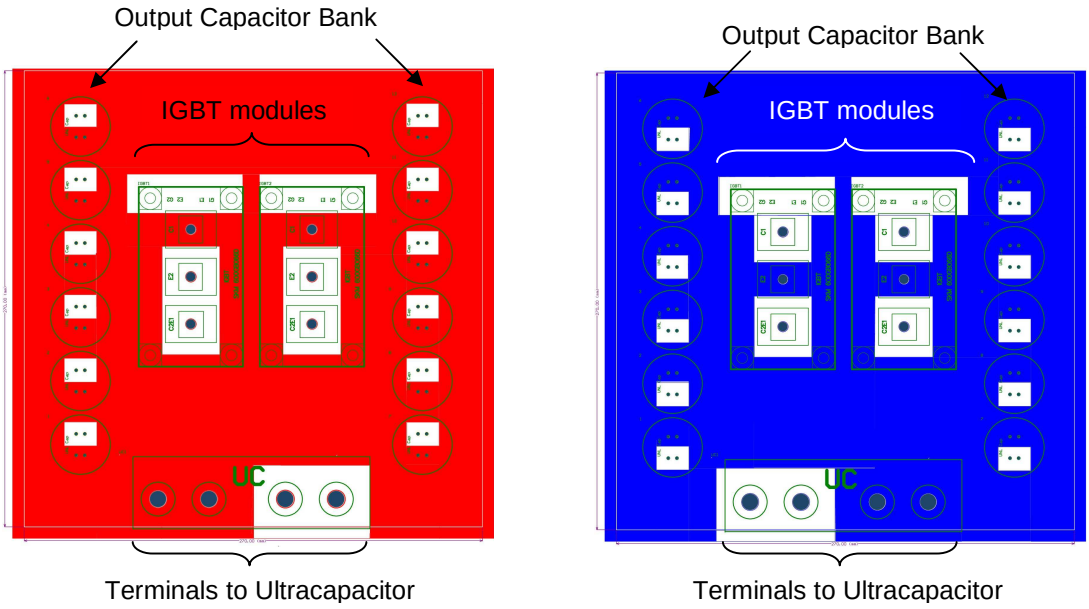
3.4 Converter layout and busbar design

To minimise the effect of circuit parasitics, circuit connections were made using planar busbars [220]. The busbars consist of two layers of copper with an insulating layer between them. The DAB converter requires two sets of busbars for each of the converter stages. High conductivity, half hard C101 copper sheet [221] with 0.4mm thickness was selected for the HV side busbar, whereas a thickness of 2mm was chosen for the LV side busbar. The copper busbars were separated by 2mm Tufnol carp sheet. The busbars were designed using Altium Protel DXP. Figures 3.8 and 3.9 show the planar busbar layouts for the HV side and LV side of the DAB converter respectively. Figures 3.8(a) and 3.9(a) show the top layers of the converter busbars, which are used for the positive voltage connections to the supply and ultracapacitor. Likewise, Figures 3.8(b) and 3.9(b) show the bottom layer busbars, which are used for the negative voltage connections to the supply and ultracapacitor. The input capacitor is bolted to the HV side busbar, whereas the output capacitors were soldered to the LV side planar busbars. The gate driving signals from the DSP controller are directly connected to the gates via twisted wire leads.



(a) (b)

Figure 3.8 Layout of DAB HV side converter (a) Top Layer (b) Bottom Layer



(a) (b)

Figure 3.9 Layout of DAB LV side converter (a) Top Layer (b) Bottom Layer

3.5 Gate driver circuit design

The DAB converter has 8 IGBTs. It requires at least 4 independent driver modules to provide driving signals for each leg of the H-Bridges. It was decided to use 15V square-wave drives to the IGBTs. Using the gate charge requirements specified in the IGBTs datasheets, the driver power, maximum output gate current and gate resistances were chosen for both HV and LV bridges [222]. A dual channel gate driver, type 2SD315AI from Concept technologies, was chosen, due to its very high output current ±18A and high drive power of 6W. A driver circuit with the necessary over current and fault status feedback protection was designed [223-228] using Altium Protel DXP and constructed to meet the desired functionality. A simplified driver circuit for one leg of the DAB converter is shown in Figure 3.10. The status output of the driver is coupled with the reset signal using NAND gates, and the resulting signal is coupled with the enable signal input of the driver using an AND gate. If a fault occurs, the status output will become low thereby the resulting signal and enable signal become low thus disabling the driver operation and cutting-off the driver signals. The driver operates in half bridge mode, and produces PWM signals for top and bottom IGBTs from the single PWM signal input from the DSP. The PWM signal from the DSP is fed to the driver via a buffer to achieve the desired voltage level of 15V. Considering the snubber capacitors charging time (see section 3.3.3), a dead-time of 2.2μs between the top and bottom IGBTs of a phase leg was chosen. By connecting suitable values of R and C, not shown in Figure 3.10, to the module, the driver can be adjusted to provide the desired dead-time between the top and bottom IGBTs. A detailed diagram of the gate driver circuit along with its PCB design is given in Appendix D. The gate driver was mounted on brackets close to the transistor gate terminals of the converter.

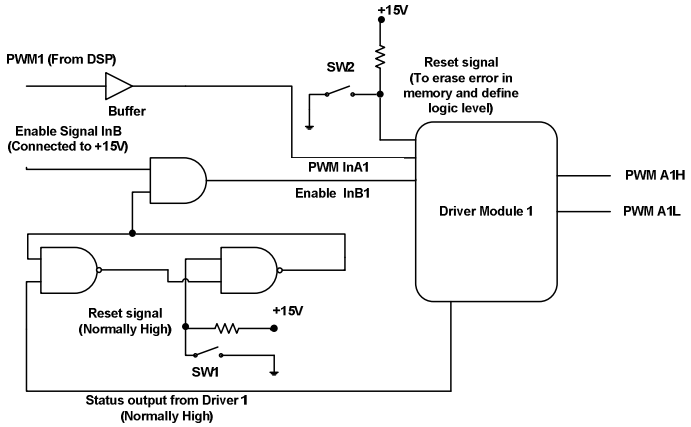


Figure 3.10 Simplified gate driver circuit for an IGBT module

3.6 Interfacing/Signal conditioning circuit for DSP control

Control signals for the DAB converter are derived using a Texas Instruments TMS320F2812 DSP. LEM current and voltage transducers were used to sense inductor current and output voltage respectively. The DSP has two event managers (EVA & EVB) for PWM signal generation and a 16 channel Analog to Digital Converter (ADC) for processing the signals from the sensors. Figures 3.11 and 3.12 show the signal conditioning circuits used to connect the current and voltage transducers to the DSP.

The current signal from the inductor is AC in form. It is necessary to convert this inductor current signal [229] into a unipolar signal with a voltage range of 0 to 3V before feeding it into the DSP. A current transducer, type LF 1005-S [229] was chosen to provide the inductor current measurement. The sensor's current measuring range is 0 - ± 1000A with ± 15V supply. Its conversion ratio is 1:5000 and its bandwidth is DC-150kHz. The secondary nominal current is ±200mA. Resistances of value 75Ω and 8.3Ω were series connected to the stabilised 15V supply to provide an offset voltage of 1.5V across the 8.3Ω resistance, thereby converting the ±200mA into a 0 to 3V signal for the DSP.

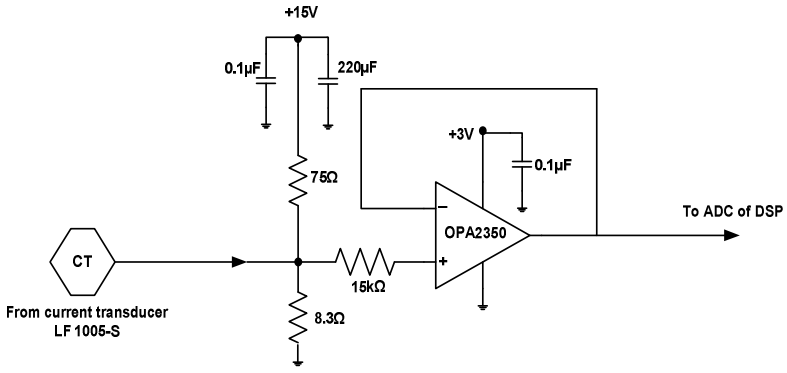


Figure 3.11 Current signal conditioning circuit

The voltage across the ultracapacitor is always positive; allowing a simple design of conditioning circuit. A voltage transducer, type LV-25P [230] was chosen to provide the ultracapacitor voltage measurement. The voltage measuring range of the transducer is 10V-500V and the conversion ratio is 2500:1000. In order to maintain an accuracy of ±0.8%, the input resistor to the transducer was chosen as 12.5kΩ, and 100Ω was chosen as the output

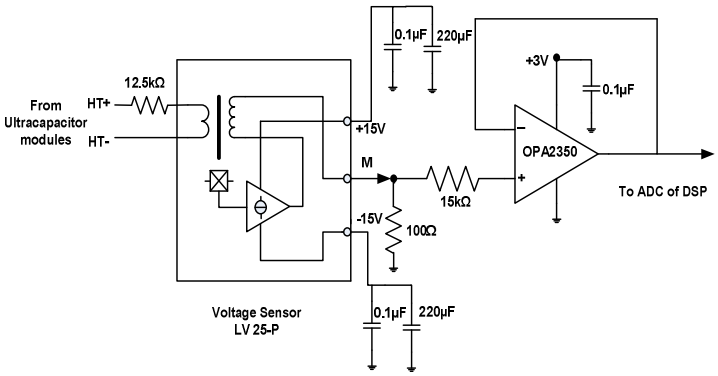


Figure 3.12 Voltage signal conditioning circuit

resistor. By this means the transducer converts 125V/62.5V to 2.5V/1.25V. PWM signals from the processor are fed to the driver via a UCC37324 buffer to boost the 3.3V control signals into 15V signals as shown in Figure 3.13. A detailed circuit diagram of the interfacing circuit and its PCB design is given in Appendix D.

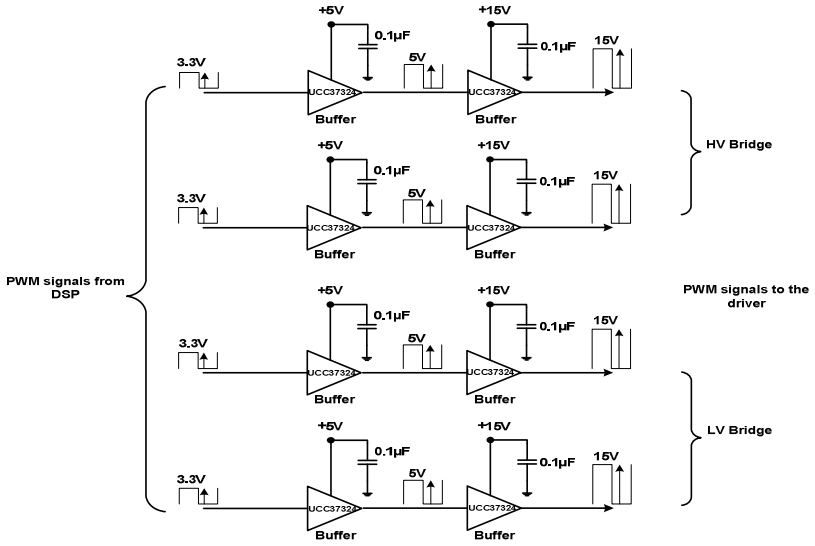
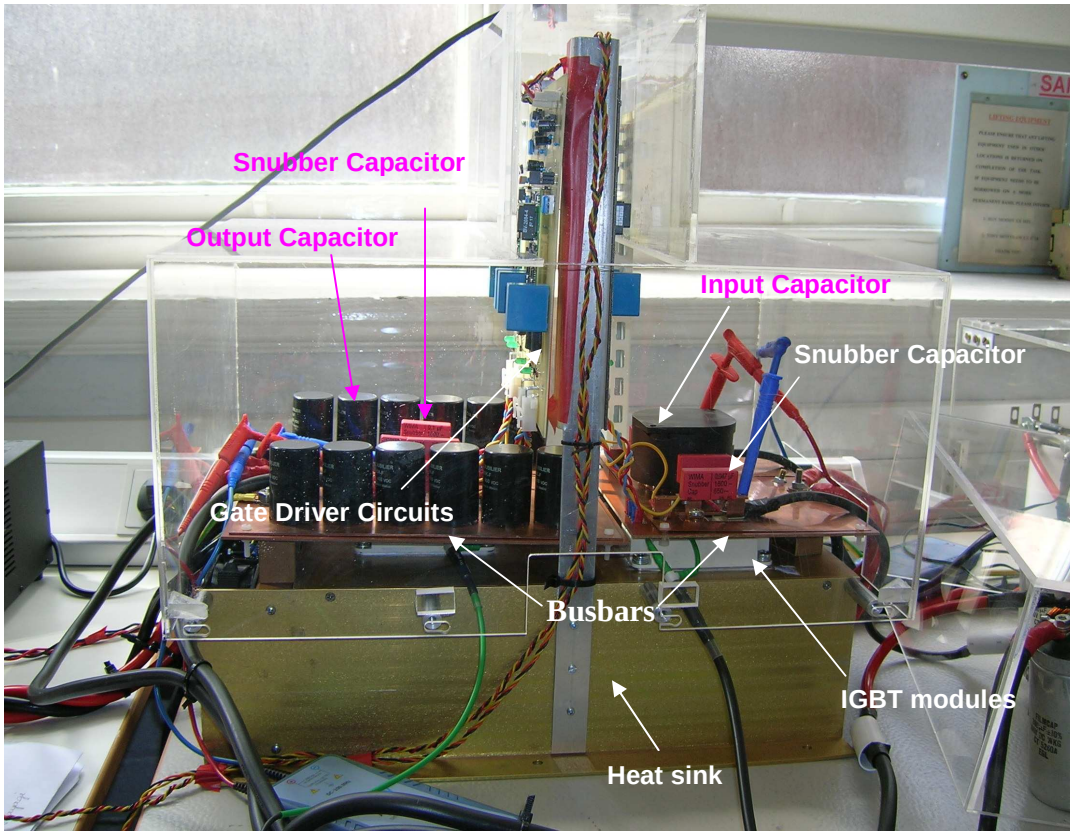


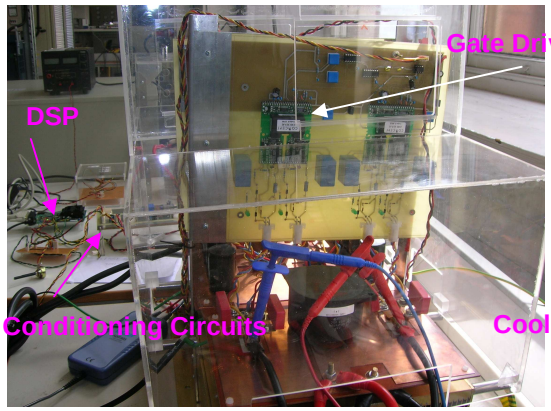
Figure 3.13 Interfacing circuit for PWM signals from DSP to driver circuit

3.7 Photograph of the DAB converter prototype

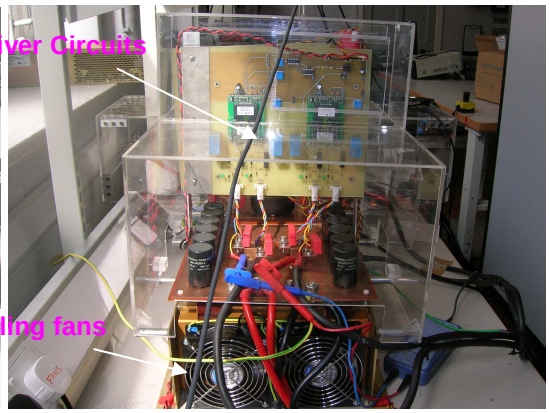
Figure 3.14 shows a photograph of the completed DAB converter prototype. Figure 3.14 (a) depicts the side view of the converter, whereas Figures 3.14 (b) and (c) portray the front and back views of the converter prototype. A full view of the experimental system is presented in Appendix E.



(a)



(b)



(c)

Figure 3.14 Photograph of DAB converter prototype (a) Side view (b) Front view (c) Back view

3.8 Summary

The detailed design and implementation of a 20kW DAB converter prototype was presented in this chapter. This includes the selection of semiconductor devices for HV and LV sides of the converter along with suitable selection of heat sink, input and output filter capacitors, design of inductor, planar busbars for the converter layout and the design of driver and signal conditioning circuits. The effect of the snubber capacitors on the IGBTs' energy loss was analysed and suitable values of snubber capacitors for HV and LV side IGBTs were selected. It has been predicted from the analysis that the switching power loss of the transistor with the snubber capacitor is only 20% of the switching power loss without snubber capacitors.

Chapter 4

Experimental Verification of DAB DC-DC Converter

4.1 Introduction

The prototype DAB converter experimental results are presented in this chapter. Testing was performed in three stages. Firstly, the HV side bridge was tested by phase shifting the voltage of the two half-bridge legs while they were connected through a high frequency AC link inductor. IGBT loss measurement was undertaken for various values of snubber capacitors and gate resistances on the HV side, and the value of the snubber capacitor for which minimal switching loss was achieved, was identified. Secondly, the LV side bridge of the converter was tested by phase shifting the voltage of its two half-bridge legs to the maximum value when connected by the inductor. During this testing the LV side IGBTs were subjected to maximum current. The conduction and switching losses of the LV side IGBTs were measured for different values of snubber capacitors. The value of the snubber capacitor for which reduced switching stress was experienced by the devices, was determined experimentally. Thirdly, DAB converter testing was undertaken and the power losses in the DAB converter prototype during maximum power transfer and on the ZVS boundary were determined. The experimental testing validated the converter prototype design, the theoretical predictions from the steady-state analysis and SABER simulation results.

4.2 HV bridge testing

The HV side bridge of the converter was tested using a 0 – 600V, 1.7A XHR600 series DC Power supply from Xantrex Technologies Inc. The two legs of the HV side bridge were interfaced through a 39µH air core inductor, and the IGBTs were subjected to maximum current flow by phase shifting their output voltages. Since the load is purely reactive, current drawn from the source only provided device conduction losses, switching losses and losses due to the passive elements. Therefore, it was possible to test the HV side of the converter up to 540V, with 80A IGBT current, with the 1.7A supply. The current rating of the power supply limited the maximum phase shift introduced (d = 0.454) between the two half-bridge legs and therefore the turn-off current of the IGBTs for the chosen inductance value. An external 6.6mF

electrolytic capacitor bank, as shown in Figure 4.1(a), was added to the input side to filter the input ripple current on the supply side. The HV bridge testing circuit and its key waveforms are shown in Figure 4.1(b) and Figure 4.2 respectively. Control signals for driving the transistors were derived from the DSP. A Rogowski current probe, type CWT1N, was used to measure the IGBT/Diode current. A Lecroy high voltage differential probe, type ADP305, was used to measure the device voltage.

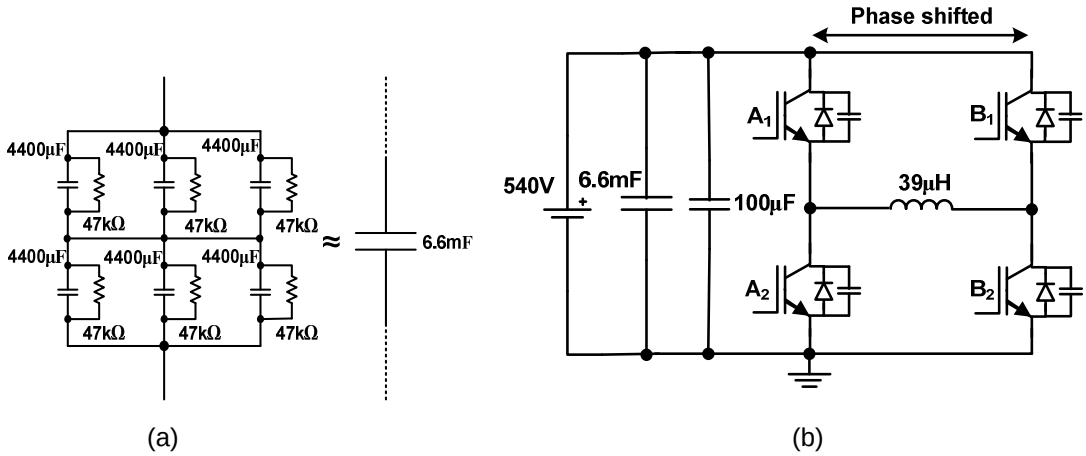


Figure 4.1 (a) Schematic of electrolytic capacitor bank (b) Schematic of HV bridge testing circuit

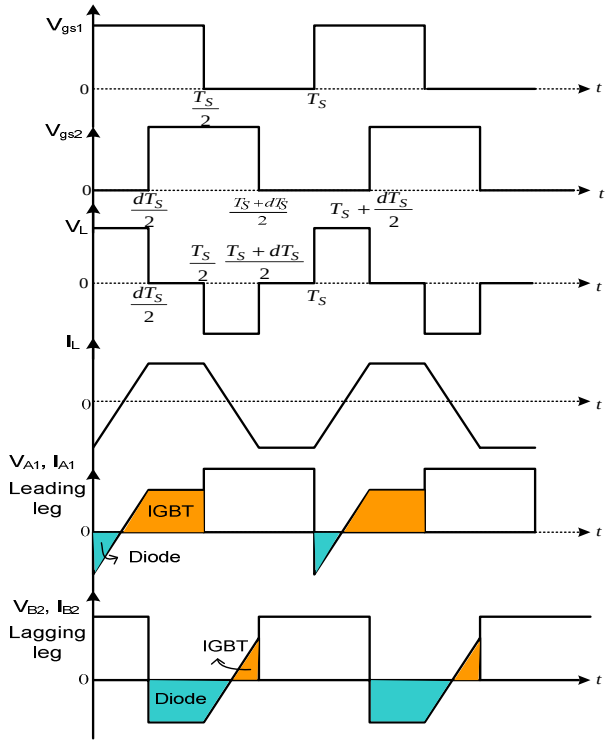


Figure 4.2 Operational waveforms of HV bridge testing circuit

4.2.1 Influence of snubber capacitor

Testing was performed initially on the HV side converter without the snubber capacitors. Figure 4.3 shows the experimental waveforms at 540V and 80A peak current of HV side converter without snubber capacitor.

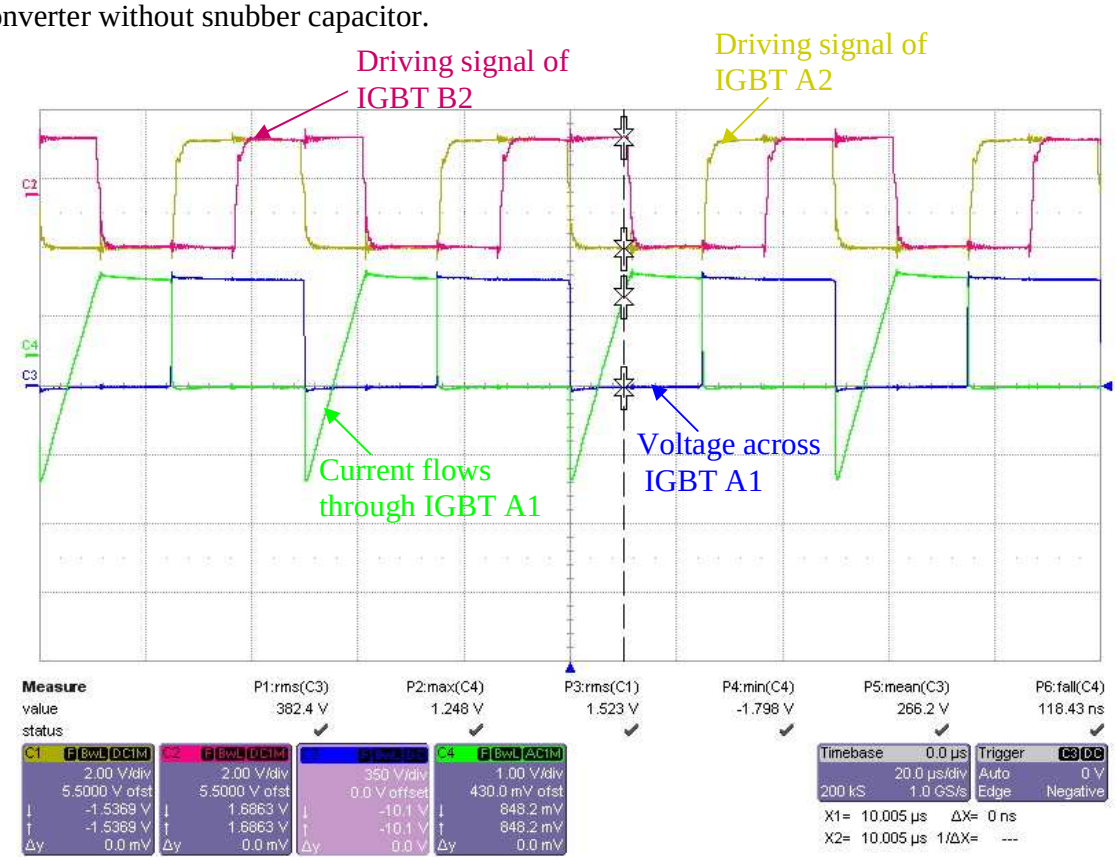


Figure 4.3 Experimental waveforms of HV side converter without snubber capacitor
V_{in} =540V, I_{in} = 1.67A, L = 39µH, V_{Lrms} = 363V, I_{Lrms} = 65.6A, f_s = 20kHz, I_{OFF} = 80A, R_G = 3Ω
Channel 1 (yellow) – driving signal of transistor A_2
Channel 2 (pink) – driving signal of transistor B_2
Channel 3 (blue) – voltage of leading-leg IGBT A_1
Channel 4 (green) – current of leading-leg IGBT A_1
Channel 4 - 50A/div measured using 20mv/A Rogowski current probe

From Figures 4.2 and 4.3, it can be observed that diode conduction starts before the transistor and has ZVS turn-on at peak current and ZVS/ZCS turn-off. The IGBT has ZVS/ZCS turn-on and ZVS turn-off at peak current. Therefore, the turn-on loss of the IGBT and the reverse recovery loss of the diode can be neglected. The turn-off instant of the IGBT is depicted in Figure 4.4. The waveforms shown in Figure 4.3 and 4.4 are almost free from parasitic ringing due to the busbar construction. From Figure 4.4, it can be clearly seen that the IGBT has been

subjected to high stress during turn-off, which results in high switching losses. The current fall-time was estimated using the Lecroy scope, and was found to be 118.43ns, which is significantly higher than the fall- time of 30ns specified in the manufacturer's datasheet. A snubber capacitor of 2.2nF was connected across each of the four IGBTs to control the turn-off switching losses.

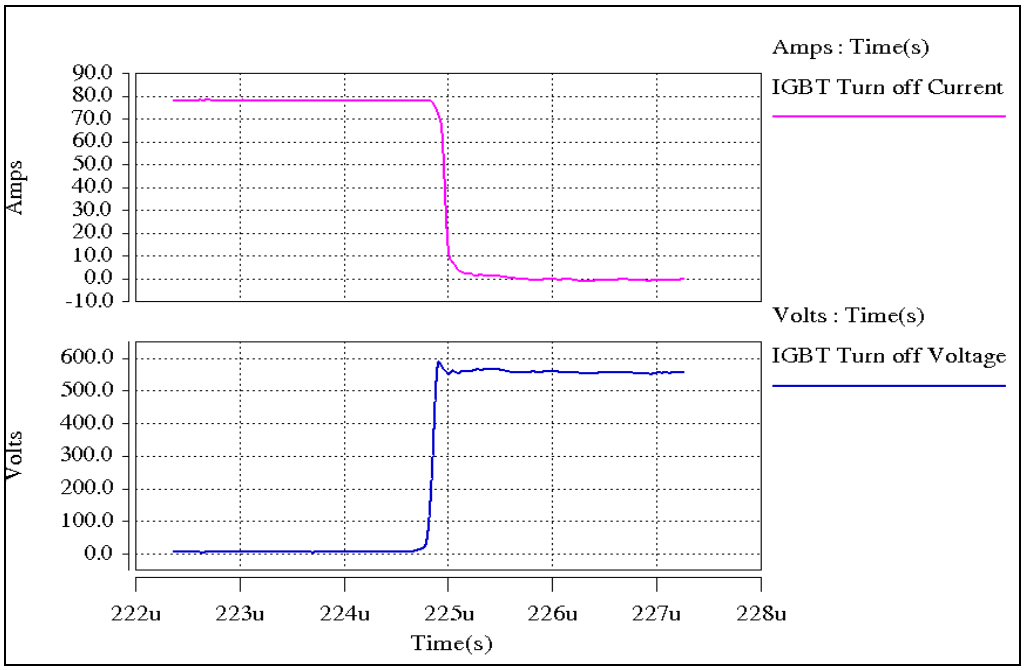


Figure 4.4 Turn-off transient of IGBT without snubber capacitor
V_{in} =540V, I_{in} = 1.67A, L = 39µH, V_{Lrms} = 363V, I_{Lrms} = 65.6A, f_s = 20kHz, I_{OFF} = 80A, R_G = 3Ω

Due to the increased current fall-time, the snubber capacitor did not have any appreciable effect in reducing turn-off switching loss. Therefore, the test was repeated with different values of snubber capacitors ranging from 2.2nF to 47nF and the corresponding IGBT waveforms were observed. Snubber capacitors were chosen with low effective series resistance (ESR) and effective series inductance (ESL), and these were mounted directly across the collector-emitter terminals of the IGBTs. Figure 4.5 shows the experimental waveforms of the HV side converter with 47nF snubber capacitors. The turn-off switching transient of a converter IGBT with a 47nF snubber is shown in Figure 4.6.

It is apparent that the experimental snubber capacitor alters the turn-off behaviour significantly. The tail current duration becomes longer with the introduction of the snubber capacitor. In order to reduce the tail current duration, the IGBT gate resistance was varied from 3Ω to 4Ω, 5Ω, 6.8 Ω and 8.2Ω. It was found that an increased gate resistance reduces the tail current duration. However, the initial current fall increases causing extra switching losses. As a result, no significant improvement in turn-off loss was observed with increases in gate resistance. Moreover, reducing the gate resistance below 3Ω did not reduce turn-off losses either.

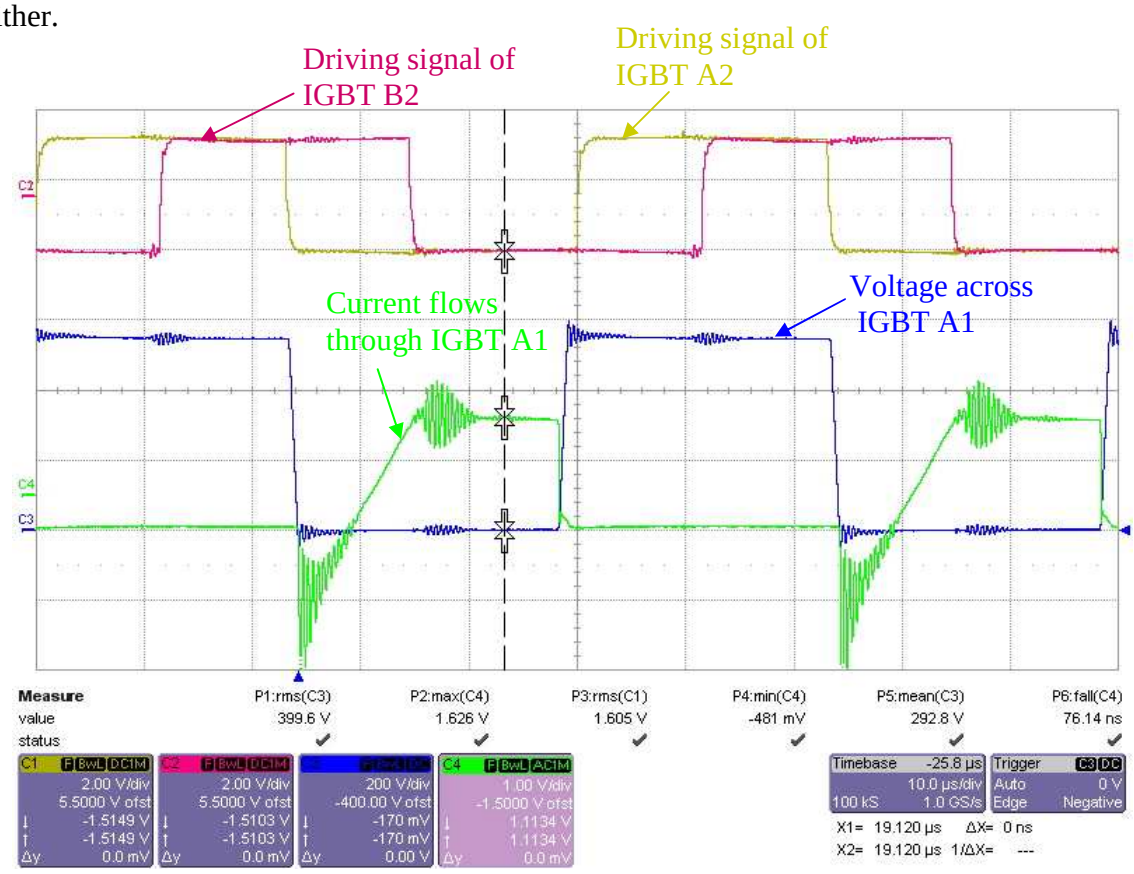


Figure 4.5 Experimental waveforms of HV side converter with a 47nF snubber capacitor
V_{in} =540V, I_{in} = 1.318A, L = 39µH, f_s = 20kHz, V_{Lrms} = 363V, I_{Lrms} = 65.6A,
I_{OFF} = 80A, R_G = 3Ω, C_s = 47nF
Channel 1 (yellow) – driving signal of transistor A_2,
Channel 2 (pink) – driving signal of transistor B_2
Channel 3 (blue) – voltage of leading-leg IGBT A_1
Channel 4 (green) – current of leading-leg IGBT A_1
Channel 4 - 50A/div measured using 20mv/A Rogowski current probe

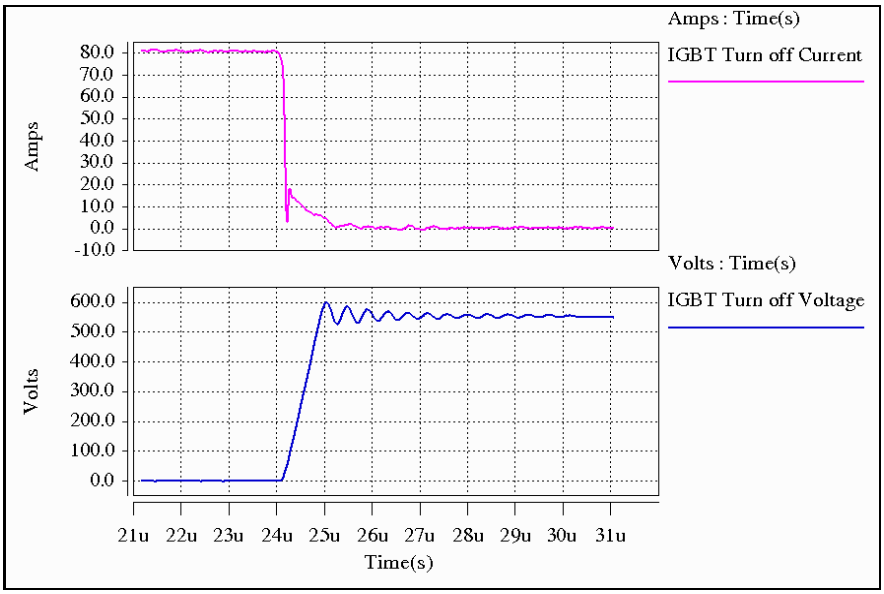


Figure 4.6 Turn-off transient of HV IGBT with a 47nF snubber
V_{in} =540V, I_{in} = 1.318A, L = 39µH, f_s = 20kHz, I_{OFF} = 80A, V_{Lrms} = 363V, I_{Lrms} = 65.6A, R_G = 3Ω, C_s = 47nF

Oscillations due to circuit stray inductance and snubber capacitance were observed during the switching process, see Figure 4.5. Although the snubber capacitors introduced ringing, a considerable reduction in switching loss was observed. The predicted turn-off loss without the snubber is 72W per IGBT and the measured loss without the snubber was 67W for the operating condition mentioned in Figure 4.3. The snubber capacitor significantly reduces the turn-off losses by limiting the *dv/dt*. This is apparent from Figure 4.6. The measured loss with the snubber was 37W. The switching loss with the snubber capacitors connected was 55% of that without capacitors, which is significantly more than predicted (20%) due to the increase in tail current with the lower *dv/dt*.

4.2.2 Estimation of power losses

The experimental power loss breakdown for the HV bridge converter, at 16.6kVA operation is plotted in Figure 4.7. Two cases have been considered: the first with a 47nF snubber capacitor connected across each of the four IGBTs of the HV side bridge and the second without the snubber capacitor. Turn-off losses for these two cases are given in Table 4.1. The losses in the leading and lagging leg devices are shown separately to illustrate the effect of the difference in conduction interval of the devices. Power losses due to the cables, busbar and connections

were omitted. Since diodes start to conduct before their anti-parallel transistors, losses due to diode reverse recovery and IGBT turn-on are negligible. From Figure 4.7, it can be observed that inductor copper losses the highest of the losses, despite the air core inductor having only 11 turns. Diode and IGBT conduction losses remain approximately constant with or without the snubber capacitors being present.

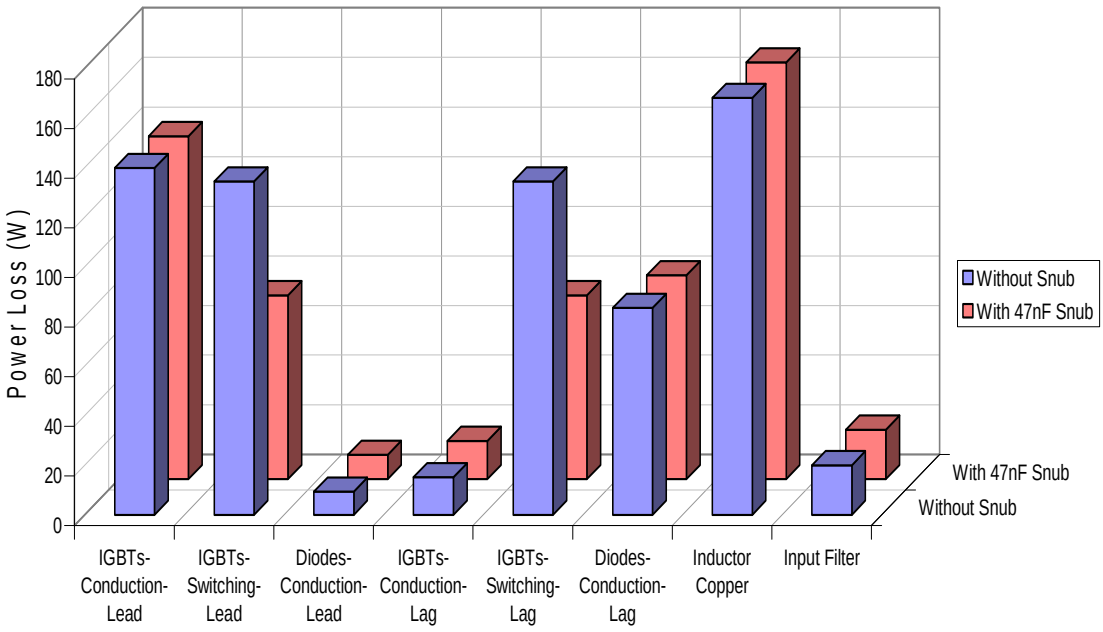


Figure 4.7 Experimental power loss distribution of HV side converter with and without snubber capacitor
V_{in} =540V, L = 39µH, f_s = 20kHz, I_{OFF} = 80A, V_{Lrms} = 363V, I_{Lrms} = 65.6A, R_G = 3Ω

Table 4.1 HV bridge turn-off loss attributes

Operation	Turn-off loss attributes							
	dv/dt **(V/µs)**	***di/dt*** **(A/µs)**	**Tail Current (A)**	**V_{max} (V)**	**Peak power loss (W)**	**Energy loss (mJ)**		
						Initial fall current	**Tail current**	**Oscillations**
Without snubber (540V,1.67A)	2580	402	13	588	28116	2.25mJ	1.11mJ	0
With 47nF snubber (540V,1.318A)	598	376	12	592	2583	11µJ	1.67mJ	175µJ

4.3 LV bridge testing

The LV side of the converter was tested using a Genesys Lambda GEN 300-11 series, 0 – 300V, 11A power supply. LV side IGBTs were subjected to a peak current of 300A at 125V. The two legs of the LV side bridge were connected through an air core inductor of value 4.17µH. The current rating of the power supply limited the maximum phase shift that could be introduced (d = 0.72) between the two half-bridge legs, and thus the turn-off current of the IGBTs. An external electrolytic capacitor bank of 19.8mF capacitance (comprised of three 6.6mF capacitor banks) was added to the DC supply to smooth the input ripple current. The LV side bridge testing circuit is depicted in Figure 4.8.

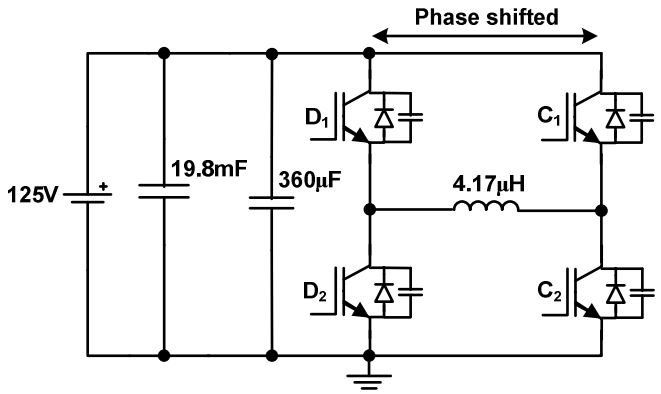


Figure 4.8 Schematic of LV bridge testing circuit

Three high current cables, each having 167A RMS current rating, were wound in parallel on a plastic former of 263mm diameter to construct the 4.17µH air core inductor.

4.3.1 Effect of snubber capacitor

Initially, the converter was tested without any snubber capacitors. Figure 4.9 shows the current and voltage waveforms of a leading-leg IGBT, and the driving signals of the IGBTs, D_2 and C_2. A CWT15 Rogowski current probe with a sensitivity of 2mV/A was used to measure the device currents. The current fall-time was measured as 205ns for the initial current fall-time, and 620ns for the tail current fall duration. This initial fall current time is much longer than the value mentioned in the datasheet. Thus, the snubber capacitor value determined during the design phase would not be sufficient to limit the switching losses. Figure 4.10 shows the turn-off transient waveforms of leading-leg IGBT C_1.

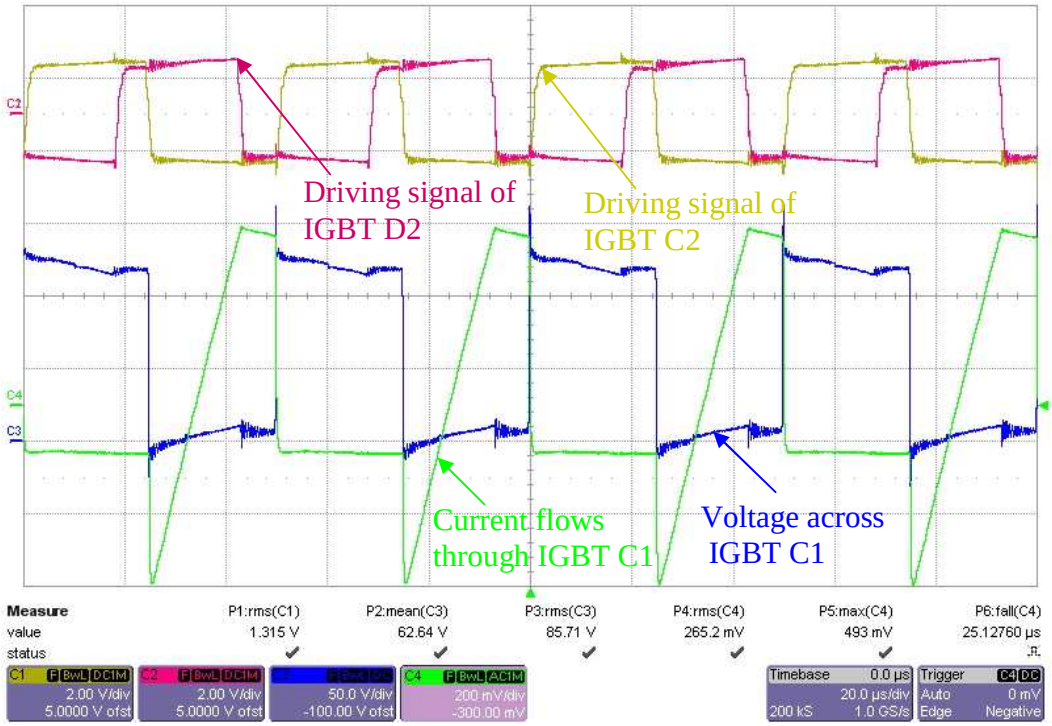


Figure 4.9 Experimental waveforms of LV side converter without snubber capacitor
V_{in} =125V, I_{in} = 10.51A, L = 4.17µH, V_{Lrms} = 106V, I_{Lrms} = 202A, f_s = 20kHz,
I_{OFF} = 300A, R_G = 2.5Ω
Channel 1 (yellow) – driving signal of transistor C_2
Channel 2 (pink) – driving signal of transistor D_2
Channel 3 (blue) – voltage of leading-leg IGBT C_1
Channel 4 (green) – current of leading-leg IGBT C_1
Channel 4 - 100A/div measured using 2mv/A Rogowski current probe

When snubber capacitors were connected across the IGBTs, severe ringing occurred in the current and voltage waveforms due to the added capacitors resonating with the stray inductances of the module (15nH – 20nH), the busbars, and the snubber capacitor connections. As a result of this ringing over current protection of the IGBTs in the gate drive was occasionally triggered and the driver then ignored the gate signals. Subsequently, the power supply protection triggered and shut down the supply. The measured frequency of ringing closely matches the value calculated from the stray inductance and snubber capacitance.

The concept behind over current protection is that the driver monitors the voltage drop across a reference resistor, R_{th}, which is connected in series with the IGBT emitter terminal for the purpose of over current/short circuit protection. The reference resistor R_{th} defines the maximum voltage drop across the turn-on transistor at which the protection function of the

driver circuit is activated and thus the power transistor is turned-off. The protection function is always active when the voltage at collector terminal exceeds the voltage at R_{th}. When the drop across R_{th} increases above the defined threshold, the driver will ignore the driving signals in order to protect the transistor from over current.

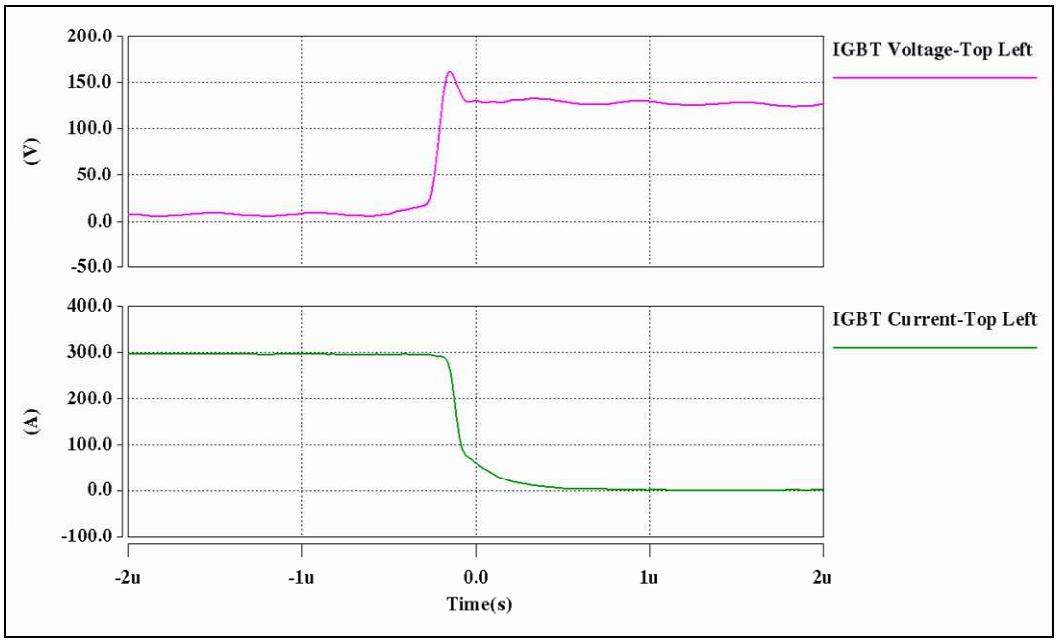


Figure 4.10 Turn-off transient of LV side IGBT without snubber capacitor
V_{in} =125V, I_{in} = 10.51A, L = 4.17µH, V_{Lrms} = 106V, I_{Lrms} = 202A, f_s = 20kHz, I_{OFF} = 300A, R_G = 2.5Ω

To avoid instantaneous supply tripping due to the ringing created by the snubber capacitor, the R_{th} reference threshold was set to a higher value. Following this, the converter was tested with snubber capacitor values varying from 47nF-220nF. However, there was no significant reduction in turn-off switching loss due to the ringing created by the snubber capacitors for the whole range of values. The 220nF snubbers were found to reduce the turn-off switching loss, but they also significantly increased the conduction loss and overall loss in the converter due to excessive ringing. Hence, it became clear that 220nF snubber capacitors were not a suitable choice. 100nF snubber capacitors were found to reduce the overall input power drawn from the source in addition to limiting the voltage rise slope. Hence, they were chosen for the LV side IGBTs. Figure 4.11 shows the experimental waveforms for LV side IGBT C_1 with a 100nF snubber capacitor. Figure 4.12 depicts the turn-off transient of IGBT C_1.

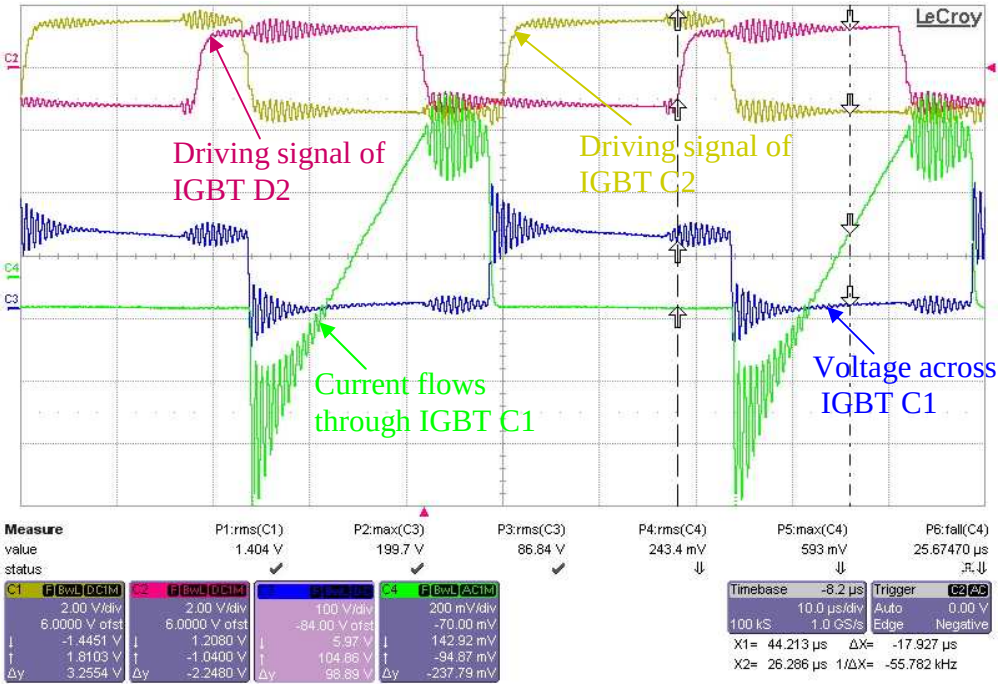


Figure 4.11 Experimental waveforms of LV side converter with 100nF snubber capacitor
V_{in} =125V, I_{in} = 9.29A, L = 4.17µH, V_{Lrms} = 106V, I_{Lrms} = 202A, f_s = 20kHz, I_{OFF} = 300A, R_G = 2.5Ω
Channel 1 (yellow) – driving signal of transistor C_2
Channel 2 (pink) – driving signal of transistor D_2
Channel 3 (blue) – voltage of leading-leg IGBT C_1
Channel 4 (green) – current of leading-leg IGBT C_1
Channel 4 - 100A/div measured using 2mv/A Rogowski current probe

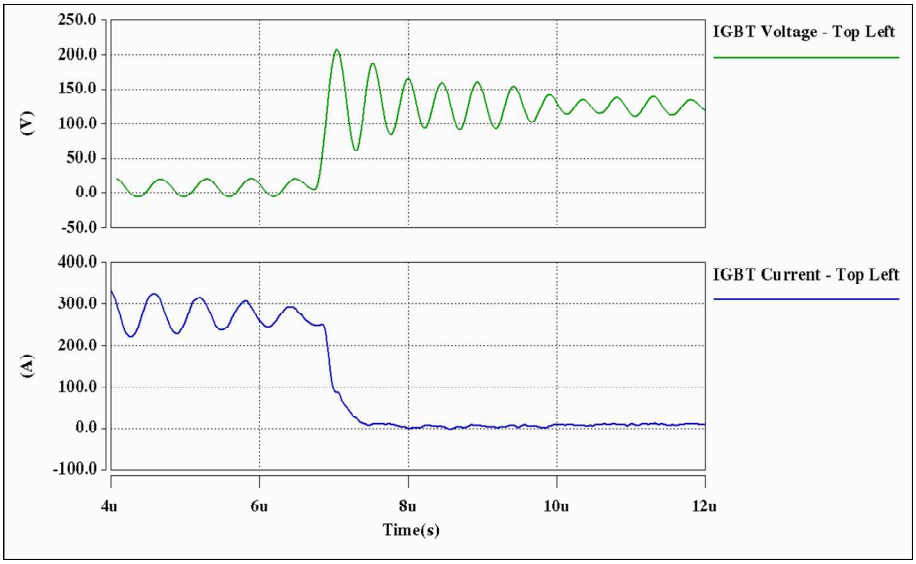


Figure 4.12 Turn-off transient of LV side IGBT with 100nF snubber capacitor
V_{in} =125V, I_{in} = 9.29A, L = 4.17µH, V_{Lrms} = 106V, I_{Lrms} = 202A, f_s = 20kHz, I_{OFF} = 300A, R_G = 2.5Ω

4.3.2 Estimation of power losses

Figure 4.13 illustrates the power loss breakdown for the LV side bridge converter at 19.2kVA operation with and without snubber capacitors, as obtained from measurements. It can be observed that the IGBT switching losses predominate. Power losses due to cables, busbars and connections are not included. When 100nF snubber capacitors were connected across the IGBTs, no significant reduction in switching losses occurred.

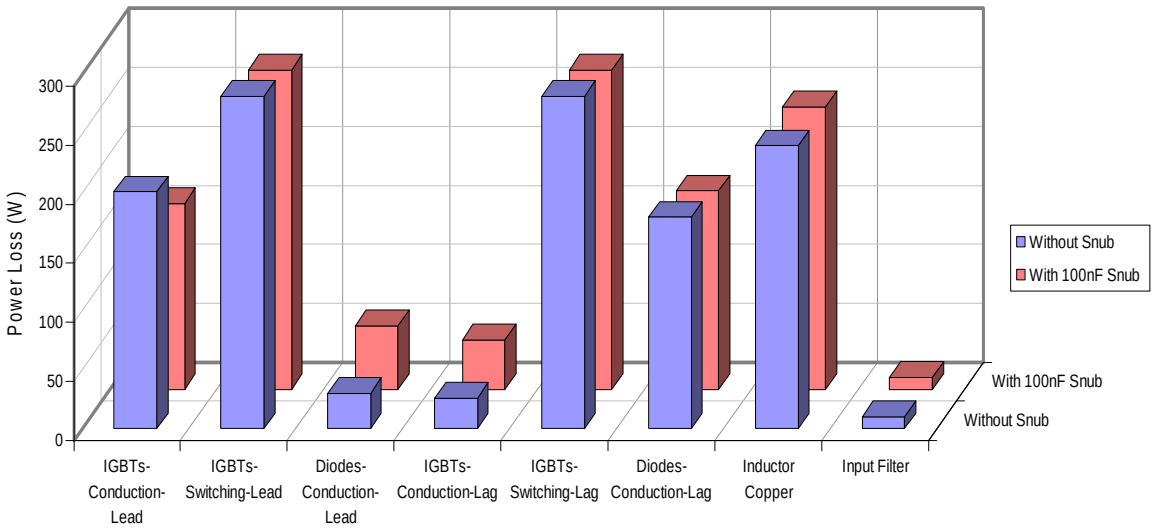


Figure 4.13 Experimental power loss distribution of LV side converter with and without snubber V_{in} =125V, L = 4.17µH, f_s = 20kHz, I_{OFF} = 300A, V_{Lrms} = 106V, I_{Lrms} = 202A, R_G = 2.5Ω

The predicted turn-off loss without snubber capacitors was 146W per IGBT and the measured loss without the capacitors was 140W for the operating condition mentioned in Figure 4.9. The measured loss with 100nF snubber capacitors was 135W. The switching loss with the snubber capacitors connected was 96.2% of that without capacitors, which is significantly more than the predicted loss (20%) due to the increase in tail current with the lower *dv/dt*. However, the turn-off loss attributes given in Table 4.2 show that there is a considerable reduction in *dv/dt* with the 100nF snubber capacitors and consequently reduced device stresses.

Table 4.2 LV turn-off loss comparison- with and without 100nF snubber capacitors

Operation	*dv/dt* (V/µs)	Tail current (A)	*di/dt* (A/µs)	V_{max} (V)	Peak power loss (W)	Energy loss (mJ)		
						Initial fall current	Tail current	Oscillations
Without snubber (125V, 10.51A)	1060	66	1112	161	44001	5.28mJ	1.52mJ	236µJ
With 100nF snubber (125V, 9.29A)	659	95	551	206	23193	3.61mJ	2.98mJ	182µJ

4.4 Experimental verification of DAB DC-DC converter

The DAB converter was tested at 1kW using a Sorensen SGI 100/50 series 100V, 50A power supply. The two bridges were interfaced through an air core inductor of value 39µH, representing the intermediate inductor/isolation transformer. The converter drew 10.9A at 100V under steady-state. To test the converter at a higher power level a 61.2µH air core inductor was used to represent the intermediate inductor/isolation transformer. A Regatron DC power supply having 500V, 160A rating [231] with a Hillstone products HLB350-48 resistive load was used for the DAB converter high power test.

4.4.1 Electromagnetic compatibility issues and their minimisation

Testing was undertaken with the 500V, 64kW high power supply. An external 19.8mF electrolytic capacitor bank (comprised of three 6.6mF capacitor banks) was connected across the power supply to smooth the input current ripple. As the supply voltage was gradually increased, high frequency oscillations in the converter waveforms were observed at 10% of the rated 500V input voltage. In order to damp the oscillations, a 1Ω, 50W resistor was added to form a R_d-C_d damping network [232]. One of the 6.6mF capacitor banks was used as C_d. But oscillations were found to be still present. Addition of an inductive filter at the input side and a capacitive filter at the output side was not beneficial. However, with the same experimental

set-up, testing with the Sorensen lower voltage power supply did not result in such high frequency oscillations.

It was deduced, through measurements using the current probes, that the Regatron Topcon power supply was the source of common mode and differential mode currents which were the cause of the oscillations. In order to overcome the problem [233, 234], the test was repeated several times with the power supply connected to various ground locations on the converter. From these tests, it was found that grounding the junction of series connections (see Figure 4.1(a)) of 4400μF electrolytic capacitors of one of the 6.6mF input filter capacitor banks was helpful in reducing the common mode current disturbances originating from the supply. The DAB converter inductor was split into two equal halves and these were connected in series with each rail of the AC link. Moreover, a 3.45mH common mode choke (CMC) [235, 236] was connected to both supply rails to provide high impedance to common mode currents flowing from the power supply. It was found that the positioning of one of the 6.6mF input capacitor banks (with no ground) before to the CMC led to an improvement in performance by suppressing the differential mode currents. With the above measures, a significant reduction of common mode and differential mode currents originating from the supply occurred. Finally, the configuration shown in Figure 3.6(d) of Chapter 3 was used, thereby a ferrite core transformer with 1:1 turns ratio was added to the AC link. 260μF capacitors were connected in series with each transformer winding to prevent DC current flow and prevent possible transformer saturation. The modified DAB converter schematic with added EMC components is shown in Figure 4.14.

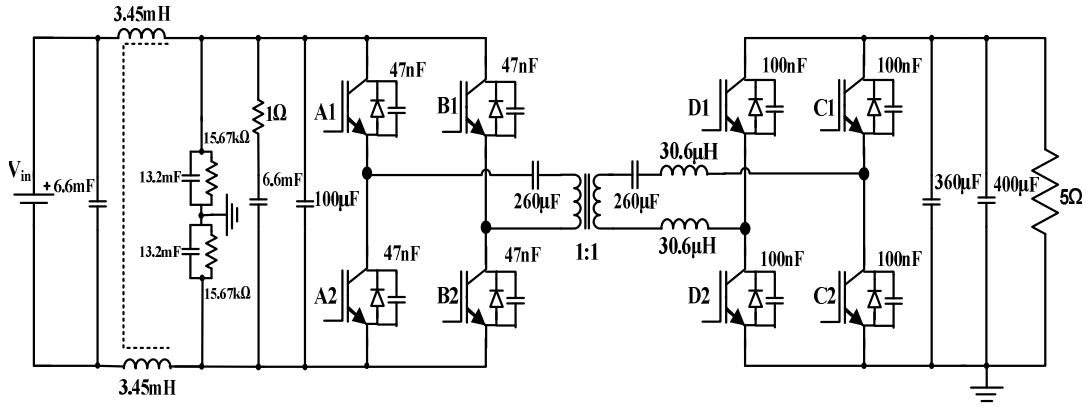


Figure 4.14 Schematic of the DAB converter with EMC components

Figure 4.15 depicts the measurements taken at 10% rated input voltage, after adopting these measures and a significant improvement was observed in the converter waveforms.

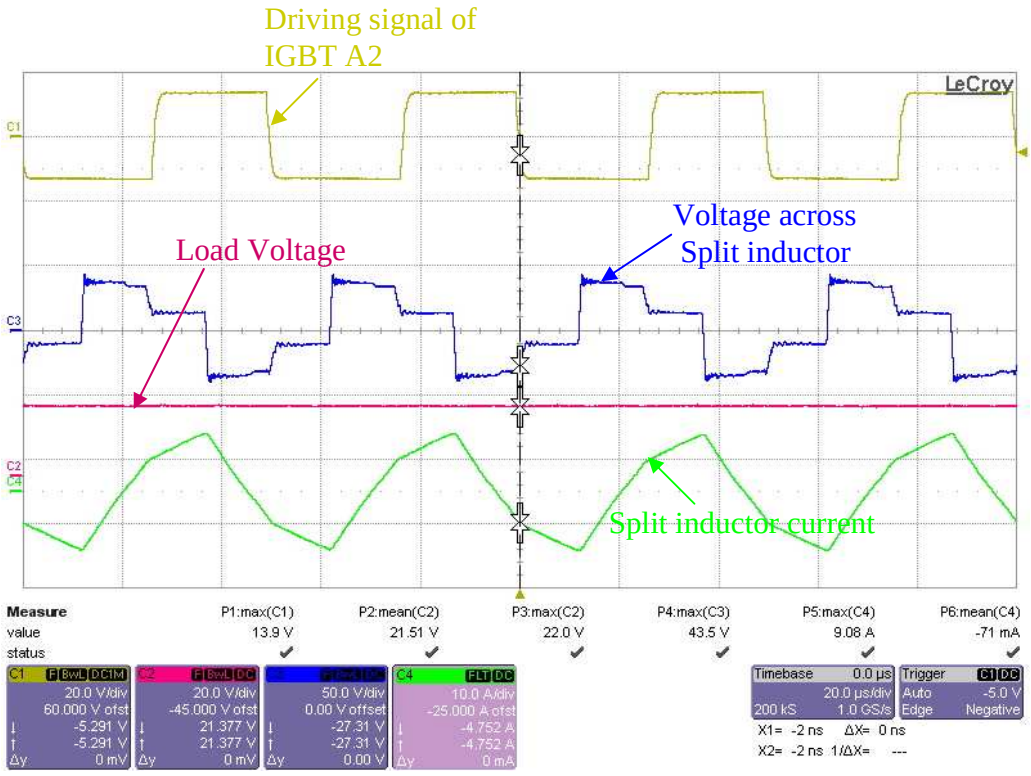


Figure 4.15 Experimental waveforms of DAB converter with EMC measures
V_{in} =50V, L = 61.2µH, f_s = 20kHz, V_0 = 25.5V, R = 5Ω, $C_{S\text{-}HV}$ = 47nF, $C_{S\text{-}LV}$ = 100nF
Channel 1 (yellow) – driving signal of transistor A_2
Channel 2 (pink) – load voltage
Channel 3 (blue) – voltage across the split inductor
Channel 4 (green) – current flow through the split inductor
Channel 4 - 10A/div measured using 2mv/A Rogowski current probe

4.4.2 Steady-state waveforms

In this section, measured waveforms of the DAB converter prototype during steady-state operation are compared with theoretical estimations and SABER simulations. Figures 4.16 to 4.20 show measured and simulated waveforms at 7kW power flow with d = 0.5. The transformer used for the experiment (shown in Figure 4.14) is a laboratory transformer designed using ferrite UU 93/152/30 core of N87 material manufactured by EPCOS. The transformer has 20 stranded turns on primary and secondary windings. A maximum allowable flux density swing of 0.6T restricts the working voltage to ±390V and thereby the power level to 7kW. All the transistors operate with a 50% duty cycle. Simulations were performed with

ideal components at a switching frequency of 20 kHz, using the schematic depicted in Figure 4.14. Figure 4.16 shows the AC link voltage and current waveforms of the DAB converter. Figure 4.17 depicts the load voltage with load current and inductor current waveforms during the charging mode (buck mode). The HV and LV device voltages and currents are shown in Figure 4.18.

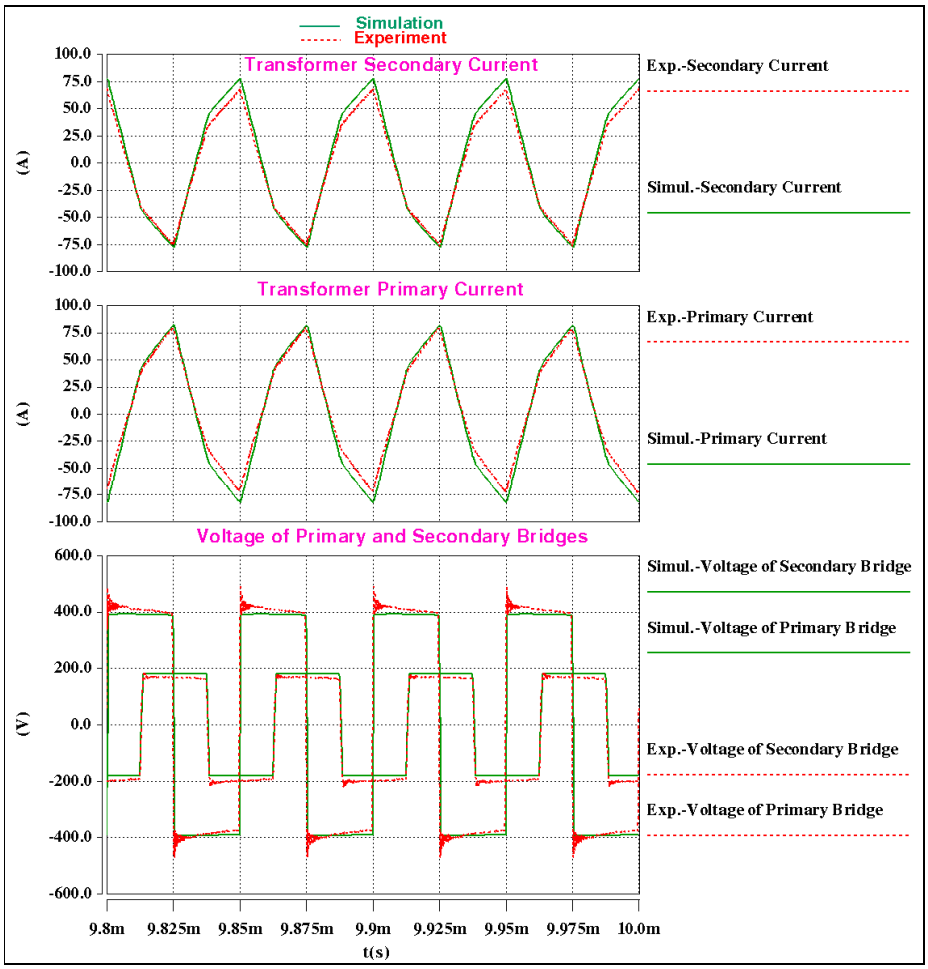


Figure 4.16 Simulated and Experimental AC link waveforms of DAB DC-DC converter at d = 0.5
V_{in} =390V, V_0 = 180.77V, $L_1 = L_2$ = 30.6µH, P_{in} = 7020W, P_0 = 6327W, f_s = 20kHz, R = 5Ω
Simulation results – displayed in green lines
Experimental measurements – displayed in dotted red lines

The measured waveforms confirm the operation of the DAB converter prototype. From Figures 4.16 to 4.18, a close agreement between experimental and simulation results is visible. However, the measured device currents and voltages exhibit ringing due to the snubber

capacitors across the devices. Parasitic inductances and capacitances were not included in the SABER simulations.

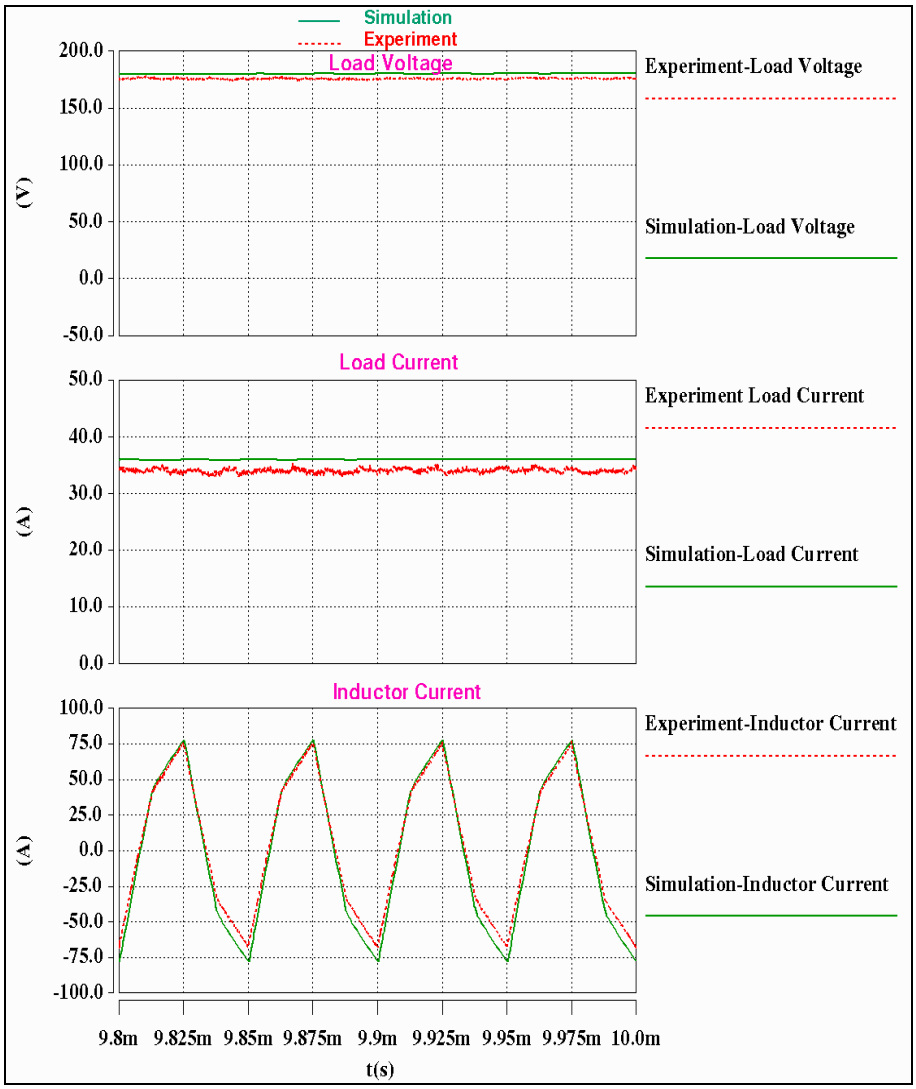


Figure 4.17 Simulated and Experimental output waveforms of DAB DC-DC converter at d = 0.5
V_{in} =390V, V_0 = 180.77V, $L_1 = L_2$ = 30.6µH, P_{in} = 7020W, P_0 = 6327W, f_s = 20kHz, R = 5Ω
Simulation results – displayed in green lines
Experimental measurements – displayed in dotted red lines

A slight difference between simulated and experimental current and voltage waveforms can be observed, due to mismatches in component values, winding resistances, dead-time generation of drivers and interfacing circuit delay. Figures 4.19 and 4.20 show the turn-on and turn-off transient waveforms of the HV and LV side IGBTs respectively.

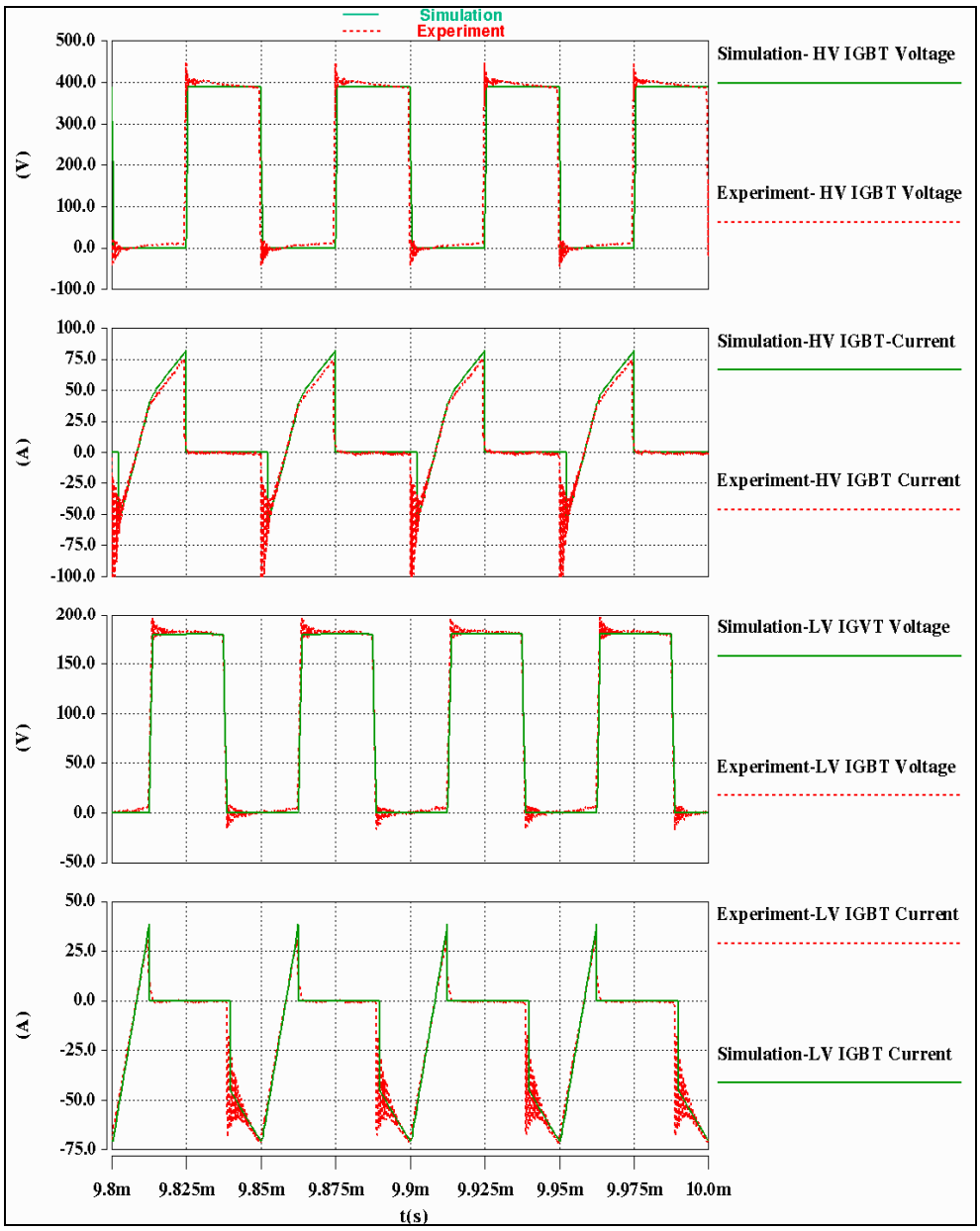
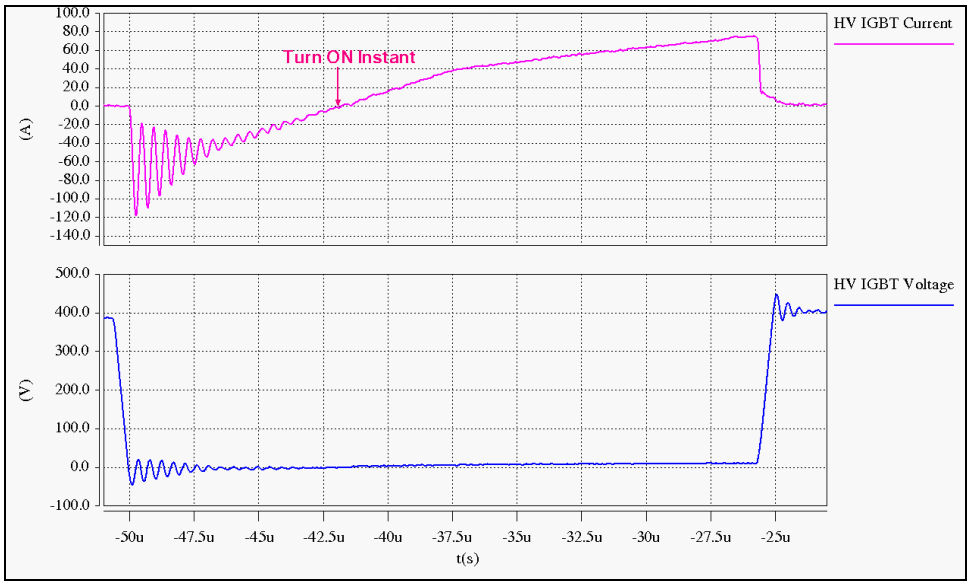


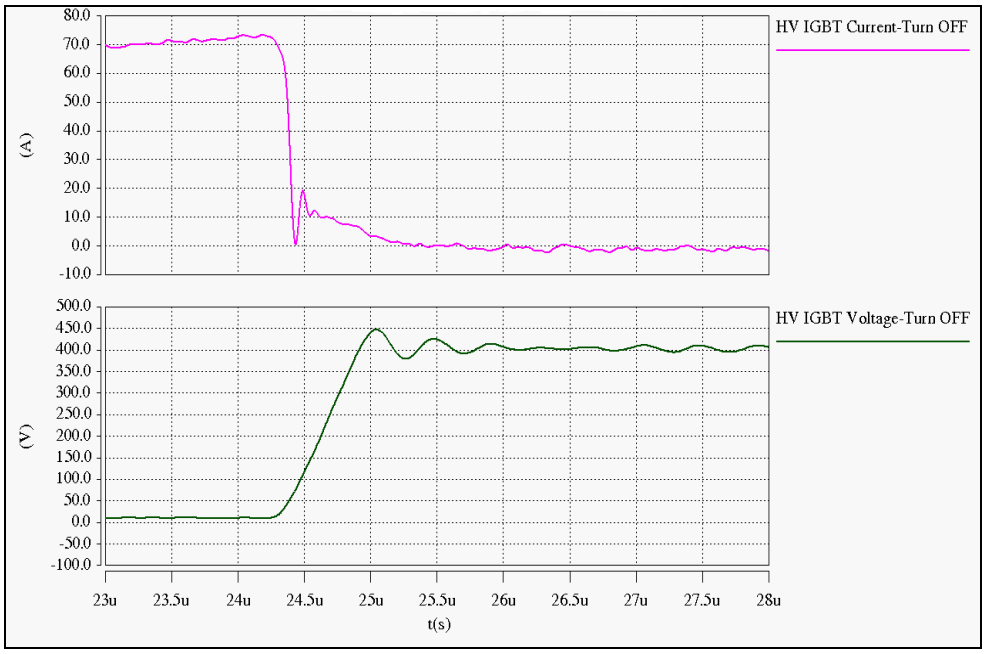
Figure 4.18 Simulated and Experimental device waveforms of DAB DC-DC converter at d = 0.5
V_{in} =390V, V_0 = 180.77V, L_1 = L_2 = 30.6µH, P_{in} = 7020W, P_0 = 6327W, f_s = 20kHz, R = 5Ω
Simulation results – displayed in green lines
Experimental measurements – displayed in dotted red lines

From Figure 4.19 (a) and 4.20 (a), it can be seen that diode conduction occurs before the transistor conducts. This ensures ZVS/ZCS turn-on of IGBTs. Moreover, the diode turns off at zero current, thus eliminating reverse recovery loss. The effect of the snubber capacitor in

limiting the voltage rising slope during device turn-off process can also be clearly seen from these figures.



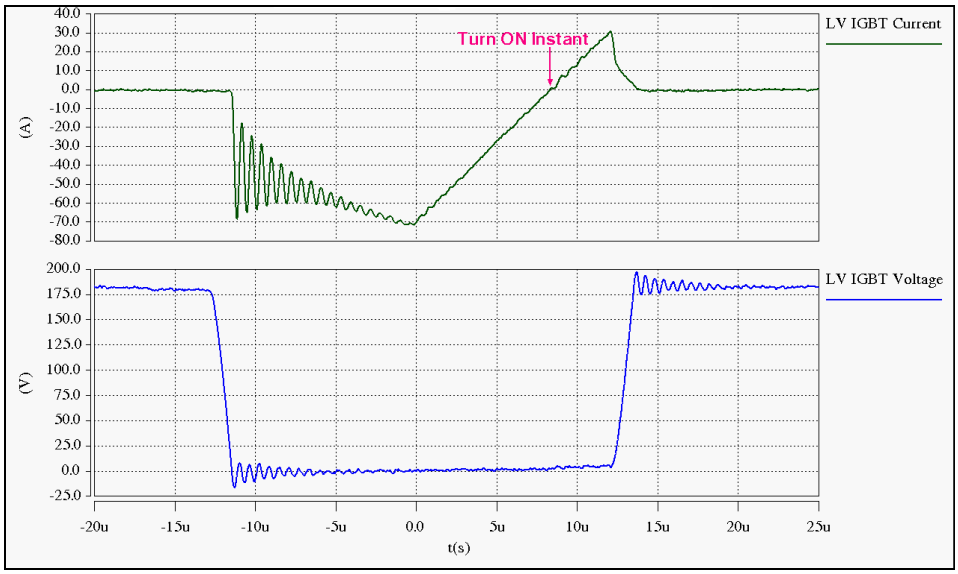
(a)



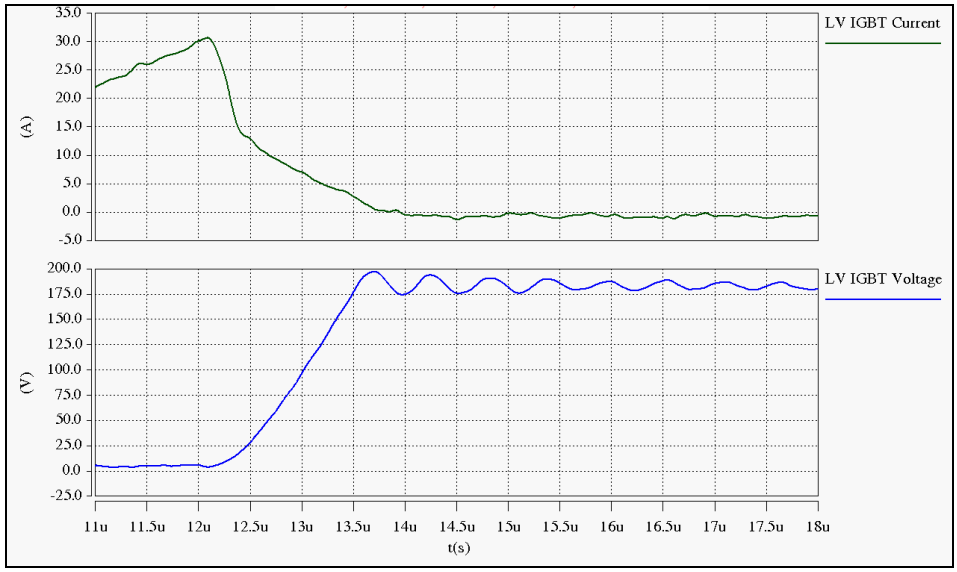
(b)

Figure 4.19 Experimental (a) Turn-on and (b) Turn-off transient waveforms of HV IGBT V_{in} =390V, V_0 = 180.77V, I_{OFF} = 73A, $L_1 = L_2$ = 30.6µH, P_{in} = 7020W, P_0 = 6327W, f_s = 20kHz, Cs = 47nF, R = 5Ω

From Figure 4.20(a), it can be observed that the duration of the diode conduction interval is longer than in Figure 4.19(a). This is due to the rectification function performed by the LV side diode of the DAB converter.



(a)



(b)

Figure 4.20 Experimental (a) Turn-on and (b) Turn-off transient waveforms of LV IGBT V_{in} =390V, V_0 = 180.77V, I_{OFF} = 31A, $L_1 = L_2$ = 30.6µH, P_{in} = 7020W, P_0 = 6327W, f_s = 20kHz, Cs = 100nF, R = 5Ω

4.4.3 ZVS boundary waveforms

Figures 4.21 to 4.26 depict the simulated and measured waveforms of the DAB converter on the ZVS boundary, with a 47nF snubber capacitor across the HV side IGBTs and a 100nF snubber capacitor across the LV side IGBTs. The ZVS boundary occurs when the duty ratio between the bridges reaches a value of d = 0.33. In the absence of a snubber capacitor, the ZVS boundary was found to be d = 0.27 from the steady-state analysis. But the switching losses due to turn-off of the transistors at peak current will be higher for no snubber capacitors, which affect the converter efficiency.

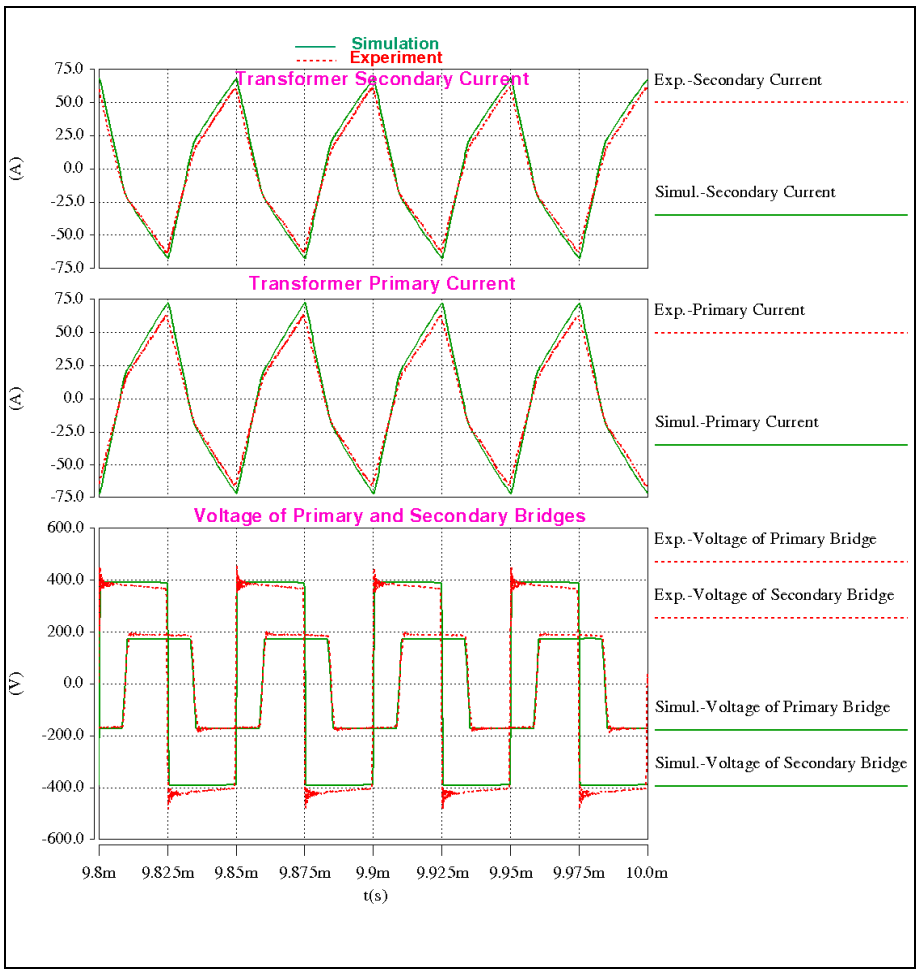


Figure 4.21 Simulated and Experimental AC link ZVS boundary waveforms of the DAB DC-DC converter
V_{in} =390V, V_0 = 174.91V, d = 0.33, $L_1 = L_2$ = 30.6µH, P_{in} = 6396W, P_0 = 5809W, f_s = 20kHz, R = 5Ω
Simulation results – displayed in green lines
Experimental measurements – displayed in dotted red lines

Figure 4.21 illustrates the AC link voltages and current waveforms of the DAB converter at ZVS boundary operation and Figure 4.22 shows the load voltage, load current and inductor current waveforms of the converter at d = 0.33. The converter operates outside the ZVS operating region shown in Figure 2.15 of Chapter 2; this is due to the converter operating with a resistive load on the LV side. ZVS boundary occurs at $V_0^{'} = 0.45$ and $I_0^{'} = 0.21$ for this operating condition. This operating point lies on the ZVS boundary for a 100nF snubber but outside the region shown in Figure 2.15. A very close agreement is visible from Figures 4.21 to 4.24 between the experimental and simulation results during ZVS boundary operation of the DAB converter.

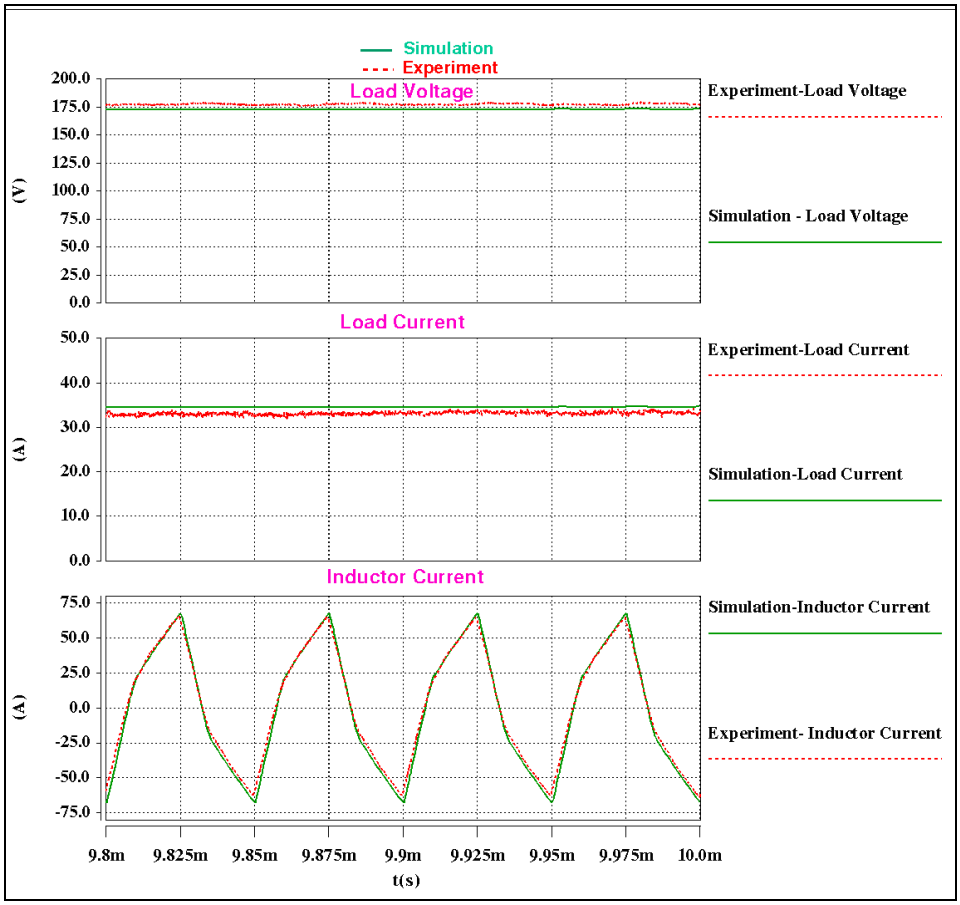


Figure 4.22 Simulated and Experimental ZVS boundary load waveforms
of DAB DC-DC converter
V_{in} =390V, V_0 = 174.91V, d = 0.33, $L_1 = L_2$ = 30.6µH, P_{in} = 6396W, P_0 = 5809W,
f_s = 20kHz, R = 5Ω
Simulation results – displayed in green lines
Experimental measurements – displayed in dotted red lines

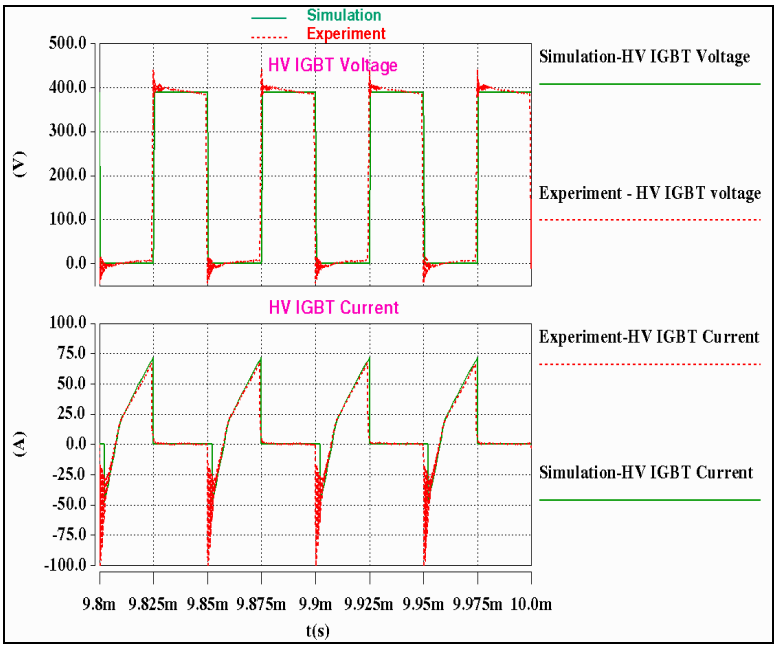


Figure 4.23 Simulated and Experimental ZVS boundary HV device waveforms
of DAB DC-DC converter
V_{in} =390V, V_0 = 174.91V, d = 0.33, $L_1 = L_2$ = 30.6µH, P_{in} = 6396W, P_0 = 5809W, f_s = 20kHz, R = 5Ω
Simulation results – displayed in green lines
Experimental measurements – displayed in dotted red lines

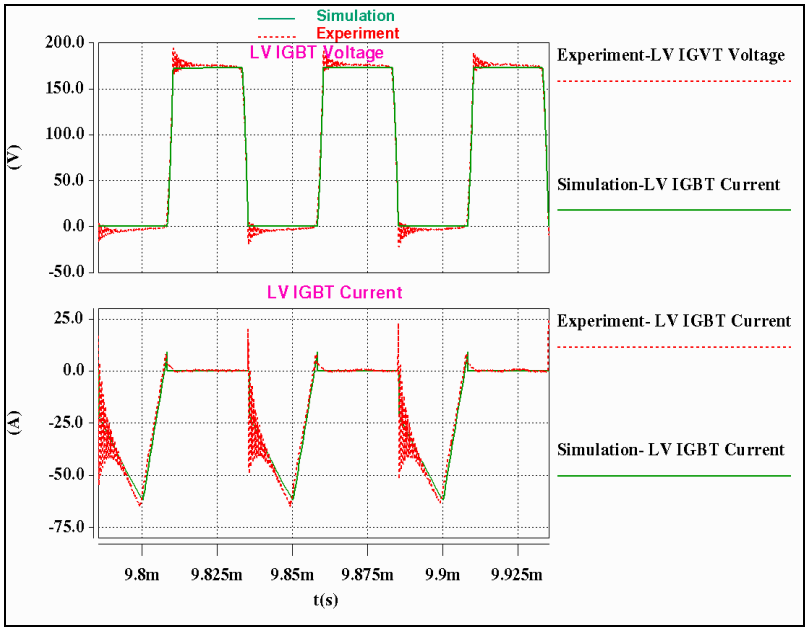


Figure 4.24 Simulated and Experimental ZVS boundary LV device waveforms
of DAB DC-DC converter
V_{in} =390V, V_0 = 174.91V, d = 0.33, $L_1 = L_2$ = 30.6µH, P_{in} = 6396W, P_0 = 5809W, f_s = 20kHz, R = 5Ω
Simulation results – displayed in green lines
Experimental measurements – displayed in dotted red lines

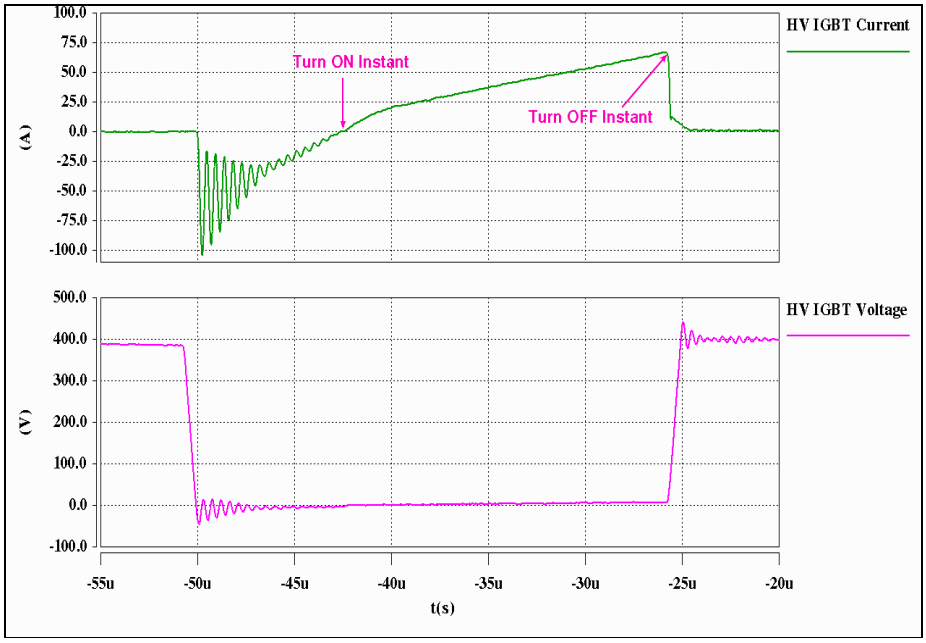


Figure 4.25 Experimental Turn-on/Turn-off transients of HV IGBT
V_{in} =390V, V_0 = 174.91V, I_{OFF} = 66A, $L_1 = L_2$ = 30.6µH, P_{in} = 6396W, P_0 = 5809W,
d = 0.33, f_s = 20kHz, Cs = 47nF, R = 5Ω

The experimental results presented in Figures 4.21 to 4.26 confirm the operation of the converter prototype on the ZVS boundary and verifies the DAB converter theory presented in Chapter 2. Parasitic ringing due to the interaction of the snubber capacitors with circuit stray inductance is absent in the simulation waveforms, as the SABER simulations correspond to ideal circuit conditions.

It can be observed from Figures 4.24 and 4.26, that positive current oscillations are present in the LV side device current waveform at turn-on of anti-parallel diode. However, the oscillations are low in magnitude, and are due to there being insufficient stored energy in the inductor to fully charge/discharge the snubber capacitor. This is because the converter is operating slightly outside the ZVS boundary, due to differences in components, resistances, duty ratios and delays in control signals between the practical system and the simulations. Overall the experimental and simulated waveforms, obtained using SABER, agree within experimental error and validate the steady-state analysis and prototype design of the DAB DC-DC converter.

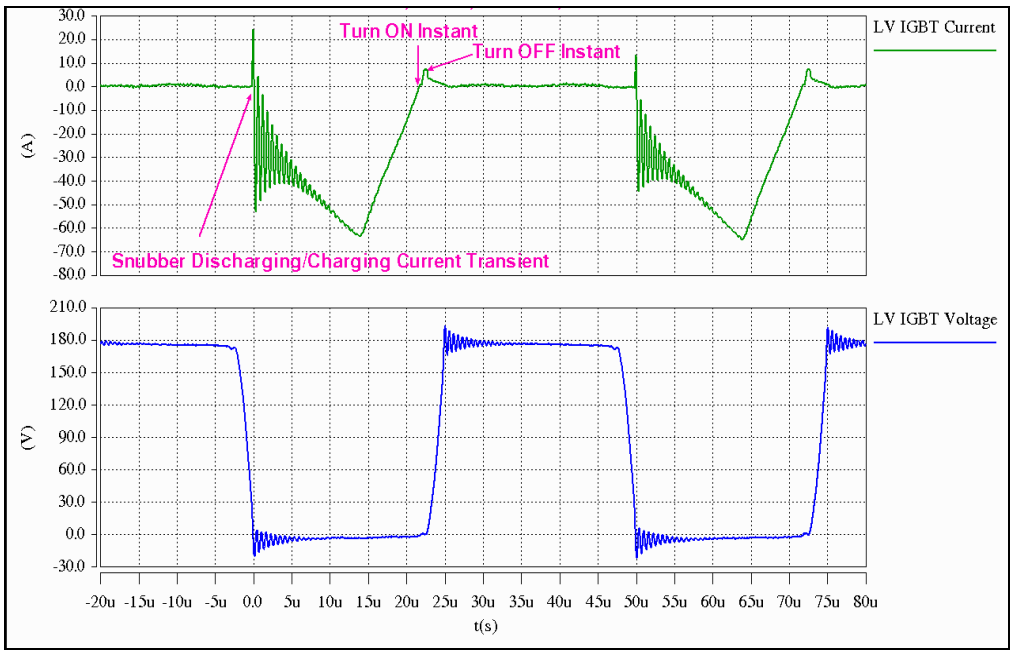


Figure 4.26 Experimental Turn-on/Turn-off transients of LV IGBT
V_{in} =390V, V_0 = 174.91V, I_{OFF} = 7.5A, $L_1 = L_2$ = 30.6µH, P_{in} = 6396W, P_0 = 5809W, d = 0.33, f_s = 20kHz, Cs = 100nF, R = 5Ω

4.4.4 Power loss distribution and converter efficiency

To calculate the converter efficiency, an estimation of device and circuit component power loss was carried out based on the measurements. Figure 4.27 shows a power loss breakdown of the DAB converter prototype at the maximum power transfer operating point viz. d = 0.5 and the ZVS boundary point (d = 0.33) with snubber capacitors present. The measured results confirm that the converter operates with an efficiency of 90.13% at d = 0.5 and 90.82% under ZVS boundary at d = 0.33. Although snubber capacitors were used across all the IGBTs, the switching losses of the HV IGBTs are very high when compared to other converter losses as highlighted in Figure 4.27. As before, power losses due to cable, busbar and connection resistances were neglected. The RMS and averaging functions of the digital scope were used to determine the RMS and mean current levels, which were then used in the power calculations. Lecroy differential voltage probes, type ADP305, Lecroy current probes, type CP150, and a Rogowski current probe, type CWT15, were used for waveform measurements.

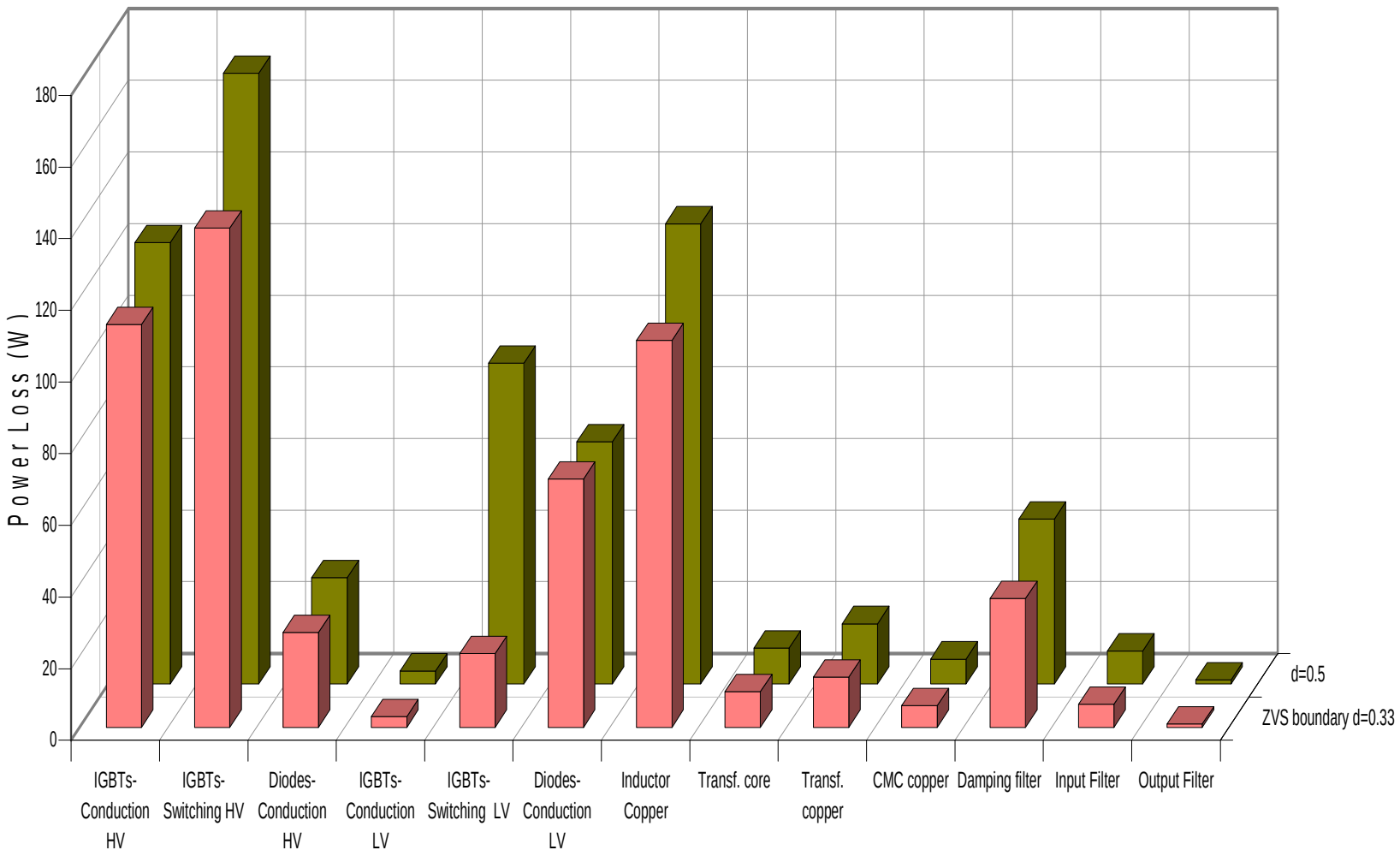


Figure 4.27 Experimental power loss distribution of DAB converter
V_{in} = 390V, f_s = 20kHz, R = 5Ω, $L_1 = L_2$ = 30.6µH , $C_{S\text{-}HV}$ = 47nF, $C_{S\text{-}LV}$ = 100nF, V_0 = 180.77V @ d = 0.5 and V_0 = 174.91V @ d = 0.33

The total loss at the maximum duty ratio was found to be 693W, which is 18.1% higher than the losses at the ZVS boundary operation of the DAB converter when snubber capacitors were present. This is mainly because of an increase in IGBT conduction and turn-off switching losses on the HV and LV sides. Diode conduction losses remain approximately constant and there is no reverse recovery loss due to ZVS operation. Copper losses incurred in the air core inductor increase as the phase shift increases, as a result of increased RMS current. Losses in the filters remain approximately constant and are of low value due to the small ESR of the filter capacitors.

A comparison of theoretical device conduction losses and passive component losses, with the experimental loss per device, at 7kW through put, is shown in Figure 4.28. A close agreement can be observed in Figure 4.28, which confirms the accuracy of the analysis.

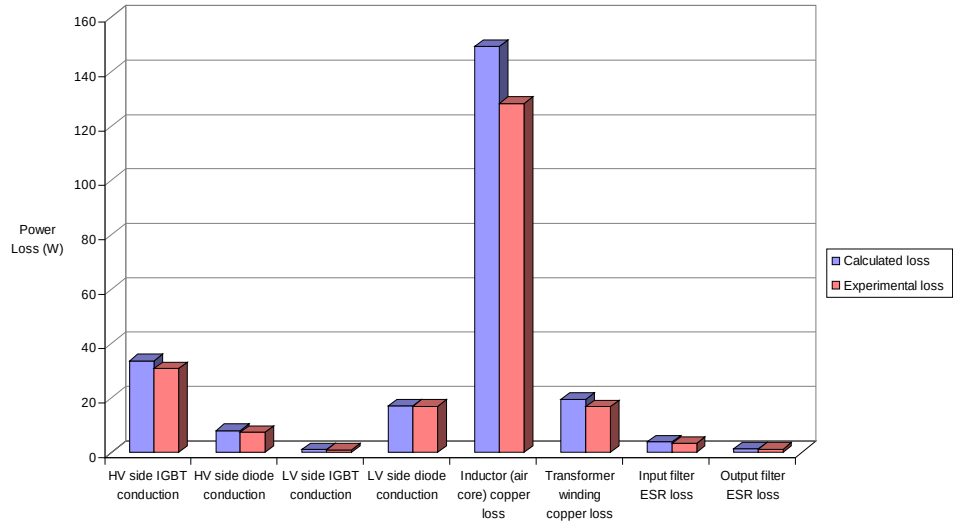


Figure 4.28 Comparison of loss predicted from the analysis with experimental losses
V_{in} =390V, V_0 = 180.77V, $L_1 = L_2$ = 30.6µH, P_{in} = 7020W, P_0 = 6327W, f_s = 20kHz, R = 5Ω

4.5 Summary

Detailed testing of the DAB converter prototype has been presented in this chapter. Initially, the HV side bridge was tested as a DC-AC converter at 540V, 80A peak current. Loss estimation of devices with and without snubber capacitors alongside various gate resistors was performed. Using snubber capacitors on the HV side converter resulted in a nearly 45% reduction in IGBT switching losses. The LV side of the converter was tested at 125V, with

600A peak to peak current and with IGBT turn-off currents of 300A. Again, device losses were accounted for with and without snubber capacitors. Introducing snubber capacitors on the LV side devices created parasitic ringing, and no significant reduction in switching power losses was observed. However, snubbers on the LV side did reduce device stresses by limiting the *dv/dt*.

Subsequently, low power testing of the DAB converter was undertaken followed by high power testing which involved dealing with electromagnetic compatibility issues. Measures were taken to overcome EMC problems such as inclusion of damping devices, common mode chokes, additional input and output filters, split inductors and a transformer. Blocking capacitors were added in series with both the primary and secondary windings of the transformer to avoid saturation. The DAB converter was tested up to 7kW, as a proof of concept, demonstrating the correctness of the steady-state analysis. A maximum flux density swing of 0.6T in the ferrite core transformer limited the working voltage to 390V, and thereby the power level to 7kW.

It has been observed that using snubber capacitors across IGBTs reduces the switching losses and device stresses and improves the converter performance. The experimental testing validated the steady-state analysis, prototype design and theoretical predictions, discussed in the earlier chapters. A close agreement between experimental waveforms and SABER simulations is evident. A power loss analysis of the DAB converter for maximum power transfer operation and the ZVS boundary operation with snubber capacitors has been presented. Measured results confirm that the converter operates with an efficiency of around 90% over the operating region.

Chapter 5
Analysis of the DAB DC-DC Converter Quasi-Square-Wave Operation

5.1 Introduction

This Chapter makes a novel contribution in deriving equations for the RMS and average device currents, and the RMS and peak inductor/transformer currents of the DAB converter operating in quasi-square-wave mode. These equations are useful in predicting the losses that occur in the devices and passive components. Although the DAB converter topology operating in square-wave mode offers various advantages as discussed in the previous Chapters; under light load conditions, the transistors are subjected to hard switching. This is because the energy stored in the coupling inductance may not be sufficient to discharge the device snubber and output capacitances. In the literature review discussed in Chapter 1, it was mentioned that additional resonant components, voltage clamping circuits and extra switching devices, were generally used to improve the soft-switching region of the DAB converter. In this Chapter, a new mode of operation is proposed to improve the soft-switching region of the converter without the need for additional components. Subsequently, the effect of ZVS region enhancement on the DAB converter performance for the new mode of operation is analysed in detail. Analysis is performed for the following three cases:

i. Imposing quasi-square-wave operation on the transformer primary voltage while retaining a square-wave voltage on the secondary side
ii. Imposing quasi-square-wave operation on the transformer secondary voltage while retaining square-wave operation on the primary side and finally
iii. Imposing quasi-square-wave operation on both transformer primary and secondary voltages

The waveform analysis for these cases is novel. Quasi-square-wave operation is realised by introducing a short dead-time in the voltage waveform on either side of the transformer, or simultaneously on both sides of the transformer. The operation of the converter was verified

through extensive SABER simulations confirming the accuracy of the analysis. Experimental results are included to support the analysis.

5.2 Quasi-square-wave applied on transformer primary

In this section, the performance of the DAB converter is analysed by imposing a quasi-square-wave voltage waveform on the transformer primary winding. The DAB converter schematic for quasi-square-wave operation on primary is shown in Figure 5.1. Dead-time is introduced in the transformer primary voltage; this is achieved by phase shifting the gate drive waveforms to the diagonal transistors of the primary H-bridge. The phase shift introduced between the diagonal devices is represented as 'δ' as shown in Figure 5.2. However, a square-wave voltage waveform is retained on the transformer secondary side in this approach.

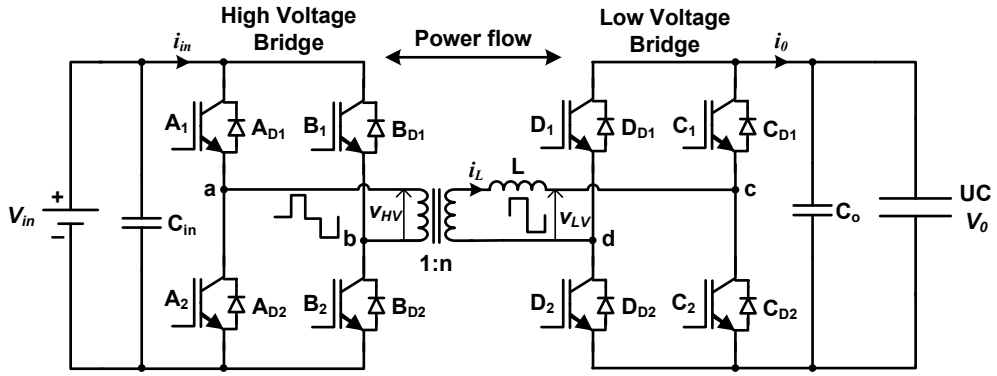


Figure 5.1 Schematic of DAB DC-DC converter with quasi-square-wave applied on transformer primary

5.2.1 Basic operation

The square-wave mode is really the quasi-square-wave mode with δ = 0. In conventional phase shift control, the parameter '*d*' that governs the phase shift introduced between the two active bridges is used to control power flow. However, in this method an additional parameter 'δ' is introduced, which influences the AC link voltage and current waveforms and controls the power flow between the two active bridges. From the Figure 5.1, the two full bridge circuits are connected through an isolation transformer and a coupling inductor L, which may be provided partly or entirely by the transformer leakage inductance. The full bridge on the

primary side operates in quasi-square-wave mode and the full bridge on the secondary side works in square-wave mode. Figure 5.2 shows the key waveforms of the DAB converter with a quasi-square-wave voltage on the transformer primary during the charging mode.

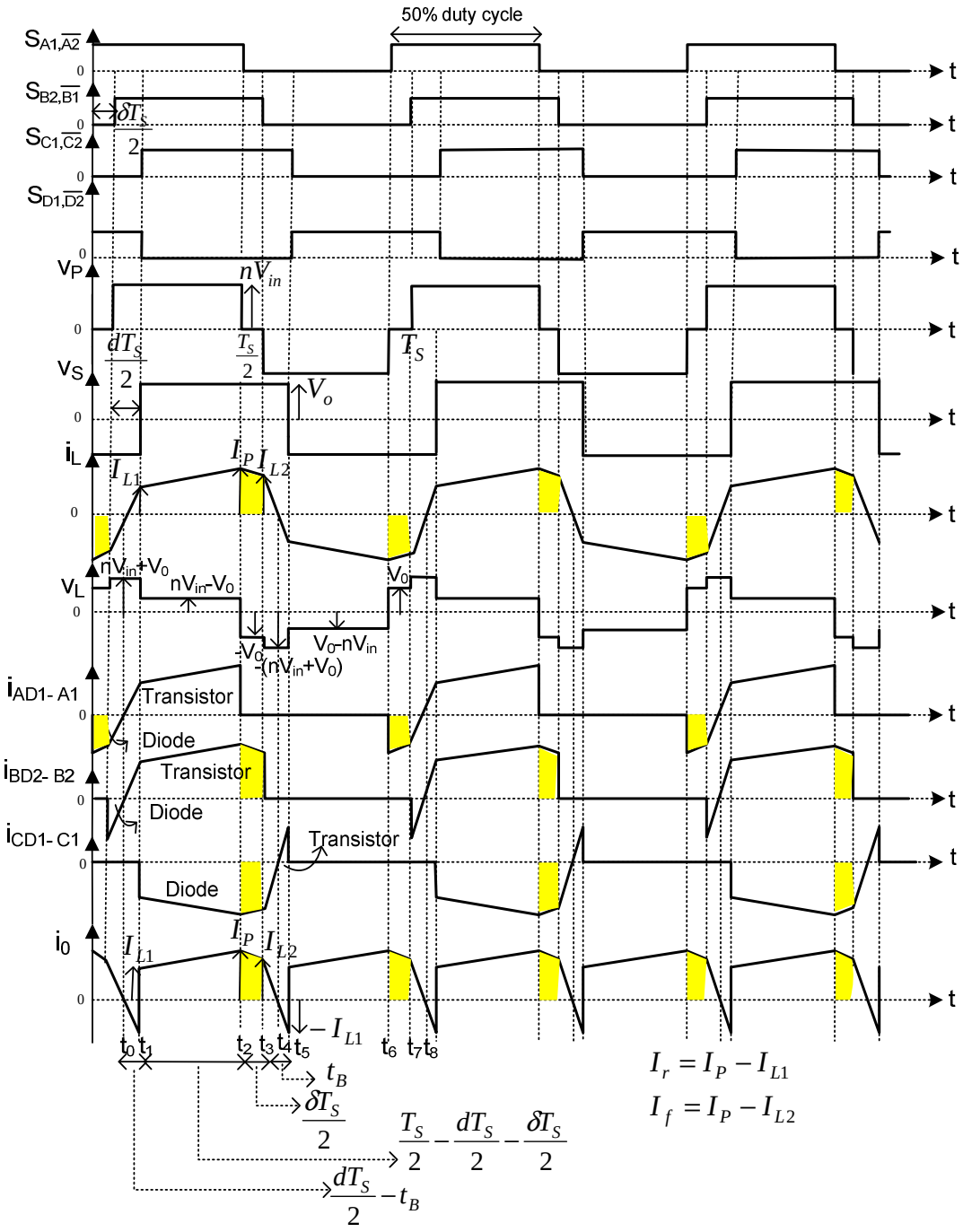


Figure 5.2 Ideal waveforms of the DAB converter for quasi-square-wave applied on transformer primary during the charging mode

The waveforms in Figure 5.2 differ by the yellow region when compared with the waveforms shown in Figure 2.2 due to the effect of dead-time introduced in the transformer primary voltage. The basic operation during charging mode is the same as described in Chapter 2 for the DAB converter with square-wave operation until the operating point t_2; therefore only the converter operation over the rest of the time period (for a half cycle) is described here. The assumptions mentioned in Chapter 2 hold good for the steady-state operation described. In Figure 5.2, gate signals of leading (S_{A1}) and lagging (S_{B2}) transistors on the primary side and gate signals of transistors S_{C1} and S_{D2} on the secondary side, voltages generated by the two bridges (V_P and V_S), the current flow through the coupling inductance i_L, the voltage across the coupling inductance V_L, the device currents $i_{AD1\text{-}A1}$, $i_{BD2\text{-}B2}$ on the primary side, $i_{CD1\text{-}C1}$ on the secondary side and the LV side terminal current i_0 are displayed. V_{in} is the HV bus voltage, and V_0 is the ultracapacitor voltage and n is the transformer turns ratio. The various time instants are indicated in Figure 5.2. In this mode, the primary bridge leads the secondary bridge by a period of $dT_s/2$, thereby power flows from the primary side to the secondary side.

- **$t_2 \rightarrow t_3$**

At t_2, transistor A_1 is turned-off under ZVS. The current from transistor A_1 is transferred to diode A_{D2} under ZVS. Now the current freewheels during the dead-time in transistor B_2 and diode A_{D2}. This freewheeling interval is marked yellow in the ideal waveforms depicted in Figure 5.2. On the secondary bridge side, diodes D_{D2} and C_{D1} continue to conduct and the transformer secondary voltage is retained at V_0. As a result, the inductor current falls to a peak of I_{L2}.

- **$t_3 \rightarrow t_4$**

At t_3, transistor B_2 is turned off under ZVS. The current from transistor B_2 is transferred to diode B_{D1}, hence A_{D2} and B_{D1} are conducting. Thereby the primary voltage is clamped to $-V_{in}$, whereas on the secondary bridge side, diodes D_{D2} and C_{D1} continue to conduct and the transformer secondary voltage is retained at V_0. As a result, the inductor current falls to zero and charges gradually in the opposite direction. This completes a half cycle. At t_4, the cycle is repeated, except that the corresponding opposite set of bridge transistors and diodes conduct. Table 5.1 summarises the device switching conditions for quasi-square-wave operation on the transformer primary when charging the ultracapacitor.

Table 5.1 Summary of switching conditions of devices during the charging mode for quasi-square-wave applied on transformer primary

Half cycle	Time instant	Conducting devices		ZVS Turn-on	ZVS Turn-off
		Input bridge	Output bridge		
First	t_0-t_1	A_1,B_2	C_2,D_1	A_1,B_2,C_2,D_1	
	t_1-t_2	A_1,B_2	C_{D1},D_{D2}		C_2,D_1
	t_2-t_3	A_{D2},B_2	C_{D1},D_{D2}		A_1
	t_3-t_4	A_{D2},B_{D1}	C_{D1},D_{D2}		B_2
Second	t_4-t_5	A_2,B_1	C_1,D_2	A_2,B_1,C_1,D_2	
	t_5-t_6	A_2,B_1	C_{D2},D_{D1}		C_1,D_2
	t_6-t_7	A_{D1},B_1	C_{D2},D_{D1}		A_2
	t_7-t_8	A_{D1},B_{D2}	C_{D2},D_{D1}		B_1

During the discharging mode, circuit operation reverses and the secondary bridge leads the primary bridge by a period of $dT_s/2$, see Figure 5.3. At time t_1, transistor A_2 is turned off and current is transferred from A_2 to A_{D1} under ZVS. Now the current freewheels during the dead-time of t_1-t_2 between the diode A_{D1} and transistor B_1. Operation during time intervals t_0-t_1, t_2-t_3 and t_3-t_4 are the same as for the operation described with intervals t_0-t_1, t_1-t_2 and t_2-t_3 respectively for the discharging mode in Chapter 2 of this Thesis. The waveforms are named and the various switching instants during this mode are marked in Figure 5.3. These waveforms differ by the yellow region when compared with the waveforms shown in Figure 2.3 due to the effect of dead-time introduced in the transformer primary voltage. Table 5.2 summarises the device switching conditions for a cycle during this mode. An important feature of the quasi-square-wave operation is that at any switching instant only one of the transistors will turn-off; hence the transistors have different ZVS boundary limits.

Table 5.2 Summary of switching conditions of devices during the discharging mode for quasi-square-wave applied on transformer primary

Half cycle	Time instant	Conducting devices		ZVS Turn-on	ZVS Turn-off
		Input bridge	Output bridge		
First	t_0-t_1	A_2, B_1	C_1, D_2	A_2, B_1, C_1, D_2	
	t_1-t_2	A_{D1}, B_1	C_1, D_2		A_2
	t_2-t_3	A_{D1}, B_{D2}	C_1, D_2		B_1
	t_3-t_4	A_{D1}, B_{D2}	C_{D2}, D_{D1}		C_1, D_2
Second	t_4-t_5	A_1, B_2	C_2, D_1	A_1, B_2, C_2, D_1	
	t_5-t_6	A_{D2}, B_2	C_2, D_1		A_1
	t_6-t_7	A_{D2}, B_{D1}	C_2, D_1		B_2
	t_7-t_8	A_{D2}, B_{D1}	C_{D1}, D_{D2}		C_2, D_1

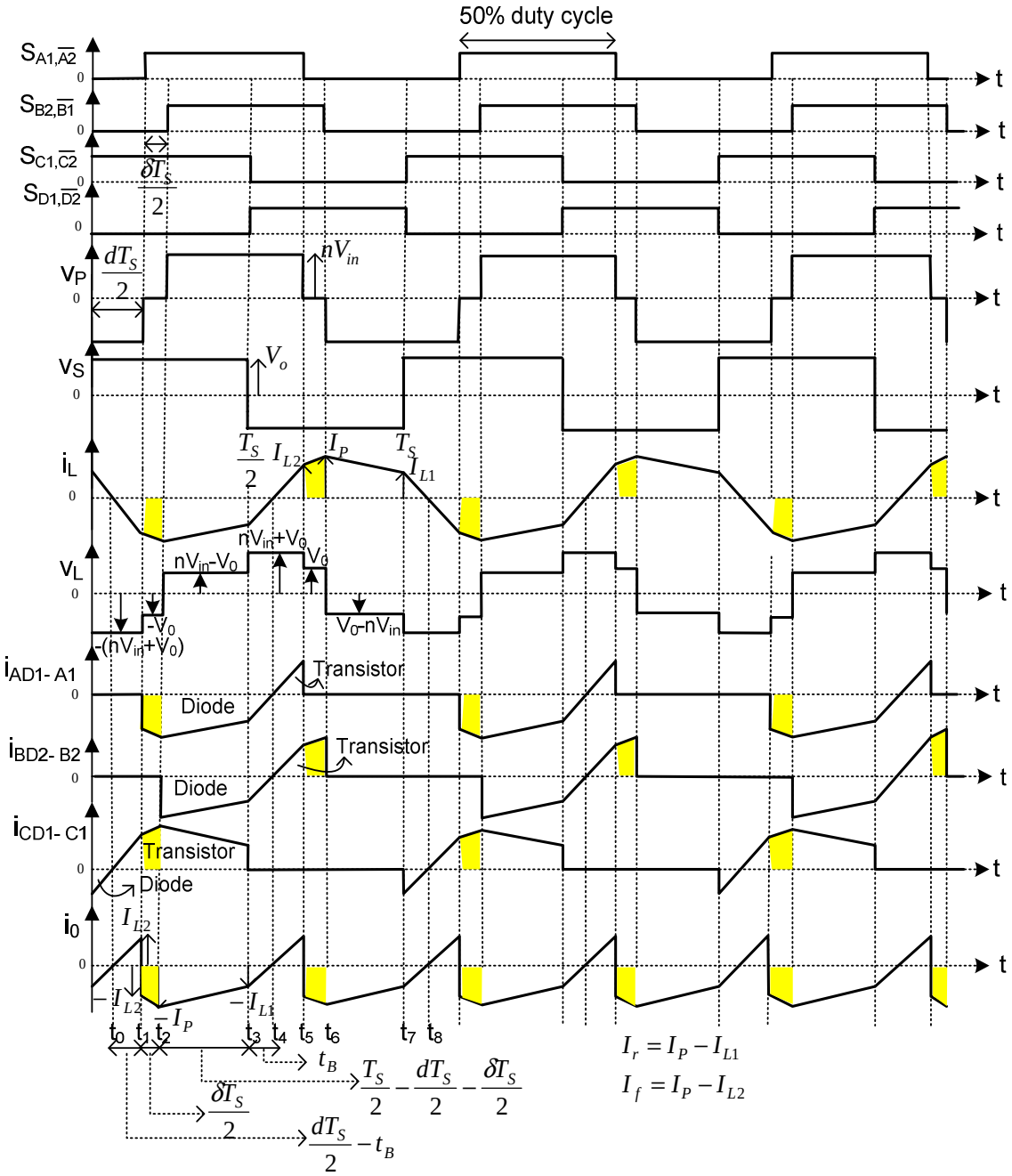
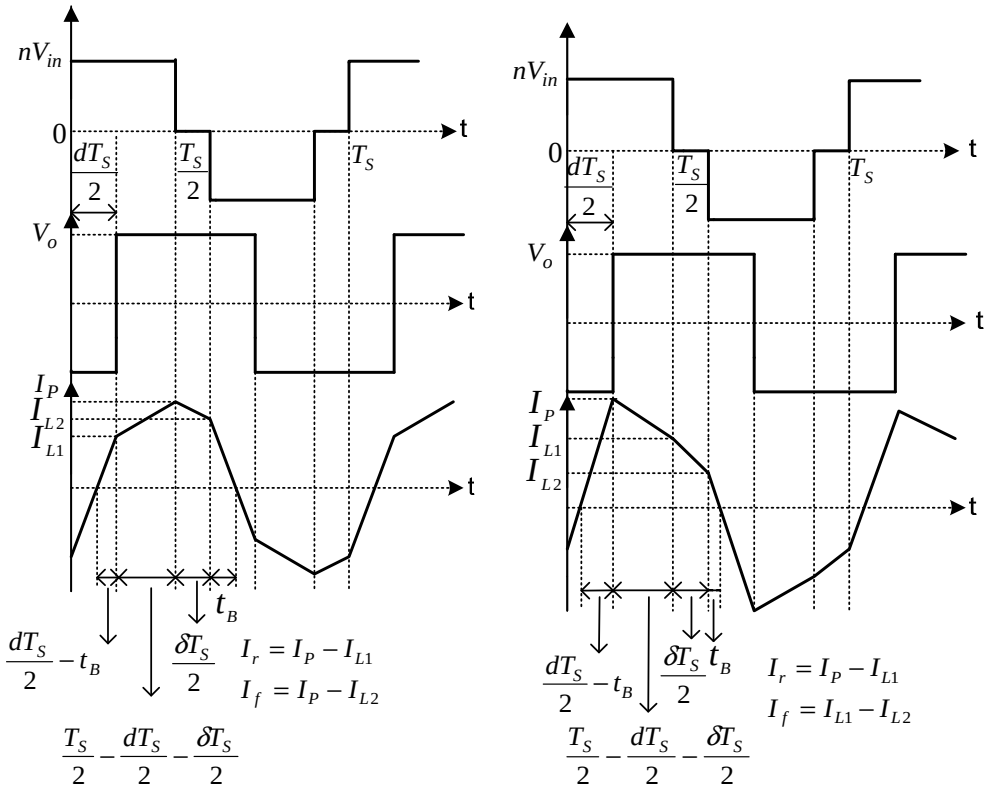


Figure 5.3 Ideal waveforms of the DAB converter for quasi-square-wave applied on transformer primary during the discharging mode

5.2.2 Mathematical model for buck and boost modes

Simplified waveforms of the DAB converter with a quasi-square-wave voltage on the transformer primary are depicted in Figure 5.4 for buck and boost modes of operation. The difference between AC link voltages is impressed across coupling inductor L. Due to half-

wave symmetry, the inductor current at various switching instants can be derived from the voltage across the coupling inductor over a half cycle. Introducing a dead-time in the transformer primary voltage makes derivation of the converter current waveform more complicated. A step-by-step analysis is given in Appendices B and C. Although buck and boost modes of operation can occur during both forward as well as reverse power flow, the analysis performed in this Chapter considers power flow in the forward direction only for buck and boost modes. This is because; the inductor current equations for various switching instants during power reversal are the same as that of forward power flow for the specified input and output voltages. During power reversal, the converter current waveforms reverse direction. Hence, expressions for reverse power flow are also given in Appendices B and C. A waveform analysis of power flow for buck and boost modes will provide two sets of current waveforms for both buck and boost modes. For succinctness, mathematical models were derived for buck and boost modes in the forward direction, assuming loss-less components and a piece-wise linear waveform for i_L, and these are given in Tables 5.3 and 5.4 respectively.



(a) Buck mode (b) Boost mode

Figure 5.4. Simplified operational waveforms of quasi-square-wave voltage on transformer primary

Table 5.3 Key equations for the buck mode – Quasi-square-wave on transformer primary

Equations
$I_{L1} = \frac{T_S}{4L}\left[nV_{in}(2d-1+\delta)+V_o\right]$
$I_{L2} = \frac{T_S}{4L}\left[nV_{in}(1-\delta)+V_o(2d-1)\right]$
$I_P = \frac{T_S}{4L}\left[nV_{in}(1-\delta)+V_O(2d-1+2\delta)\right]$
$t_B = \frac{T_S\left[nV_{in}(1-\delta)+V_O(2d-1)\right]}{4(nV_{in}+V_O)}$
$I_o = \frac{nV_{in}T_S}{2L}\left(d-d^2-d\delta+\frac{\delta}{2}-\frac{\delta^2}{2}\right)$
$I_{RMS}=\sqrt{\frac{2}{T_S}\left[\frac{(I_{L1})2\left(\frac{dT_S}{2}-t_B\right)}{3}+\left(\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}\right)\left(I_{L1}^2+\frac{I_r^2}{3}+I_{L1}I_r\right)+\frac{\delta T_S}{2}\left(I_P^2+\frac{I_f^2}{3}-I_PI_f\right)+\frac{I_{L2}^2t_B}{3}\right]}$
$I_{L1} = \frac{T_S}{4L}\left[nV_{in}(2d-1+\delta)+V_O\right] \geq 0$, condition for ZVS
$d \geq 0.5-\frac{\delta}{2}-\frac{V_O^{'}}{2}$, duty ratio at which ZVS occurs

Table 5.4 Key equations for the boost mode – Quasi-square-wave on transformer primary

Equations
$I_{L1} = \frac{T_S}{4L}\left[nV_{in}(1-\delta)+V_O(2d-1+2\delta)\right]$
$I_{L2} = \frac{T_S}{4L}\left[nV_{in}(1-\delta)+V_O(2d-1)\right]$
$I_P = \frac{T_S}{4L}\left[nV_{in}(2d-1+\delta)+V_O\right]$
$t_B = \frac{T_S\left[nV_{in}(1-\delta)+V_O(2d-1)\right]}{4(nV_{in}+V_O)}$
$I_O = \frac{nV_{in}T_S}{2L}\left(d-d^2-d\delta+\frac{\delta}{2}-\frac{\delta^2}{2}\right)$
$I_{RMS}=\sqrt{\frac{2}{T_S}\left[\frac{I_P^2}{3}\left(\frac{dT_S}{2}-t_B\right)+\left(\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}\right)\left(I_P^2+\frac{I_r^2}{3}-I_PI_r\right)+\left(\frac{\delta T_S}{2}\right)\left(I_{L1}^2+\frac{I_f^2}{3}-I_{L1}I_f\right)+\frac{I_{L2}^2t_B}{3}\right]}$
$I_{L2} = \frac{T_S}{4L}\left[nV_{in}(1-\delta)+V_O(2d-1)\right] \geq 0$, condition for ZVS
$d \geq 0.5-\frac{0.5}{V_O^{'}}(1-\delta)$, duty ratio at which ZVS occurs

The converter waveforms are presented in Appendices B and C. Average current values of the converter are determined by dividing the area under each waveform by the length of its base. Areas above the axis are counted as positive, while areas below the axis are negative. Over any time interval, the converter current waveforms have either a triangular or trapezoidal wave shape. By splitting the waveform into triangular and trapezoidal shapes and applying their effective time intervals, equations for the average currents in the converter can be obtained. The RMS current equations were derived by the normal process of squaring, adding, dividing by the periodic time and taking the square root. Although the converter waveforms are complicated, an important attribute is that all the waveforms exhibit piecewise linearity over any time interval. Moreover, the waveforms can be split into triangular and trapezoidal regions.

By following the above steps, analytical expressions for the average and RMS currents of the DAB converter were obtained for the quasi-square-wave mode of operation. These equations are useful for predicting device losses, and losses that occur in the passive components of the DAB converter. The performance parameters of the converter, for example, average output current, peak inductor/transformer current and input (HV) and output (LV) RMS currents can be determined for any desired value of duty ratio and dead-time. The equations are also useful for selecting suitable power devices and passive components, especially sizing the input and output filter capacitors. Tables 5.5 and 5.6 provide the average and RMS equations of the converter during buck mode. Tables 5.7 and 5.8 give the average and RMS equations of the converter under boost mode. Considering the power flow in the forward direction only during boost mode, the devices on the primary are named as LV devices and the devices on the secondary are named as HV devices. A detailed derivation of the equations for inductor/transformer RMS currents, and transistor and diode currents are given in Appendix C for both buck and boost modes.

Table 5.5 Average current equations of various devices of the DAB converter under buck mode - Quasi-square-wave applied on transformer primary

Device	Average current equation
HV side leading Transistor	$\frac{\frac{1}{2}\times I_{L1}\times\left(\frac{dT_S}{2}-t_B\right)+\frac{1}{2}\times(I_{L1}+I_P)\times\left(\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}\right)}{\left(\frac{T_S}{2}-\frac{\delta T_S}{2}-t_B\right)}$
HV side leading Diode	$\frac{\frac{1}{2}\times(I_P+I_{L2})\times\frac{\delta T_S}{2}+\frac{1}{2}\times(I_{L2})\times t_B}{\left(\frac{\delta T_S}{2}+t_B\right)}$
HV side lagging Transistor	$\frac{\frac{1}{2}\times I_{L1}\times\left(\frac{dT_S}{2}-t_B\right)+\frac{1}{2}\times(I_{L1}+I_P)\times\left(\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}\right)+\frac{1}{2}\times(I_P+I_{L2})\times\frac{\delta T_S}{2}}{\left(\frac{T_S}{2}-t_B\right)}$
HV side lagging Diode	$\frac{\frac{1}{2}\times I_{L2}\times t_B}{t_B}$
LV side Transistor	$\frac{\frac{1}{2}\times I_{L1}\times\left(\frac{dT_S}{2}-t_B\right)}{\left(\frac{dT_S}{2}-t_B\right)}$
LV side Diode	$\frac{\frac{1}{2}\times(I_{L1}+I_P)\times\left(\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}\right)+\frac{1}{2}\times(I_P+I_{L2})\times\frac{\delta T_S}{2}+\frac{1}{2}\times I_{L2}\times t_B}{\left(\frac{T_S}{2}-\frac{dT_S}{2}+t_B\right)}$

Table 5.6 RMS current equations of various devices of the DAB converter under buck mode - Quasi-square-wave applied on transformer primary

Device	RMS current equation
HV side leading Transistor	$\sqrt{\frac{1}{T_S}\left[\frac{I_{L1}^2\times\left(\frac{dT_S}{2}-t_B\right)}{3}+\left(\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}\right)\times\left(I_{L1}^2+\frac{I_r^2}{3}+I_{L1}I_r\right)\right]}$
HV side leading Diode	$\sqrt{\frac{1}{T_S}\left[\left(\frac{\delta T_S}{2}\right)\times\left(I_P^2+\frac{I_f^2}{3}-I_PI_f\right)+\frac{I_{L2}^2\times(t_B)}{3}\right]}$
HV side lagging Transistor	$\sqrt{\frac{1}{T_S}\left[\frac{I_{L1}^2\times\left(\frac{dT_S}{2}-t_B\right)}{3}+\left(\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}\right)\times\left(I_{L1}^2+\frac{I_r^2}{3}+I_{L1}I_r\right)+\left(\frac{\delta T_S}{2}\right)\times\left(I_P^2+\frac{I_f^2}{3}-I_PI_f\right)\right]}$
HV side lagging Diode	$\sqrt{\frac{1}{T_S}\left[\frac{I_{L2}^2\times(t_B)}{3}\right]}$
LV side Transistor	$\sqrt{\frac{1}{T_S}\left[\frac{I_{L1}^2\times\left(\frac{dT_S}{2}-t_B\right)}{3}\right]}$
LV side Diode	$\sqrt{\frac{1}{T_S}\left[\left(\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}\right)\times\left(I_{L1}^2+\frac{I_r^2}{3}+I_{L1}I_r\right)+\left(\frac{\delta T_S}{2}\right)\times\left(I_P^2+\frac{I_f^2}{3}-I_PI_f\right)+\frac{I_{L2}^2\times t_B}{3}\right]}$

Table 5.7 Average current equations of various devices of the DAB converter under boost mode - Quasi-square-wave applied on transformer primary

Device	Average current equation
LV side leading Transistor	$\frac{\frac{1}{2}\times I_P\times\left(\frac{dT_S}{2}-t_B\right)+\frac{1}{2}\times(I_P+I_{L1})\times\left(\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}\right)}{\left(\frac{T_S}{2}-\frac{\delta T_S}{2}-t_B\right)}$
LV side leading Diode	$\frac{\frac{1}{2}\times(I_{L1}+I_{L2})\times\frac{\delta T_S}{2}+\frac{1}{2}\times(I_{L2})\times t_B}{\left(\frac{\delta T_S}{2}+t_B\right)}$
LV side lagging Transistor	$\frac{\frac{1}{2}\times I_P\times\left(\frac{dT_S}{2}-t_B\right)+\frac{1}{2}\times(I_P+I_{L1})\times\left(\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}\right)+\frac{1}{2}\times(I_{L1}+I_{L2})\times\frac{\delta T_S}{2}}{\left(\frac{T_S}{2}-t_B\right)}$
LV side lagging Diode	$\frac{\frac{1}{2}\times I_{L2}\times t_B}{t_B}$
HV side Transistor	$\frac{\frac{1}{2}\times I_P\times\left(\frac{dT_S}{2}-t_B\right)}{\left(\frac{dT_S}{2}-t_B\right)}$
HV side Diode	$\frac{\frac{1}{2}\times(I_P+I_{L1})\times\left(\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}\right)+\frac{1}{2}\times(I_{L1}+I_{L2})\times\frac{\delta T_S}{2}+\frac{1}{2}\times I_{L2}\times t_B}{\left(\frac{T_S}{2}-\frac{dT_S}{2}+t_B\right)}$

Table 5.8 RMS current equations of various devices of the DAB converter under boost mode – Quasi-square-wave applied on transformer primary

Device	RMS current equation
LV side leading Transistor	$\sqrt{\frac{1}{T_S}\left[\frac{I_P^2\times\left(\frac{dT_S}{2}-t_B\right)}{3}+\left(\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}\right)\times\left(I_P^2+\frac{I_r^2}{3}-I_P I_r\right)\right]}$
LV side leading Diode	$\sqrt{\frac{1}{T_S}\left[\left(\frac{\delta T_S}{2}\right)\times\left(I_{L1}^2+\frac{I_f^2}{3}-I_{L1}I_f\right)+\frac{I_{L2}^2\times(t_B)}{3}\right]}$
LV side lagging Transistor	$\sqrt{\frac{1}{T_S}\left[\frac{I_P^2\times\left(\frac{dT_S}{2}-t_B\right)}{3}+\left(\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}\right)\times\left(I_P^2+\frac{I_r^2}{3}-I_P I_r\right)+\left(\frac{\delta T_S}{2}\right)\times\left(I_{L1}^2+\frac{I_f^2}{3}-I_{L1}I_f\right)\right]}$
LV side lagging Diode	$\sqrt{\frac{1}{T_S}\left[\frac{I_{L2}^2\times(t_B)}{3}\right]}$
HV side Transistor	$\sqrt{\frac{1}{T_S}\left[\frac{I_P^2\times\left(\frac{dT_S}{2}-t_B\right)}{3}\right]}$
HV side Diode	$\sqrt{\frac{1}{T_S}\left[\left(\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}\right)\times\left(I_P^2+\frac{I_r^2}{3}-I_P I_r\right)+\left(\frac{\delta T_S}{2}\right)\times\left(I_{L1}^2+\frac{I_f^2}{3}-I_{L1}I_f\right)+\frac{I_{L2}^2\times t_B}{3}\right]}$

5.2.3 Performance evaluation

From the mathematical models, the performance of the DAB converter was evaluated, focussing on the ZVS operating range, average power transfer and efficiency. Since the quasi-square-wave operation influences the AC link current waveforms, it is essential to analyse its impact on converter performance. Therefore, the RMS and peak inductor/transformer current values for the proposed mode of operation are needed. The following sections discuss the DAB converter operation for a quasi-square-wave voltage applied to the transformer primary.

5.2.3.1 ZVS operating range

An interesting observation is that, under buck mode of operation, the quasi-square-wave voltage on the transformer primary increases the ZVS range of operation to more than that of the conventional square-wave mode of operation. This beneficially reduces the switching losses during buck mode of operation. A comparison of ZVS boundaries for the square-wave mode and for the quasi-square-wave mode, with different values of dead-time, is depicted in Figure 5.5. The corresponding percentage improvement in ZVS range is illustrated in Figure 5.6.

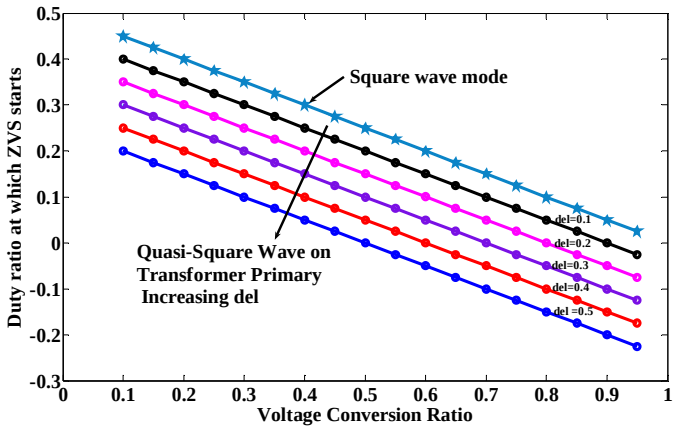


Figure 5.5 Comparison of square-wave mode ZVS boundary with quasi-square-wave mode boundary (del = δ)

It was given in Table 5.4 that the current I_{L2} decides the ZVS boundary for boost mode of operation. The parameter nV_{in} (for square-wave) is now multiplied by the term (1-δ) in the equation for I_{L2}. As a result, the magnitude of current I_{L2} decreases. Hence, the introduction of a dead-time (δ) on the transformer primary does not contribute to an increase in the ZVS

boundary during the boost mode of operation. As a result, quasi-square-wave voltage on primary degrades the converter performance during boost mode.

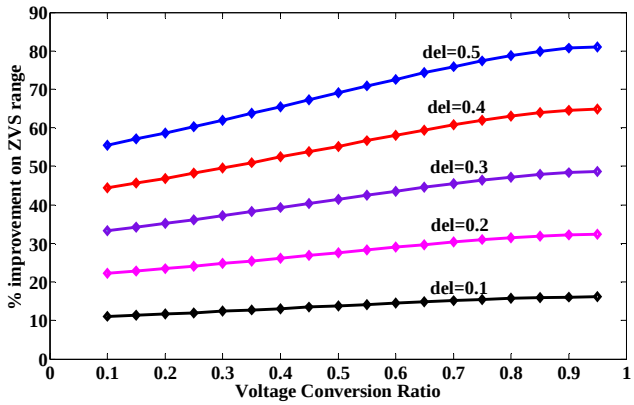


Figure 5.6 Percentage improvement in ZVS operating range for quasi-square-wave on transformer primary in comparison with square-wave mode (del = δ)

5.2.3.2 Power transfer and converter efficiency

Another interesting observation is that an increase in average power transfer is achieved, as high as 54%, for a reduced dead-time ($\delta = 0.1$) and duty ratio ($d = 0.075$) for the quasi-square-wave mode, compared to the square-wave operating mode. This was found to improve the performance and efficiency at a lower dead-time and duty ratio, which is clearly evident from Figure 5.7,which shows the power output versus ultracapacitor voltage at two values of duty ratio, with and without a dead-time. However, for a higher value of dead-time, the net power flow through the converter reduces. Figure 5.8 shows the variation of normalized average output current versus variation in duty ratio for different values of dead-time in the transformer primary. A quasi-square-wave voltage on the transformer primary shifts the performance curves towards the left, as can be seen in Figure 5.8. Hence, maximum power transfer occurs for a duty ratio of less than 0.5 for the quasi-square-wave mode of operation. As with the square-wave mode, the region on the left ($d \rightarrow 0$ to 0.5) of Figure 5.8 is of interest, since the RMS and peak currents for the given phase shift are lower than on the right-hand-side ($d \rightarrow 0.5$ to 1). For this reason it is preferable to operate on the left side of maximum power transfer operating point.

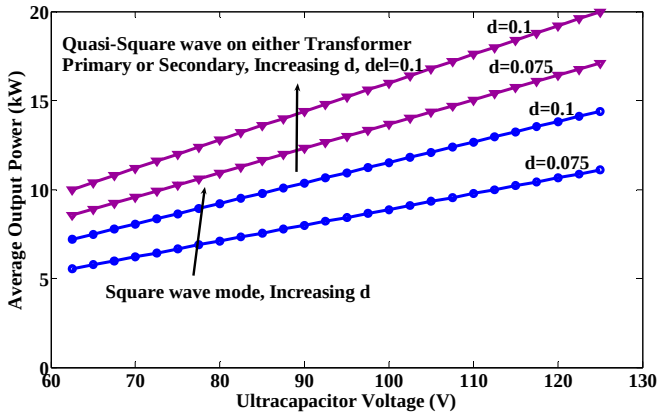


Figure 5.7 Improvement in average power transfer at reduced dead-time and duty ratio (del = δ)

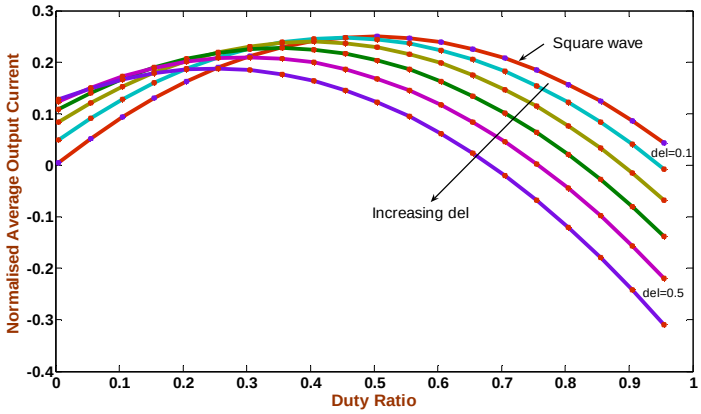


Figure 5.8 Normalised average output current vs Duty ratio for different values of δ (del = δ)

5.2.3.3 RMS and peak inductor/transformer currents

In contrast to switching losses, a notable increase in coupling inductor RMS current is observed for the proposed mode of operation. A comparison of the RMS and peak inductor currents of the DAB converter has been made at maximum power transfer for square-wave and quasi-square-wave modes of operation. Figures 5.9 and 5.10 depict the increase in RMS current and peak current flow through the coupling inductor for the proposed mode of operation, over the respective currents for the square-wave mode. Therefore, ZVS enhancement is achieved at the expense of increased device conduction losses at higher power flow. However, under light-load conditions, the proposed mode of operation increases the average power to a large extent and tends to improve the converter efficiency, as discussed in the above section. Hence, the conduction losses due to the increase in RMS currents may not degrade the converter performance under light-loads.

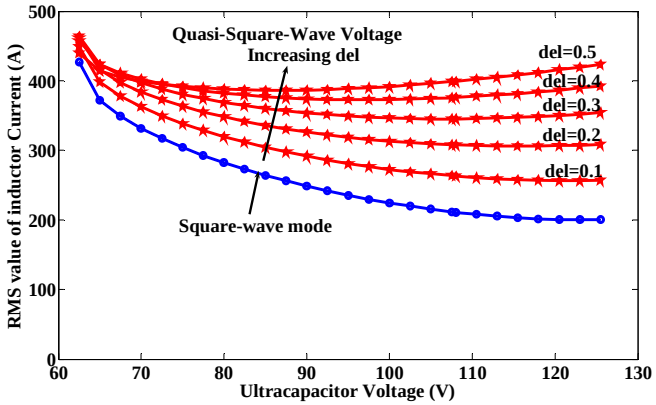


Figure 5.9 RMS value of inductor current at maximum power transfer operating condition for quasi-square-wave and square-wave modes (del = δ)

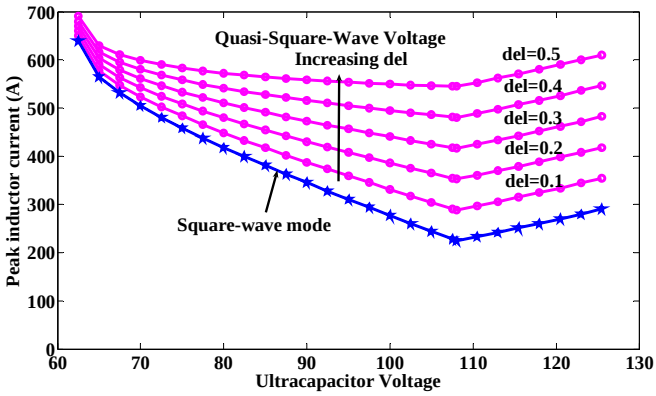


Figure 5.10 Peak value of inductor current at maximum power transfer operating condition for quasi-square-wave and square-wave modes (del = δ)

5.2.4 Simulation and Experimental results

This section presents the simulation results and experimental verification of the DAB converter with a quasi-square-wave voltage waveform on the transformer primary. These results confirm the mathematical models presented in section 5.2.2 of this Chapter. Operating conditions and circuit parameters corresponding to the simulation and experiments are given in the figure captions. Figure 5.11 illustrates the SABER simulation waveforms for the buck mode of operation. Voltages generated by the active bridges, inductor current, leading/lagging device currents on the quasi-square-wave HV side, device current on the LV side and the load current and voltages are shown. According to the mathematical analysis, the steady state

values are I_{L1} = 5.21A, I_{L2} = 23.4A, peak inductor current I_P = 26.41A, average output current I_0 = 14.7A and inductor RMS current I_{RMS} = 16.73A. These values correlate well with the SABER results, shown below. The freewheeling current interval due to the quasi-square-wave mode of operation on the HV side can be clearly seen from the lagging leg device current (I_{B1}/I_{BD1}) waveforms portrayed in Figure 5.11.

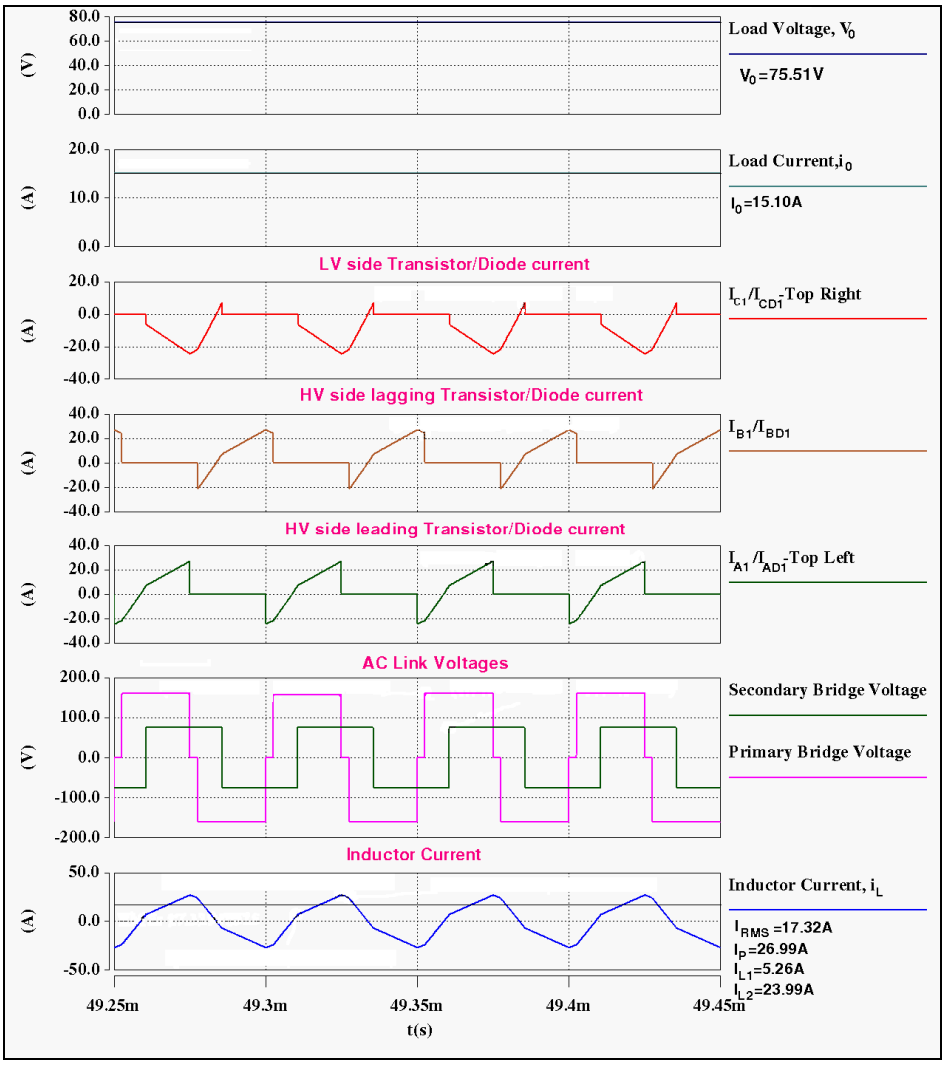


Figure 5.11 Simulation waveforms for quasi-square-wave applied on transformer primary
V_{in} = 160V, L = 61.2μH, f_S = 20kHz, P_{in} = 1kW, R = 5Ω, V_0 = 75.5V, δ = 0.1, d = 0.3

The experimental prototype designed for square-wave mode of operation, presented in Chapter 3 of this Thesis, was used to validate the quasi-square-wave mode of operation presented in this Chapter. Figures 5.12 to 5.14 depict the experimental results for a quasi-square-wave

voltage at 1kW, as a proof of concept with a 5Ω load resistor connected on the LV side. Figure 5.12 shows the voltages generated by the primary and secondary side active bridges and also primary and secondary currents of the isolation transformer. SABER simulation results are also displayed.

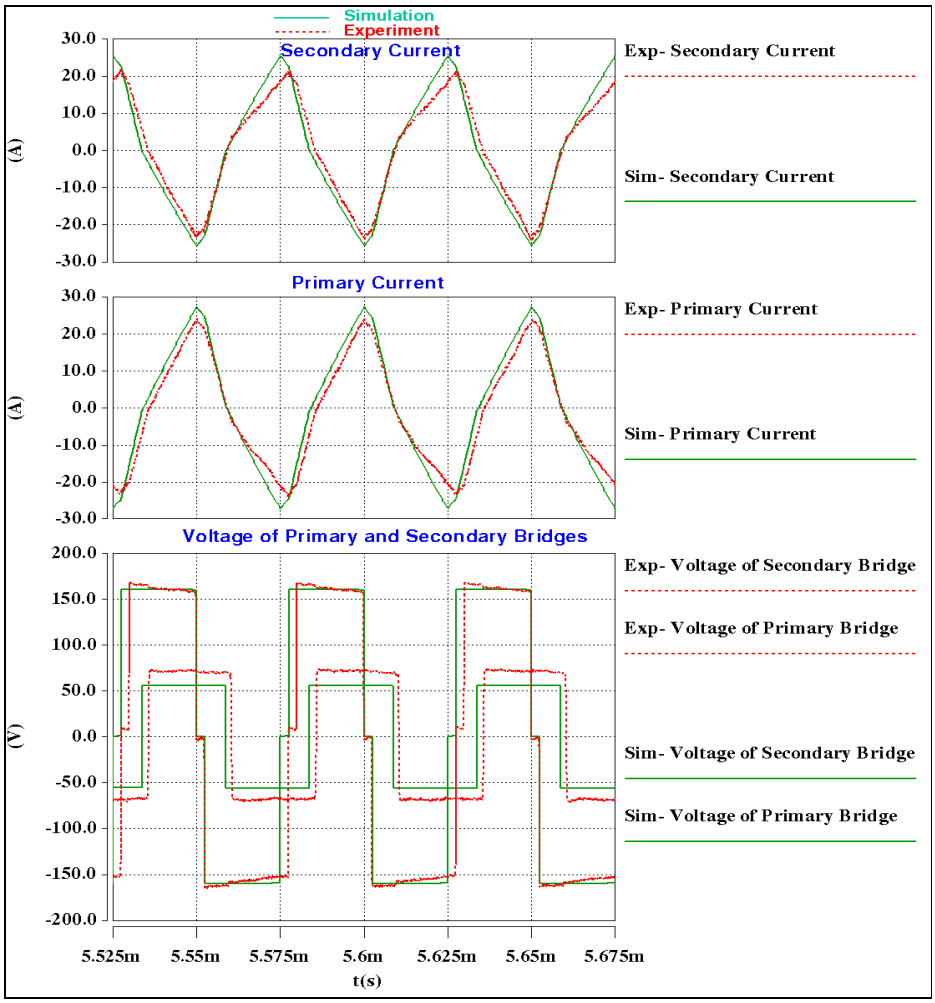


Figure 5.12 Experimental verification of AC link waveforms of the DAB converter for quasi-square-wave applied on transformer primary
V_{in} = 160V, L = 61.2μH, f_S = 20kHz, P_{in} = 1kW, R = 5Ω, V_0 = 65.45V, δ = 0.1, d = 0.3

Figure 5.13 depicts the HV side transistor and diode currents and voltages. From the waveforms, the duty cycle of the HV side transistor B_1 is seen to be greater than that of the simulation waveforms. This is due to the driver signal generation characteristics, which is subsequently explained.

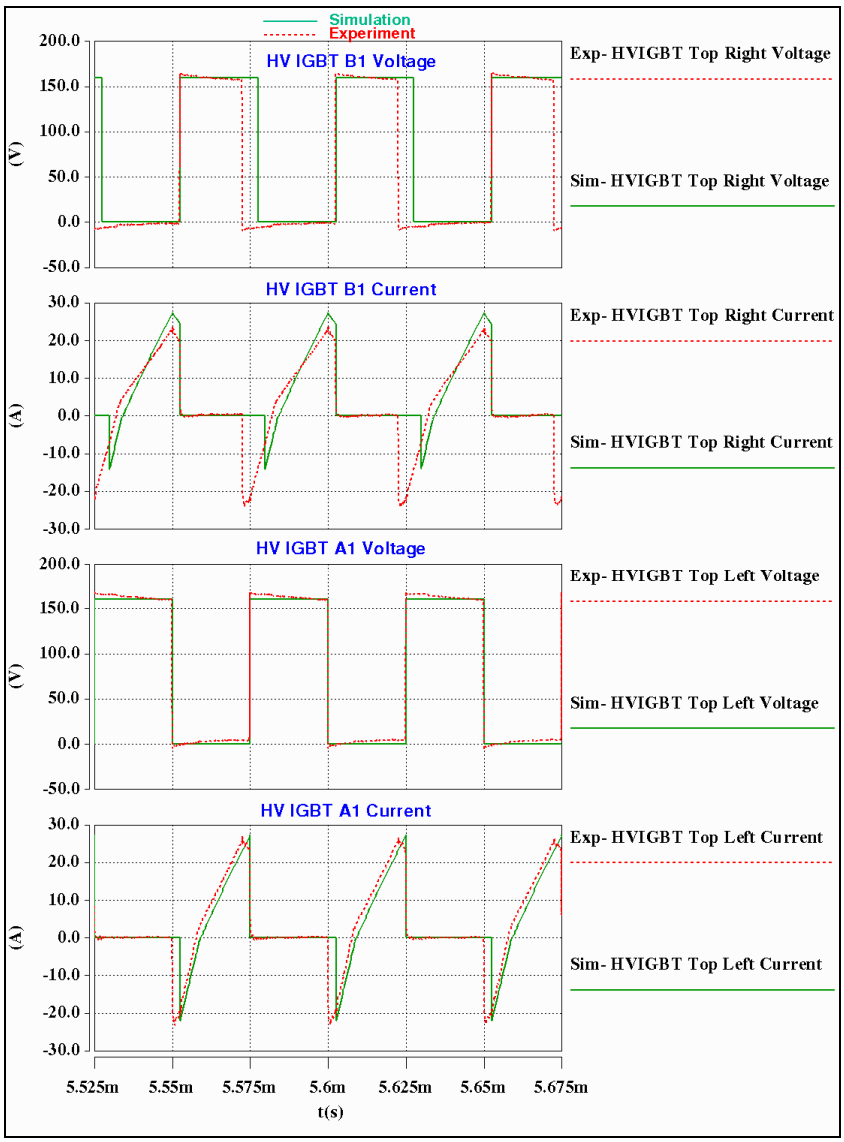


Figure 5.13 Experimental verification of HV side device waveforms of the DAB converter for quasi-square-wave applied on transformer primary
V_{in} = 160V, L = 61.2μH, f_S = 20kHz, P_{in} = 1kW, R = 5Ω, V_0 = 65.45V, δ = 0.1, d = 0.3

Figure 5.14 displays the LV device waveforms and the load voltage and current waveforms with a quasi-square-wave voltage waveform.

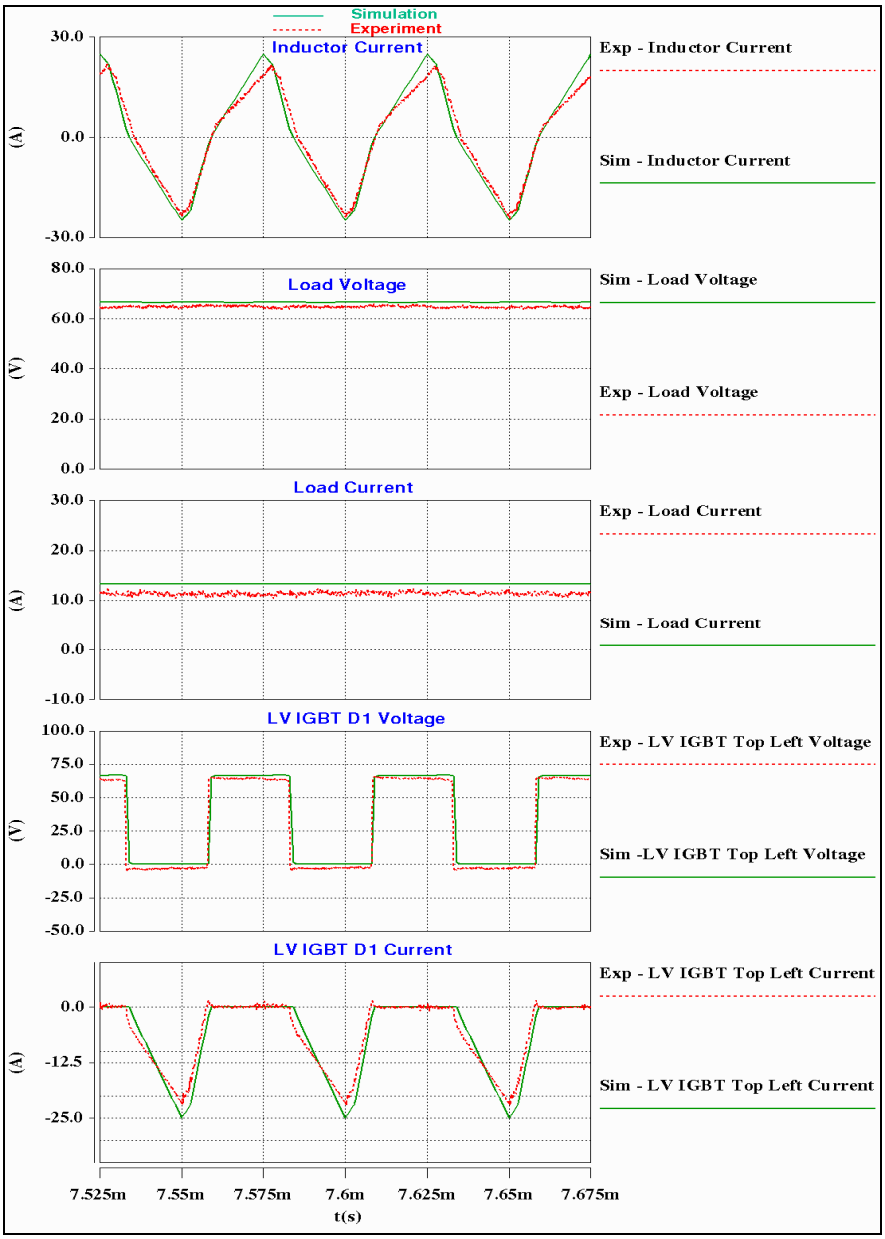


Figure 5.14 Experimental verification of LV side device, load voltage and current waveforms of the DAB converter for quasi-square-wave applied on transformer primary
V_{in} = 160V, L = 61.2μH, f_S = 20kHz, P_{in} = 1kW, R = 5Ω, V_0 = 65.45V, δ = 0.1, d = 0.3

Overall, a close agreement between measured and simulation results can be seen. However, there is a slight difference between the measured and simulated results, which is due to the driving signals generated by the dual channel driver of the DAB converter. The driver is designed to work in half bridge mode, where the driving signal for both transistors in each leg is generated based on the single PWM signal input to the driver from the DSP. Since the driver

provides a dead-time between top and bottom driving signals for the transistors, these are not therefore in perfect alignment with the simulation. This is evident in all the experimental waveforms presented in this Chapter. The experimental results confirmed that the converter operates at 91.8% efficiency for a quasi-square-wave voltage applied on the transformer primary. A 17% reduction in switching losses of the HV bridge devices was achieved, and a 9.7% increase in the average output current was obtained, thereby verifying the converter operation and confirming the analysis given earlier in this Chapter. The improvement in average output current results from the introduction of a dead-time on the primary voltage waveform, which increases the magnitude of the average output current. In order to compare the performance of the converter when operating in square-wave mode, experimental results were taken under a similar operating condition (for d = 0.3), for the square-wave mode with the same experimental setup. Figures 5.15 to 5.17 show the experimental results for square-wave operation. Figure 5.15 depicts the AC link voltage waveforms generated by the two active bridges and the transformer primary and secondary current waveforms.

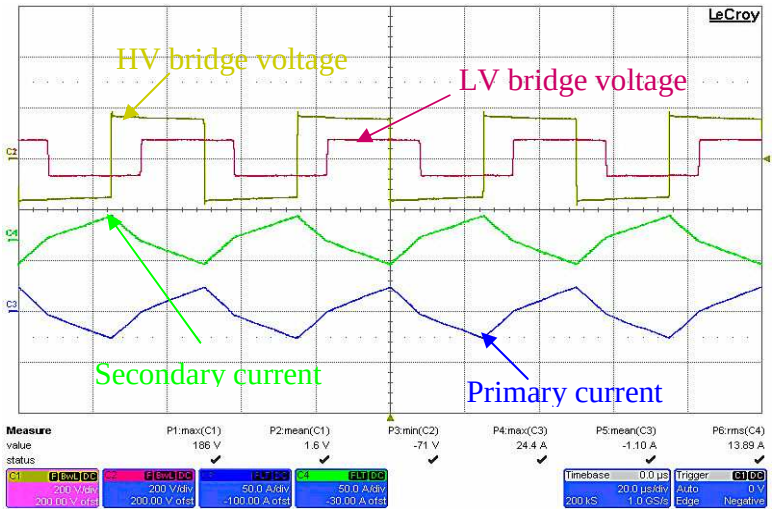


Figure 5.15 Experimental results of AC link waveforms of square-wave mode of DAB converter
V_{in} = 160V, L = 61.2μH, f_S = 20kHz, P_{in} = 1kW, R = 5Ω, V_0 = 65.32V, d = 0.3

The HV and the LV side device voltage and current waveforms are displayed in Figure 5.16. Load voltage and load current waveforms and the inductor current waveform are shown in Figure 5.17. From the measured results, it was found that the converter operates with an efficiency of 83.5% in the square-wave mode of operation. Experiments were performed

without snubber capacitors since the snubber demands more energy to be stored in the coupling inductance to achieve ZVS for this operating condition. Hence, without snubbers, for the same operating condition (d = 0.3) and δ = 0.1, a quasi-square-wave voltage on the primary results in a 10% improvement in efficiency and a 16.8% increase in ZVS operating range over the square-wave operating mode. These results once again confirm the theoretical analysis presented in section 5.2.2.

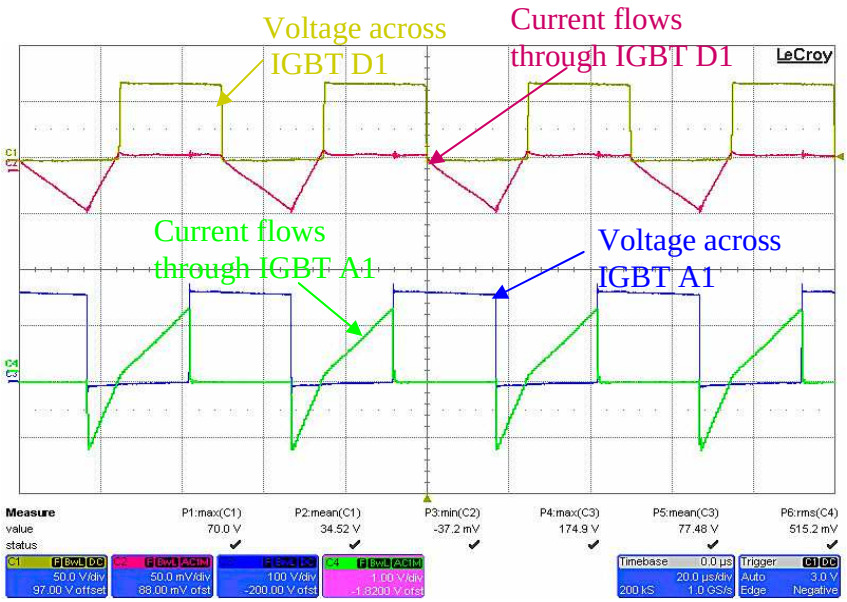


Figure 5.16 Experimental results of device waveforms of square-wave mode of the DAB converter
V_{in} = 160V, L = 61.2μH, f_S = 20kHz, P_{in} = 1kW, R = 5Ω, V_0 = 65.32V, d = 0.3

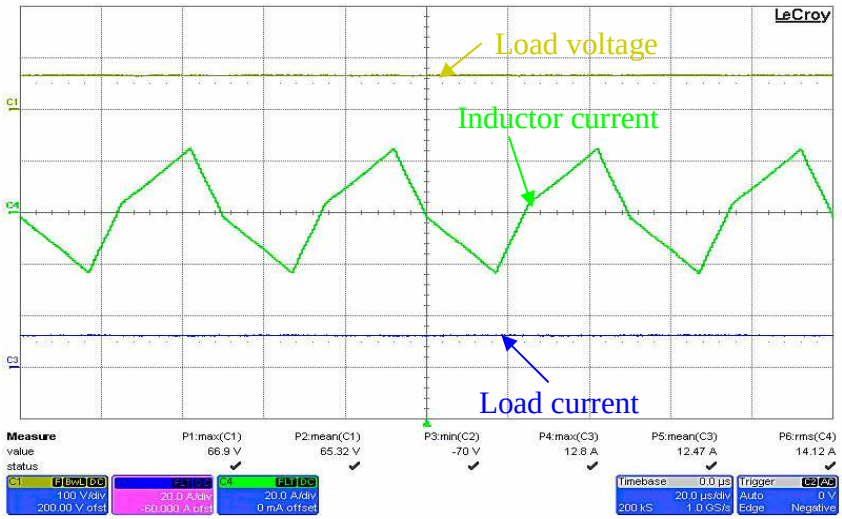


Figure 5.17 Experimental results of inductor current, load current and load voltage waveforms of square-wave mode of the DAB converter
V_{in} = 160V, L = 61.2μH, f_S = 20kHz, P_{in} = 1kW, R = 5Ω, V_0 = 65.32V, d = 0.3

5.3 Quasi-square-wave applied on transformer secondary

In this section, the effect of introducing dead-time on the transformer secondary voltage is analysed in detail. To obtain a quasi-square-wave voltage on the transformer secondary, the diagonal transistors are shifted in phase on the secondary H-bridge and a square-wave voltage waveform is maintained on the transformer primary.

5.3.1 Basic operation

A quasi-square-wave voltage on the transformer secondary allows only one device to turn-off at a time in the secondary H-bridge. This can be clearly seen from the ideal waveforms shown in Figures 5.18 and 5.19 for the charging and discharging modes respectively. Therefore, only the basic operation during the freewheeling interval is described here. During the charging mode at t_1, transistor C_2 turns off and current is transferred from transistor C_2 to the diode C_{D1} under ZVS. The current now freewheels between the diode C_{D1} and the transistor D_1 during the interval t_1-t_2. At t_2, transistor D_1 turns off and current transfers from transistor D_1 to diode D_{D2} under ZVS. The current now flows through the diodes D_{D2} and C_{D1} during the interval t_2-t_3. A similar freewheeling operation is repeated during the second half cycle of the charging mode with the corresponding opposite set of bridge transistors and diodes. Since a square-wave voltage is maintained on the transformer primary, the operation described in Chapter 2 for the primary H-bridge holds good for the charging and discharging modes. The orange coloured region of the ideal waveforms shown in Figures 5.18 and 5.19 represents the freewheeling intervals. Gate signals of transistors S_{A1}, S_{B2} on the primary side and gate signals of leading (S_{C1}) and lagging (S_{D2}) transistors on the secondary side, voltages generated by the two full bridges, V_P on the primary side bridge (which is the primary referred voltage) and V_S on the secondary side bridge, the current flowing through the coupling inductance i_L, the voltage across the coupling inductance V_L, the device currents $i_{AD1\text{-}A1}$ on the primary side, $i_{CD1\text{-}C1}$ and $i_{DD2\text{-}D2}$ on the secondary side and the LV side terminal current i_0 are depicted in Figures 5.18 and 5.19. V_{in} is the HV bus voltage, V_0 is the ultracapacitor voltage and n is the transformer turns ratio. Tables 5.9 and 5.10 summarise the switching conditions of various devices during the charging and discharging modes. The introduction of dead-time on the secondary can be used to control the power flow in addition to the phase shift introduced between the two H-bridges. Until now in the existing literature, an analysis of the DAB

Table 5.9 Summary of switching conditions of devices during charging mode for quasi-square-wave applied on transformer secondary

Half cycle	Time instant	Conducting devices		ZVS Turn ON	ZVS Turn OFF
		Input bridge	Output bridge		
First	t_0-t_1	A_1,B_2	C_2,D_1	A_1,B_2,C_2,D_1	
	t_1-t_2	A_1,B_2	C_{D1},D_1		C_2
	t_2-t_3	A_1,B_2	C_{D1},D_{D2}		D_1
	t_3-t_4	A_{D2},B_{D1}	C_{D1},D_{D2}		A_1,B_2
Second	t_4-t_5	A_2,B_1	C_1,D_2	A_2,B_1,C_1,D_2	
	t_5-t_6	A_2,B_1	C_{D2},D_2		C_1
	t_6-t_7	A_2,B_1	C_{D2},D_{D1}		D_2
	t_7-t_8	A_{D1},B_{D2}	C_{D2},D_{D1}		A_2,B_1

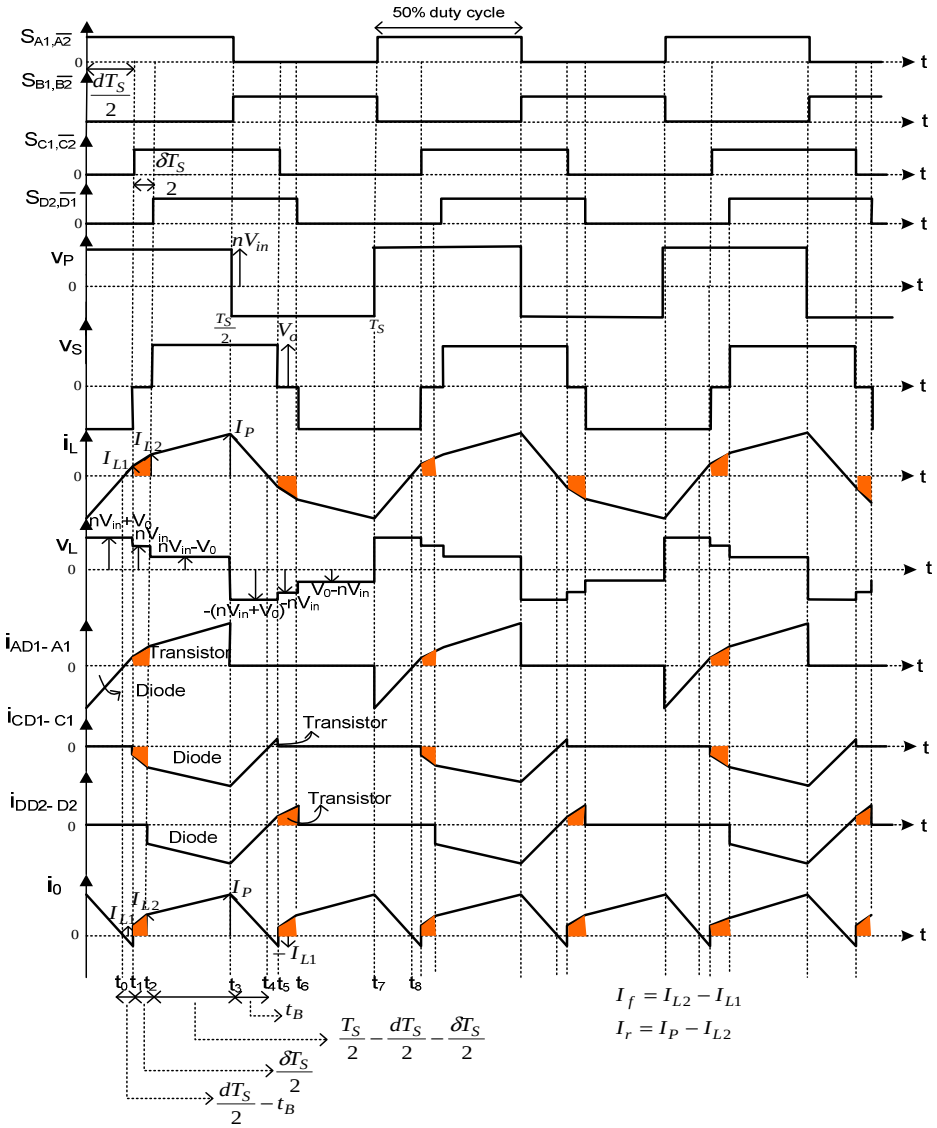


Figure 5.18 Ideal waveforms of DAB converter for quasi-square-wave applied on transformer secondary during charging mode

Table 5.10 Summary of switching conditions of devices during discharging mode for quasi-square-wave applied on transformer secondary

Half cycle	Time instant	Conducting devices		ZVS Turn ON	ZVS Turn OFF
		Input bridge	Output bridge		
First	t_0-t_1	A_2,B_1	C_1,D_2	A_2,B_1,C_1,D_2	
	t_1-t_2	A_{D1},B_{D2}	C_1,D_2		A_2,B_1
	t_2-t_3	A_{D1},B_{D2}	C_{D2},D_2		C_1
	t_3-t_4	A_{D1},B_{D2}	C_{D2},D_{D1}		D_2
Second	t_4-t_5	A_1,B_2	C_2,D_1	A_1,B_2,C_2,D_1	
	t_5-t_6	A_{D2},B_{D1}	C_2,D_1		A_1,B_2
	t_6-t_7	A_{D2},B_{D1}	C_{D1},D_1		C_2
	t_7-t_8	A_{D2},B_{D1}	C_{D1},D_{D2}		D_1

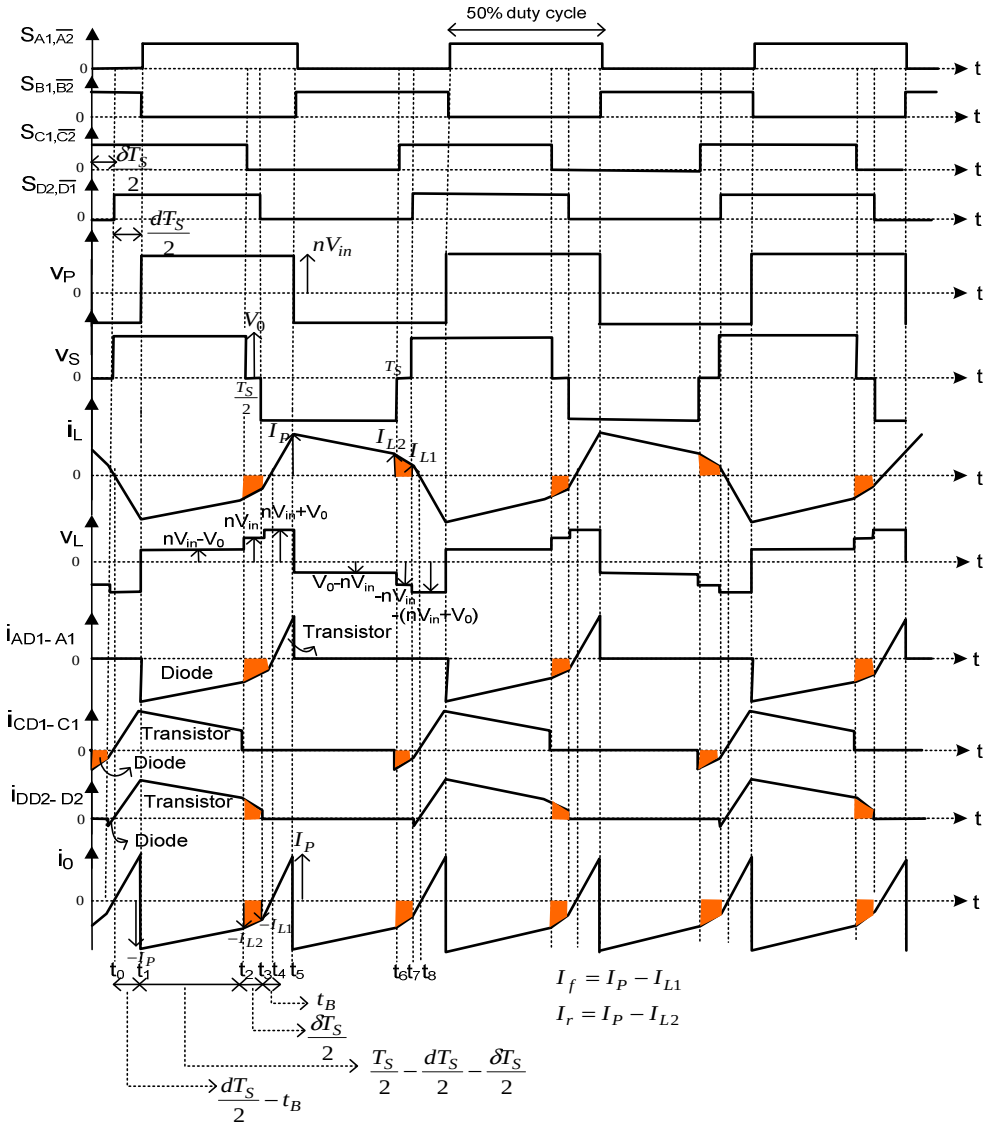
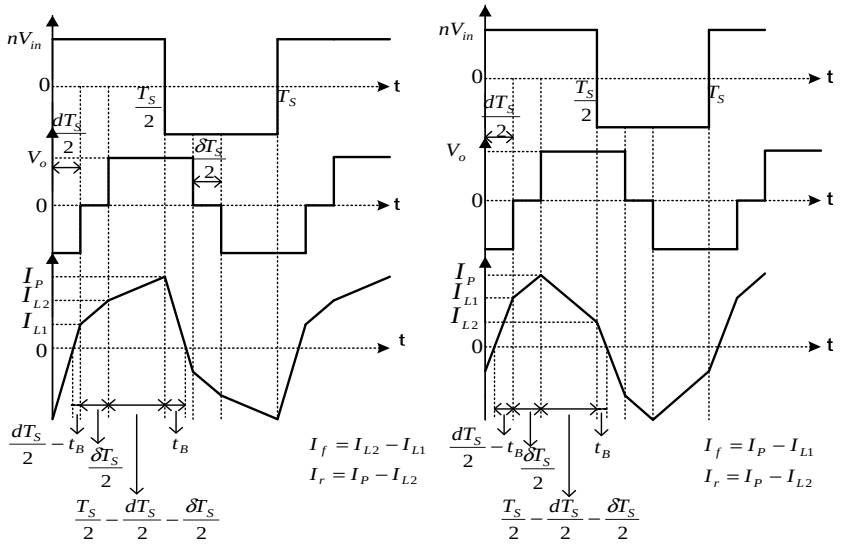


Figure 5.19 Ideal waveforms of DAB converter for quasi-square-wave applied on transformer secondary during discharging mode

converter performance for quasi-square-wave mode of operation has not been published in terms of the average, RMS and peak currents, average power transfer and ZVS operating range. The performance evaluation of the DAB converter is done through a detailed analysis of the quasi-square-wave mode of operation, as presented in the following sections.

5.3.2 Mathematical model for buck and boost modes

The analysis was performed by adopting a similar methodology as described in the previous section to derive the equations for the key parameters. Figures 5.20 (a) and (b) show the simplified operational waveforms of the converter, with a quasi-square-wave voltage on the transformer secondary winding, for buck and boost modes of operation. Various intervals of the inductor current waveform are marked for a periodic half cycle. The difference between the A.C link voltages is impressed across the coupling inductor. The quasi-square-wave voltage on the transformer secondary provides three-levels of voltage on the secondary and significantly influences the inductor current waveforms during both modes. The inductor current levels at various switching instants are marked in Figure 5.20. Mathematical models were derived based on the assumption of loss-less components and a piece-wise linear waveform for i_L, and are given in Tables 5.11 and 5.12 respectively. The detailed step-by step analysis for a quasi-square-wave voltage on the transformer secondary is presented in Appendices B and C.



(a) Buck mode (b) Boost mode

Figure 5.20. Simplified operational waveforms of quasi-square-wave voltage on transformer secondary

Table 5.11 Key equations of quasi-square-wave on transformer secondary - buck mode

Key Equations
$I_{L1}=\frac{T_S}{4L}\left[nV_{in}(2d-1)+V_O(1-\delta)\right]$
$I_P=\frac{T_S}{4L}\left[nV_{in}+V_O(2d+\delta-1)\right]$
$I_{L2}=\frac{T_S}{4L}\left[nV_{in}(2d+2\delta-1)+V_O(1-\delta)\right]$
$t_B=\frac{T_S\left[nV_{in}+V_O(2d+\delta-1)\right]}{4(nV_{in}+V_O)}$
$I_O=\frac{nV_{in}T_S}{2L}\left(d-d^2-d\delta+\frac{\delta}{2}-\frac{\delta^2}{2}\right)$
$I_{RMS}=\sqrt{\frac{2}{T_S}\left[\frac{I_{L1}^2}{3}\left(\frac{dT_S}{2}-t_B\right)+\left(\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}\right)\left(I_{L2}^2+\frac{I_r^2}{3}+I_{L2}I_r\right)+\left(\frac{\delta T_S}{2}\right)\left(I_{L1}^2+\frac{I_f^2}{3}+I_{L1}I_f\right)+\frac{I_P^2t_B}{3}\right]}$
$I_{L1}=\frac{T_S}{4L}\left[nV_{in}(2d-1)+V_O(1-\delta)\right]\geq 0$, condition for ZVS
$d \geq 0.5-\frac{V_O'}{2}(1-\delta)$, duty ratio at which ZVS occurs

Table 5.12 Key equations of quasi-square-wave on transformer secondary - boost mode

Key Equations
$I_{L1}=\frac{T_S}{4L}\left[nV_{in}(2d-1)+V_O(1-\delta)\right]$
$I_P=\frac{T_S}{4L}\left[nV_{in}(2d+2\delta-1)+V_O(1-\delta)\right]$
$I_{L2}=\frac{T_S}{4L}\left[nV_{in}+V_O(2d+\delta-1)\right]$
$t_B=\frac{T_S\left[nV_{in}+V_O(2d+\delta-1)\right]}{4(nV_{in}+V_O)}$
$I_O=\frac{nV_{in}T_S}{2L}\left(d-d^2-d\delta+\frac{\delta}{2}-\frac{\delta^2}{2}\right)$
$I_{RMS}=\sqrt{\frac{2}{T_S}\left[\frac{I_{L1}^2}{3}\left(\frac{dT_S}{2}-t_B\right)+\left(\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}\right)\left(I_P^2+\frac{I_r^2}{3}-I_PI_r\right)+\left(\frac{\delta T_S}{2}\right)\left(I_{L1}^2+\frac{I_f^2}{3}+I_{L1}I_f\right)+\frac{I_{L2}^2t_B}{3}\right]}$
$I_{L2}=\frac{T_S}{4L}\left[nV_{in}+V_O(2d+\delta-1)\right]\geq 0$, condition for ZVS
$d \geq 0.5-\frac{\delta}{2}-\frac{0.5}{V_O'}$, duty ratio at which ZVS occurs

Based on the procedure outlined in section 5.2.2, the average and RMS current equations of the DAB converter were derived and are listed in Tables 5.13 to 5.16 for buck and boost modes. The detailed derivations are presented in Appendices B and C.

Table 5.13 Average current equations of various devices of the DAB converter under buck mode - Quasi-square-wave applied on transformer secondary

Device	Average current equation
HV side Transistor	$\frac{\frac{1}{2}\times I_{L1}\times\left(\frac{dT_S}{2}-t_B\right)+\frac{1}{2}\times(I_{L1}+I_{L2})\times\frac{\delta T_S}{2}+\frac{1}{2}\times(I_{L2}+I_P)\times\left(\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}\right)}{\left(\frac{T_S}{2}-t_B\right)}$
HV side Diode	$\frac{\frac{1}{2}\times I_P\times t_B}{t_B}$
LV side leading Transistor	$\frac{\frac{1}{2}\times I_{L1}\times\left(\frac{dT_S}{2}-t_B\right)}{\left(\frac{dT_S}{2}-t_B\right)}$
LV side leading Diode	$\frac{\frac{1}{2}\times(I_{L1}+I_{L2})\times\frac{\delta T_S}{2}+\frac{1}{2}\times(I_{L2}+I_P)\times\left(\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}\right)+\frac{1}{2}\times I_P\times t_B}{\left(\frac{T_S}{2}-\frac{dT_S}{2}+t_B\right)}$
LV side lagging Transistor	$\frac{\frac{1}{2}\times(I_{L1}+I_{L2})\times\frac{\delta T_S}{2}+\frac{1}{2}\times I_{L1}\times\left(\frac{dT_S}{2}-t_B\right)}{\left(\frac{dT_S}{2}+\frac{\delta T_S}{2}-t_B\right)}$
LV side lagging Diode	$\frac{\frac{1}{2}\times(I_{L2}+I_P)\times\left(\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}\right)+\frac{1}{2}\times I_P\times t_B}{\left(\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}+t_B\right)}$

Table 5.14 RMS current equations of various devices of the DAB converter under buck mode - Quasi-square-wave applied on transformer secondary

Device	RMS current equation
HV side Transistor	$\sqrt{\frac{1}{T_S}\left[\frac{I_{L1}^2\times\left(\frac{dT_S}{2}-t_B\right)}{3}+\left(I_{L1}^2+\frac{I_f^2}{3}+I_{L1}I_f\right)\times\frac{\delta T_S}{2}+\left(\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}\right)\times\left(I_{L2}^2+\frac{I_r^2}{3}+I_{L2}I_r\right)\right]}$
HV side Diode	$\sqrt{\frac{1}{T_S}\left[\frac{I_P^2\times(t_B)}{3}\right]}$
LV side leading Transistor	$\sqrt{\frac{1}{T_S}\left[\frac{I_{L1}^2\times\left(\frac{dT_S}{2}-t_B\right)}{3}\right]}$
LV side leading Diode	$\sqrt{\frac{1}{T_S}\left[\left(\frac{\delta T_S}{2}\right)\times\left(I_{L1}^2+\frac{I_f^2}{3}+I_{L1}I_f\right)+\left(\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}\right)\times\left(I_{L2}^2+\frac{I_r^2}{3}+I_{L2}I_r\right)+\frac{I_P^2\times(t_B)}{3}\right]}$
LV side lagging Transistor	$\sqrt{\frac{1}{T_S}\left[\frac{I_{L1}^2\times\left(\frac{dT_S}{2}-t_B\right)}{3}+\left(\frac{\delta T_S}{2}\right)\times\left(I_{L1}^2+\frac{I_f^2}{3}+I_{L1}I_f\right)\right]}$
LV side lagging Diode	$\sqrt{\frac{1}{T_S}\left[\left(\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}\right)\times\left(I_{L2}^2+\frac{I_r^2}{3}+I_{L2}I_r\right)+\frac{I_P^2\times t_B}{3}\right]}$

Table 5.15 Average current equations of various devices of the DAB converter under boost mode - Quasi-square-wave applied on transformer secondary

Device	Average current equation
LV side Transistor	$\frac{\frac{1}{2}\times I_{L1}\times\left(\frac{dT_S}{2}-t_B\right)+\frac{1}{2}\times(I_{L1}+I_P)\times\frac{\delta T_S}{2}+\frac{1}{2}\times(I_P+I_{L2})\times\left(\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}\right)}{\left(\frac{T_S}{2}-t_B\right)}$
LV side Diode	$\frac{\frac{1}{2}\times I_{L2}\times t_B}{t_B}$
HV side leading Transistor	$\frac{\frac{1}{2}\times I_{L1}\times\left(\frac{dT_S}{2}-t_B\right)}{\left(\frac{dT_S}{2}-t_B\right)}$
HV side leading Diode	$\frac{\frac{1}{2}\times(I_{L1}+I_P)\times\frac{\delta T_S}{2}+\frac{1}{2}\times(I_P+I_{L2})\times\left(\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}\right)+\frac{1}{2}\times I_{L2}\times t_B}{\left(\frac{T_S}{2}-\frac{dT_S}{2}+t_B\right)}$
HV side lagging Transistor	$\frac{\frac{1}{2}\times I_{L1}\times\left(\frac{dT_S}{2}-t_B\right)+\frac{1}{2}\times(I_{L1}+I_P)\times\frac{\delta T_S}{2}}{\left(\frac{dT_S}{2}+\frac{\delta T_S}{2}-t_B\right)}$
HV side lagging Diode	$\frac{\frac{1}{2}\times(I_P+I_{L2})\times\left(\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}\right)+\frac{1}{2}\times I_{L2}\times t_B}{\left(\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}+t_B\right)}$

Table 5.16 RMS current equations of various devices of the DAB converter under boost mode - Quasi-square-wave applied on transformer secondary

Device	RMS current equation
LV side Transistor	$\sqrt{\frac{1}{T_S}\left[\frac{I_{L1}^2\times\left(\frac{dT_S}{2}-t_B\right)}{3}+\left(I_{L1}^2+\frac{I_f^2}{3}+I_{L1}I_f\right)\times\frac{\delta T_S}{2}+\left(\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}\right)\times\left(I_P^2+\frac{I_r^2}{3}-I_PI_r\right)\right]}$
LV side Diode	$\sqrt{\frac{1}{T_S}\left[\frac{I_{L2}^2\times(t_B)}{3}\right]}$
HV side leading Transistor	$\sqrt{\frac{1}{T_S}\left[\frac{I_{L1}^2\times\left(\frac{dT_S}{2}-t_B\right)}{3}\right]}$
HV side leading Diode	$\sqrt{\frac{1}{T_S}\left[\left(\frac{\delta T_S}{2}\right)\times\left(I_{L1}^2+\frac{I_f^2}{3}+I_{L1}I_f\right)+\left(\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}\right)\times\left(I_P^2+\frac{I_r^2}{3}-I_PI_r\right)+\frac{I_{L2}^2\times(t_B)}{3}\right]}$
HV side lagging Transistor	$\sqrt{\frac{1}{T_S}\left[\frac{I_{L1}^2\times\left(\frac{dT_S}{2}-t_B\right)}{3}+\left(\frac{\delta T_S}{2}\right)\times\left(I_{L1}^2+\frac{I_f^2}{3}+I_{L1}I_f\right)\right]}$
HV side lagging Diode	$\sqrt{\frac{1}{T_S}\left[\left(\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}\right)\times\left(I_P^2+\frac{I_r^2}{3}-I_PI_r\right)+\frac{I_{L2}^2\times t_B}{3}\right]}$

5.3.3 Performance evaluation

From the mathematical models, the performance of the DAB converter was evaluated by considering the effect of introducing dead-time on transformer secondary voltage with respect to ZVS operating range, average power transfer, converter efficiency, and the RMS and peak inductor/transformer currents. The following sections discuss the DAB converter performance.

5.3.3.1 ZVS operating range

The DAB converter features an enhanced ZVS range over a wide operating voltage during boost mode, as depicted in Figure 5.21. From the figure, it can be observed that for a given voltage conversion ratio, the duty ratio at which ZVS begins becomes lower for higher values of dead-time over a wide operating voltage range. The percentage improvement in ZVS range is highlighted in Figure 5.22. It can be observed from the analysis that introduction of dead-time in the transformer secondary voltage waveform does not contribute to an increase in the ZVS boundary during the buck mode of operation. This is because with the inclusion of dead-time, the current peak (I_{L1}) occurs early by a time period of $\frac{\delta T_S}{2}$, as shown in Figure 5.20(a). Therefore the turn-off of transistors in the LV bridge occurs at $I_{L1,}$ which is now lower than the peak value of I_{L1} that corresponds to the ZVS boundary in the square-wave mode. As a result, this degrades the converter performance during buck mode, as can be seen from Figure 5.20(a). The ZVS boundary equations of the mathematical model are listed in Table 5.7.

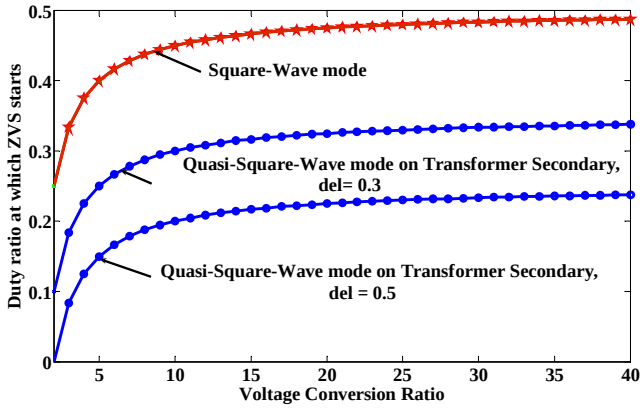


Figure 5.21 ZVS boundaries for a quasi-square-wave voltage on the transformer secondary winding versus voltage conversion ratio (del = δ)

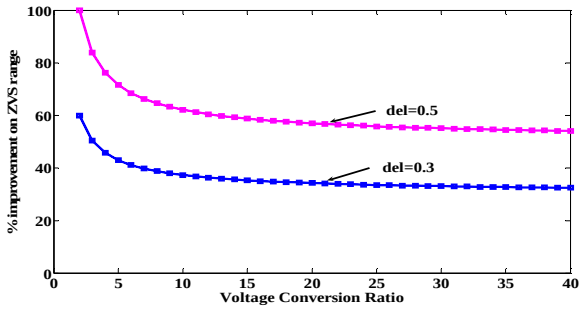


Figure 5.22 Percentage improvements of ZVS operating range for quasi-square-wave voltage on the transformer secondary versus voltage conversion ratio (del = δ)

5.3.3.2 Power transfer and converter efficiency

As stated in section 5.2, introduction of dead-time in the transformer secondary voltage shifts the maximum power transfer operating point towards the left (lower duty ratios) as portrayed in Figure 5.23. Similar to the previous mode, operating at duty ratios lower than that at the peak of a curve in Figure 5.23 is of interest, since the RMS and peak currents for a given phase shift are lower than on the right-hand-side of the curves. Similar to the earlier analysis, average power increases for lower values of dead-time and duty ratio. This is because at lower values of dead-time, the negative area in the output current waveform decreases and the positive area increases due to the freewheeling interval, thereby average output current is increased. Since the average output current equation for a given 'δ' is the same whether the dead-time is introduced on the primary or on the secondary of the isolation transformer, the average power transfer curves shown in Figure 5.7 are valid for this mode of operation as well. This once again proves that the converter power transfer is enhanced at low power/light load operating conditions.

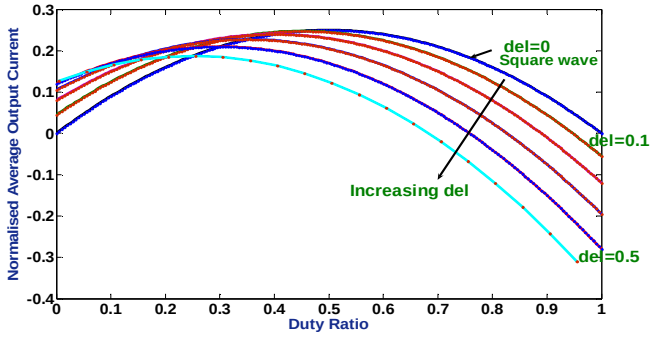


Figure 5.23 Normalised average output current as a function of duty ratio for different values of dead-time introduced into the transformer secondary voltage – Quasi-square-wave voltage on transformer secondary (del = δ)

5.3.3.3 RMS and peak inductor/transformer currents

To estimate the performance of the DAB converter under this mode of operation, the RMS and peak values of coupling inductor current were calculated and compared with those for the square-wave mode at the maximum power transfer operating point (d = 0.5) over a range of ultracapacitor voltages. Increased values of RMS and peak AC link currents for the quasi-square-wave mode can be observed from Figures 5.24 and 5.25 respectively, and these result in increased conduction losses and device stresses. However, increased link currents allow a wide ZVS range and enhanced average power transfer at light-loads and reduced dead-time. Hence, there is a trade-off between conduction and switching losses.

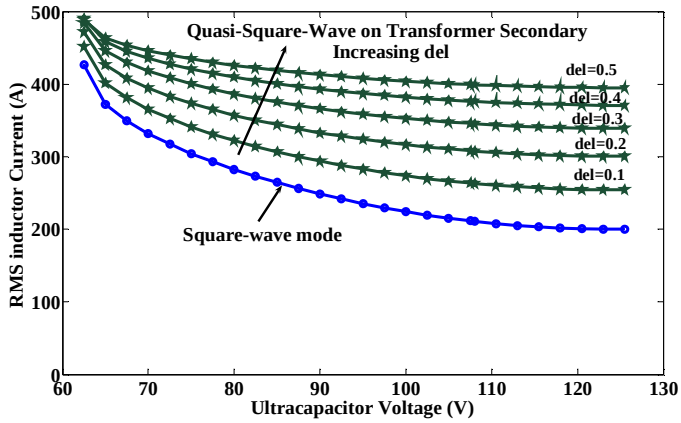


Figure 5.24 RMS value of inductor current for square-wave and quasi-square-wave voltages at maximum power transfer (del = δ)

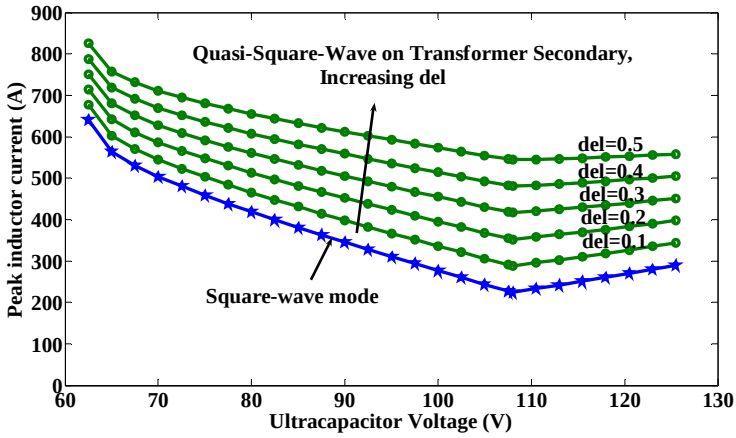


Figure 5.25 Peak value of inductor current for square-wave and quasi-square-wave voltages during maximum power transfer (del = δ)

5.3.4 Simulation and Experimental results

This section presents simulation results and gives an experimental verification of the DAB converter with a quasi-square-wave voltage on the transformer secondary. The results confirm the mathematical models presented in section 5.3.2. Figure 5.26 shows the SABER simulation waveforms for the buck mode of operation. Voltages generated by the active bridges, inductor current, leading/lagging device currents on the quasi-square-wave LV side, device current on the HV side and the load current and voltage are displayed. From the theoretical analysis, the steady state values are I_{L1} = 0.4A, I_{L2} = 6.98A, peak inductor current I_P = 28.17A, average output current I_0 = 14.7A and inductor RMS current I_{RMS} = 16.95A. These values agree well with the SABER results shown below. The freewheeling current interval due to the quasi-square-wave mode of operation on the LV side can be clearly seen from the lagging leg device current (I_{D1}/I_{DD1}) waveforms portrayed in Figure 5.26.

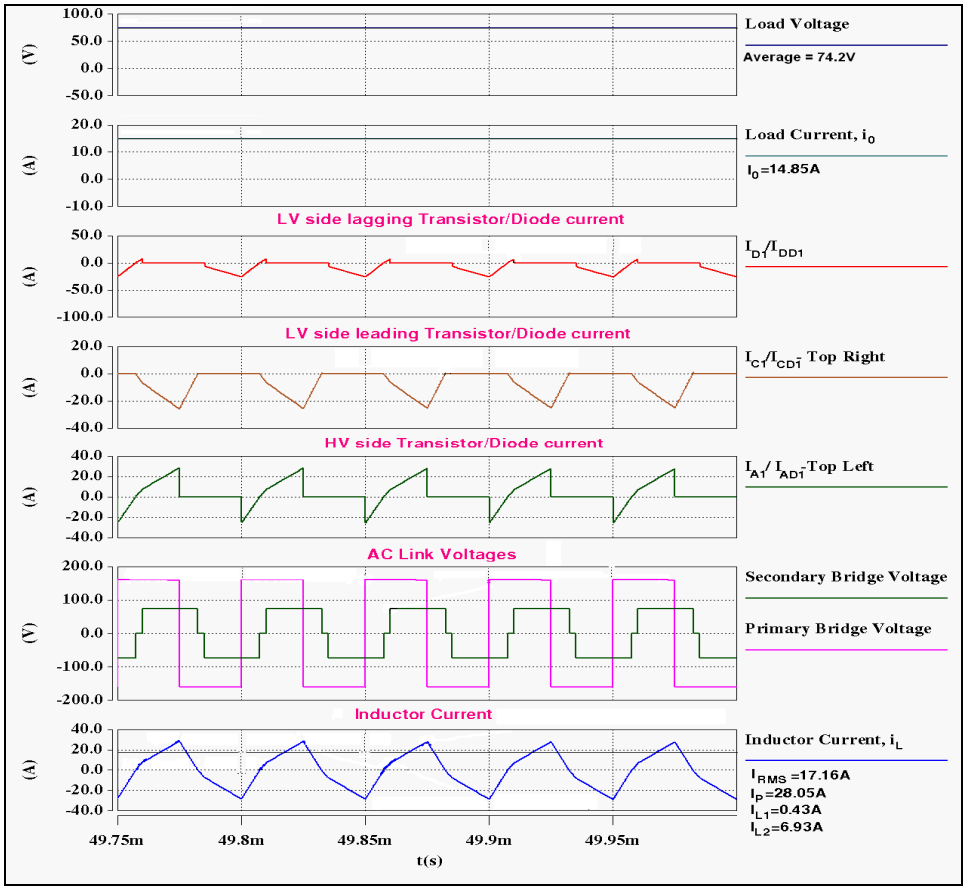


Figure 5.26 Simulation waveforms for quasi-square-wave applied on transformer secondary
V_{in} = 160V, L = 61.2μH, f_S = 20kHz, P_{in} = 1kW, R = 5Ω, V_0 = 74.26V, δ = 0.1, d = 0.3

The experimental results were taken for d = 0.3, with δ = 0.1. Control signals were derived from the DSP. Figure 5.27 illustrates the AC link voltage and current waveforms of the DAB converter with a quasi-square-wave voltage applied to the transformer secondary. A close agreement is observable between the simulation waveforms and the experimental waveforms. However, the measured experimental values are slightly lower than the simulation values and this is attributable to circuit losses, which were not included in the simulation.

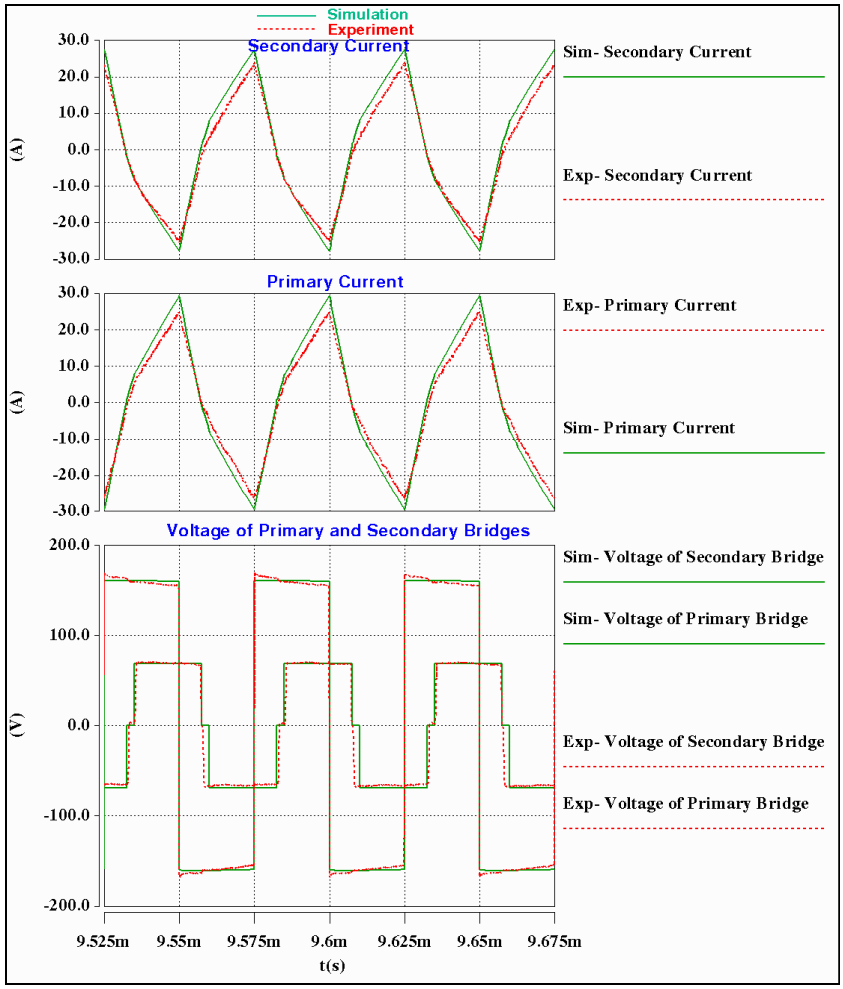


Figure 5.27 Experimental verification of AC link waveforms of the DAB converter for a quasi-square-wave voltage applied on transformer secondary
V_{in} = 160V, L = 61.2μH, f_S = 20kHz, P_{in} = 1kW, R = 5Ω, V_0 = 66.64V, δ = 0.1, d = 0.3

Figure 5.28 shows a HV side device (B_1) current and voltage waveforms and load voltage and load current waveforms. The load voltage waveform shown in Figure 5.28 confirms that there

is virtually no output voltage ripple. Since the devices on the HV side operate in the square-wave mode, there is no variation in the duty ratio of the device voltage waveforms.

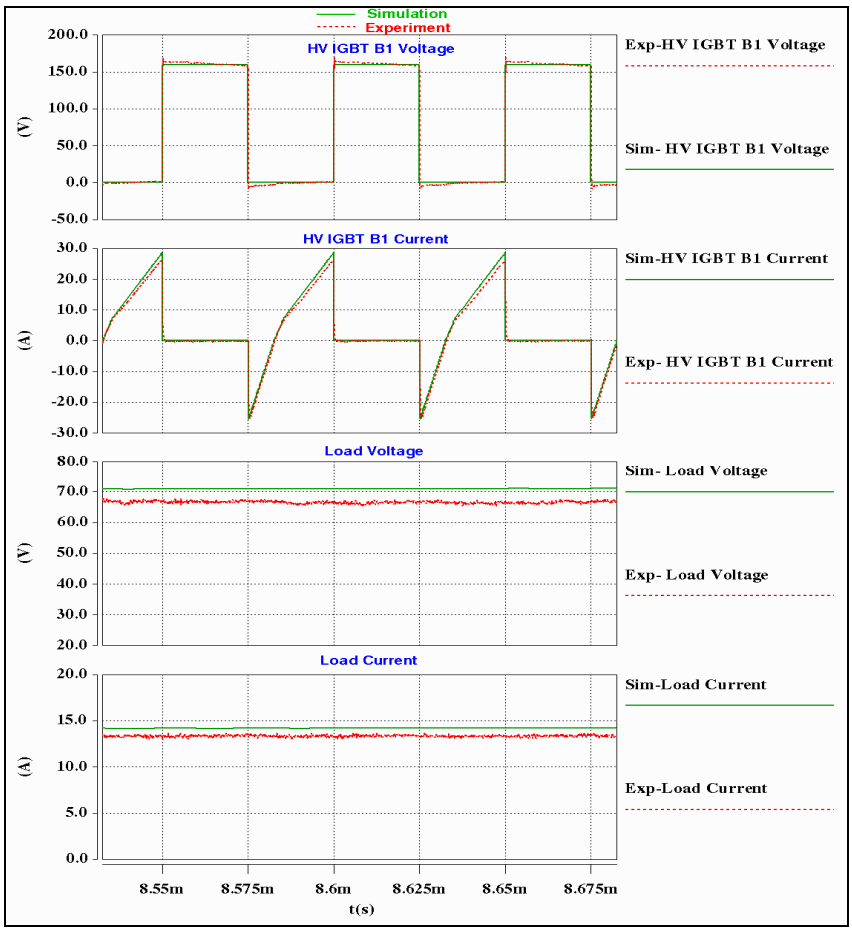


Figure 5.28 Experimental verification of HV device and load waveforms of the DAB converter for quasi-square-wave applied on transformer secondary
V_{in} = 160V, L = 61.2μH, f_S = 20kHz, P_{in} = 1kW, R = 5Ω, V_0 = 66.64V, δ = 0.1, d = 0.3

Figure 5.29 portrays LV side lagging and leading device voltage and current waveforms. From Figure 5.29, it can be observed that the experimental measurement of LV IGBT D_1 voltage waveform (shown in dotted red lines) goes slightly negative. This is due to auto-zero problems with the measurement probe (ADP305). There is a slight variation in the duty ratio of device voltage waveforms. This is due to a slight mismatch in the driver signal generation for phase-leg IGBT modules, component values, winding resistances, and delay in control signals. A little pulse of magnitude 5A is observed in the C_1 device current waveform; this shows that the devices in the LV side operate in ZVS boundary region. The experiment confirmed that the

converter was operating at 91% efficiency. A 6.8% improvement in the average output current was observed in comparison with square-wave mode, thereby verifying the converter operation and confirming the analysis. As predicted from the analysis, the ZVS operating region shrinks when a quasi-square-wave voltage is imposed on the transformer secondary under buck mode. For the operating conditions of Figure 5.29, as per the analysis, a 6.4% reduction in ZVS operation is estimated; however, experimental results show only a 1.4% reduction in ZVS operation. This may be due to the energy stored in external filters, which aids in charging/discharging of the device output capacitances. The switching losses on the LV side increased 2.4 times in comparison with the square-wave mode under similar conditions due to an increase in switching current from 1A to 6.5A. This resulted in a slight reduction in converter efficiency when compared with the case of a quasi-square-wave voltage on the transformer primary.

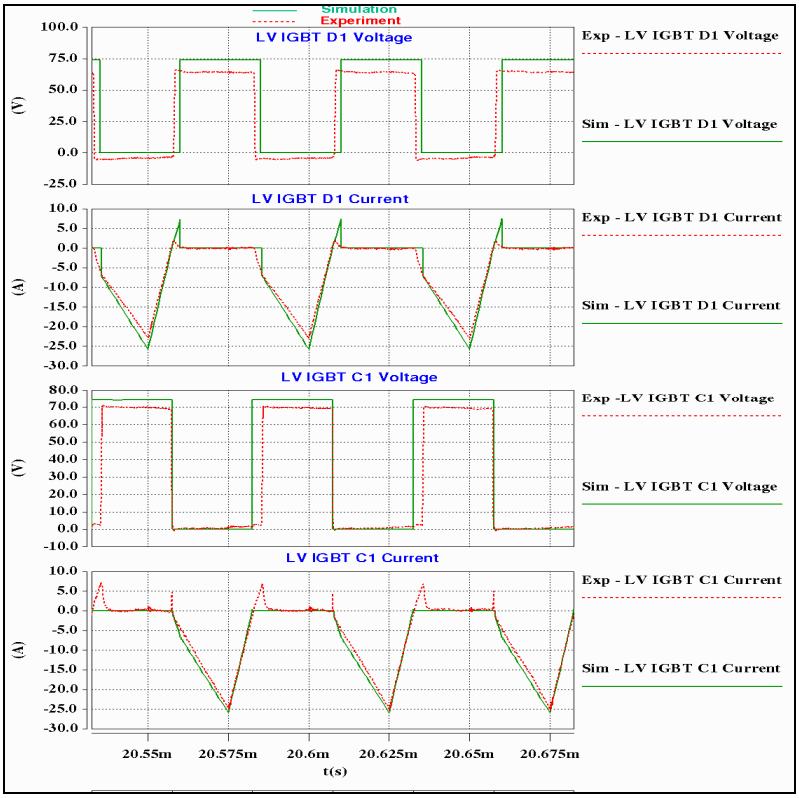


Figure 5.29 Experimental verification of LV side device waveforms of the DAB converter for quasi-square-wave applied on transformer secondary
V_{in} = 160V, L = 61.2μH, f_S = 20kHz, P_{in} = 1kW, R = 5Ω, V_0 = 66.64V, δ = 0.1, d = 0.3

5.4 Quasi-square-wave voltages applied on both transformer primary and secondary

This section describes the application of dead-time simultaneously to both primary and secondary voltages of the transformer, which is realised by phase shifting diagonal transistors on the primary and secondary H-bridges. The effects of these quasi-square-wave voltages on the DAB converter performance are analysed here.

5.4.1 Basic operation

In conventional phase shift modulation, at a fixed frequency f_s, it is not possible to directly influence the shape of the AC link current waveform since it is dependent on the DC voltages and phase shift introduced between the two bridges. When quasi-square-wave voltages are applied to both transformer primary and secondary, a dead-time is introduced on the HV side and the LV side of the transformer, in addition to the phase shift introduced between the two active bridges and this modifies the AC link current waveform. The mode may pave the way for enhancing the ZVS operating range of the DAB converter in buck and boost modes of operation. The dead-time can also be used to control the overall power transfer between the bridges. A detailed mathematical analysis and performance evaluation is presented in the following sections, to explain the benefits of the quasi-square-wave mode of operation. During this mode, only one device will turn off at any one time. This can be clearly seen from the ideal waveforms of the converter during charging and discharging modes, depicted in Figures 5.30 and 5.31. Gate signals of leading (S_{A1}) and lagging (S_{B2}) transistors on the primary side and gate signals of leading (S_{C1}) and lagging (S_{D2}) transistors on the secondary side are shown in Figures 5.30 and 5.31. Voltages generated by the two full bridges, V_P on the primary side bridge (which is the primary referred voltage) and V_S on the secondary side bridge, the current flowing through the coupling inductance i_L, voltage across the coupling inductance V_L are also shown. In addition, the device currents $i_{AD1\text{-}A1}$, $i_{BD2\text{-}B2}$ on the primary side, device currents $i_{CD1\text{-}C1}$ and $i_{DD2\text{-}D2}$ on the secondary side and the LV side terminal current i_0 are also portrayed in Figures 5.30 and 5.31. V_{in} is the HV bus voltage, V_0 is the ultracapacitor voltage and n is the transformer turns ratio. A summary of the various device switching conditions is given in Table 5.17 for the charging mode and Table 5.18 for the discharging mode. In order to

highlight the influence of quasi-square-wave operation on the AC link and device current waveforms, freewheeling intervals are coloured green in the ideal waveforms of Figures 5.30 and 5.31.

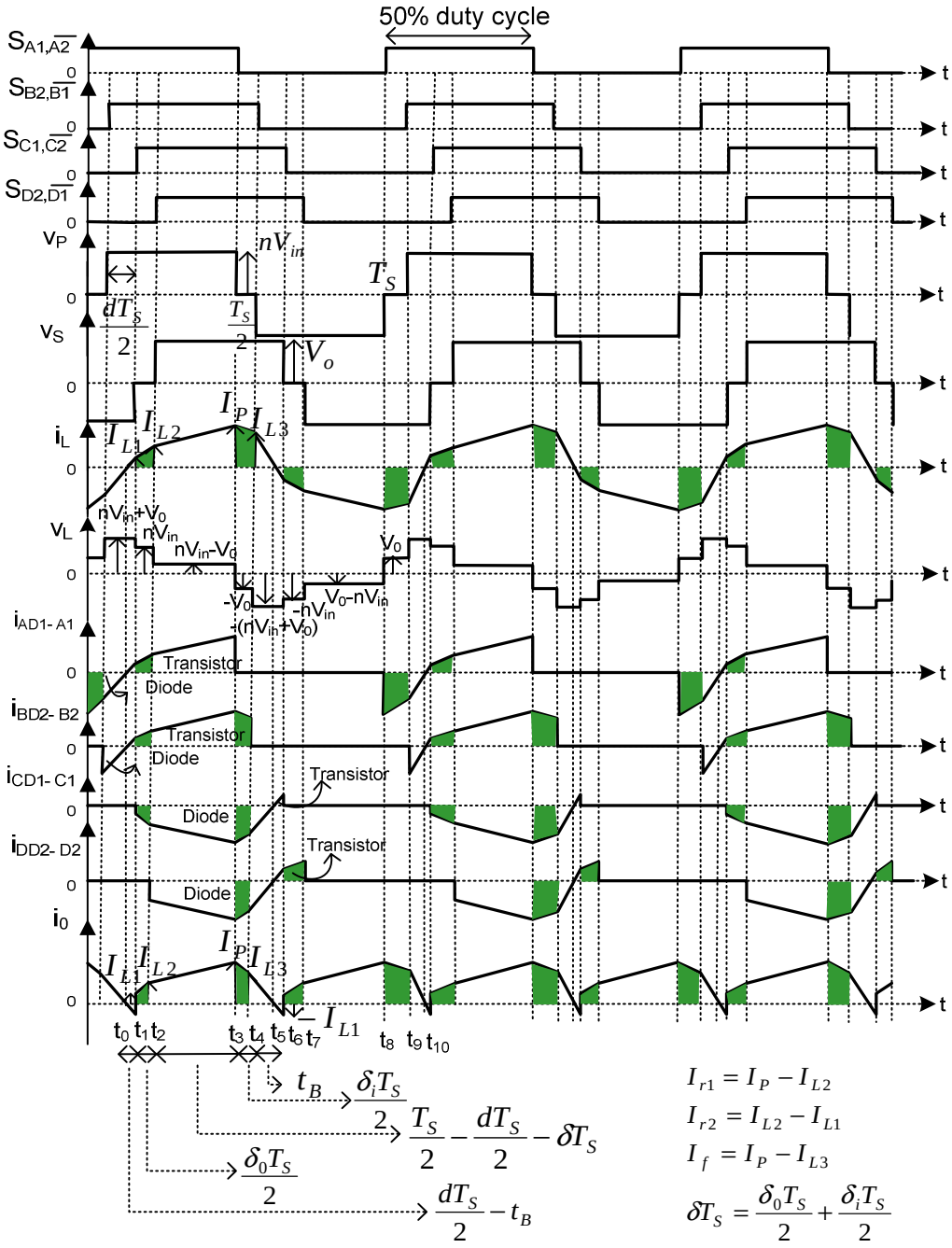


Figure 5.30 Ideal waveforms during charging mode for quasi-square-wave applied on transformer primary and secondary

The waveforms shown in Figure 5.30 and Figure 5.31 differ by the green region when compared to the waveforms shown in Figure 2.2 and Figure 2.3 respectively, due to the effect of dead-time introduced in the transformer primary and secondary voltages. The dead-time increases the average output current of the converter thereby improving the efficiency and the ZVS operation. The increased average current is due to the increased conduction intervals of the devices when compared with the square-wave mode. Hence, ZVS enhancement is achieved at the expense of increased conduction losses. Only one device turns off at any one switching instant, hence the devices have different ZVS boundary limits to achieve ZVS.

Table 5.17 Summary of switching conditions of devices during charging mode for quasi-square-wave applied on transformer primary and secondary

Half cycle	Time instant	Conducting devices		ZVS Turn ON	ZVS Turn OFF
		Input bridge	Output bridge		
First	t_0-t_1	A_1,B_2	C_2,D_1	A_1,B_2,C_2,D_1	
	t_1-t_2	A_1,B_2	C_{D1},D_1		C_2
	t_2-t_3	A_1,B_2	C_{D1},D_{D2}		D_1
	t_3-t_4	A_{D2},B_2	C_{D1},D_{D2}		A_1
	t_4-t_5	A_{D2},B_{D1}	C_{D1},D_{D2}		B_2
Second	t_5-t_6	A_2,B_1	C_1,D_2	A_2,B_1,C_1,D_2	
	t_6-t_7	A_2,B_1	C_{D2},D_2		C_1
	t_7-t_8	A_2,B_1	C_{D2},D_{D1}		D_2
	t_8-t_9	A_{D1},B_1	C_{D2},D_{D1}		A_2
	t_9-t_{10}	A_{D1},B_{D2}	C_{D2},D_{D1}		B_1

Table 5.18 Summary of switching conditions of devices during discharging mode for quasi-square-wave applied on transformer primary and secondary

Half cycle	Time instant	Conducting devices		ZVS Turn ON	ZVS Turn OFF
		Input bridge	Output bridge		
First	t_0-t_1	A_2,B_1	C_1,D_2	A_1,B_2,C_2,D_1	
	t_1-t_2	A_{D1},B_1	C_1,D_2		A_2
	t_2-t_3	A_{D1},B_{D2}	C_1,D_2		B_1
	t_3-t_4	A_{D1},B_{D2}	C_{D2},D_2		C_1
	t_4-t_5	A_{D1},B_{D2}	C_{D2},D_{D1}		D_2
Second	t_5-t_6	A_1,B_2	C_2,D_1	A_2,B_1,C_1,D_2	
	t_6-t_7	A_{D2},B_2	C_2,D_1		A_1
	t_7-t_8	A_{D2},B_{D1}	C_2,D_1		B_2
	t_8-t_9	A_{D2},B_{D1}	C_{D1},D_1		C_2
	t_9-t_{10}	A_{D2},B_{D1}	C_{D1},D_{D2}		D_1

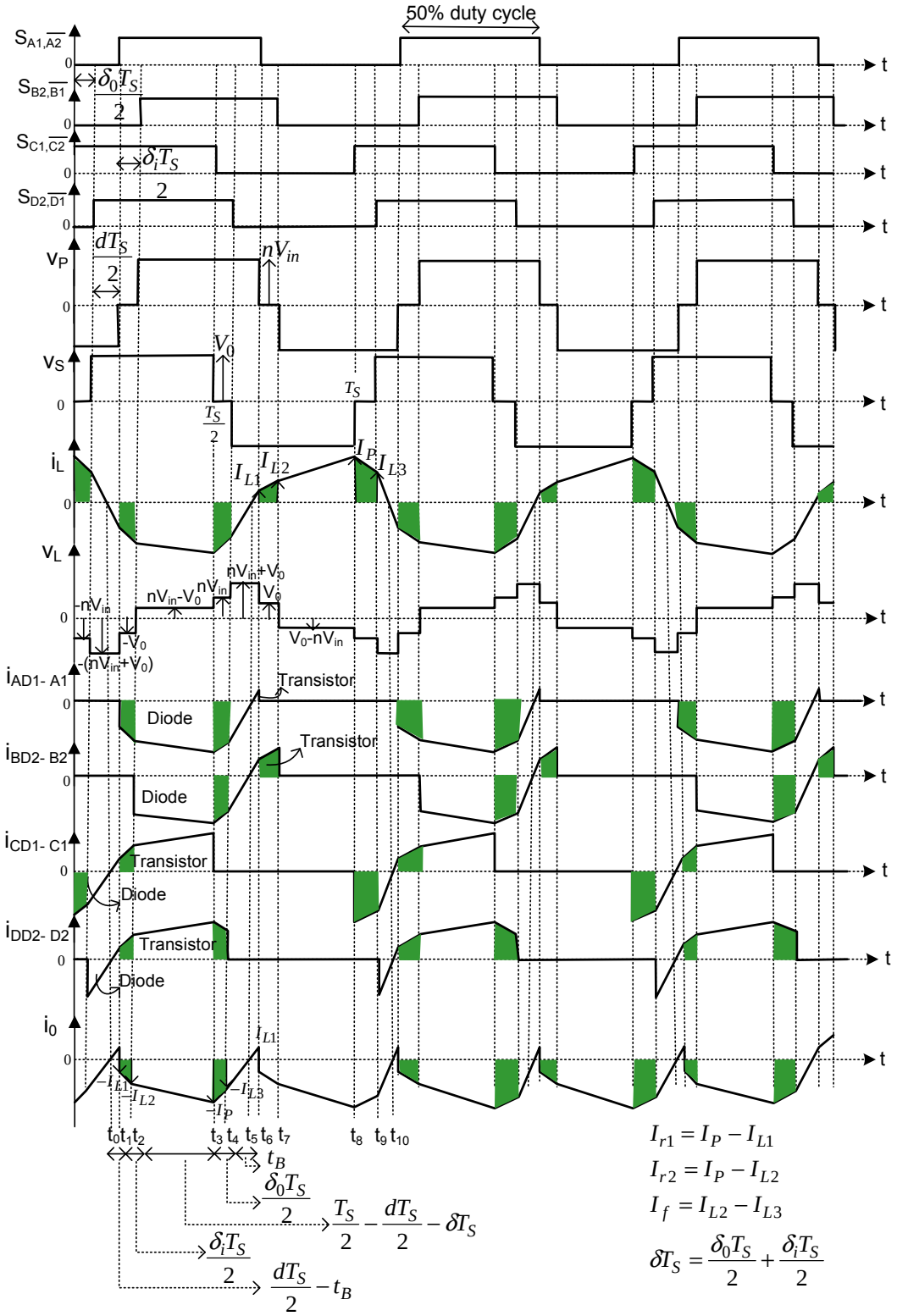
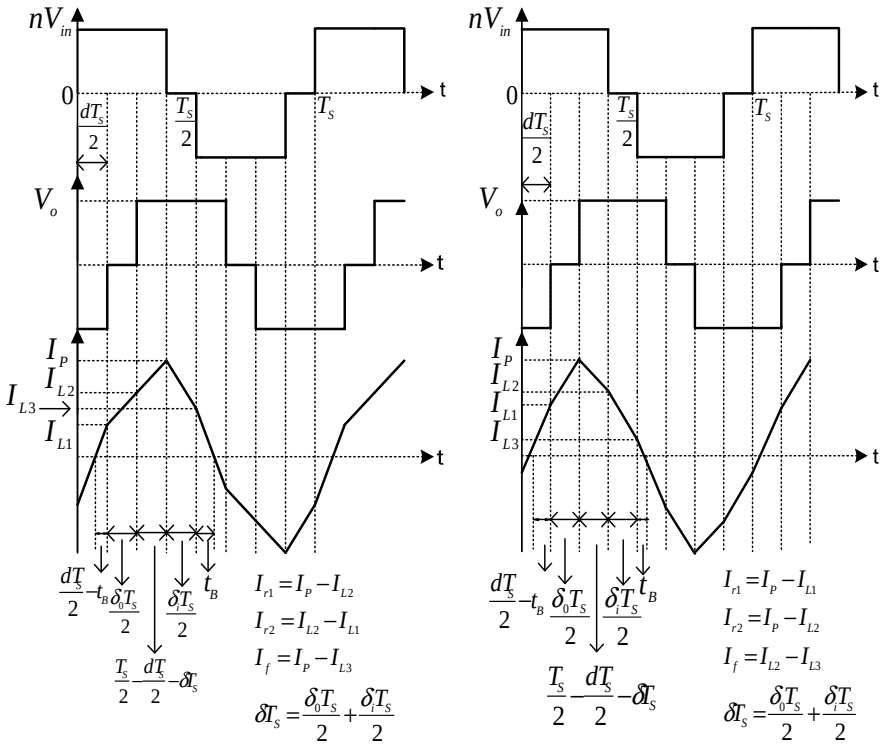


Figure 5.31 Ideal waveforms during discharging mode for quasi-square-wave applied on transformer primary and secondary

5.4.2 Mathematical model for buck and boost modes

Imposing a quasi-square-wave voltage on both sides of the transformer adds more complexity to the transformer and coupling inductor current waveforms. An analysis was performed by considering unequal dead-times in primary and secondary voltages. The average and RMS current equations were derived based on the assumption of loss-less components and a piece-wise linear waveform for i_L. Expressions for equal dead-times on primary and secondary voltages were obtained by substituting $\delta_i = \delta_0$. A detailed analysis for this mode of operation is given in Appendices B and C. Figure 5.32 presents simplified operational waveforms of the DAB converter for this method of control. 'δ_i' refers to the dead-time in the primary voltage and 'δ_0' indicates the dead-time in the secondary voltage of the transformer. The time intervals for various currents are marked in Figure 5.32. Tables 5.19 and 5.20 list the key equations for buck and boost modes respectively.



(a) Buck mode (b) Boost mode

Figure 5.32 Simplified operational waveforms for quasi-square-wave voltage applied on transformer primary and secondary

Table 5.19 Key equations for quasi-square-wave applied on transformer primary and secondary – Buck mode

$I_{L3} = \frac{T_S}{4L}\left[nV_{in}(1-\delta_i) + V_o(2d+\delta_0-1)\right]$
$I_{L1} = \frac{T_S}{4L}\left[nV_{in}(2d+\delta_i-1) + V_o(1-\delta_0)\right]$
$I_P = \frac{T_S}{4L}\left[nV_{in}(1-\delta_i) + V_0(2d-1+\delta_0+2\delta_i)\right]$
$I_{L2} = \frac{T_S}{4L}\left[nV_{in}(2d+\delta_i+2\delta_0-1) + V_o(1-\delta_0)\right]$
$t_B = \frac{T_S\left[nV_{in}(1-\delta_i) + V_o(2d+\delta_0-1)\right]}{4(nV_{in}+V_o)}$
$I_o = \frac{nV_{in}T_S}{2L}\left(d - d^2 - d\delta_i - d\delta_0 + \frac{\delta_i}{2} + \frac{\delta_0}{2} - \frac{{\delta_i}^2}{2} - \frac{{\delta_0}^2}{2} - \frac{\delta_i\delta_0}{2}\right)$
$I_{RMS} = \sqrt{\frac{2}{T_S}\left[\frac{{I_{L1}}^2}{3}\left(\frac{dT_S}{2} - t_B\right) + \left(\frac{\delta T_S}{2}\right)\left({I_{L1}}^2 + \frac{{I_{r2}}^2}{3} + I_{L1}I_{r2} + {I_P}^2 + \frac{{I_f}^2}{3} - I_P I_f\right) + \left(\frac{T_S}{2} - \frac{dT_S}{2} - \delta T_S\right)\left({I_{L2}}^2 + \frac{{I_{r1}}^2}{3} + I_{L2}I_{r1}\right) + \frac{{I_{L3}}^2 t_B}{3}\right]}$
$I_{L1} = \frac{T_S}{4L}\left[nV_{in}(2d+\delta_i-1) + V_o(1-\delta_0)\right] \geq 0$, condition for ZVS
$d \geq 0.5 - \frac{\delta_i}{2} - \frac{V_o'}{2}(1-\delta_0)$, duty ratio at which ZVS occurs

Table 5.20 Key equations of quasi-square-wave applied on transformer primary and secondary – Boost mode

$I_{L3} = \frac{T_S}{4L}\left[nV_{in}(1-\delta_i) + V_o(2d+\delta_0-1)\right]$
$I_{L1} = \frac{T_S}{4L}\left[nV_{in}(2d+\delta_i-1) + V_o(1-\delta_0)\right]$
$I_P = \frac{T_S}{4L}\left[nV_{in}(2d+\delta_i+2\delta_0-1) + V_o(1-\delta_0)\right]$
$I_{L2} = \frac{T_S}{4L}\left[nV_{in}(1-\delta_i) + V_0(2d-1+\delta_0+2\delta_i)\right]$
$t_B = \frac{T_S\left[nV_{in}(1-\delta_i) + V_o(2d+\delta_0-1)\right]}{4(nV_{in}+V_o)}$
$I_o = \frac{nV_{in}T_S}{2L}\left(d - d^2 - d\delta_i - d\delta_0 + \frac{\delta_i}{2} + \frac{\delta_0}{2} - \frac{{\delta_i}^2}{2} - \frac{{\delta_0}^2}{2} - \frac{\delta_i\delta_0}{2}\right)$
$I_{RMS} = \sqrt{\frac{2}{T_S}\left[\frac{{I_{L1}}^2}{3}\left(\frac{dT_S}{2} - t_B\right) + \left(\frac{\delta T_S}{2}\right)\left({I_{L1}}^2 + \frac{{I_{r1}}^2}{3} + I_{L1}I_{r1} + {I_{L2}}^2 + \frac{{I_f}^2}{3} - I_{L2}I_f\right) + \left(\frac{T_S}{2} - \frac{dT_S}{2} - \delta T_S\right)\left({I_P}^2 + \frac{{I_{r2}}^2}{3} - I_P I_{r2}\right) + \frac{{I_{L3}}^2 t_B}{3}\right]}$
$I_{L3} = \frac{T_S}{4L}\left[nV_{in}(1-\delta_i) + V_o(2d+\delta_0-1)\right] \geq 0$, condition for ZVS
$d \geq 0.5 - \frac{\delta_0}{2} - \frac{1}{2V_o'}(1-\delta_i)$, duty ratio at which ZVS occurs

Tables 5.21 and 5.22 give the average and RMS current equations of the converter for the buck mode of operation with unequal dead-times on the primary and secondary voltages respectively. Various device current waveforms are presented and step-by-step derivations are given in Appendices B and C.

Table 5.21 Average current equations of various devices in the DAB converter under buck mode - Quasi-square-wave voltage on transformer primary and secondary

Device	Average current equation
HV side leading Transistor	$\frac{\frac{1}{2}\times I_{L1}\times\left(\frac{dT_S}{2}-t_B\right)+\frac{1}{2}\times(I_{L1}+I_{L2})\times\frac{\delta_0 T_S}{2}+\frac{1}{2}\times(I_{L2}+I_P)\times\left(\frac{T_S}{2}-\frac{dT_S}{2}-\delta T_S\right)}{\left(\frac{T_S}{2}-\delta T_S+\frac{\delta_0 T_S}{2}-t_B\right)}$
HV side leading Diode	$\frac{\frac{1}{2}\times(I_P+I_{L3})\times\frac{\delta_i T_S}{2}+\frac{1}{2}\times(I_{L3})\times t_B}{\left(\frac{\delta_i T_S}{2}+t_B\right)}$
HV side lagging Transistor	$\frac{\frac{1}{2}\times I_{L1}\times\left(\frac{dT_S}{2}-t_B\right)+\frac{1}{2}\times(I_{L1}+I_{L2})\times\frac{\delta_0 T_S}{2}+\frac{1}{2}\times(I_{L2}+I_P)\times\left(\frac{T_S}{2}-\frac{dT_S}{2}-\delta T_S\right)+\frac{1}{2}\times(I_P+I_{L3})\times\frac{\delta_i T_S}{2}}{\left(\frac{T_S}{2}-t_B\right)}$
HV side lagging Diode	$\frac{\frac{1}{2}\times(I_{L3})\times t_B}{t_B}$
LV side leading Transistor	$\frac{\frac{1}{2}\times I_{L1}\times\left(\frac{dT_S}{2}-t_B\right)}{\left(\frac{dT_S}{2}-t_B\right)}$
LV side leading Diode	$\frac{\frac{1}{2}\times(I_{L1}+I_{L2})\times\frac{\delta_0 T_S}{2}+\frac{1}{2}\times(I_{L2}+I_P)\times\left(\frac{T_S}{2}-\frac{dT_S}{2}-\delta T_S\right)+\frac{1}{2}\times(I_P+I_{L3})\times\frac{\delta_i T_S}{2}+\frac{1}{2}\times I_{L3}\times(t_B)}{\left(\frac{T_S}{2}-\frac{dT_S}{2}+t_B\right)}$
LV side lagging Transistor	$\frac{\frac{1}{2}\times I_{L1}\times\left(\frac{dT_S}{2}-t_B\right)+\frac{1}{2}\times(I_{L1}+I_{L2})\times\frac{\delta_0 T_S}{2}}{\left(\frac{dT_S}{2}-t_B+\frac{\delta_0 T_S}{2}\right)}$
LV side lagging Diode	$\frac{\frac{1}{2}\times(I_{L2}+I_P)\times\left(\frac{T_S}{2}-\frac{dT_S}{2}-\delta T_S\right)+\frac{1}{2}\times(I_P+I_{L3})\times\frac{\delta_i T_S}{2}+\frac{1}{2}\times I_{L3}\times(t_B)}{\left(\frac{T_S}{2}-\frac{dT_S}{2}-\delta T_S+\frac{\delta_i T_S}{2}+t_B\right)}$

Table 5.22 RMS current equations of various devices in the DAB converter under buck mode - Quasi-square-wave voltage on transformer primary and secondary

Device	RMS current equation
HV side leading Transistor	$\sqrt{\frac{1}{T_S}\left[\frac{I_{L1}^2\times\left(\frac{dT_S}{2}-t_B\right)}{3}+\left(I_{L1}^2+\frac{I_{r2}^2}{3}+I_{L1}I_{r2}\right)\times\frac{\delta_0 T_S}{2}+\left(\frac{T_S}{2}-\frac{dT_S}{2}-\delta T_S\right)\times\left(I_{L2}^2+\frac{I_{r1}^2}{3}+I_{L2}I_{r1}\right)\right]}$
HV side leading Diode	$\sqrt{\frac{1}{T_S}\left[\left(\frac{\delta_i T_S}{2}\right)\times\left(I_P^2+\frac{I_f^2}{3}-I_P I_f\right)+\frac{I_{L3}^2\times(t_B)}{3}\right]}$
HV side lagging Transistor	$\sqrt{\frac{1}{T_S}\left[\frac{I_{L1}^2\times\left(\frac{dT_S}{2}-t_B\right)}{3}+\left(\frac{\delta_0 T_S}{2}\right)\times\left(I_{L1}^2+\frac{I_{r2}^2}{3}+I_{L1}I_{r2}\right)+\left(\frac{T_S}{2}-\frac{dT_S}{2}-\delta T_S\right)\times\left(I_{L2}^2+\frac{I_{r1}^2}{3}+I_{L2}I_{r1}\right)+\left(\frac{\delta_i T_S}{2}\right)\times\left(I_P^2+\frac{I_f^2}{3}-I_P I_f\right)\right]}$
HV side lagging Diode	$\sqrt{\frac{1}{T_S}\left[\frac{I_{L3}^2\times(t_B)}{3}\right]}$
LV side leading Transistor	$\sqrt{\frac{1}{T_S}\left[\frac{I_{L1}^2\times\left(\frac{dT_S}{2}-t_B\right)}{3}\right]}$
LV side leading Diode	$\sqrt{\frac{1}{T_S}\left[\left(\frac{\delta_0 T_S}{2}\right)\times\left(I_{L1}^2+\frac{I_{r2}^2}{3}+I_{L1}I_{r2}\right)+\left(\frac{T_S}{2}-\frac{dT_S}{2}-\delta T_S\right)\times\left(I_{L2}^2+\frac{I_{r1}^2}{3}+I_{L2}I_{r1}\right)+\left(\frac{\delta_i T_S}{2}\right)\times\left(I_P^2+\frac{I_f^2}{3}-I_P I_f\right)+\frac{I_{L3}^2\times(t_B)}{3}\right]}$
LV side lagging Transistor	$\sqrt{\frac{1}{T_S}\left[\frac{I_{L1}^2\times\left(\frac{dT_S}{2}-t_B\right)}{3}+\left(I_{L1}^2+\frac{I_{r2}^2}{3}+I_{L1}I_{r2}\right)\times\frac{\delta_0 T_S}{2}\right]}$
LV side lagging Diode	$\sqrt{\frac{1}{T_S}\left[\left(\frac{T_S}{2}-\frac{dT_S}{2}-\delta T_S\right)\times\left(I_{L2}^2+\frac{I_{r1}^2}{3}+I_{L2}I_{r1}\right)+\left(\frac{\delta_i T_S}{2}\right)\times\left(I_P^2+\frac{I_f^2}{3}-I_P I_f\right)+\frac{I_{L3}^2\times(t_B)}{3}\right]}$

Similarly for the boost mode, with unequal dead-times on primary and secondary voltages, the resulting average and RMS device current equations are presented in Tables 5.23 and 5.24 respectively. A detailed analysis can be found in Appendices B and C.

Table 5.23 Average current equations of various devices in the DAB converter under boost mode - Quasi-square-wave voltage on transformer primary and secondary

Device	Average current equation
LV side leading Transistor	$\frac{\frac{1}{2}\times I_{L1}\times\left(\frac{dT_S}{2}-t_B\right)+\frac{1}{2}\times(I_{L1}+I_P)\times\frac{\delta_0 T_S}{2}+\frac{1}{2}\times(I_P+I_{L2})\times\left(\frac{T_S}{2}-\frac{dT_S}{2}-\delta T_S\right)}{\left(\frac{T_S}{2}-\delta T_S+\frac{\delta_0 T_S}{2}-t_B\right)}$
LV side leading Diode	$\frac{\frac{1}{2}\times(I_{L2}+I_{L3})\times\frac{\delta_i T_S}{2}+\frac{1}{2}\times(I_{L3})\times t_B}{\left(\frac{\delta_i T_S}{2}+t_B\right)}$
LV side lagging Transistor	$\frac{\frac{1}{2}\times I_{L1}\times\left(\frac{dT_S}{2}-t_B\right)+\frac{1}{2}\times(I_{L1}+I_P)\times\frac{\delta_0 T_S}{2}+\frac{1}{2}\times(I_P+I_{L2})\times\left(\frac{T_S}{2}-\frac{dT_S}{2}-\delta T_S\right)+\frac{1}{2}\times(I_{L2}+I_{L3})\times\frac{\delta_i T_S}{2}}{\left(\frac{T_S}{2}-t_B\right)}$
LV side lagging Diode	$\frac{\frac{1}{2}\times(I_{L3})\times t_B}{t_B}$
HV side leading Transistor	$\frac{\frac{1}{2}\times I_{L1}\times\left(\frac{dT_S}{2}-t_B\right)}{\left(\frac{dT_S}{2}-t_B\right)}$
HV side leading Diode	$\frac{\frac{1}{2}\times(I_{L1}+I_P)\times\frac{\delta_0 T_S}{2}+\frac{1}{2}\times(I_P+I_{L2})\times\left(\frac{T_S}{2}-\frac{dT_S}{2}-\delta T_S\right)+\frac{1}{2}\times(I_{L2}+I_{L3})\times\frac{\delta_i T_S}{2}+\frac{1}{2}\times I_{L3}\times(t_B)}{\left(\frac{T_S}{2}-\frac{dT_S}{2}+t_B\right)}$
HV side lagging Transistor	$\frac{\frac{1}{2}\times I_{L1}\times\left(\frac{dT_S}{2}-t_B\right)+\frac{1}{2}\times(I_{L1}+I_P)\times\frac{\delta_0 T_S}{2}}{\left(\frac{dT_S}{2}-t_B+\frac{\delta_0 T_S}{2}\right)}$
HV side lagging Diode	$\frac{\frac{1}{2}\times(I_P+I_{L2})\times\left(\frac{T_S}{2}-\frac{dT_S}{2}-\delta T_S\right)+\frac{1}{2}\times(I_{L2}+I_{L3})\times\frac{\delta_i T_S}{2}+\frac{1}{2}\times I_{L3}\times(t_B)}{\left(\frac{T_S}{2}-\frac{dT_S}{2}-\delta T_S+\frac{\delta_i T_S}{2}+t_B\right)}$

Table 5.24 RMS current equations of various devices in the DAB converter under boost mode - Quasi-square-wave voltage on transformer primary and secondary

Device	RMS current equation
LV side leading Transistor	$\sqrt{\frac{1}{T_S}\left[\frac{I_{L1}^2\times\left(\frac{dT_S}{2}-t_B\right)}{3}+\left(I_{L1}^2+\frac{I_{r1}^2}{3}+I_{L1}I_{r1}\right)\times\frac{\delta_0 T_S}{2}+\left(\frac{T_S}{2}-\frac{dT_S}{2}-\delta T_S\right)\times\left(I_P^2+\frac{I_{r2}^2}{3}-I_P I_{r2}\right)\right]}$
LV side leading Diode	$\sqrt{\frac{1}{T_S}\left[\left(\frac{\delta_i T_S}{2}\right)\times\left(I_{L2}^2+\frac{I_f^2}{3}-I_{L2}I_f\right)+\frac{I_{L3}^2\times(t_B)}{3}\right]}$
LV side lagging Transistor	$\sqrt{\frac{1}{T_S}\left[\frac{I_{L1}^2\times\left(\frac{dT_S}{2}-t_B\right)}{3}+\left(\frac{\delta_0 T_S}{2}\right)\times\left(I_{L1}^2+\frac{I_{r1}^2}{3}+I_{L1}I_{r1}\right)+\left(\frac{T_S}{2}-\frac{dT_S}{2}-\delta T_S\right)\times\left(I_P^2+\frac{I_{r2}^2}{3}-I_P I_{r2}\right)+\left(\frac{\delta_i T_S}{2}\right)\times\left(I_{L2}^2+\frac{I_f^2}{3}-I_{L2}I_f\right)\right]}$
LV side lagging Diode	$\sqrt{\frac{1}{T_S}\left[\frac{I_{L3}^2\times(t_B)}{3}\right]}$
HV side leading Transistor	$\sqrt{\frac{1}{T_S}\left[\frac{I_{L1}^2\times\left(\frac{dT_S}{2}-t_B\right)}{3}\right]}$
HV side leading Diode	$\sqrt{\frac{1}{T_S}\left[\left(\frac{\delta_0 T_S}{2}\right)\times\left(I_{L1}^2+\frac{I_{r1}^2}{3}+I_{L1}I_{r1}\right)+\left(\frac{T_S}{2}-\frac{dT_S}{2}-\delta T_S\right)\times\left(I_P^2+\frac{I_{r2}^2}{3}-I_P I_{r2}\right)+\left(\frac{\delta_i T_S}{2}\right)\times\left(I_{L2}^2+\frac{I_f^2}{3}-I_{L2}I_f\right)+\frac{I_{L3}^2\times(t_B)}{3}\right]}$
HV side lagging Transistor	$\sqrt{\frac{1}{T_S}\left[\frac{I_{L1}^2\times\left(\frac{dT_S}{2}-t_B\right)}{3}+\left(I_{L1}^2+\frac{I_{r1}^2}{3}+I_{L1}I_{r1}\right)\times\frac{\delta_0 T_S}{2}\right]}$
HV side lagging Diode	$\sqrt{\frac{1}{T_S}\left[\left(\frac{T_S}{2}-\frac{dT_S}{2}-\delta T_S\right)\times\left(I_P^2+\frac{I_{r2}^2}{3}-I_P I_{r2}\right)+\left(\frac{\delta_i T_S}{2}\right)\times\left(I_{L2}^2+\frac{I_f^2}{3}-I_{L2}I_f\right)+\frac{I_{L3}^2\times(t_B)}{3}\right]}$

5.4.3 Performance evaluation

The performance of the DAB converter has been evaluated based on the mathematical models for buck and boost modes considering equal dead-times on the transformer primary and secondary voltages for the sake of simplicity. The following sub-sections give more detail.

5.4.3.1 ZVS operating range

The quasi-square-wave mode of operation improves the ZVS operating range of the converter in buck and boost modes of operation over a wide range of voltage conversion ratios. This is

evident from Figures 5.33 and 5.34. The duty ratio required to achieve soft switching is far less than that for the square-wave mode of operation. For example, even for a very short dead-time of $\delta_i = \delta_0 = 0.1$, with a voltage conversion ratio of 0.5 during buck mode, ZVS occurs at $d = 0.225$. This enables an improvement in ZVS range in comparison with the square-wave mode of 10%. During boost mode for $\delta_i = \delta_0 = 0.2$, and with a voltage conversion ratio of 10, ZVS occurs at $d = 0.36$, providing an improvement in ZVS range compared to the square-wave mode of 20%.

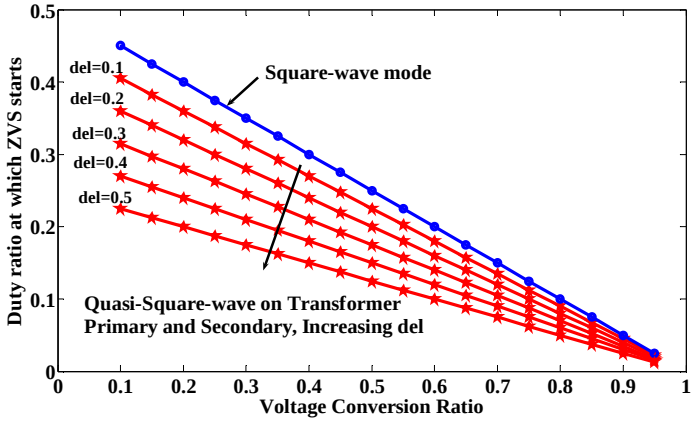


Figure 5.33 ZVS boundaries for buck mode of operation and various values of dead-time (del = δ)

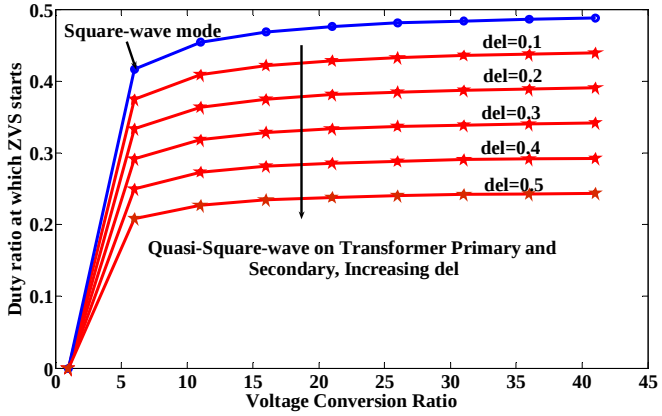


Figure 5.34 ZVS boundaries for boost mode of operation and various values of dead-time (del = δ)

5.4.3.2 Power transfer and converter efficiency

Figure 5.35 shows output current versus duty ratio for several values of δ. Introducing dead-time in the transformer primary and secondary voltages shifts the maximum power transfer point towards lower duty ratios and this makes maximum power transfer possible for duty

ratios less than 0.5. As with the previous mode, the region to the left of the maximum of each curve in Figure 5.35 is of interest, since the RMS and peak currents for the given phase shift are more to the right of the maximum. Another advantage (apart from ZVS enhancement) of quasi-square-wave mode is that it increases the net power transfer by as much as 100%, at a reduced value of duty ratio and dead-time. For example, the net power transferred when operating with conventional square-wave mode is 11.1kW at 125V and at d = 0.075; for the quasi-square-wave mode with $\delta_i = \delta_0 = 0.1$ and d = 0.075, net power transferred is 22.3kW. Thus, there is over a 100% increase. This is summarised in Figure 5.36.

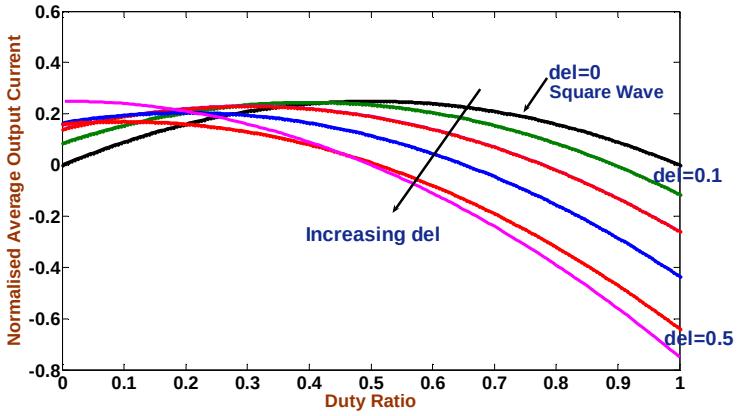


Figure 5.35 Normalised average output current as a function of duty ratio for different values of dead-time (del = δ)

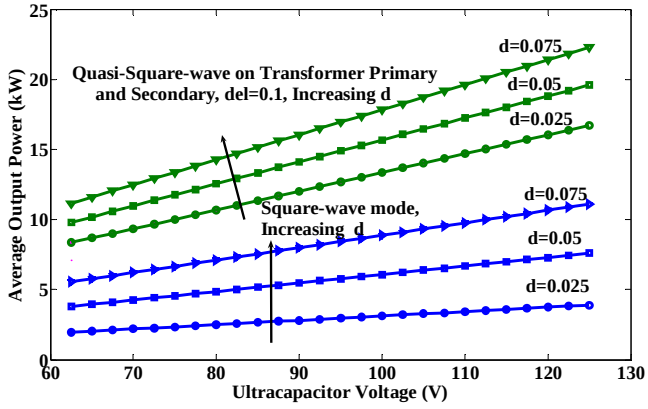


Figure 5.36 Comparison of average power transfer of quasi-square-wave mode with square-wave mode (del = δ)

5.4.3.3 RMS and peak inductor/transformer currents

RMS and peak values of inductor currents for the quasi-square-wave mode are compared with those of the square-wave mode in this section. Increased values of RMS and peak currents over those of the square-wave mode are observed; this is illustrated for different values of the dead-time in Figures 5.37 and 5.38. Consequently, there is a trade-off between conduction and switching losses at high power transfer. However, the approach increases the net power flow compared to that of the square-wave mode for a reduced duty ratio and dead-time, thus it is possible to transfer the rated power of 20kW at a reduced level of duty ratio and dead-time as discussed in section 5.4.3.2. Hence, an increase in RMS current at a reduced phase shift would not reduce the efficiency nor degrade the performance of the converter. It can be concluded that the quasi-square-wave mode of operation is suitable for low power transfer and enhancement of the ZVS range, whereas when operating in square-wave mode, ZVS becomes impossible under light-load conditions.

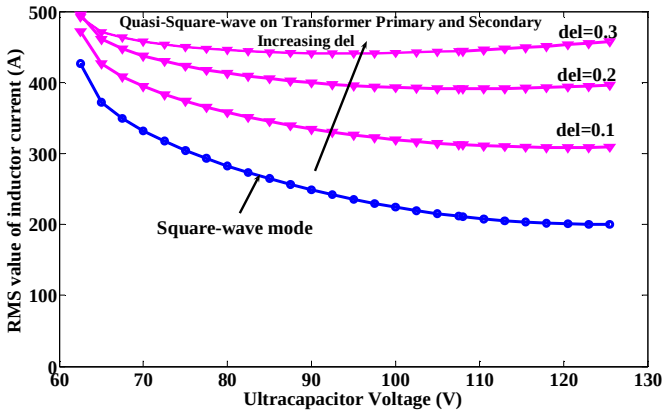


Figure 5.37 RMS value of leakage inductor current during quasi-square-wave mode (del = δ)

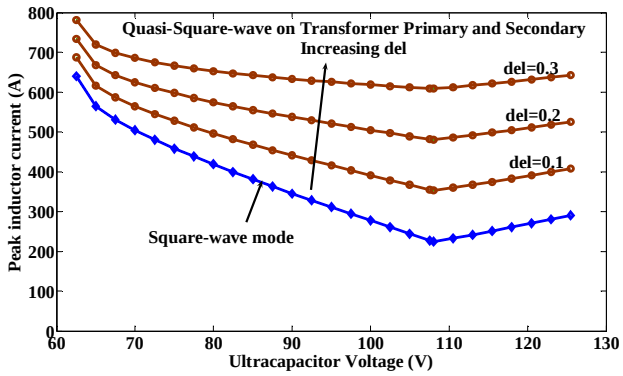


Figure 5.38 Peak value of leakage inductor current during quasi-square-wave mode (del = δ)

5.4.4 Simulation and Experimental results

This section presents the simulation and experimental results corresponding to quasi-square-wave voltages applied to both sides of the isolation transformer. Experimental results presented are for equal and unequal dead-times on both sides of the transformer. These results confirm the theory and mathematical models presented in the earlier sections. Figure 5.39 displays the simulation results for quasi-square-wave mode on both sides of the isolation transformer. It shows the AC link waveforms, device voltages and currents on the HV side and the LV side, and load voltage and current waveforms. According to the theoretical analysis, the steady state values are I_{L1} = 4.3A, I_{L2} = 10.85A, I_{L3} = 24.7A, peak inductor current I_P = 27.84A, average output current I_0 = 15.36A and inductor RMS current I_{RMS} = 16.93A. These values agree well with the SABER results, shown below.

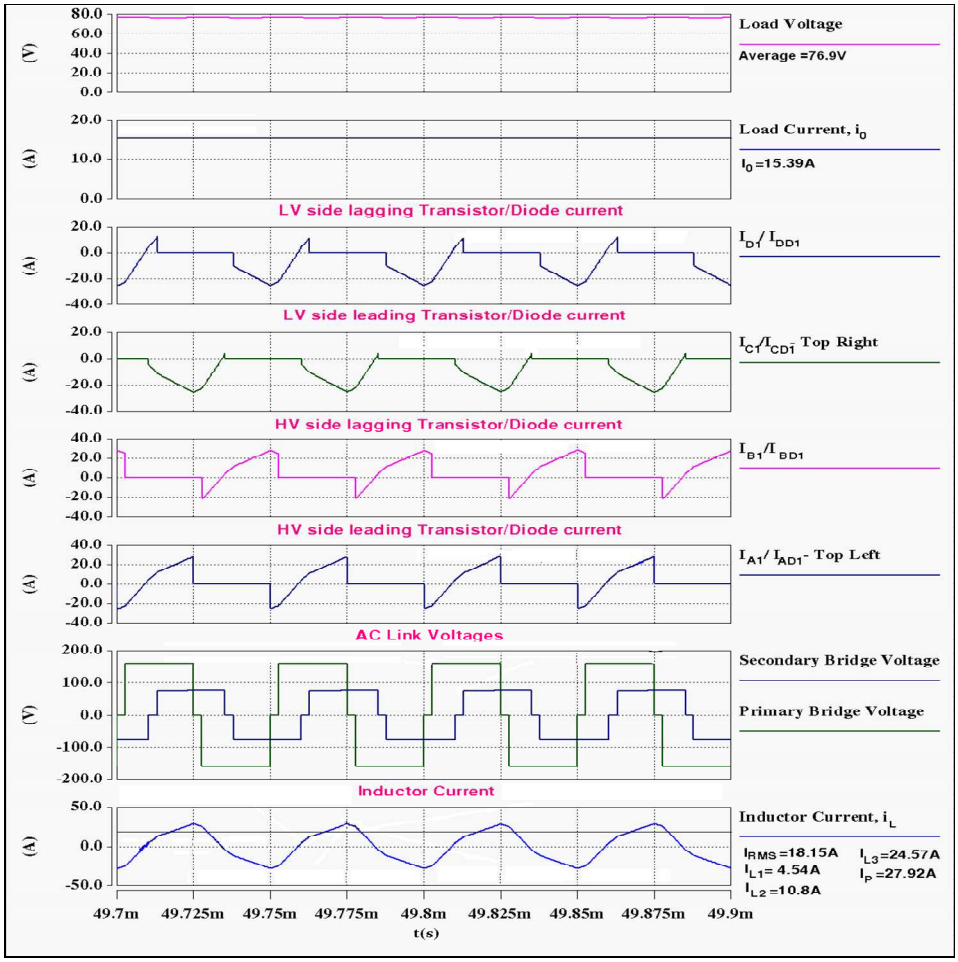


Figure 5.39 Simulation waveforms for quasi-square-wave on transformer primary and secondary
V_{in} = 160V, L = 61.2μH, f_S = 20kHz, P_{in} = 1kW, R = 5Ω, V_0 = 76.95V, $\delta_i = \delta_0$ = 0.1, d = 0.3

Figures 5.40 to 5.43 display the experimental waveforms of the DAB converter with quasi-square-wave voltages on both transformer primary and secondary. A dead-time of $\delta_i = \delta_0 = 0.1$ was introduced simultaneously on both sides of the transformer. In general, close agreement is evident between measured and simulation results. Figure 5.40 displays the AC link waveforms of the converter, and shows transformer primary and secondary currents and voltages generated by both bridges.

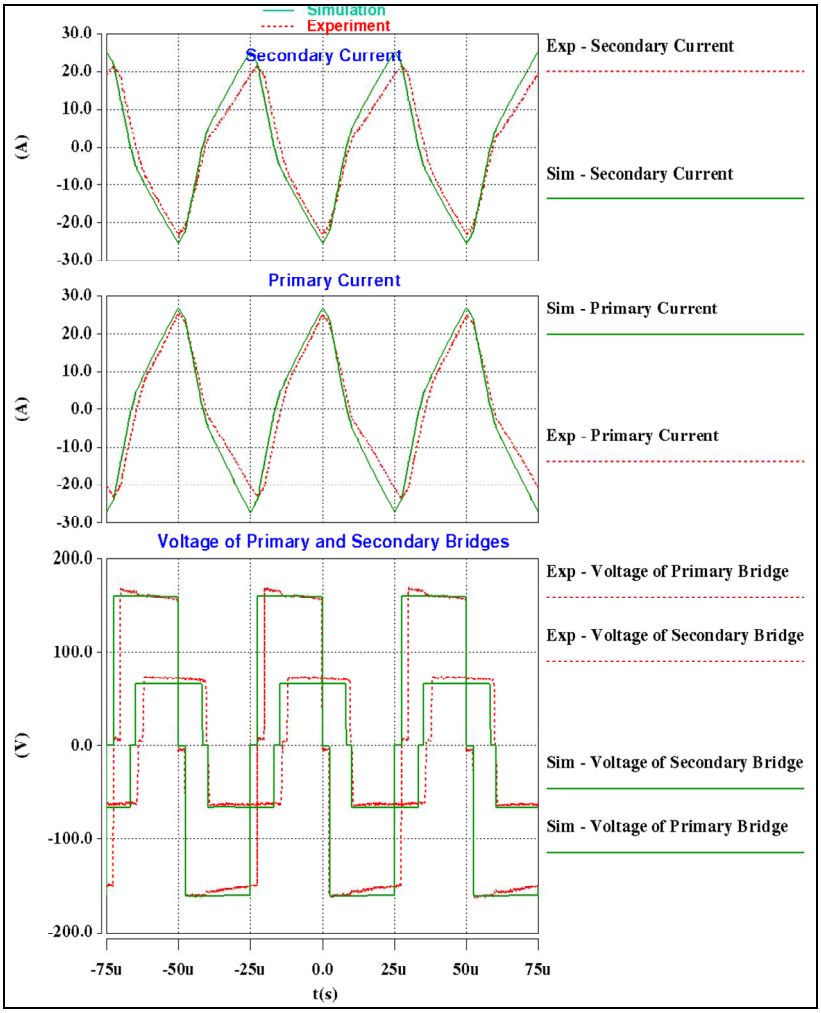


Figure 5.40 Experimental verification of AC link waveforms of the DAB converter for quasi-square-wave applied on transformer primary and secondary
V_{in} = 160V, L = 61.2μH, f_S = 20kHz, P_{in} = 1kW, R = 5Ω, V_0 = 65.05V, $\delta_i = \delta_0$ = 0.1, d = 0.3

Figure 5.41 shows the HV side device voltages and current waveforms. A slight variation in the duty ratio of the device voltages is seen due to the dual driver signal generation pattern for

phase leg IGBTs. The freewheeling interval of current is clearly seen from the slanting edge before turn-off of HV IGBT B_1 current waveforms as a result of the quasi-square-wave mode of operation.

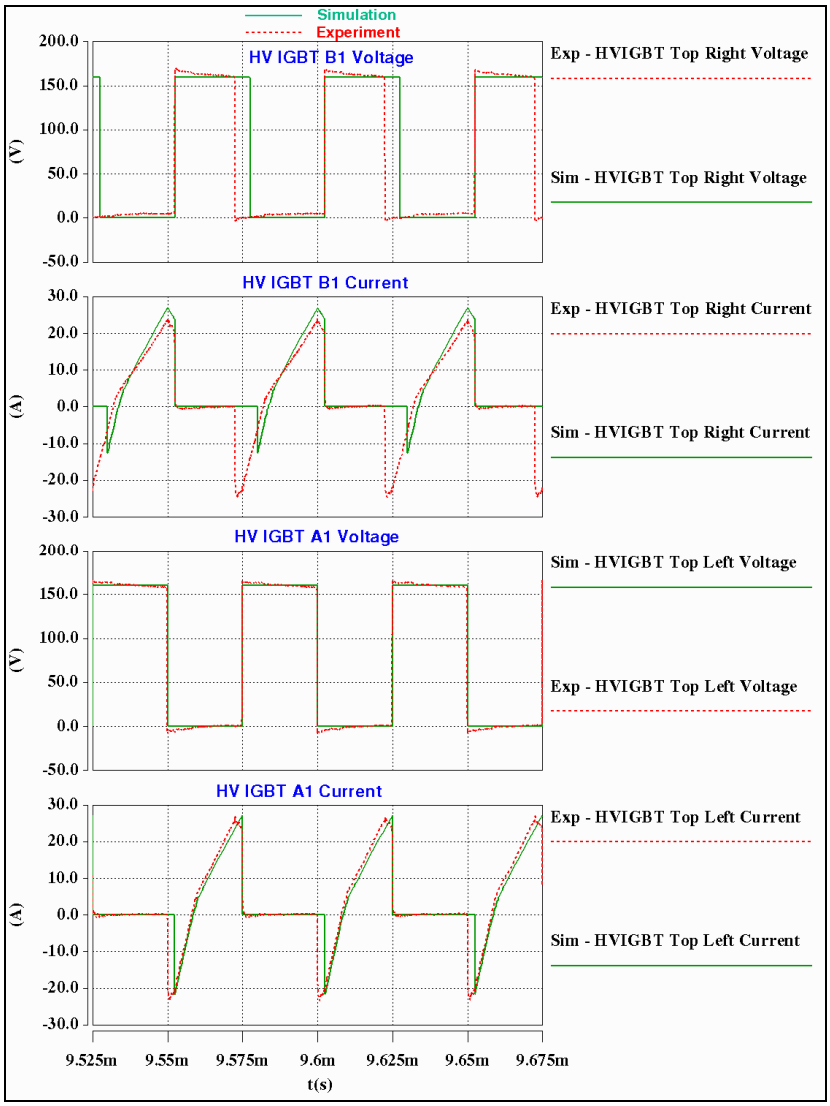


Figure 5.41 Experimental verification of HV side device waveforms of the DAB converter for quasi-square-wave applied on transformer primary and secondary
V_{in} = 160V, L = 61.2μH, f_S = 20kHz, P_{in} = 1kW, R = 5Ω, V_0 = 65.05V, $\delta_i = \delta_0$ = 0.1, d = 0.3

Figure 5.42 displays the LV device voltage and current waveforms. ZVS occurs at a duty ratio of 0.267 with $\delta_i = \delta_0$ = 0.1. However, for square-wave mode ZVS occurs at d = 0.297. Thus there is a 10% improvement in the ZVS operating range of the converter when quasi-square-wave voltages are applied to both sides of the transformer.

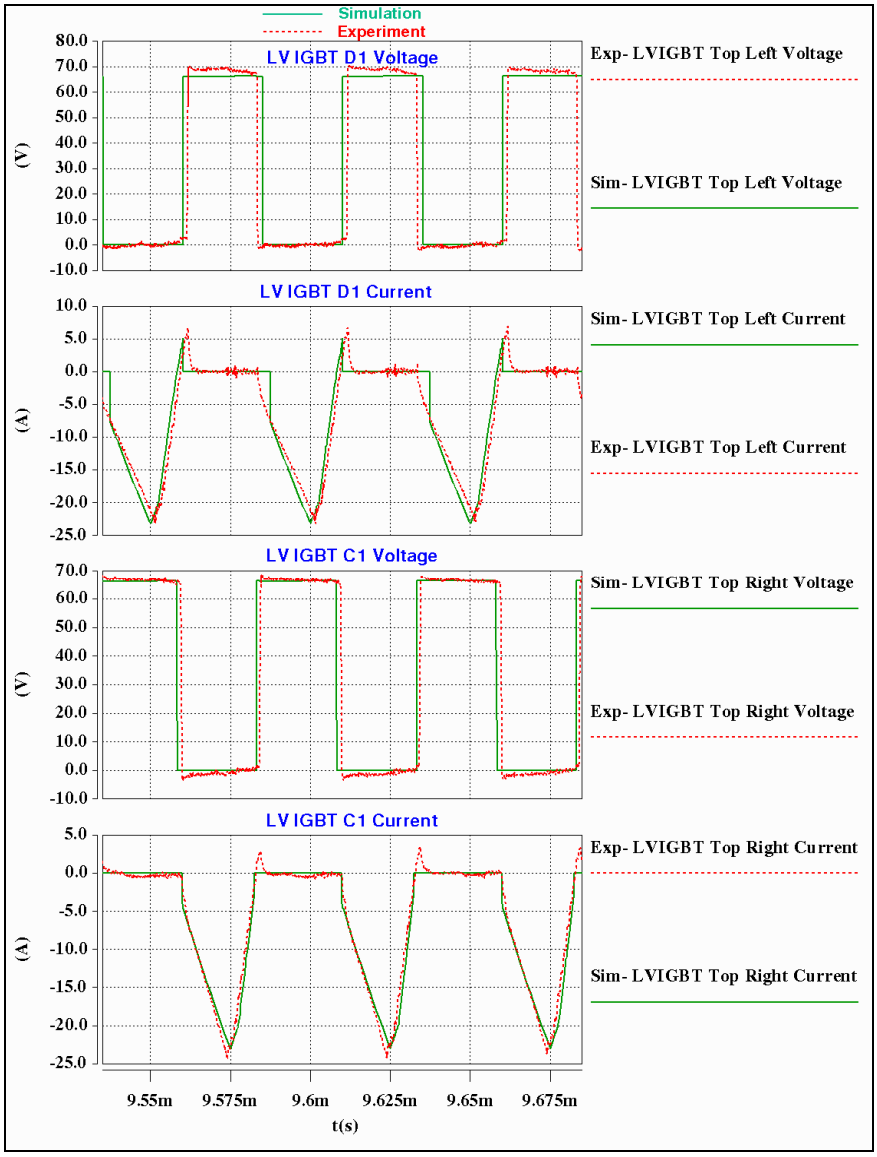


Figure 5.42 Experimental verification of LV side device waveforms of the DAB converter with quasi-square-wave applied on both transformer primary and secondary
V_{in} = 160V, L = 61.2μH, f_S = 20kHz, P_{in} = 1kW, R = 5Ω, V_0 = 65.05V, $\delta_i = \delta_0$ = 0.1, d = 0.3

Figure 5.43 shows the load current, load voltage and inductor current waveforms of the converter. The near zero voltage ripple at the output of the converter can be observed from the load voltage waveforms. The measured results confirm that the DAB converter operates with a high efficiency of 97.5% for quasi-square-wave mode on both the sides of the transformer, thus there is an improvement in efficiency over the square-wave mode of operation of 16.8%. This is because there is a 17% increase in the average output current of the converter over that

of the square-wave mode. An 11% reduction in switching losses on the HV side was observed due to ZVS and a 6.9 times higher switching loss on the LV side was observed due to increased switching current compared to that of the square-wave mode.

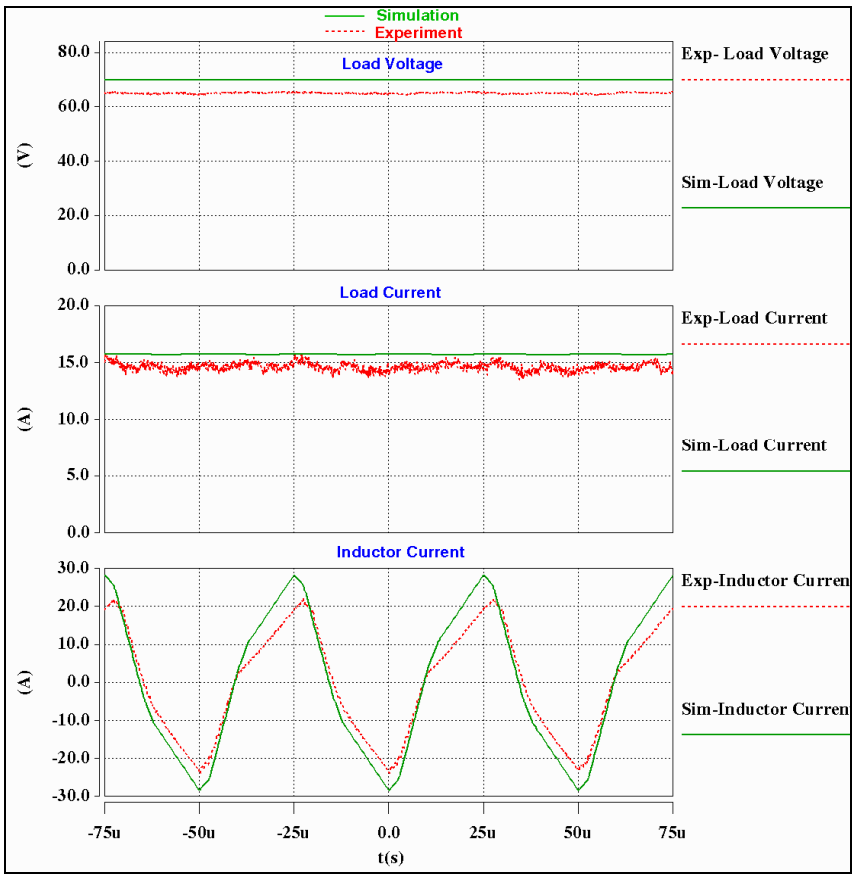


Figure 5.43 Experimental verification of load voltage, current and inductor current waveforms of the DAB converter for quasi-square-wave applied on both transformer primary and secondary V_{in} = 160V, L = 61.2μH, f_S = 20kHz, P_{in} = 1kW, R = 5Ω, V_0 = 65.05V, $\delta_i = \delta_0$ = 0.1, d = 0.3

Figures 5.44 to 5.47 display the experimental waveforms of the DAB converter for δ_i = 0.1 and δ_0 = 0.15. Once again, the measured results confirm the theory and mathematical models presented in section 5.4 of this Chapter. Experimental results were also taken for unequal dead-times δ_i = 0.15 and δ_0 =0.1. These results are similar to those obtained earlier with δ_i = 0.1 and δ_0 =0.15 on the primary and secondary sides respectively. Hence, the results pertaining to δ_i = 0.1 and δ_0 =0.15 are displayed as a proof of concept. Figure 5.44 shows the AC link waveforms of the converter.

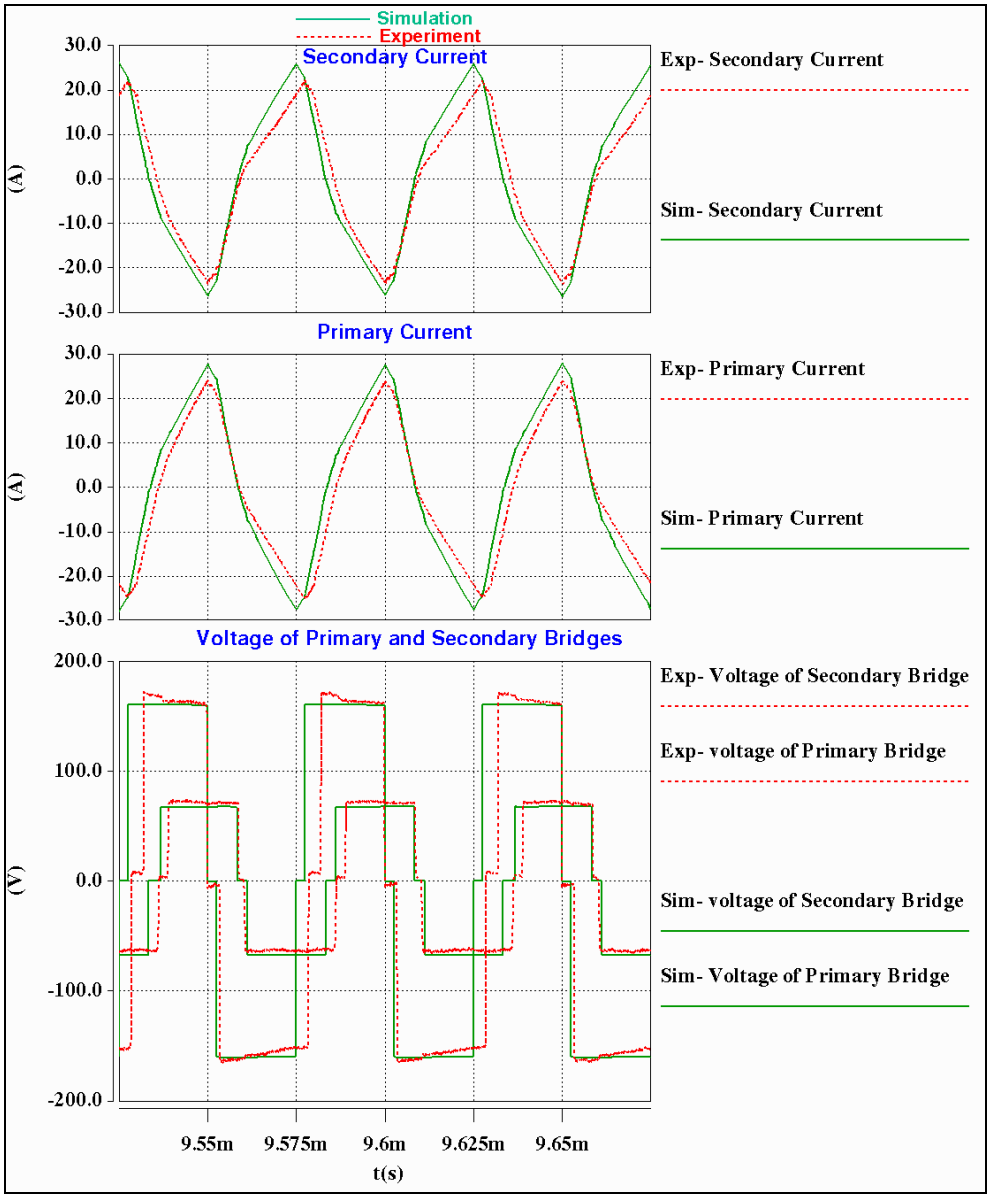


Figure 5.44 Experimental verification of AC link waveforms of the DAB converter for quasi-square-wave applied on both transformer primary and secondary
V_{in} = 160V, L = 61.2μH, f_S = 20kHz, P_{in} = 1kW, R = 5Ω, V_0 = 71.8V, δ_i = 0.1, δ_0 = 0.15, d = 0.3

Figure 5.45 depicts the HV side IGBTs (A_1 and B_1) voltage and current waveforms. Again, the duty ratio variations due to the driver signals are apparent in the voltage and current waveforms of the converter. Slight mismatches in the component values, winding resistances and duty ratios in the practical system produce further differences between the experimental and simulated waveforms.

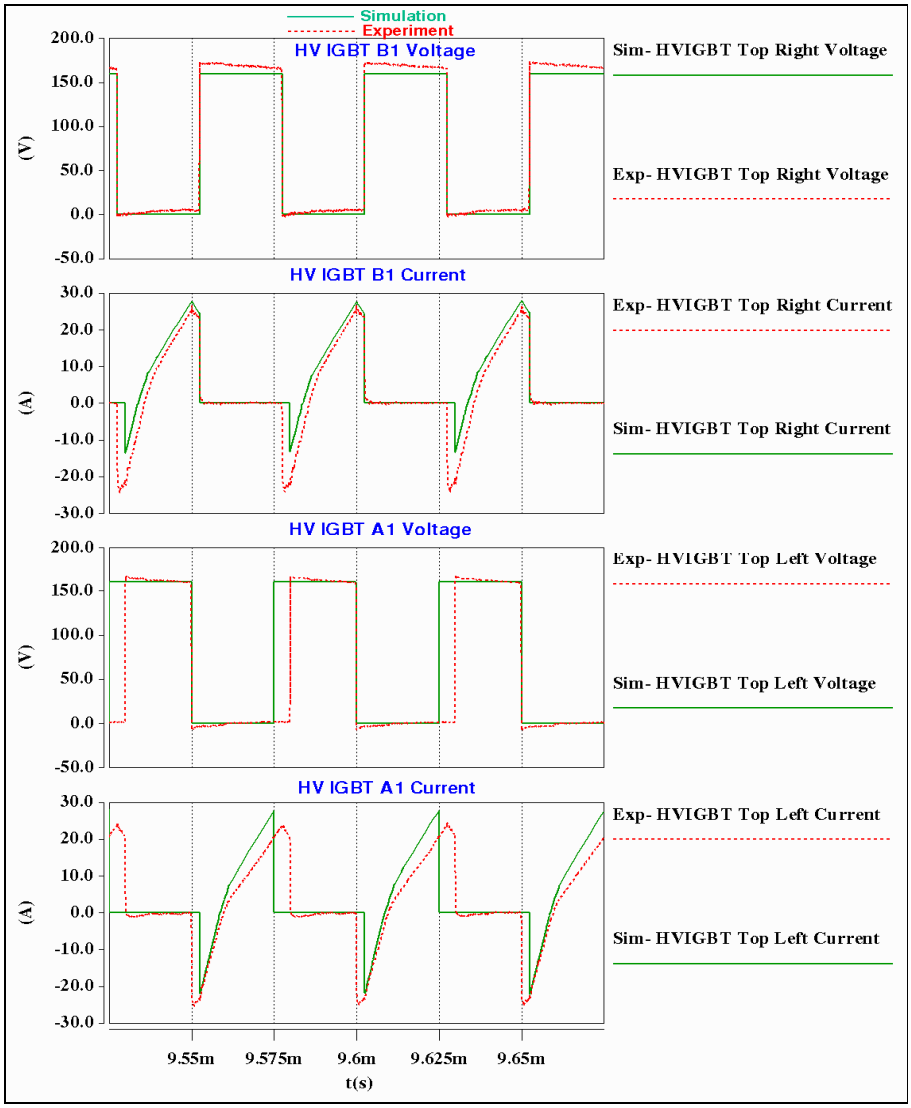


Figure 5.45 Experimental verification of HV side device waveforms of the DAB converter for quasi-square-wave applied on transformer primary and secondary
V_{in} = 160V, L = 61.2μH, f_S = 20kHz, P_{in} = 1kW, R = 5Ω, V_0 = 71.8V, δ_i = 0.1, δ_0 = 0.15, d = 0.3

Figure 5.46 shows the LV side devices (C_1 and D_2) voltage and current waveforms. From Figure 5.46, it can be noticed that the experimental measurement of LV IGBT D_2 voltage waveform (shown in dotted red lines) goes slightly negative. This is due to auto-zero problems with the measurement probe (ADP305). A current pulse of nearly 9A appears in the LV side IGBT D_2 current waveform. This is due to the converter operating slightly outside ZVS

boundary region due to slight mismatch in the component values, duty ratios and winding resistances in the practical system.

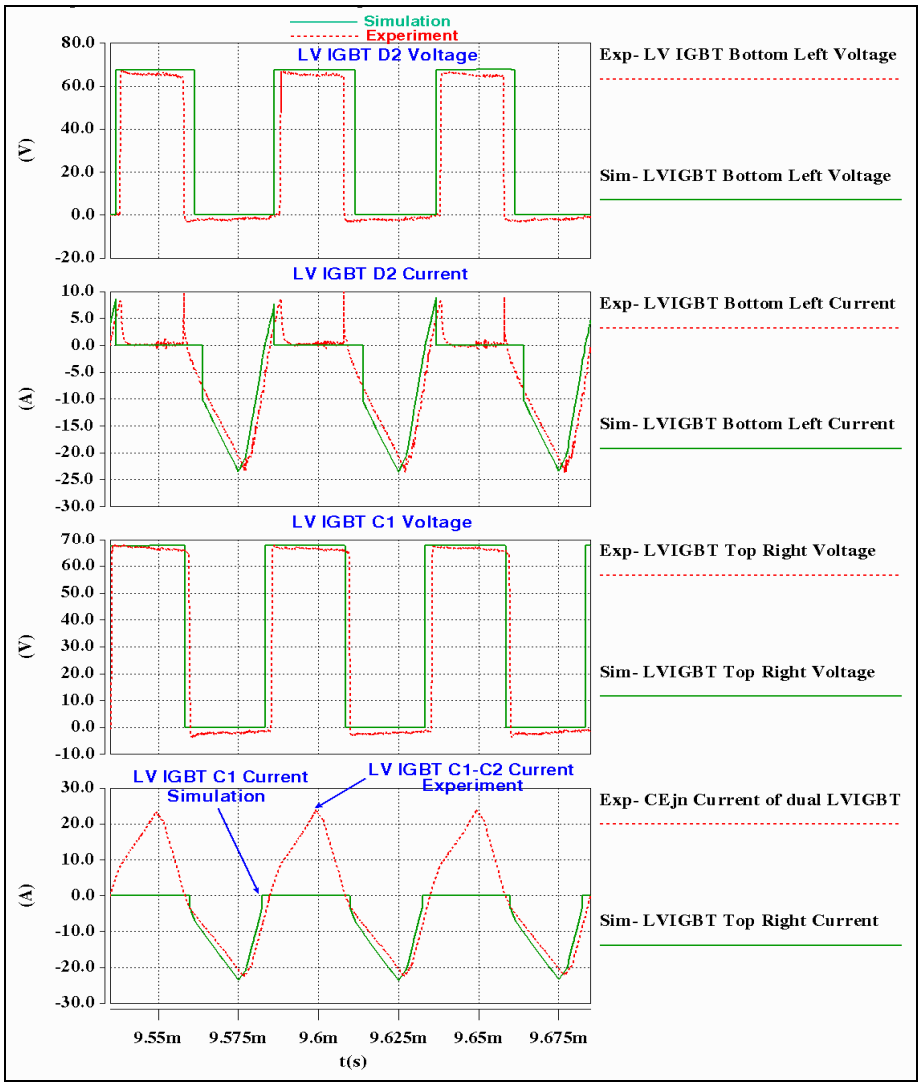


Figure 5.46 Experimental verification of LV side device waveforms of the DAB converter for quasi-square-wave applied on transformer primary and secondary
V_{in} = 160V, L = 61.2μH, f_S = 20kHz, P_{in} = 1kW, R = 5Ω, V_0 = 71.8V, δ_i = 0.1, δ_0 = 0.15, d = 0.3

ZVS occurs at a duty ratio of 0.259 for the operating condition of Figure 5.46, which implies a 12.4% improvement in ZVS region compared to that of the square-wave operation. The current waveform of LV side IGBTs C_1 and C_2 was measured using a CWT15 Rogowski current probe and is shown in Figure 5.46. The load voltage, current and inductor current waveforms are portrayed in Figure 5.47. The measured results confirm the converter operation

at a high efficiency of 98.7%, which is 18.2% higher than that of the square-wave mode. Measured results show a 7.6% improvement in average output current and a 21.7% decrease in HV side device switching losses. However, a 6 times increase in LV side device switching loss was observed over that of the square wave mode due to the increased switching current.

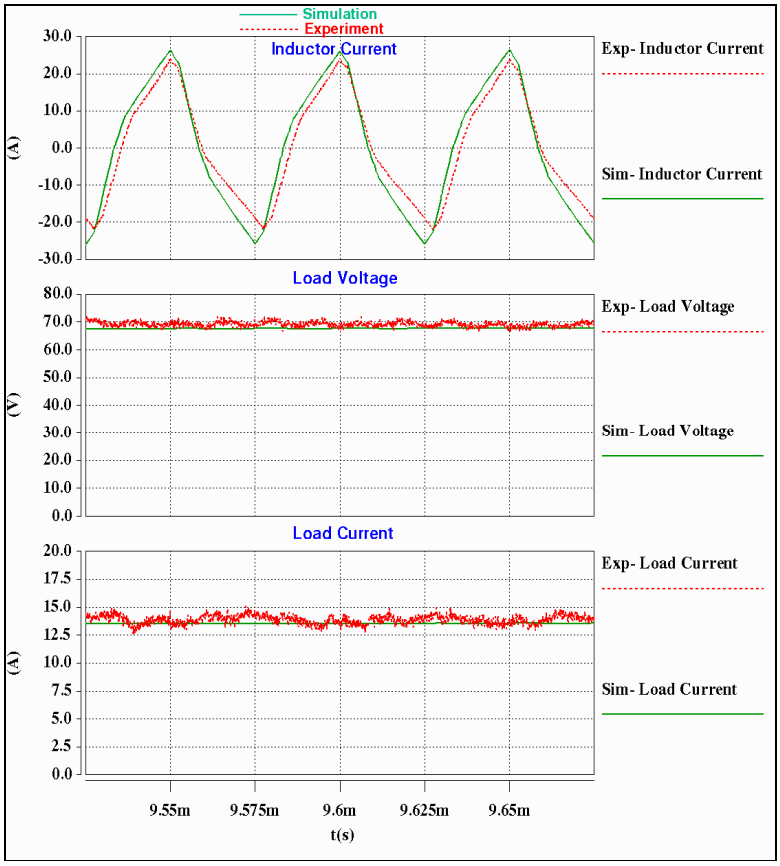


Figure 5.47 Experimental verification of load voltage, current and inductor current waveforms of the DAB converter for quasi-square-wave applied on transformer primary and secondary
V_{in} = 160V, L = 61.2µH, f_S = 20kHz, P_{in} = 1kW, R = 5Ω, V_0 = 71.8V, δ_i = 0.1, δ_0 = 0.15, d = 0.3

5.5 Summary

This Chapter has presented a steady-state analysis of the DAB converter for the quasi-square-wave mode of operation by presenting equations for the RMS, average device currents and RMS, peak inductor/transformer currents. In the steady-state analysis, the effect of introducing dead-time on the transformer voltage was analysed extensively for three cases:

i) quasi-square-wave voltage on transformer primary, square-wave voltage on secondary

ii) quasi-square-wave voltage on transformer secondary, square-wave voltage on primary, and

iii) quasi-square-wave voltages on both transformer primary and secondary

The average and RMS current equations of various devices, and the peak and RMS equations of inductor/transformer currents are derived for the above scenarios. These equations are useful in predicting device losses and losses that occur in the passive components of the DAB converter. With these equations the performance of the converter for any desired value of duty ratio and dead-time can be evaluated. Moreover, these equations will aid design of the converter in terms of selecting suitable power devices and passive components, especially in the choice of filter capacitors. The use of quasi-square-wave voltages extends the soft-switching region of the converter over a wide operating voltage range. A higher power transfer can be achieved under light-load conditions thereby enhancing the converter efficiency at light-loads. The operation of the DAB DC-DC converter has been extensively simulated to confirm the accuracy of the analysis. Experimental results are included to support the analysis for the above three cases, which support the following points:

i) ZVS enhancement is achieved for lower voltage conversion ratios $\left(V_0^{'} < 1\right)$. The experimental results confirm that the converter operates at 91.8% efficiency at 1kW with 17% improvement in the ZVS operating range and 9.7% increase in average output current, when compared to square-wave operation on both sides of the isolation transformer, thereby verifying the converter operation and confirming the accuracy of the analysis.

ii) Higher converter efficiency is obtained under light-loads and the ZVS operating region is enhanced for higher voltage conversion ratios. Proof of concept experimental results at 1kW confirm that the converter operates with 91% efficiency. A 6.8% improvement in average output current was observed over square-wave operation, thereby verifying the converter operation and confirming the analysis.

iii) The measured results confirm that the DAB converter operates with a high efficiency of 97.5% at 1kW for quasi-square-wave voltage operation with $\delta_i = \delta_0 = 0.1$ on both

sides of the transformer, thus improving efficiency and ZVS operating range over the square-wave operation of the DAB converter by 16.8% and 10% respectively. Measurements at different conditions (δ_i = 0.1 and δ_0 =0.15) confirm that the converter operates with an efficiency of about 98%, and with a 12.4% improvement in ZVS operating range.

The quasi-square-wave mode of operation increases RMS and peak currents. Therefore at the design stage there must be a trade-off between conduction and switching losses. Nevertheless, the proposed approach enhances the net power transfer and increases efficiency under light-loads with a reduced dead-time. Hence, the quasi-square-wave mode will be very useful if the converter is to operate under a light-load condition, as it increases the ZVS operating range over a range of voltage conversion ratios whilst increasing power transfer in comparison to the square-wave mode.

Chapter 6

Bidirectional Control of the DAB DC-DC Converter

6.1 Introduction

This chapter presents a novel controller for bidirectional operation of the DAB DC-DC converter and some preliminary investigations are undertaken to show its operation for active control of power flow in both the directions, between the aircraft high voltage DC bus and the energy storage capacitor. The principle of the proposed bidirectional current control technique is described. A SABER simulation model has been developed for the proposed current control technique and the simulations corresponding to a 540V/ 20kW prototype show that the proposed control system exhibits good static and dynamic performance during bidirectional operation. The same technique has been extended to control the quasi-square-wave mode of operation of the DAB converter. The performance of the converter was verified by extensive SABER simulations and the simulation results confirm the mathematical analysis presented in Chapters 2 and 5.

6.2 Proposed bidirectional control strategy

In general, literature dealing with DAB DC-DC converter control predominantly discusses control of the output voltage of the converter [87, 94, 170]. In voltage control, a change in line or load voltage must first be sensed as an output change and then corrected by the feedback loop. This usually results in a slow response [145]. Current control offers the potential benefit of a fast response. This is because, any difference between the input and output voltages will immediately reflect on the inductor current waveform, as its slope is determined by the difference in the line/load voltage changes. In addition, current control also has an inherent current limiting capability as it can instantly clamp potential overcurrents to the required current demand [147].

In order to meet the dynamic power demands of aircraft electric loads using stored energy from the ultracapacitors, and to recharge the ultracapacitors during load regeneration, a high frequency AC link current control is proposed for the DAB DC-DC converter. Variations

in the supply voltage or load voltage will be reflected immediately on the high frequency current waveform, since at all times the difference between input and output voltage appears across the coupling inductor. The basic concept of inductor current control is illustrated in Figure 6.1. FBC1 is the full bridge converter 1 which is connected to the high voltage DC bus and FBC2 is the full bridge converter 2 which is connected to the low voltage ultracapacitor.

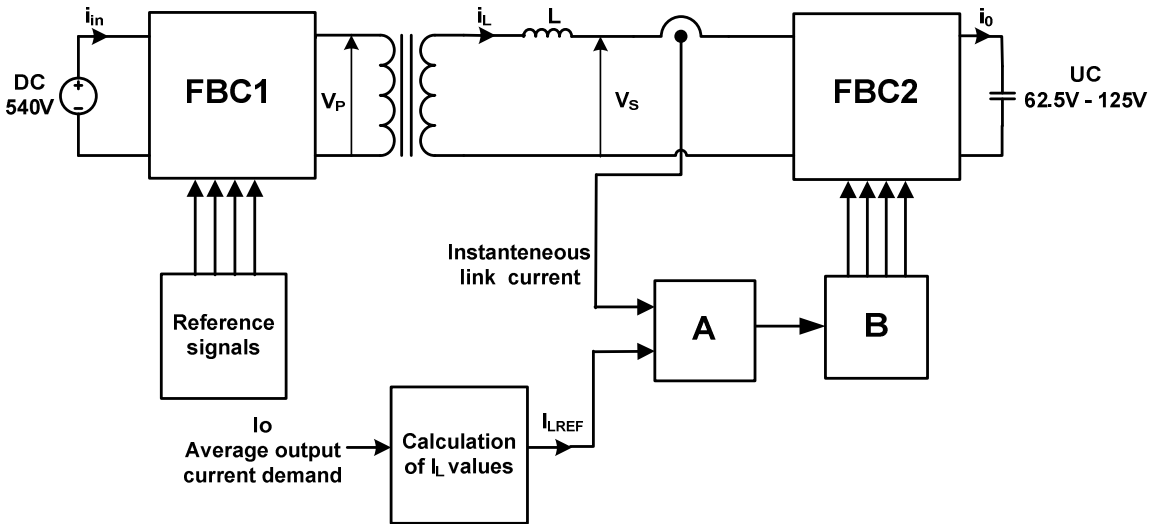


Figure 6.1 Simplified block diagram representation of proposed high frequency current control for the DAB DC-DC converter

The current demand 'I_0', which represents the required average output current, decides the direction and amount of power flow. A positive current demand gives rise to forward power flow that charges the ultracapacitor whereas a negative current demand results in a reverse power flow that discharges the ultracapacitor. From the average current value (using equations (2.8) and (2.3)) the required value of $I_{L,}$ which is here referred to as I_{LREF} is calculated. Block A, shown in Figure 6.1, compares the instantaneous link current i_L with I_{LREF} and produces a square-wave signal, the phase of which informs block B whether the link current is greater than or less than the required value of I_0. Block B phase shifts the gate drives to FBC2 with respect to FBC1 accordingly, to correct the error in link current. Figure 6.2 shows the basic model of block A and block B to perform the function. Block A consists of two comparators, an inverter and an OR gate and block B is composed of a latch.

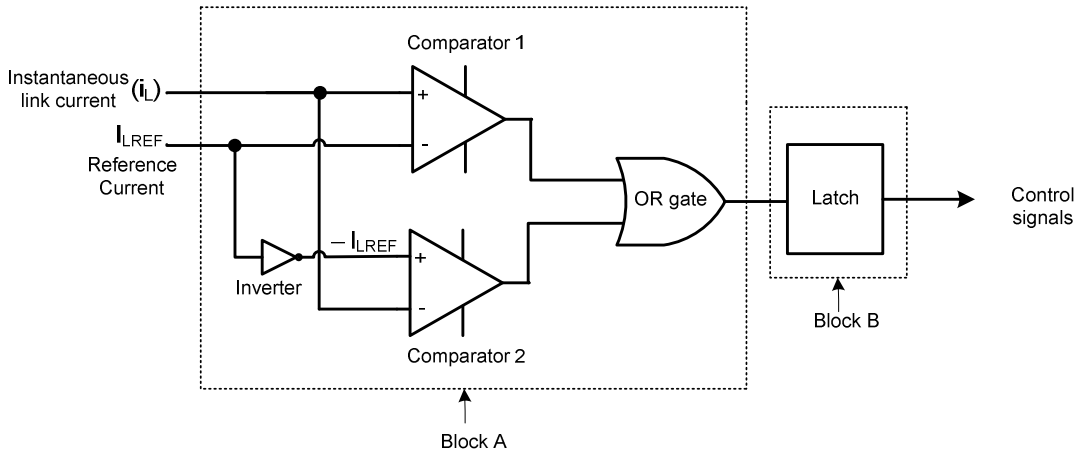


Figure 6.2 Basic model of block A and block B

During the positive half cycle of inductor current, the calculated reference current (I_{LREF}) is compared with the instantaneous link current i_L using comparator 1. When the magnitude of instantaneous link current exceeds the calculated reference current, comparator 1 output goes high. Similarly for the negative half cycle, negative current reference ($-I_{LREF}$) is obtained using an inverter and is compared with the instantaneous link current using comparator 2. When the magnitude of instantaneous link current exceeds the calculated reference current in the negative domain, comparator 2 output goes high. The output of the two comparators are summed using an OR gate and fed to a positive edge triggered latch to generate 20 kHz control signals. Simplified logic waveforms for generating the control signals using block A and block B are illustrated in Figure 6.3 (a) for a nominal I_0, (b) for a high I_0 and (c) for a low I_0. The variation in link current for various values of I_0 and the corresponding variation in the latch output can be seen in Figure 6.3. For a high I_0, the latch output is delayed and thereby the phase shift between the gate signals of FBC1 and FBC2 is increased. For a low I_0, the latch output is advanced and the phase shift between the gate signals of FBC1 and FBC2 is decreased.

Under light load conditions, in order to produce the minimum phase shift, the first peak of the link current goes negative (see Figure 6.3(c)). Hence, the output of the comparators

exceeds the duration of a half cycle. Therefore, in order to limit the width of the pulses, a monostable multivibrator is used to provide pulses of specific width to trigger the latch, preventing instability. This monostable multivibrator is placed between the comparator and the OR gate of Figure 6.2.

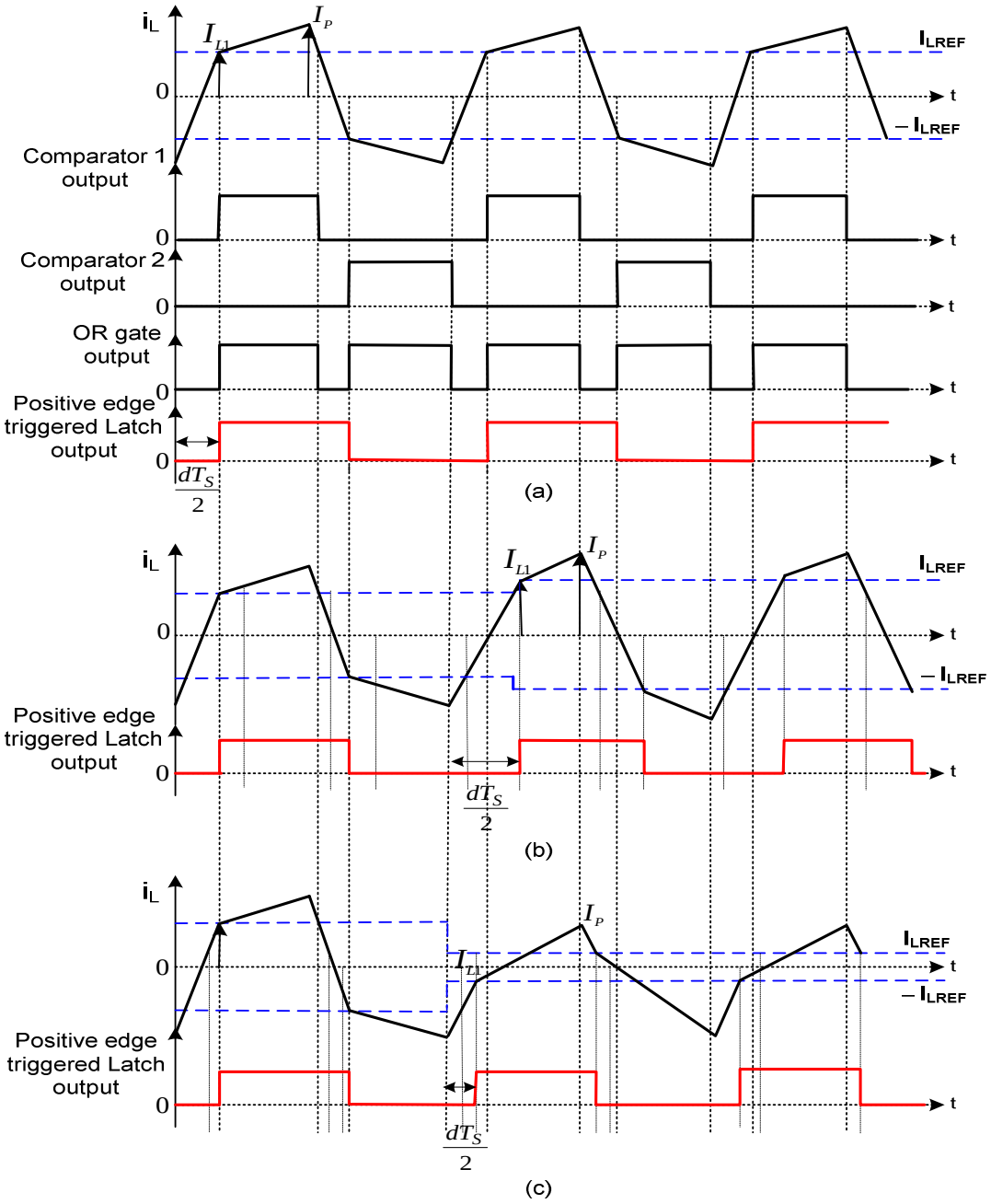


Figure 6.3 Simplified control logic waveforms (a) When I_0 is nominal (b) When I_0 is high (c) When I_0 is low

Figure 6.4 shows a block diagram representation of the proposed current control for bidirectional power transfer. During reverse power flow, the required average output current I_0 is negative; in that case equations (2.20) and (2.15) are used to estimate the values of $I_{LREF.}$ According to the polarity of I_0, a multiplexer determines which of the H-bridges are provided with phase shifted signals for bidirectional power transfer. For example, if power flows from the high voltage side to the low voltage side (forward flow), reference signals are fed to FBC1 and phase shifted control signals are fed to FBC2 using switches activated by the multiplexer. If power flow reverses, the reference signals are fed to FBC2 and phase shifted signals are fed to FBC1.

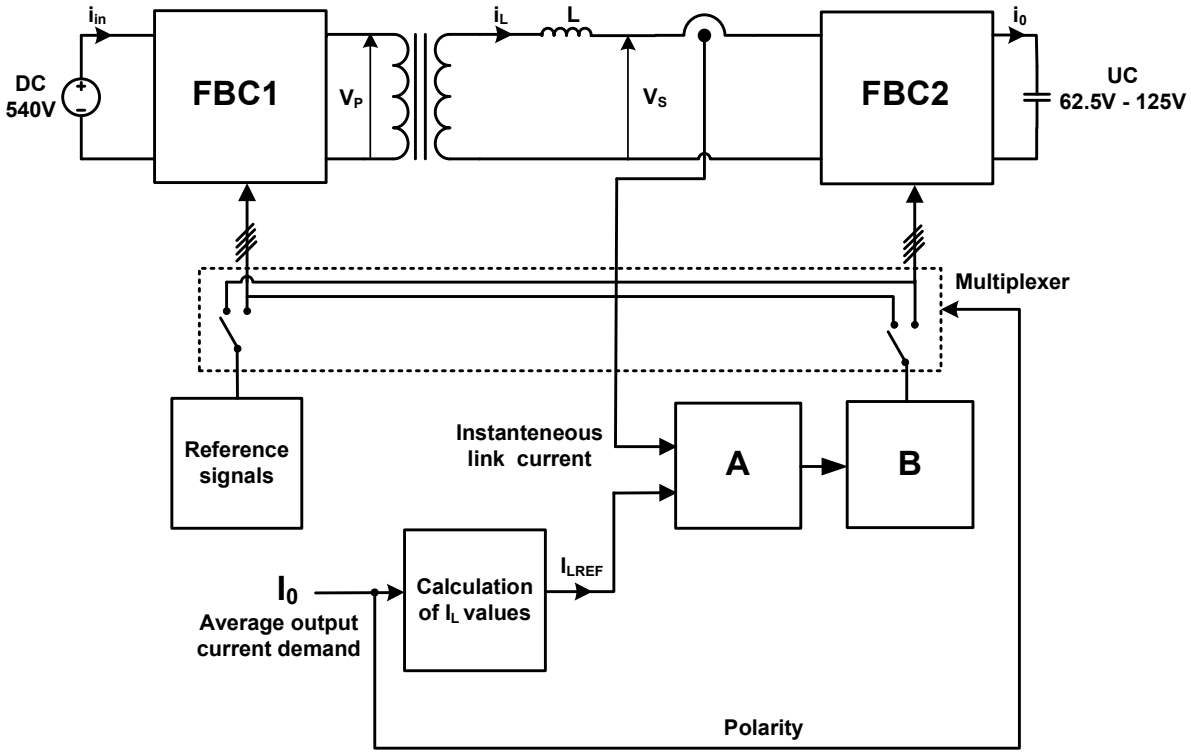


Figure 6.4 Block diagram representation of proposed bidirectional current control for the DAB DC-DC converter

The key AC link waveforms during forward (charging) and reverse (discharging) power transfer modes are depicted in Figure 6.5. The first peak of the link current, which occurs at $dT_s/2$ as shown in Figure 6.5, is considered to be the reference current I_{LREF}. I_{LREF} has different values during forward ($I_{LREF} = I_{L1}$) and reverse ($I_{LREF} = I_P$) power flow. V_P and V_S are

the AC link voltages shown in Figure 6.4. It can be observed from Figure 6.5(a) that $V_{S,}$ the voltage generated by the secondary bridge, lags behind the voltage generated by the primary bridge V_P thereby confirming the forward power flow. During power reversal, V_P lags the voltage V_S and power flows from the ultracapacitor to the high voltage DC bus.

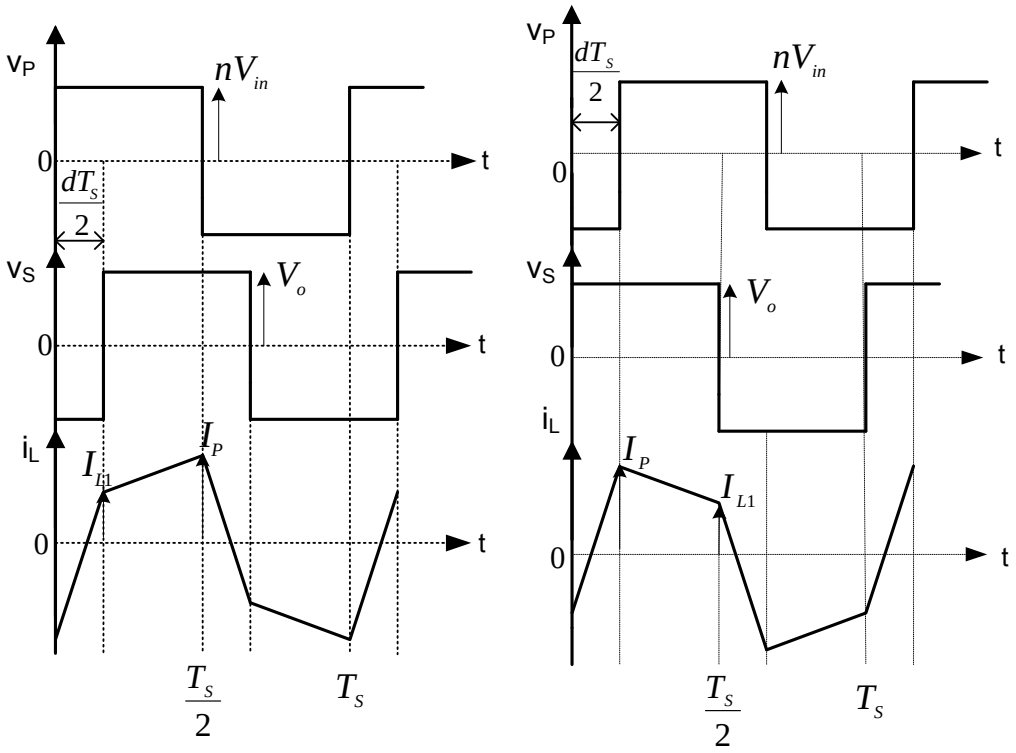


Figure 6.5 Key AC link waveforms during (a) charging mode (b) discharging mode

6.3 SABER simulation model

To accurately simulate the fundamental operation of the converter, switching transitions and transient operation of the DAB converter, circuit simulations were performed using SABER simulation software. The circuit model created using SABER for bidirectional current control of the DAB converter is depicted in Figure 6.6. Ideal switches with an antiparallel diode were used to model the transistor switches of the DAB converter. An ultracapacitor template model from the SABER library was used, but with the specifications of Maxwell's 125V ultracapacitor.

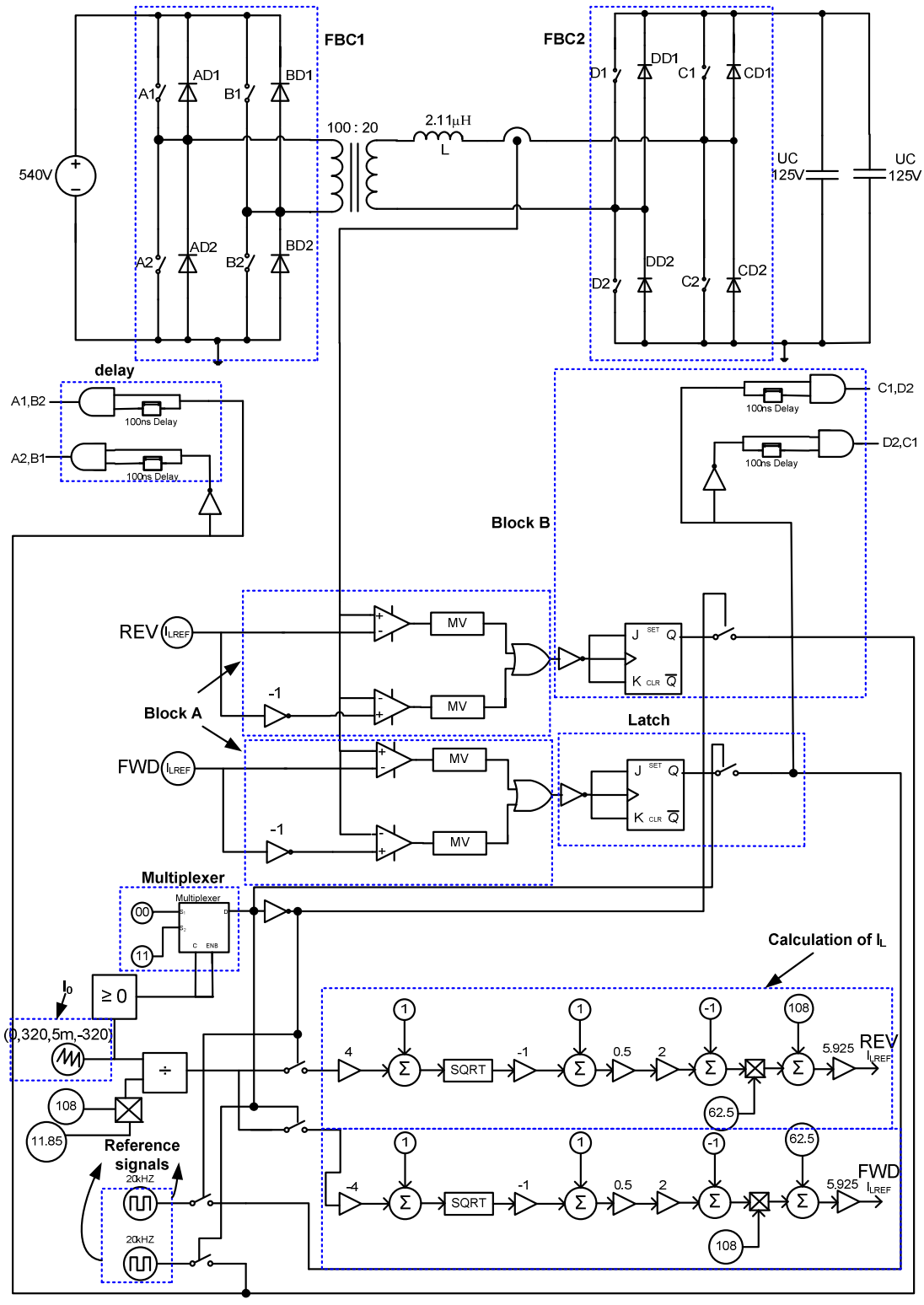


Figure 6.6 SABER simulation schematic for bidirectional power transfer using high frequency current control

The circuit parameters used in the simulations were set to match those of the prototype converter discussed in Chapter 3. The computation of reference current 'I_{LREF}' was performed in SABER using the models available for multiplication/division and/or addition with gain paths for the 'I_0' average current demand input. The various blocks described in section 6.2 are highlighted and named in the SABER model shown in Figure 6.6. Since I_{LREF} has different values during forward and reverse power flow, two sets of blocks (one for forward and another for reverse) were used to produce phase shifted control signals.

The control stage of the simulation model processes information based on the input current demand I_0 and derives the reference current I_{LREF}, which is then compared with the instantaneous link current from the power stage. In a practical system, signal conditioning circuits are used to process the instantaneous link current measured using the sensor from the power stage but these are omitted from the SABER model. According to the current demand polarity, the multiplexer selects the gate signals for the active bridges during forward or reverse power flow. Reference gate signals for the leading bridge are generated using a logic clock. Phase shifted gate signals for the lagging bridge are generated using blocks A and B. When the reference current I_{LREF} equals the instantaneous link current, phase shifted gate signals are fed to the lagging full bridge of the converter in order to maintain the required output current demand. For positive current demand, reference gate signals are fed to FBC1 and phase shifted gate signals are fed to FBC2. During negative current demand, reference gate signals will be provided to FBC2 and shifted gate signals will be supplied to FBC1. Swapping of reference and phase shifted signals, according to the polarity of current demand, is achieved using the multiplexer and switches.

By using the above principle, a further SABER simulation was created for quasi-square-wave operation of the DAB converter. The SABER circuit schematic for bidirectional power flow using the quasi-square-wave mode is shown in Figure 6.7. The SABER simulation described for square-wave AC link voltages is applicable for quasi-square-wave AC link voltages, but with additional inputs of dead-time (δ_i and δ_0). Average output current (I_0) equations derived in Chapter 5 for quasi-square wave mode are non-linear. Due to the computational complexity involved in calculating the reference current I_{LREF} from the

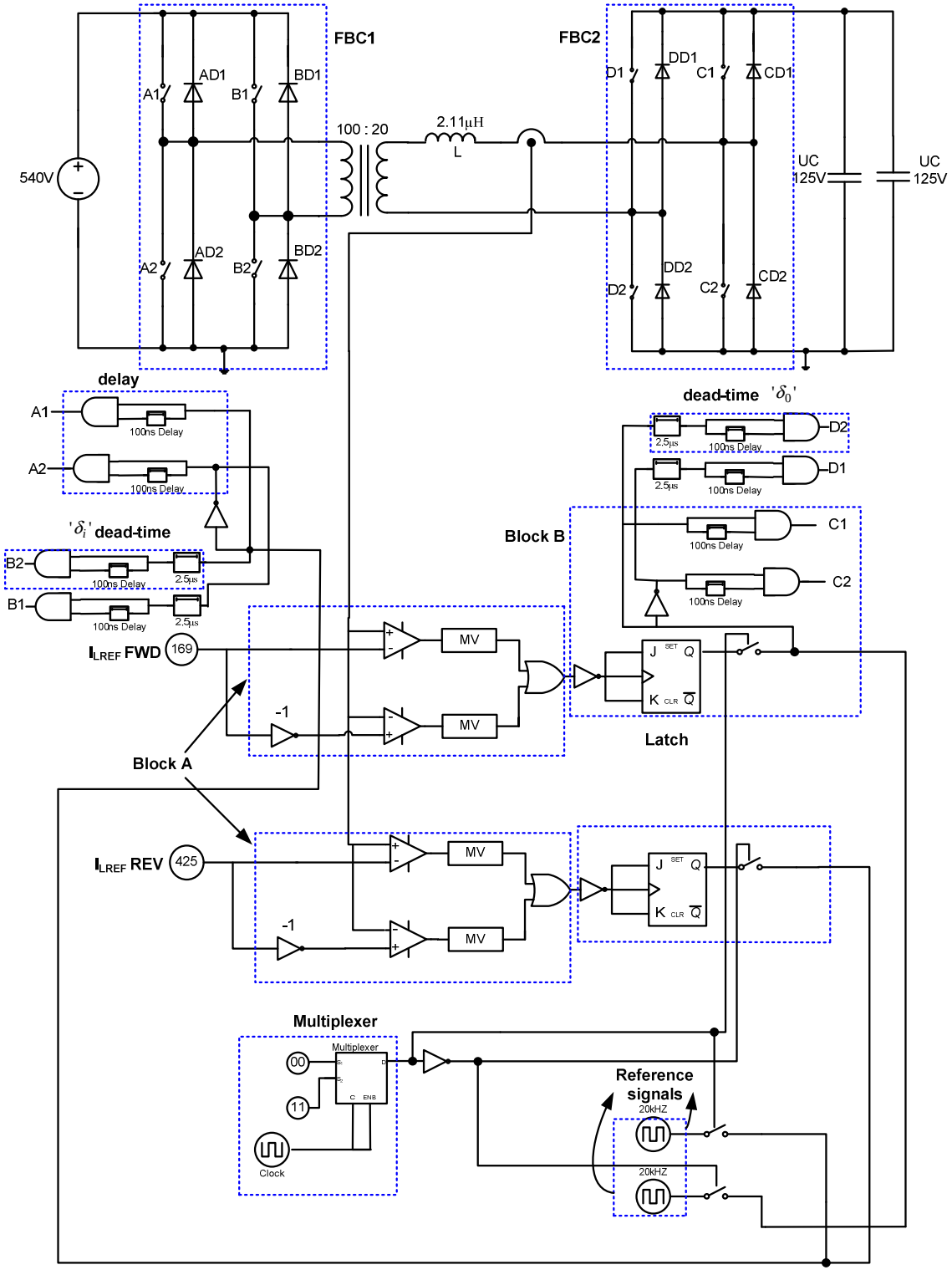


Figure 6.7 SABER simulation schematic for quasi-square-wave operation of DAB converter with bidirectional power transfer using high frequency current control

current demand input I_0 and dead-time inputs (δ_i and δ_0) for the quasi-square-wave mode, I_{LREF} is directly fed to one input of the comparator for the chosen value of dead-time and the other input of the comparator is fed from the instantaneous link current sensor, which is shown in Figure 6.7. The required value of dead-time (δ_i and/or δ_0) can be set in the delay element model of SABER.

6.4 Simulation results of proposed control for square-wave mode of operation

Detailed simulation results corresponding to the proposed control strategy for square-wave operation of the DAB converter are presented in this section.

6.4.1 Performance of control system during steady-state operation

The fundamental operation of the converter was verified by the SABER model for charging and discharging modes. Time domain results from the SABER simulation are illustrated in Figure 6.8 for charging mode and Figure 6.9 for discharging mode of the ultracapacitor. These Figures show the inductor current, voltage generated by the two active bridges, HV side and LV side transistor and diode currents, source side terminal current and ultracapacitor side terminal current for 20kW power transfer. Figure 6.8 shows the simulated response for charging mode. It is apparent from Figure 6.8 that the ultracapacitor current is positive and power transfer takes place from the source 540V (which represents the aircraft DC bus) to the ultracapacitor. This shows that the ultracapacitor modules are charging and devices on the HV side perform inverter operation and devices on the LV side perform rectification. This verifies the theory and confirms the values obtained through steady-state analysis, presented in Chapter 2 of this Thesis. Figure 6.9 shows that the ultracapacitor side terminal current is negative and power flow takes place from the ultracapacitor modules to the DC link. This process discharges the ultracapacitor and devices on the HV side perform rectification and devices on the LV side perform inversion. This can be clearly seen from the device waveforms shown in Figure 6.9. Thus the SABER simulations verify the performance of the proposed control technique during steady-state operation.

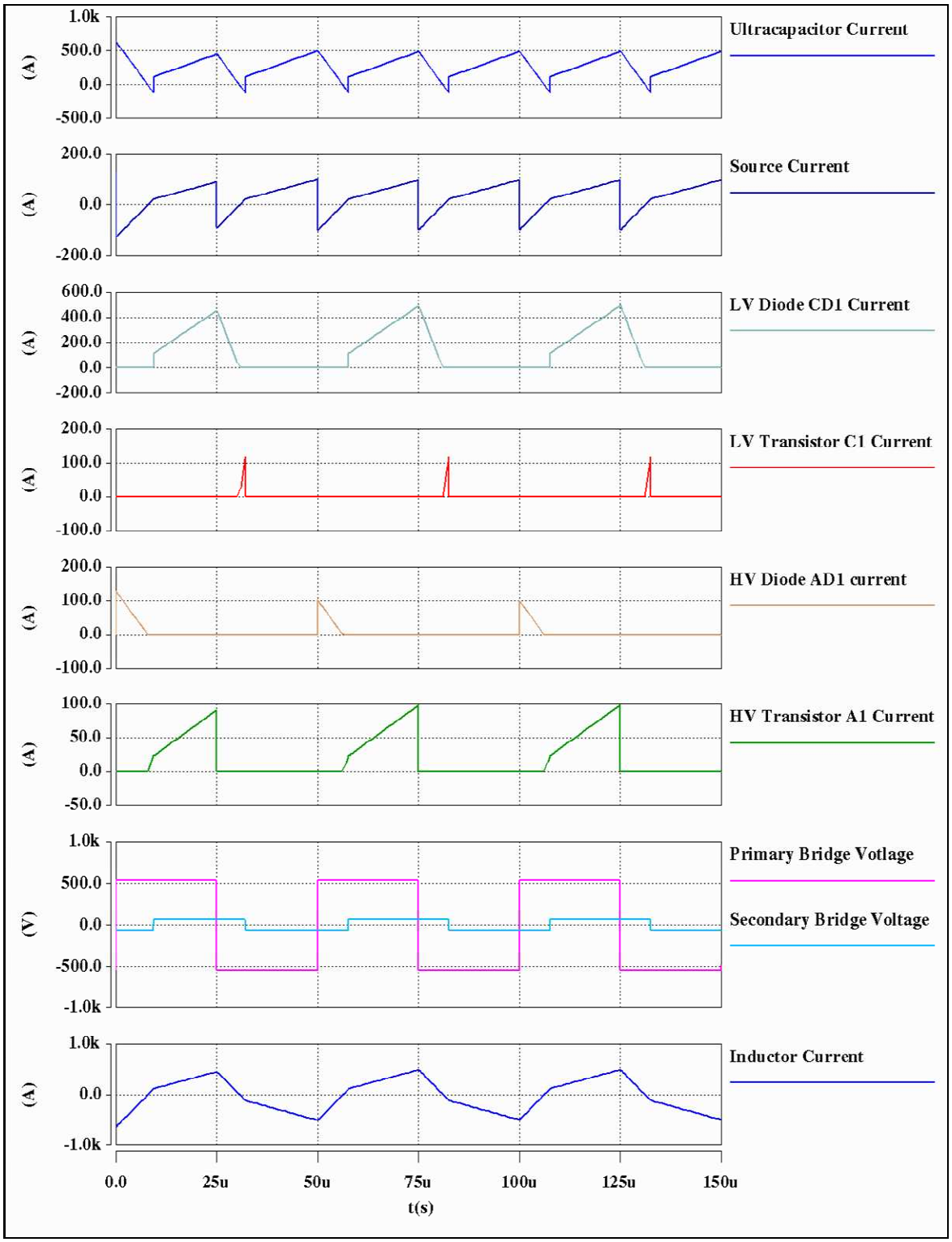


Figure 6.8 Performance of control system during steady-state operation for charging mode of the ultracapacitor
V_{in} = 540V, V_0 = 62.5V, d = 0.5, P_0 = 20kW, I_0 = 320A, f_s = 20kHz, L = 2.109µH

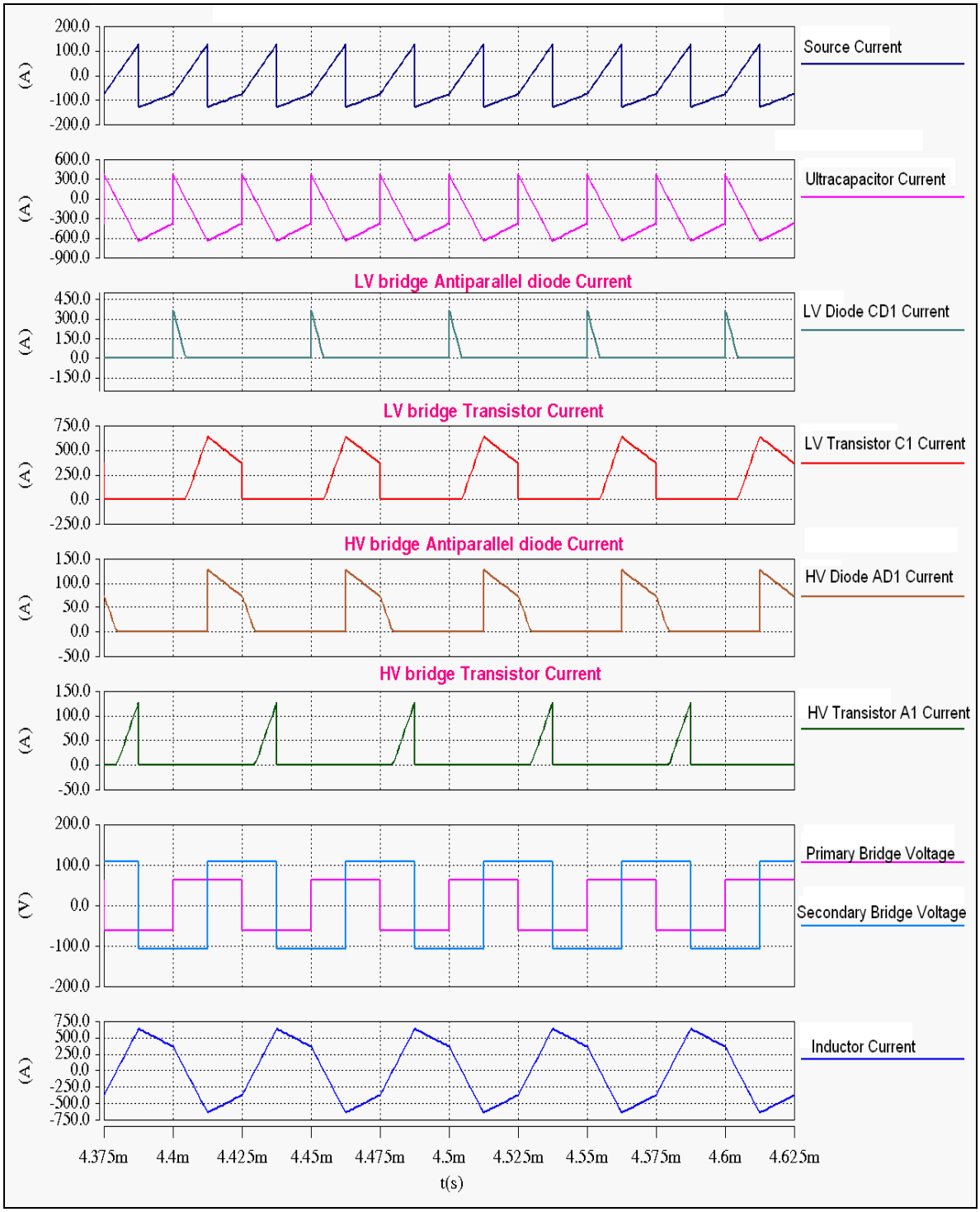


Figure 6.9 Performance of control system during steady-state operation
for discharging mode of the ultracapacitor
V_{in} = 540V, V_0 = 62.5V, d = 0.5, P_0 = 20kW, I_0 = -320A, f_s = 20kHz, L = 2.109µH

6.4.2 Evaluation of control system during transients

To demonstrate the dynamic performance of the proposed control system, SABER simulations were repeated for a series of current and voltage transients. Figures 6.10 and 6.11 depict the time domain transient results. Figure 6.10 shows the response of the control system for a consecutive variation in current demand, typical of real time aircraft electric loads [237]. It depicts a sudden change in current demand from +320A to -230A at 5ms and a momentary increase in the current demand in the reverse direction from -230A to -300A at 5.2ms. Figure 6.11 shows the response of the control system for successive variations in source voltage, portraying a decrease in supply voltage from 540V to 320V at 5.45ms and an increase in supply voltage from 320V to 450V at 5.15ms. Simulation results confirm that the system is stable and the proposed control works well under transients. An example of bidirectional power transfer operation is depicted in Figures 6.12 and 6.13. The ultracapacitor module delivers power to the source and thereby the converter operates in discharging mode until 5ms. At 5ms, the current demand reverses and as a result the control system provides leading

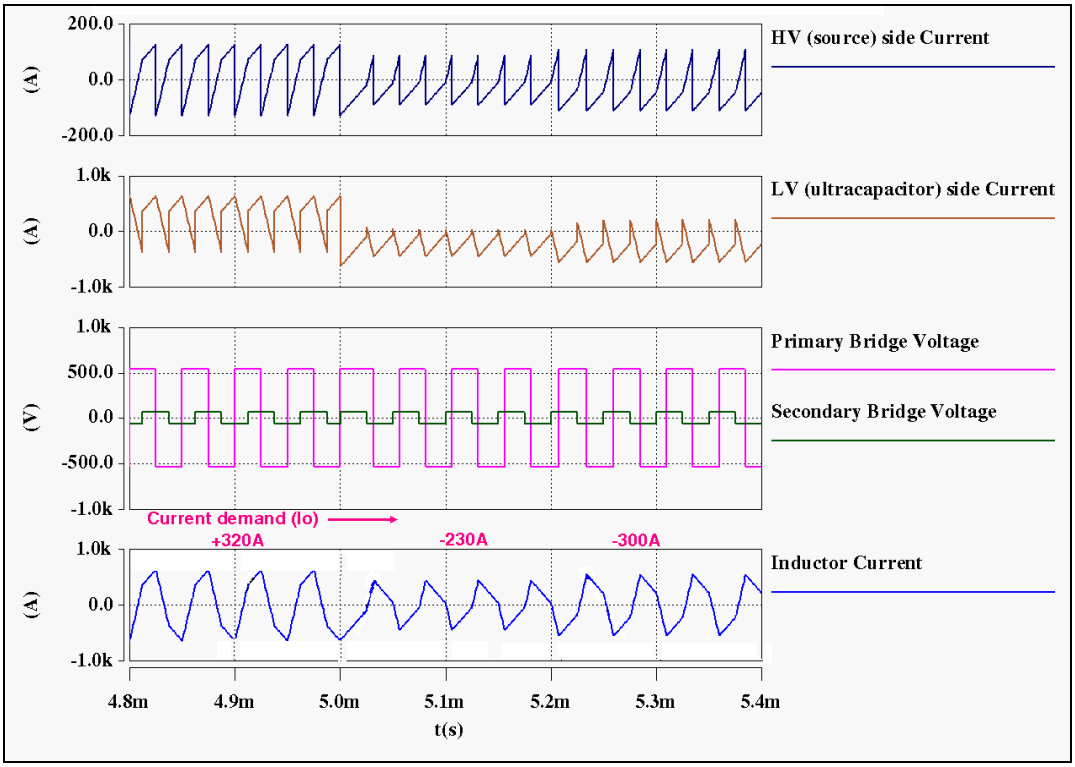


Figure 6.10 Evaluation of control system during current transients from +320A to -230A at 5ms and from -230A to -300A at 5.2ms
V_{in} = 540V, V_0 = 62.5V, f_s = 20kHz, L = 2.109µH, n = 1:0.2

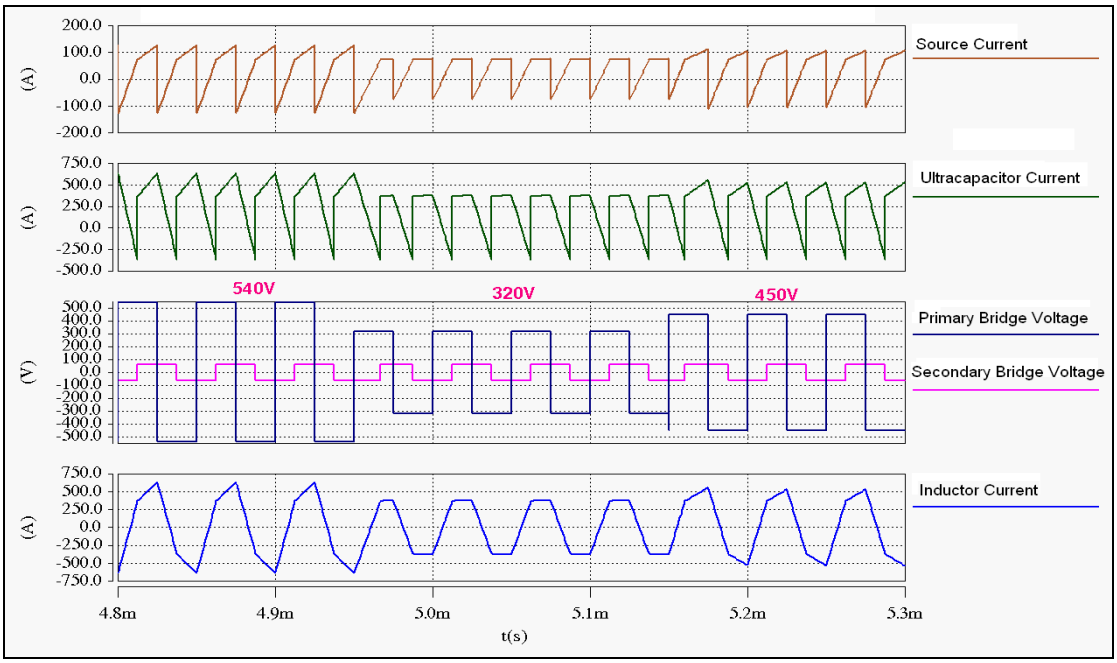


Figure 6.11 Evaluation of control system during voltage transients from 540V to 320V at 4.95ms and from 320V to 450V at 5.15ms

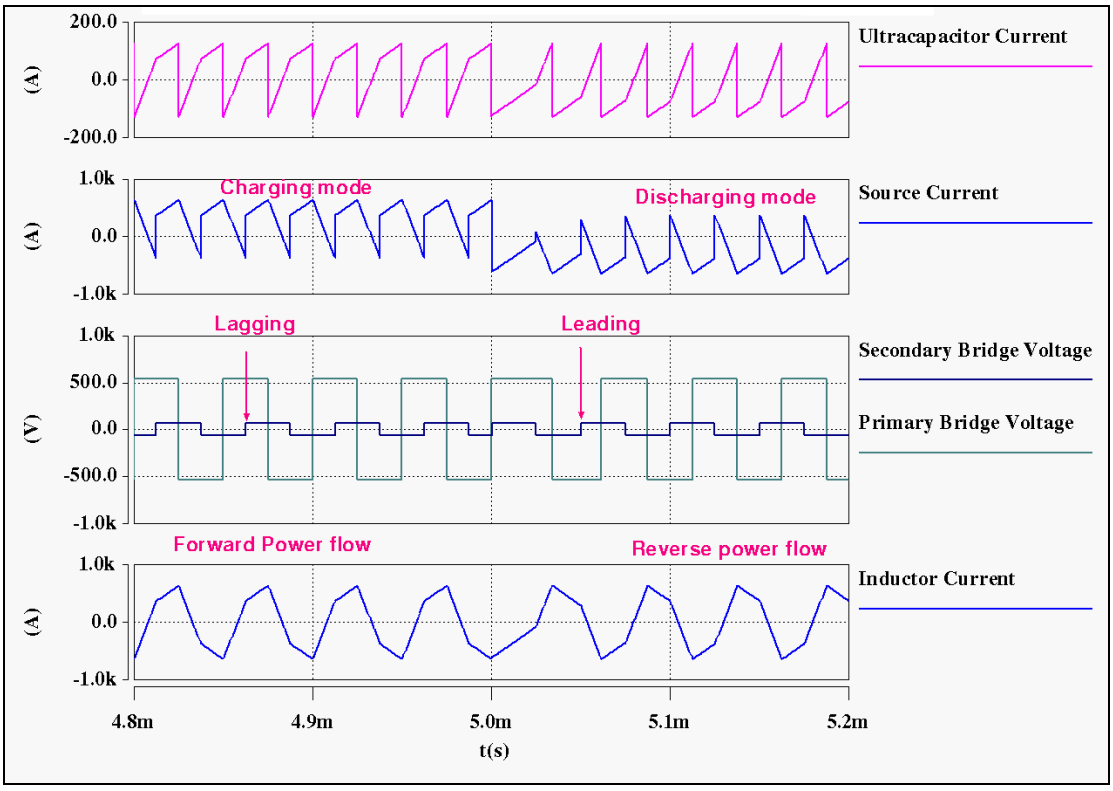


Figure 6.12 Evaluation of control system during bidirectional power flow showing key waveforms V_{in} = 540V, V_0 = 62.5V, d = +/- 0.5, P_0 = 20kW, I_0 =+/ -320A, f_s = 20kHz, L = 2.109µH, n = 1:0.2

signals to the HV side bridge and lagging signals to the LV side bridge, thereby charging the ultracapacitor modules. Figure 6.13 shows waveforms of the DAB converter during a change of current flow direction. The transient current occurring during the power reversal is well within limits, which once again shows the performance of the proposed control strategy.

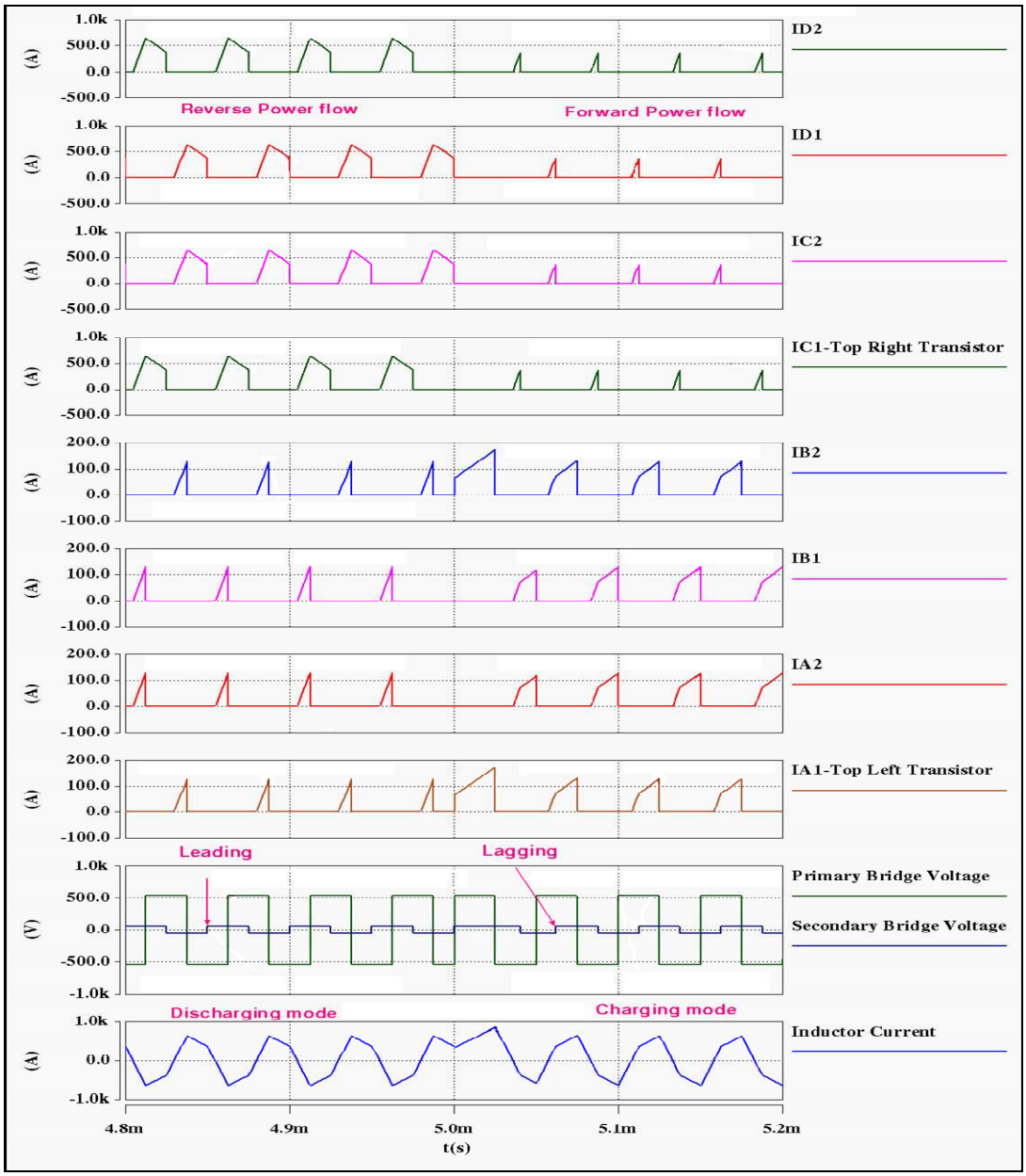


Figure 6.13 Evaluation of control system during bidirectional power transfer showing DAB converter waveforms
V_{in} = 540V, V_0 = 62.5V, d = +/- 0.5, P_0 = 20kW, I_0 = +/-320A, f_s = 20kHz, L = 2.109µH, n = 1:0.2

6.4.3 Confirmation of simulation results with mathematical analysis

To validate the performance of the control system at various voltage conversion ratios, SABER simulation results were compared with theoretical results obtained from the analysis presented in Chapter 2. Figure 6.14 illustrates the performance of the converter during forward power flow for different voltage conversion ratios (0.2 to 5) and plots normalised average output current against normalised reference current. There is a close agreement between the simulation (marked as 'x') and calculated (solid line) values. ZVS boundaries obtained from simulation as well as steady-state analysis for buck and boost modes are also included. It can be observed from Figure 6.14 that ZVS is achieved over the full control range for a unity voltage conversion ratio. The ZVS region reduces as the voltage conversion ratio decreases below or increases beyond unity. The operating region within the V curve of the ZVS boundary represents the soft switching region of the converter.

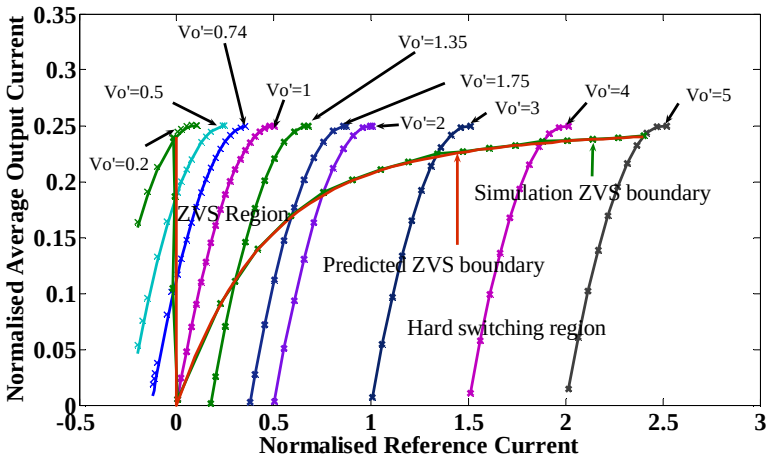


Figure 6.14 Normalised average output current vs normalised reference current for voltage conversion range (Vo' = 0.2 to 5); x = simulated, solid line = calculated

6.5 Simulation results of proposed control for quasi-square-wave operation

This section presents detailed simulation results for steady-state and transient performance of the proposed control technique applied to quasi-square-wave operation on the transformer primary alone, quasi-square-wave operation on the transformer secondary alone and quasi-square-wave operation applied simultaneously to both transformer primary and secondary. In

the following discussions, the HV side is referred to as the transformer primary and the LV side is referred to as the transformer secondary.

6.5.1 Proposed control applied to quasi-square-wave mode on transformer primary only

In this section, steady-state and transient performance of the DAB converter controller are examined with a quasi-square-wave on the transformer primary, retaining a square-wave on the transformer secondary, using SABER simulations. Dead-time and reference current are the two inputs to the SABER model.

6.5.1.1 Steady-state performance of control system

Figures 6.15 and 6.16 depict the steady-state waveforms of the DAB converter for charging and discharging modes. From these figures, the charging and discharging current of the ultracapacitor can be clearly seen for the given input of $\delta = 0.2$ and $d = 0.3$.

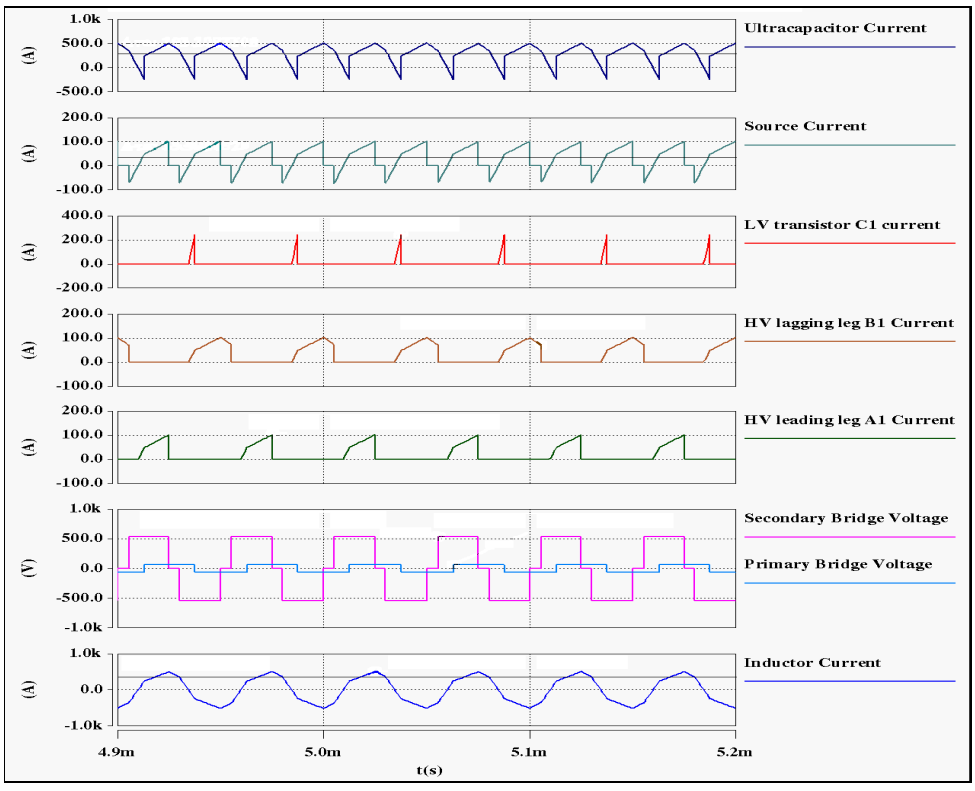


Figure 6.15 Performance of control system during steady-state operation for charging mode of ultracapacitor with quasi-square-wave on transformer primary $V_{in} = 540V$, $V_0 = 62.5V$, d = 0.3, δ = 0.2, $P_0 = 18.4kW$, $I_0 = 294A$, $f_s = 20kHz$, $L = 2.109\mu H$

Simulation results confirm that the SABER model behaves well in steady-state.

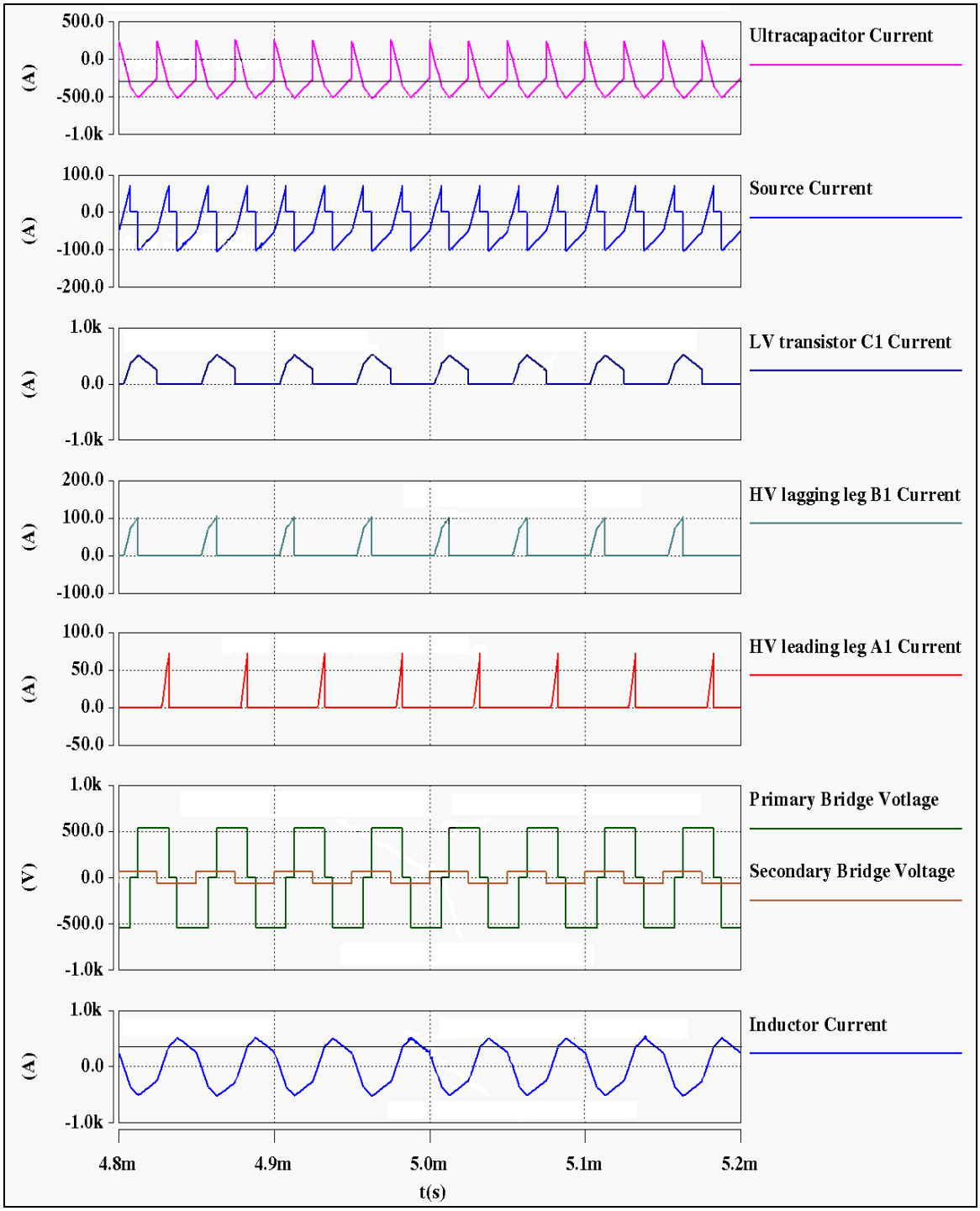


Figure 6.16 Performance of control system during steady-state operation for discharging mode of ultracapacitor with quasi-square-wave on transformer primary V_{in} = 540V, V_0 = 62.5V, d = 0.3, δ = 0.2, P_0 = 18.4kW, I_0 = -294A, f_s = 20kHz, L = 2.109µH

6.5.1.2 Evaluation of control system during transients

The performance of the proposed control technique was evaluated for current and voltage transients. Figures 6.17 and 6.18 portray the DAB converter performance for current and voltage transients. Current transients occur at 5.8ms as shown in Figure 6.17, and are caused by a step change in reference current from 150A to 300A (forward power transfer) and again at 6ms, from 300A to 360A (reverse power flow). The control system smoothly handles the power transfer during the step increase and during the changeover from forward to reverse directions. This once again verifies the functionality of the proposed control.

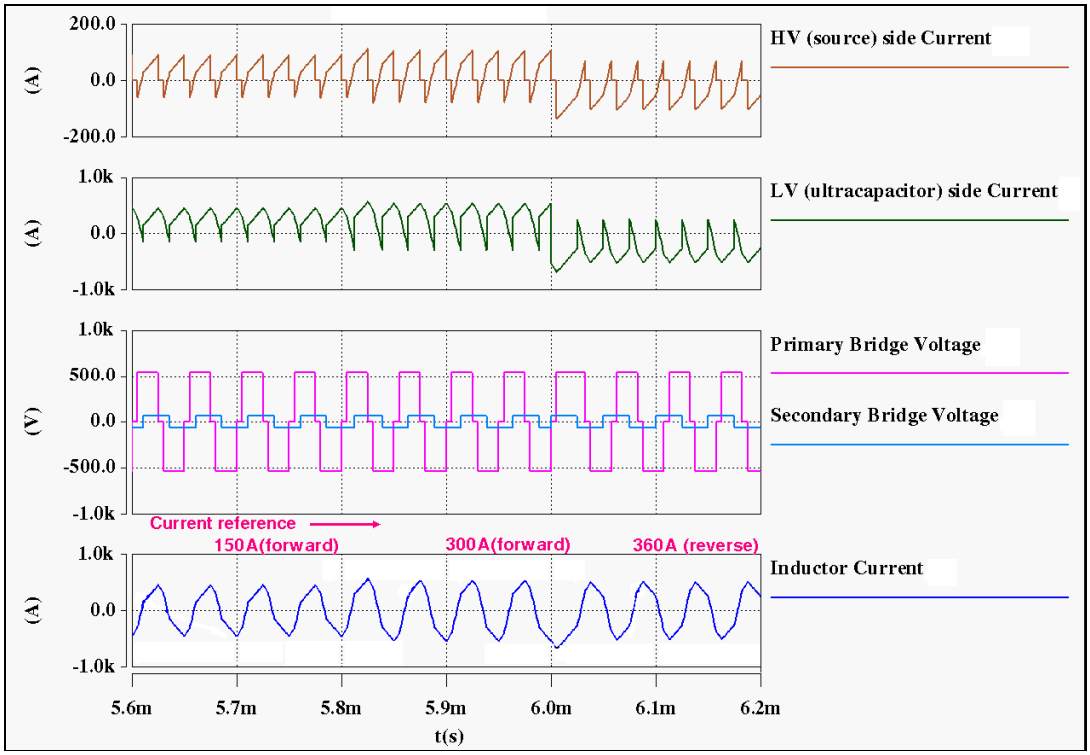


Figure 6.17 Evaluation of control system during current transients from 150A to 300A at 5.8ms and 300A to 360A at 6ms with quasi-square-wave on transformer primary
V_{in} = 540V, V_0 = 62.5V, δ = 0.2, P_0 = 20kW, f_s = 20kHz, L = 2.109μH

A series of input voltage transients were given to the control system to observe its response. Voltage transient-1 from 540V to 270V was given at 3.5ms and then a further transient (transient-2) from 270V to 540V was given at 3.75ms to mimic typical transients in an aircraft. These can be observed in Figure 6.18. The change in input voltage is reflected in the inductor current waveform very rapidly. The waveforms of Figure 6.18 show that the system is stable.

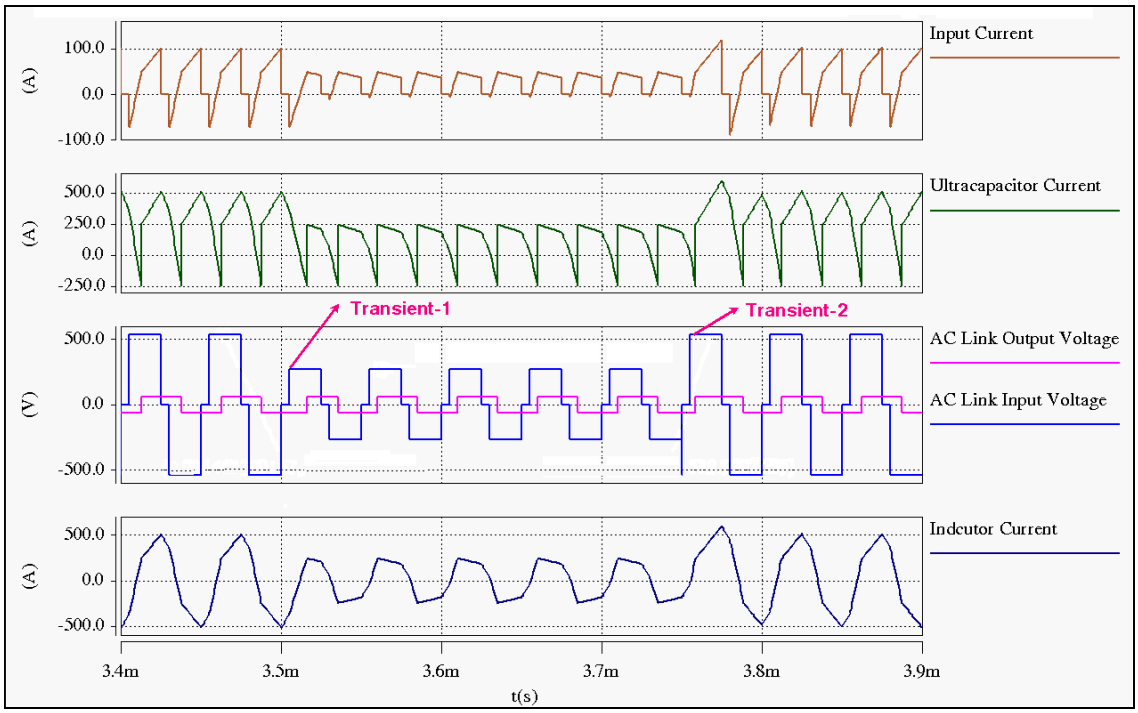


Figure 6.18 Evaluation of control system during voltage transients from 540V to 270V at 3.5ms and from 270V to 540V at 3.75ms with quasi-square-wave on transformer primary
V_0 = 62.5V, δ = 0.2, d = 0.3, f_s = 20kHz, L = 2.109µH, n = 1: 0.2

Figure 6.19 depicts the converter waveforms during a reversal of power transfer. Initially the system charges the ultracapacitor and power flow takes place from source to the energy storage system. At 5ms, the power flow is reversed so as to subsequently discharge the ultracapacitor. It can be observed from Figure 6.19 that the quasi-square-wave voltage was leading the square-wave voltage during forward power flow and after 5ms, the quasi-square-wave voltage lags the square-wave voltage indicating reverse power transfer. Charging and discharging currents of the ultracapacitor can be clearly seen during this transient. For quasi-square-wave operation, leading-leg transistors (A_1, A_2) and diodes (A_{D1}, A_{D2}) exhibit similar current waveforms and lagging-leg transistors (B_1, B_2) and diodes (B_{D1}, B_{D2}) exhibit similar current waveforms. For square-wave operation, the current waveforms of all the transistors/diodes in a full bridge are similar. Therefore, leading-leg transistor (I_{A1}) and diode (I_{AD1}) currents, and lagging-leg transistor (I_{B1}) and diode (I_{BD1}) currents, which produce the quasi-square-wave voltage on the primary, and transistor (I_{C1}), diode current (I_{CD1}) which produce the square-wave on the secondary side are also included in Figure 6.19, to show the variation in device currents as a result of power reversal. The controller was able to cope with

the fast variation in power transfer. A current transient introduced as a result of power reversal is well within the limit and can be clearly seen in Figure 6.19. These waveforms once again confirm the suitability of the proposed control for improved performance in aerospace applications.

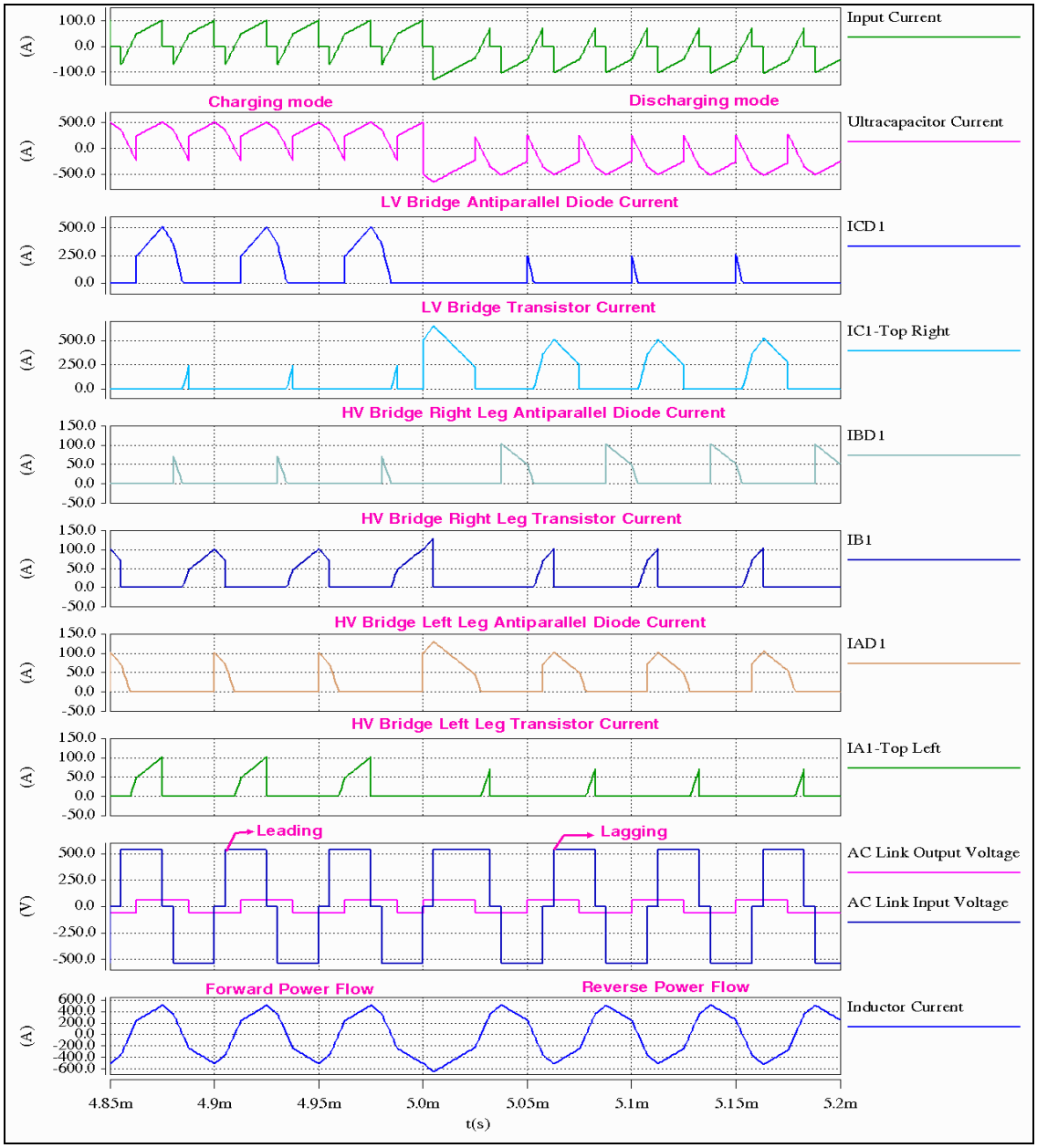


Figure 6.19 Evaluation of control system during bidirectional power transfer showing DAB converter waveforms with quasi-square-wave on transformer primary
V_{in} = 540V, V_0 = 62.5V, d = +/- 0.3, δ = 0.2, P_0 = 18.4kW, f_s = 20kHz, L = 2.109µH

6.5.1.3 Confirmation of simulation results with mathematical analysis

To examine the performance of the control system over a wide operating voltage range, simulations were repeated for various voltage conversion ratios. The waveform analysis presented in Chapter 5 was used to obtain the curves, which depict the performance of the DAB converter. Figure 6.20 shows the curves of the DAB converter for voltage conversion ratios ranging from 0.2 to 5 as 'd' varies from 0 to 0.5. The simulation results are highlighted in '*' and the values obtained from the mathematical analysis are represented using solid lines. Figure 6.20 depicts normalised average output current against normalised reference current during forward power transfer. In order to mark the ZVS boundaries, the duty ratio at which ZVS occurs was obtained from analysis. The normalised reference currents and normalised output currents for the corresponding duty ratio were then calculated. The ZVS boundaries for the buck and boost modes are shown in red and dark green lines respectively in Figure 6.20 for various values of dead-time ($\delta \rightarrow 0$ to 0.3). The figure below gives an insight into how dead-time and reference current variations influence ZVS. It is evident from Figure 6.20 that as dead-time varies from 0 to 0.3, the maximum power throughput decreases. This can be observed from the blue, pink and light green curves. However, at a higher voltage conversion ratio (e.g. $V_0' > 3$, $\delta = 0.3$), the ZVS operating region is improved when compared with square-wave mode as can be seen in Figure 6.20. The curve for $\delta = 0$ depicts the performance of the converter under square-wave mode of operation.

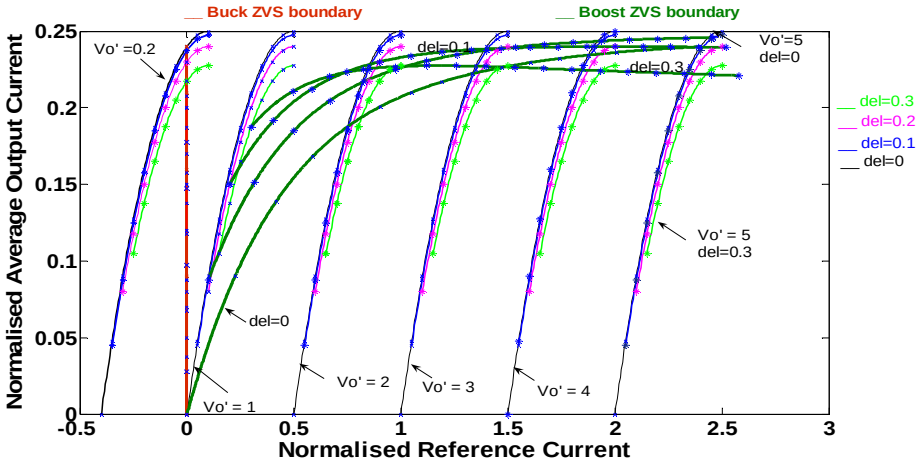


Figure 6.20 Normalised average output current vs normalised reference current for voltage conversion range (Vo' = 0.2 to 5) with quasi-square-wave on transformer primary; * = Simulation, Solid line = Mathematical analysis

6.5.2 Proposed control applied to quasi-square-wave on transformer secondary

This section investigates the converter controller performance under steady-state and transient conditions with a quasi-square-wave voltage on the transformer secondary whilst retaining a square-wave voltage on the transformer primary.

6.5.2.1 Steady-state performance of control system

The steady-state performance of the converter with the proposed control during charging and discharging modes is illustrated in Figures 6.21 and 6.22 respectively. Inductor current,

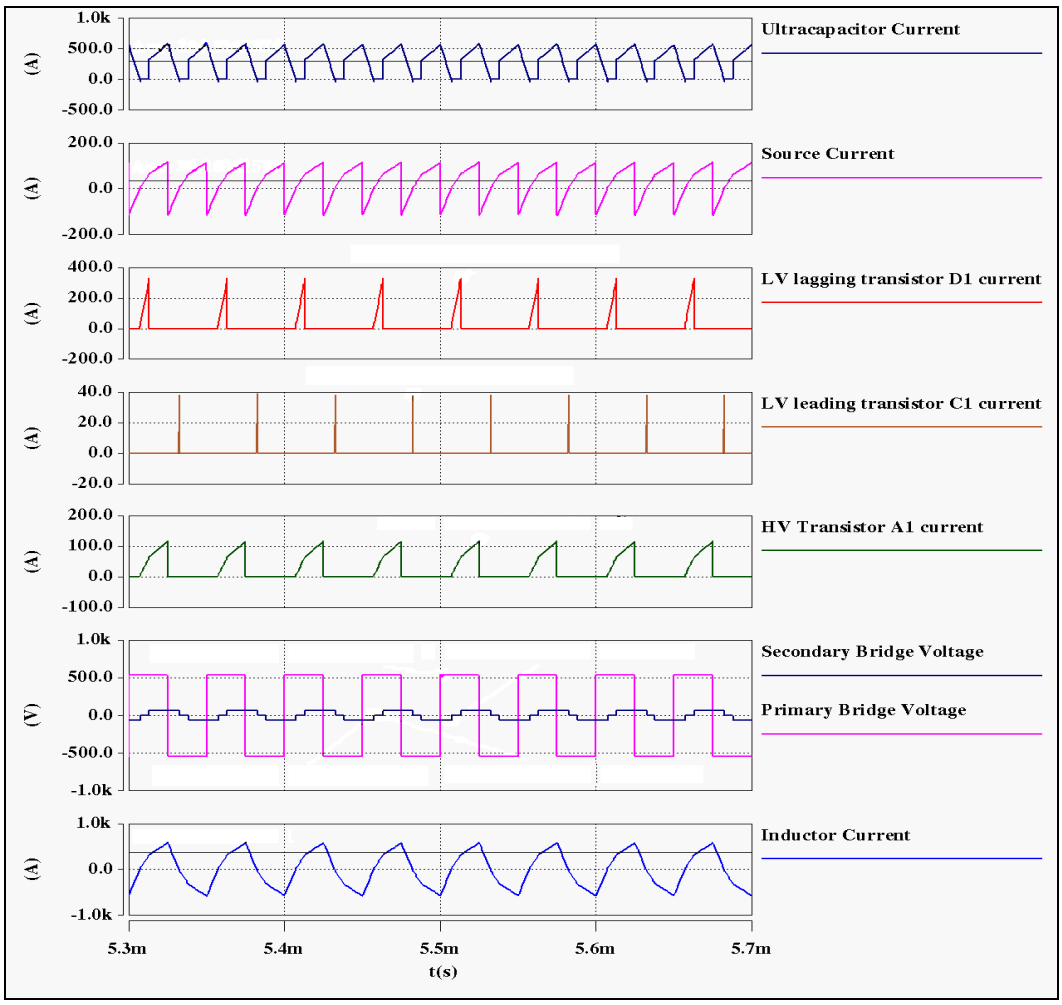


Figure 6.21 Performance of control system during steady-state operation for charging mode of ultracapacitor with quasi-square-wave on transformer secondary V_{in} = 540V, V_0 = 62.5V, d = 0.3, δ = 0.2, P_0 = 18.4kW, I_0 = 294A, f_s = 20 kHz, L = 2.109μH, n = 1: 0.2

voltage generated by the two full bridges, transistor and diode currents on the HV and LV sides, source current and ultracapacitor current waveforms are displayed for a dead-time of $\delta = 0.2$. Waveforms are without glitches confirming the robustness of the controller in ensuring the steady-state operation of the DAB converter. Ultracapacitor charging and discharging currents are evident from those figures.

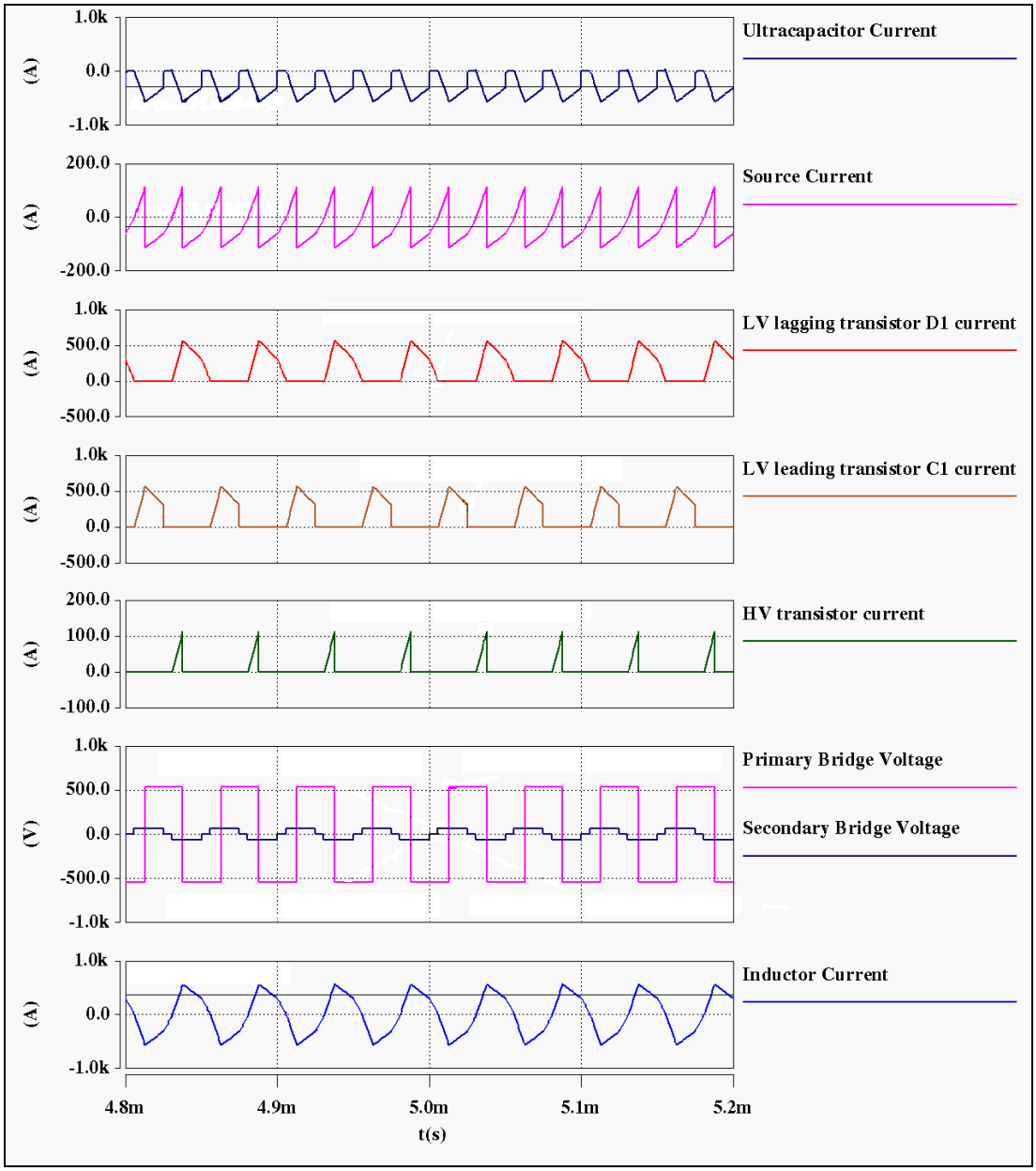


Figure 6.22 Performance of control system during steady-state operation for discharging mode of ultracapacitor with quasi-square-wave on transformer secondary
V_{in} = 540V, V_0 = 62.5V, d = 0.3, δ = 0.2, P_0 = 18.4kW, I_0 = -294A, f_s = 20kHz, L = 2.109µH, n =1: 0.2

6.5.2.2 Evaluation of control system during transients

Time domain transient results from the SABER simulator for current and voltage transients are depicted in Figures 6.23 and 6.24 respectively. A reference current step change occurs from 50A to 200A at 4.85ms (forward power flow) and from 200A to 566A at 5ms (power reversal) as shown in Figure 6.23.

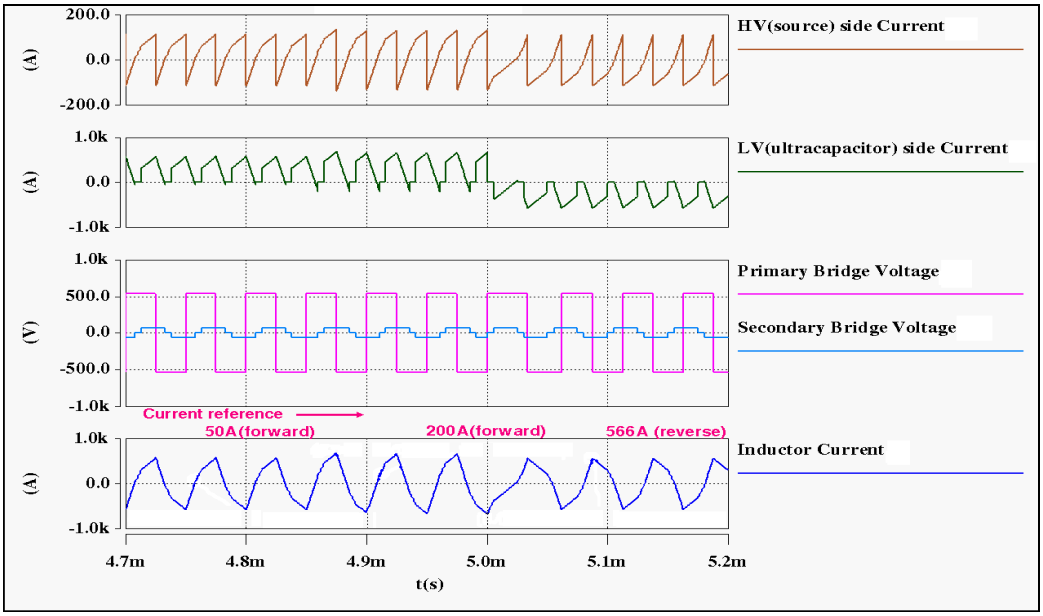


Figure 6.23 Evaluation of control system during current transients from 50A to 200A at 4.85ms and 200A to 566A at 5ms with quasi-square-wave on transformer secondary
V_{in} = 540V, V_0 = 62.5V, δ = 0.2, f_s = 20kHz, L = 2.109µH, n =1: 0.2

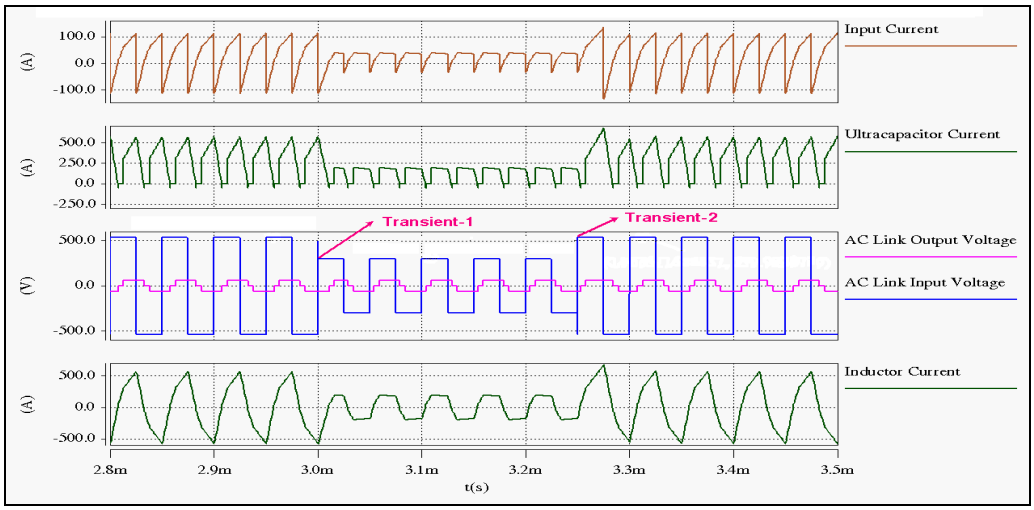


Figure 6.24 Evaluation of control system during voltage transients from 540V to 300V at 3ms and from 300V to 540V at 3.25ms with quasi-square-wave on transformer secondary
V_0 = 62.5V, d = 0.3, δ = 0.2, f_s = 20kHz, L = 2.109µH, n =1: 0.2

Smooth transitions from 50A to 200A and from 200A to 566A are apparent from the waveforms shown in Figure 6.23. The results confirm that the control system works well under transients. In Figure 6.24, an input voltage change from 540V to 300V occurred at 3ms and subsequently another change occurred at 3.25ms from 300V to 540V. The variation in the input voltage was reflected on the inductor current waveform during these transients. The waveforms shown in Figure 6.24 once again confirm that the proposed controller exhibits good performance under transients. Figure 6.25 depicts the converter performance with the proposed control during a reversal of power flow.

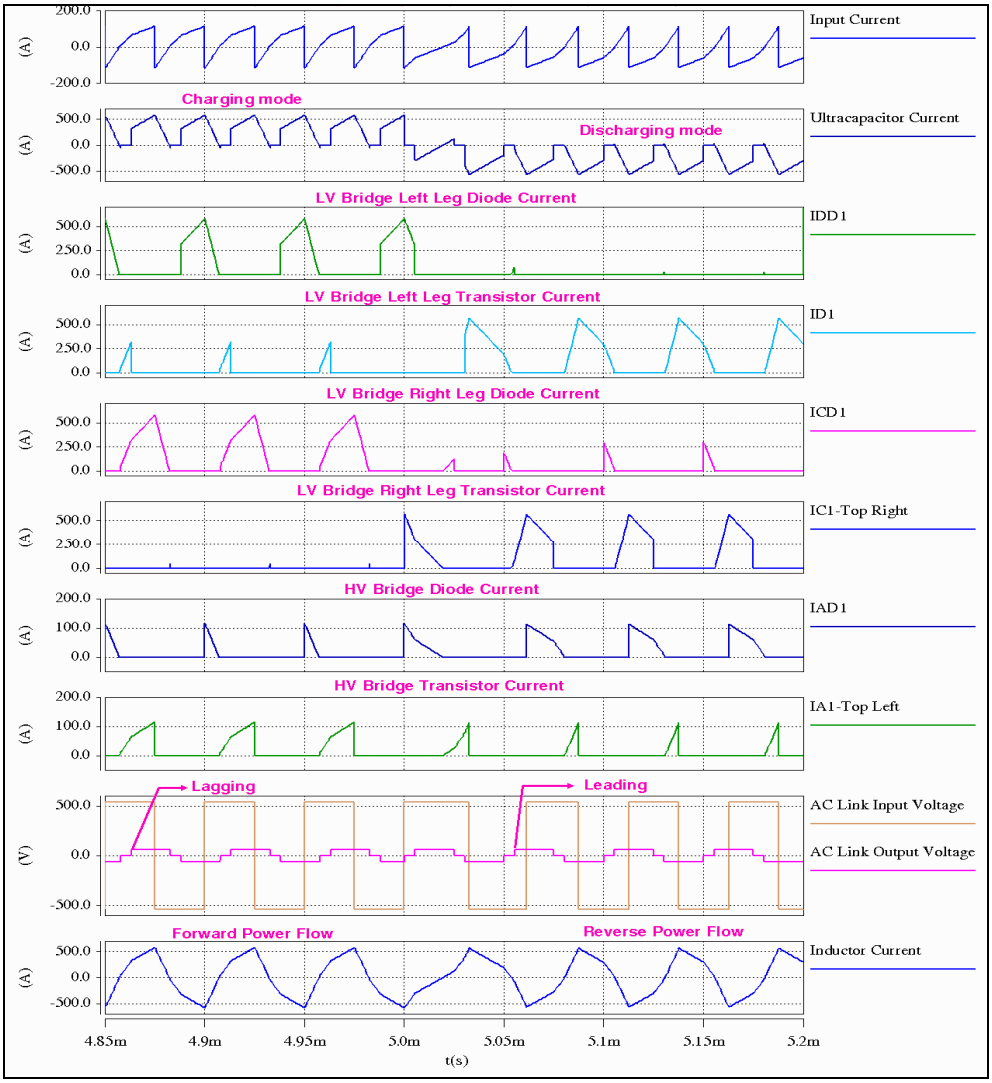


Figure 6.25 Evaluation of control system during bidirectional power transfer showing DAB converter waveforms with quasi-square-wave on transformer secondary
V_{in} = 540V, V_0 = 62.5V, d =+/- 0.3, δ = 0.2, P_0 = 18.4kW, f_s = 20kHz, L = 2.109µH, n =1: 0.2

Inductor currents, AC link voltages, transistor and diode currents for the HV and LV sides, source and ultracapacitor currents are displayed in Figure 6.25. Initially power transfer occurs from the HV side to the LV side, which charges the ultracapacitor. At 5ms, power reversal occurs due to a peak power demand of 18.4kW from the HV side DC bus. As a result, the ultracapacitor discharges to meet the power demand from the HV side. This can be clearly seen from the waveforms shown in Figure 6.25. This once again confirms that the proposed control exhibits a good performance during transients under different scenarios.

6.5.2.3 Confirmation of simulation results with mathematical analysis

Performance of the converter over an operating voltage range (V_0' → 0.2 to 5) is depicted in Figure 6.26, which shows a group of curves for the variation of normalised reference current over normalised average output current with a dead-time variation from 0 to 0.2. The curves are scattered due to the quasi-square-wave mode, which shifts the performance curves towards the left as discussed in Chapter 5 for an increase in the value of dead-time. This can be seen from the black, blue and pink curves of V_0' = 0.5 of Figure 6.26. The ZVS boundaries for buck and boost modes are highlighted in red and green lines respectively. It can be observed from Figure 6.26 that an increase in dead-time on the secondary side of the transformer decreases the boost ZVS boundary as discussed in Chapter 5. These curves are obtained following a similar procedure to that described in section 6.5.1.3. Simulation results are highlighted by '*' and values obtained from the mathematical analysis are represented using solid lines. A good agreement is evident between the simulated and calculated values.

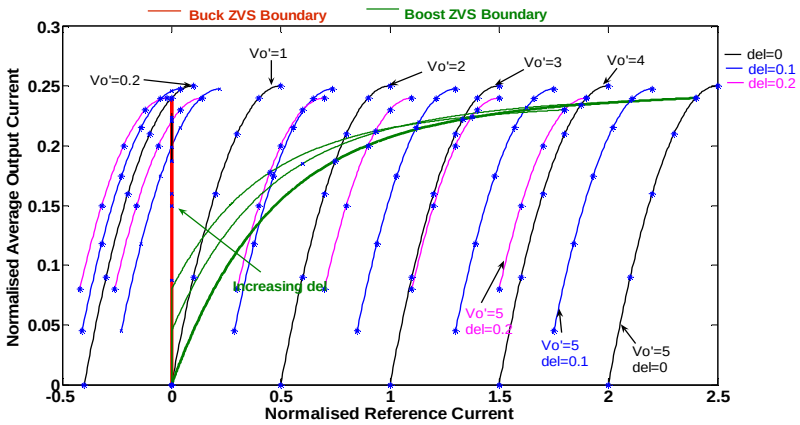


Figure 6.26 Normalised average output current vs normalised reference current for voltage conversion range (Vo' = 0.2 to 5) with quasi-square-wave on transformer secondary

6.5.3 Proposed control applied to converter with a quasi-square-wave voltage on both transformer primary and secondary

This section presents the steady-state and transient response of the proposed controller, for the converter having a quasi-square-wave voltage on transformer primary and secondary sides.

6.5.3.1 Steady-state performance of control system

The simulated steady-state response of the converter for a duty ratio of 0.3 with a dead-time of 0.2 on both sides of the transformer is depicted in Figures 6.27 and 6.28 for charging and discharging modes respectively. From Figure 6.27, the positive average current of the

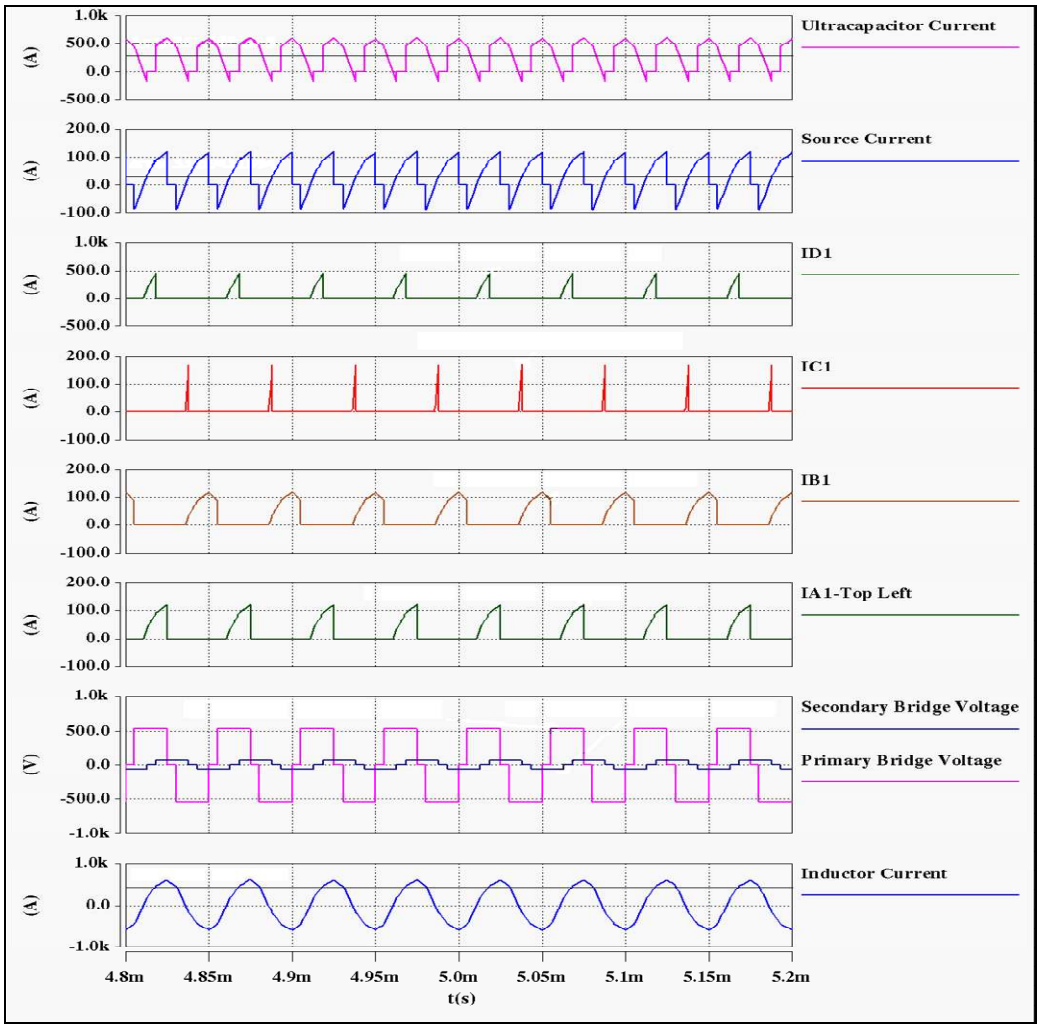


Figure 6.27 Performance of control system during steady-state operation for charging mode of ultracapacitor with quasi-square-wave on transformer primary and secondary V_{in} = 540V, V_0 = 62.5V, d = 0.3, $\delta_i = \delta_0$ = 0.2, P_0 = 18.4kW, I_0 = 294A, f_s = 20kHz, L = 2.109µH, n = 1:0.2

ultracapacitor during charging mode confirms that power is being delivered from the HV side DC bus to the ultracapacitor side. Similarly from Figure 6.28, the negative average current of the ultracapacitor confirms that the ultracapacitor module delivers energy to the HV side DC bus. Analysis of waveforms over a full simulation interval of 10ms showed no glitches or instabilities, which shows that the controller works well during steady-state operation. Figure 6.28 shows in detail some of the waveforms from the 10ms simulation.

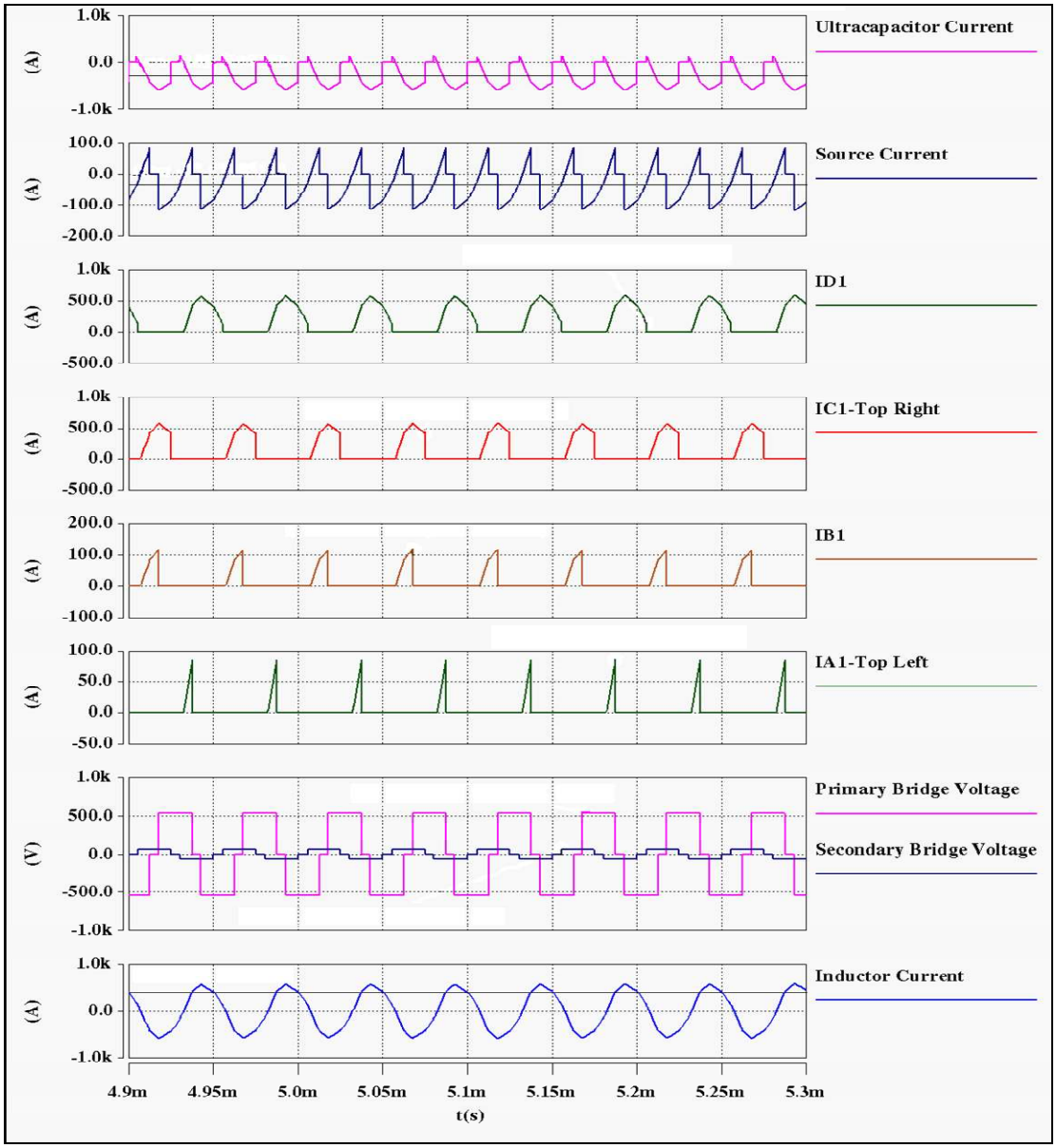


Figure 6.28 Performance of control system during steady-state operation for discharging mode of ultracapacitor with quasi-square-wave on transformer primary and secondary V_{in} = 540V, V_0 = 62.5V, d = 0.3, $\delta_i = \delta_0$ = 0.2, P_0 = 18.4kW, I_0 = - 294A, f_s = 20kHz, L = 2.109µH, n = 1:0.2

6.5.3.2 Evaluation of control system during transients

Figure 6.29 shows the simulated transient response of the converter for a reference current variation from 169A to 350A at 4.85ms illustrating a change in forward power flow and from 350A to 425A at 5ms for a change in power flow direction. The forward current step change shows that the regenerative energy of loads on the DC bus can be used to charge the ultracapacitor, and the reversal of link current shows that loads can be fed by the stored energy from the ultracapacitor. The control response is smooth for the reference current transients; this is apparent from Figure 6.29. Figure 6.30 shows the simulated transient response of the converter under successive input voltage transients, one from 540V to 250V at 3.5ms and another from 250V to 540V at 3.65ms to mimic DC bus transients due to impulsive aircraft electric loads. The variation in input voltage during these time instants is reflected immediately on the inductor current waveforms. As a result, the subsequent variation in inductor, source and ultracapacitor currents can be clearly observed in Figure 6.30. This shows that the proposed controller for the DAB converter can achieve good response under transient voltage changes.

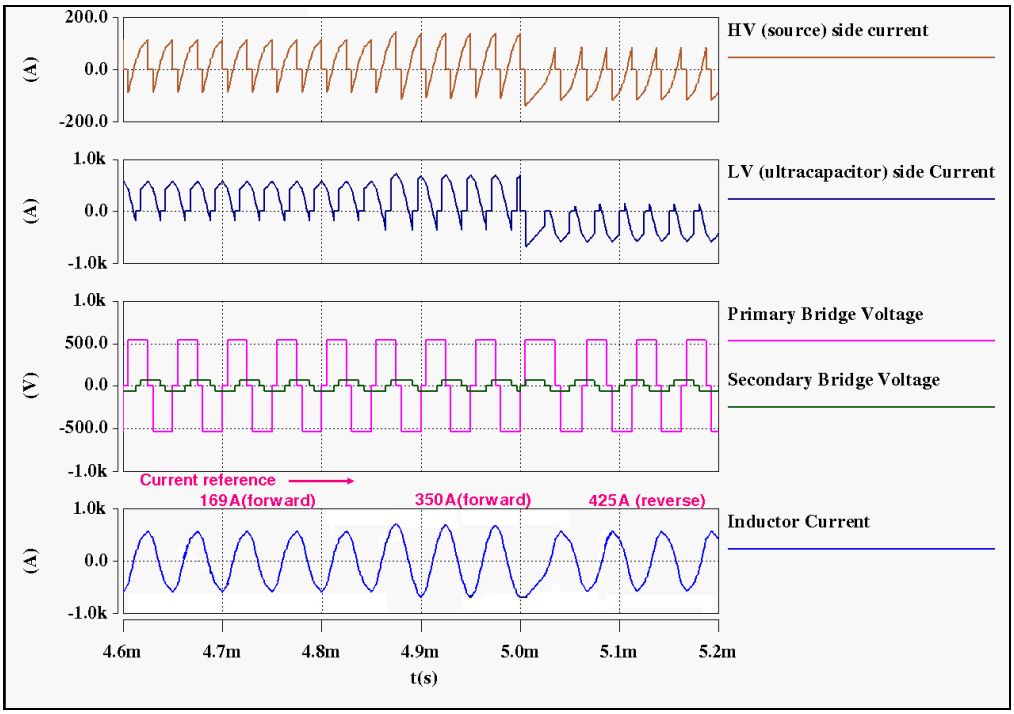


Figure 6.29 Evaluation of control system during current transients from 169A to 350A at 4.85ms and 350A to 425A at 5ms with quasi-square-wave on transformer primary and secondary V_{in} = 540V, V_0 = 62.5V, $\delta_i = \delta_0$ = 0.2, f_s = 20kHz, L = 2.109µH, n = 1:0.2

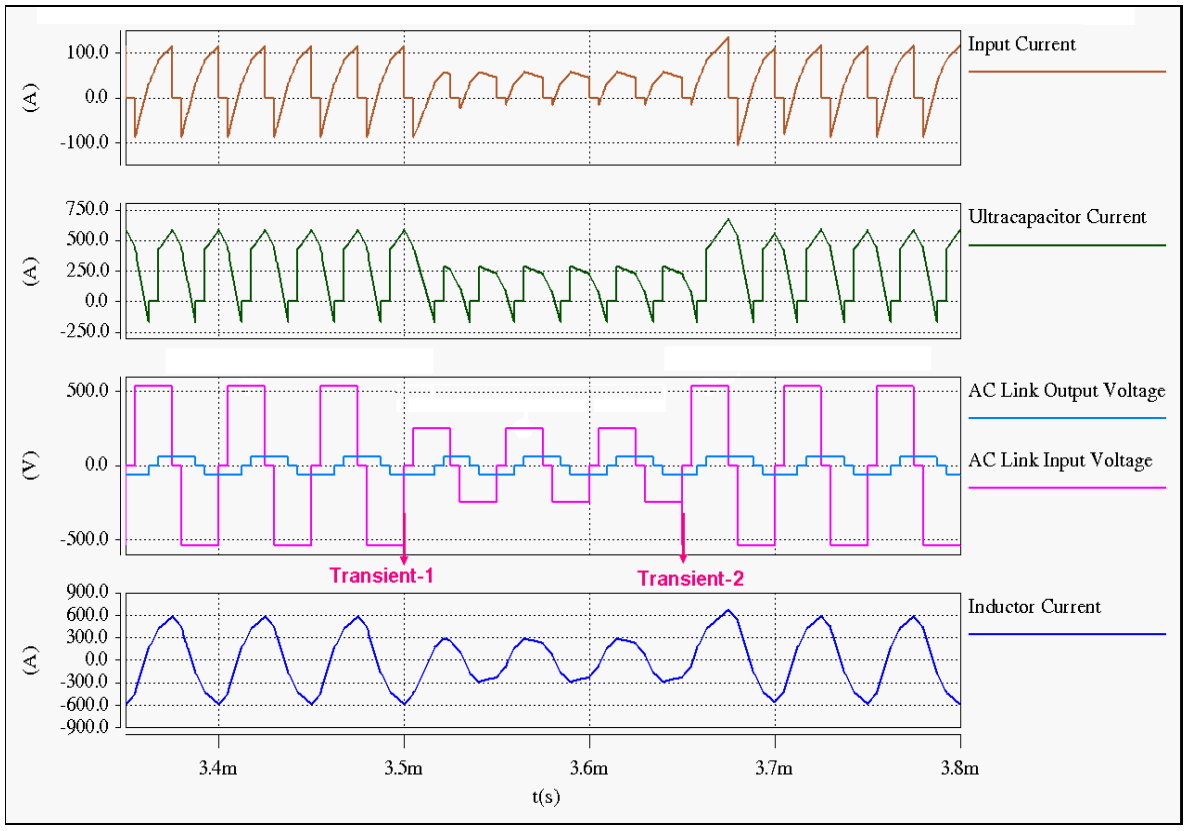


Figure 6.30 Evaluation of control system during voltage transients from 540V to 250V at 3.5ms and from 250V to 540V at 3.65ms with quasi-square-wave on transformer primary and secondary $V_0 = 62.5V$, $\delta_i = \delta_0 = 0.2$, $f_s = 20kHz$, $L = 2.109\mu H$, $n = 1{:}0.2$

Figure 6.31 depicts the response of the converter when a reversal of power transfer is required. Positive current in the ultracapacitor until 5ms illustrates that power is being delivered to the ultracapacitor module. However, at 5ms, due to the power reversal, the stored energy from the ultracapacitor module is delivered to the HV side DC bus. This can be observed from lagging and leading secondary side AC link quasi-square-wave voltage waveforms with respect to the primary quasi-square-wave voltage waveforms before and after 5ms respectively. The device currents on the HV and LV sides of the converter during power transfer reversal are also depicted in Figure 6.31. The function of inversion and rectification of HV and LV side devices during charging is replaced by rectification and inversion during discharging. This can be clearly seen from the device current waveforms of Figure 6.31 for bidirectional power flow. The transient during power reversal is minimal and thus the developed control strategy facilitates smooth operation of the DAB converter.

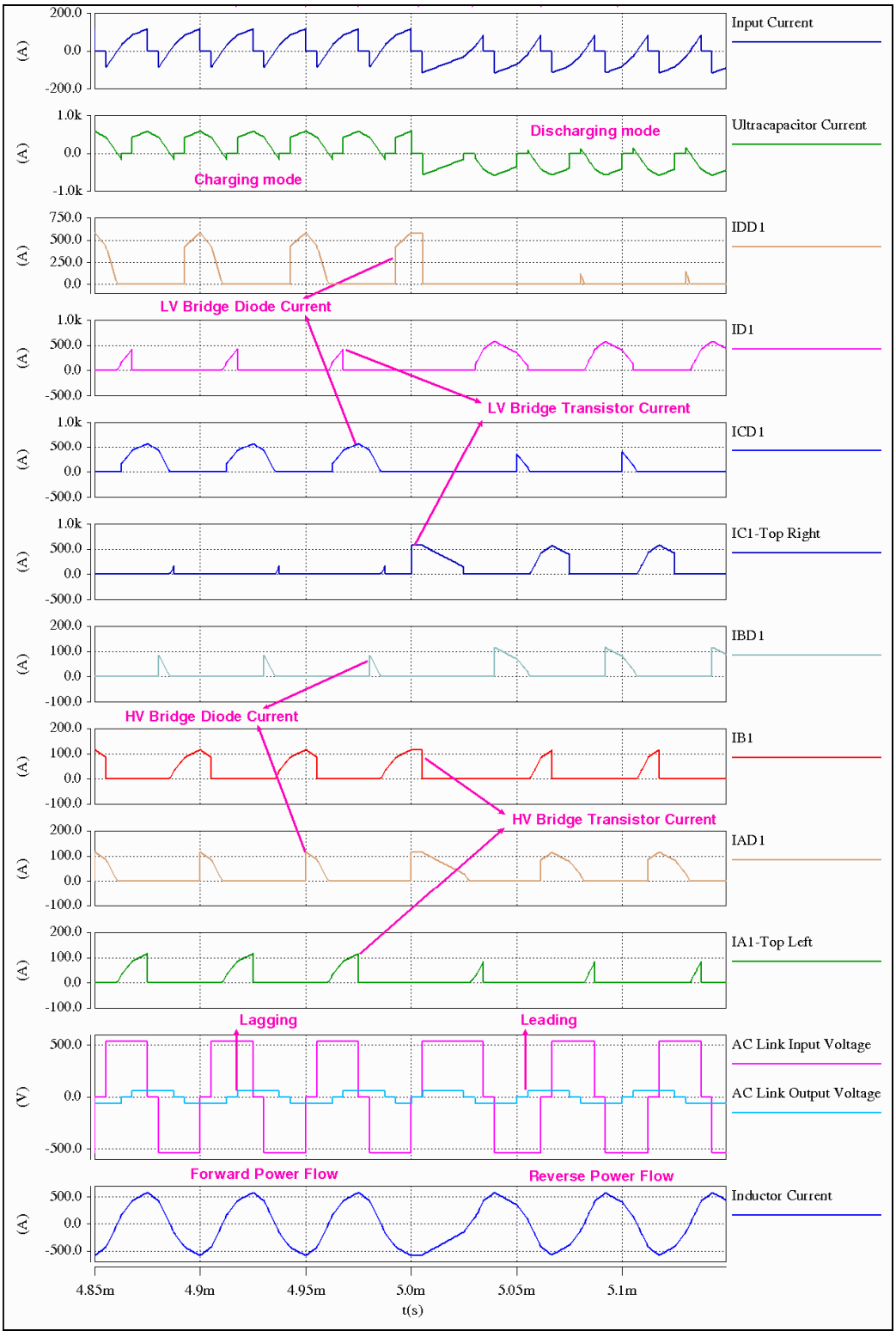


Figure 6.31 Evaluation of control system during bidirectional power transfer showing DAB converter waveforms with quasi-square-wave on transformer primary and secondary V_{in} = 540V, V_0 = 62.5V,d = +/- 0.3, $\delta_i = \delta_0$ = 0.2, P_0 = 18.4kW, f_s = 20kHz, L = 2.109µH, n = 1:0.2

6.5.3.3 Confirmation of simulation results with mathematical analysis

Figure 6.32 shows the performance curves of the DAB converter during forward power flow for a range of voltage conversion ratios from 0.2 to 5. Figure 6.32 depicts the variation of normalised average output current for the variation of normalised reference current, when d varies from 0 to 0.5. Reference current and average output current equations are given in Chapter 5. Solid lines were obtained through the mathematical analysis, presented in Chapter 5. Simulation results are plotted with '*' in the graph. There is a very close agreement between the simulated and calculated values, which confirms the operation of the converter with the proposed control strategy. In order to compare the performance of the converter in quasi-square-wave mode with square-wave mode, a dead-time of $\delta = 0$ is also included.

Equal dead-times ($\delta_i = \delta_0$) are applied on primary and secondary voltage sides to simplify the converter performance curves and these vary from 0 to 0.2 in Figure 6.32. In a manner similar to the previous modes, quasi-square-wave operation on the primary and secondary shifts the performance curves towards the left as δ changes from 0 to 0.2. This can be observed from the black, blue and pink lines (for e.g. $V_0' = 5$) of Figure 6.32. Moreover, an increase in dead-time decreases the maximum power throughput. ZVS boundaries for buck and boost modes are illustrated by the red and green lines respectively in Figure 6.32. It can be seen from Figure 6.32 that the increase in dead-time enhances the ZVS region in buck and boost modes as predicted from the mathematical analysis of Chapter 5.

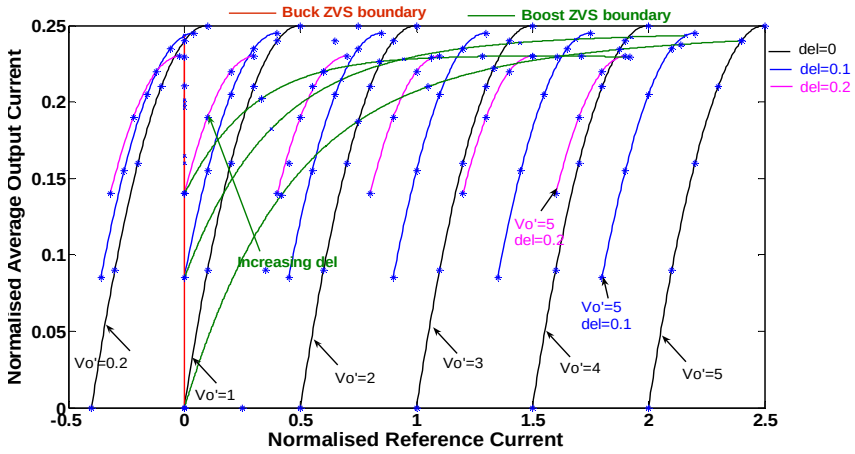


Figure 6.32 Normalised average output current vs normalised reference current for voltage conversion range (Vo' = 0.2 to 5) with quasi-square-wave applied on transformer primary and secondary

6.6 High frequency current sampling and DSP performance

This section describes the practical work undertaken using a DSP and the performance of the DSP under high frequency operation is discussed. In the current mode control strategy, modelled using SABER, inductor current is monitored continuously and the sensed current is compared with the calculated reference current to generate transistor control waveforms. The inductor current frequency is 20 kHz, and hence a direct implementation of the proposed current mode control in real-time using digital hardware is not straight-forward, since a moderately priced very fast Analog to Digital Converter (ADC) with a high number of samples per switching period would be required. Hence, to improve the performance in digital current control, a predictive current control technique [238, 239] was adopted using linear extrapolation, as illustrated in Figure 6.33. Based on present and previous samples of the inductor current, the future sample is predicted as follows.

$$I_{(n+1)} = I_{(n)} + \left(I_{(n)} - I_{(n-1)}\right) \qquad (6.1)$$

Where $I_{(n+1)}$, $I_{(n)}$ and $I_{(n-1)}$ are the future, present and previous samples of inductor current respectively. From Figure 6.33,

$$\frac{I_{(n)} - I_{(n-1)}}{I_{ref} - I_{(n)}} = \frac{\Delta t}{Switchingtime} \qquad (6.2)$$

Therefore, the switching time can be calculated as,

$$\text{Switching time} = \frac{I_{ref} - I_{(n)}}{I_{(n)} - I_{(n-1)}} \times \Delta t \qquad (6.3)$$

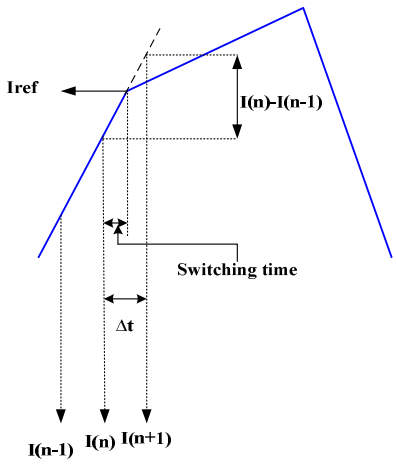


Figure 6.33 Principle of predictive current sampling

The DSP has two main tasks. The first is to compute reference current based on input current demand. This task is computationally intensive because the value of duty ratio has to be obtained first. If the calculated duty ratio falls outside the converter soft switching region, then it is modified to fall within the ZVS operating region of the converter. This is done by measuring the output voltage and computing the ZVS limits for the same. Once this is done, the reference current has to be estimated for the desired value of duty ratio. The second task is to sample the high frequency inductor current and compare it with the calculated reference current value. When the sampled value is found to be greater than the calculated value, the correct switching time is estimated using (6.3) to generate the PWM signal for the target H-bridge.

A Texas Instruments (TI) TMS320F2812 [240-248] Digital Signal Processor (DSP) was programmed using Code Composer Studio (CCS) to carry out these tasks. The speed, resolution, on chip memory, integrated low and high speed peripherals such as 12bit 16 channel ADC and Event managers for PWM generation respectively, and other features of this DSP make it a good choice. CCS Integrated Development Environment (IDE) [249] is a key element of the DSP Software and Development Tools strategy from Texas Instruments. The user can design, code and build, debug, analyze and tune the developed software using CCS IDE. The IDE includes DSP/BIOS support, real-time analysis capabilities, debugger and optimization tools, C/C++ compiler [250,251], assembler, linker, simulators and emulation drivers. This debug facility allows the finding and fixing of real-time issues. The number of processor cycles for calculating the reference current in floating point and fixed-point control algorithms using TMS320F2812 DSP (150MHz) was estimated using the code composer studio real time emulation platform. The reference current computation time for floating point calculation equalled 3343 processor cycles, which is 22.297μs. The F2812 DSP is a fixed point DSP. This fixed-point processor has an internal hardware that supports operations with integer data. Therefore, the DSP expects all data to be in fixed-point data types. There are limitations in the dynamic range of this processor due to the 32 bit fixed-point feature. Texas Instruments C28X DSP has an “IQmath” library, which is a collection of optimised and high precision mathematical functions used to port floating point algorithms into fixed-point code. Input numbers are split into two parts: I-integer, Q-quotient, called IQ numbers. Since the

computation time is very long using a floating-point algorithm, the algorithm was tuned in fixed point using the IQ numbers library [252] of TI. There was a significant reduction in computation time, achieved using IQ numbers. The estimated computation time for the developed program is 706 processor cycles, which is 4.709µs. Although the computation time was improved by using IQ numbers, the sampling of high frequency inductor current using this DSP was cumbersome. An experimental real time input of 270A peak-to-peak current from the current sensor was fed to the DSP through a signal conditioning circuit. The ADC clock speed as per the datasheet [253, 254] was 25MHz, with a maximum sampling frequency of 12.5MHz. The ADC sampling frequency was varied from 2.5MHz, capturing samples every 400ns (200ns sampling+200ns hold). The performance of the ADC was poor for the chosen frequency due to the high sampling speed. The sampling interval was increased to 1.28µs ensuring the ADC operated at a sampling frequency of 781.25 kHz. However, experiments showed that the ADC was not capable of sampling an AC signal at such a high rate. Figures 6.34 and 6.35 depict the DSP samples in terms of their real time values displayed in the Time/frequency graph (yellow region). The top signal is the measured current after DSP

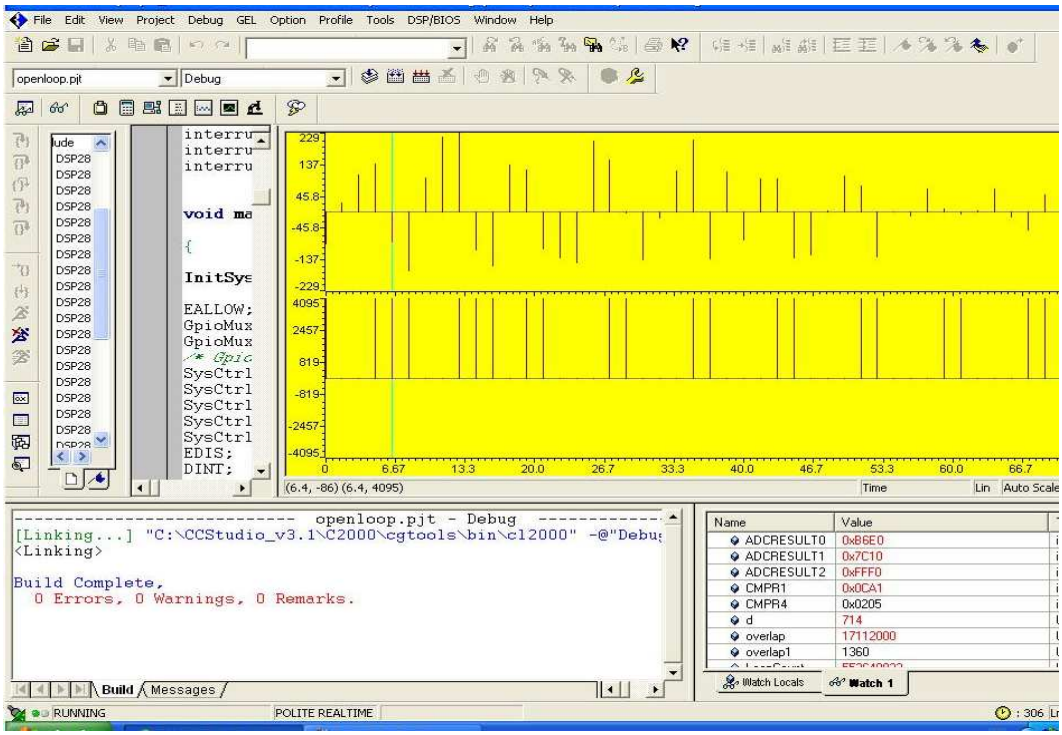


Figure 6.34 DSP sampling performance for high frequency signals in bar representation
Top signal - 20 kHz inductor current input, Bottom signal – 20 kHz PWM signal input

computation; the bottom signal is the 20 kHz PWM signal generated by the DSP. Figure 6.34 depicts the sampling instants in 'bar', whereas Figure 6.35 depicts it in 'line'. To determine the actual number of samples of the measured current per switching cycle, the measured current was compared with the PWM signal, which was fed to the ADC input from the digital output of the processor. The ADC was not able to sample the current and PWM signals for the assigned sampling interval of 1.28µs. This can be observed from Figures 6.34 and 6.35; the clean 20 kHz PWM signal was not sampled completely. The number of samples measured is shown in bars in Figure 6.34, it confirms that the samples are not at a specified sampling rate of 1.28µs.

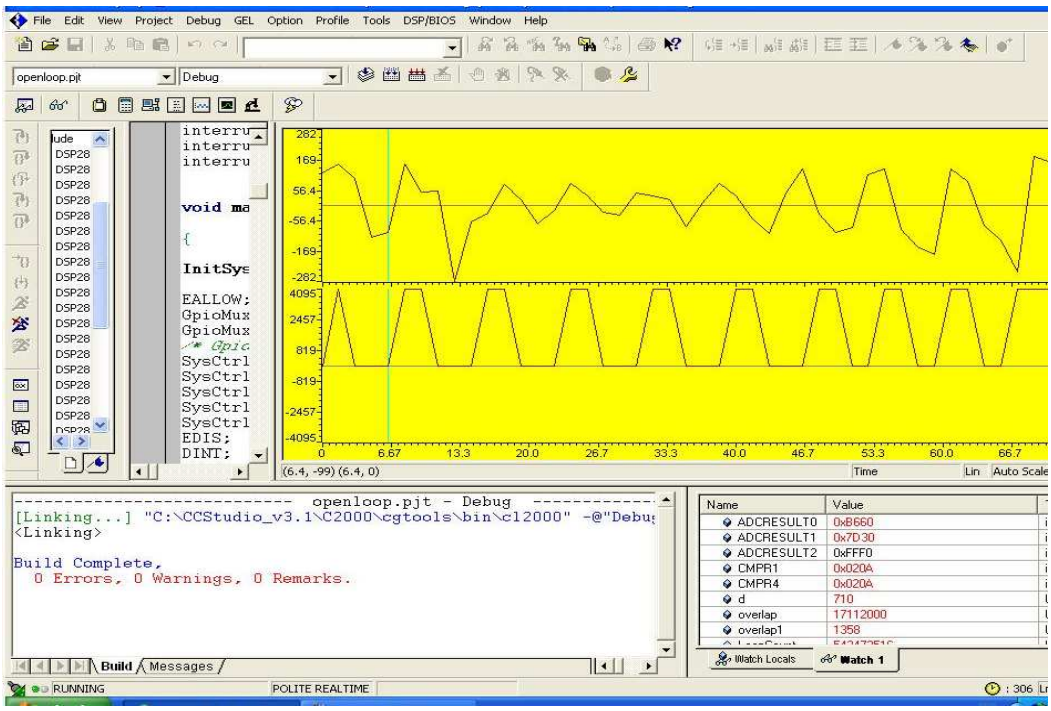


Figure 6.35 DSP sampling performance for high frequency signals in line representation
Top signal - 20 kHz inductor current input, Bottom signal – 20 kHz PWM signal input

Sampling and controlling the inductor current in the DAB DC/DC converter using a DSP presents a great challenge in addition to the demands on the digital hardware. In order to effectively control the fast changing inductor current, it is necessary to obtain essential samples of the inductor current before the first occurring reference current peak. The digital controller has to sample the inductor current at appropriate time instants to measure the correct value of current [255, 256]. Due to these reasons, predictive current control was not

achievable for this application using the above-mentioned DSP. Based on the operating region of the DAB converter discussed in Chapter 2, under the best case condition (90 degree phase shift) for the chosen switching frequency, desired samples fall within one fourth of the switching period (12.5μs), which is 80kHz. This requires a very fast ADC to produce multiple samples of the sensed current per quarter of the switching period. For the worst-case scenario, the essential samples fall within 1.7μs, which is 589 kHz. Achieving such a wide range of control needs an extremely fast ADC, data acquisition interfaces and a very high-speed processor. Moreover, the computational burden assigned to the processor to achieve high frequency current control is significantly high. Therefore, it might not be presently feasible to implement this technique with modest digital hardware resources [257].

6.7 Summary

A novel controller for the DAB DC-DC converter has been presented and some preliminary investigations were undertaken to show its operation. A SABER simulation model has been developed for the proposed control strategy considering high frequency inductor current as the control parameter. The performance of the DAB converter was verified through simulations and mathematical analysis for square-wave and quasi-square-wave operation. Steady-state and transient performance evaluation of the converter using SABER simulation confirms that the proposed control improves the performance of the converter during peak power demands. Practical issues regarding the implementation of the proposed control were investigated. The most significant problem in achieving the desired control was found to be the high frequency inductor current sampling. Moreover, the computational burden assigned to the processor to achieve high frequency current control is significantly high. The need for a moderately priced very fast ADC to produce multiple samples of the sensed current per switching period, and the corresponding need for large signal processing capabilities may require excessively complex hardware. Hence, it might not be feasible to implement the proposed high frequency current control with modest digital hardware resources. Although the proposed control exhibits good performance with SABER simulations, the challenges in the practical implementation have to be overcome to examine the performance of the proposed control in real-time scenarios. Also, further improvements can be made in the implementation of the controller. The design and

evaluation of the performance of the DAB converter in real-time is thus suggested as a direction for further research.

Chapter 7
Conclusions and Scope for Future Work

In this final Chapter, a concise description of the contributions to knowledge, outlined in this Thesis, is provided followed by a brief discussion of potential research directions resulting from the work described.

7.1 Summary of Thesis contributions

7.1.1 Steady-state analysis

This Thesis has made a contribution to the steady-state analysis of the DAB DC-DC converter for square-wave operation by presenting equations for RMS and average device currents and RMS and peak inductor/transformer currents. These equations are useful in predicting the losses that occur in the devices and passive components. Using the analytical expressions for the RMS currents, it is possible to size suitable filter capacitors on the HV and LV sides of the converter. In addition, expressions for average and RMS device currents are useful in selecting suitable power semiconductor components for the converter, and determining power losses and converter efficiency at any operating point.

The converter operating conditions to achieve virtually loss-less zero-voltage switching conditions were derived from the analysis for charging and discharging modes. The zero-voltage switching region of the converter was obtained through analysis. The operation of the DAB DC-DC converter has been verified through extensive simulations confirming the accuracy of the analysis. The converter was designed and built and experimental results provided to support the analysis for a 7kW, 390/180V, 20 kHz operation of the prototype converter with a measured efficiency of 90%.

7.1.2 Quasi-square-wave mode of operation

To overcome the drawbacks present in the traditional square-wave mode of operation of the DAB converter under light-load conditions, a quasi-square-wave mode of operation for the

DAB converter was proposed, by introducing a dead-time on the transformer primary (HV bridge) voltage waveform alone, a dead-time on the transformer secondary (LV bridge) alone and a dead-time simultaneously on both transformer primary (HV bridge) and secondary (LV bridge). This improved the zero-voltage switching region of the converter without additional passive elements.

7.1.2.1 Quasi-square-wave applied on transformer primary

A new waveform analysis of the DAB converter was performed by introducing a quasi-square-wave voltage on the transformer primary (HV bridge) side and retaining the square-wave voltage on the transformer secondary (LV bridge) side. The analysis provided equations for device RMS and average currents and the peak and RMS currents of the inductor/transformer. The zero-voltage switching condition of the converter was determined from the device current waveforms. The duty ratio corresponding to the zero-voltage switching limit was obtained for buck and boost modes of operation.

The analysis is useful as it defines the limit for soft-switching over a wide operating voltage range for quasi-square-wave operation and the average and RMS expressions derived are useful in predicting the losses that occur in the devices and passive components. Furthermore, the performance of the converter has been analysed in the context of ZVS operating range, the RMS and peak inductor/transformer currents, and the influence of dead-time on the primary during power transfer. This allows a study of converter characteristics. Power transfer is improved under light-load conditions thereby enhancing the converter efficiency at light-loads. ZVS enhancement is achieved for lower voltage conversion ratios $\left(V_0^{'} < 1\right)$ at the expense of increased conduction losses. The operation of the DAB converter has been validated through extensive SABER simulations and experiments. The experimental results confirm that the converter operates at 91.8% efficiency at 1kW with a 17% improvement in the ZVS operating range and a 9.7% increase in average output current, when compared to square-wave operation on both the sides of isolation transformer, thereby verifying the converter operation and confirming the accuracy of the analysis.

7.1.2.2 Quasi-square-wave applied on transformer secondary

A similar analysis has been undertaken by introducing a quasi-square-wave voltage on the transformer secondary (LV bridge) and retaining a square-wave voltage (HV bridge) on the transformer primary. A mathematical model of the DAB converter under buck and boost modes of operation has been derived. The expressions for the average and RMS device currents and the peak and RMS currents of the coupling inductor/transformer were obtained through analysis.

The zero-voltage switching conditions were determined based on the device current waveforms. The duty ratio corresponding to the zero-voltage switching limit was obtained for buck and boost modes of operation. This paves the way for estimating the soft-switching region of the converter for any operating voltage range. Loss prediction of the devices and passive components in the converter could be done using the equations obtained through the steady-state analysis. The performance of the converter was analysed from the viewpoint of ZVS operating range, the RMS and peak inductor/transformer currents, power transfer and converter efficiency. Higher converter efficiency is obtained under light-loads and the ZVS operating region is enhanced for higher voltage conversion ratios. Proof of concept experimental results at 1kW confirm that the converter operates with 91% efficiency. A 6.8% improvement in the average output current was observed over square-wave operation, thereby verifying the converter operation and confirming the analysis. Simulation and experimental results are in close agreement, which demonstrates the veracity of the analysis.

7.1.2.3 Quasi-square-wave applied on both transformer primary and secondary

The performance of the converter was analysed by introducing a quasi-square-wave voltage on the transformer primary (HV bridge) side as well as on the transformer secondary (LV bridge) side. The analysis produced equations for device RMS and average currents and the peak and RMS currents in the coupling inductor/transformer. The zero-voltage switching boundary limits for the converter operation were determined based on the device current waveforms.

Mathematical models obtained from the analysis permit a study of the converter characteristics. These models are useful for converter design as they allow loss calculation of various devices enabling the most suitable power semiconductor devices for a specific application and the input and output filter capacitors for the desired voltage ripple to be selected. The effect of dead-time on the transformer primary and secondary bridges was analysed in terms of ZVS operating range, RMS and peak inductor/transformer currents, power transfer and converter efficiency. Improvement in the ZVS operating range was achieved over a wide operating voltage range and higher converter efficiency was obtained under light-loads. The analysis was validated through extensive simulations and experimental results. The measured results confirm that the DAB converter operates with a high efficiency of 97.5% at 1kW for quasi-square-wave operation with $\delta_i = \delta_0 = 0.1$ on both sides of the transformer. Thus there is an improvement in efficiency and ZVS operating range over the square-wave operation of the DAB converter by 16.8% and 10% respectively. Measurements at different conditions ($\delta_i = 0.1$ and $\delta_0 = 0.15$) confirm that the converter operates with an efficiency of about 98%, with a 12.4% improvement in ZVS operating range.

Few papers have been published on the quasi-square-wave mode of operation of the DAB converter, based on modification of the duty ratio of the quasi-square-wave voltage. However, in this Thesis, quasi-square-wave operation was analysed in detail by varying the dead-time in the quasi-square-wave voltage. Such a detailed waveform analysis is not present in the existing literature. Furthermore, the derivation of expressions for the device RMS and average currents and the RMS and peak inductor/transformer currents and the ZVS boundary conditions are unique and novel contributions.

7.1.3 Bidirectional control technique

A novel bidirectional current control technique was proposed to generate phase shifted PWM signals for the DAB converter and some preliminary investigations were undertaken to improve the dynamics of the power conversion system during bidirectional power transfer. The coupling inductor current was chosen as the control parameter. The first peak of the inductor current waveform at which the lagging bridge switching instant takes place was

chosen as the reference current. A SABER simulation model has been developed to validate the proposed control strategy.

The performance of the converter has been verified under steady-state and transient conditions for square-wave and quasi-square-wave modes of operation using the proposed control technique. The proposed control exhibits a good response under current and voltage transients as well as during bidirectional power flow. A time domain transient simulation response obtained using SABER confirms that the proposed control will improve the dynamics of the system under transients and verifies the accuracy of the analysis presented in this Thesis. However, challenges in the practical implementation and optimising the performance of the proposed control in real-time remain. Application-Specific Integrated Circuit (ASIC) technology can possibly be used to overcome the problems that exist with high frequency current sampling in such advanced control, particularly for this special application.

7.2 Directions for further research

This research could pave the way for further research in this area in the following ways:

7.2.1 Challenges in bidirectional current control

Practical design of the proposed bidirectional current controller for the DAB converter has several challenges, especially in real-time implementation and testing. Experimental verification of the proposed controller in an ultracapacitor energy storage system would help to further analyse and investigate the behaviour of the power electronic interface and the energy storage system dynamics under transients in real-time. This would pave the way for validating the idea proposed in Chapter 6.

7.2.2 Study of system dynamics in testing with active loads of IEPNEF

Investigating the behaviour of the aircraft electrical power network by testing the converter with active loads in the Intelligent Electrical Power Networks Evaluation Facility could extend this research, which is of particular interest for designers of electrical systems for future aircraft. This would enable an understanding of the difficulties to be met with the regenerative

capability of real-time aircraft loads and allow designers to examine and analyse the performance of the converter as well as to study the aircraft power system dynamics.

7.2.3 Research on discontinuous current mode

Recent literature [88, 107-108] addresses trapezoidal and triangular discontinuous current modes in quasi-square-wave operation of the DAB converter. However, further research is needed to examine converter performance under such peculiar modes in the context of zero-voltage/zero-current switching operating range, effect of discontinuous current on the RMS and peak inductor/transformer currents and device losses and power conversion efficiency.

7.2.4 Active combination of two or more energy storage systems

Further research could be done by examining the performance of the aircraft power system with an active combination of two or more energy storage devices (such as batteries and ultracapacitors) interfaced via additional active bridges on the low voltage, high current side. Interaction of slow battery energy storage and fast ultracapacitor energy storage with the aircraft power system under various power demands can be studied. Such an active combination could possibly lead to an efficient energy storage system with reduced size and weight for advanced aircraft.

7.2.5 Extended converter control

From the analysis of the DAB converter with quasi-square-wave mode of operation, it can be observed that a wide range of control is achievable with zero-voltage switching and converter efficiency can be enhanced under light load conditions. To avail these benefits, a controller has to be suitably designed to switchover between quasi-square-wave and square-wave modes while changing from light-load to heavy-load conditions respectively. However, this may demand a sophisticated controller with large signal processing capabilities and a very fast analog-to-digital converter to produce multiple samples of the sensed signal per switching cycle.

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APPENDIX A

Derivation of RMS Current Equations of DAB DC-DC Converter

A.1 Inductor/Transformer RMS current derivation for charging mode

This section gives the step-by-step derivation of the inductor/transformer RMS current equation of the DAB DC-DC converter during charging mode. This is to support the analysis presented in Chapter 2 of this Thesis. Since the inductor/transformer current waveform is similar and piece-wise linear, the waveform can be split into triangular or trapezoidal shapes over any time interval. The effective intervals of those triangular and trapezoidal shapes were used to individually obtain their RMS currents and summed together to get the total RMS current equation of DAB converter waveforms. Figure A.1 depicts the waveforms of the inductor/transformer i_L, the HV (i_{A1}, i_{AD1}) and the LV device (i_{C1}, i_{CD1}) currents and the output (LV-side terminal) current i_0. Various notations used in the analysis are marked in Figure A.1. Actual interval is marked in i_L current waveform and the effective intervals are marked below the i_0 current waveform of Figure A.1, for the purpose of elucidating the derivation.

From Figure A.1, it can be observed that the inductor/transformer current is periodic and symmetrical over a cycle; hence the RMS value for a half cycle has been used to determine the corresponding value for the whole period. The instantaneous current $I(t)$ over a half cycle is represented as follows:

$$I(t) = \frac{I_{L1}}{\frac{dT_S}{2} - t_B} t, 0 < t < \frac{dT_S}{2} - t_B$$

$$= I_{L1} + \frac{I_r t}{\frac{T_S}{2} - t_B}, \frac{dT_S}{2} - t_B < t < \frac{T_S}{2} - t_B$$

$$= I_P - \frac{I_P t}{\frac{T_S}{2}}, \frac{T_S}{2} - t_B < t < \frac{T_S}{2}$$

Changing the limits to their effective interval as indicated in Figure A.1 for simplification purpose gives,

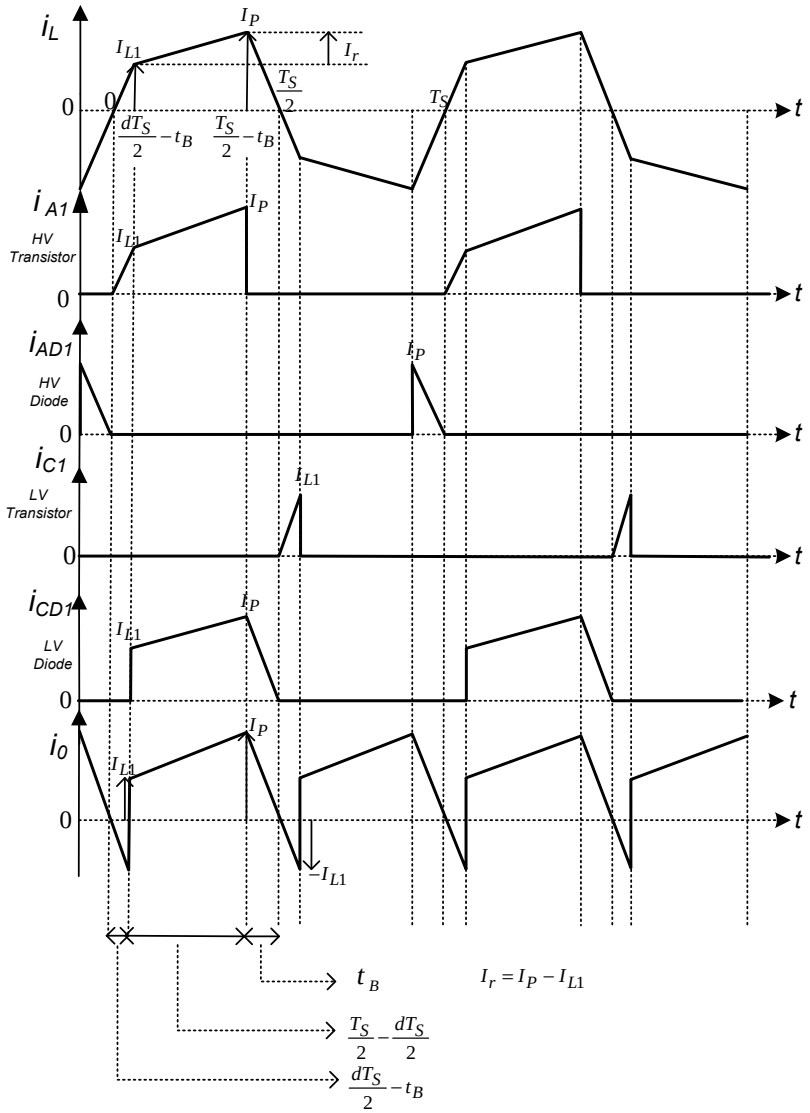

Figure A.1 Transformer/inductor, output and device current waveforms of the DAB converter

$$I(t) = \frac{I_{L1}}{\frac{dT_S}{2} - t_B} t, 0 < t < \frac{dT_S}{2} - t_B$$

$$= I_{L1} + \frac{I_r t}{\frac{T_S}{2} - \frac{dT_S}{2}}, 0 < t < \frac{T_S}{2} - \frac{dT_S}{2}$$

$$= I_P - \frac{I_P t}{t_B}, 0 < t < t_B$$

$$I_{RMS} = \sqrt{\frac{2}{T_S} \int_0^{\frac{T_s}{2}} I^2(t)\,dt} \qquad \text{(A.1)}$$

Squaring the transformer current over the intervals,

$$I^2(t) = \left(\frac{I_{L1}}{\frac{dT_S}{2} - t_B}\right)^2 t^2, 0 < t < \frac{dT_S}{2} - t_B$$

$$= {I_{L1}}^2 + \left(\frac{I_r}{\frac{T_S}{2} - \frac{dT_S}{2}}\right)^2 t^2 + \frac{2I_{L1}I_r t}{\frac{T_S}{2} - \frac{dT_S}{2}}, 0 < t < \frac{T_S}{2} - \frac{dT_S}{2}$$

$$= {I_P}^2 + \left(\frac{I_P}{t_B}\right)^2 t^2 - \frac{2{I_P}^2 t}{t_B}, 0 < t < t_B$$

Substituting $I^2(t)$ in equation (A.1),

$$I_{RMS} = \sqrt{\frac{2}{T_S}\left[\int_0^{\frac{dT_S}{2}-t_B}\left(\frac{I_{L1}}{\frac{dT_S}{2}-t_B}\right)^2 t^2 dt + \int_0^{\frac{T_S}{2}-\frac{dT_S}{2}}\left({I_{L1}}^2 + \left(\frac{I_r}{\frac{T_S}{2}-\frac{dT_S}{2}}\right)^2 t^2 + \frac{2I_{L1}I_r t}{\frac{T_S}{2}-\frac{dT_S}{2}}\right)dt + \int_0^{t_B}\left({I_P}^2 + \left(\frac{I_P}{t_B}\right)^2 t^2 - \frac{2I_P^2 t}{t_B}\right)dt\right]}$$

Minimising and simplifying further, the final expression for the transformer RMS current during charging mode is obtained and expressed as,

$$I_{RMS} = \sqrt{\frac{2}{T_S}\left[\frac{(I_{L1})^2\left(\frac{dT_S}{2}-t_B\right)}{3} + \left(\frac{T_S}{2}-\frac{dT_S}{2}\right)\left({I_{L1}}^2 + \frac{{I_r}^2}{3} + I_{L1}I_r\right) + \frac{{I_P}^2 t_B}{3}\right]} \quad \text{(A.2)}$$

A.2 LV side terminal (output) RMS current derivation

Similar procedure is applied as above to derive the expression for RMS current equation of the output (LV side terminal) charging current i_0. The charging current waveform shown in Figure A.1 is represented by the instantaneous values for various intervals as given below. This waveform is periodic over a half cycle. Hence, for a half cycle, the instantaneous current

$$I(t) = I_{L1} + \frac{I_r}{\frac{T_S}{2} - \frac{dT_S}{2}} t, 0 < t < \frac{T_S}{2} - \frac{dT_S}{2}$$

$$= I_P - \frac{I_P t}{\frac{T_S}{2} - \frac{dT_S}{2} + t_B}, \frac{T_S}{2} - \frac{dT_S}{2} < t < \frac{T_S}{2} - \frac{dT_S}{2} + t_B$$

$$= \frac{-I_{L1}t}{\frac{T_S}{2}}, \frac{T_S}{2} - \frac{dT_S}{2} + t_B < t < \frac{T_S}{2}$$

Converting the limits of the above current to its effective interval for simplification,

$$I(t) = I_{L1} + \frac{I_r}{\frac{T_S}{2} - \frac{dT_S}{2}} t, 0 < t < \frac{T_S}{2} - \frac{dT_S}{2}$$

$$= I_P - \frac{I_P t}{t_B}, 0 < t < t_B$$

$$= \frac{-I_{L1}t}{\frac{dT_S}{2} - t_B}, 0 < t < \frac{dT_S}{2} - t_B$$

Squaring the current over the intervals,

$$I^2(t) = {I_{L1}}^2 + \left(\frac{I_r}{\frac{T_S}{2} - \frac{dT_S}{2}} \right)^2 t^2 + \frac{2I_{L1}I_r t}{\frac{T_S}{2} - \frac{dT_S}{2}}, 0 < t < \frac{T_S}{2} - \frac{dT_S}{2}$$

$$= {I_P}^2 + \left(\frac{I_P}{t_B} \right)^2 t^2 - \frac{2{I_P}^2 t}{t_B}, 0 < t < t_B$$

$$= \left(\frac{-I_{L1}}{\frac{dT_S}{2} - t_B} \right)^2 t^2, 0 < t < \frac{dT_S}{2} - t_B$$

Then, the RMS value can be written as,

$$I_{RMS} = \sqrt{\frac{2}{T_S} \int_0^{\frac{T_S}{2}} I^2(t)\, dt}$$

Substituting $I^2(t)$ in equation (A.3) gives,

$$I_{RMS} = \sqrt{\frac{2}{T_S}\left[\int_0^{\frac{T_S}{2} - \frac{dT_S}{2}} \left({I_{L1}}^2 + \left(\frac{I_r}{\frac{T_S}{2} - \frac{dT_S}{2}} \right)^2 t^2 + \frac{2I_{L1}I_r t}{\frac{T_S}{2} - \frac{dT_S}{2}} \right) dt + \int_0^{t_B} \left({I_P}^2 + \left(\frac{I_P}{t_B} \right)^2 t^2 - \frac{2I_P^2 t}{t_B} \right) dt + \int_0^{\frac{dT_S}{2} - t_B} \left(\frac{-I_{L1}}{\frac{dT_S}{2} - t_B} \right)^2 t^2 dt \right]}$$

Reducing further, the final equation for the RMS current of the LV side terminal is obtained as follows,

$$I_{RMS}=\sqrt{\frac{2}{T_S}\left[\frac{(I_{L1})^2\left(\frac{dT_S}{2}-t_B\right)}{3}+\left(\frac{T_S}{2}-\frac{dT_S}{2}\right)\left(I_{L1}{}^2+\frac{I_r{}^2}{3}+I_{L1}I_r\right)+\frac{I_P{}^2t_B}{3}\right]} \quad \text{(A.3)}$$

A.3 Transistor and Diode RMS current derivation

A.3.1 HV side transistor RMS current derivation

For the HV side transistor current shown in Figure A.1, the waveform is periodic over a cycle. The instantaneous current is expressed as,

$$I(t)=\frac{I_{L1}}{\frac{dT_S}{2}-t_B}t,0<t<\frac{dT_S}{2}-t_B$$

$$=I_{L1}+\frac{I_r t}{\frac{T_S}{2}-t_B},\frac{dT_S}{2}-t_B<t<\frac{T_S}{2}-t_B$$

$$=0,\frac{T_S}{2}-t_B<t<T_S$$

Changing the limits to their effective interval as indicated in Figure A.1 for simplification,

$$I(t)=\frac{I_{L1}}{\frac{dT_S}{2}-t_B}t,0<t<\frac{dT_S}{2}-t_B$$

$$=I_{L1}+\frac{I_r t}{\frac{T_S}{2}-\frac{dT_S}{2}},0<t<\frac{T_S}{2}-\frac{dT_S}{2}$$

Then squaring the above current gives,

$$I^2(t)=\left(\frac{I_{L1}}{\frac{dT_S}{2}-t_B}\right)^2 t^2,0<t<\frac{dT_S}{2}-t_B$$

$$=I_{L1}{}^2+\left(\frac{I_r}{\frac{T_S}{2}-\frac{dT_S}{2}}\right)^2 t^2+\frac{2I_{L1}I_r t}{\frac{T_S}{2}-\frac{dT_S}{2}},0<t<\frac{T_S}{2}-\frac{dT_S}{2}$$

RMS equation,

$$I_{RMS} = \sqrt{\frac{1}{T_S}\int_0^{T_S} I^2(t)\,dt}$$

Substituting the squared current in the above equation,

$$I_{RMS} = \sqrt{\frac{1}{T_S}\left[\int_0^{\frac{dT_S}{2}-t_B}\left(\frac{I_{L1}}{\frac{dT_S}{2}-t_B}\right)^2 t^2 d + \int_0^{\frac{T_S}{2}-\frac{dT_S}{2}}\left(I_{L1}^2 + \left(\frac{I_r}{\frac{T_S}{2}-\frac{dT_S}{2}}\right)^2 t^2 + \frac{2I_{L1}I_r t}{\frac{T_S}{2}-\frac{dT_S}{2}}\right)dt\right]}$$

Simplifying further gives the RMS current equation of HV transistor

$$I_{RMS} = \sqrt{\frac{1}{T_S}\left[\frac{(I_{L1})^2\left(\frac{dT_S}{2}-t_B\right)}{3} + \left(\frac{T_S}{2}-\frac{dT_S}{2}\right)\left(I_{L1}^2 + \frac{I_r^2}{3} + I_{L1}I_r\right)\right]} \quad \text{(A.4)}$$

A.3.2 HV side diode RMS current derivation

HV side diode has a triangular current waveform. Similar procedure is followed to derive the RMS current expression. Considering the effective intervals, the instantaneous current of HV side diode can be expressed as,

$$I(t) = I_P - \frac{I_P t}{t_B}, 0 < t < t_B$$

$$= 0, t_B < t < T_S$$

Squaring the current,

$$I^2(t) = I_P^2 + \left(\frac{I_P}{t_B}\right)^2 t^2 - \frac{2I_P^2 t}{t_B}, 0 < t < t_B$$

The expression for unknown interval t_B is given in the steady state analysis presented in chapter 2. The RMS current is given by,

$$I_{RMS} = \sqrt{\frac{1}{T_S}\int_0^{T_S} I^2(t)\,dt}$$

Substituting $I^2(t)$,

$$I_{RMS} = \sqrt{\frac{1}{T_S}\left[\int_0^{t_B}\left(I_P{}^2 + \left(\frac{I_P}{t_B}\right)^2 t^2 - \frac{2I_P^2 t}{t_B}\right)dt\right]}$$

Minimising further, the RMS current equation of the HV side diode can be obtained as,

$$I_{RMS} = \sqrt{\frac{1}{T_S}\left[\frac{I_P{}^2 t_B}{3}\right]} \tag{A.5}$$

A.3.3 LV side transistor RMS current derivation

The LV side transistor current waveform during charging mode has triangular wave shape. Considering the effective interval, the instantaneous current is given by,

$$I(t) = \frac{I_{L1}}{\frac{dT_S}{2} - t_B} t, 0 < t < \frac{dT_S}{2} - t_B$$

Squaring the current gives,

$$I^2(t) = \left(\frac{I_{L1}}{\frac{dT_S}{2} - t_B}\right)^2 t^2, 0 < t < \frac{dT_S}{2} - t_B$$

Estimating the RMS value over a cycle,

$$I_{RMS} = \sqrt{\frac{1}{T_S}\left[\int_0^{\frac{dT_S}{2}-t_B}\left(\frac{I_{L1}}{\frac{dT_S}{2}-t_B}\right)^2 t^2 dt\right]}$$

Simplifying further, the RMS current equation of the LV transistor is given as,

$$I_{RMS} = \sqrt{\frac{1}{T_S}\left[\frac{(I_{L1})^2\left(\frac{dT_S}{2}-t_B\right)}{3}\right]} \tag{A.6}$$

A.3.4 LV side diode RMS current derivation

The instantaneous LV side diode current over the effective intervals is given by,

$$I(t) = I_{L1} + \frac{I_r}{\frac{T_S}{2} - \frac{dT_S}{2}} t, 0 < t < \frac{T_S}{2} - \frac{dT_S}{2}$$

$$= I_P - \frac{I_P t}{t_B}, 0 < t < t_B$$

Squaring the currents over the intervals gives,

$$I^2(t) = {I_{L1}}^2 + \left(\frac{I_r}{\frac{T_S}{2} - \frac{dT_S}{2}} \right)^2 t^2 + \frac{2 I_{L1} I_r t}{\frac{T_S}{2} - \frac{dT_S}{2}}, 0 < t < \frac{T_S}{2} - \frac{dT_S}{2}$$

$$= {I_P}^2 + \left(\frac{I_P}{t_B} \right)^2 t^2 - \frac{2 {I_P}^2 t}{t_B}, 0 < t < t_B$$

Then substituting the squared current to find RMS equation,

$$I_{RMS} = \sqrt{\frac{1}{T_S} \int_0^{T_S} I^2(t)\, dt}$$

$$I_{RMS} = \sqrt{\frac{1}{T_S} \left[\int_0^{\frac{T_S}{2} - \frac{dT_S}{2}} \left({I_{L1}}^2 + \left(\frac{I_r}{\frac{T_S}{2} - \frac{dT_S}{2}} \right)^2 t^2 + \frac{2 I_{L1} I_r t}{\frac{T_S}{2} - \frac{dT_S}{2}} \right) dt + \int_0^{t_B} \left({I_P}^2 + \left(\frac{I_P}{t_B} \right)^2 t^2 - \frac{2 I_P^2 t}{t_B} \right) dt \right]}$$

Deducing further,

$$I_{RMS} = \sqrt{\frac{1}{T_S} \left[\left(\frac{T_S}{2} - \frac{dT_S}{2} \right) \left({I_{L1}}^2 + \frac{{I_r}^2}{3} + I_{L1} I_r \right) + \frac{(I_P)^2 t_B}{3} \right]} \qquad \text{(A.7)}$$

A.4 Transformer/Inductor RMS current derivation for discharging mode

Figure A.2 illustrates the transformer current waveform during the discharging mode of the ultracapacitor. The waveform is symmetrical and periodic over a cycle. The instantaneous current over a half cycle can then be expressed as,

$$I(t) = \frac{I_P}{\frac{dT_S}{2} - t_B} t, 0 < t < \frac{dT_S}{2} - t_B$$

$$= I_P - \frac{I_r t}{\frac{T_S}{2} - t_B}, \frac{dT_S}{2} - t_B < t < \frac{T_S}{2} - t_B$$

$$= I_{L1} - \frac{I_{L1} t}{\frac{T_S}{2}}, \frac{T_S}{2} - t_B < t < \frac{T_S}{2}$$

Changing the limits to their effective interval for simplification,

$$I(t) = \frac{I_P}{\frac{dT_S}{2} - t_B} t, 0 < t < \frac{dT_S}{2} - t_B$$

$$= I_P - \frac{I_r t}{\frac{T_S}{2} - \frac{dT_S}{2}}, 0 < t < \frac{T_S}{2} - \frac{dT_S}{2}$$

$$= I_{L1} - \frac{I_{L1} t}{t_B}, 0 < t < t_B$$

Squaring the transformer current over the intervals gives,

$$I^2(t) = \left(\frac{I_P}{\frac{dT_S}{2} - t_B} \right)^2 t^2, 0 < t < \frac{dT_S}{2} - t_B$$

$$= {I_P}^2 + \left(\frac{I_r}{\frac{T_S}{2} - \frac{dT_S}{2}} \right)^2 t^2 - \frac{2 I_P I_r t}{\frac{T_S}{2} - \frac{dT_S}{2}}, 0 < t < \frac{T_S}{2} - \frac{dT_S}{2}$$

$$= {I_{L1}}^2 + \left(\frac{I_{L1}}{t_B} \right)^2 t^2 - \frac{2 {I_{L1}}^2 t}{t_B}, 0 < t < t_B$$

Then the RMS current is,

$$I_{RMS} = \sqrt{\frac{2}{T_S} \int_0^{\frac{T_S}{2}} I^2(t)\, dt}$$

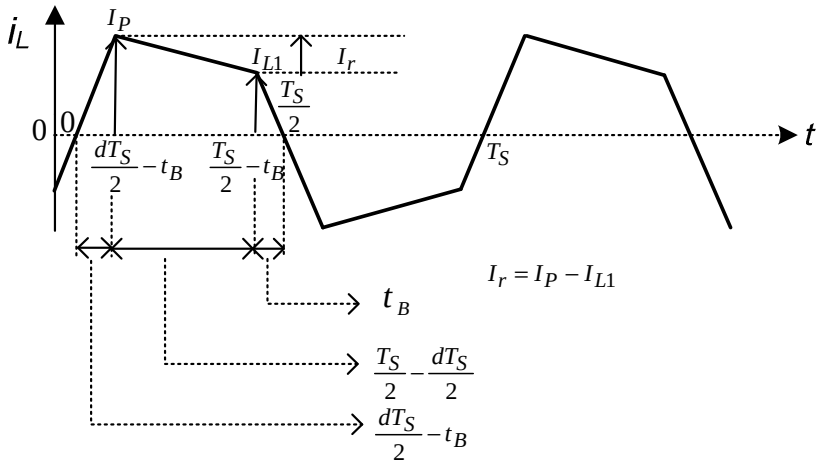

Figure A.2 Transformer current waveform during the discharging mode

Substituting $I^2(t)$ in the above equation,

$$I_{RMS}=\sqrt{\frac{2}{T_S}\left[\int_0^{\frac{dT_S}{2}-t_B}\left(\frac{I_P}{\frac{dT_S}{2}-t_B}\right)^2 t^2dt+\int_0^{\frac{T_S}{2}-\frac{dT_S}{2}}\left(I_P{}^2+\left(\frac{I_r}{\frac{T_S}{2}-\frac{dT_S}{2}}\right)^2 t^2-\frac{2I_PI_rt}{\frac{T_S}{2}-\frac{dT_S}{2}}\right)dt+\int_0^{t_B}\left(I_{L1}{}^2+\left(\frac{I_{L1}}{t_B}\right)^2 t^2-\frac{2I_{L1}^2t}{t_B}\right)dt\right]}$$

Further minimisations results in the final expression for transformer RMS current as,

$$I_{RMS}=\sqrt{\frac{2}{T_S}\left[\frac{(I_P)^2\left(\frac{dT_S}{2}-t_B\right)}{3}+\left(\frac{T_S}{2}-\frac{dT_S}{2}\right)\left(I_P{}^2+\frac{I_r{}^2}{3}-I_PI_r\right)+\frac{I_{L1}{}^2t_B}{3}\right]} \quad \text{(A.8)}$$

Figure A.3 shows the SABER simulation circuit diagram with all circuit parameters used to obtain the simulation results of Chapter 2.

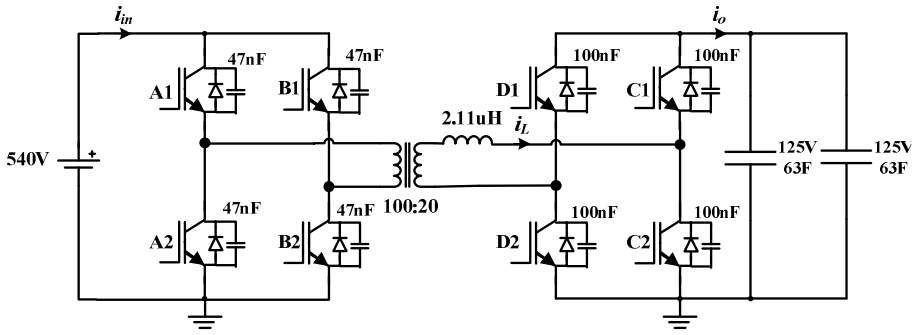

Figure A.3 Schematic of DAB converter with component values used in SABER simulation

Appendix B
Mathematical Analysis of Quasi-Square-Wave Mode of DAB DC-DC Converter

B.1 Mathematical analysis for quasi-square-wave on transformer primary

The waveform analysis for quasi-square-wave mode of the DAB converter is presented in this Appendix. In square-wave mode, the current at HV switching instant is the same for all the HV devices and the current at LV switching instant is the same for all the LV devices. However, during quasi-square-wave mode by introducing dead-time, the current at HV/LV switching instants differ for the devices on HV/LV sides depending on whether quasi-square-wave is introduced on transformer primary or transformer secondary or transformer primary and secondary. Hence, the device switching instants are named as HV leading/lagging transistor on the HV side and LV leading/lagging transistor on the LV side for explanation purpose.

B.1.1 Buck mode

The analysis is performed based on the following steps considering power is transferred from transformer primary to secondary (charging mode) for buck ($nV_{in} > V_o$) and boost ($nV_{in} < V_o$) modes of operation of the converter. However, for discharging mode the variation in the expressions of the analysis are mentioned in all the sections of this Appendix for the sake of clarity.

1. From the geometry of the converter current waveform, current at various switching instants were identified and labelled.
2. Voltage across the inductor L over a half cycle is analysed to determine the peak-to-peak change in the inductor current. Then the expressions were derived for the inductor current at various switching instants.

3. Area under the ultracapacitor charging/discharging current waveform was then shaded and named.
4. Shaded regions of the ultracapacitor current waveform are averaged to obtain the average output current.

Analysis is performed based on the assumption of loss-less components and a piece-wise linear waveform for i_L. Let V_L be the voltage across the inductor and i_L be the current flowing through the inductor, L. The waveforms depicted by Figure. B.1 is for buck mode of operation. For a half cycle,

$$\int V_L dt = (nV_{in} + V_o)\frac{dT_S}{2} + (nV_{in} - V_o)\left(\frac{T_S}{2} - \frac{\delta T_S}{2} - \frac{dT_S}{2}\right) - V_o\frac{\delta T_S}{2}$$

$$= \frac{T_S}{2}\left[nV_{in}(1-\delta) + V_o(2d-1)\right]$$

where d is the duty ratio, n is the turns ratio, T_S is the switching time period for a cycle and δ is the dead-time introduced in the transformer primary voltage. During this half cycle, inductor current change from $-I_{L2}$ to $+I_{L2}$.

Therefore, peak-to-peak change in current $I_{L2PP} = \frac{\int V_L dt}{L}$

$$= \frac{T_S}{2L}\left[nV_{in}(1-\delta) + V_o(2d-1)\right]$$

Therefore, the current at the HV lagging transistor switching instant I_{L2} is given by,

$$I_{L2} = \frac{T_S}{4L}\left[nV_{in}(1-\delta) + V_o(2d-1)\right] \quad \text{(B.1)}$$

Solving for the LV switching instant current based on the current slope during the interval $\frac{dT_S}{2}$ gives,

$$I_{L1} = \left(\frac{(nV_{in} + V_o)}{L}\right)\frac{dT_S}{2} - I_{L2}$$

Substituting (B.1) in the above equation, the expression for LV switching instant current I_{L1} can be obtained as,

$$I_{L1} = \frac{T_S}{4L}\left[nV_{in}(2d-1+\delta) + V_o\right] \quad \text{(B.2)}$$

The current change during the interval $\left(\frac{T_S}{2}-\frac{\delta T_S}{2}-\frac{dT_S}{2}\right)$ where the current is increased from I_{L1} to I_P can be written as,

$$=\frac{(nV_{in}-V_o)}{L}\left(\frac{T_S}{2}-\frac{\delta T_S}{2}-\frac{dT_S}{2}\right)$$

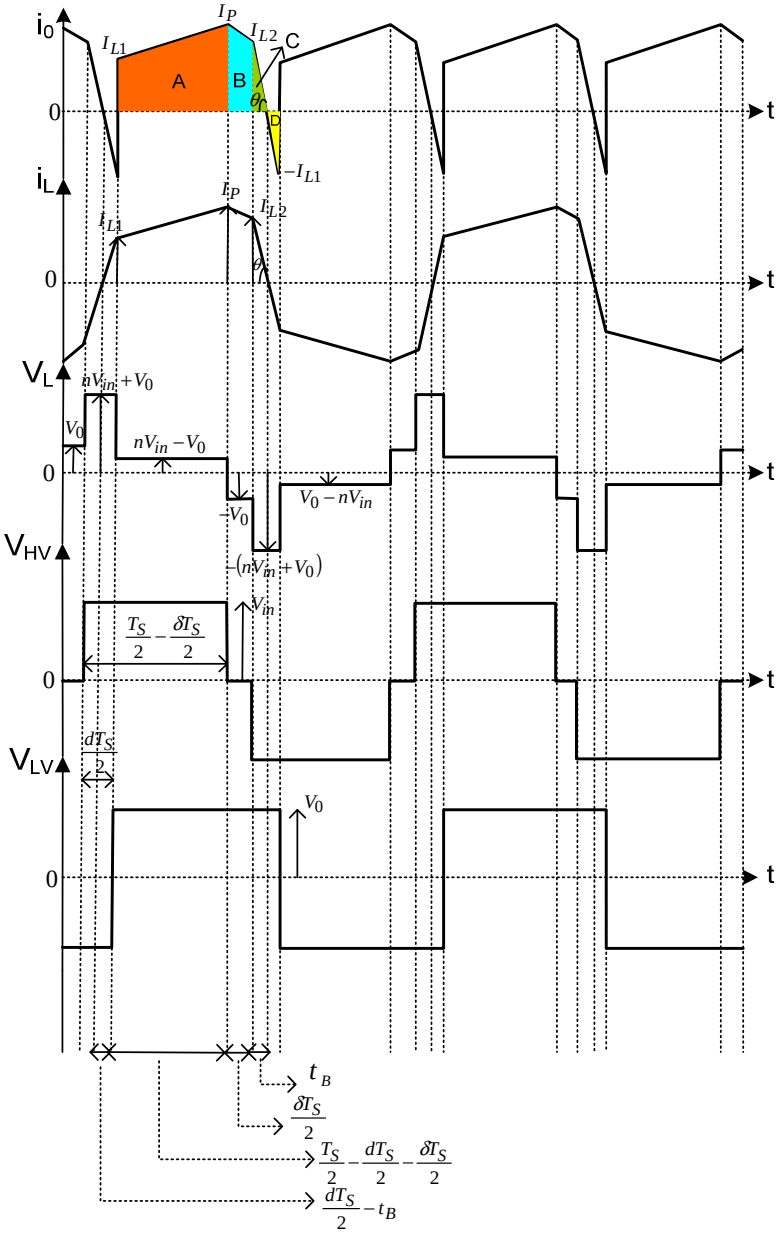

Figure B.1 AC-link voltage and current waveforms with quasi-square-wave on transformer primary ($nV_{in} > V_o$)

Now solving for the HV leading transistor switching instant current gives,

$$I_P = \frac{T_S}{4L}\left[nV_{in}(1-\delta)+V_o(2d-1+2\delta)\right] \tag{B.3}$$

In order to find the average output (ultracapacitor) current, the expression is required for the interval t_B; the time taken for i_L to fall to zero following the HV lagging transistor switching instant. Since the output current waveform is piece-wise linear, this can be calculated from the following,

From Figure B.1,

$$\frac{I_{L2}+I_{L1}}{\frac{dT_S}{2}} = \frac{I_{L2}}{t_B} = \tan\theta \tag{B.4}$$

where θ is the angle marked on the i_0 and i_L current waveforms shown in Figure B.1. The total current change during the interval $\frac{dT_S}{2}$, where the current is increased from $-I_{L2}$ to $+I_{L1}$ can be written as,

$$I_{L2}+I_{L1} = \left(\frac{(nV_{in}+V_o)}{L}\right)\frac{dT_S}{2} \tag{B.5}$$

Substituting (B.1) and (B.5) in (B.4), then solving for t_B gives,

$$t_B = \frac{T_S\left[nV_{in}(1-\delta)+V_o(2d-1)\right]}{4(nV_{in}+V_o)} \tag{B.6}$$

Using the above equations, the area under the i_0 current waveform shown as shaded regions in Figure B.1 is obtained. Since the waveform is periodic over half a cycle, dividing the area by the duration, which is $\frac{T_S}{2}$, gives the average output current of the DAB converter. The shaded regions marked as A, B, C and D in Figure B.1 are represented by,

$$A = \left(\frac{I_{L1}+I_P}{2}\right)\left(\frac{T_S}{2}-\frac{\delta T_S}{2}-\frac{dT_S}{2}\right)$$

$$B = \left(\frac{I_P+I_{L2}}{2}\right)\frac{\delta T_S}{2}$$

$$C = \frac{t_B I_{L2}}{2}$$

$$D = \frac{1}{2}\left(\frac{dT_S}{2}-t_B\right)I_{L1}$$

Then the average output current, $I_o = \dfrac{A+B+C-D}{\frac{T_S}{2}}$

Averaging A and B terms will give,

$$\frac{A+B}{\frac{T_S}{2}} = \frac{T_S}{4L}\left[nV_{in}(d+\delta-d\delta-\delta^2-d^2)+V_o(d-d^2)\right] \quad \text{(B.7)}$$

Averaging C and D terms will result in

$$\frac{C-D}{\frac{T_S}{2}} = \frac{-nV_{in}d\delta T_S}{4L}+\frac{V_o d^2 T_S}{4L}-\frac{nV_{in}d^2T_S}{4L}+\frac{nV_{in}dT_S}{8L}-\frac{V_o dT_S}{8L}+\frac{T_S}{16L(nV_{in}+V_o)}(2nV_{in}^2d-2V_o^2d) \quad \text{(B.8)}$$

Finally adding (B.7) and (B.8) and simplifying further, the equation for the average output current can be obtained as follows.

$$I_o = \frac{nV_{in}T_S}{2L}\left(d-d^2-d\delta+\frac{\delta}{2}-\frac{\delta^2}{2}\right) \quad \text{(B.9)}$$

Normalising the average output current by the base value $\frac{nV_{in}T_S}{2L}$ gives,

Normalised average output current $I_o^{'} = \left(d-d^2-d\delta+\frac{\delta}{2}-\frac{\delta^2}{2}\right)$ (B.10)

A similar analysis may be undertaken for the discharging mode, that is when power is transferred from the secondary LV side to the primary HV side. The corresponding expressions for the currents at the HV and LV switching instants, (I_{L2}, I_P) and I_{L1} respectively in (B.1), (B.3) and (B.2) are unchanged. However in the expressions for i_0, the secondary side terminal current, the term within brackets in equations (B.9) and (B.10) would be multiplied by 'minus' sign to signify the reverse power flow.

B.1.1.1 Condition for ZVS:

By applying the zero-voltage switching conditions (mentioned in Chapter 2) to the device current waveforms shown in Figure C.1, the current at the LV switching instant must be greater than zero to achieve ZVS in the LV bridge. Therefore using (B.2), the following

condition must be satisfied for ZVS in the LV bridge:

$$I_{L1} = \frac{T_S}{4L}\left[nV_{in}(2d - 1 + \delta) + V_o\right] \geq 0 \tag{B.11}$$

Solving for the inequality given in (B.11), the duty ratio at which ZVS occurs can be obtained as,

$$d \geq 0.5 - \frac{\delta}{2} - \frac{V_0^{'}}{2} \tag{B.12}$$

Where $V_0^{'}$ is the normalized voltage conversion ratio and is given by $V_0^{'} = \frac{V_0}{nV_{in}}$

Equation (B.12) is applicable when $V_0^{'} < 1$. To achieve ZVS in the HV bridge, the current at the HV lagging transistor switching instant given in (B.1) must be positive. However, this condition is normally achieved and the limiting condition for ZVS is that given in (B.12).

B.1.2 Boost mode

Similar analysis is undertaken to derive the mathematical model for boost ($nV_{in} < V_o$) mode of operation, where the power flows from transformer primary (LV) side to the secondary (HV) side with quasi-square-wave applied on transformer primary. Expression for the inductor current at various switching instants I_{L1}, I_{L2}, I_P shown in Figure B.2 are given by,

The current at the LV leading transistor switching instant is expressed as,

$$I_{L1} = \frac{T_S}{4L}\left[nV_{in}(1 - \delta) + V_o(2d - 1 + 2\delta)\right] \tag{B.13}$$

The current at the LV lagging transistor switching instant is expressed as,

$$I_{L2} = \frac{T_S}{4L}\left[nV_{in}(1 - \delta) + V_o(2d - 1)\right] \tag{B.14}$$

The current at the HV switching instant can be given as,

$$I_P = \frac{T_S}{4L}\left[nV_{in}(2d - 1 + \delta) + V_o\right] \tag{B.15}$$

In order to find the average output (ultracapacitor) current, the expression is required for the interval t_B; the time taken for i_L to fall to zero following the LV lagging transistor switching instant. Since the output current waveform is piece-wise linear, this can be derived as,

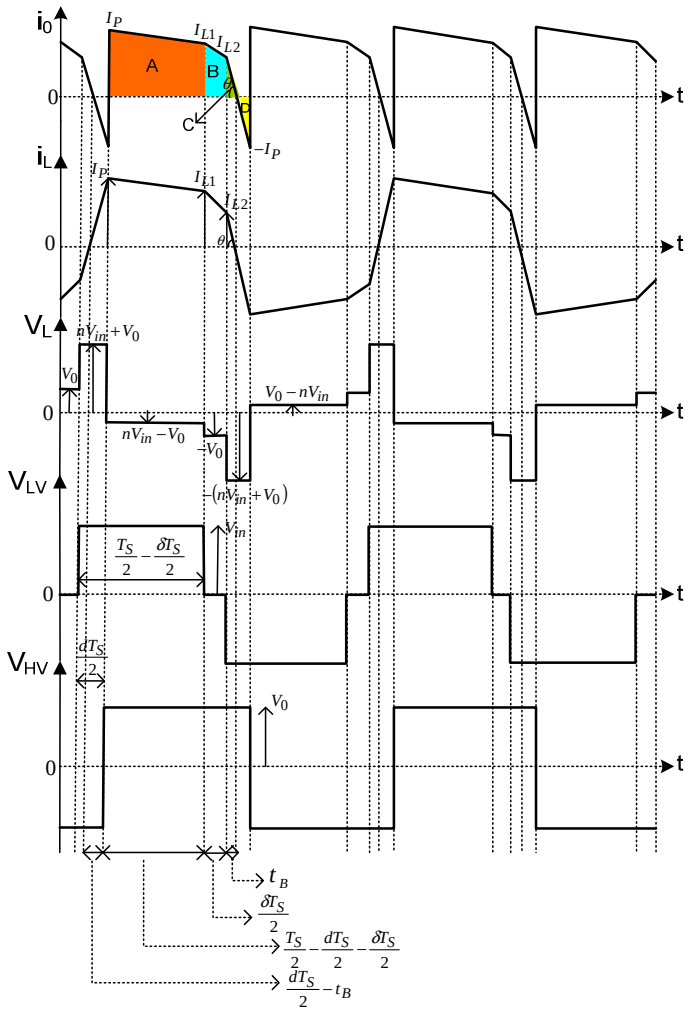

Figure B.2 AC-link voltage and current waveforms with quasi-square-wave on transformer primary ($nV_{in} < V_o$)

$$t_B = \frac{T_S\left[nV_{in}(1-\delta)+V_o(2d-1)\right]}{4\left(nV_{in}+V_o\right)} \tag{B.16}$$

Using the above equations, the area under the i_0 current waveform shown as shaded regions in Figure B.2 is obtained. Since the waveform is periodic over half a cycle, dividing the area by the duration, which is $\frac{T_S}{2}$, gives the average output current of the DAB converter.

The shaded regions marked as A, B, C and D in Figure B.2 are represented by,

$$A=\left(\frac{I_{L1}+I_P}{2}\right)\left(\frac{T_S}{2}-\frac{\delta T_S}{2}-\frac{dT_S}{2}\right)$$

$$B = \left(\frac{I_{L1} + I_{L2}}{2} \right) \frac{\delta T_S}{2}$$

$$C = \frac{t_B I_{L2}}{2}$$

$$D = \frac{1}{2} \left(\frac{dT_S}{2} - t_B \right) I_P$$

Then the average output current can be obtained as,

$$I_o = \frac{A + B + C - D}{\frac{T_S}{2}}$$

Grouping $\frac{T_S}{2}$ term together in the above expressions for A, B, D and then averaging gives,

$$= \frac{T_S}{4L} \left[\frac{3nV_{in}d}{2} - 2nV_{in}d^2 - \frac{3nV_{in}d\delta}{2} + nV_{in}\delta - nV_{in}\delta^2 - V_o d^2 + \frac{V_o d}{2} \right] \quad \text{(B.17)}$$

Then grouping the remaining t_B expressions in C and D terms and then averaging,

$$= \frac{V_o d^2 T_S}{4L} - \frac{nV_{in} d\delta T_S}{8L} + \frac{T_S}{16L(nV_{in} + V_o)} (2nV_{in}^2 d - 2V_o^2 d) \quad \text{(B.18)}$$

Expression for the average output current is obtained by adding (B.17) and (B.18) and then reducing it further,

$$I_o = \frac{nV_{in}T_S}{2L} \left(d - d^2 - d\delta + \frac{\delta}{2} - \frac{\delta^2}{2} \right) \quad \text{(B.19)}$$

Normalising the average output current by the base value $\frac{nV_{in}T_S}{2L}$ gives the normalised average output current, which can be written as,

$$I_o^{'} = \left(d - d^2 - d\delta + \frac{\delta}{2} - \frac{\delta^2}{2} \right) \quad \text{(B.20)}$$

B.1.2.1 Condition for ZVS:

By applying the zero-voltage switching conditions to the device current waveforms shown in Figure C.2, the current at the LV lagging transistor switching instant must be greater than zero to achieve ZVS in the LV bridge. Therefore using (B.14), the following condition must be

satisfied for ZVS in the LV bridge:

$$I_{L2} = \frac{T_S}{4L}\left[nV_{in}(1-\delta) + V_o(2d-1)\right] \geq 0 \tag{B.21}$$

Solving for the inequality given in (B.21), the duty ratio at which ZVS occurs can be obtained as,

$$d \geq 0.5 - \frac{0.5}{V_o^{'}}(1-\delta) \tag{B.22}$$

Where $V_o^{'}$ is the normalized voltage conversion ratio and $V_0^{'} = \frac{V_0}{nV_{in}}$

To achieve ZVS for the leading transistor in the LV bridge, the current given by (B.13) must be positive. However, this condition occurs later than the LV lagging transistor switching instant. Hence, the limiting condition for the LV bridge is determined by (B.22). To achieve ZVS in the HV bridge, the current at the HV switching instant given in (B.15) must be positive. However, this condition is normally achieved and the limiting condition for ZVS is that given in (B.22).

During power reversal, when the converter operates in the discharging mode (Power is transferred from the secondary side to the primary side), the zero-voltage switching limit is again found to occur in the LV bridge and may again be expressed by (B.11), (B.12), (B.21) and (B.22).

B.2 Mathematical analysis for quasi-square-wave on transformer secondary

B.2.1 Buck mode

Similar analysis is undertaken for quasi-square-wave on transformer secondary considering power flows from the transformer primary to secondary side for buck ($nV_{in} > V_o$) and boost ($nV_{in} < V_o$) modes. The notation used in the following analysis is indicated in Figure B.3. Considering V_L over a half cycle,

$$\int V_L dt = (nV_{in} + V_o)\frac{dT_S}{2} + nV_{in}\frac{\delta T_S}{2} + (nV_{in} - V_o)\left(\frac{T_S}{2} - \frac{\delta T_S}{2} - \frac{dT_S}{2}\right)$$

$$= \frac{T_S}{2}\left[nV_{in} + V_o(2d + \delta - 1)\right]$$

During the half cycle, the inductor current changes from $-I_P$ to $+I_P$. The peak-to-peak change in the inductor current I_{PP} is given by,

$$I_{PP} = \frac{\int V_L \, dt}{L}$$

$$= \frac{T_S}{2L}\left[nV_{in} + V_o(2d + \delta - 1)\right]$$

The current at HV switching instant I_P is given by,

$$I_P = \frac{T_S}{4L}\left[nV_{in} + V_o(2d + \delta - 1)\right] \tag{B.23}$$

Solving for the LV leading transistor switching instant current based on the current slope during the interval $\frac{dT_S}{2}$ gives,

$$I_{L1} = \left(\frac{\left(nV_{in} + V_o\right)}{L}\right)\frac{dT_S}{2} - I_P$$

Substituting (B.23) in the above equation and minimising further gives,

$$I_{L1} = \frac{T_S}{4L}\left[nV_{in}(2d - 1) + V_o(1 - \delta)\right] \tag{B.24}$$

Current change during the interval $\frac{\delta T_S}{2}$, where the current is increased from I_{L1} to I_{L2} can be written as,

$$\therefore I_{L2} = I_{L1} + \frac{nV_{in}\delta T_S}{2L}$$

Substituting (B.24) in the above equation and simplifying further gives the expression for LV lagging transistor switching instant current as,

$$I_{L2} = \frac{T_S}{4L}\left[nV_{in}(2d - 1 + 2\delta) + V_o(1 - \delta)\right] \tag{B.25}$$

In order to find the average output (ultracapacitor) current, the expression is required for the interval t_B; the time taken for i_L to fall to zero following the HV switching instant. Since the output current waveform is piece-wise linear, this can be calculated from the following,

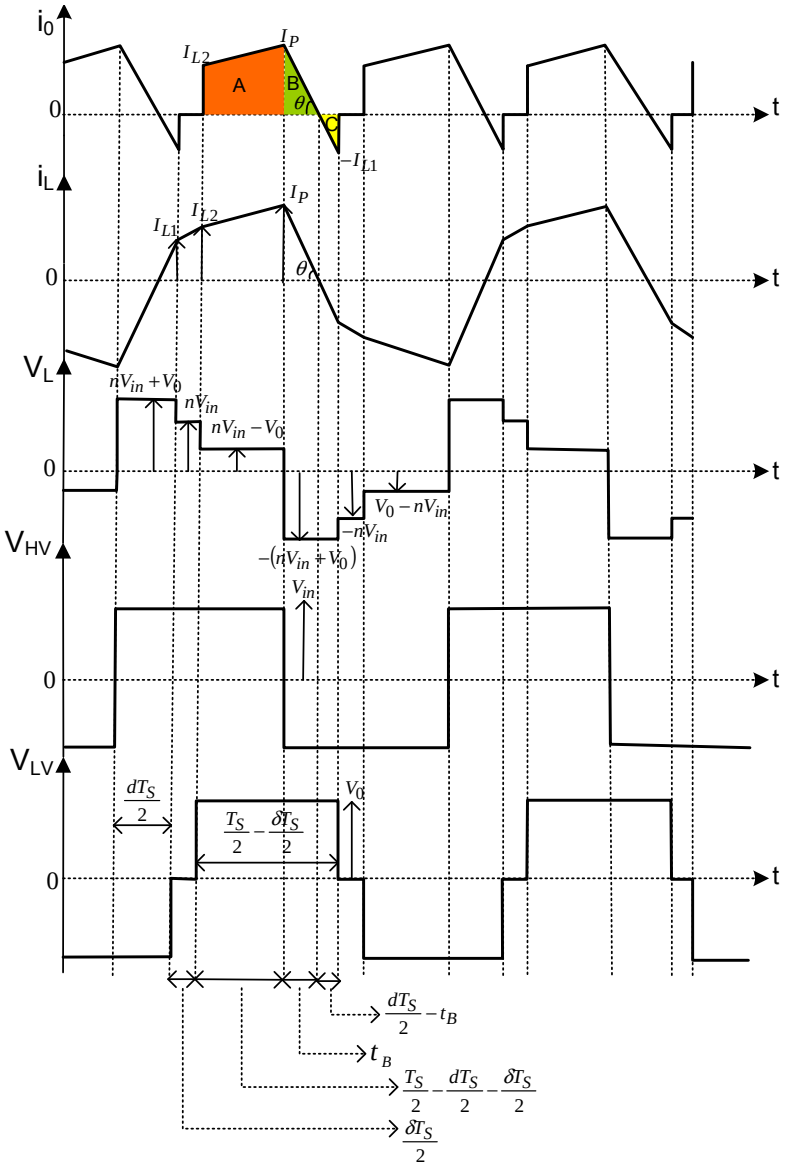

Figure B.3 AC-link voltage and current waveforms with quasi-square-wave on transformer secondary

$$nV_{in} > V_o$$

$$\frac{I_P + I_{L1}}{\frac{dT_S}{2}} = \frac{I_P}{t_B} = \tan\theta \tag{B.26}$$

where θ is the angle marked on the i_0 and i_L current waveforms shown in Figure B.3. The total current change during the interval $\frac{dT_S}{2}$, where the current is increased from -I_P to +I_{L1} can be written as,

$$I_P + I_{L1} = \left(\frac{(nV_{in} + V_o)}{L}\right)\frac{dT_S}{2} \tag{B.27}$$

Substituting (B.23) and (B.27) in (B.26), then solving for t_B gives,

$$t_B = \frac{T_S\left[nV_{in} + V_o(2d + \delta - 1)\right]}{4(nV_{in} + V_o)}$$

Using the above equations, the area under the i_0 current waveform shown as shaded regions in Figure B.3 is obtained. Since the waveform is periodic over half a cycle, dividing the area by the duration, which is $\frac{T_S}{2}$, gives the average output current of the DAB converter. The shaded regions marked as A, B, and C in Figure B.3 are represented by,

$$A = \left(\frac{I_{L2} + I_P}{2}\right)\left(\frac{T_S}{2} - \frac{\delta T_S}{2} - \frac{dT_S}{2}\right)$$

$$B = \frac{t_B I_P}{2}$$

$$C = \frac{1}{2}\left(\frac{dT_S}{2} - t_B\right)I_{L1}$$

Then the average output current can be obtained as,

$$I_o = \frac{A + B - C}{\frac{T_S}{2}}$$

Substituting the values of A, B and C terms in the average output current equation and grouping the $\frac{T_s}{2}$ terms alone together and subsequently averaging,

$$= \frac{T_S}{4L}\left[\frac{3nV_{in}d}{2} + nV_{in}\delta - 2nV_{in}d^2 - 2nV_{in}d\delta - nV_{in}\delta^2 - \frac{V_o d\delta}{2} + \frac{V_o d}{2} - V_o d^2\right] \tag{B.28}$$

Grouping the remaining t_B terms and averaging gives,

$$= \frac{T_S}{16L(nV_{in} + V_o)}(2nV_{in}^2 d + 4V_o^2 d^2 + 2V_o^2 d\delta - 2V_o^2 d + 4nV_{in}V_o d^2 + 2nV_{in}V_o d\delta) \tag{B.29}$$

Adding (B.28) and (B.29) and simplifying further, the expression for average output current can be obtained as,

$$I_o = \frac{nV_{in}T_S}{2L}\left(d - d^2 - d\delta + \frac{\delta}{2} - \frac{\delta^2}{2}\right) \tag{B.30}$$

Normalising the average output current by the base value $\frac{nV_{in}T_S}{2L}$ gives,

$$I_o^{'} = \left(d - d^2 - d\delta + \frac{\delta}{2} - \frac{\delta^2}{2} \right) \tag{B.31}$$

A similar analysis may be undertaken for the discharging mode, that is when power is transferred from the secondary LV side to the primary HV side. The corresponding expressions for the currents at the HV and LV switching instants, I_P and (I_{L1}, I_{L2}) respectively in (B.23) and (B.24), (B.25) are unchanged. However in the expressions for i_0, the secondary side terminal current, the term within brackets in equations (B.30) and (B.31) would be multiplied by 'minus' sign to signify the reverse power flow.

B.2.1.1 Condition for ZVS:

By applying the zero-voltage switching conditions to the device current waveforms shown in Figure C.3, the current at the LV leading transistor switching instant must be greater than zero to achieve ZVS in the LV bridge. Therefore using (B.24), the following condition must be satisfied for ZVS in the LV bridge:

$$I_{L1} = \frac{T_S}{4L}\left[nV_{in}(2d-1) + V_O(1-\delta)\right] \geq 0 \tag{B.32}$$

Solving for the inequality given in (B.32), the duty ratio at which ZVS occurs can be obtained as,

$$d \geq 0.5 - \frac{V_o^{'}}{2}(1-\delta) \tag{B.33}$$

Where $V_o^{'}$ is the normalized voltage conversion ratio and $V_0^{'} = \frac{V_0}{nV_{in}}$

To achieve ZVS for the lagging transistor in the LV bridge, the current given in (B.25) must be positive. However, this condition occurs later than the LV leading transistor switching instant. Hence, the limiting condition for the LV bridge is determined by (B.33). To achieve ZVS in the HV bridge, the current at the HV switching instant given in (B.23) must be positive. However, this condition is normally achieved and the limiting condition for ZVS is that given in (B.33).

B.2.2 Boost mode

Similar analysis is undertaken to derive the mathematical model for boost ($nV_{in} < V_o$) mode of operation, where the power flows from transformer primary (LV) side to the secondary (HV) side with quasi-square-wave applied on transformer secondary. Expression for the inductor current at various switching instants I_{L1}, I_{L2}, I_P shown in Figure B.4 are given by,

The current at HV leading transistor switching instant is expressed as,

$$I_{L1} = \frac{T_S}{4L}\left[nV_{in}(2d-1)+V_o(1-\delta)\right] \tag{B.34}$$

The current at HV lagging transistor switching instant is expressed as,

$$I_P = \frac{T_S}{4L}\left[nV_{in}(2d-1+2\delta)+V_o(1-\delta)\right] \tag{B.35}$$

The current at LV switching instant is expressed as,

$$I_{L2} = \frac{T_S}{4L}\left[nV_{in}+V_o(2d+\delta-1)\right] \tag{B.36}$$

In order to find the average output (ultracapacitor) current, the expression is required for the interval t_B; the time taken for i_L to fall to zero following the LV switching instant. Since the output current waveform is piece-wise linear, this can be derived as,

$$t_B = \frac{T_S\left[nV_{in}+V_o(2d+\delta-1)\right]}{4(nV_{in}+V_o)} \tag{B.37}$$

Using the above equations, the area under the i_0 current waveform shown as shaded regions in Figure B.4 is obtained. Since the waveform is periodic over half a cycle, dividing the area by the duration, which is $\frac{T_S}{2}$, gives the average output current of the DAB converter.

The shaded areas A, B and C marked in Figure B.4 are given by,

$$A = \left(\frac{I_{L2}+I_P}{2}\right)\left(\frac{T_S}{2}-\frac{\delta T_S}{2}-\frac{dT_S}{2}\right)$$

$$B = \frac{t_B I_{L2}}{2}$$

$$C = \frac{1}{2}\left(\frac{dT_S}{2}-t_B\right)I_{L1}$$

Then the average output current can be obtained by,

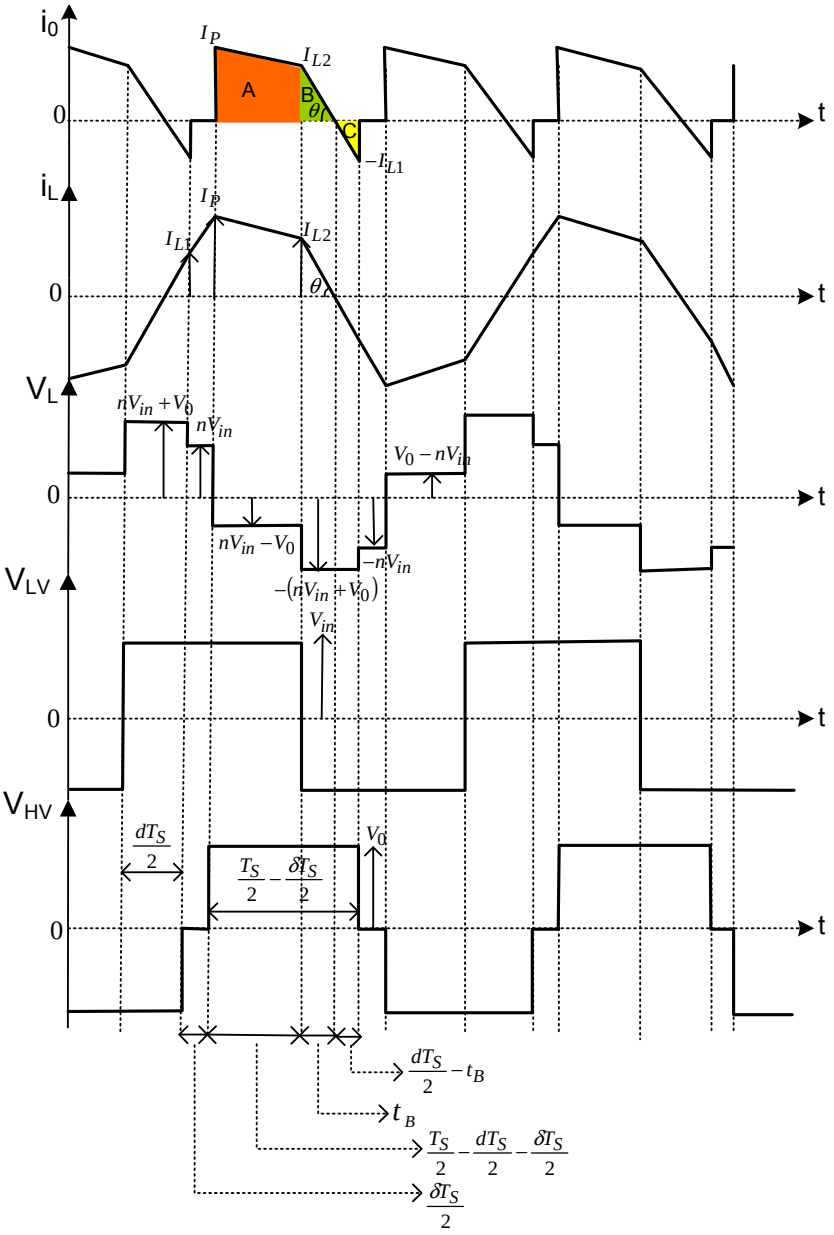

Figure B.4 AC-link voltage and current waveforms with quasi-square-wave on transformer secondary ($nV_{in} < V_o$)

$$I_o = \frac{A+B-C}{\frac{T_S}{2}}$$

Substituting the expressions for A, B and C terms in the average output current and simplifying, the final expression for the average output current is obtained as follows,

$$I_o = \frac{nV_{in}T_S}{2L}\left(d - d^2 - d\delta + \frac{\delta}{2} - \frac{\delta^2}{2}\right) \quad \text{(B.38)}$$

Normalising the average output current by the base $\frac{nV_{in}T_S}{2L}$ value gives,

$$I_o^{'} = \left(d - d^2 - d\delta + \frac{\delta}{2} - \frac{\delta^2}{2}\right) \quad \text{(B.39)}$$

B.2.2.1 Condition for ZVS:

By applying the zero-voltage switching conditions to the device current waveforms shown in Figure C.4, the current at the LV switching instant must be greater than zero to achieve ZVS in the LV bridge. Therefore using (B.36), the following condition must be satisfied for ZVS in the LV bridge:

$$I_{L2} = \frac{T_S}{4L}\left[nV_{in} + V_o(2d + \delta - 1)\right] \geq 0 \quad \text{(B.40)}$$

Solving for the inequality given in (B.40), the duty ratio at which ZVS occurs can be obtained as,

$$d \geq 0.5 - \frac{\delta}{2} - \frac{0.5}{V_o^{'}} \quad \text{(B.41)}$$

To achieve ZVS in the HV bridge, the current at the HV leading transistor switching instant given in (B.34) must be positive. To achieve ZVS in the HV lagging transistor, the current given in (B.35) must be positive. This occurs later than HV leading transistor switching instant. Hence, limiting condition to achieve ZVS in the HV bridge is given by (B.34). However, this condition is normally achieved and the limiting condition for ZVS is that given in (B.41).

During power reversal, when the converter operates in the discharging mode (power flows from secondary side to primary side), the zero-voltage switching limit is again found to occur in the LV bridge and may again be expressed by (B.32), (B.33), (B.40) and (B.41).

B.3 Mathematical analysis for quasi-square-wave on transformer primary and secondary

B.3.1 Buck mode

In this section, analysis is undertaken for quasi-square-wave on transformer primary and secondary by considering power flow from the transformer primary to secondary side for buck ($nV_{in} > V_o$) and boost ($nV_{in} < V_o$) modes. In Figures B.5 and B.6, δ_i and δ_0 signify the dead-time on transformer primary and secondary sides respectively. The integral of voltage across the inductor *L* over a half cycle is given as,

$$\int V_L dt = (nV_{in} + V_o)\frac{dT_S}{2} + nV_{in}\frac{\delta_0 T_S}{2} + (nV_{in} - V_o)\left(\frac{T_S}{2} - \frac{dT_S}{2} - \frac{\delta_i T_S}{2} - \frac{\delta_0 T_S}{2}\right) - V_o\frac{\delta_i T_S}{2}$$

$$= \frac{T_S}{2}\left[nV_{in}(1-\delta_i) + V_o(2d + \delta_0 - 1)\right]$$

During the half cycle, the inductor current changes from $-I_{L3}$ to $+I_{L3}$. Therefore, peak-to-peak change in the inductor current I_{L3} is given by,

$$I_{L3PP} = \frac{T_S}{2L}\left[nV_{in}(1-\delta_i) + V_o(2d + \delta_0 - 1)\right]$$

The current at HV lagging transistor switching instant is expressed as,

$$I_{L3} = \frac{T_S}{4L}\left[nV_{in}(1-\delta_i) + V_o(2d + \delta_0 - 1)\right] \qquad \text{(B.42)}$$

Solving for the LV leading transistor switching instant current based on the current slope during the interval $\frac{dT_s}{2}$ gives,

$$\therefore I_{L1} = \left(\frac{(nV_{in} + V_o)}{L}\right)\frac{dT_S}{2} - I_{L3}$$

Substituting (B.42) in the above equation and further simplification gives the current at LV leading transistor switching instant as,

$$I_{L1} = \frac{T_S}{4L}\left[nV_{in}(2d + \delta_i - 1) + V_o(1-\delta_0)\right] \qquad \text{(B.43)}$$

Solving for the LV lagging transistor switching instant current based on the current slope during the interval $\frac{\delta T_S}{2}$ gives,

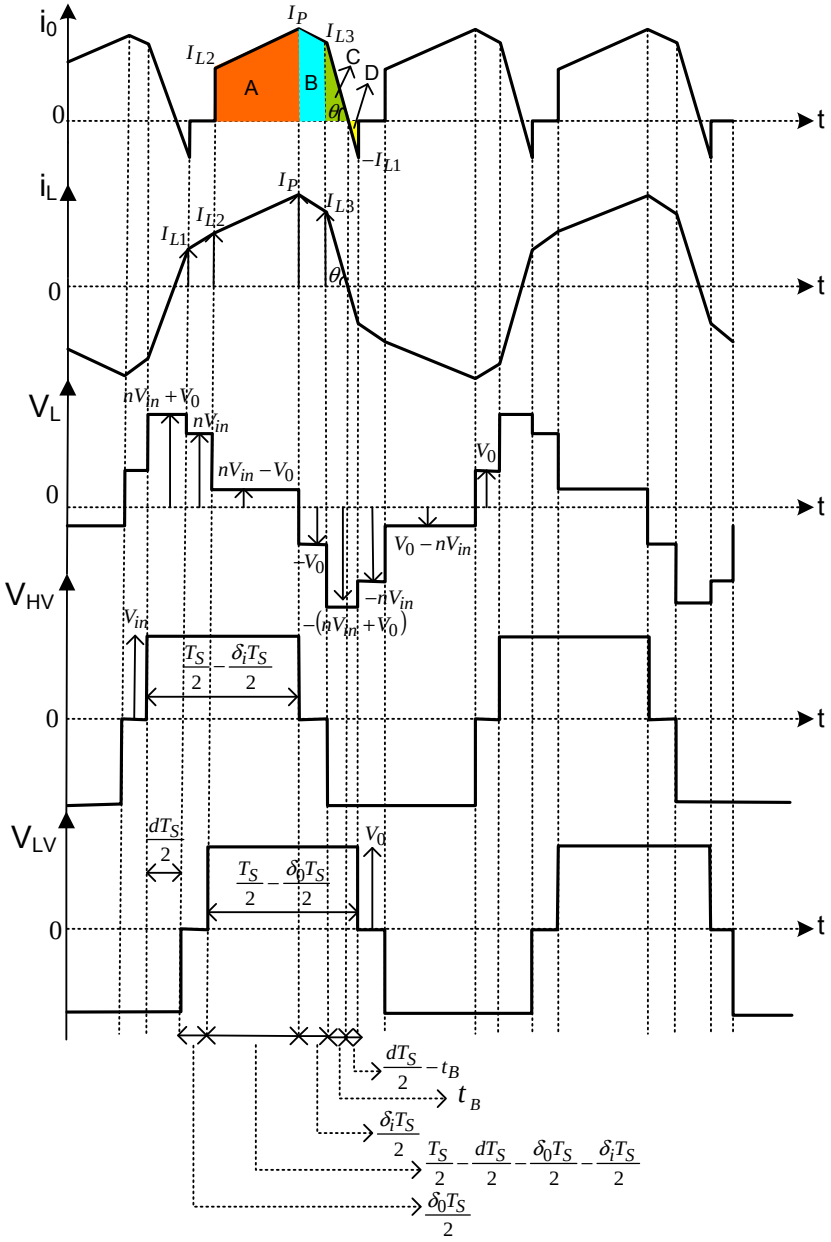

Figure B.5 AC-link voltage and current waveforms with quasi-square-wave on primary and secondary voltages $nV_{in} > V_o$

$$\therefore I_{L2} = I_{L1} + \frac{nV_{in}\delta_0 T_S}{2L}$$

Substituting (B.43) in the above equation and further reducing provides the LV lagging transistor switching instant as,

$$I_{L2} = \frac{T_S}{4L}\left[nV_{in}(2d + \delta_i + 2\delta_0 - 1) + V_o(1 - \delta_0)\right] \quad \text{(B.44)}$$

Similarly, solving for the HV leading transistor switching instant current based on the current slope during the interval $\left(\frac{T_S}{2} - \frac{dT_S}{2} - \frac{\delta_i T_S}{2} - \frac{\delta_0 T_S}{2}\right)$ gives,

$$I_P = I_{L2} + \frac{(nV_{in} - V_o)}{L}\left(\frac{T_S}{2} - \frac{dT_S}{2} - \frac{\delta_i T_S}{2} - \frac{\delta_0 T_S}{2}\right)$$

Substituting (B.44) in the above equation and simplifying gives HV leading transistor switching instant current as,

$$I_P = \frac{T_S}{4L}\left[nV_{in}(1 - \delta_i) + V_0(2d - 1 + \delta_0 + 2\delta_i)\right] \quad \text{(B.45)}$$

In order to find the average output (ultracapacitor) current, the expression is required for the interval t_B; the time taken for i_L to fall to zero following the HV lagging transistor switching instant. Since the output current waveform is piece-wise linear, this can be derived as,

$$t_B = \frac{T_S\left[nV_{in}(1 - \delta_i) + V_o(2d + \delta_0 - 1)\right]}{4(nV_{in} + V_o)} \quad \text{(B.46)}$$

Using the above equations, the area under the i_0 current waveform shown as shaded regions in Figure B.5 is obtained. Since the waveform is periodic over half a cycle, dividing the area by the duration, which is $\frac{T_S}{2}$, gives the average output current of the DAB converter.

Where the regions A, B, C and D in Figure B.5 are given by

$$A = \left(\frac{I_{L2} + I_P}{2}\right)\left(\frac{T_S}{2} - \frac{dT_S}{2} - \frac{\delta_i T_S}{2} - \frac{\delta_0 T_S}{2}\right)$$

$$B = \left(\frac{I_P + I_{L3}}{2}\right)\frac{\delta_i T_S}{2}$$

$$C = \frac{t_B I_{L3}}{2}$$

$$D = \frac{1}{2}\left(\frac{dT_S}{2} - t_B\right)I_{L1}$$

Average output current is then given as $I_o = \frac{A + B + C - D}{\frac{T_S}{2}}$

Substituting all the above terms in the average output current equation and grouping the $\frac{T_S}{2}$ terms alone, and then minimising,

$$=\frac{T_S}{8L}\left[3nV_{in}d+2nV_{in}\delta_0-4nV_{in}d^2-3nV_{in}d\delta_i-4nV_{in}d\delta_0+2nV_{in}\delta_i-2nV_{in}\delta_i^2-2nV_{in}\delta_i\delta_0-2nV_{in}\delta_0^2+V_od-2V_od^2-V_od\delta_0\right] \quad \text{(B.47)}$$

Now grouping the remaining t_B terms and further reducing,

$$=\frac{T_S}{16L(nV_{in}+V_o)}(2nV_{in}^2d-2nV_{in}^2d\delta_i+4V_o^2d^2+2V_o^2d\delta_0-2V_o^2d+4nV_{in}V_od^2+2nV_{in}V_0d\delta_0-2nV_{in}V_0d\delta_i) \quad \text{(B.48)}$$

Now adding (B.47) and (B.48) and simplifying further, the expression for average output current is obtained as follows.

$$I_o=\frac{nV_{in}T_S}{2L}\left(d-d^2-d\delta_i-d\delta_0+\frac{\delta_i}{2}+\frac{\delta_0}{2}-\frac{\delta_i^2}{2}-\frac{\delta_0^2}{2}-\frac{\delta_i\delta_0}{2}\right) \quad \text{(B.49)}$$

For $\delta_i=\delta_0$, the average output current equation will get reduced to,

$$I_o=\frac{nV_{in}T_S}{2L}\left(d-d^2-2d\delta+\delta-\frac{3\delta^2}{2}\right) \quad \text{(B.50)}$$

The normalising the average output current by the base $\frac{nV_{in}T_S}{2L}$ value,

$$I_o^{'}=\left(d-d^2-d\delta_i-d\delta_0+\frac{\delta_i}{2}+\frac{\delta_0}{2}-\frac{\delta_i^2}{2}-\frac{\delta_0^2}{2}-\frac{\delta_i\delta_0}{2}\right) \quad \text{(B.51)}$$

For $\delta_i=\delta_0$, the normalised average output current equation will be,

$$I_o^{'}=\left(d-d^2-2d\delta+\delta-\frac{3\delta^2}{2}\right) \quad \text{(B.52)}$$

A similar analysis may be undertaken for the discharging mode, that is when power is transferred from the secondary LV side to the primary HV side. The corresponding expressions for the currents at the HV and LV switching instants, (I_{L3}, I_P) and (I_{L1}, I_{L2}) respectively in (B.42), (B.45) and (B.43), (B.44) are unchanged. However in the expressions for i_0, the secondary side terminal current, the term within brackets in equations (B.49), (B.50), (B.51) and (B.52) would be multiplied by 'minus' sign to signify the reverse power flow.

B.3.1.1 Condition for ZVS:

By applying the zero-voltage switching conditions to the device current waveforms shown in Figure C.5, the current at the LV leading transistor switching instant must be greater than zero to achieve ZVS in the LV bridge. Therefore using (B.43), the following condition must be satisfied for ZVS in the LV bridge:

$$I_{L1} = \frac{T_S}{4L}\left[nV_{in}\left(2d + \delta_i - 1\right) + V_o(1 - \delta_0)\right] \geq 0 \qquad \text{(B.53)}$$

Solving for the inequality given in (B.53), the duty ratio at which ZVS occurs can be obtained as,

$$d \geq 0.5 - \frac{\delta_i}{2} - \frac{V_o^{'}}{2}(1 - \delta_0) \qquad \text{(B.54)}$$

To achieve ZVS for the LV lagging transistor, the current given in (B.44) must be positive. From the waveforms shown in Figure C.5, this condition occurs only after (B.54). Hence, the limiting condition for the LV bridge is given by (B.54).

To achieve ZVS in the HV bridge, the current at the HV lagging transistor switching instant given in (B.42) must be positive for lagging transistor and the current at the HV leading transistor switching instant given in (B.45) must be positive to achieve ZVS for leading transistor. From the waveforms, (B.42) occurs earlier than (B.45), ZVS in the HV bridge is determined by (B.42). However, this condition is normally achieved and the limiting condition for ZVS is that given in (B.54).

B.3.2 Boost mode

Similar analysis is undertaken to derive the mathematical model for boost ($nV_{in} < V_o$) mode of operation, where the power flows from transformer primary (LV) side to the secondary (HV) side with quasi-square-wave applied on transformer primary and secondary. Expression for the inductor current at various switching instants I_{L1}, I_{L2}, I_{L3}, I_P shown in Figure B.6 are given by,

The current at LV lagging transistor switching instant is given as,

$$I_{L3} = \frac{T_S}{4L}\left[nV_{in}(1 - \delta_i) + V_o(2d + \delta_0 - 1)\right] \qquad \text{(B.55)}$$

The current at HV leading transistor switching instant may be expressed as,

$$I_{L1} = \frac{T_S}{4L}\left[nV_{in}\left(2d + \delta_i - 1\right) + V_o(1 - \delta_0)\right] \tag{B.56}$$

The current at HV lagging transistor switching instant may be expressed as,

$$I_P = \frac{T_S}{4L}\left[nV_{in}(2d + \delta_i + 2\delta_0 - 1) + V_o(1 - \delta_0)\right] \tag{B.57}$$

The current at LV leading transistor switching instant is given as,

$$I_{L2} = \frac{T_S}{4L}\left[nV_{in}\left(1 - \delta_i\right) + V_0\left(2d - 1 + \delta_0 + 2\delta_i\right)\right] \tag{B.58}$$

In order to find the average output (ultracapacitor) current, the expression is required for the interval t_B; the time taken for i_L to fall to zero following the LV lagging transistor switching instant. Since the output current waveform is piece-wise linear, this can be derived as,

$$t_B = \frac{T_S\left[nV_{in}(1 - \delta_i) + V_o\left(2d + \delta_0 - 1\right)\right]}{4\left(nV_{in} + V_o\right)} \tag{B.59}$$

Using the above equations, the area under the i_0 current waveform shown as shaded regions in Figure B.6 is obtained. Since the waveform is periodic over half a cycle, dividing the area by the duration, which is $\frac{T_S}{2}$, gives the average output current of the DAB converter as,

$$I_0 = \frac{A + B + C - D}{\frac{T_S}{2}}$$

Where,

$$A = \left(\frac{I_{L2} + I_P}{2}\right)\left(\frac{T_S}{2} - \frac{dT_S}{2} - \frac{\delta_i T_S}{2} - \frac{\delta_0 T_S}{2}\right)$$

$$B = \left(\frac{I_P + I_{L3}}{2}\right)\frac{\delta_i T_S}{2}$$

$$C = \frac{t_B I_{L3}}{2}$$

$$D = \frac{1}{2}\left(\frac{dT_S}{2} - t_B\right)I_{L1}$$

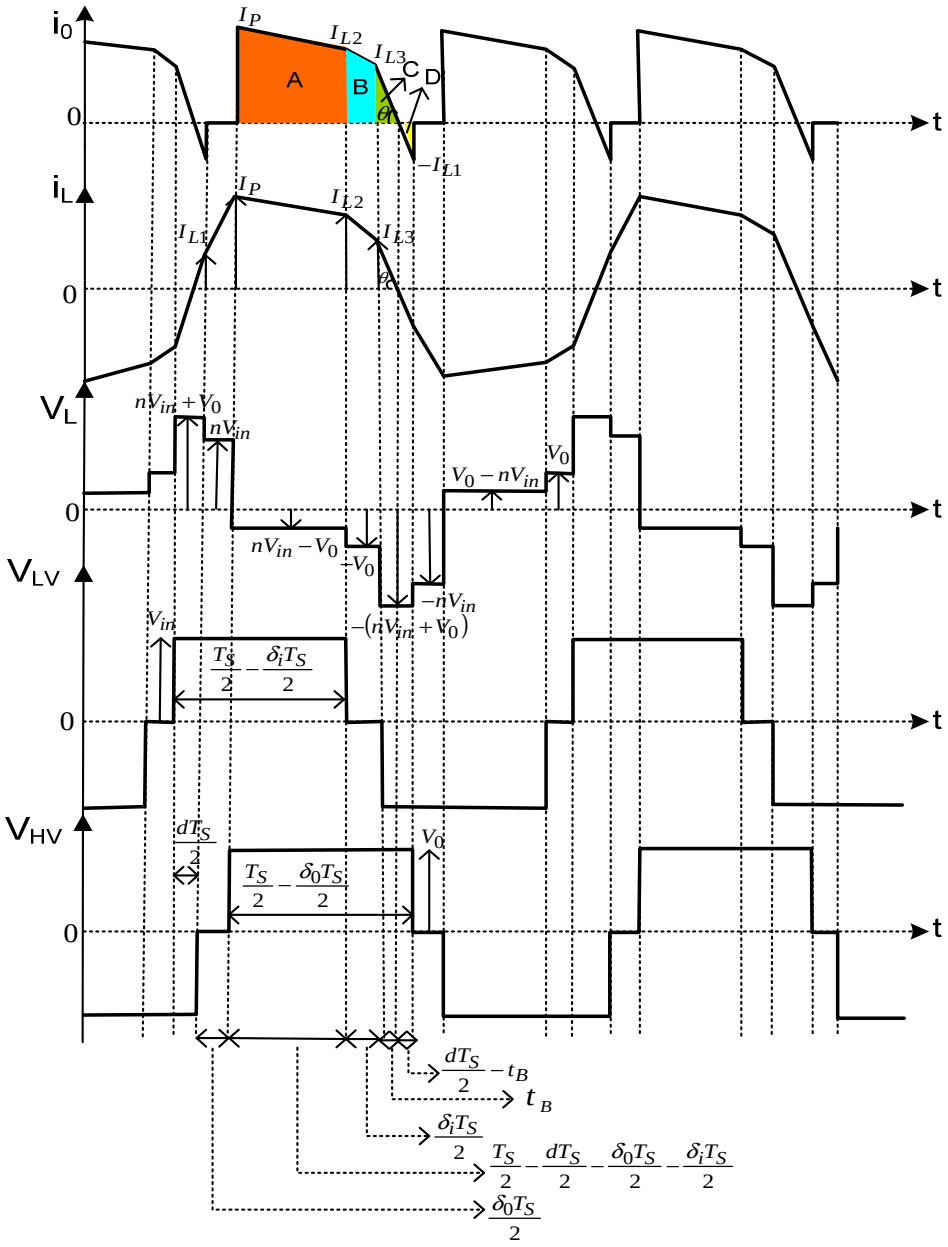

Figure B.6 AC-link voltage and current waveforms with quasi-square-wave on transformer primary and secondary voltages $nV_{in} < V_o$

Substituting the expressions for A, B, C and D terms in the average output current and simplifying further gives the expression for the same as follows,

$$I_o = \frac{nV_{in}T_S}{2L}\left(d - d^2 - d\delta_i - d\delta_0 + \frac{\delta_i}{2} + \frac{\delta_0}{2} - \frac{{\delta_i}^2}{2} - \frac{{\delta_0}^2}{2} - \frac{\delta_i\delta_0}{2}\right) \tag{B.60}$$

For equal dead-time values on transformer primary and secondary ($\delta_i = \delta_0$), the average output current equation will be,

$$I_o = \frac{nV_{in}T_S}{2L}\left(d - d^2 - 2d\delta + \delta - \frac{3\delta^2}{2} \right) \tag{B.61}$$

Normalising the average output current by the base $\frac{nV_{in}T_S}{2L}$ value,

$$I_o^{'} = \left(d - d^2 - d\delta_i - d\delta_0 + \frac{\delta_i}{2} + \frac{\delta_0}{2} - \frac{\delta_i^{\,2}}{2} - \frac{\delta_0^{\,2}}{2} - \frac{\delta_i\delta_0}{2} \right) \tag{B.62}$$

For $\delta_i = \delta_0$, the normalised average output current equation will be,

$$I_o^{'} = \left(d - d^2 - 2d\delta + \delta - \frac{3\delta^2}{2} \right) \tag{B.63}$$

B.3.2.1 Condition for ZVS:

By applying the zero-voltage switching conditions to the device current waveforms shown in Figure C.6, the current at the LV lagging transistor switching instant must be greater than zero to achieve ZVS in the LV bridge. Therefore using (B.55), the following condition must be satisfied for ZVS in the LV bridge:

Soft switching constraints are applied to derive the condition for ZVS as,

$$I_{L3} = \frac{T_S}{4L}\left[nV_{in}(1-\delta_i) + V_O(2d + \delta_0 - 1) \right] \geq 0 \tag{B.64}$$

Solving for the inequality given in (B.64), the duty ratio at which ZVS occurs can be obtained as,

$$d \geq 0.5 - \frac{\delta_0}{2} - \frac{1}{2V_o^{'}}(1-\delta_i) \tag{B.65}$$

To achieve ZVS for the LV leading transistor, the current given in (B.58) must be positive. From the waveforms shown in Figure C.6, this condition occurs only after (B.65). Hence, the limiting condition for the LV bridge is given by (B.65).

To achieve ZVS in the HV bridge, the current at the HV leading transistor switching instant given in (B.56) must be positive for leading transistor and the current at the HV lagging

transistor switching instant given in (B.57) must be positive to achieve ZVS for lagging transistor. From the waveforms, (B.56) occurs earlier than (B.57), ZVS in the HV bridge is determined by (B.56). However, this condition is normally achieved and the limiting condition for ZVS is that given in (B.65).

During power reversal, when the converter operates in the discharging mode (i.e. power flows from transformer secondary side to the primary side), the zero-voltage switching limit is again found to occur in the LV bridge and may again be expressed by (B.53), (B.54), (B.64) and (B.65).

Appendix C

RMS Current Derivations for Quasi-Square-Wave Operation of DAB DC-DC Converter

C.1 RMS current derivation for quasi-square-wave on transformer primary

C.1.1 Buck mode

Figure C.1 depicts the inductor and various device current waveforms of the DAB converter with quasi-square-wave on primary under buck mode. i_L denotes the current flowing through the coupling inductance, i_{A1} and i_{AD1} are the HV side leading transistor and diode currents respectively, i_{B2} and i_{BD2} are the HV side lagging transistor and diode currents respectively and i_{C1} and i_{CD1} are the LV side transistor and diode currents respectively. Effective intervals are marked for a half cycle of the converter waveform. From Figure C.1, the RMS current equation of inductor/transformer current is derived. Since the transformer exhibits a similar wave shape as that of the inductor, RMS value of inductor/transformer is obtained from the current waveforms of Figure C.1. Equation of the inductor/transformer instantaneous current during various intervals over a half cycle is given as,

$$I(t) = \frac{I_{L1}}{\frac{dT_S}{2} - t_B} t, 0 < t < \frac{dT_S}{2} - t_B$$

$$= I_{L1} + \frac{I_r t}{\frac{T_S}{2} - \frac{\delta T_S}{2} - t_B}, \frac{dT_S}{2} - t_B < t < \frac{T_S}{2} - \frac{\delta T_S}{2} - t_B$$

$$= I_P - \frac{I_f t}{\frac{T_S}{2} - t_B}, \frac{T_S}{2} - \frac{\delta T_S}{2} - t_B < t < \frac{T_S}{2} - t_B$$

$$= I_{L2} - \frac{I_{L2} t}{\frac{T_S}{2}}, \frac{T_S}{2} - t_B < t < \frac{T_S}{2}$$

Changing the intervals to their respective effective intervals, instantaneous current of inductor/transformer can be written as,

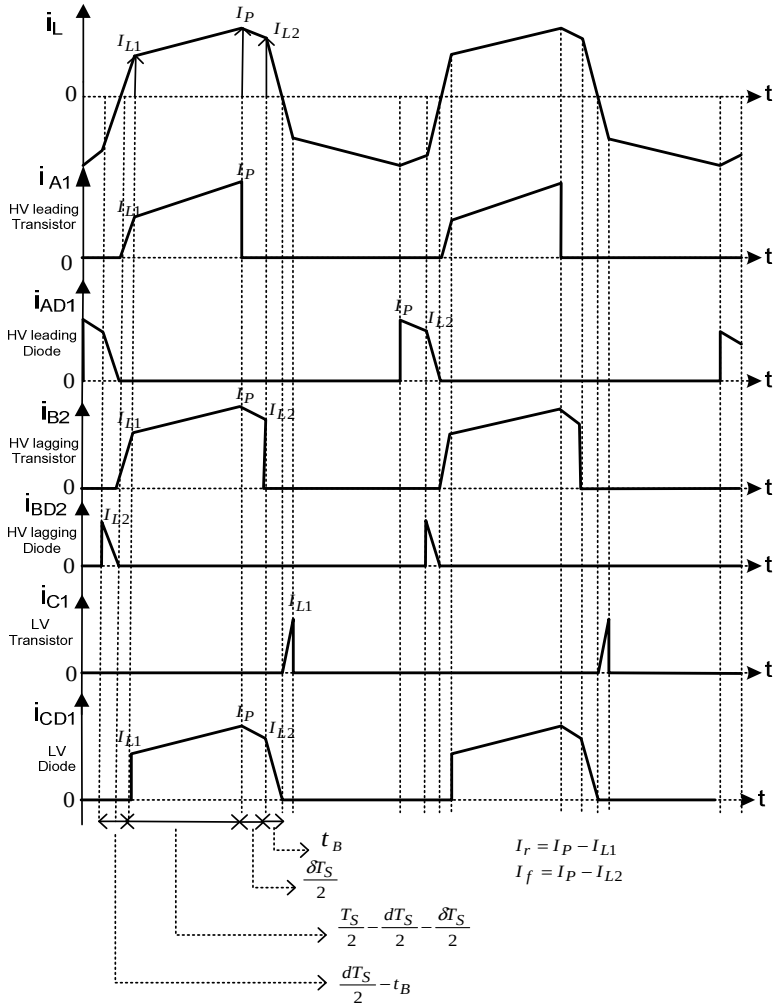

Figure C.1 Inductor and device currents under buck mode of the DAB converter during quasi-square-wave on transformer primary

$$I(t) = \frac{I_{L1}}{\frac{dT_S}{2} - t_B} t, 0 < t < \frac{dT_S}{2} - t_B$$

$$= I_{L1} + \frac{I_r t}{\frac{T_S}{2} - \frac{dT_S}{2} - \frac{\delta T_S}{2}}, 0 < t < \frac{T_S}{2} - \frac{dT_S}{2} - \frac{\delta T_S}{2}$$

$$= I_P - \frac{I_f t}{\frac{\delta T_S}{2}}, 0 < t < \frac{\delta T_S}{2}$$

$$= I_{L2} - \frac{I_{L2} t}{t_B}, 0 < t < t_B$$

Squaring the current,

$$I^2(t)=\left(\frac{I_{L1}}{\frac{dT_S}{2}-t_B}\right)^2 t^2, 0<t<\frac{dT_S}{2}-t_B$$

$$=I_{L1}{}^2+\left(\frac{I_r}{\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}}\right)^2 t^2+\frac{2I_{L1}I_r t}{\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}}, 0<t<\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}$$

$$=I_P{}^2+\left(\frac{I_f}{\frac{\delta T_S}{2}}\right)^2 t^2-\frac{2I_P I_f t}{\frac{\delta T_S}{2}}, 0<t<\frac{\delta T_S}{2}$$

$$=I_{L2}{}^2+\left(\frac{I_{L2}}{t_B}\right)^2 t^2-\frac{2I_{L2}{}^2 t}{t_B}, 0<t<t_B$$

$$I_{RMS}=\sqrt{\frac{2}{T_S}\int_0^{\frac{T_S}{2}} I^2(t)\,dt}$$

Substituting the squared current over a half cycle gives,

$$I_{RMS}=\sqrt{\frac{2}{T_S}\left[\int_0^{\frac{dT_S}{2}-t_B}\left(\frac{I_{L1}}{\frac{dT_S}{2}-t_B}\right)^2 t^2 dt+\int_0^{\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}}\left(I_{L1}{}^2+\left(\frac{I_r}{\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}}\right)^2 t^2+\frac{2I_{L1}I_r t}{\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}}\right)dt+\int_0^{\frac{\delta T_S}{2}}\left(I_P{}^2+\left(\frac{I_f}{\frac{\delta T_S}{2}}\right)^2 t^2-\frac{2I_P I_f t}{\frac{\delta T_S}{2}}\right)dt+\int_0^{t_B}\left(I_{L2}{}^2+\left(\frac{I_{L2}}{t_B}\right)^2 t^2-\frac{2I_{L2}{}^2 t}{t_B}\right)dt\right]}$$

Simplifying further,

$$=\sqrt{\frac{2}{T_S}\left[\left(\frac{I_{L1}}{\frac{dT_S}{2}-t_B}\right)^2\frac{\left(\frac{dT_S}{2}-t_B\right)^3}{3}+\left(I_{L1}{}^2\left(\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}\right)+\left(\frac{I_r}{\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}}\right)^2\frac{\left(\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}\right)^3}{3}+\frac{2I_{L1}I_r t}{\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}}\frac{\left(\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}\right)^2}{2}\right)+\left(I_P{}^2\left(\frac{\delta T_S}{2}\right)+\left(\frac{I_f}{\frac{\delta T_S}{2}}\right)^2\frac{\left(\frac{\delta T_S}{2}\right)^3}{3}-\frac{2I_P I_f}{\frac{\delta T_S}{2}}\frac{\left(\frac{\delta T_S}{2}\right)^2}{2}\right)+\left(I_{L2}{}^2 t_B+\left(\frac{I_{L2}}{t_B}\right)^2\frac{t_B^3}{3}-\frac{2I_{L2}{}^2 t_B^2}{t_B}\frac{}{2}\right)\right]}$$

RMS value of transformer/inductor current equation during buck mode is found to be,

$$I_{RMS}=\sqrt{\frac{2}{T_S}\left[\frac{(I_{L1})^2\left(\frac{dT_S}{2}-t_B\right)}{3}+\left(\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}\right)\left(I_{L1}{}^2+\frac{I_r{}^2}{3}+I_{L1}I_r\right)+\frac{\delta T_S}{2}\left(I_P{}^2+\frac{I_f{}^2}{3}-I_P I_f\right)+\frac{I_{L2}{}^2 t_B}{3}\right]} \quad (C.1)$$

C.1.1.1 Transistor and Diode RMS current derivation

C.1.1.1.1 HV side leading transistor RMS current derivation

For the HV side transistor current shown in Figure C.1, the waveform is periodic over a cycle. The instantaneous current with their effective intervals is expressed as,

$$I(t) = \frac{I_{L1}}{\frac{dT_S}{2} - t_B} t, 0 < t < \frac{dT_S}{2} - t_B$$

$$= I_{L1} + \frac{I_r t}{\frac{T_S}{2} - \frac{dT_S}{2} - \frac{\delta T_S}{2}}, 0 < t < \frac{T_S}{2} - \frac{dT_S}{2} - \frac{\delta T_S}{2}$$

Then squaring the above current gives,

$$I^2(t) = \left(\frac{I_{L1}}{\frac{dT_S}{2} - t_B} \right)^2 t^2, 0 < t < \frac{dT_S}{2} - t_B$$

$$= {I_{L1}}^2 + \left(\frac{I_r}{\frac{T_S}{2} - \frac{dT_S}{2} - \frac{\delta T_S}{2}} \right)^2 t^2 + \frac{2 I_{L1} I_r t}{\frac{T_S}{2} - \frac{dT_S}{2} - \frac{\delta T_S}{2}}, 0 < t < \frac{T_S}{2} - \frac{dT_S}{2} - \frac{\delta T_S}{2}$$

RMS equation,

$$I_{RMS} = \sqrt{\frac{1}{T_S} \int_0^{T_S} I^2(t)\, dt}$$

Substituting the squared current in the above equation,

$$I_{RMS} = \sqrt{\frac{1}{T_S} \left[\int_0^{\frac{dT_S}{2} - t_B} \left(\frac{I_{L1}}{\frac{dT_S}{2} - t_B} \right)^2 t^2 d + \int_0^{\frac{T_S}{2} - \frac{dT_S}{2} - \frac{\delta T_S}{2}} \left({I_{L1}}^2 + \left(\frac{I_r}{\frac{T_S}{2} - \frac{dT_S}{2} - \frac{\delta T_S}{2}} \right)^2 t^2 + \frac{2 I_{L1} I_r t}{\frac{T_S}{2} - \frac{dT_S}{2} - \frac{\delta T_S}{2}} \right) dt \right]}$$

Simplifying further gives the RMS current equation of HV side leading transistor

$$I_{RMS} = \sqrt{\frac{1}{T_S} \left[\frac{(I_{L1})^2 \left(\frac{dT_S}{2} - t_B \right)}{3} + \left(\frac{T_S}{2} - \frac{dT_S}{2} - \frac{\delta T_S}{2} \right) \left({I_{L1}}^2 + \frac{{I_r}^2}{3} + I_{L1} I_r \right) \right]} \quad \text{(C.2)}$$

C.1.1.1.2 HV side leading diode RMS current derivation

HV side diode has a trapezoidal and triangular current waveform. Similar procedure is followed here as well to derive the RMS current expression. Considering the effective intervals, the instantaneous current is expressed as,

$$I(t) = I_P - \frac{I_f t}{\frac{\delta T_S}{2}}, 0 < t < \frac{\delta T_S}{2}$$

$$= I_{L2} - \frac{I_{L2} t}{t_B}, 0 < t < t_B$$

Squaring the current,

$$I^2(t) = {I_P}^2 + \left(\frac{I_f}{\frac{\delta T_S}{2}}\right)^2 t^2 - \frac{2 I_P I_f t}{\frac{\delta T_S}{2}}, 0 < t < \frac{\delta T_S}{2}$$

$$= {I_{L2}}^2 + \left(\frac{I_{L2}}{t_B}\right)^2 t^2 - \frac{2 {I_{L2}}^2 t}{t_B}, 0 < t < t_B$$

The expression for the interval t_B is given in the steady state analysis presented in Chapter 5 and in Appendix B. The RMS current is given by,

$$I_{RMS} = \sqrt{\frac{1}{T_S} \int_0^{T_S} I^2(t)\, dt}$$

Substituting $I^2(t)$,

$$I_{RMS} = \sqrt{\frac{1}{T_S}\left[\int_0^{\frac{\delta T_S}{2}} \left({I_P}^2 + \left(\frac{I_f}{\frac{\delta T_S}{2}}\right)^2 t^2 - \frac{2 I_P I_f t}{\frac{\delta T_S}{2}}\right) + \int_0^{t_B} \left({I_{L2}}^2 + \left(\frac{I_{L2}}{t_B}\right)^2 t^2 - \frac{2 {I_{L2}}^2 t}{t_B}\right) dt\right]}$$

Minimising further, the RMS current equation of HV side leading diode can be obtained as,

$$I_{RMS} = \sqrt{\frac{1}{T_S}\left[\left(\frac{\delta T_S}{2}\right) \times \left(I_P^2 + \frac{I_f^2}{3} - I_P I_f\right) + \frac{I_{L2}^2 \times (t_B)}{3}\right]} \qquad \text{(C.3)}$$

C.1.1.1.3 HV side lagging transistor RMS current derivation

For the HV side transistor current shown in Figure C.1, the waveform is periodic over a cycle. The instantaneous current with their effective intervals is expressed as,

$$I(t) = \frac{I_{L1}}{\frac{dT_S}{2} - t_B} t, 0 < t < \frac{dT_S}{2} - t_B$$

$$= I_{L1} + \frac{I_r t}{\frac{T_S}{2} - \frac{dT_S}{2} - \frac{\delta T_S}{2}}, 0 < t < \frac{T_S}{2} - \frac{dT_S}{2} - \frac{\delta T_S}{2}$$

$$= I_P - \frac{I_f t}{\frac{\delta T_S}{2}}, 0 < t < \frac{\delta T_S}{2}$$

Then squaring the above current gives,

$$I^2(t) = \left(\frac{I_{L1}}{\frac{dT_S}{2} - t_B} \right)^2 t^2, 0 < t < \frac{dT_S}{2} - t_B$$

$$= {I_{L1}}^2 + \left(\frac{I_r}{\frac{T_S}{2} - \frac{dT_S}{2} - \frac{\delta T_S}{2}} \right)^2 t^2 + \frac{2 I_{L1} I_r t}{\frac{T_S}{2} - \frac{dT_S}{2} - \frac{\delta T_S}{2}}, 0 < t < \frac{T_S}{2} - \frac{dT_S}{2} - \frac{\delta T_S}{2}$$

$$= {I_P}^2 + \left(\frac{I_f}{\frac{\delta T_S}{2}} \right)^2 t^2 - \frac{2 I_P I_f t}{\frac{\delta T_S}{2}}, 0 < t < \frac{\delta T_S}{2}$$

RMS equation,

$$I_{RMS} = \sqrt{\frac{1}{T_S} \int_0^{T_S} I^2(t)\, dt}$$

Substituting the squared current in the above equation,

$$I_{RMS} = \sqrt{\frac{1}{T_S} \left[\int_0^{\frac{dT_S}{2} - t_B} \left(\frac{I_{L1}}{\frac{dT_S}{2} - t_B} \right)^2 t^2 dt + \int_0^{\frac{T_S}{2} - \frac{dT_S}{2} - \frac{\delta T_S}{2}} \left({I_{L1}}^2 + \left(\frac{I_r}{\frac{T_S}{2} - \frac{dT_S}{2} - \frac{\delta T_S}{2}} \right)^2 t^2 + \frac{2 I_{L1} I_r t}{\frac{T_S}{2} - \frac{dT_S}{2} - \frac{\delta T_S}{2}} \right) dt + \int_0^{\frac{\delta T_S}{2}} \left({I_P}^2 + \left(\frac{I_f}{\frac{\delta T_S}{2}} \right)^2 t^2 - \frac{2 I_P I_f t}{\frac{\delta T_S}{2}} \right) \right]}$$

Simplifying further gives the RMS current equation of HV side lagging transistor

$$I_{RMS} = \sqrt{\frac{1}{T_S} \left[\frac{I_{L1}^2 \times \left(\frac{dT_S}{2} - t_B \right)}{3} + \left(\frac{T_S}{2} - \frac{dT_S}{2} - \frac{\delta T_S}{2} \right) \times \left(I_{L1}^2 + \frac{I_r^2}{3} + I_{L1} I_r \right) + \left(\frac{\delta T_S}{2} \right) \times \left(I_P^2 + \frac{I_f^2}{3} - I_P I_f \right) \right]} \qquad \text{(C.4)}$$

C.1.1.1.4 HV side lagging diode RMS current derivation

HV side diode has a triangular current waveform. Similar procedure is followed here as well to derive the RMS current expression. Considering the effective intervals, the instantaneous current is expressed as,

$$I(t) = I_{L2} - \frac{I_{L2}t}{t_B}, 0 < t < t_B$$

$$= 0, t_B < t < T_S$$

Squaring the current,

$$I^2(t) = {I_{L2}}^2 + \left(\frac{I_{L2}}{t_B}\right)^2 t^2 - \frac{2{I_{L2}}^2 t}{t_B}, 0 < t < t_B$$

The expression for unknown interval t_B is given in the steady state analysis presented in Chapter 5. The RMS current is given by,

$$I_{RMS} = \sqrt{\frac{1}{T_S}\int_0^{T_S} I^2(t)\,dt}$$

Substituting $I^2(t)$,

$$I_{RMS} = \sqrt{\frac{1}{T_S}\left[\int_0^{t_B}\left({I_{L2}}^2 + \left(\frac{I_{L2}}{t_B}\right)^2 t^2 - \frac{2{I_{L2}}^2 t}{t_B}\right)dt\right]}$$

Minimising further, the RMS current equation of HV side lagging diode can be obtained as,

$$I_{RMS} = \sqrt{\frac{1}{T_S}\left[\frac{{I_{L2}}^2 t_B}{3}\right]} \qquad \text{(C.5)}$$

C.1.1.1.5 LV side transistor RMS current derivation

The LV side transistor current waveform during charging mode has triangular wave shape. Considering the effective interval, the instantaneous current is given by,

$$I(t) = \frac{I_{L1}}{\frac{dT_S}{2} - t_B} t, 0 < t < \frac{dT_S}{2} - t_B$$

Squaring the current gives,

$$I^2(t) = \left(\frac{I_{L1}}{\frac{dT_S}{2} - t_B} \right)^2 t^2, 0 < t < \frac{dT_S}{2} - t_B$$

Estimating the RMS value over a cycle,

$$I_{RMS} = \sqrt{\frac{1}{T_S}\left[\int_0^{\frac{dT_S}{2}-t_B} \left(\frac{I_{L1}}{\frac{dT_S}{2} - t_B} \right)^2 t^2 dt \right]}$$

Simplifying further, the RMS current equation of LV side transistor is given as,

$$I_{RMS} = \sqrt{\frac{1}{T_S}\left[\frac{(I_{L1})^2 \left(\frac{dT_S}{2} - t_B \right)}{3} \right]} \quad \text{(C.6)}$$

C.1.1.1.6 LV side diode RMS current derivation

For the LV side diode current shown in Figure C.1, the waveform is periodic over a cycle. The instantaneous current with their effective intervals is expressed as,

$$I(t) = I_{L1} + \frac{I_r t}{\frac{T_S}{2} - \frac{dT_S}{2} - \frac{\delta T_S}{2}}, 0 < t < \frac{T_S}{2} - \frac{dT_S}{2} - \frac{\delta T_S}{2}$$

$$= I_P - \frac{I_f t}{\frac{\delta T_S}{2}}, 0 < t < \frac{\delta T_S}{2}$$

$$= I_{L2} - \frac{I_{L2}}{t_B} t, 0 < t < t_B$$

Then squaring the above current gives,

$$I^2(t) = {I_{L1}}^2 + \left(\frac{I_r}{\frac{T_S}{2} - \frac{dT_S}{2} - \frac{\delta T_S}{2}} \right)^2 t^2 + \frac{2 I_{L1} I_r t}{\frac{T_S}{2} - \frac{dT_S}{2} - \frac{\delta T_S}{2}}, 0 < t < \frac{T_S}{2} - \frac{dT_S}{2} - \frac{\delta T_S}{2}$$

$$= {I_P}^2 + \left(\frac{I_f}{\frac{\delta T_S}{2}} \right)^2 t^2 - \frac{2 I_P I_f t}{\frac{\delta T_S}{2}}, 0 < t < \frac{\delta T_S}{2}$$

$$= {I_{L2}}^2 + \left(\frac{I_{L2}}{t_B}\right)^2 t^2 - \frac{2{I_{L2}}^2 t}{t_B}, 0 < t < t_B$$

RMS equation,

$$I_{RMS} = \sqrt{\frac{1}{T_S}\int_0^{T_S} I^2(t)\,dt}$$

Substituting the squared current in the above equation,

$$I_{RMS} = \sqrt{\frac{1}{T_S}\left[\int_0^{\frac{\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}}{2}} \left({I_{L1}}^2 + \left(\frac{I_r}{\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}}\right)^2 t^2 + \frac{2I_{L1}I_r t}{\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}}\right) dt + \int_0^{\frac{\frac{\delta T_S}{2}}{2}} \left({I_P}^2 + \left(\frac{I_f}{\frac{\delta T_S}{2}}\right)^2 t^2 - \frac{2I_P I_f t}{\frac{\delta T_S}{2}}\right) + \int_0^{t_B} \left({I_{L2}}^2 + \left(\frac{I_{L2}}{t_B}\right)^2 t^2 - \frac{2{I_{L2}}^2 t}{t_B}\right) dt\right]}$$

Simplifying further gives the RMS current equation of LV side diode

$$I_{RMS} = \sqrt{\frac{1}{T_S}\left[\left(\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}\right)\times\left(I_{L1}^2 + \frac{I_r^2}{3} + I_{L1}I_r\right) + \left(\frac{\delta T_S}{2}\right)\times\left(I_P^2 + \frac{I_f^2}{3} - I_P I_f\right) + \frac{I_{L2}^2 \times t_B}{3}\right]} \quad \text{(C.7)}$$

C.1.2 Boost mode

Figure C.2 depicts the waveforms of inductor and device currents of the DAB converter under boost mode with quasi-square-wave on transformer primary. Equation of the transformer/inductor instantaneous current during boost mode for various intervals over a half cycle is given as,

$$I(t) = \frac{I_P}{\frac{dT_S}{2} - t_B} t, 0 < t < \frac{dT_S}{2} - t_B$$

$$= I_P - \frac{I_r t}{\frac{T_S}{2} - \frac{\delta T_S}{2} - t_B}, \frac{dT_S}{2} - t_B < t < \frac{T_S}{2} - \frac{\delta T_S}{2} - t_B$$

$$= I_{L1} - \frac{I_f t}{\frac{T_S}{2} - t_B}, \frac{T_S}{2} - \frac{\delta T_S}{2} - t_B < t < \frac{T_S}{2} - t_B$$

$$= I_{L2} - \frac{I_{L2} t}{\frac{T_S}{2}}, \frac{T_S}{2} - t_B < t < \frac{T_S}{2}$$

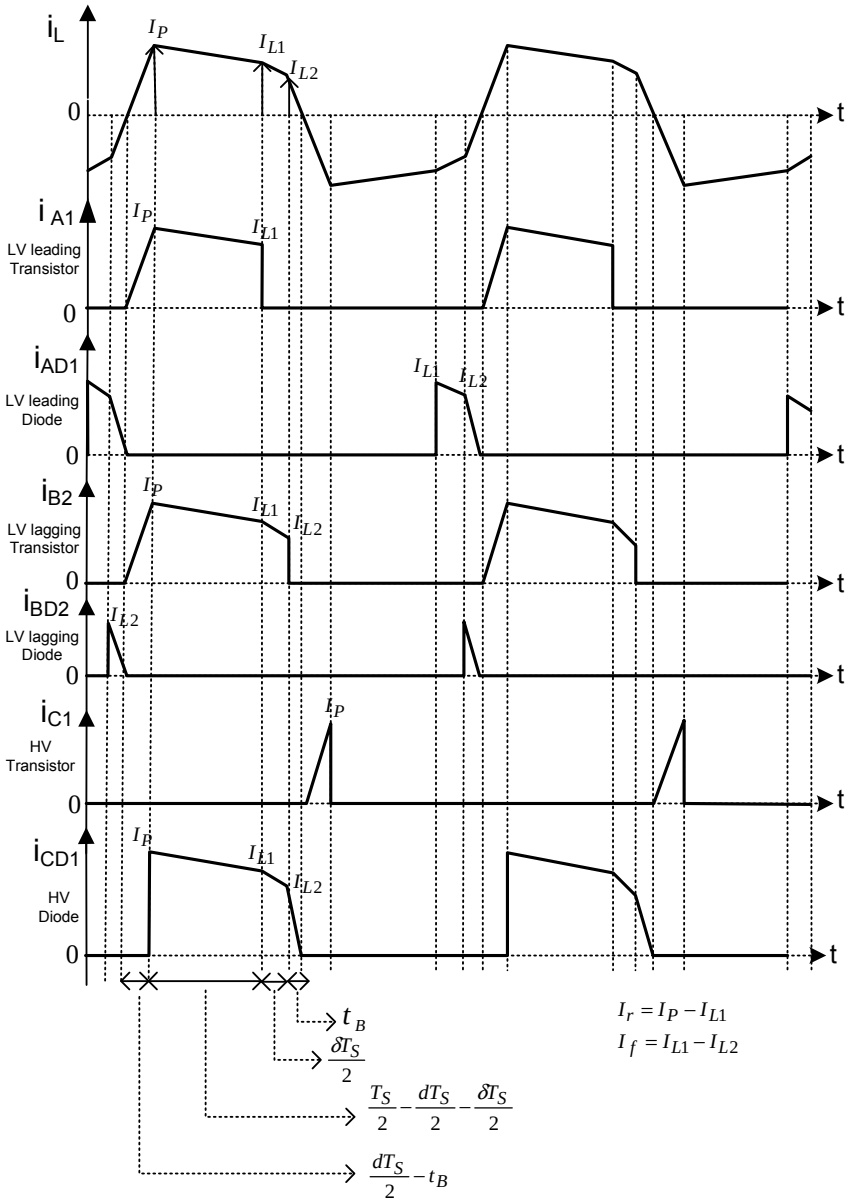

Figure C.2 Inductor and device currents of the DAB converter under boost mode with quasi-square-wave on transformer primary

Changing the intervals to their respective effective intervals, the instantaneous current of inductor/transformer can be written as,

$$I(t) = \frac{I_P}{\frac{dT_S}{2} - t_B} t, 0 < t < \frac{dT_S}{2} - t_B$$

$$= I_P - \frac{I_r t}{\frac{T_S}{2} - \frac{dT_S}{2} - \frac{\delta T_S}{2}}, 0 < t < \frac{T_S}{2} - \frac{dT_S}{2} - \frac{\delta T_S}{2}$$

$$= I_{L1} - \frac{I_f t}{\frac{\delta T_S}{2}}, 0 < t < \frac{\delta T_S}{2}$$

$$= I_{L2} - \frac{I_{L2} t}{t_B}, 0 < t < t_B$$

Squaring the current,

$$I^2(t) = \left(\frac{I_P}{\frac{dT_S}{2} - t_B} \right)^2 t^2, 0 < t < \frac{dT_S}{2} - t_B$$

$$= {I_P}^2 + \left(\frac{I_r}{\frac{T_S}{2} - \frac{dT_S}{2} - \frac{\delta T_S}{2}} \right)^2 t^2 - \frac{2 I_P I_r t}{\frac{T_S}{2} - \frac{dT_S}{2} - \frac{\delta T_S}{2}}, 0 < t < \frac{T_S}{2} - \frac{dT_S}{2} - \frac{\delta T_S}{2}$$

$$= {I_{L1}}^2 + \left(\frac{I_f}{\frac{\delta T_S}{2}} \right)^2 t^2 - \frac{2 I_{L1} I_f t}{\frac{\delta T_S}{2}}, 0 < t < \frac{\delta T_S}{2}$$

$$= {I_{L2}}^2 + \left(\frac{I_{L2}}{t_B} \right)^2 t^2 - \frac{2 {I_{L2}}^2 t}{t_B}, 0 < t < t_B$$

$$I_{RMS} = \sqrt{\frac{2}{T_S} \int_0^{\frac{T_S}{2}} I^2(t)\, dt}$$

Substituting the squared current over a half cycle,

$$I_{RMS} = \sqrt{\frac{2}{T_S} \left[\int_0^{\frac{dT_S}{2} - t_B} \left(\frac{I_P}{\frac{dT_S}{2} - t_B} \right)^2 t^2 dt + \int_0^{\frac{T_S}{2} - \frac{dT_S}{2} - \frac{\delta T_S}{2}} \left({I_P}^2 + \left(\frac{I_r}{\frac{T_S}{2} - \frac{dT_S}{2} - \frac{\delta T_S}{2}} \right)^2 t^2 - \frac{2 I_P I_r t}{\frac{T_S}{2} - \frac{dT_S}{2} - \frac{\delta T_S}{2}} \right) dt + \int_0^{\frac{\delta T_S}{2}} \left({I_{L1}}^2 + \left(\frac{I_f}{\frac{\delta T_S}{2}} \right)^2 t^2 - \frac{2 I_{L1} I_f t}{\frac{\delta T_S}{2}} \right) dt + \int_0^{t_B} \left({I_{L2}}^2 + \left(\frac{I_{L2}}{t_B} \right)^2 t^2 - \frac{2 {I_{L2}}^2 t}{t_B} \right) dt \right]}$$

Simplifying further,

$$= \sqrt{\frac{2}{T_S}\left[\left(\frac{I_P}{\frac{dT_S}{2}-t_B}\right)^2\frac{\left(\frac{dT_S}{2}-t_B\right)^3}{3}+\left(I_P^2\left(\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}\right)+\left(\frac{I_r}{\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}}\right)^2\frac{\left(\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}\right)^3}{3}-\frac{2I_PI_rt}{\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}}\frac{\left(\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}\right)^2}{2}\right)+\left(I_{L1}^2\left(\frac{\delta T_S}{2}\right)+\left(\frac{I_f}{\frac{\delta T_S}{2}}\right)^2\frac{\left(\frac{\delta T_S}{2}\right)^3}{3}-\frac{2I_{L1}I_f}{\frac{\delta T_S}{2}}\frac{\left(\frac{\delta T_S}{2}\right)^2}{2}\right)+\left(I_{L2}^2t_B+\left(\frac{I_{L2}}{t_B}\right)^2\frac{t_B^3}{3}-\frac{2I_{L2}^2t_B^2}{t_B}\frac{}{2}\right)\right]}$$

RMS value of transformer/inductor current equation during boost mode is found to be,

$$I_{RMS}=\sqrt{\frac{2}{T_S}\left[\frac{(I_P)^2\left(\frac{dT_S}{2}-t_B\right)}{3}+\left(\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}\right)\left(I_P^{\,2}+\frac{I_r^{\,2}}{3}-I_PI_r\right)+\frac{\delta T_S}{2}\left(I_{L1}^{\,2}+\frac{I_f^{\,2}}{3}-I_{L1}I_f\right)+\frac{I_{L2}^{\,2}t_B}{3}\right]} \quad \text{(C.8)}$$

Similar to the buck mode, RMS current derivations for all the devices has been obtained for boost mode as shown in Figure C.2 and are listed below.

LV side leading transistor RMS current can be given as,

$$I_{RMS}=\sqrt{\frac{1}{T_S}\left[\frac{I_P^2\times\left(\frac{dT_S}{2}-t_B\right)}{3}+\left(\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}\right)\times\left(I_P^2+\frac{I_r^2}{3}-I_PI_r\right)\right]} \quad \text{(C.9)}$$

LV side leading diode RMS current can be written as,

$$I_{RMS}=\sqrt{\frac{1}{T_S}\left[\left(\frac{\delta T_S}{2}\right)\times\left(I_{L1}^2+\frac{I_f^2}{3}-I_{L1}I_f\right)+\frac{I_{L2}^2\times(t_B)}{3}\right]} \quad \text{(C.10)}$$

LV side lagging transistor RMS current can be expressed as,

$$I_{RMS}=\sqrt{\frac{1}{T_S}\left[\frac{I_P^2\times\left(\frac{dT_S}{2}-t_B\right)}{3}+\left(\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}\right)\times\left(I_P^2+\frac{I_r^2}{3}-I_PI_r\right)+\left(\frac{\delta T_S}{2}\right)\times\left(I_{L1}^2+\frac{I_f^2}{3}-I_{L1}I_f\right)\right]} \quad \text{(C.11)}$$

LV side lagging diode RMS current can be written as,

$$I_{RMS}=\sqrt{\frac{1}{T_S}\left[\frac{I_{L2}^2\times(t_B)}{3}\right]} \quad \text{(C.12)}$$

HV side transistor RMS current can be given by,

$$I_{RMS}=\sqrt{\frac{1}{T_S}\left[\frac{I_P^2\times\left(\frac{dT_S}{2}-t_B\right)}{3}\right]} \tag{C.13}$$

HV side diode RMS current can be given as,

$$I_{RMS}=\sqrt{\frac{1}{T_S}\left[\left(\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}\right)\times\left(I_P^2+\frac{I_r^2}{3}-I_P I_r\right)+\left(\frac{\delta T_S}{2}\right)\times\left(I_{L1}^2+\frac{I_f^2}{3}-I_{L1}I_f\right)+\frac{I_{L2}^2\times t_B}{3}\right]} \tag{C.14}$$

C.2 RMS current derivation for quasi-square-wave on transformer secondary

C.2.1 Buck mode

Figure C.3 depicts inductor and various device current waveforms of the DAB converter under buck mode, waveform labels and intervals are illustrated in Figure C.3. The following RMS current equation is derived with quasi-square-wave on transformer secondary side for buck mode. Equation of the instantaneous current of transformer/inductor over a half cycle is given in terms of their effective intervals as,

$$I(t)=\frac{I_{L1}}{\frac{dT_S}{2}-t_B}t,0<t<\frac{dT_S}{2}-t_B$$

$$=I_{L1}+\frac{I_f t}{\frac{\delta T_S}{2}},0<t<\frac{\delta T_S}{2}$$

$$=I_{L2}+\frac{I_r t}{\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}},0<t<\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}$$

$$=I_P-\frac{I_P t}{t_B},0<t<t_B$$

Squaring the current,

$$I^2(t)=\left(\frac{I_{L1}}{\frac{dT_S}{2}-t_B}\right)^2 t^2,0<t<\frac{dT_S}{2}-t_B$$

$$=I_{L1}{}^2+\left(\frac{I_f}{\frac{\delta T_S}{2}}\right)^2 t^2+\frac{2I_{L1}I_f t}{\frac{\delta T_S}{2}},0<t<\frac{\delta T_S}{2}$$

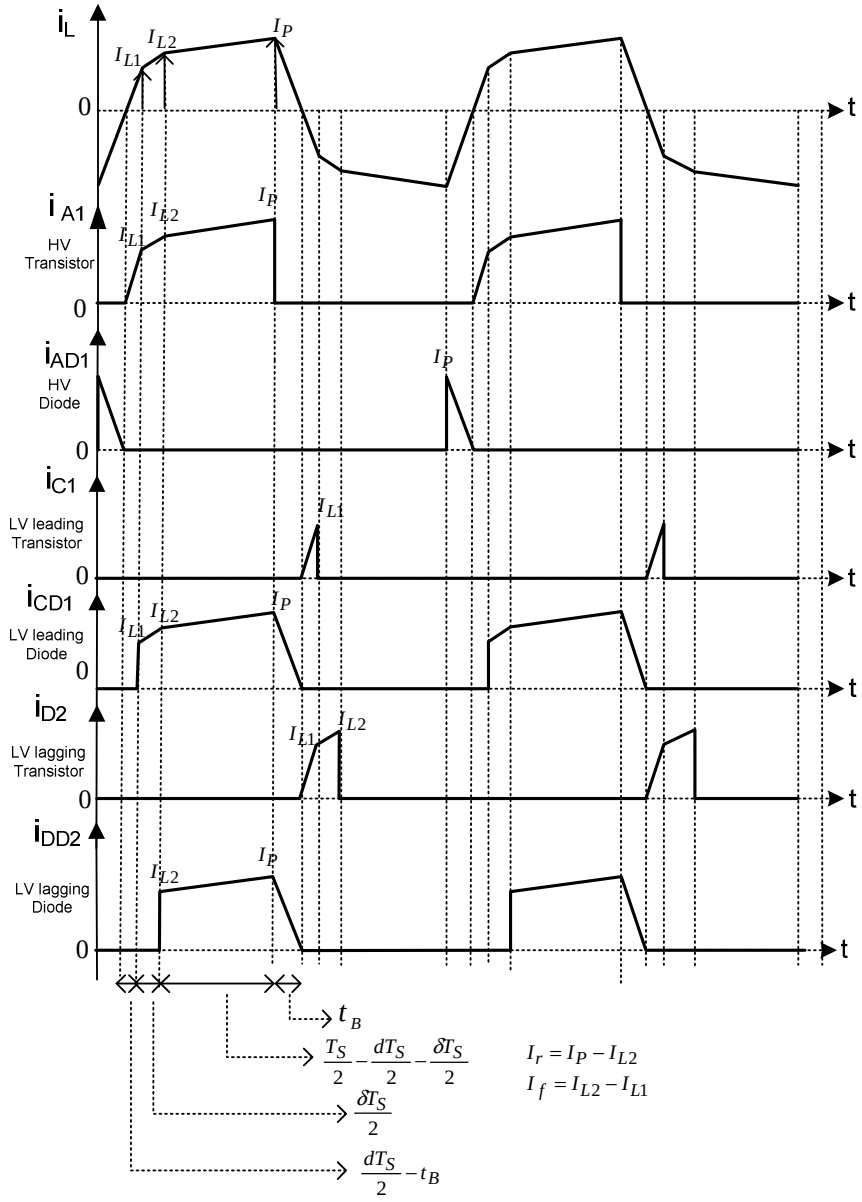

Figure C.3. Inductor and device current waveforms of the converter under buck mode for quasi-square-wave on transformer secondary

$$= {I_{L2}}^2 + \left(\frac{I_r}{\frac{T_S}{2} - \frac{dT_S}{2} - \frac{\delta T_S}{2}} \right)^2 t^2 + \frac{2 I_{L2} I_r t}{\frac{T_S}{2} - \frac{dT_S}{2} - \frac{\delta T_S}{2}}, 0 < t < \frac{T_S}{2} - \frac{dT_S}{2} - \frac{\delta T_S}{2}$$

$$= {I_P}^2 + \left(\frac{I_P}{t_B} \right)^2 t^2 - \frac{2 {I_P}^2 t}{t_B}, 0 < t < t_B$$

$$I_{RMS} = \sqrt{\frac{2}{T_S}\int_0^{\frac{T_S}{2}} I^2(t)\,dt}$$

Substituting the squared current over a half cycle gives,

$$I_{RMS}=\sqrt{\frac{2}{T_S}\left[\int_0^{\frac{dT_S}{2}-t_B}\left(\frac{I_{L1}}{\frac{dT_S}{2}-t_B}\right)^2 t^2dt+\int_0^{\frac{\delta T_S}{2}}\left(I_{L1}^{\,2}+\left(\frac{I_f}{\frac{\delta T_S}{2}}\right)^2 t^2+\frac{2I_{L1}I_f t}{\frac{\delta T_S}{2}}\right)dt+\int_0^{\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}}\left(I_{L2}^{\,2}+\left(\frac{I_r}{\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}}\right)^2 t^2+\frac{2I_{L2}I_r t}{\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}}\right)dt+\int_0^{t_B}\left(I_P^{\,2}+\left(\frac{I_P}{t_B}\right)^2 t^2-\frac{2I_P^{\,2}t}{t_B}\right)dt\right]}$$

Simplifying further,

$$=\sqrt{\frac{2}{T_S}\left[\left(\frac{I_{L1}}{\frac{dT_S}{2}-t_B}\right)^2\frac{\left(\frac{dT_S}{2}-t_B\right)^3}{3}+\left(I_{L1}^{\,2}\left(\frac{\delta T_S}{2}\right)+\left(\frac{I_f}{\frac{\delta T_S}{2}}\right)^2\frac{\left(\frac{\delta T_S}{2}\right)^3}{3}+\frac{2I_{L1}I_f}{\frac{\delta T_S}{2}}\frac{\left(\frac{\delta T_S}{2}\right)^2}{2}\right)+\left(I_{L2}^{\,2}\left(\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}\right)+\left(\frac{I_r}{\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}}\right)^2\frac{\left(\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}\right)^3}{3}+\frac{2I_{L2}I_r t}{\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}}\frac{\left(\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}\right)^2}{2}\right)+\left(I_P^{\,2}t_B+\left(\frac{I_P}{t_B}\right)^2\frac{t_B^{\,3}}{3}-\frac{2I_P^{\,2}}{t_B}\frac{t_B^{\,2}}{2}\right)\right]}$$

RMS value of transformer/inductor current equation is found to be,

$$I_{RMS}=\sqrt{\frac{2}{T_S}\left[\frac{(I_{L1})^2\left(\frac{dT_S}{2}-t_B\right)}{3}+\frac{\delta T_S}{2}\left(I_{L1}^{\,2}+\frac{I_f^{\,2}}{3}+I_{L1}I_f\right)+\left(\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}\right)\left(I_{L2}^{\,2}+\frac{I_r^{\,2}}{3}+I_{L2}I_r\right)+\frac{I_P^{\,2}t_B}{3}\right]} \qquad \text{(C.15)}$$

C.2.1.1 Transistors and diodes RMS current derivation for quasi-square-wave on transformer secondary - Buck mode

C.2.1.1.1HV side transistor RMS current derivation

For the HV side transistor current shown in Figure C.3, the waveform is periodic over a cycle. The instantaneous current with their effective intervals is expressed as,

$$I(t) = \frac{I_{L1}}{\frac{dT_S}{2} - t_B} t, 0 < t < \frac{dT_S}{2} - t_B$$

$$= I_{L1} + \frac{I_f t}{\frac{\delta T_S}{2}}, 0 < t < \frac{\delta T_S}{2}$$

$$= I_{L2} + \frac{I_r t}{\frac{T_S}{2} - \frac{dT_S}{2} - \frac{\delta T_S}{2}}, 0 < t < \frac{T_S}{2} - \frac{dT_S}{2} - \frac{\delta T_S}{2}$$

Then squaring the above current gives,

$$I^2(t) = \left(\frac{I_{L1}}{\frac{dT_S}{2} - t_B} \right)^2 t^2, 0 < t < \frac{dT_S}{2} - t_B$$

$$= {I_{L1}}^2 + \left(\frac{I_f}{\frac{\delta T_S}{2}} \right)^2 t^2 + \frac{2 I_{L1} I_f t}{\frac{\delta T_S}{2}}, 0 < t < \frac{\delta T_S}{2}$$

$$= {I_{L2}}^2 + \left(\frac{I_r}{\frac{T_S}{2} - \frac{dT_S}{2} - \frac{\delta T_S}{2}} \right)^2 t^2 + \frac{2 I_{L2} I_r t}{\frac{T_S}{2} - \frac{dT_S}{2} - \frac{\delta T_S}{2}}, 0 < t < \frac{T_S}{2} - \frac{dT_S}{2} - \frac{\delta T_S}{2}$$

RMS equation,

$$I_{RMS} = \sqrt{\frac{1}{T_S} \int_0^{T_S} I^2(t)\, dt}$$

Substituting the squared current in the above equation,

$$I_{RMS} = \sqrt{\frac{1}{T_S} \left[\int_0^{\frac{dT_S}{2} - t_B} \left(\frac{I_{L1}}{\frac{dT_S}{2} - t_B} \right)^2 t^2 dt + \int_0^{\frac{\delta T_S}{2}} \left({I_{L1}}^2 + \left(\frac{I_f}{\frac{\delta T_S}{2}} \right)^2 t^2 + \frac{2 I_{L1} I_f t}{\frac{\delta T_S}{2}} \right) + \int_0^{\frac{T_S}{2} - \frac{dT_S}{2} - \frac{\delta T_S}{2}} \left({I_{L2}}^2 + \left(\frac{I_r}{\frac{T_S}{2} - \frac{dT_S}{2} - \frac{\delta T_S}{2}} \right)^2 t^2 + \frac{2 I_{L2} I_r t}{\frac{T_S}{2} - \frac{dT_S}{2} - \frac{\delta T_S}{2}} \right) dt \right]}$$

Simplifying further gives the RMS current equation of HV side transistor

$$I_{RMS} = \sqrt{\frac{1}{T_S} \left[\frac{I_{L1}^2 \times \left(\frac{dT_S}{2} - t_B \right)}{3} + \left(I_{L1}^2 + \frac{I_f^2}{3} + I_{L1} I_f \right) \times \frac{\delta T_S}{2} + \left(\frac{T_S}{2} - \frac{dT_S}{2} - \frac{\delta T_S}{2} \right) \times \left(I_{L2}^2 + \frac{I_r^2}{3} + I_{L2} I_r \right) \right]} \qquad \text{(C.16)}$$

C.2.1.1.2 HV side diode RMS current derivation

Equation derived in section C.1.1.1.4 hold well with I_{L2} replaced by I_P, which gives the expression as,

$$I_{RMS} = \sqrt{\frac{1}{T_S}\left[\frac{I_P^2 \times (t_B)}{3}\right]} \tag{C.17}$$

C.2.1.1.3 LV side leading transistor RMS current derivation

Equation derived in section C.1.1.1.5 is applicable for this LV side leading transistor as they exhibit exact parameters. Therefore, the RMS current is given as,

$$I_{RMS} = \sqrt{\frac{1}{T_S}\left[\frac{I_{L1}^2 \times \left(\frac{dT_S}{2} - t_B\right)}{3}\right]} \tag{C.18}$$

C.2.1.1.4 LV side leading diode RMS current derivation

The instantaneous current with their effective intervals is expressed as,

$$I(t) = I_{L1} + \frac{I_f t}{\frac{\delta T_S}{2}}, 0 < t < \frac{\delta T_S}{2}$$

$$= I_{L2} + \frac{I_r t}{\frac{T_S}{2} - \frac{dT_S}{2} - \frac{\delta T_S}{2}}, 0 < t < \frac{T_S}{2} - \frac{dT_S}{2} - \frac{\delta T_S}{2}$$

$$= I_P - \frac{I_P t}{t_B}, 0 < t < t_B$$

Then squaring the above current gives,

$$I^2(t) = {I_{L1}}^2 + \left(\frac{I_f}{\frac{\delta T_S}{2}}\right)^2 t^2 + \frac{2 I_{L1} I_f t}{\frac{\delta T_S}{2}}, 0 < t < \frac{\delta T_S}{2}$$

$$= {I_{L2}}^2 + \left(\frac{I_r}{\frac{T_S}{2} - \frac{dT_S}{2} - \frac{\delta T_S}{2}}\right)^2 t^2 + \frac{2 I_{L2} I_r t}{\frac{T_S}{2} - \frac{dT_S}{2} - \frac{\delta T_S}{2}}, 0 < t < \frac{T_S}{2} - \frac{dT_S}{2} - \frac{\delta T_S}{2}$$

$$= I_P^2 + \left(\frac{I_P}{t_B}\right)^2 t^2 - \frac{2 I_P^2 t}{t_B}, 0 < t < t_B$$

RMS equation,

$$I_{RMS} = \sqrt{\frac{1}{T_S}\int_0^{T_S} I^2(t)\,dt}$$

Substituting the squared current in the above equation,

$$I_{RMS}=\sqrt{\frac{1}{T_S}\left[\int_0^{\frac{\delta T_S}{2}}\left(I_{L1}{}^2+\left(\frac{I_f}{\frac{\delta T_S}{2}}\right)^2 t^2+\frac{2I_{L1}I_f t}{\frac{\delta T_S}{2}}\right)dt+\int_0^{\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}}\left(I_{L2}{}^2+\left(\frac{I_r}{\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}}\right)^2 t^2+\frac{2I_{L2}I_r t}{\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}}\right)dt+\int_0^{t_B}\left(I_P^2+\left(\frac{I_P}{t_B}\right)^2 t^2-\frac{2I_P^2 t}{t_B}\right)dt\right]}$$

Simplifying further gives the RMS current equation of LV side leading diode

$$I_{RMS}=\sqrt{\frac{1}{T_S}\left[\left(I_{L1}^2+\frac{I_f^2}{3}+I_{L1}I_f\right)\times\frac{\delta T_S}{2}+\left(\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}\right)\times\left(I_{L2}^2+\frac{I_r^2}{3}+I_{L2}I_r\right)+\frac{I_P^2\times(t_B)}{3}\right]} \qquad \text{(C.19)}$$

C.2.1.1.5 LV side lagging transistor RMS current derivation

The instantaneous current with their effective intervals is expressed as,

$$I(t) = \frac{I_{L1}}{\frac{dT_S}{2}-t_B}t, 0 < t < \frac{dT_S}{2}-t_B$$

$$= I_{L1}+\frac{I_f t}{\frac{\delta T_S}{2}}, 0 < t < \frac{\delta T_S}{2}$$

Then squaring the above current gives,

$$I^2(t) = \left(\frac{I_{L1}}{\frac{dT_S}{2}-t_B}\right)^2 t^2, 0 < t < \frac{dT_S}{2}-t_B$$

$$= I_{L1}{}^2+\left(\frac{I_f}{\frac{\delta T_S}{2}}\right)^2 t^2+\frac{2I_{L1}I_f t}{\frac{\delta T_S}{2}}, 0 < t < \frac{\delta T_S}{2}$$

RMS equation,

$$I_{RMS} = \sqrt{\frac{1}{T_S}\int_0^{T_S} I^2(t)\,dt}$$

Substituting the squared current in the above equation,

$$I_{RMS}=\sqrt{\frac{1}{T_S}\left[\int_0^{\frac{dT_S}{2}-t_B}\left(\frac{I_{L1}}{\frac{dT_S}{2}-t_B}\right)^2 t^2dt+\int_0^{\frac{\delta T_S}{2}}\left({I_{L1}}^2+\left(\frac{I_f}{\frac{\delta T_S}{2}}\right)^2 t^2+\frac{2I_{L1}I_f t}{\frac{\delta T_S}{2}}\right)dt\right]}$$

Simplifying further gives the RMS current equation of LV side lagging transistor

$$I_{RMS}=\sqrt{\frac{1}{T_S}\left[\frac{I_{L1}^2\times\left(\frac{dT_S}{2}-t_B\right)}{3}+\left(I_{L1}^2+\frac{I_f^2}{3}+I_{L1}I_f\right)\times\frac{\delta T_S}{2}\right]} \quad \text{(C.20)}$$

C.2.1.1.6 LV side lagging diode RMS current derivation

The instantaneous current with their effective intervals is expressed as,

$$I(t)=I_{L2}+\frac{I_r t}{\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}},0<t<\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}$$

$$=I_P-\frac{I_P t}{t_B},0<t<t_B$$

Then squaring the above current gives,

$$I^2(t)={I_{L2}}^2+\left(\frac{I_r}{\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}}\right)^2 t^2+\frac{2I_{L2}I_r t}{\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}},0<t<\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}$$

$$=I_P^2+\left(\frac{I_P}{t_B}\right)^2 t^2-\frac{2I_P^2 t}{t_B},0<t<t_B$$

RMS equation,

$$I_{RMS}=\sqrt{\frac{1}{T_S}\int_0^{T_S} I^2(t)dt}$$

Substituting the squared current in the above equation,

$$I_{RMS}=\sqrt{\frac{1}{T_S}\left[\int_0^{\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}}\left({I_{L2}}^2+\left(\frac{I_r}{\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}}\right)^2 t^2+\frac{2I_{L2}I_r t}{\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}}\right)dt+\int_0^{t_B}\left(I_P^2+\left(\frac{I_P}{t_B}\right)^2 t^2-\frac{2I_P^2 t}{t_B}\right)dt\right]}$$

Simplifying further gives the RMS current equation of LV side leading diode

$$I_{RMS}=\sqrt{\frac{1}{T_S}\left[\left(\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}\right)\times\left(I_{L2}^2+\frac{I_r^2}{3}+I_{L2}I_r\right)+\frac{I_P^2\times(t_B)}{3}\right]} \quad \text{(C.21)}$$

C.2.2 Boost mode

Figure C.4 illustrates the waveforms of inductor and various device currents of the converter under boost mode. Waveforms are labelled and various time intervals are also indicated in Figure C.4. Similar to the previous mode, equation of the instantaneous current of transformer/inductor over a half cycle, expressed in terms of their effective intervals is given by the following.

$$I(t) = \frac{I_{L1}}{\frac{dT_S}{2} - t_B} t, 0 < t < \frac{dT_S}{2} - t_B$$

$$= I_{L1} + \frac{I_f t}{\frac{\delta T_S}{2}}, 0 < t < \frac{\delta T_S}{2}$$

$$= I_P - \frac{I_r t}{\frac{T_S}{2} - \frac{dT_S}{2} - \frac{\delta T_S}{2}}, 0 < t < \frac{T_S}{2} - \frac{dT_S}{2} - \frac{\delta T_S}{2}$$

$$= I_{L2} - \frac{I_{L2} t}{t_B}, 0 < t < t_B$$

Squaring the current,

$$I^2(t) = \left(\frac{I_{L1}}{\frac{dT_S}{2} - t_B} \right)^2 t^2, 0 < t < \frac{dT_S}{2} - t_B$$

$$= {I_{L1}}^2 + \left(\frac{I_f}{\frac{\delta T_S}{2}} \right)^2 t^2 + \frac{2 I_{L1} I_f t}{\frac{\delta T_S}{2}}, 0 < t < \frac{\delta T_S}{2}$$

$$= {I_P}^2 + \left(\frac{I_r}{\frac{T_S}{2} - \frac{dT_S}{2} - \frac{\delta T_S}{2}} \right)^2 t^2 - \frac{2 I_P I_r t}{\frac{T_S}{2} - \frac{dT_S}{2} - \frac{\delta T_S}{2}}, 0 < t < \frac{T_S}{2} - \frac{dT_S}{2} - \frac{\delta T_S}{2}$$

$$= {I_{L2}}^2 + \left(\frac{I_{L2}}{t_B} \right)^2 t^2 - \frac{2 {I_{L2}}^2 t}{t_B}, 0 < t < t_B$$

$$I_{RMS} = \sqrt{\frac{2}{T_S} \int_0^{\frac{T_s}{2}} I^2(t)\, dt}$$

Substituting the squared current for a half cycle gives,

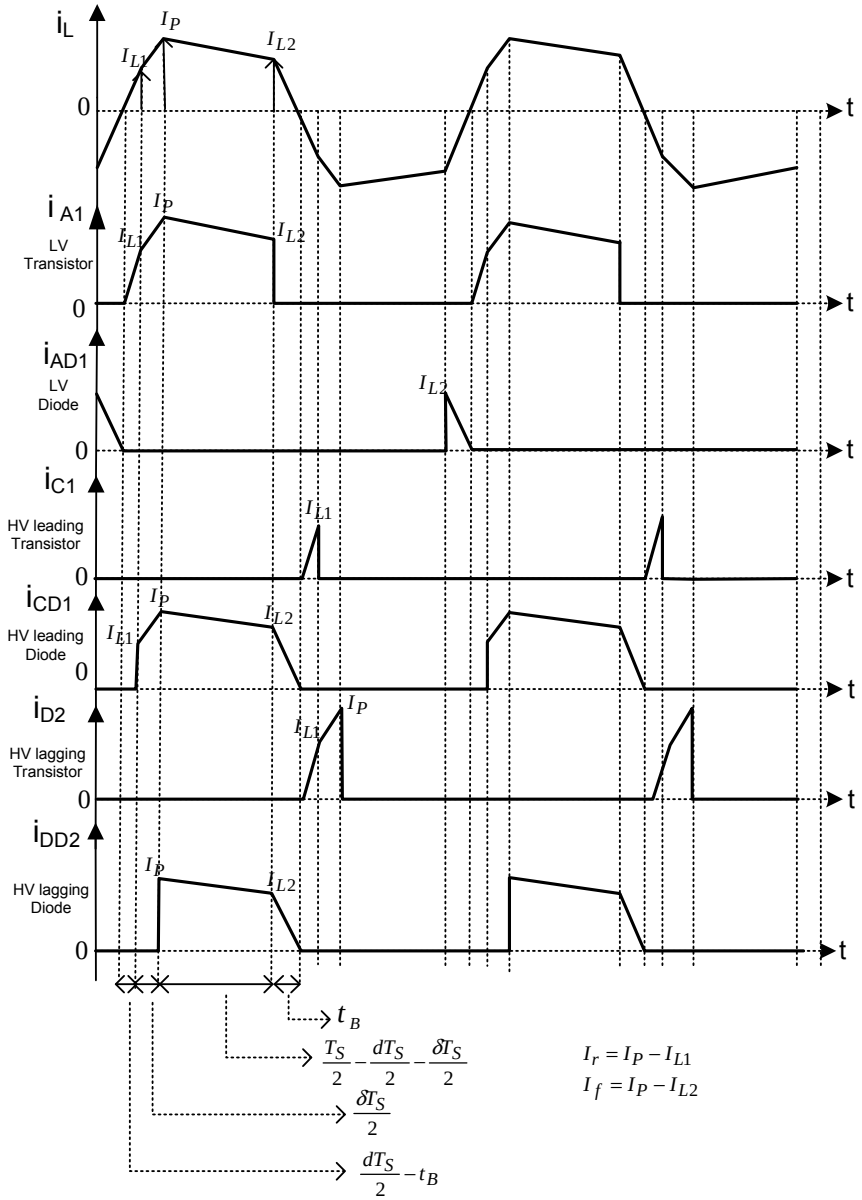

Figure C.4. Inductor and device currents of the DAB converter under boost mode with quasi-square-wave on transformer secondary

$$I_{RMS}=\sqrt{\frac{2}{T_S}\left[\int_0^{\frac{dT_S}{2}-t_B}\left(\frac{I_{L1}}{\frac{dT_S}{2}-t_B}\right)^2 t^2dt+\int_0^{\frac{\delta T_S}{2}}\left(I_{L1}{}^2+\left(\frac{I_f}{\frac{\delta T_S}{2}}\right)^2 t^2+\frac{2I_{L1}I_f t}{\frac{\delta T_S}{2}}\right)dt+\int_0^{\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}}\left(I_P{}^2+\left(\frac{I_r}{\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}}\right)^2 t^2-\frac{2I_P I_r t}{\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}}\right)dt+\int_0^{t_B}\left(I_{L2}{}^2+\left(\frac{I_{L2}}{t_B}\right)^2 t^2-\frac{2I_{L2}{}^2 t}{t_B}\right)dt\right]}$$

On simplifying further,

$$= \sqrt{\frac{2}{T_S}\left[\left(\frac{I_{L1}}{\frac{dT_S}{2}-t_B}\right)^2\frac{\left(\frac{dT_S}{2}-t_B\right)^3}{3}+\left(I_{L1}^2\left(\frac{\delta T_S}{2}\right)+\left(\frac{I_f}{\frac{\delta T_S}{2}}\right)^2\frac{\left(\frac{\delta T_S}{2}\right)^3}{3}+\frac{2I_{L1}I_f}{\frac{\delta T_S}{2}}\frac{\left(\frac{\delta T_S}{2}\right)^2}{2}\right)+\right.}$$

$$\sqrt{\left.I_P^2\left(\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}\right)+\left(\frac{I_r}{\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}}\right)^2\frac{\left(\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}\right)^3}{3}-\frac{2I_PI_rt}{\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}}\frac{\left(\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}\right)^2}{2}\right)+\left(I_{L2}^2t_B+\left(\frac{I_{L2}}{t_B}\right)^2\frac{t_B^3}{3}-\frac{2I_{L2}^2t_B^2}{t_B}\frac{}{2}\right)\right]}$$

RMS value of transformer/inductor current equation during boost mode is found to be,

$$I_{RMS}=\sqrt{\frac{2}{T_S}\left[\frac{(I_{L1})^2\left(\frac{dT_S}{2}-t_B\right)}{3}+\frac{\delta T_S}{2}\left(I_{L1}^2+\frac{I_f^2}{3}+I_{L1}I_f\right)+\left(\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}\right)\left(I_P^2+\frac{I_r^2}{3}-I_PI_r\right)+\frac{I_{L2}^2t_B}{3}\right]} \quad \text{(C.22)}$$

Same procedure as that of the buck mode is applied to derive the equations for device currents as shown in Figure C.4 during boost mode of operation. These are given below.

LV side transistor RMS current

$$I_{RMS}=\sqrt{\frac{1}{T_S}\left[\frac{I_{L1}^2\times\left(\frac{dT_S}{2}-t_B\right)}{3}+\left(I_{L1}^2+\frac{I_f^2}{3}+I_{L1}I_f\right)\times\frac{\delta T_S}{2}+\left(\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}\right)\times\left(I_P^2+\frac{I_r^2}{3}-I_PI_r\right)\right]} \quad \text{(C.23)}$$

LV side diode RMS current is given as,

$$I_{RMS}=\sqrt{\frac{1}{T_S}\left[\frac{I_{L2}^2\times(t_B)}{3}\right]} \quad \text{(C.24)}$$

HV side leading transistor RMS current is given as,

$$I_{RMS}=\sqrt{\frac{1}{T_S}\left[\frac{I_{L1}^2\times\left(\frac{dT_S}{2}-t_B\right)}{3}\right]} \quad \text{(C.25)}$$

HV side leading diode current is expressed as,

$$I_{RMS}=\sqrt{\frac{1}{T_S}\left[\left(\frac{\delta T_S}{2}\right)\times\left(I_{L1}^2+\frac{I_f^2}{3}+I_{L1}I_f\right)+\left(\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}\right)\times\left(I_P^2+\frac{I_r^2}{3}-I_PI_r\right)+\frac{I_{L2}^2\times(t_B)}{3}\right]} \quad \text{(C.26)}$$

HV side lagging transistor current is expressed as,

$$I_{RMS}=\sqrt{\frac{1}{T_S}\left[\frac{I_{L1}^2\times\left(\frac{dT_S}{2}-t_B\right)}{3}+\left(\frac{\delta T_S}{2}\right)\times\left(I_{L1}^2+\frac{I_f^2}{3}+I_{L1}I_f\right)\right]} \quad \text{(C.27)}$$

HV side lagging diode current is given as,

$$I_{RMS}=\sqrt{\frac{1}{T_S}\left[\left(\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta T_S}{2}\right)\times\left(I_P^2+\frac{I_r^2}{3}-I_P I_r\right)+\frac{I_{L2}^2\times t_B}{3}\right]} \quad \text{(C.28)}$$

C.3 RMS current derivation for quasi-square-wave applied on transformer primary and secondary

C.3.1 Buck mode

Figure C.5 depicts the inductor current and various device current waveforms of the converter under buck mode with quasi-square-wave on transformer primary and secondary. Equation of the instantaneous current of transformer/inductor over a half cycle is expressed in terms of their effective intervals as,

$$I(t)=\frac{I_{L1}}{\frac{dT_S}{2}-t_B}t,0<t<\frac{dT_S}{2}-t_B$$

$$=I_{L1}+\frac{I_{r2}t}{\frac{\delta_0 T_S}{2}},0<t<\frac{\delta_0 T_S}{2}$$

$$=I_{L2}+\frac{I_{r1}t}{\frac{T_S}{2}-\frac{dT_S}{2}-\delta T_S},0<t<\frac{T_S}{2}-\frac{dT_S}{2}-\delta T_S$$

$$=I_P-\frac{I_f t}{\frac{\delta_i T_S}{2}},0<t<\frac{\delta_i T_S}{2}$$

$$=I_{L3}-\frac{I_{L3}t}{t_B},0<t<t_B$$

Squaring the current,

$$I^2(t)=\left(\frac{I_{L1}}{\frac{dT_S}{2}-t_B}\right)^2 t^2,0<t<\frac{dT_S}{2}-t_B$$

$$= I_{L1}^{\,2} + \left(\frac{I_{r2}}{\frac{\delta_0 T_S}{2}} \right)^2 t^2 + \frac{2 I_{L1} I_{r2} t}{\frac{\delta_0 T_S}{2}}, 0 < t < \frac{\delta_0 T_S}{2}$$

$$= I_{L2}^{\,2} + \left(\frac{I_{r1}}{\frac{T_S}{2} - \frac{dT_S}{2} - \delta T_S} \right)^2 t^2 + \frac{2 I_{L2} I_{r1} t}{\frac{T_S}{2} - \frac{dT_S}{2} - \delta T_S}, 0 < t < \frac{T_S}{2} - \frac{dT_S}{2} - \delta T_S$$

$$= I_P^{\,2} + \left(\frac{I_f}{\frac{\delta_i T_S}{2}} \right)^2 t^2 - \frac{2 I_P I_f t}{\frac{\delta_i T_S}{2}}, 0 < t < \frac{\delta_i T_S}{2}$$

$$= I_{L3}^{\,2} + \left(\frac{I_{L3}}{t_B} \right)^2 t^2 - \frac{2 I_{L3}^{\,2} t}{t_B}, 0 < t < t_B$$

$$I_{RMS} = \sqrt{\frac{2}{T_S} \int_0^{\frac{T_S}{2}} I^2(t)\, dt}$$

Substituting the squared current over a half cycle gives,

$$I_{RMS} = \sqrt{\frac{2}{T_S}\left[\int_0^{\frac{dT_S}{2} - t_B} \left(\frac{I_{L1}}{\frac{dT_S}{2} - t_B} \right)^2 t^2 dt + \int_0^{\frac{\delta_0 T_S}{2}} \left(I_{L1}^{\,2} + \left(\frac{I_{r2}}{\frac{\delta_0 T_S}{2}} \right)^2 t^2 + \frac{2 I_{L1} I_{r2} t}{\frac{\delta_0 T_S}{2}} \right) dt + \int_0^{\frac{T_S}{2} - \frac{dT_S}{2} - \delta T_S} \left(I_{L2}^{\,2} + \left(\frac{I_{r1}}{\frac{T_S}{2} - \frac{dT_S}{2} - \delta T_S} \right)^2 t^2 + \frac{2 I_{L2} I_{r1} t}{\frac{T_S}{2} - \frac{dT_S}{2} - \delta T_S} \right) dt + \int_0^{\frac{\delta_i T_S}{2}} \left(I_P^{\,2} + \left(\frac{I_f}{\frac{\delta_i T_S}{2}} \right)^2 t^2 - \frac{2 I_P I_f t}{\frac{\delta_i T_S}{2}} \right) dt + \int_0^{t_B} \left(I_{L3}^{\,2} + \left(\frac{I_{L3}}{t_B} \right)^2 t^2 - \frac{2 I_{L3}^{\,2} t}{t_B} \right) dt \right]}$$

Reducing further,

$$= \sqrt{\frac{2}{T_S}\left[\left(\frac{I_{L1}}{\frac{dT_S}{2} - t_B} \right)^2 \frac{\left(\frac{dT_S}{2} - t_B \right)^3}{3} + \left(I_{L1}^{\,2} \left(\frac{\delta_0 T_S}{2} \right) + \left(\frac{I_{r2}}{\frac{\delta_0 T_S}{2}} \right)^2 \frac{\left(\frac{\delta_0 T_S}{2} \right)^3}{3} + \frac{2 I_{L1} I_{r2}}{\frac{\delta_0 T_S}{2}} \frac{\left(\frac{\delta_0 T_S}{2} \right)^2}{2} \right) + \left(I_P^{\,2} \left(\frac{\delta_i T_S}{2} \right) + \left(\frac{I_f}{\frac{\delta_i T_S}{2}} \right)^2 \frac{\left(\frac{\delta_i T_S}{2} \right)^3}{3} - \frac{2 I_P I_f}{\frac{\delta_i T_S}{2}} \frac{\left(\frac{\delta_i T_S}{2} \right)^2}{2} \right) \right.$$
$$\left. + \left(I_{L2}^{\,2} \left(\frac{T_S}{2} - \frac{dT_S}{2} - \delta T_S \right) + \left(\frac{I_{r1}}{\frac{T_S}{2} - \frac{dT_S}{2} - \delta T_S} \right)^2 \frac{\left(\frac{T_S}{2} - \frac{dT_S}{2} - \delta T_S \right)^3}{3} + \frac{2 I_{L2} I_{r1} t}{\frac{T_S}{2} - \frac{dT_S}{2} - \delta T_S} \frac{\left(\frac{T_S}{2} - \frac{dT_S}{2} - \delta T_S \right)^2}{2} \right) + \left(I_{L3}^{\,2} t_B + \left(\frac{I_{L3}}{t_B} \right)^2 \frac{t_B^{\,3}}{3} - \frac{2 I_{L3}^{\,2}}{t_B} \frac{t_B^{\,2}}{2} \right) \right]}$$

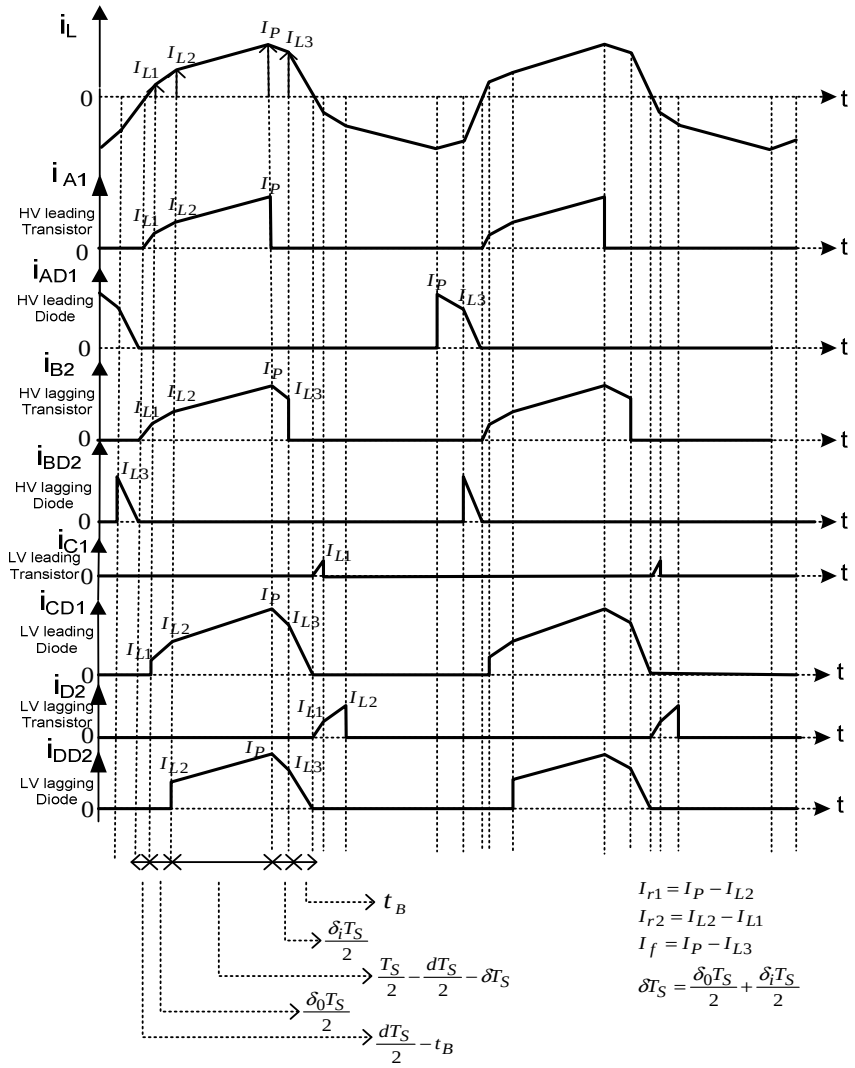

Figure C.5. Inductor and device currents of the DAB converter under buck mode with quasi-square-wave on transformer primary and secondary

RMS value of transformer/inductor current equation for $\delta_i \neq \delta_0$ is found to be,

$$I_{RMS}=\sqrt{\frac{2}{T_S}\left[\frac{(I_{L1})^2\left(\frac{dT_S}{2}-t_B\right)}{3}+\frac{\delta_0 T_S}{2}\left(I_{L1}^2+\frac{I_{r2}^2}{3}+I_{L1}I_{r2}\right)+\left(\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta_i T_S}{2}-\frac{\delta_0 T_S}{2}\right)\left(I_{L2}^2+\frac{I_{r1}^2}{3}+I_{L2}I_{r1}\right)+\frac{\delta_i T_S}{2}\left(I_P^2+\frac{I_f^2}{3}-I_P I_f\right)+\frac{I_{L3}^2 t_B}{3}\right]} \quad \text{(C.29)}$$

When equal dead-time is applied on both the sides, i.e. $\delta_i = \delta_0$,

$$I_{RMS}=\sqrt{\frac{2}{T_S}\left[\frac{(I_{L1})^2\left(\frac{dT_S}{2}-t_B\right)}{3}+\frac{\delta T_S}{2}\left(I_{L1}^{\ 2}+\frac{I_{r2}^{\ 2}}{3}+I_{L1}I_{r2}+I_P^{\ 2}+\frac{I_f^{\ 2}}{3}-I_PI_f\right)+\left(\frac{T_S}{2}-\frac{dT_S}{2}-\delta T_S\right)\left(I_{L2}^{\ 2}+\frac{I_{r1}^{\ 2}}{3}+I_{L2}I_{r1}\right)+\frac{I_{L3}^{\ 2}t_B}{3}\right]} \quad \text{(C.30)}$$

C.3.1.1 Transistors and diodes RMS current derivation

C.3.1.1.1 HV side leading transistor RMS current derivation

Instantaneous current of HV side leading transistor over the effective intervals are

$$I(t)=\frac{I_{L1}}{\frac{dT_S}{2}-t_B}t,0<t<\frac{dT_S}{2}-t_B$$

$$=I_{L1}+\frac{I_{r2}t}{\frac{\delta_0 T_S}{2}},0<t<\frac{\delta_0 T_S}{2}$$

$$=I_{L2}+\frac{I_{r1}t}{\frac{T_S}{2}-\frac{dT_S}{2}-\delta T_S},0<t<\frac{T_S}{2}-\frac{dT_S}{2}-\delta T_S$$

Squaring the current,

$$I^2(t)=\left(\frac{I_{L1}}{\frac{dT_S}{2}-t_B}\right)^2t^2,0<t<\frac{dT_S}{2}-t_B$$

$$=I_{L1}^{\ 2}+\left(\frac{I_{r2}}{\frac{\delta_0 T_S}{2}}\right)^2t^2+\frac{2I_{L1}I_{r2}t}{\frac{\delta_0 T_S}{2}},0<t<\frac{\delta_0 T_S}{2}$$

$$=I_{L2}^{\ 2}+\left(\frac{I_{r1}}{\frac{T_S}{2}-\frac{dT_S}{2}-\delta T_S}\right)^2t^2+\frac{2I_{L2}I_{r1}t}{\frac{T_S}{2}-\frac{dT_S}{2}-\delta T_S},0<t<\frac{T_S}{2}-\frac{dT_S}{2}-\delta T_S$$

$$I_{RMS}=\sqrt{\frac{1}{T_S}\int_0^{T_S}I^2(t)dt}$$

Substituting the squared current gives,

$$I_{RMS}=\sqrt{\frac{1}{T_S}\left[\int_0^{\frac{dT_S}{2}-t_B}\left(\frac{I_{L1}}{\frac{dT_S}{2}-t_B}\right)^2 t^2dt+\int_0^{\frac{\delta_0 T_S}{2}}\left(I_{L1}^2+\left(\frac{I_{r2}}{\frac{\delta_0 T_S}{2}}\right)^2 t^2+\frac{2I_{L1}I_{r2}t}{\frac{\delta_0 T_S}{2}}\right)dt+\int_0^{\frac{T_S}{2}-\frac{dT_S}{2}-\delta T_S}\left(I_{L2}^2+\left(\frac{I_{r1}}{\frac{T_S}{2}-\frac{dT_S}{2}-\delta T_S}\right)^2 t^2+\frac{2I_{L2}I_{r1}t}{\frac{T_S}{2}-\frac{dT_S}{2}-\delta T_S}\right)dt\right]}$$

Reducing further,

$$=\sqrt{\frac{1}{T_S}\left[\left(\frac{I_{L1}}{\frac{dT_S}{2}-t_B}\right)^2\frac{\left(\frac{dT_S}{2}-t_B\right)^3}{3}+\left(I_{L1}^2\left(\frac{\delta_0 T_S}{2}\right)+\left(\frac{I_{r2}}{\frac{\delta_0 T_S}{2}}\right)^2\frac{\left(\frac{\delta_0 T_S}{2}\right)^3}{3}+\frac{2I_{L1}I_{r2}}{\frac{\delta_0 T_S}{2}}\frac{\left(\frac{\delta_0 T_S}{2}\right)^2}{2}\right)+\left(I_{L2}^2\left(\frac{T_S}{2}-\frac{dT_S}{2}-\delta T_S\right)+\left(\frac{I_{r1}}{\frac{T_S}{2}-\frac{dT_S}{2}-\delta T_S}\right)^2\frac{\left(\frac{T_S}{2}-\frac{dT_S}{2}-\delta T_S\right)^3}{3}+\frac{2I_{L2}I_{r1}t}{\frac{T_S}{2}-\frac{dT_S}{2}-\delta T_S}\frac{\left(\frac{T_S}{2}-\frac{dT_S}{2}-\delta T_S\right)^2}{2}\right)\right]}$$

RMS value of leading transistor on HV side is found to be,

$$I_{RMS}=\sqrt{\frac{1}{T_S}\left[\frac{(I_{L1})^2\left(\frac{dT_S}{2}-t_B\right)}{3}+\frac{\delta_0 T_S}{2}\left(I_{L1}^2+\frac{I_{r2}^2}{3}+I_{L1}I_{r2}\right)+\left(\frac{T_S}{2}-\frac{dT_S}{2}-\delta T_S\right)\left(I_{L2}^2+\frac{I_{r1}^2}{3}+I_{L2}I_{r1}\right)\right]} \quad \text{(C.31)}$$

C.3.1.1.2 HV side leading diode RMS current derivation

Equation derived in section C.1.1.1.2 is hold good for this HV side leading diode current with I_{L2} replaced by I_{L3} and δ replaced by δ_i which is given as,

$$I_{RMS}=\sqrt{\frac{1}{T_S}\left[\left(\frac{\delta_i T_S}{2}\right)\times\left(I_P^2+\frac{I_f^2}{3}-I_P I_f\right)+\frac{I_{L3}^2\times(t_B)}{3}\right]} \quad \text{(C.32)}$$

C.3.1.1.3 HV side lagging transistor RMS current derivation

Equation of the instantaneous current of the transistor is expressed in terms of their effective intervals as,

$$I(t)=\frac{I_{L1}}{\frac{dT_S}{2}-t_B}t, 0<t<\frac{dT_S}{2}-t_B$$

$$=I_{L1}+\frac{I_{r2}t}{\frac{\delta_0 T_S}{2}}, 0<t<\frac{\delta_0 T_S}{2}$$

$$=I_{L2}+\frac{I_{r1}t}{\frac{T_S}{2}-\frac{dT_S}{2}-\delta T_S}, 0<t<\frac{T_S}{2}-\frac{dT_S}{2}-\delta T_S$$

$$= I_P - \frac{I_f t}{\frac{\delta_i T_S}{2}}, 0 < t < \frac{\delta_i T_S}{2}$$

Squaring the current,

$$I^2(t) = \left(\frac{I_{L1}}{\frac{dT_S}{2} - t_B} \right)^2 t^2, 0 < t < \frac{dT_S}{2} - t_B$$

$$= {I_{L1}}^2 + \left(\frac{I_{r2}}{\frac{\delta_0 T_S}{2}} \right)^2 t^2 + \frac{2 I_{L1} I_{r2} t}{\frac{\delta_0 T_S}{2}}, 0 < t < \frac{\delta_0 T_S}{2}$$

$$= {I_{L2}}^2 + \left(\frac{I_{r1}}{\frac{T_S}{2} - \frac{dT_S}{2} - \delta T_S} \right)^2 t^2 + \frac{2 I_{L2} I_{r1} t}{\frac{T_S}{2} - \frac{dT_S}{2} - \delta T_S}, 0 < t < \frac{T_S}{2} - \frac{dT_S}{2} - \delta T_S$$

$$= {I_P}^2 + \left(\frac{I_f}{\frac{\delta_i T_S}{2}} \right)^2 t^2 - \frac{2 I_P I_f t}{\frac{\delta_i T_S}{2}}, 0 < t < \frac{\delta_i T_S}{2}$$

$$I_{RMS} = \sqrt{\frac{1}{T_S} \int_0^{T_S} I^2(t)\, dt}$$

Substituting the squared current gives,

$$I_{RMS} = \sqrt{\frac{1}{T_S}\left[\int_0^{\frac{dT_S}{2} - t_B} \left(\frac{I_{L1}}{\frac{dT_S}{2} - t_B} \right)^2 t^2 dt + \int_0^{\frac{\delta_0 T_S}{2}} \left({I_{L1}}^2 + \left(\frac{I_{r2}}{\frac{\delta_0 T_S}{2}} \right)^2 t^2 + \frac{2 I_{L1} I_{r2} t}{\frac{\delta_0 T_S}{2}} \right) dt + \int_0^{\frac{T_S}{2} - \frac{dT_S}{2} - \delta T_S} \left({I_{L2}}^2 + \left(\frac{I_{r1}}{\frac{T_S}{2} - \frac{dT_S}{2} - \delta T_S} \right)^2 t^2 + \frac{2 I_{L2} I_{r1} t}{\frac{T_S}{2} - \frac{dT_S}{2} - \delta T_S} \right) dt + \int_0^{\frac{\delta_i T_S}{2}} \left({I_P}^2 + \left(\frac{I_f}{\frac{\delta_i T_S}{2}} \right)^2 t^2 - \frac{2 I_P I_f t}{\frac{\delta_i T_S}{2}} \right) dt \right]}$$

Simplifying further gives the equation for RMS current of HV side lagging transistor as,

$$I_{RMS} = \sqrt{\frac{1}{T_S}\left[\frac{I_{L1}^2 \times \left(\frac{dT_S}{2} - t_B \right)}{3} + \left(\frac{\delta_0 T_S}{2} \right) \times \left(I_{L1}^2 + \frac{I_{r2}^2}{3} + I_{L1} I_{r2} \right) + \left(\frac{T_S}{2} - \frac{dT_S}{2} - \delta T_S \right) \times \left(I_{L2}^2 + \frac{I_{r1}^2}{3} + I_{L2} I_{r1} \right) + \left(\frac{\delta_i T_S}{2} \right) \times \left(I_P^2 + \frac{I_f^2}{3} - I_P I_f \right) \right]} \quad \text{(C.33)}$$

C.3.1.1.4 HV side lagging diode RMS current derivation

Equation derived in section C.1.1.1.4 hold good for this HV side lagging diode current with I_{L2} replaced by I_{L3}. This is given as,

$$I_{RMS} = \sqrt{\frac{1}{T_S}\left[\frac{I_{L3}^2 \times (t_B)}{3}\right]} \quad \text{(C.34)}$$

C.3.1.1.5 LV side leading transistor RMS current derivation

Equation derived in section C.1.1.1.5 hold good for this LV side leading transistor current which is given by,

$$I_{RMS} = \sqrt{\frac{1}{T_S}\left[\frac{I_{L1}^2 \times \left(\frac{dT_S}{2} - t_B\right)}{3}\right]} \quad \text{(C.35)}$$

C.3.1.1.6 LV side leading diode RMS current derivation

Equation of the instantaneous current of LV side leading diode is expressed in terms of their effective intervals as,

$$I(t) = I_{L1} + \frac{I_{r2}t}{\frac{\delta_0 T_S}{2}}, 0 < t < \frac{\delta_0 T_S}{2}$$

$$= I_{L2} + \frac{I_{r1}t}{\frac{T_S}{2} - \frac{dT_S}{2} - \delta T_S}, 0 < t < \frac{T_S}{2} - \frac{dT_S}{2} - \delta T_S$$

$$= I_P - \frac{I_f t}{\frac{\delta_i T_S}{2}}, 0 < t < \frac{\delta_i T_S}{2}$$

$$= I_{L3} - \frac{I_{L3}t}{t_B}, 0 < t < t_B$$

Squaring the current,

$$I^2(t) = {I_{L1}}^2 + \left(\frac{I_{r2}}{\frac{\delta_0 T_S}{2}}\right)^2 t^2 + \frac{2 I_{L1} I_{r2} t}{\frac{\delta_0 T_S}{2}}, 0 < t < \frac{\delta_0 T_S}{2}$$

$$= {I_{L2}}^2 + \left(\frac{I_{r1}}{\frac{T_S}{2} - \frac{dT_S}{2} - \delta T_S}\right)^2 t^2 + \frac{2 I_{L2} I_{r1} t}{\frac{T_S}{2} - \frac{dT_S}{2} - \delta T_S}, 0 < t < \frac{T_S}{2} - \frac{dT_S}{2} - \delta T_S$$

$$= {I_P}^2 + \left(\frac{I_f}{\frac{\delta_i T_S}{2}}\right)^2 t^2 - \frac{2 I_P I_f t}{\frac{\delta_i T_S}{2}}, 0 < t < \frac{\delta_i T_S}{2}$$

$$= I_{L3}^{\ 2} + \left(\frac{I_{L3}}{t_B}\right)^2 t^2 - \frac{2 I_{L3}^{\ 2} t}{t_B}, 0 < t < t_B$$

$$I_{RMS} = \sqrt{\frac{1}{T_S}\int_0^{T_S} I^2(t)\,dt}$$

Substituting the squared current gives,

$$I_{RMS} = \sqrt{\frac{1}{T_S}\left(\int_0^{\frac{\delta_0 T_S}{2}}\left(I_{L1}^2 + \left(\frac{I_{r2}}{\frac{\delta_0 T_S}{2}}\right)^2 t^2 + \frac{2 I_{L1} I_{r2} t}{\frac{\delta_0 T_S}{2}}\right)dt + \int_0^{\frac{T_S}{2}-\frac{dT_S}{2}-\delta T_S}\left(I_{L2}^2 + \left(\frac{I_{r1}}{\frac{T_S}{2}-\frac{dT_S}{2}-\delta T_S}\right)^2 t^2 + \frac{2 I_{L2} I_{r1} t}{\frac{T_S}{2}-\frac{dT_S}{2}-\delta T_S}\right)dt + \int_0^{\frac{\delta_1 T_S}{2}}\left(I_P^2 + \left(\frac{I_f}{\frac{\delta_1 T_S}{2}}\right)^2 t^2 - \frac{2 I_P I_f t}{\frac{\delta_1 T_S}{2}}\right)dt + \int_0^{t_B}\left(I_{L3}^2 + \left(\frac{I_{L3}}{t_B}\right)^2 t^2 - \frac{2 I_{L3}^2 t}{t_B}\right)dt\right)}$$

Simplifying further gives the equation for LV side lagging diode RMS current as,

$$I_{RMS} = \sqrt{\frac{1}{T_S}\left[\left(\frac{\delta_0 T_S}{2}\right)\times\left(I_{L1}^2 + \frac{I_{r2}^2}{3} + I_{L1} I_{r2}\right) + \left(\frac{T_S}{2} - \frac{dT_S}{2} - \delta T_S\right)\times\left(I_{L2}^2 + \frac{I_{r1}^2}{3} + I_{L2} I_{r1}\right) + \left(\frac{\delta_1 T_S}{2}\right)\times\left(I_P^2 + \frac{I_f^2}{3} - I_P I_f\right) + \frac{I_{L3}^2 \times (t_B)}{3}\right]} \quad \text{(C.36)}$$

C.3.1.1.7 LV side lagging transistor RMS current derivation

Instantaneous current of LV side lagging transistor over the effective intervals are

$$I(t) = \frac{I_{L1}}{\frac{dT_S}{2} - t_B} t, 0 < t < \frac{dT_S}{2} - t_B$$

$$= I_{L1} + \frac{I_{r2} t}{\frac{\delta_0 T_S}{2}}, 0 < t < \frac{\delta_0 T_S}{2}$$

Squaring the current,

$$I^2(t) = \left(\frac{I_{L1}}{\frac{dT_S}{2} - t_B}\right)^2 t^2, 0 < t < \frac{dT_S}{2} - t_B$$

$$= I_{L1}^{\ 2} + \left(\frac{I_{r2}}{\frac{\delta_0 T_S}{2}}\right)^2 t^2 + \frac{2 I_{L1} I_{r2} t}{\frac{\delta_0 T_S}{2}}, 0 < t < \frac{\delta_0 T_S}{2}$$

$$I_{RMS} = \sqrt{\frac{1}{T_S}\int_0^{T_S} I^2(t)\,dt}$$

Substituting the squared current gives,

$$I_{RMS}=\sqrt{\frac{1}{T_S}\left[\int_0^{\frac{dT_S}{2}-t_B}\left(\frac{I_{L1}}{\frac{dT_S}{2}-t_B}\right)^2 t^2dt+\int_0^{\frac{\delta_0 T_S}{2}}\left(I_{L1}^2+\left(\frac{I_{r2}}{\frac{\delta_0 T_S}{2}}\right)^2 t^2+\frac{2I_{L1}I_{r2}t}{\frac{\delta_0 T_S}{2}}\right)dt\right]}$$

Reducing further,

$$=\sqrt{\frac{1}{T_S}\left[\left(\frac{I_{L1}}{\frac{dT_S}{2}-t_B}\right)^2\frac{\left(\frac{dT_S}{2}-t_B\right)^3}{3}+\left(I_{L1}^2\left(\frac{\delta_0 T_S}{2}\right)+\left(\frac{I_{r2}}{\frac{\delta_0 T_S}{2}}\right)^2\frac{\left(\frac{\delta_0 T_S}{2}\right)^3}{3}+\frac{2I_{L1}I_{r2}}{\frac{\delta_0 T_S}{2}}\frac{\left(\frac{\delta_0 T_S}{2}\right)^2}{2}\right)\right]}$$

RMS value of lagging transistor on LV side is found to be,

$$I_{RMS}=\sqrt{\frac{1}{T_S}\left[\frac{(I_{L1})^2\left(\frac{dT_S}{2}-t_B\right)}{3}+\frac{\delta_0 T_S}{2}\left(I_{L1}^2+\frac{I_{r2}^2}{3}+I_{L1}I_{r2}\right)\right]} \quad \text{(C.37)}$$

C.3.1.1.8 LV side lagging diode RMS current derivation

Equation of the instantaneous current of LV side lagging diode is expressed in terms of their effective intervals as,

$$I(t)=I_{L2}+\frac{I_{r1}t}{\frac{T_S}{2}-\frac{dT_S}{2}-\delta T_S},0<t<\frac{T_S}{2}-\frac{dT_S}{2}-\delta T_S$$

$$=I_P-\frac{I_f t}{\frac{\delta_i T_S}{2}},0<t<\frac{\delta_i T_S}{2}$$

$$=I_{L3}-\frac{I_{L3}t}{t_B},0<t<t_B$$

Squaring the current,

$$I^2(t)=I_{L2}^2+\left(\frac{I_{r1}}{\frac{T_S}{2}-\frac{dT_S}{2}-\delta T_S}\right)^2 t^2+\frac{2I_{L2}I_{r1}t}{\frac{T_S}{2}-\frac{dT_S}{2}-\delta T_S},0<t<\frac{T_S}{2}-\frac{dT_S}{2}-\delta T_S$$

$$=I_P^2+\left(\frac{I_f}{\frac{\delta_i T_S}{2}}\right)^2 t^2-\frac{2I_P I_f t}{\frac{\delta_i T_S}{2}},0<t<\frac{\delta_i T_S}{2}$$

$$= I_{L3}{}^2 + \left(\frac{I_{L3}}{t_B}\right)^2 t^2 - \frac{2 I_{L3}{}^2 t}{t_B}, 0 < t < t_B$$

$$I_{RMS} = \sqrt{\frac{1}{T_S}\int_0^{T_S} I^2(t)\,dt}$$

Substituting the squared current gives,

$$I_{RMS} = \sqrt{\frac{2}{T_S}\left[\int_0^{\frac{T_S}{2}-\frac{dT_S}{2}-\delta T_S}\left(I_{L2}{}^2 + \left(\frac{I_{r1}}{\frac{T_S}{2}-\frac{dT_S}{2}-\delta T_S}\right)^2 t^2 + \frac{2 I_{L2} I_{r1} t}{\frac{T_S}{2}-\frac{dT_S}{2}-\delta T_S}\right)dt + \int_0^{\frac{\delta_i T_S}{2}}\left(I_P{}^2 + \left(\frac{I_f}{\frac{\delta_i T_S}{2}}\right)^2 t^2 - \frac{2 I_P I_f t}{\frac{\delta_i T_S}{2}}\right)dt + \int_0^{t_B}\left(I_{L3}{}^2 + \left(\frac{I_{L3}}{t_B}\right)^2 t^2 - \frac{2 I_{L3}{}^2 t}{t_B}\right)dt\right]}$$

Minimising further gives the equation for LV side lagging diode RMS current as,

$$I_{RMS} = \sqrt{\frac{1}{T_S}\left[\left(\frac{T_S}{2}-\frac{dT_S}{2}-\delta T_S\right)\times\left(I_{L2}^2 + \frac{I_{r1}^2}{3} + I_{L2} I_{r1}\right) + \left(\frac{\delta_i T_S}{2}\right)\times\left(I_P^2 + \frac{I_f^2}{3} - I_P I_f\right) + \frac{I_{L3}^2\times(t_B)}{3}\right]} \quad \text{(C.38)}$$

C.3.2 Boost mode

Figure C.6 depicts the waveforms of inductor current and device currents of the DAB converter under boost mode with quasi-square-wave on transformer primary and secondary. Waveforms are labelled and the respective time intervals are indicated in Figure C.6. Equation of the instantaneous current of transformer/inductor over a half cycle, expressed in terms of their effective intervals is given by,

$$I(t) = \frac{I_{L1}}{\frac{dT_S}{2} - t_B} t, 0 < t < \frac{dT_S}{2} - t_B$$

$$= I_{L1} + \frac{I_{r1} t}{\frac{\delta_0 T_S}{2}}, 0 < t < \frac{\delta_0 T_S}{2}$$

$$= I_P - \frac{I_{r2} t}{\frac{T_S}{2} - \frac{dT_S}{2} - \delta T_S}, 0 < t < \frac{T_S}{2} - \frac{dT_S}{2} - \delta T_S$$

$$= I_{L2} - \frac{I_f t}{\frac{\delta_i T_S}{2}}, 0 < t < \frac{\delta_i T_S}{2}$$

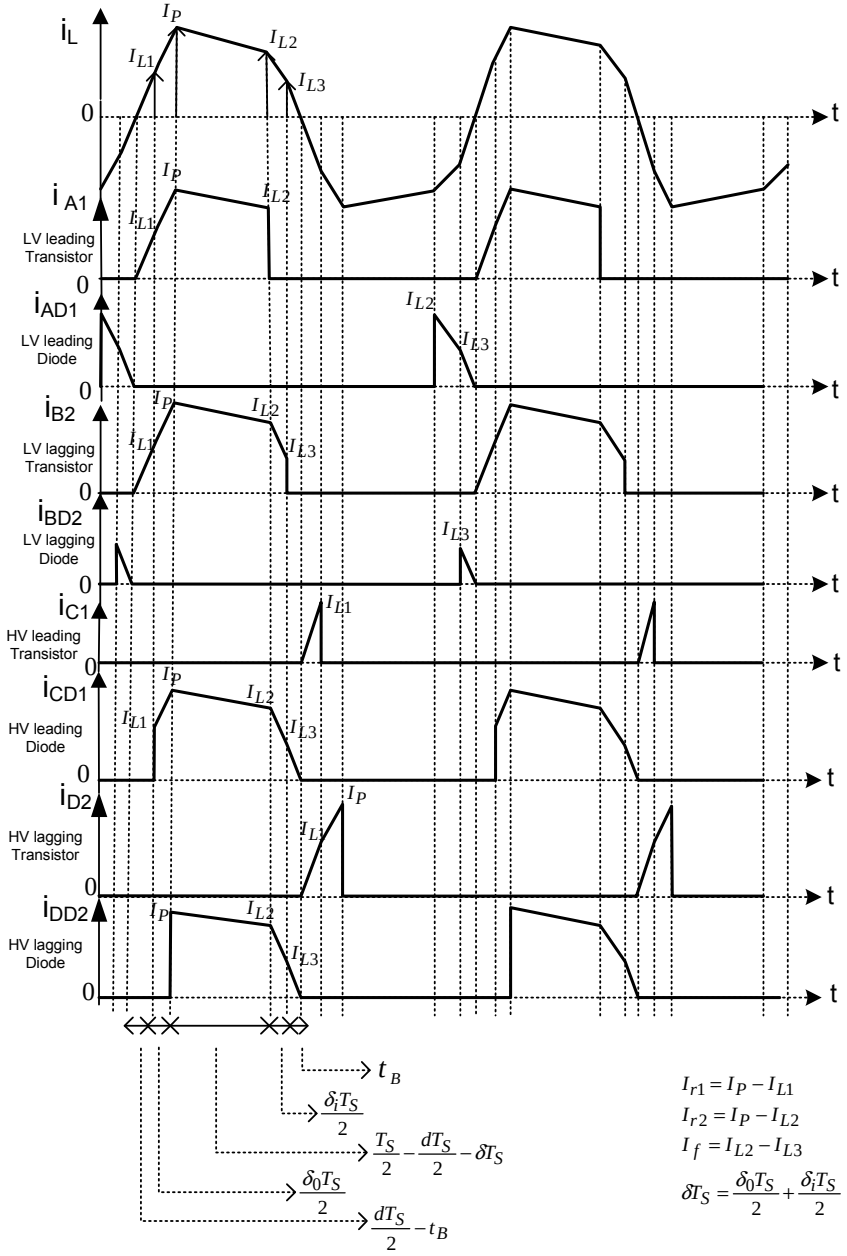

Figure C.6. Inductor and device currents of the DAB converter under boost mode with quasi-square-wave on transformer primary and secondary

$$= I_{L3} - \frac{I_{L3}t}{t_B}, 0 < t < t_B$$

Squaring the current,

$$I^2(t) = \left(\frac{I_{L1}}{\frac{dT_S}{2} - t_B} \right)^2 t^2, 0 < t < \frac{dT_S}{2} - t_B$$

$$= I_{L1}{}^2 + \left(\frac{I_{r1}}{\frac{\delta_0 T_S}{2}}\right)^2 t^2 + \frac{2I_{L1}I_{r1}t}{\frac{\delta_0 T_S}{2}}, 0 < t < \frac{\delta_0 T_S}{2}$$

$$= I_P{}^2 + \left(\frac{I_{r2}}{\frac{T_S}{2} - \frac{dT_S}{2} - \delta T_S}\right)^2 t^2 - \frac{2I_P I_{r2}t}{\frac{T_S}{2} - \frac{dT_S}{2} - \delta T_S}, 0 < t < \frac{T_S}{2} - \frac{dT_S}{2} - \delta T_S$$

$$= I_{L2}{}^2 + \left(\frac{I_f}{\frac{\delta_i T_S}{2}}\right)^2 t^2 - \frac{2I_{L2}I_f t}{\frac{\delta_i T_S}{2}}, 0 < t < \frac{\delta_i T_S}{2}$$

$$= I_{L3}{}^2 + \left(\frac{I_{L3}}{t_B}\right)^2 t^2 - \frac{2I_{L3}{}^2 t}{t_B}, 0 < t < t_B$$

$$I_{RMS} = \sqrt{\frac{2}{T_S}\int_0^{\frac{T_S}{2}} I^2(t)\,dt}$$

Substituting the squared current during the half cycle gives,

$$I_{RMS} = \sqrt{\frac{2}{T_S}\left[\int_0^{\frac{dT_S}{2}-t_B}\left(\frac{I_{L1}}{\frac{dT_S}{2}-t_B}\right)^2 t^2 dt + \int_0^{\frac{\delta_i T_S}{2}}\left(I_{L1}{}^2 + \left(\frac{I_{r1}}{\frac{\delta_0 T_S}{2}}\right)^2 t^2 + \frac{2I_{L1}I_{r1}t}{\frac{\delta_0 T_S}{2}}\right)dt + \int_0^{\frac{T_S}{2}-\frac{dT_S}{2}-\delta T_S}\left(I_P{}^2 + \left(\frac{I_{r2}}{\frac{T_S}{2}-\frac{dT_S}{2}-\delta T_S}\right)^2 t^2 - \frac{2I_P I_{r2}t}{\frac{T_S}{2}-\frac{dT_S}{2}-\delta T_S}\right)dt + \int_0^{\frac{\delta_i T_S}{2}}\left(I_{L2}{}^2 + \left(\frac{I_f}{\frac{\delta_i T_S}{2}}\right)^2 t^2 - \frac{2I_{L2}I_f t}{\frac{\delta_i T_S}{2}}\right)dt + \int_0^{t_B}\left(I_{L3}{}^2 + \left(\frac{I_{L3}}{t_B}\right)^2 t^2 - \frac{2I_{L3}{}^2 t}{t_B}\right)dt\right]}$$

On further simplification,

$$= \sqrt{\frac{2}{T_S}\left[\left(\frac{I_{L1}}{\frac{dT_S}{2}-t_B}\right)^2 \frac{\left(\frac{dT_S}{2}-t_B\right)^3}{3} + \left(I_{L1}{}^2\left(\frac{\delta_0 T_S}{2}\right) + \left(\frac{I_{r1}}{\frac{\delta_0 T_S}{2}}\right)^2 \frac{\left(\frac{\delta_0 T_S}{2}\right)^3}{3} + \frac{2I_{L1}I_{r1}}{\frac{\delta_0 T_S}{2}}\frac{\left(\frac{\delta_0 T_S}{2}\right)^2}{2}\right) + \left(I_{L2}{}^2\left(\frac{\delta_i T_S}{2}\right) + \left(\frac{I_f}{\frac{\delta_i T_S}{2}}\right)^2 \frac{\left(\frac{\delta_i T_S}{2}\right)^3}{3} - \frac{2I_{L2}I_f}{\frac{\delta_i T_S}{2}}\frac{\left(\frac{\delta_i T_S}{2}\right)^2}{2}\right)\right.$$
$$\left. + \left(I_P{}^2\left(\frac{T_S}{2}-\frac{dT_S}{2}-\delta T_S\right) + \left(\frac{I_{r2}}{\frac{T_S}{2}-\frac{dT_S}{2}-\delta T_S}\right)^2 \frac{\left(\frac{T_S}{2}-\frac{dT_S}{2}-\delta T_S\right)^3}{3} - \frac{2I_P I_{r2}t}{\frac{T_S}{2}-\frac{dT_S}{2}-\delta T_S}\frac{\left(\frac{T_S}{2}-\frac{dT_S}{2}-\delta T_S\right)^2}{2}\right) + \left(I_{L3}{}^2 t_B + \left(\frac{I_{L3}}{t_B}\right)^2 \frac{t_B{}^3}{3} - \frac{2I_{L3}{}^2}{t_B}\frac{t_B{}^2}{2}\right)\right]}$$

RMS value of transformer/inductor current equation for $\delta_i \neq \delta_0$ is found to be,

$$I_{RMS}=\sqrt{\frac{2}{T_S}\left[\frac{(I_{L1})^2\left(\frac{dT_S}{2}-t_B\right)}{3}+\frac{\delta_0 T_S}{2}\left(I_{L1}^{\ 2}+\frac{I_{r1}^{\ 2}}{3}+I_{L1}I_{r1}\right)+\left(\frac{T_S}{2}-\frac{dT_S}{2}-\frac{\delta_i T_S}{2}-\frac{\delta_0 T_S}{2}\right)\left(I_P^{\ 2}+\frac{I_{r2}^{\ 2}}{3}-I_P I_{r2}\right)+\frac{\delta_i T_S}{2}\left(I_{L2}^{\ 2}+\frac{I_f^{\ 2}}{3}-I_{L2}I_f\right)+\frac{I_{L3}^{\ 2}t_B}{3}\right]} \quad \text{(C.39)}$$

When equal dead-time is applied on both the sides, i.e. with $\delta_i = \delta_0$,

$$I_{RMS}=\sqrt{\frac{2}{T_S}\left[\frac{(I_{L1})^2\left(\frac{dT_S}{2}-t_B\right)}{3}+\frac{\delta_i T_S}{2}\left(I_{L1}^{\ 2}+\frac{I_{r1}^{\ 2}}{3}+I_{L1}I_{r1}+I_{L2}^{\ 2}+\frac{I_f^{\ 2}}{3}-I_{L2}I_f\right)+\left(\frac{T_S}{2}-\frac{dT_S}{2}-\delta_i T_S\right)\left(I_P^{\ 2}+\frac{I_{r2}^{\ 2}}{3}-I_P I_{r2}\right)+\frac{I_{L3}^{\ 2}t_B}{3}\right]} \quad \text{(C.40)}$$

Since the device currents during boost mode exhibits the similar wave shapes, their RMS current can be obtained by applying the procedure of buck mode device current derivations. These are listed below.

LV side leading transistor RMS current

$$I_{RMS}=\sqrt{\frac{1}{T_S}\left[\frac{I_{L1}^2\times\left(\frac{dT_S}{2}-t_B\right)}{3}+\left(I_{L1}^2+\frac{I_{r1}^2}{3}+I_{L1}I_{r1}\right)\times\frac{\delta_0 T_S}{2}+\left(\frac{T_S}{2}-\frac{dT_S}{2}-\delta_i T_S\right)\times\left(I_P^2+\frac{I_{r2}^2}{3}-I_P I_{r2}\right)\right]} \quad \text{(C.41)}$$

LV side leading diode RMS current is given as,

$$I_{RMS}=\sqrt{\frac{1}{T_S}\left[\left(\frac{\delta_i T_S}{2}\right)\times\left(I_{L2}^2+\frac{I_f^2}{3}-I_{L2}I_f\right)+\frac{I_{L3}^2\times(t_B)}{3}\right]} \quad \text{(C.42)}$$

LV side lagging transistor RMS current is expressed as,

$$I_{RMS}=\sqrt{\frac{1}{T_S}\left[\frac{I_{L1}^2\times\left(\frac{dT_S}{2}-t_B\right)}{3}+\left(\frac{\delta_0 T_S}{2}\right)\times\left(I_{L1}^2+\frac{I_{r1}^2}{3}+I_{L1}I_{r1}\right)+\left(\frac{T_S}{2}-\frac{dT_S}{2}-\delta_i T_S\right)\times\left(I_P^2+\frac{I_{r2}^2}{3}-I_P I_{r2}\right)+\left(\frac{\delta_i T_S}{2}\right)\times\left(I_{L2}^2+\frac{I_f^2}{3}-I_{L2}I_f\right)\right]} \quad \text{(C.43)}$$

LV side lagging diode RMS current is given as,

$$I_{RMS}=\sqrt{\frac{1}{T_S}\left[\frac{I_{L3}^2\times(t_B)}{3}\right]} \quad \text{(C.44)}$$

HV side leading transistor RMS current is given as,

$$I_{RMS}=\sqrt{\frac{1}{T_S}\left[\frac{I_{L1}^2\times\left(\frac{dT_S}{2}-t_B\right)}{3}\right]} \quad \text{(C.45)}$$

HV side leading diode current is expressed as,

$$I_{RMS}=\sqrt{\frac{1}{T_S}\left[\left(\frac{\delta_0 T_S}{2}\right)\times\left(I_{L1}^2+\frac{I_{r1}^2}{3}+I_{L1}I_{r1}\right)+\left(\frac{T_S}{2}-\frac{dT_S}{2}-\delta T_S\right)\times\left(I_P^2+\frac{I_{r2}^2}{3}-I_P I_{r2}\right)+\left(\frac{\delta_1 T_S}{2}\right)\times\left(I_{L2}^2+\frac{I_f^2}{3}-I_{L2}I_f\right)+\frac{I_{L3}^2\times(t_B)}{3}\right]} \quad \text{(C.46)}$$

HV side lagging transistor current is expressed as,

$$I_{RMS}=\sqrt{\frac{1}{T_S}\left[\frac{I_{L1}^2\times\left(\frac{dT_S}{2}-t_B\right)}{3}+\left(I_{L1}^2+\frac{I_{r1}^2}{3}+I_{L1}I_{r1}\right)\times\frac{\delta_0 T_S}{2}\right]} \quad \text{(C.47)}$$

HV side lagging diode current is given as,

$$I_{RMS}=\sqrt{\frac{1}{T_S}\left[\left(\frac{T_S}{2}-\frac{dT_S}{2}-\delta T_S\right)\times\left(I_P^2+\frac{I_{r2}^2}{3}-I_P I_{r2}\right)+\left(\frac{\delta_1 T_S}{2}\right)\times\left(I_{L2}^2+\frac{I_f^2}{3}-I_{L2}I_f\right)+\frac{I_{L3}^2\times(t_B)}{3}\right]} \quad \text{(C.48)}$$

Appendix D

Circuit Diagrams and PCB Layers of Driver and Interface Circuits of the DAB Converter

D.1 Circuit diagram of driver circuit

Figure D.1 shows the schematic of HV side IGBT driver circuit, while the schematic of the LV side IGBT driver circuit is shown in Figure D.2.

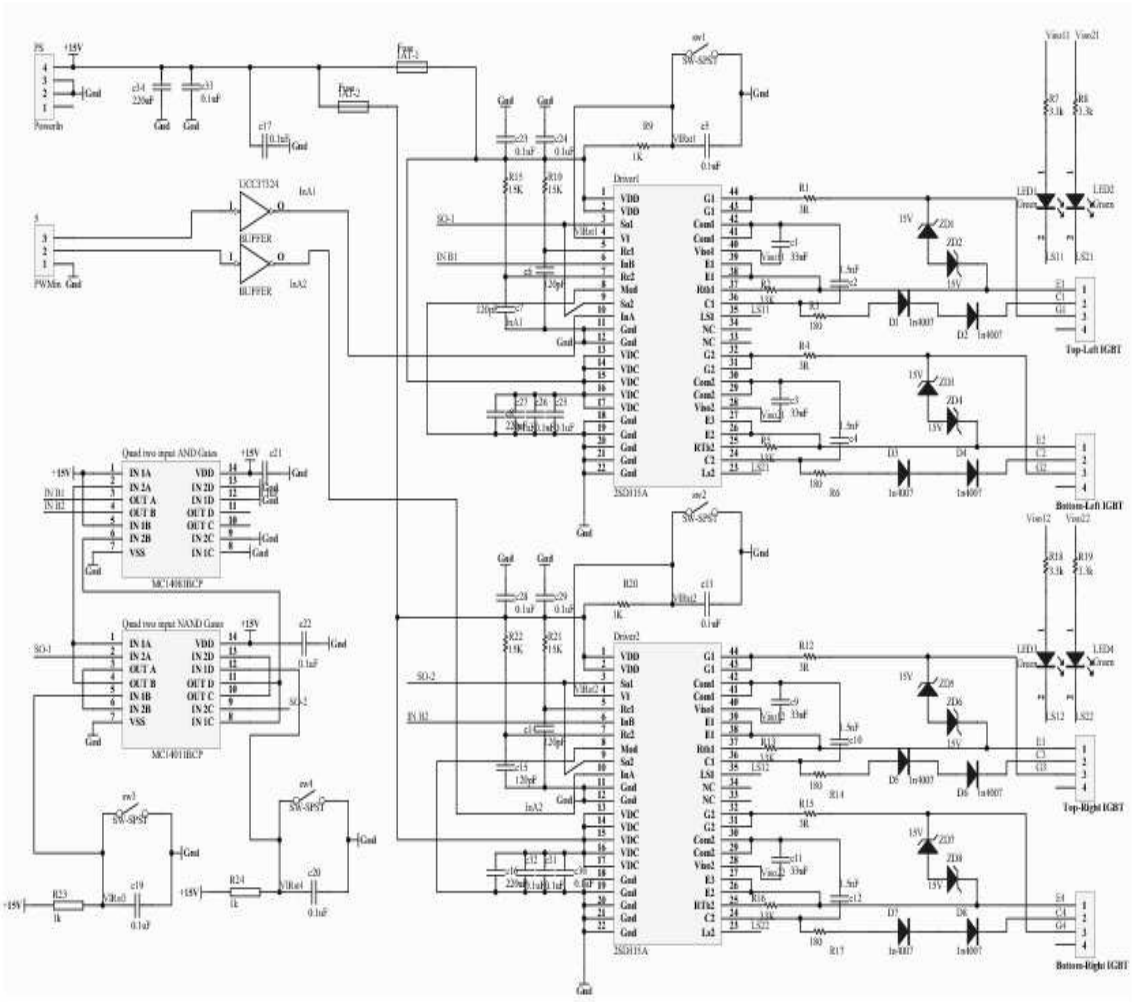

Figure D.1 Schematic of HV side IGBT driver circuit

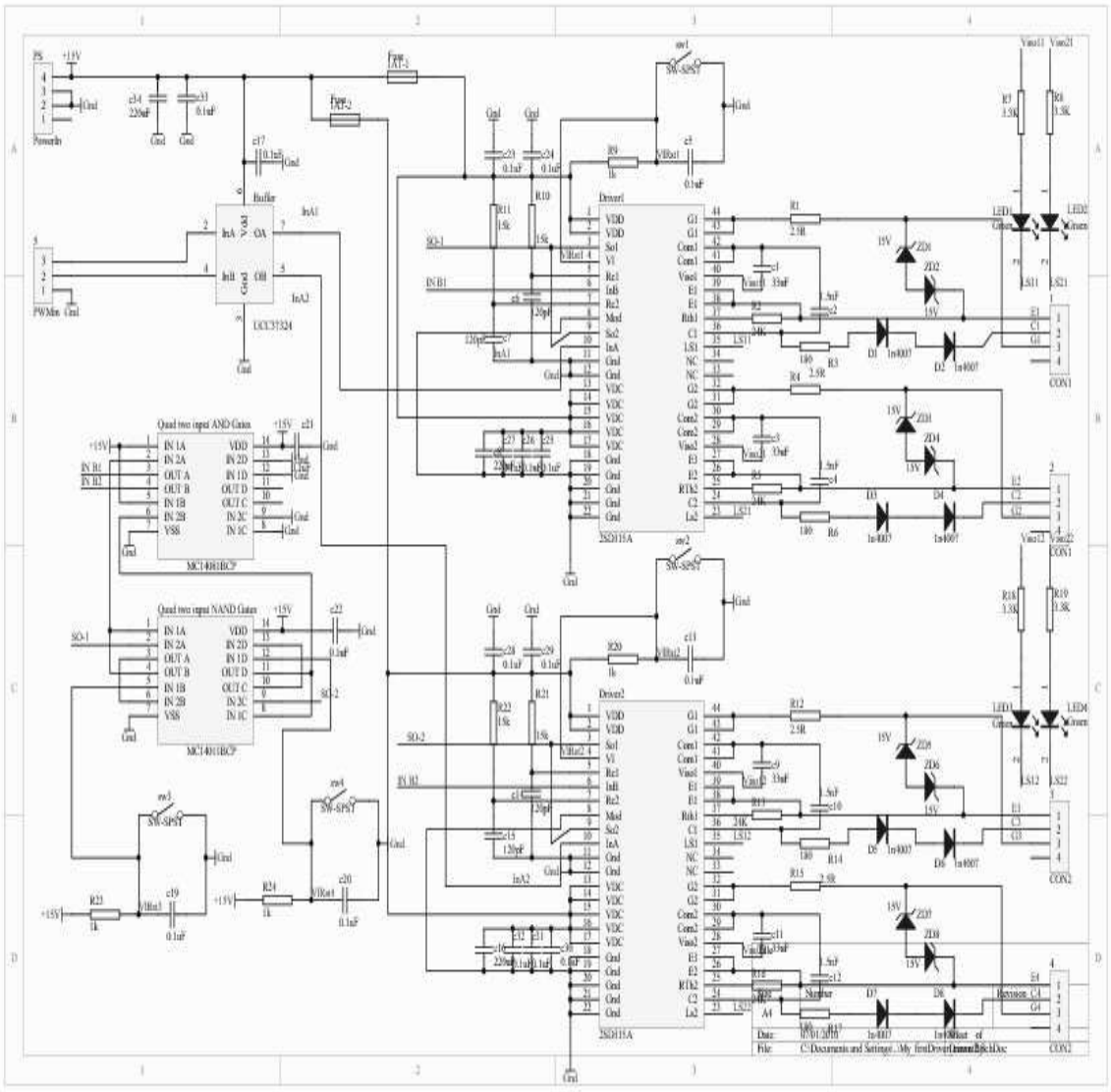

Figure D.2 Schematic of LV side IGBT driver circuit

D.2 PCB layers of driver circuits

Figures D.3 to D.6 show the top and bottom PCB layers of driver circuits on the HV and LV sides of the DAB DC-DC converter respectively.

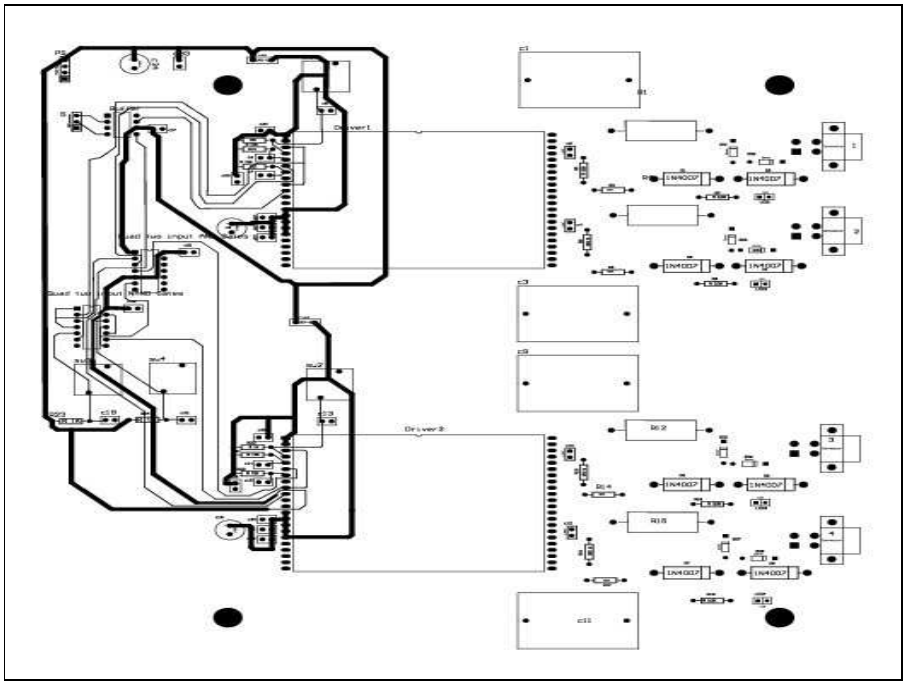

Figure D.3 Top layer of HV side driver circuit

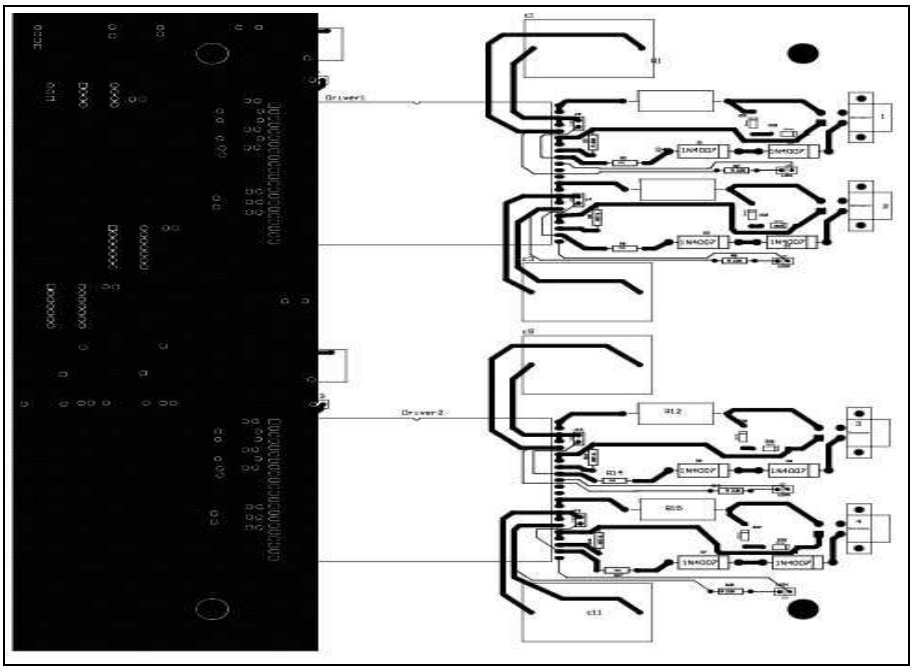

Figure D.4 Bottom layer of HV side driver circuit

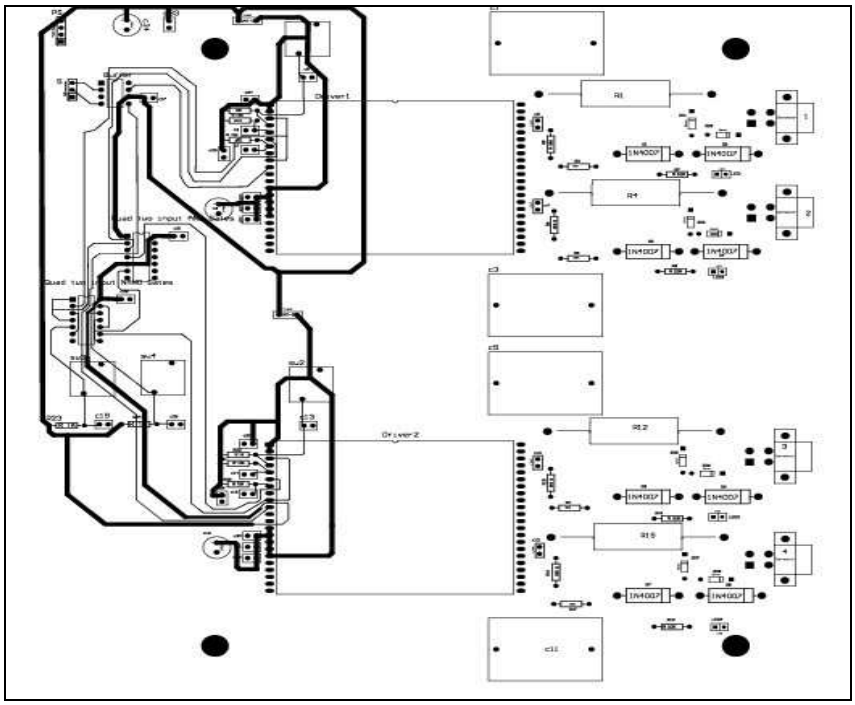

Figure D.5 Top layer of LV side driver circuit

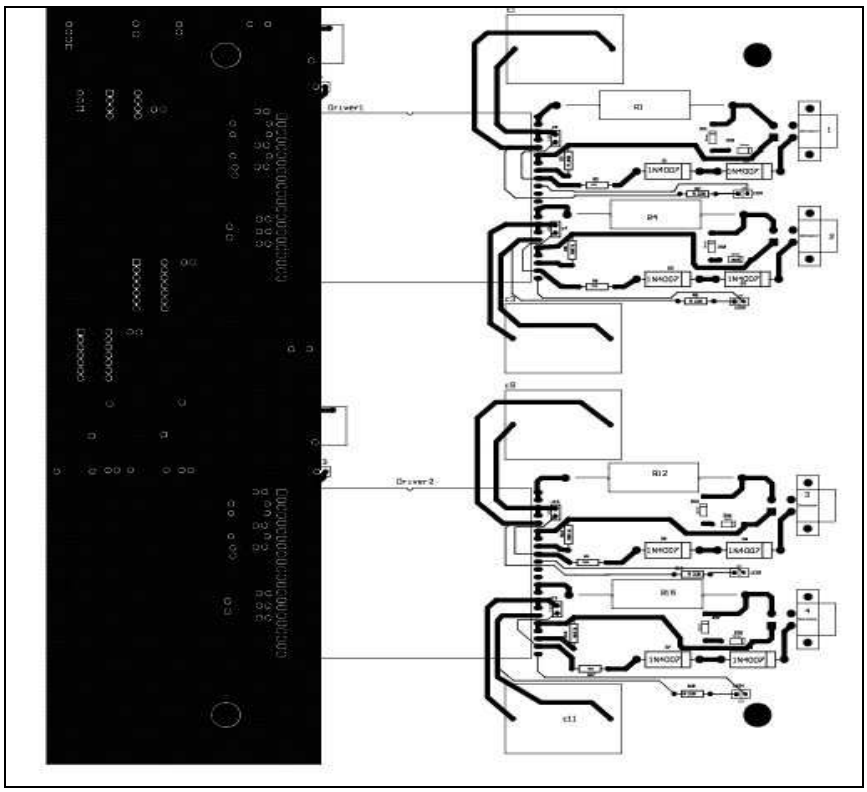

Figure D.6 Bottom layer of LV side driver circuit

D.3 Circuit diagram and PCB layers of interfacing circuit

Figure D.7 shows the schematic of signal conditioning circuit used for the DSP control of DAB DC-DC converter.

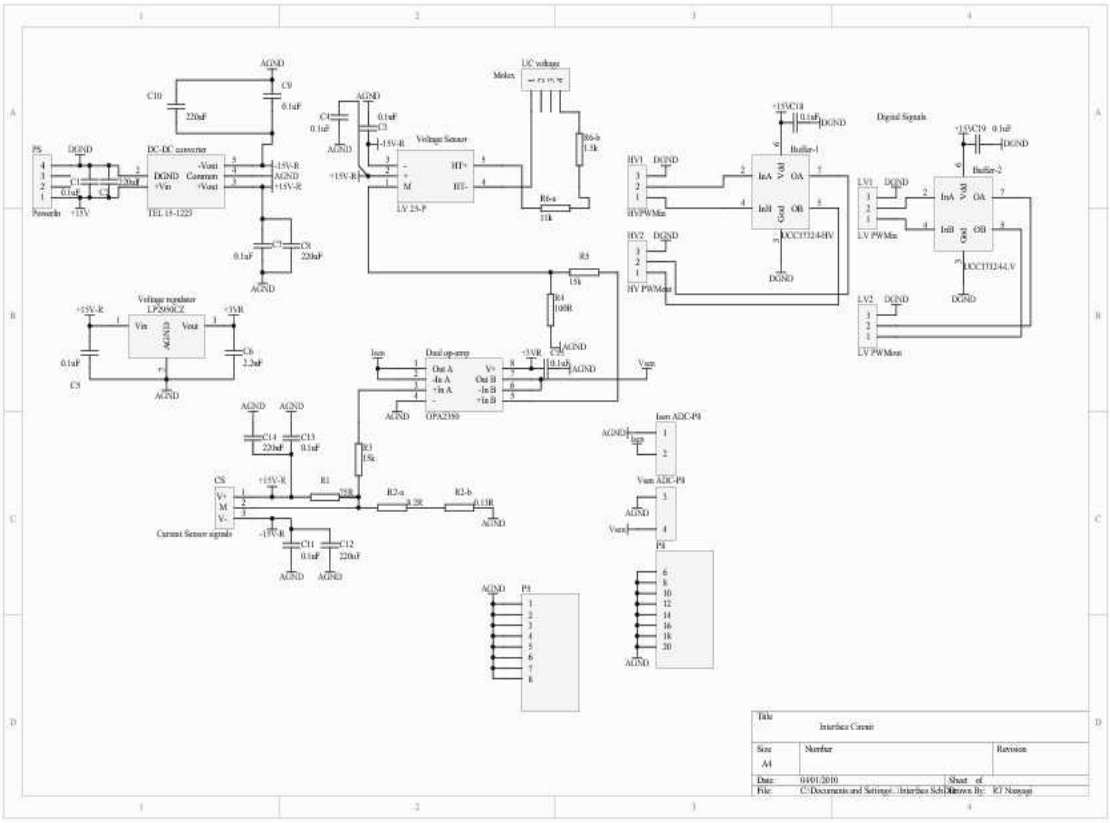

Figure D.7 Schematic of interfacing circuit

The following Figures D.8 and D.9 show the top and bottom PCB layers of the interfacing circuit.

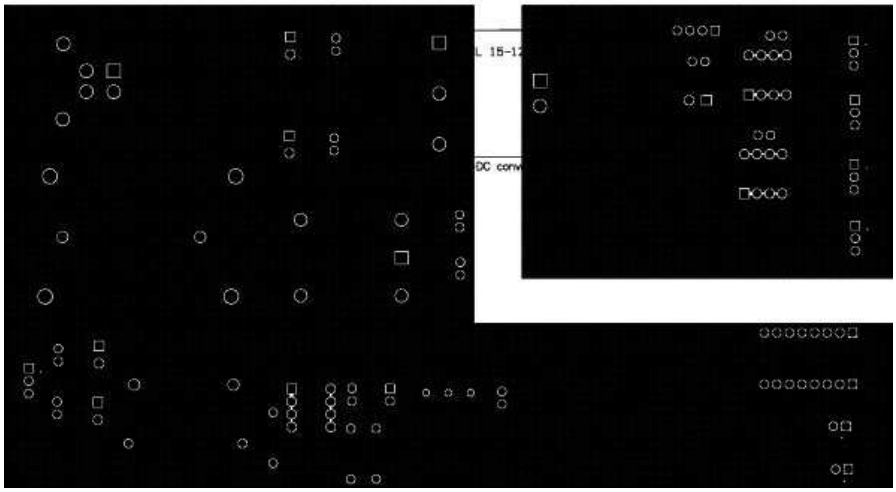

Figure D.8 Top layer of interfacing circuit

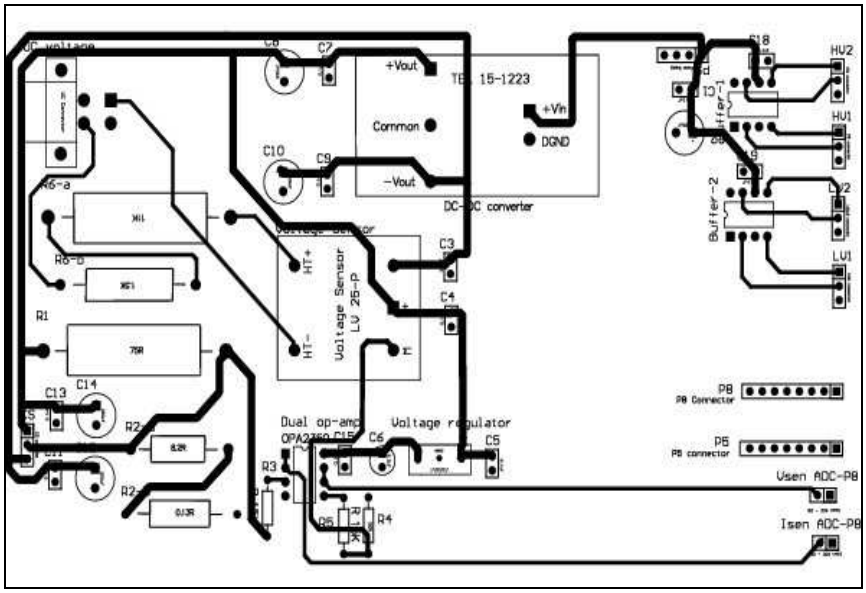

Figure D.9 Bottom layer of interfacing circuit

Appendix E

Pictures of DAB Converter Prototype and Circuit Components

Pictures of the converter prototype system with circuit components and laboratory equipments are presented below. Figure E.1 shows the photograph of the DAB converter prototype with Hilstone product load bank (left) and TopCon DC high Power Supply (right).

Figure E.1 Photograph of the DAB converter prototype with load bank and high power supply

Figure E.2 shows the photograph of the converter prototype verifying square wave mode of operation and Figure E.3 shows the picture of DSP control and signal conditioning circuits of the DAB converter.

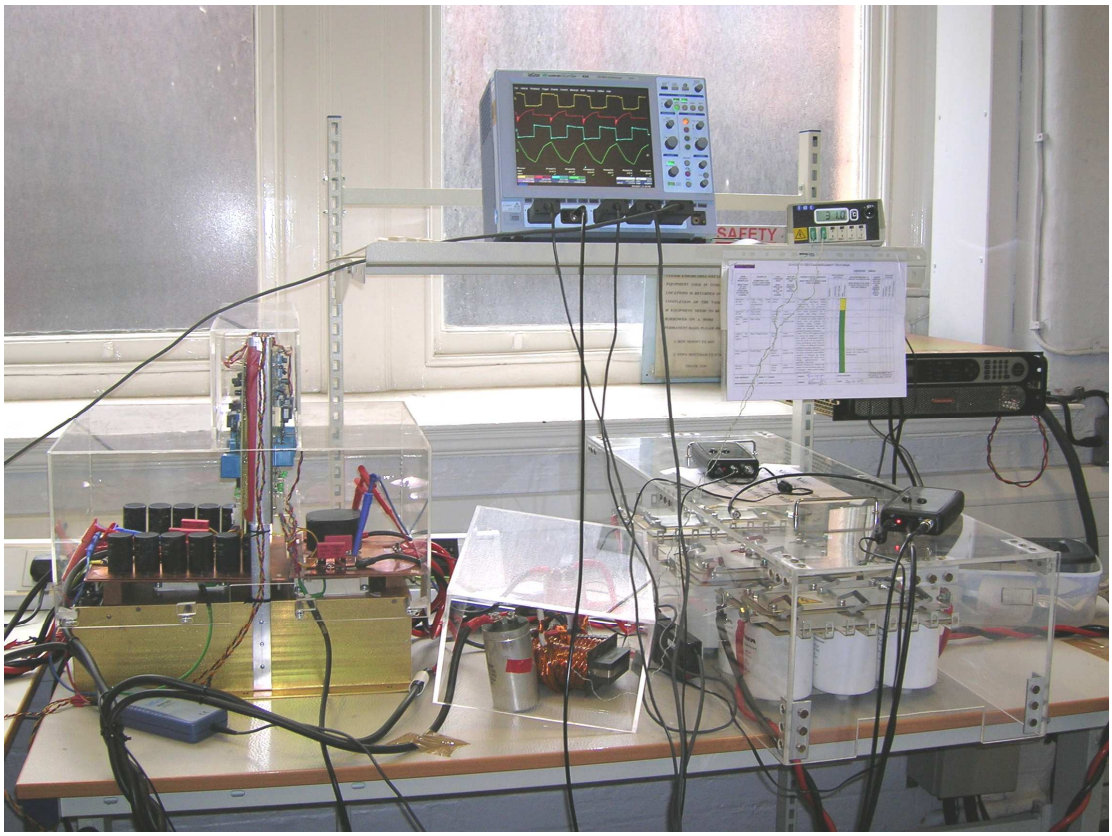

Figure E.2 Photograph of DAB converter verifying the square wave operation

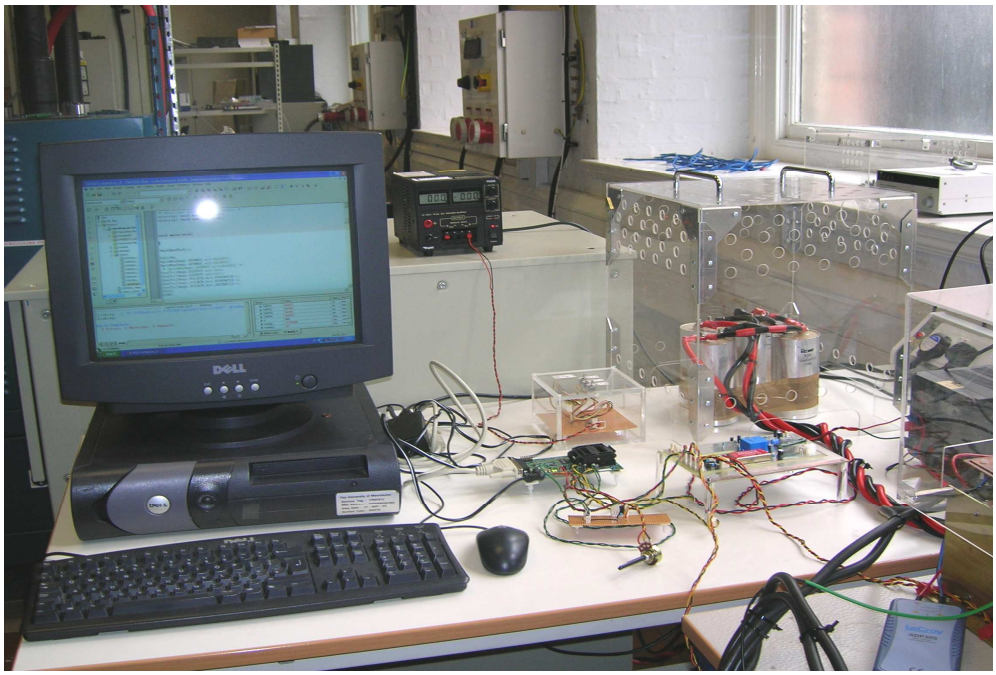

Figure E.3 Photograph of DSP control and signal conditioning circuits for the DAB converter

Figures E.4 and E.5 show the photograph of air core inductors used for DAB converter testing.

Figure E.4 Photograph of 61.2µH Air core inductor used in DAB converter

Figure E.5 Photograph of 4.17µH Air core inductor with copper busbars on its terminals used for high current testing on low voltage side of the DAB converter.