DIGITAL AVERAGE-CURRENT CONTROL FOR THE DUAL INTERLEAVED BOOST CONVERTER

A thesis submitted to The University of Manchester for the degree of

Doctor of Philosophy

in the Faculty of Engineering and Physical Sciences

2015

By

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Final word count: 59,517

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Symbol	Meaning
$\langle i_1(t)\rangle_{Tsw}, \langle i_2(t)\rangle_{Tsw}$	Local average of the current flowing through port 1/port 2 of the boost converter switch network over a switching period.
$\langle v_1(t)\rangle_{Tsw}, \langle v_2(t)\rangle_{Tsw}$	Local average of the voltage across port 1/port 2 of the boost converter switch network over a switching period.
$\mathbf{A}_{av}$	State-space matrix of the averaged small-signal model.
A_{AV}	Gain of the level-shifter for the ADC module.
$\mathbf{B}_{av}$	Input matrix of the averaged small-signal model.
$C(z)$	Compensator transfer function.
$\mathbf{C}_{av}$	Output matrix of the small-signal averaged model.
C_{in}	Converter input capacitance.
C_o	Converter output capacitance.
D	Quiescent duty-ratio of the converter assuming $D_a = D_b = D$.
$d(t)$	Instantaneous duty-ratio of a simple boost converter.
$\tilde{d}$	Small-signal component of a simple boost converter duty-ratio in the time-domain.
D'	Complement of the quiescent duty-ratio of the converter, $(1 - D)$.
D_a, D_b	Quiescent duty-ratio of phase-a/phase-b.
$\tilde{d}_a, \tilde{d}_b$	Small-signal component of the phase-a/phase-b transistor duty-ratio in the time-domain.
$\tilde{d}_a(s), \tilde{d}_b(s)$	Small-signal component of the phase-a/phase-b transistor duty-ratio in the Laplace-domain.
$\tilde{d}_a(z), \tilde{d}_b(z)$	Small-signal component of the phase-a/phase-b transistor duty-ratio in the z-domain.
$d_{a,n}$, $d_{b,n}$	Duty-ratio of phase-a/phase-b at interval n.
$d_a[n]$, $d_b[n]$, $d_x[n]$	Digital representation of phase-a/phase-b duty-ratio.
$\mathbf{D}_{av}$	Feed forward matrix of the small-signal averaged model.
D_{min}	Minimum duty-ratio constraint for immediate-update DPWM operation.
f	Converter switching frequency/sampling frequency.
$f^*(s)$	Laplace-transform of an impulse sampled function $f(t)$.
f_{clk}	Frequency of the master clock signal of the digital signal controller.
f_{clk_DPWM}	Frequency of the clock signal of the DPWM modules.
$G_{daia}(s)$	Phase-a control-to-phase-a current transfer function in the Laplace-domain.

$G_{daia}(z)$	Phase-a control-to-phase-a current transfer function in the z-domain.
$G_{daib}(s)$	Phase-a control-to-phase-b current transfer function in the Laplace-domain.
$G_{daib}(z)$	Phase-a control-to-phase-b current transfer function in the z-domain.
$G_{davo}(s)$	Phase-a control-to-output voltage transfer function in the Laplace-domain.
$G_{dbia}(s)$	Phase-b control-to-phase-a current transfer function in the Laplace-domain.
$G_{dbia}(z)$	Phase-b control-to-phase-a current transfer function in the z-domain.
$G_{dbib}(s)$	Phase-b control-to-phase-b current transfer function in the Laplace-domain.
$G_{dbib}(z)$	Phase-b control-to-phase-b current transfer function in the z-domain.
$G_{dbvo}(s)$	Phase-b control-to-output voltage transfer function in the Laplace-domain.
$G_{di}(z)$	Direct control-to-phase current transfer function in the z-domain.
$G_{di}H_a(z)$, $G_{di}H_b(z)$	Constituent transfer functions of the converter control loop in the z-domain. See Table 4.1.
$G_{dxi}(z)$	Cross-coupling control-to-phase current transfer function in the z-domain.
$G_{h0}(s)$	Zero-order hold transfer function in the Laplace domain.
$g_{h0}(t)$	Zero-order hold response to an impulse function in the time-domain.
$G_{iairef}(z)$, $G_{ibiref}(z)$	Closed-loop transfer functions of the converter in the z-domain.
$G_{izia}(s)$	Disturbance current-to-phase-a current transfer function.
$G_{izib}(s)$	Disturbance current-to-phase-b current transfer function.
$G_{izvo}(s)$	Disturbance current-to-output voltage transfer function.
$G_M(s)$	DPWM transfer function in the Laplace-domain.
$G_{dxi\theta}(z)$, $G_{dxi\phi}H_a(z)$	Constituent transfer functions of the converter control loop in the z-domain. See Table 4.1.
$G_{dxi\phi}(z)$, $G_{dxi\theta}H_b(z)$	Constituent transfer functions of the converter control loop in the z-domain. See Table 4.1.
$H_a(s)$, $H_b(s)$	Current-transducer transfer functions in the Laplace-domain.
$H_a(z)$, $H_b(z)$	Current-transducer transfer functions in the z-domain.
$\boldsymbol{I}$	Identity matrix.
$i_1(t)$, $i_2(t)$	Instantaneous current flowing through port 1/port 2 of the boost converter switch network.
I_1, I_2	DC component of the current flowing through port 1/port 2 of the boost converter switch network.
$\tilde{i}_1$, $\tilde{i}_2$	Small-signal component of the current flowing through port 1 of the boost converter switch network.
$i_a(t)$, $i_b(t)$, $i_x(t)$	Instantaneous phase-a/phase-b current.
$i_a^*(t)$, $i_b^*(t)$, $i_{ref}^*(t)$	Sampled phase-a, phase-b and reference currents.
I_a, I_b	Average value or dc component of the phase-a/phase-b current.

$\tilde{i}_a$, $\tilde{i}_b$	Small-signal component of the phase-a/phase-b current in the time-domain.
$\tilde{i}_a(s)$, $\tilde{i}_b(s)$	Small-signal component of the phase-a current in the Laplace-domain.
$\tilde{i}_a(z)$, $\tilde{i}_b(z)$	Small-signal component of the phase-a current in the z-domain.
$i_a[n]$, $i_b[n]$, $i_x[n]$	Digital representation of the Instantaneous phase-a/phase-b current.
i_{a0}	Intersection of the $i_{a1}(t)$ segment with the y-axis.
$i_{a1}(t)$, $i_{a2}(t)$,…, $i_{a5}(t)$	Line-segment functions comprising the phase-a current.
$\tilde{i}_c$	Small-signal component of the output capacitor current.
$i_{diff}(t)$	Instantaneous differential current, defined as half of the difference of the inter-phase transformer winding currents.
I_{Lin}	Average value or dc component of the input inductor current.
$i_{Lin}(t)$	Instantaneous input inductor current.
$i_o(t)$	Instantaneous converter overall output current. (Delivered to the load resistor).
I_o	dc component of the converter overall output current. (Delivered to the load resistor).
$\tilde{i}_o$	Small-signal component of the converter overall output current. (Delivered to the load resistor).
I_{oa}, I_{ob}	dc component of the output current flowing through the switch networks A and B of the converter.
$\tilde{i}_{oa}$, $\tilde{i}_{ob}$	Small-signal component of the output current flowing through the switch networks A and B of the converter.
I_{oab}	dc component of the converter output current. (Delivered to the output filter).
$\tilde{i}_{oab}$	Small-signal component of the converter output current. (Delivered to the output filter).
$i_{ref}(t)$	Instantaneous reference-current.
$\tilde{i}_{ref}(z)$	Small-signal component of the reference-current in the z-domain.
$\tilde{i}_{ref\theta}(z)$	Small-signal component of the delayed reference-current in the z-domain.
$i_{ref}[n]$	Digital representation of the instantaneous reference-current.
$\tilde{i}_z$	Small-signal component of the perturbation current in the time-domain.
$\tilde{i}_z(s)$	Small-signal component of the perturbation current in the Laplace-domain.
j	Imaginary unit. $j^2 = -1$.
k	Coupling coefficient.
K_i	Integral gain of a PI compensator.
K_n	Conversion ratio of the hall-effect current sensors.
K_p	Proportional gain of a PI compensator.
K_{PWM}	DPWM gain.

L_a	IPT winding a self-inductance.
L_b	IPT winding b self-inductance.
L_c	Self-inductance of the inter-phase transformer windings when $L_a = L_b = L_c$.
L_{diff}	Differential inductance of the inter-phase transformer windings.
L_{in}	Inductance of the Input inductor.
L_m	Mutual inductance of the inter-phase transformer windings.
L_{Tot}	Sum of inductances: $L_{Tot} = 2L_{in}\left(L_c + L_m\right) + \left(L_c^2 - L_m^2\right)$
$m_1, m_2, \ldots, m_5$	Slopes of the line-segments comprising the phase-a current.
N_{ADC}	Resolution of the ADC in bits.
P_o	Output power.
R_A, R_B, R_C, R_D	Values of the resistor network comprising the level-shifting stage for the ADC.
R_{in}	Input inductor parasitic resistance.
R_{load}	Converter load resistance.
R_m	Measurement resistor for current sensor.
R_{mod}	Mode selector resistor for the gate-drivers.
R_{wa}, R_{wb}	IPT Winding a/b resistance.
S	Generic sampler.
S_0	Slow-rate sampler.
S_a, S_b	Phase-a, phase-b samplers.
T	Converter switching period/sampling period.
$T(z)$	Open-loop transfer function.
t_{ADC}	Total conversion time of the ADC.
t_{ADC_INT}	Length of time of the ADC interrupt service routine.
t_d	Time that the ADC takes from the request of a conversion to the start of the sampling sequence.
$t_{d(on)}$	IGBT turn-on delay.
$t_{d(sch)}$	Time that takes for the results of the analogue-to-digital conversion to appear in the result-registers of the ADC module.
t_{d_proc}	Time that the digital controller takes from the start of an analogue-to-digital conversion to the calculation of a new duty ratio for the corresponding control-loop.
t_{dQ}	Time length from the moment where the DPWM channel is set high to the moment where its corresponding transistor fully conducts the phase-current.
t_{INT_SRVC}	Time that the processor takes from the moment where an interrupt is acknowledged to the start of the interrupt-service routine.
t_{p_gd}	Gate-driver propagation delay.
$t_{r(on)}$	IGBT current rise-time.
t_{SH}	Width of the sample-and-hold acquisition window of the ADC module.

T_{SH}	Sampling period of the ADC module sampling sequence.
$\tilde{\mathbf{u}}$	Input-vector of the averaged small-signal model in the time-domain.
$u_s(t)$	Unit-step function.
$v_1(t)$, $v_2(t)$	Instantaneous voltage measured at port 1/port 2 of the boost converter switch network.
V_1, V_2	dc component of the voltage measured at port 1/port 2 of the boost converter switch network.
$\tilde{v}_1$, $\tilde{v}_2$	Small-signal component of the voltage measured at port 1 of the boost converter switch network.
V_{ADCmax}	Maximum analog input voltage of the ADC.
v_{cmax}	Maximum count of the DPWM module digital counters.
$V_{diff(pkpk)}$	Differential peak-to-peak voltage.
$v_{diff}(t)$	Instantaneous differential voltage.
$V_{ge1a}(t)$, $V_{ge1b}(t)$, $V_{ge2a}(t)$, $V_{ge2b}(t)$	Instantaneous IGBT gate-to-emitter voltages.
$v_{ia}(t)$, $v_{ib}(t)$, $v_{ix}(t)$	Conditioned voltage signals representing the phase-currents.
$v_{ia}[n]$, $v_{ib}[n]$, $v_{ix}[n]$	Digital representation of the conditioned voltage signals representing the phase-currents.
$v_{in}(t)$	Instantaneous input voltage of the converter.
V_{in}	Average value or dc component of the converter input voltage.
$\tilde{v}_{in}$	Small-signal component of the converter input-voltage.
$V_{Lin(pkpk)}$	Input inductor peak-to-peak voltage.
$v_{Lin}(t)$	Instantaneous voltage across the input inductor.
$v_o(t)$	Instantaneous output voltage of the converter.
V_o	Average value or dc component of the converter output voltage.
$\tilde{v}_o$	Small-signal component of the converter output voltage in the time-domain.
$\tilde{v}_o(s)$	Small-signal component of the converter output voltage in the Laplace-domain.
$y^*(t)_n$	Original output signal of a decomposed sampler.
$y^*_0(t)$, $y^*_1(t)$,…, $y^*_p(t)$	Partial output signals of a decomposed sampler.
$\tilde{\mathbf{x}}$	State-vector of the averaged small-signal model in the time-domain.
ΔI_{diff}	Amplitude of the differential current ripple.
ΔI_{Lin}	Amplitude of the input inductor current ripple.
ΔI_{lrg}	Peak-to-peak value of the largest ripple in the phase-a/phase-b current.
ΔI_{smll}	Peak-to-peak value of the smallest ripple in the phase-a/phase-b current.
$\Delta PWM(s)$	DPWM delay transfer function.
ω	Angular frequency.

List of Abbreviations

Abbreviation	Meaning
A/D	Analogue-to-Digital
ac	Alternating current
ADC	Analogue-to-Digital Converter
ADC_ISR	Analogue-to-Digital Converter Interrupt Service Routine
CCM	Continuous Current Mode
CPU	Central Processing Unit
D/A	Digital-to-Analogue
DAC	Digital-to-Analogue Converter
dc	Direct Current
DCM	Discontinuous Current Mode
DIBC	Dual-Interleaved Boost Converter
DPWM	Digital Pulse Width Modulator
DSC	Digital Signal Controller
EOC	End-Of-Conversion
EV	Electric Vehicle
FPGA	Field Programmable Gate Array
HEV	Hybrid Electric Vehicle
IGBT	Insulated Gate Bipolar Transistor
IPT	Inter-Phase Transformer
LCO	Limit Cycling Oscillation
MOSFET	Metal-Oxide Semiconductor Field-Effect Transistor
MSPS	Mega-Samples Per-Second
PI	Proportional Integral
PWM	Pulse Width Modulator
SOC	Start-Of-Conversion
TDSA	Time-Domain System Analyser
WWF	World Wildlife Fund
ZOH	Zero Order Hold
ZVS	Zero-Voltage Switching

Abstract

This Thesis addressed the challenge of ensuring balanced currents in the phases of a multi-kW, interleaved dc-dc converter by means of closed-loop digital control.

The Thesis examines uniformly-sampled, valley-current, peak-current and average-current control for a dual interleaved boost converter with inter-phase transformer which might form part of the power train of an electric vehicle. Also, an enhancement of the average-current control is investigated in which the transistor duty-ratio is updated more rapidly, which allows an improvement of approximately ten times in the response speed of the system. Based on the theoretical analysis, the average-current control methodology was determined to be the most suitable technique for this type of converter as it ensures well-balanced phase currents over a wide range.

To provide a basis for control system analysis and design for interleaved converters, a modelling methodology is developed based on a combination of multi-rate data-sampled theory and a small-signal averaged converter model. The model is shown to represent accurately the interaction between the interleaved phases, revealing a reduced stability range compared with a non-interleaved converter.

The modelling and control methods are validated using switched and average value simulations obtained with the SABER software and by experimental results from a 25 kW, 30 kHz converter prototype. The control techniques were implemented on a Texas Instruments TMS320F28335 digital signal controller.

Declaration

No portion of the work referred to in this Thesis has been submitted in support of an application for another degree or qualification of this or any other university or other institute of learning.

Copyright statement

Dedicated to my parents, Vicente and Laura Velia, and my dearest sister, Laura, who have supported, inspired and encouraged me throughout my life.

"Caelum, non animum, mutant qui trans mare currunt" - Horace

Acknowledgements

First, my sincere gratitude to my supervisor, Professor Andrew J. Forsyth, for his guidance, support and insightful advice given throughout the development of this research project. Also, I would like to thank him for the time he dedicated to provide invaluable suggestions during the writing stage of this Thesis.

I am also grateful to the National Council of Science and Technology of Mexico (CONACyT), the National Polytechnic Institute of Mexico (IPN), and the Public Ministry of Education of Mexico (SEP), for their financial support to pursue my PhD degree.

I thank my parents and sister, Vicente, Laura Velia and Laura for all their love, help and support that carried me through difficult times.

Special thanks to Dr Gerardo Calderon-Lopez for his experience, useful discussions and friendship. Also I would like to thank my friends Jesus Carmona and Dr Damian Vilchis for the moments together.

I am very grateful with my friends Gillian Menichino, Carlos A. Duran, Jana Kefurtova and Alexander Cassell for their invaluable support and the great moments we lived together.

Last, I would like to thank Dr Ismael Araujo-Vargas for the encouragement to pursue a PhD degree.

Chapter 1
Introduction and literature review

1.1. Introduction

With terrestrial transport accounting for around one quarter of the UK's total CO_2 emissions [1], the transition to low carbon vehicle technologies is critical to meeting the targets set by the UK Climate Change Act. The Act commits the UK to reduce in 2050 greenhouse gas emissions by at least *80 %* compared with 1990 levels [2], and to meet this objective, the CO_2 emissions have to be reduced in 2020 by at least *34 %* relative to those generated in 1990 according to a report presented to the World Wildlife Fund UK in 2010 (WWF UK) [3].

1.1.1. Electric vehicles

Due to the growing concerns for the reduction of CO_2 emissions and for the depletion of fossil fuels [4], significant progress has been made during the past two decades in the development of electric vehicles, EVs. However, further improvements in range and reductions in cost are needed to make the technology more attractive and competitive in the market [5].

The range of an EV is limited by the capacity of the on-board power source and the efficiency of the systems that form the electrical power-train [6, 7]. The use of high-capacity batteries and/or fuel-cell storage systems has been a common solution proposed, often accompanied by a bank of super-capacitors or a flywheel in order to meet the high-power surges demanded by the traction drive and to absorb the energy from braking. An alternative approach which has had better success in the market in recent years, is the

combination of an internal combustion engine with an electric propulsion system. Such vehicles are known as Hybrid Electric Vehicles, HEVs [5, 8].

A large number of electrical power-train architectures exist depending on the combinations of energy sources employed in the vehicle. A study carried out in 2006 [9] identifies at least 30 different architectures. For illustrative purposes Figure 1.1 depicts an overview of the power-train on an electric vehicle which can be powered by fuel-cells, batteries or both [10]. The voltage provided by the battery/fuel-cell and super-capacitors has to be stepped up and regulated by one or more bidirectional/unidirectional dc-dc converters. The regulated voltage is delivered into a high-voltage dc-bus. A dc-ac converter is supplied from the dc-bus to drive the traction motor of the EV.

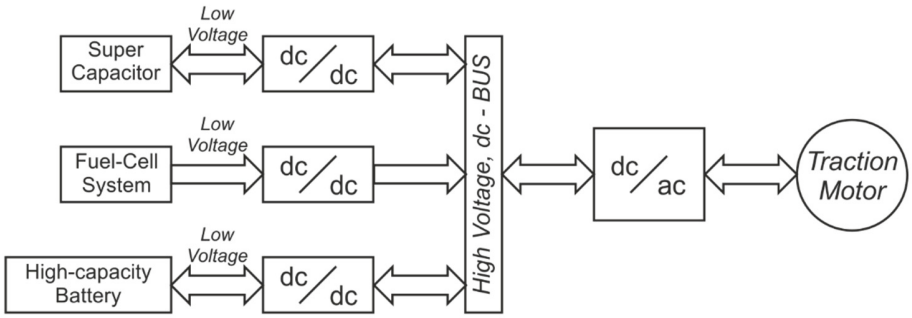

Figure 1.1. Illustrative configuration of the electrical power-train on board of an electric vehicle [10].

Besides high-power capacity and bidirectional power flow capabilities, the dc-dc converters employed in the electrical power-train must be light-weight, highly-efficient, small-sized, highly-reliable, have low electromagnetic interference and have low current-ripple [10, 11]. To meet these demands switching frequencies are being increased, often through the adoption of new device technologies such as silicon carbide [12-14], and different circuit topologies are under investigation. These topologies can be hard-switched, soft-switched, multi-phase/interleaved, multi-port, isolated, or non-isolated depending on the requirements of the application [15].

The research presented in this thesis is based on a hard-switched, non-isolated topology named dual-interleaved boost converter with inter-phase transformer shown in Figure 1.2. This converter topology has been proposed by several researchers to interface the different voltage levels of fuel cells, super capacitors, battery banks and traction drives

within an electrical vehicle power train, mainly due to its high power-density capabilities [16-19], and was used in this work as a great deal of research work has been invested in this converter topology within the Power Conversion research group of the University of Manchester and several prototypes were readily available for their use.

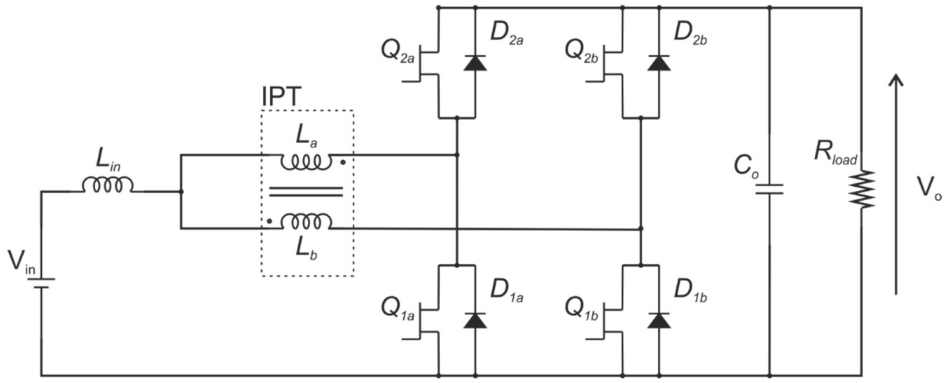

Figure 1.2. Dual interleaved boost converter with inter-phase transformer.

Furthermore, to achieve the necessary voltage regulation and manage the bidirectional power flow of these increasingly complex, high frequency converters, high performance controllers are required. Due to the relatively high operating frequency typically above *20 kHz*, dc-dc converters tend to be controlled by relatively simple analogue based methods. Whilst these methods offer high-bandwidth, real-time operation capabilities and theoretically infinite voltage resolution, they suffer from a number of limitations: they are sensitive to noise and temperature variations which are common in automotive applications, they usually comprise passive devices that are subject to ageing and have to be replaced/exchanged in order to perform modifications, such as parameter changes, and they require a prohibitive number of components when complex control algorithms have to be implemented thereby increasing cost and size. Furthermore, these characteristics can lead to poor reliability. However, the evolution of microprocessors and microcontrollers into faster and more versatile digital signal controllers and the advent of Field Programmable Gate Arrays, FPGAs, has created the possibility of dc-dc converter control through digital means.

Digital control provides a way to overcome many of the limitations of analogue control through the use of software that is more reliable and that provides the flexibility to

change parameters in real-time. It also facilitates the implementation of complex and advanced control algorithms without the need of extra components. Other advantages are insensitivity to component ageing, robustness to noise, the possibility to run self-diagnosis and tests, and the ability to interface directly with other digital systems embedded in the vehicle, thereby leading to a full digital implementation of the control system of an EV. However, the limited resolution of analog-to-digital converters and digital pulse-width modulation modules together with the processing delay caused by the digital signal controller, can have detrimental effects on the control bandwidth and the overall system performance [20]. For these reasons, there has been an increased interest in digital control in power converter applications generally and several studies have proposed new techniques and architectures to overcome these performance issues.

1.1.2. Objectives

The overall objective of the research reported in this thesis is to devise and demonstrate digital control techniques for dual-interleaved dc-dc converters that might form part of an EV power train, and to develop and validate a theoretical basis for the analysis and design of such systems. The key challenges include ensuring balanced currents in the two interleaved phases by means of cycle-by-cycle current control and representing accurately the interleaved current sharing in the system model.

1.1.3. Structure of the literature review

The literature survey is organized in five sections. In Section 1.2, a review of the most common control methodologies for simple dc-dc converters is presented as most of the research on digital control has been carried out for basic topologies and low-power applications. In Section 1.3, a review of digital control methods for multi-phase dc-dc converter topologies is undertaken since the converter studied in this thesis is a variation of a multi-phase dc-dc converter. Section 1.4 introduces the modelling techniques for digitally controlled dc-dc converters. In Section 1.5, the linear compensator design methodologies are reviewed. Finally, in Section 1.6, a survey of the most relevant modelling techniques for multi-phase dc-dc converters is presented focused on the dual-interleaved converter.

1.2. Control for switched dc-dc converters

The main objective of dc-dc converter control is usually the regulation of the output-voltage and this is typically achieved through a closed-loop control system that feeds back the output-voltage, and sometimes other circuit variables as well, to adjust the on-time-to-period ratio or duty-ratio of the transistors. Two figures-of-merit that are often used to quantify the performance of dc-dc converter controllers are based on the systems ability to regulate the output-voltage in the presence of variations in the input voltage and/or load current: the line-regulation and the load-regulation. The former is defined as the change in the output voltage corresponding to a specific change in the input voltage, whilst the latter is defined as the change in the output voltage to a specific change in the load current [21, 22]. The controller implementation may be either analogue or digital.

1.2.1. Analog control techniques

Analogue control techniques for dc-dc converters are well-established and mature. Although numerous control approaches have been published in the literature, two main control strategies can be identified: voltage-mode control and current-programmed control [21-24].

1.2.1.1. Voltage-mode control

Voltage-mode control in its most simple form incorporates a single control-loop to regulate the output voltage of the converter. Figure 1.3 illustrates a schematic diagram where the voltage-mode control is implemented for a boost or step-up converter. The output-voltage of the converter, v_o, is fed back and compared against a target constant voltage-reference, v_{ref}. The error between the signals, v_{err}, is passed through an analog compensation network, *H(s),* which in its simplest form can be lead, lag or a lead-lag compensator. The compensator network generates a control signal, v_m, forming the input to the PWM modulator, which in its simplest form consists of a saw tooth waveform generator and a comparator. The compensation network usually comprises one or more operational amplifiers plus passive components. Whilst being simple and easy to implement, this architecture is not particularly effective at compensating for rapid load- and

line-variations as these will take some time to be reflected in the output-voltage, resulting in a slow response, large voltage deviations and/or the requirement for a large output filter capacitor [21].

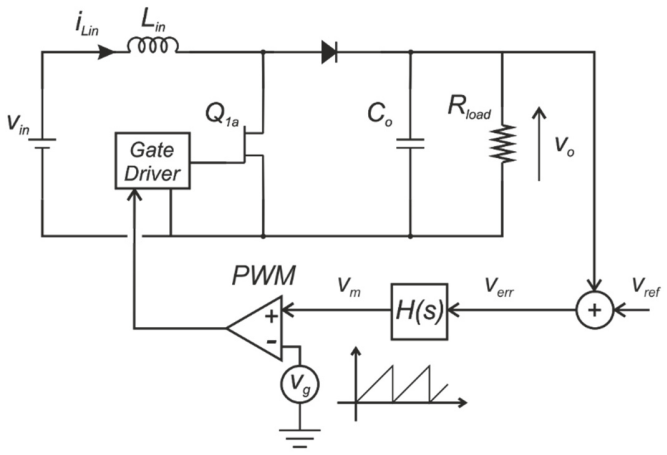

Figure 1.3. Boost converter with analog voltage-mode control.

A variant of this architecture is sometimes used to improve immunity to line-variations [24]. In this variant, the input-voltage is employed as a feed-forward signal to adjust the slope of the modulator ramp. In consequence, any change in the input voltage is compensated for almost immediately, improving the overall dynamic response of the system.

1.2.1.2. Current-mode control

Many types of current-mode control are described in the literature which may be divided in two categories: fixed-frequency and variable-frequency, fixed frequency being the most common. Figure 1.4(a) illustrates the architecture of the peak-current mode control for a boost converter which is a form of fixed-frequency control. There are two control loops an outer voltage-loop and an inner current-loop. The inner control loop regulates the peak current or maximum current circulating through the input inductor, whilst the outer control loop provides a reference current for the inner control loop.

In contrast to voltage-mode control, the duty-ratio of the converter transistor is generated by comparing the sensed inductor current against a threshold value. This is commonly accomplished by employing an analog comparator. When the inductor current

reaches the threshold, the comparator resets the state of an SR-latch, which consequently turns the transistor off. A fixed-frequency clock-pulse is fed into the set terminal of the SR-latch which turns the transistor on at the start of each cycle. The constant activation/deactivation of the SR-latch produces a fixed-frequency driving signal. The outer-loop operates in a similar way to voltage-mode control. The sensed output voltage is fed-back and compared with a target reference. The error signal generated is then passed through a compensation network which will produce the reference current signal.

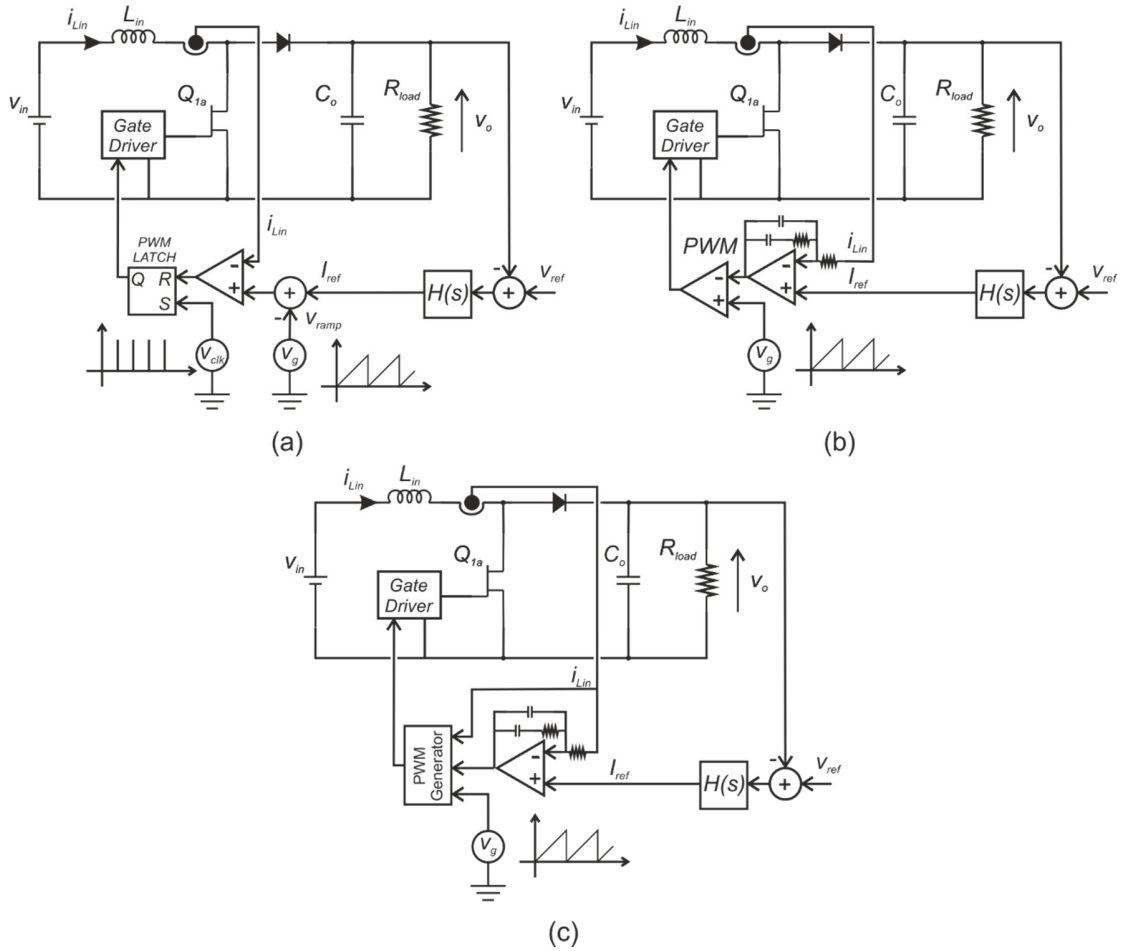

Figure 1.4. Boost converter with analog current-mode control. (a) Peak-current mode control. (b) Average-current mode control. (c) I^2 averaged-current mode control [30].

Employing this technique can be problematic in that instability is caused by the propagation of sub-harmonic oscillations when the converter operates at duty-ratios above 0.5. To address this issue, a compensating ramp is added to the reference current before it is compared against the inductor current. The slope of the compensating ramp is selected to ensure stability of the system over a determined range of operation [25].

The advantages of the current-mode control can be summarized as: immediate response to input voltage variations effectively providing input-voltage feed-forward, reduction of the order of the system transfer functions since the operation of the input inductor is similar to that of a voltage-controlled current source, inherent over-current protection, and inherent load-sharing when several converters are employed in parallel. The main disadvantage of this type of control is its susceptibility to switching noise generated by the transistor switching transients which might generate current over-shoots larger than peak-current and that can result in erratic operation and instability [21, 23, 24].

A number of variations on this control method have been proposed, for example using fixed on-time or fixed off-time in the current control loop as a free-running hysteresis technique [21]. Also an integrator is sometimes included in the current control loop to force the average inductor current to follow the current reference signal. This technique is known as average-current mode control [26], Figure 1.4(b), and is often employed in applications where the converter input current must be shaped or accurately controlled, for example in power factor correction circuits [27].

More recently (2014), a new control method termed I^2 average-current mode control has been proposed in [28] to improve the transient response of average current mode control and also improve light-load efficiency through using fixed on-time, variable switching frequency. Figure 1.4(c) shows a diagram of a boost converter with this control where an outer voltage loop is employed for voltage regulation. This technique combines both the fast-direct feedback of the peak-current mode control to ensure fast transient response with the slow integral feedback of the average-current mode control to achieve an accurate control of the inductor current. Moreover, by the use of fixed on-time modulation in conjunction with this technique, the propagation of sub-harmonic oscillations is avoided thereby eliminating the requirement for a compensating ramp.

1.2.2. Digital control techniques

A direct approach to form a digital controller for a dc-dc converter would be to reproduce digitally the well-known analog control techniques. However, such implementation yields an expensive solution as highly-specialized components would be

required to achieve the necessary sampling and processing speeds. For this reason, research effort has been devoted to finding cost-effective control solutions employing market available Digital Signal Controllers, DSC. The following section will review the architectures employed to control a dc-dc converter employing a DSC. Moreover, the operation and limitations of the techniques are considered.

1.2.2.1. Architecture and elements of a digital controlled dc-dc converter

Figure 1.5 illustrates the key-components that form a digital controlled dc-dc converter. As seen in this diagram, the power stage is interfaced with the DSC by scaling and conditioning stages in the feedback path and the gate-driver for the power-stage transistor(s). The DSC has three main elements: the Analog-to-Digital Converter, ADC, the Central Processing Unit, CPU, and the Digital Pulse-Width Modulator. Most of the DSCs available in the market have at least one ADC module and several DPWM modules [29, 30].

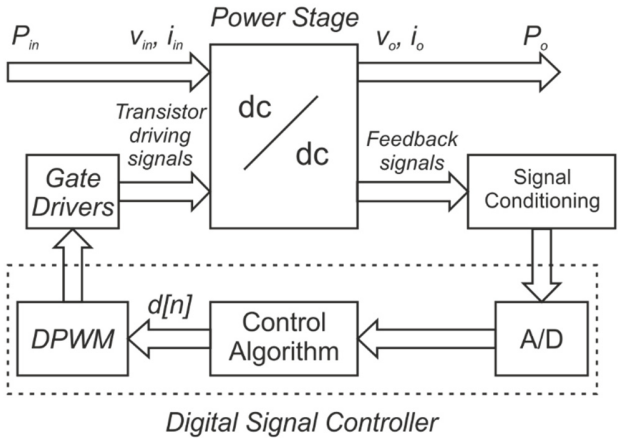

Figure 1.5. Architecture of a digitally controlled dc-dc converter.

The ADC converts the feedback signals into a digital representation. The typical sampling speeds of the ADC modules embedded in microcontrollers for motor-control and power converter applications are in the range of *4 MSPS* to *12.5 MSPS* [29, 30]. These figures correspond to conversion times of *250 ns* to *80 ns* respectively. The conversion speed of the ADC contributes to the processing delay of the controller and increases with the number of signals converted.

Following the analog-to-digital conversion process, the CPU executes the control calculation and determines the duty-ratio of the converter. The controller can be programmed to execute many different algorithms to ensure that the control target is met. However, the processing speed of the CPU is limited and it increases with the complexity of the algorithms implemented. Typical clock-frequencies of available DSCs range from *40 MHz* to *300 MHz [29, 30].* The duty-ratio determined by the control algorithm, is converted into a transistor driving signal by means of the DPWM. The most common implementation of DPWM found in the DSCs available in the market is uniformly-sampled PWM, UPWM.

Figure 1.6(a) illustrates the functional block diagram of a uniformly-sampled PWM, whilst Figure 1.6(b), 1.6(c) and 1.6(d) show the key waveforms for different modes of operation. This implementation is directly derived from a naturally-sampled PWM architecture by substituting its main elements for digital components [22]. The operation is explained for the case where the binary-counter is programmed in count up mode and with the aid of the plots in Figure 1.6(b).

Under count up mode, the binary counter generates a digital leading-edge ramp waveform, v_c. The binary counter is incremented at the rising-edge of the DPWM clock-signal. The *DPWM clock* is commonly sourced from the master-clock signal of the digital signal controller which may be divided down by means of a prescaler circuit to achieve slower switching frequencies. v_c is constantly compared against a reference-register which contains the value of the programmed duty-ratio, v_m, sometimes called the modulating signal. This is accomplished by means of a binary comparator. When the value of v_c crosses v_m, an interrupt-request is triggered by the digital comparator. The interrupt-request is used for two purposes: to set the DPWM output-signal, v_{out}, to zero and to inform the processor of this event. When v_c reaches its maximum value, v_{c_max}, it is reset to zero and v_{out} is set high. At the same time, the reference-register containing v_m is updated with the new programmed duty-ratio. Since v_m is updated only once per switching period, it is plotted as a constant value during the whole v_c cycle. In contrast, in an analogue naturally-sampled PWM generator, the duty-ratio signal or modulating signal varies continuously, and as a result the digital, uniformly sampled, PWM exhibits an additional delay, which, for high duty-ratio pulses can approach a switching cycle for leading-edge and trailing-edge

modulation and half switching cycle for the triangular carrier modulation. This effect can limit the achievable control bandwidth when using digital control [31-33].

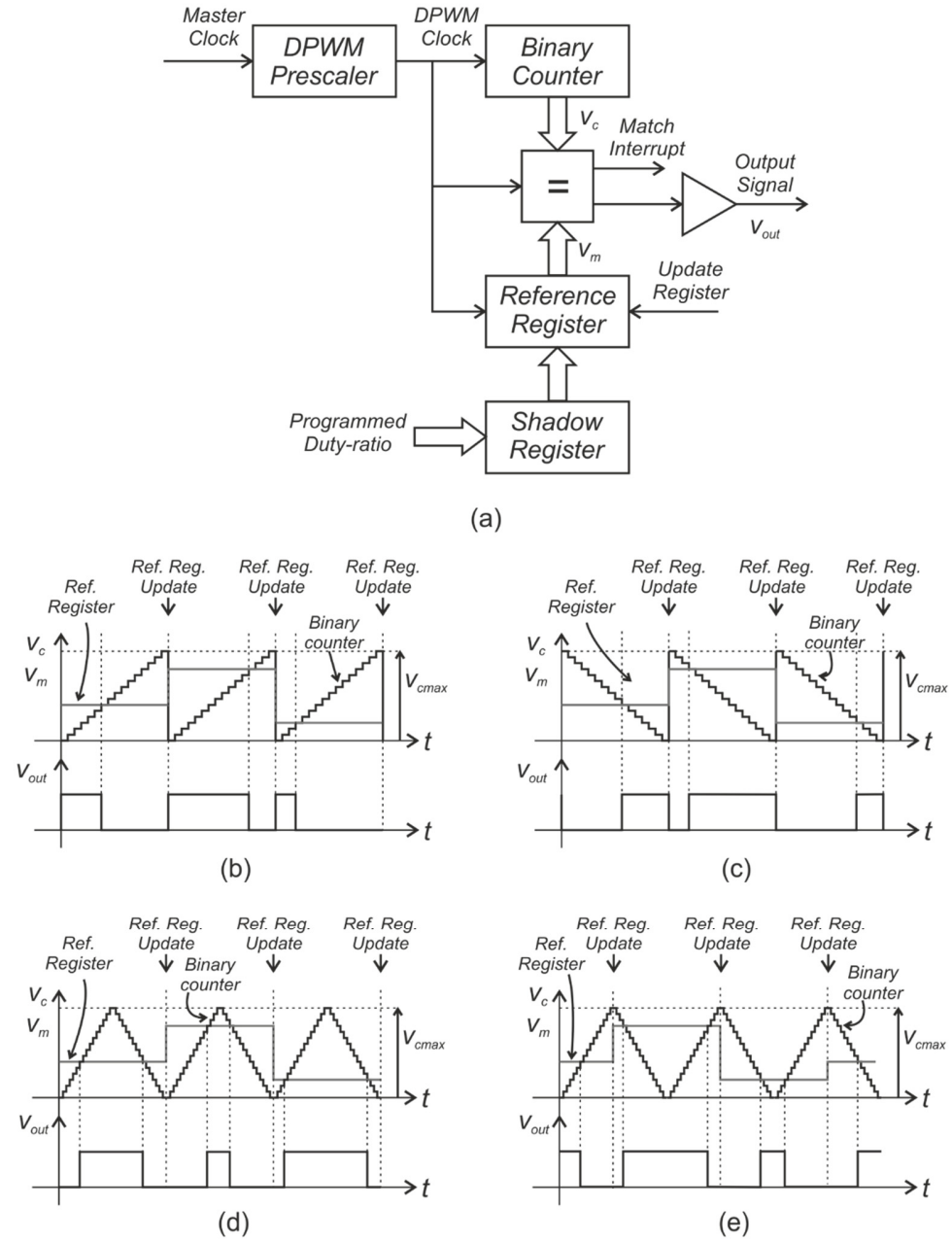

Figure 1.6. Digital pulse-width modulator: Uniformly-sampled implementation [22]. (a) Functional block diagram; (b) Count up mode operation; (c) Count down mode operation; (d) Count up-down mode operation; Count down-up mode (e).

In addition to the count up mode of operation, it is also possible to program the binary-counter in two alternative modes: count down mode and count up-down mode. In the former, the operation is similar to that of the count up mode, Figure 1.6(c). In the latter,

the only difference is that the update of the reference-register can be carried out when the counter reaches either its maximum or its minimum value, Figure 1.6(d).

1.2.2.2. Synchronization of the ADC and the DPWM for current-control

To avoid continuous sampling of the inductor current, a strategy adopted in digital current-controlled converters is to synchronize the operation of the ADC and the DPWM. Three forms of synchronization are possible allowing immediate access to the valley-current, peak-current or the average-current of the inductor. To sample the inductor valley-current, the DPWM is operated in count up mode and the ADC sampling is triggered when the DPWM counter is reset to zero, the inductor current is therefore sampled at the transistor turn on instant. Similarly, to acquire the inductor peak-current, the DPWM is operated in count down mode and the sampling occurs when the DPWM counter is reset, the inductor current is then sampled at the transistor turn off instant. Finally, to acquire the average-current, the DPWM counter is operated in count up-down mode and the sampling instants occur when the counter reaches its maximum value. This will result in the average value of the inductor current being obtained since the current is sampled in the middle of the transistor on-interval [31, 34, 35].

1.2.3. Review of digital control techniques for dc-dc converters

This section of the literature survey aims to review and classify the digital control methods found in the literature for the basic dc-dc converter topologies: buck, boost and buck-boost converters. In the following classification, the digital control strategies are grouped according to the methodology employed to regulate the inductor current, the output voltage or both. Five methodologies were identified: linear compensation methods or conventional methods, predictive/estimative methods, multi-sampling methods, mixed-signal methods and non-linear methods. This classification does not distinguish whether the implementation is carried out in a DSC or a FPGA.

1.2.3.1. Linear compensation or conventional compensation methods

These methods usually regulate the voltage or the current by means of a conventional linear digital compensator such as a PI or PID controller [36, 37]. In these

methodologies the feedback signals are the only information required to control the system. According to [38] in the late 1990s a great deal of work was focused on optimal design of linear compensators that performed as well as their analog counterparts. Enhanced versions of the linear controllers have been reported in the literature [39, 40] where extra poles and zeros are added to compensate the processing delay of the controller.

1.2.3.2. Predictive or estimative methods

Predictive current control methods in dc-dc converters have been proposed as a way to eliminate or reduce the phase-lag generated by the digital control-loop [34, 41-43]. The majority of these techniques employ extra information about the dc-dc converter usually in the form of a model which relies on circuit parameters or variables such as the value of the inductor or the input voltage. Errors in the model or parameter values will degrade the performance of the controller leading to poor robustness against parameter variations, for example due to ageing or temperature changes.

For instance, [34] presents a very interesting predictive current control technique where the switch duty-ratio of the next switching cycle is estimated employing the input voltage, output voltage and the inductor-current. The predictive technique is derived for three different control targets: inductor valley-current, average-current and peak-current. It was found that by choosing appropriately the modulation method for each control target, the predictive current law is the same for all the cases and the propagation of sub-harmonic oscillations is avoided. The correlation found was as follows: valley-current control under trailing-edge modulation; peak-current control under leading-edge modulation and average-current control under triangular carrier modulation. Furthermore, the control law is extended for use in buck, boost and buck-boost converters. The technique is validated experimentally employing current-mode control for a 100 W prototype of a power factor correction boost rectifier. The control strategy was implemented on a DSP and the outer voltage-loop was regulated using a conventional PI controller. One of the disadvantages of this control strategy is that the calculations for the prediction depend on the value of the

inductor employed in the converter, which is likely to be affected by temperature variations and manufacturing variations.

A subcategory of predictive controllers is the dead-beat controller. This technique aims to design a compensator that relocates all the poles of a closed-loop transfer function to the origin of the z-plane. The dead-beat response presents special transient characteristics such as: zero steady-state error, minimum rise-time, minimum settling-time and less than 2% overshoot/undershoot [44]. However, the design of deadbeat controllers is very difficult for dc-dc converters as an accurate model of the system is required [45].

Despite this, [45] derives a dead-beat current-control law for a single-phase buck converter with current-mode control. The approach stands out as it does not follow conventional discrete control design methodologies. Instead, the design is based on an analysis of the operation and the geometry of the converter waveforms. However there are two limitations to this method: the control law has to be modified to account for the computational delay, and the duty-ratio has to be kept constant for two switching-periods. The outer voltage control-loop of the controller uses a three-step-ahead predictive PI compensator. The proposed technique is validated experimentally employing a DSC and a 140 W buck converter prototype. The results show that the deadbeat implementation has very good performance, almost equal to that of analog peak-current-mode control.

1.2.3.3. Multi-sampling methodologies

These techniques have been proposed to improve the limited bandwidth of digital controllers [32, 33, 46, 47]. The principles are straightforward, while keeping the same switching frequency, the sampling frequency is increased by a factor of *N* and the control algorithm is executed *N* times during the switching period. A modelling study carried out in [46] identified two major drawbacks of this strategy: it injects high-frequency disturbances into the feedback-loop due to the voltage/current ripple and its interaction with the ADC and DPWM quantization may enhance limit-cycle oscillations. Also, due to the nature of the sampling requirements, these methods are best suited to FPGAs as several tasks can be achieved in parallel. An implementation in a DSC is possible but is likely to be limited by the maximum sampling frequency of the inbuilt ADC and the associated processing delay.

Moreover, the task is computationally intensive leaving the processor with little resources to execute other tasks.

1.2.3.4. Mixed-signal methodologies

These methods combine digital and analog elements to exploit the best characteristics of both technologies [48, 49]. In [48] a digitally calculated reference-current is converted to the analog domain by means of a one-bit Δ-∑ digital-to-analog converter, and then used in an analogue control loop. A dedicated integrated-circuit was built for the application. In [49], a continuous-time comparator inbuilt into the microcontroller is employed to compare the reference-current generated by a digital-to-analogue converter with the real-time inductor current. The slope compensation is combined digitally with the current-reference, which is generated by amplifying the voltage control loop error with a two-pole, two-zero compensator. The principal disadvantage of this approach with regard to multi-phase converters is that digital signal controllers do not usually have sufficient inbuilt comparators.

1.2.3.5. Non-linear methodologies

A large number of papers have been written examining the application of non-linear techniques to improve the performance of digitally controlled dc-dc converters. As this area is peripheral to the main topic of the research in the thesis, only a few interesting examples of these control methodologies are described [50, 51]. In these papers, a digital control algorithm is proposed where two different compensation approaches are employed for steady-state operation/small-load changes and for large-load changes. During steady-state operation the system is compensated with a typical current-mode architecture, whilst in the presence of large-load changes an algorithm based on the principle of capacitor charge balance is employed to obtain optimal dynamic response.

In [43] a time optimal control algorithm is presented, which attempts to drive the converter to steady-state operation in the minimum time possible by estimating the capacitor zero-current cross-over point. Using this information, the required duty-ratio to achieve optimal-time response is loaded from a look-up table that has been previously

calculated. These controllers behave in a linear manner when the converter is in steady-state and as a non-linear controller for transient conditions.

1.3. Control techniques for multi-phase dc-dc converters

Multi-phase or interleaved dc-dc converters have been widely adopted for applications such as power supplies for microprocessors and communications systems [52-55], power factor correction, [56-58], and power conversion systems for electric vehicles, [59-62], amongst others.

The parallel connected channels in an interleaved converter use the same topology, component-values and switching frequency, but the switching cycles are delayed with respect to each other to create an even distribution of the waveforms over a switching period. With two interleaved channels, the switching delay is half the switching period, with three it would be one third of the period and so on. This results in the ripple-current amplitude in the common input and output filter being reduced whilst its frequency is increased. Consequently the size of input and output filter capacitors can be reduced [21, 61-65].

Also, by the use of several phases the input power is distributed across several devices, reducing the current stress and thermal load. However, one of the challenges in the operation of interleaved converters is ensuring a balanced current distribution between the phases [58, 62, 63, 65]. This practical issue arises due to the non-identical characteristics of the parallel converters, such as passive and semiconductor component mismatches and parameter variations caused by temperature changes. Current mismatches between phases might affect overall system stability and limit the operation region [63]. Also, if one of the converter phases has an excessive load current, it will experience higher thermal stress, possibly reducing the system reliability [58]. More crucially, if a coupled inductor or inter-phase transformer is used to combine the interleaved channels, current mismatches can result in the saturation of the magnetic components causing a rapid rise in circuit current, potentially damaging the semiconductor devices.

For systems with a small number of phases, this issue can be mitigated by the use of an individual current control-loop for every converter comprising the system. The current control-loops share the same reference-current, thereby all the parallel converters will track the same target-reference [66]. However, when the number of phases is high, the number of current-loops that have to be implemented creates a significant increase in cost, weight and control complexity which can make the system impractical [61, 63, 65].

Simple and cost-effective techniques for ensuring balanced operation of voltage-mode controlled interleaved converter for automotive applications were presented in [61] and [63]. These papers demonstrated that by operating the converter phases in discontinuous conduction mode the use of current-control loops for each phase may become unnecessary and therefore they can be eliminated. The control methodology employed was implemented in a FPGA and the practical evidence presented was obtained employing a sixteen-phase bidirectional converter in [61], and both sixteen- and thirty six-phase bidirectional converters in [63].

Other cost-effective techniques are introduced in references [62] and [65], which describe digital control methodologies to balance the phase currents of interleaved converters employing a single DC-link current sensor. This methodology, previously employed in three-phase PWM inverters, estimates the average value of the converter phase currents by strategically sampling the DC-link current in the middle of the transistor on-intervals and it is demonstrated that a similar performance to that of multi-loop current controller is achieved. In [62] the methodology is validated employing a 5 kW four-phase dc-dc converter for automotive battery-charging applications, whilst in [65] it is validated employing a 300 W dual-phase interleaved converter.

Other forms of control for interleaved converters include [55, 67, 68]. In [55] and [67] hysteretic voltage-mode control is employed in conjunction with a digital current balancing methodology for an *n*-phase interleaved converter that is used for a microprocessor voltage regulator. This methodology presents reduced undershoot and overshoot current caused by large magnitude transients, which is highly desirable in power supplies where tight regulation is required. Finally [68] proposes a non-linear sliding mode

control methodology to ensure current sharing in a dual-phase interleaved voltage regulator module for a microprocessor.

1.3.1. Control techniques for the dual interleaved boost converter

Relatively few papers have been published specifically relating to the control of interleaved boost converters. The studies presented in [16, 69] employ analog peak-current-mode control. The work in [16] describes a zero-voltage-switching, dual interleaved boost converter which is controlled using a commercially available dedicated integrated circuit, the UCC28220 of Texas Instruments. The work in [69] introduces a new analog control methodology, termed time-multiplexing current balance, which enhances the dynamic performance of the peak-current-mode control by reducing the effects of the right half-plane zero and achieves current balance at the same time. The control technique is implemented on a dedicated integrated circuit.

The work described in [37, 60] is concerned with the implementation of digital average-current control of the dual interleaved boost converter. Both techniques employ digital PI compensators and the control-loops are implemented in DSCs. The design of the PI compensators is carried out using an averaged small-signal model of the converter. In [37], the controller and converter are designed to operate in DCM. Conversely, in [60] the converter is designed to operate in CCM. Both publications show experimental results for a *20 kW* and a *30 kW* prototype of the converter respectively, detailing the dynamic performance of the system. However, they do not consider the effectiveness of the control methodology in balancing the phase currents.

In [70] another dual-loop digital average-current control methodology is presented, however, in contrast to the studies in [37, 60] an inner current control-loop is employed to ensure the equal distribution of the currents between the converter phases. The outer control-loop is a standard voltage regulation loop. However, the experimental results included to validate the control architecture correspond to a single point of operation and do not show the behaviour of the phase-currents during transitory events, such as load or reference changes.

[71, 72] both examine the use of predictive techniques for the control of the dual interleaved boost converter. In particular [72] shows the implementation of the predictive technique described in [34] employing valley-current control. The methodology is exhaustively verified using simulations; however, few experimental results which do not show the converter phase-currents are included, making it difficult to verify the fact that the phase-currents are balanced.

Non-linear control techniques for the dual interleaved boost converter are presented in [73-75]. In [73] a sliding-mode control methodology is implemented using a mixed-signal architecture. Reference [74] presents a current-mode controller based on hysteresis which is implemented on a FPGA.

In reference [76] an interesting multisampling control methodology implemented in a FPGA is presented. The technique stands out as the dynamic performance of the system is close to that achieved with peak current-mode control whilst also maintaining a good balance of the currents in the converter phases. In this technique, both the output voltage and the phase currents are sampled several times over a switching period. To eliminate the injection of high-frequency harmonics in the feedback loop due to the output voltage/phase current ripple discussed in [46], a moving-average filter is employed. In addition, to achieve the current regulation, the differential and the common mode currents of the converter are controlled using PI compensators.

1.4. Small-signal modelling of digitally controlled dc-dc converters and compensator design

Modelling the dynamics of all power electronic circuits including dc-dc converters is challenging due to the inherent high frequency switching action, consequently many different techniques have been proposed as a basis for control analysis and design. Amongst others, the most important modelling approaches employed in power electronics are the state-space averaging method and the sampled-data method.

The state-space averaging methodology was unified by Middlebrook and Cúk in 1977 [77]. This methodology allows derivation of an approximate, continuous, linear model of the converter by averaging the state-space equations of the different topological stages

of a circuit over a switching period and then linearizing the equations by considering small changes in the variables around a steady-state operating point. Small-signal models are often preferred for the design of converter control systems since their linear nature allows the full range of linear system techniques to be used. One of the major drawbacks of the state-space averaging approach is that it is not possible to model directly systems that employ a control variable which is different to the duty-ratio [25]. A notable extension to this modelling methodology was introduced by Ridley in [78] which enables the incorporation of the dynamics of peak-current-mode control.

So far, the most accurate technique to model dc-dc converters is the sampled-data modelling methodology [79] which is sometimes also referred to as the exact-modelling approach. This approach derives a model of the converter by the use of small-signal linearized difference equations, which describe the evolution of the state-variables at specific time-instants. However, in order to solve the difference equations, it is necessary to make use of terms with matrix exponentials, requiring a complex mathematical solution. This is perhaps, the major drawback of the methodology. Another significant drawback is that the procedure produces the converter model in closed-loop form. Therefore the mathematical procedure has to be carried out for each specific control approach.

The circuit averaging technique is a simple and intuitive approach which predates the state-space averaging method [22, 80]. There was renewed interest in the method after the development of the state-space averaging technique largely through the work of Vórperian in the early 90's [81, 82]. In his work, Vórperian proposes replacing the transistor and diode of the basic dc-dc converter topologies, by a general "averaged PWM-switch model". In this way he set out a more systematic approach for the use of circuit averaging. Another author who has also made significant contributions to models employing the circuit averaging method is Kazimierczuk [23, 83].

The detailed application of the circuit averaging method to a boost converter is presented in more detail in Chapter 2, Section 2.3.1, as it is the basis of the model developed in this work for the dual-interleaved boost converter with inter-phase transformer.

1.4.1. Modelling of digital average-current-controlled dc-dc converters

Figure 1.7 depicts the functional block diagram of a dc-dc converter with digital average-current control implemented in a DSC. The key elements are: the current transducers and their associated measurement delay, the analog-to-digital converter represented by an ideal sampler, the compensation process with its associated computational delay, the uniformly-sampled DPWM model, and the small-signal transfer function of the converter that represents the dynamics of the inductor-current response to perturbations in the duty-ratio. In this diagram it is assumed that the DPWM and the ADC are synchronized, allowing the average-current of the converter to be sampled in every cycle as described in Section 1.2.2.2. On this basis averaged converter models can be used directly to analyse the controller operation and design. Moreover, the quantization non-linearity of the ADC is often disregarded in the modelling procedure as it increases the complexity of the system, therefore the ADC is represented using an ideal sampler [31, 84, 85].

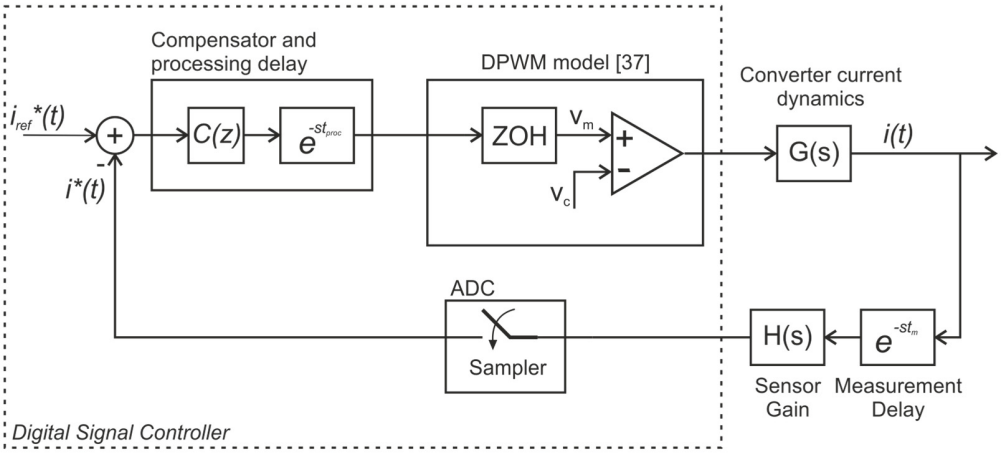

Figure 1.7. Block diagram of the model of a digital average-current controlled dc-dc converter [37].

1.4.1.1. DPWM Model

Since the duty-ratio of the output waveform for a DPWM generator remains fixed across the switching cycle, the DPWM signal is commonly modelled as an extrapolating device such as the Zero-Order Hold, ZOH. The impulse response of a ZOH over a sampling

period *T* can be represented mathematically as the sum of two unit-step functions [44], $u_s(t)$, as follows:

$$g_{h0}(t) = u_s(t) - u_s(t-T) \tag{1.1}$$

By taking the Laplace transform of Equation (1.1), the transfer function of the ZOH can be found:

$$G_{h0}(s) = \frac{1-e^{-sT}}{s} \tag{1.2}$$

Equation (1.2) is usually found connected in cascade with the converter transfer functions to represent the effects of the modulator. This model has been widely employed by different authors to model the behaviour of a DPWM in power converters and is also adopted in this thesis. However, more detailed small-signal models of this element have been proposed by several authors. Some of the earliest derivations of the small-signal model of the UPWM with leading-edge operation were carried out in [86, 87]. More recently (2004), a Laplace-domain small-signal model of this element was developed in [35] for the three most common configurations: trailing-edge, leading-edge and triangular carrier modulation. Table 1.1 summarizes the expressions for this model. Two years later, this work was extended when the z-domain small-signal expressions of the DPWM were determined [84].

Table 1.1. Laplace-domain and frequency-domain models for uniformly-sampled pulse-width modulations as described in [37] by Van de Sype et al.

Modulation Strategy	DPWM(s)	DPWM(jω)
Leading-edge	e^{-sDT}	$1\angle(-j\omega DT)$
Trailing-edge	$e^{-s(1-D)T}$	$1\angle(-j\omega(1-D)T)$
Triangular carrier Symmetric on-time	$\frac{1}{2}\left(e^{-s\frac{1}{2}(1-D)T}+e^{-s\frac{1}{2}(1+D)T}\right)$	$\cos\left(\frac{\omega DT}{2}\right)\angle\left(-\frac{\omega T}{2}\right)$
Triangular carrier Symmetric off-time	$\frac{1}{2}\left(e^{-sDT}+e^{-s(2-D)T}\right)$	$\cos\left(\frac{\omega(1-D)T}{2}\right)\angle\left(-\frac{\omega T}{2}\right)$
Triangular carrier Double update-mode	$\frac{1}{2}\left(e^{-s(1-D)T}+e^{-sDT}\right)$	$\cos\left(\omega(D-\frac{1}{2})T\right)\angle\left(-\frac{\omega T}{2}\right)$

*D: Quiescent duty-cycle, T: Sampling period.

Furthermore, other authors, [85], have presented closed-form discrete models for the buck, boost, and buck-boost converters, where the effects of the DPWM are incorporated in the closed-loop model for leading- and trailing-edge modulation and z-domain expressions are given for each case.

Buso and Mattavelli in [31] introduced an approximation of the DPWM small-signal model proposed in [37] when the triangular carrier modulation with symmetric on-time is employed. The authors conclude that for this particular modulation case and when a small-signal averaged model is employed to describe the converter dynamics, it is sufficient to approximate the transfer-function of the DPWM by that of a ZOH.

1.4.1.2. Quantization and limit cycle oscillations

Limit cycle oscillations, LCOs, caused by the quantization effects in digital controllers are due to the limited resolution of the ADC and DPWM [44, 88]. However for the sake of simplicity, these effects are not usually considered in the modelling of dc-dc converters. In [89-91] the presence of LCOs in dc-dc converters is studied and it is concluded that a high integral gain and that a coarse DPWM resolution contribute significantly to the presence of LCOs amongst other conditions. To improve the resolution of DPWM modules without the need to increase their clock frequency, techniques such as dithering and phase-locked loops have been proposed in [38, 90].

1.5. Compensator design for digital controlled dc-dc converters

Digital redesign and direct digital design [44, 88, 92] are the two main approaches that have been widely employed for the design of linear compensators in dc-dc converters. More recently in [93] an intuitive digital design approach was proposed which allows the use of analogue control tools to design digital compensators for dc-dc converters. These methodologies will be reviewed in the following sections.

1.5.1. Digital redesign

This is an indirect design technique where a digital equivalent of an analog compensator is used to regulate the system. In the design process the analog compensator

is first devised in the continuous-domain by means of a Laplace-domain model of the plant. The resulting analog compensator is then transformed to its equivalent in the digital domain, or the z-domain, by means of an appropriate discretization method. The principal advantage of this approach is that it provides the designer with the intuitiveness of analog control theory where several techniques such as root-locus, Bode diagrams and Nyquist plots amongst others, can be employed to choose a compensator to satisfy the desired system performance. A variety of discretization methods is available to approximate the analog controller. The most common are: the forward Euler method or forward rectangular rule, the backward Euler method or backward rectangular rule, the step-invariant or zero-order-hold method, the bilinear transformation or Tustin's method, and the pole-zero matching method [92].

However, this design approach has a number of limitations. First, it requires an accurate model of the complete system including the effects of the digital-to-analog and the analog-to-digital converters. This can be achieved by the use of zero-order-hold transfer functions and by the incorporation of transport delays. However the use of transport delays introduces a non-linearity. To overcome this issue, these delays are typically represented by the Padé approximation of the transport delay [94].

Second, none of the discretization methods preserves all the characteristics of the original analog controller in the digital domain. The backward Euler and forward Euler transformations are the simplest but they only provide an exact match in the time domain. Any information in the frequency domain is distorted due to aliasing effects [92]. The bilinear transformation preserves the magnitude and phase response of the system in the frequency-domain up to 1/10 of the sampling frequency, nonetheless, the time domain response is not accurately represented [92]. The step-invariant transformation maintains the response of the system to step or staircase inputs only. Finally, the pole-zero match transformation retains the location of the poles and zeros of the compensator, but its implementation is complicated and is affected by aliasing if the frequency-location of the zeros of the compensator is greater than half of the sampling frequency [92].

However, in spite of these difficulties, the digital redesign methodology has been widely adopted and studied for dc-dc converters. In [95, 96] studies were carried out to

determine the best discretization method to use in the design of a dc-dc converter controller. An analog PI compensator was discretized using the techniques described above and it was concluded that the backward Euler method offered the best performance. Some examples of the use of digital redesign for dc-dc converters can be found in [37, 39, 41, 45, 49, 95, 96].

1.5.2. Direct digital design

In the direct digital design methodology, the controller is directly devised in the z-domain by means of a discrete-time model of the plant. When the model of the plant is already in the z-domain the design procedure can be carried out directly. However, if the model of the plant is in the Laplace-domain, it is necessary to find an approximate z-domain model. Provided that the Laplace-model of the plant is connected in cascade with a digital-to-analog converter and that the digital-to-analog converter can be modelled as a zero-order-hold, then the approximated discrete-time model of the plant and the DAC can be derived by the use of the zero-order-hold transform [44, 88, 92]. This is usually the case in power electronics and other application areas.

This design technique is advantageous as it allows the modelling of the different delays involved in the digital control process without the need for linear approximations. Moreover the digital compensator designed can be directly implemented in a microcontroller without any loss of accuracy. This design approach also enables the use of exclusive digital control tools, such as the design of dead-beat compensators. Perhaps, the most serious disadvantage of this approach is that it lacks the intuitiveness of analog control design procedures which are wide spread and well-known. For instance, the use of Bode plots, which are commonly used for dc-dc converters is not straightforward since the variable z is related to $j\omega$ by means of $e^{j\omega}$ [44]. In power converter controller design, although it has been demonstrated that the use of direct digital design leads to better performance than digital redesign [38, 95], direct digital design has not been widely adopted and only a few publications have been found employing this approach.

1.5.3. Other design methodologies

In 2007 [93], Al-Atrash proposed a new design approach where direct-digital design is carried out without the need of a discrete-time model of the converter. This is accomplished by plotting the combined frequency response of all the elements comprising the open-loop transfer function. The frequency response of the digital-elements, such as time-delays and zero-order-holds, is obtained using the direct relation $z^{-1} = e^{-sT} = e^{-j2\pi fT}$, which in contrast to the typical discretization methods such as backward Euler, or the bilinear transformation is an exact relationship. Therefore the frequency response is valid for any range of frequencies. Moreover, in this work, Al-Atrash defines a set of discrete zeroes, poles and complex conjugated zeroes and poles, which have a frequency response in the digital domain that is similar to that of their analog counterparts. With these two tools, the design of a digital compensator can be carried out in the analog domain without any loss of accuracy. Perhaps, the only disadvantage of this methodology is that a computational tool is necessary to obtain the frequency response of the mixed-signal system.

1.6. Review of modelling of multi-phase dc-dc converters

By far, the most widely used technique for analysing and designing the controllers for interleaved converters is the state-space averaging method [60, 70, 97-101]. This technique is mostly applied to model digitally controlled dc-dc converters with average-current control, which is used to justify the use of an averaged model. Other methodologies reported, which do not necessarily use digital control include sampled-data modelling [102], signal flow graphs [103], multi-frequency small-signal modelling [54] and non-linear approaches [104, 105].

In the research presented in [97] and [98] a state-space averaged model is developed for the steady-state analysis of a dual interleaved boost converter in the time domain. In [97] only CCM is considered, whilst in [98] both CCM and DCM are considered. However, small-signal transfer functions are not derived in these papers.

The research in [70] and [99] describes the small-signal averaged state-space model of a dual interleaved boost converter with inter-phase transformer under CCM. In [70] the model equations are presented by considering the small-signal perturbations of the duty-ratios for each of the converter phases independently. As a consequence, a cross-coupling transfer-function between the phases arises in the system. However, this new information is not exploited in the design of the controller that was proposed and the procedure to derive the model equations is not described. In [99] the full procedure to obtain the small-signal model is illustrated for the unidirectional and the bidirectional operation of the converter. However, the small-signal perturbation of the duty-ratios of the converter phases are considered to be identical limiting the accuracy of the model.

In references [60] and [100] the small-signal averaged PWM switch techniques based on the approaches proposed by Kazimierczuk et al. in [83] and Vórperian et al. in [81] respectively, are employed to model multi-phase dc-dc boost converters. However, the models obtained assume identical duty-ratios in the converter phases even for small-signal perturbations.

The research in [52] and [69] presents small-signal averaged models of peak current mode controlled interleaved converters used as voltage regulators for microprocessors, which are derived employing the enhanced averaged model proposed by Ridely in [78]. In [52] a dual-phase interleaved buck converter is considered with and without coupled inductors. The model developed takes into account the small-signal perturbation of the duty-ratio of the converter phases independently and the performance of the converter is compared using the coupled and the non-coupled versions, revealing that the coupled inductors, or inter-phase transformer, improve the bandwidth of the system. In [69] a dual-phase interleaved buck converter is employed where a control technique termed time-multiplexing current balance control is proposed. Employing the model of the converter, which includes the small-signal perturbation of the phase duty-ratios separately, it is demonstrated that the control technique improves the system bandwidth by relocating the right-half plane zero of the control-to-input-current transfer function to higher frequencies. However, the models presented in both [52] and [69] do not account for the interleaved operation of the converter phases.

References [106] and [101] report the development of state-space averaged models for two different multiphase dc-dc converters. In [106], a generalized algebraic methodology is presented to obtain the small-signal state-space average model of a multiphase converter composed of 2N boost cells with coupled inductors. Two key-assumptions are made for the development of this model: the parameters of the boost cells are identical and the small-signal perturbations in the duty-ratios are the same for all the converters. The transfer-functions obtained from this model are second order no matter how many phases are employed in the converter. Moreover, the performance of the control-to-output, line-to-output and output impedance transfer functions are compared for different inductor couplings by simulation in the frequency-domain and in the time-domain experimentally. It is concluded that the use of directly-coupled inductors offers low overshoot and insensitivity to input-voltage variations; and that the use of inversely coupled inductors provides fast response and insensitivity to load variations. However, this modelling approach disregards the interleaved operation of the boost cells, and does not include any feedback control.

In [101] the modelling of a multiphase interleaved buck converter is presented. Similar to the work in [106], a generalized methodology is proposed to model *n* interleaved buck converter stages. However, in contrast with [106], this work takes into account the small-signal perturbation of each of the converter duty-ratios and several stages of coupled inductors are considered. The algebraic model is then applied to an eight-phase buck converter, and the resultant transfer functions obtained are employed to design a PI compensator using the digital-redesign approach. The performance of the design is verified experimentally in the frequency and the time domain. Also, ripple and efficiency analyses are presented. However, the modelling procedure of the current-feedback loop does not account for the effects of zero-order-holds and the interleaved interaction of the converter phases.

The sampled-data model of a dual interleaved boost converter with inter-phase transformer under peak current-mode control was described in [15, 102]. This model is capable of predicting the stability limits of the converter with a great deal of accuracy and is based on the technique introduced in [79]. The methodology proposed exploits the

symmetry of the converter waveforms to reduce the complexity of the algebraic procedure, nevertheless, the model obtained is still very complex and difficult to use for control design. This study also presents a detailed analysis of how the pole and zero locations of the control-to-output transfer functions of the converter are affected by steady-state operating conditions and the circuit parameters such as the ratio between input inductance and IPT self-inductance.

A notable study reported in [104] demonstrated by means of nonlinear analyses the inability of state-space averaging to distinguish between converters operating in phase from those operating using interleaving and the ineffectiveness of the technique to account for fast scale dynamics.

Currently, most of the reported research using state-space averaged models, apart from [52, 69, 70, 101], assumes that both the quiescent values of the duty-ratios and their small-signal perturbations are identical for each of the converter phases. Also, none of the modelling techniques presented using averaging techniques account for the interaction between the interleaved converters. This shortcoming is addressed in this thesis through the development of a method that enables an averaged model to account for the interleaved operation and interaction of a two-phase interleaved boost converter. This is carried out by means of multi-rate sampled-data systems theory and is used to establish new stability limits for the converter. To the best of the author's knowledge this technique has not previously been applied to dc-dc converters.

1.7. Summary of literature review

Digital control of the basic dc-dc converter topologies has been widely researched and reported in the literature, especially for low-power applications with operating frequencies of the order of hundreds of *kHz* and in some cases up to *1 MHz.* In these applications a key objective is achieving a fast-dynamic performance. As a consequence, improved linear compensators, predictive techniques and multi-sampling methodologies have been proposed to overcome the processing delay that can have a detrimental effect on the current-control-loop bandwidth. The use of DSCs, FPGAs and dedicated integrated-circuits has been reported for several applications favouring the use of DSCs as they already

contain all the necessary modules to control a power converter allowing rapid application development. However, most of the research work introducing new control architectures and techniques have been reported employing FPGAs.

With respect to multi-phase converters, a key priority is control strategies that ensure equal current-sharing between the converter cells whilst also providing good dynamic performance. These converters are widely applied in high-power applications as they allow a reduction in the size of passive components due to the effective increase of input and output ripple frequencies and reduced-stress on semiconductor devices. When a high number of converter cells are employed, cost-effective control solutions which reduce or eliminate the need of a single current-control loop per phase are desired. For converters with a small number of phases, such as the dual interleaved boost converter, the use of a single current-control loop per phase has been widely adopted as it ensures the equal distribution of the current between the converter cells. Analog control and digital average-current control implementations in DSCs and FPGAs have been reported in the literature.

With regard to the modelling and analysis of multi-phase converters, averaging techniques tend to be preferred due to their simplicity. Other techniques such as sampled-data modelling and non-linear approaches have also been employed to explore non-linear and switching related phenomena and to demonstrate the limitations of the averaging techniques.

Since much of the development of digital control techniques has been carried out for single-phase dc-dc converters, the compensator design for multi-phase converter tends to be approached in the same way. Also, there is a lack of a well-defined methodology to model the elements of a digital power electronic control-loop. Moreover, digital redesign has been widely adopted due to its strong links with analog control methodologies. Nonetheless, this technique has been demonstrated to be less accurate than direct digital design. Overall, digital modelling of power converters is a field still in development, and direct digital design has not been widely adopted since digital redesign is more similar to the familiar analogue design methodologies.

In this thesis a direct digital design approach is used to model the dual interleaved boost converter in closed-loop and by the use of multi-rate data-sampled theory the circuit averaging techniques are enhanced to predict instabilities caused by the interleaved operation of multi-phase converters.

1.8. Outline of this thesis

In the first part of Chapter 2, the methodology employed to obtain a small-signal, averaged model of the dual-interleaved boost converter with inter-phase transformer is presented. The model is validated employing simulations from SABER. In the second part of Chapter 2, the operation of the converter employing digital valley-current, average-current and peak-current control is examined and the advantages and disadvantages of the techniques are identified.

In Chapter 3, the design and construction of a digital control platform for the dual-interleaved boost converter and the implementation of the digital average-current control are presented together with the development of a detailed closed-loop SABER model. The correct operation of the control platform and the SABER simulation model are verified using steady-state and transient experimental results from a *25 kW* prototype.

In Chapter 4, a modelling methodology based on the sampler decomposition technique is introduced which allows to obtain the small-signal, closed-loop transfer functions of the converter accounting for the interleaved sampling and operation of the converter phases. It is demonstrated that the model is able to predict instabilities caused by this feature of the interleaved converter. The results of the proposed model are validated using time-domain and frequency-domain simulation results from the SABER models developed in Chapter 3.

In the first part of Chapter 5, a sensitivity analysis of the pole trajectories of the model developed in Chapter 4 is undertaken to identify how the main parameter variations of the converter affect the absolute stability of the system. In the second part of this Chapter the parameters of a PI compensator are selected to ensure maximum response speed and minimum overshoot to step-change transients based on the theories and models

developed in this thesis. The final design is validated using simulation and experimental results from the converter prototype.

Finally Chapter 6, presents the conclusions of this dissertation and its contributions to the field of research. The chapter concludes by suggesting potential areas where future research work can be carried out.

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Chapter 2
Converter operation, modelling and digital control

2.1. Introduction

This Chapter begins with a brief analysis of the dual-interleaved boost converter with inter-phase transformer under steady-state, continuous conduction mode. The main waveforms are examined and their relevant mathematical expressions are presented. Then, a methodology to obtain the averaged small-signal ac model of the converter is described and the state-space representation of this model is derived. Next, the averaged small-signal ac model is validated by the use of a switched and a large-signal averaged model implemented in SABER. Finally, the last section explains the principles of the digital phase-current regulation for the converter employing uniformly-sampled pulse-width modulation. Three different modulation strategies are described: leading-edge modulation, trailing-edge modulation and triangular carrier modulation with symmetric on-time.

2.2. Operation of the dual interleaved boost converter with inter-phase transformer

Figure 2.1 presents the circuit diagram of the dual interleaved boost converter with inter-phase transformer, DIBC with IPT. The circuit comprises an H-bridge formed by IGBTs connected with antiparallel diodes. The mid-point nodes of the switching legs of the H-bridge are denoted *A* and *B* in the circuit diagram. This will be used to designate the converter phases. In addition, the IGBTs and their respective diodes are designated according to their position in the switching legs, namely the upper transistors and diodes

Q_{2a}, D_{2a}, Q_{2b} and D_{2b}; and the bottom ones Q_{1a}, D_{1a}, Q_{1b} and D_{1b}. For the purposes of this work, the circuit is assumed to operate in boost or step-up mode only. In consequence, only the bottom transistors, Q_{1a} and Q_{1b}, are operated and their corresponding quiescent duty-ratios are referred to as D_a and D_b. The top transistors are deactivated at all times allowing their antiparallel diodes, D_{2a} and D_{2b}, to handle the current flowing towards the load. Normally, under steady-state conditions the duty-ratios of Q_{1a} and Q_{1b} would be equal, but with the turn-on instant of Q_{1b} delayed by half a cycle behind Q_{1a} thereby producing the interleaved operation of the circuit.

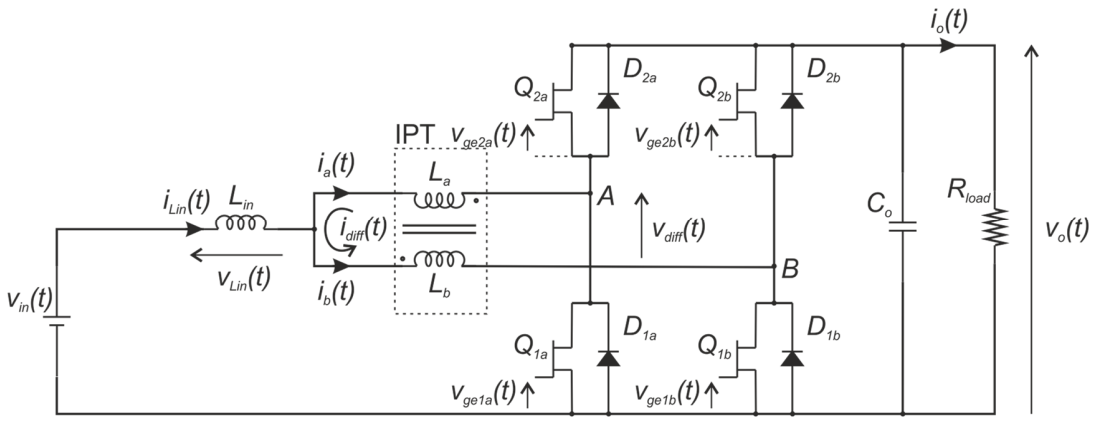

Figure 2.1. Dual interleaved boost converter with inter-phase transformer.

A pair of tightly, inverse-coupled inductors is connected to nodes *A* and *B* of the H-bridge, and the centre-tap of the coupled inductors forms the connection to the input-inductor L_{in}. Assuming that the input current divides equally between the windings of the IPT, the dc flux is zero due to the inverse coupling of the windings and only ac flux is present in the core. The IPT acts as an inductive voltage-divider and furthermore, due to the phase-shift between the boost cells, the frequency of the inductor's voltage is twice the switching frequency.

In the schematic of the circuit, the self-inductance of the coupled inductors is denoted L_a and L_b respectively, whilst their mutual inductance will be denoted L_m. The total inductance measured between the nodes *A* and *B*, will be referred to as the differential inductance of the IPT, $L_{diff} = L_a + L_b + 2L_m$. Finally, the positive and negative rails of the H-bridge are connected to the converter output, comprising the output capacitor, C_o, connected in parallel with the load resistance, R_{load}.

Under steady-state conditions, $D_a = D_b = D$, and assuming that the current flowing through the IPT windings is continuous, three operating modes can be identified: $D < 0.5$, $D = 0.5$ and $D > 0.5$. Figure 2.2 illustrates the principal voltage and current waveforms of the converter for these operating modes. The waveforms were sketched under the assumption that $L_a = L_b$ and that the windings are perfectly coupled. Furthermore it is assumed that the input-current divides equally between the two halves of the IPT.

The first graph of each group shows the transistor gate-to-emitter voltages. The solid waveform corresponds to the phase-a transistor, $v_{ge1a}(t)$, while the dashed waveform belongs to the transistor of phase-b, $v_{ge1b}(t)$. The second and third graphs show the input inductor voltage, $v_{Lin}(t)$, and the voltage between the nodes *A* and *B*, also known as the differential voltage, $v_{diff}(t)$. In the next two graphs, the input inductor current, $i_{Lin}(t)$, and the differential current, $i_{diff}(t)$, are sketched. Finally the last graph depicts the currents flowing through the IPT windings, $i_a(t)$ and $i_b(t)$, in solid and dashed waveforms respectively.

The converter can assume four different circuit configurations depending on the combination of active diodes/transistors. These configurations are identified with Roman numerals at the top of the waveforms and are illustrated in Figure 2.3. For $D < 0.5$, the converter switches between configurations I, II and III. For $D > 0.5$ configurations I, III, and IV occur. Finally, for the case of $D = 0.5$ only configurations I and II are present.

In configuration I transistor Q_{1a} is activated clamping node A to ground. Simultaneously diode D_{2b} is in conduction connecting node B to the converter output, consequently the differential voltage $v_{diff}(t)$ equals $-V_o$, where V_o is the average value of the output voltage. Additionally, a voltage divider is formed by the IPT windings, and for this reason the voltage level across the input inductor is $v_{Lin}(t) = V_{in} - V_o/2$.

In configuration II transistors Q_{1a} and Q_{1b} are deactivated whilst diodes D_{2a} and D_{2b} are in conduction. As a consequence, nodes *A* and *B* are connected to the same terminal and therefore $v_{diff}(t)$ is equal to zero. Furthermore, owing to the perfect coupling of the IPT the windings appear as a short-circuit to the input-current $i_{in}(t)$, therefore the input inductor voltage is $v_{Lin}(t) = V_{in} - V_o$, where V_{in} is the average value of the input voltage.

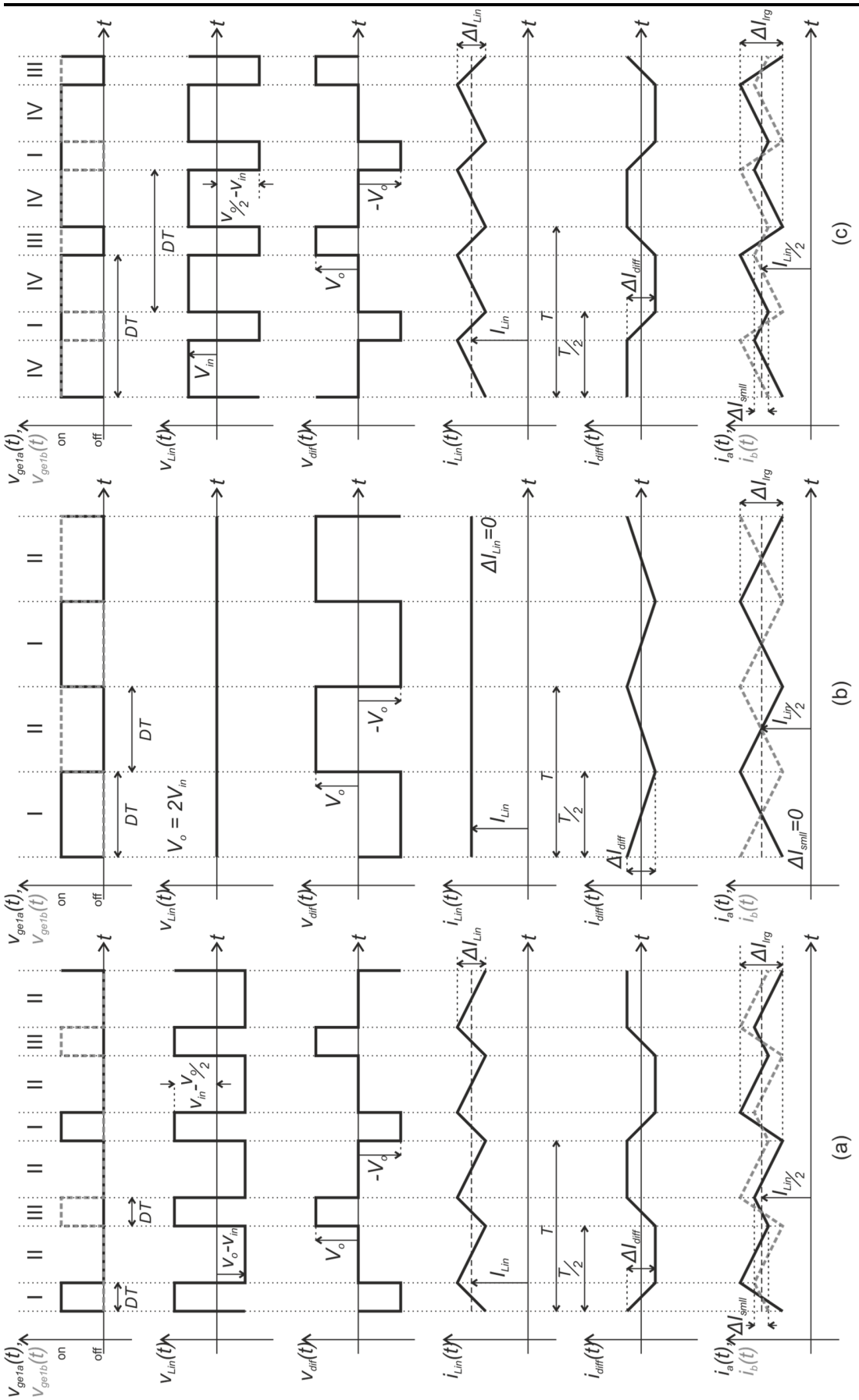

Figure 2.2. Ideal steady-state waveforms of the dual interleaved boost converter with IPT. (a) *D < 0.5*; (b) *D = 0.5*; (c) *D > 0.5*.

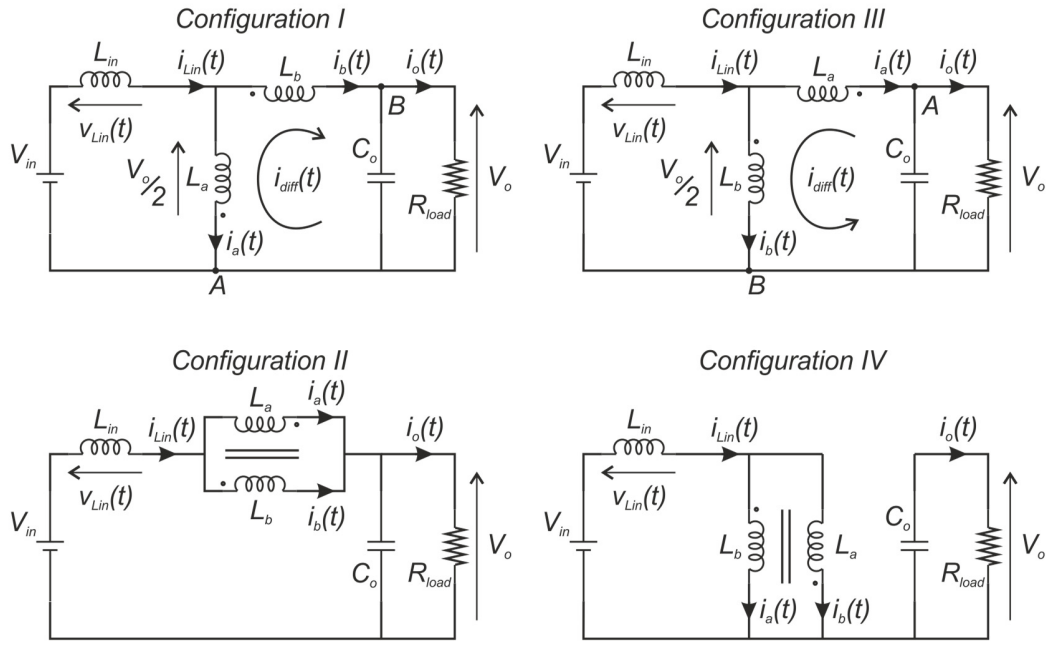

Figure 2.3. Equivalent circuits of the dual interleaved boost converter with inter-phase transformer for continuous conduction mode of operation.

Configuration III arises when Q_{1b} is activated and D_{2a} is conducting. This configuration is a mirror image of configuration I where the differential voltage $v_{diff}(t)$ is now equal to $+V_o$ and the input inductor voltage is $v_{Lin}(t) = V_{in} - V_o/2$.

Finally Configuration IV arises when both transistors Q_{1a} and Q_{1b} are activated clamping the nodes *A* and *B* to ground and making $v_{diff}(t)$ equal to zero. The voltage seen across the input inductor in this case is $v_{Lin}(t) = V_{in}$.

Whenever the converter operates with $D \neq 0.5$ it switches between four configurations over a switching period. For this reason the input inductor voltage in Figure 2.2(a) and 2.2(c) is an asymmetrical square waveform alternating between two levels at twice the switching frequency. The differential voltage instead, is a three-step waveform at the switching frequency with a peak-to-peak value of twice V_o.

The voltage conversion ratio of the converter, is obtained by equating the positive and negative volt-seconds across L_{in} and is identical to that for the single-phase boost converter operating in the continuous conduction mode, [1,2]:

$$\frac{V_o}{V_{in}} = \frac{1}{1-D} \tag{2.1}$$

From Equation (2.1) and assuming that the converter is lossless, a reciprocal expression for the current conversion ratio may be determined:

$$I_{Lin} = \frac{V_o}{R_{load}(1-D)} = \frac{V_{in}}{R_{load}(1-D)^2} \tag{2.2}$$

where R_{load} is the load resistor. The input inductor ripple current, ΔI_{Lin}, and the peak-to-peak value of the differential current, ΔI_{diff}, can be inferred from their respective voltage waveforms. The equations to calculate these ripples are shown in Table 2.1. Of particular note is the fact that the input ripple current, ΔI_{Lin}, is zero for $D = 0.5$.

As the input current divides equally between the IPT windings, the phase currents are equal to half of the input current plus the differential current generated by the differential voltage across the IPT. Therefore, the resulting phase currents can be expressed as:

$$i_a(t) = \frac{i_{Lin}(t)}{2} - i_{diff}(t) \tag{2.3}$$

$$i_b(t) = \frac{i_{Lin}(t)}{2} + i_{diff}(t) \tag{2.4}$$

Table 2.1. Summary of ripple current expressions for the DIBC with IPT. $D_a = D_b = D$.

	D < 0.5	***D = 0.5***	***D > 0.5***
Input current ripple	$\Delta I_{Lin} = \frac{V_{in}DT}{2L_{in}}\left(\frac{1-2D}{1-D}\right)$	$\Delta I_{Lin} = 0$	$\Delta I_{Lin} = \frac{V_{in}T}{2L_{in}}(2D-1)$
Differential current ripple	$\Delta I_{diff} = \frac{V_{in}DT}{L_{diff}}\left(\frac{1}{1-D}\right)$	$\Delta I_{diff} = \frac{V_{in}T}{L_{diff}}$	$\Delta I_{diff} = \frac{V_{in}T}{L_{diff}}$
Large phase-current ripple	$\Delta I_{lrg} = \frac{V_{in}DT}{(1-D)}\left(\frac{1-2D}{4L_{in}} + \frac{1}{L_{diff}}\right)$	$\Delta I_{lrg} = \frac{V_{in}T}{L_{diff}}$	$\Delta I_{lrg} = V_{in}T\left(\frac{2D-1}{4L_{in}} + \frac{1}{L_{diff}}\right)$
Small phase-current ripple	$\Delta I_{smll} = \frac{V_{in}DT}{(1-D)}\left(\frac{1-2D}{4L_{in}} - \frac{1}{L_{diff}}\right)$	$\Delta I_{smll} = 0$	$\Delta I_{smll} = V_{in}T\left(\frac{2D-1}{4L_{in}} - \frac{1}{L_{diff}}\right)$

The waveforms corresponding to these currents are illustrated in the last graph of Figure 2.2. Two different ripple levels denoted large ripple-current, ΔI_{lrg}, and small ripple-current, ΔI_{smll}, are identified in these current waveforms.

Table 2.1 summarizes the expressions of the ripple-currents for $i_{Lin}(t)$, $i_{diff}(t)$, $i_a(t)$ and $i_b(t)$ for the three modes of operation of the DIBC with IPT. The derivation of these expressions is given in Appendix A.

2.3. Small-signal ac modelling of the converter

The small-signal model of the dual interleaved boost converter with IPT employed in this work is based on an extension of the well-known circuit averaging method. This technique referred to as averaged switch modelling by Erickson, [3], aims to replace the converter switching elements by an equivalent averaged switch model, thereby eliminating the time-dependent-switching of the circuit topology. The resulting equivalent circuit of the converter can then be perturbed and linearized to obtain a small-signal model. The following section will review this procedure for the single-phase boost converter.

2.3.1. Averaged switch modelling of the boost converter

Figure 2.4(a) depicts a single-phase boost converter switch-network comprising a transistor and a diode. The instantaneous voltages and currents at the ports of this network are denoted $v_1(t)$, $i_1(t)$, $v_2(t)$ and $i_2(t)$. For convenience ports *1* and *2* will be referred to as the input port and the output port respectively. Assuming lossless components and instantaneous switching, the waveforms of $v_1(t)$ and $i_2(t)$ are sketched in Figure 2.4(b). In this Figure a single period of the waveforms is illustrated. From Figure 2.4(b), $v_1(t)$ and $i_2(t)$ can be expressed as:

$$v_1(\mathrm{t}) = \begin{cases} 0 & 0 < t < dT \\ v_2(\mathrm{t}) & dT < t < T \end{cases} \tag{2.5}$$

$$i_2(\mathrm{t}) = \begin{cases} 0 & 0 < t < dT \\ i_1(\mathrm{t}) & dT < t < T \end{cases} \tag{2.6}$$

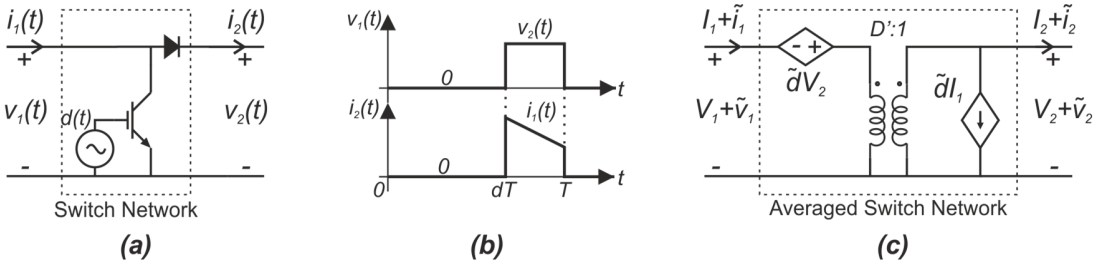

Figure 2.4. (a) Single-phase boost converter switch network. (b) Switch network waveforms. (c) Equivalent dc and ac small-signal averaged switch network model.

Under the assumption that the switching ripples of $v_1(t)$ and $i_2(t)$ are small or at least linear functions of time, Equations (2.5) and (2.6) can be averaged over a switching period, T, yielding:

$$\langle v_1(t)\rangle_T = (1-d(t))\langle v_2(t)\rangle_T \tag{2.7}$$

$$\langle i_2(t)\rangle_T = (1-d(t))\langle i_1(t)\rangle_T \tag{2.8}$$

Equations (2.7) and (2.8) may then be perturbed and linearized about a quiescent point of operation yielding:

$$V_1+\tilde{v}_1 = (1-D)(V_2+\tilde{v}_2)-\tilde{d}V_2-\tilde{d}\tilde{v}_2 \tag{2.9}$$

$$I_2+\tilde{i}_2 = (1-D)(I_1+\tilde{i}_1)-\tilde{d}I_1-\tilde{d}\tilde{i}_1 \tag{2.10}$$

where the voltage and currents at the input and output ports and the duty-ratio are expressed as the sum of the quiescent value plus a small ac variation: $V_1+\tilde{v}_1$, $I_1+\tilde{i}_1$, $V_2+\tilde{v}_2$, $I_2+\tilde{i}_2$ and $D+\tilde{d}$. The equivalent averaged switch model, Figure 2.4(c), can be obtained from Equations (2.9) and (2.10) by neglecting the nonlinear terms $\tilde{d}\tilde{v}_2$ and $\tilde{d}\tilde{i}_1$. This assumption is valid provided that the ac variations are much smaller than the quiescent values. The equivalent averaged circuit shown in Figure 2.4(c) is an alternative version of the original one devised by Vórperian [4] which results in a simpler boost circuit model. The equivalent switch comprises three elements:

1. A dependent voltage source, $\tilde{d}V_2$, where $\tilde{d}$ is the small ac variation of the converter duty ratio and V_2 is the quiescent value of the voltage at the output port of the switch network.

2. An ideal (dc) transformer with turns-ratio *D':1*, where *D' = (1 - D)* and *D* is the quiescent value of the transistors duty ratio.

3. A dependent current source, $\tilde{d}I_1$, where the term I_1 is the dc or quiescent value of the current at the input port of the switch network.

The procedure followed to obtain the model of the DIBC converter using the switch model of Figure 2.4(c) will be explained next.

2.3.2. Averaged small-signal modelling of the dual interleaved boost converter

The DIBC with IPT is shown in Figure 2.5 where the transistors of each boost cell are controlled by the independent sources $d_a(t)$ and $d_b(t)$. Also two additional elements are included: the series resistance of the input inductor, R_{in}, and a small-signal current source, $i_z(t)$, connected in parallel with the load resistor. The latter element is also known as a perturbation current and can be employed to emulate load changes in the circuit model. Two switch networks are identified in this circuit which can be replaced by the averaged model of Figure 2.4(c).

Moreover, to model this converter accurately it is necessary to account for the presence of the inter-phase transformer. As demonstrated by Maksimović in [5], the well-known model of a transformer based on self and mutual inductances is well suited when the leakage inductance of the coupled inductors does not play a determinant role in the converter operation.

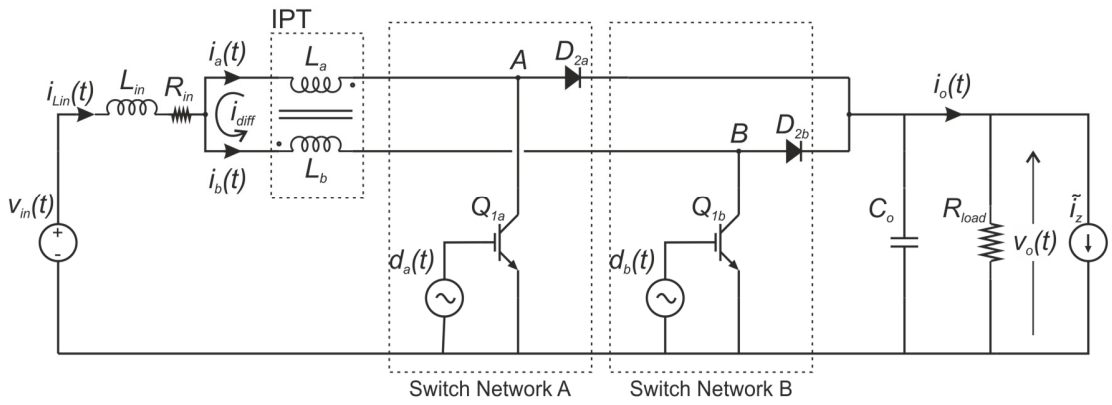

Figure 2.5. Open loop circuit of the dual interleaved boost converter with IPT.

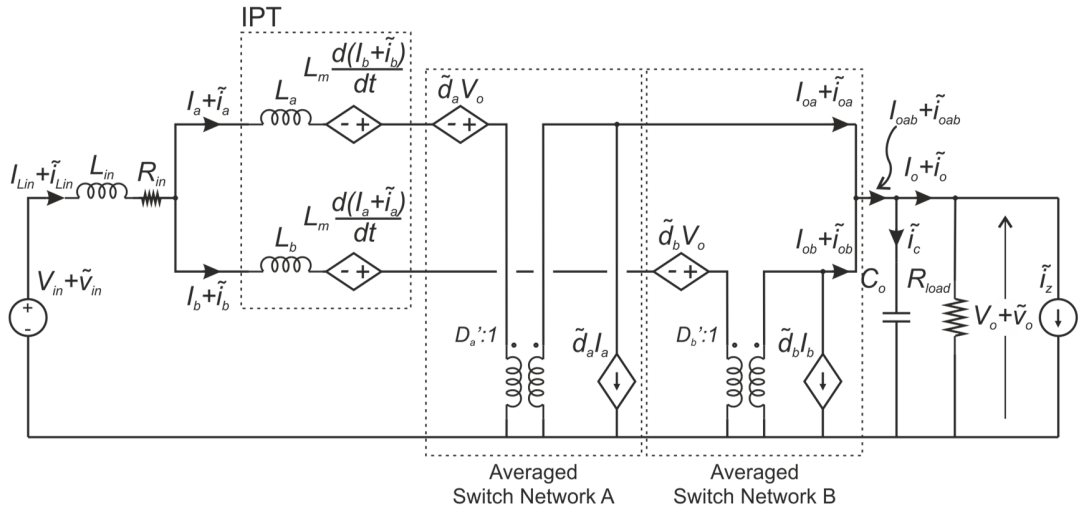

Figure 2.6. dc and small-signal averaged model of the DIBC with IPT.

Upon replacement of the equivalent switch networks and substitution of the IPT by its equivalent model, the dc and averaged small-signal ac model of the converter shown in Figure 2.6 is obtained. In this new circuit the voltage at the input port of each averaged switch network is equal to the local average voltage at the nodes *A* and *B* of the original circuit respectively, whilst the input port currents are easily identified as the perturbed local average phase currents $I_a+\tilde{i}_a$ and $I_b+\tilde{i}_b$.

Owing to the parallel connection of the switch networks, the output port voltage of each network is the same as the converter output voltage. Similarly, the output currents at each network are denoted $I_{oa}+\tilde{i}_{oa}$ and $I_{ob}+\tilde{i}_{ob}$ which comprise together the total output current, $I_{oab}+\tilde{i}_{oab}$, delivered to C_o and R_{load}. Finally, the current flowing through C_o is denoted $\tilde{i}_c$ and the current delivered to the load resistance is $I_o+\tilde{i}_o$.

By inspection of Figure 2.6 and employing Equation (2.10), the current at the output ports of the switch networks A and B can be written as:

$$\left(I_{oa}+\tilde{i}_{oa}\right)=\left(1-D_a\right)\left(I_a+\tilde{i}_a\right)-I_a\tilde{d}_a \tag{2.11}$$

$$\left(I_{ob}+\tilde{i}_{ob}\right)=\left(1-D_b\right)\left(I_b+\tilde{i}_b\right)-I_b\tilde{d}_b \tag{2.12}$$

Adding Equations (2.11) and (2.12) to obtain the total converter output current, yields:

$$I_o + \tilde{i}_o + \tilde{i}_c + \tilde{i}_z = (1-D_a)(I_a + \tilde{i}_a) - I_a\tilde{d}_a + (1-D_b)(I_b + \tilde{i}_b) - I_b\tilde{d}_b \quad (2.13)$$

Equation (2.13) may be split by grouping the steady-state and the small-signal terms from both sides of the equation into two separate equations:

$$I_o = (1-D_a)I_a + (1-D_b)I_b \quad (2.14a)$$

$$\tilde{i}_o + \tilde{i}_c + \tilde{i}_z = (1-D_a)\tilde{i}_a - I_a\tilde{d}_a + (1-D_b)\tilde{i}_b - I_b\tilde{d}_b \quad (2.14b)$$

Under steady-state conditions, the quiescent value of the duty-ratios D_a and D_b can be assumed identical, in other words $D_a = D_b = D$. Furthermore as I_{Lin} divides equally between the IPT windings, the quiescent value of the phase currents I_a and I_b is equal to $I_{Lin}/2$. Under these assumptions, Equations (2.14a) and (2.14b) can be rearranged as shown in Equations (2.15a) and (2.15b) respectively,

$$I_o = I_{Lin}(1-D) \quad (2.15a)$$

$$C_o\frac{d\,\tilde{v}_o}{dt} = (1-D)\tilde{i}_a + (1-D)\tilde{i}_b - \frac{I_{Lin}}{2}\tilde{d}_a - \frac{I_{Lin}}{2}\tilde{d}_b - \frac{1}{R_{load}}\tilde{v}_o - \tilde{i}_z \quad (2.15b)$$

where $\tilde{i}_c = C_o\,d\tilde{v}_o/dt$ and $\tilde{i}_o = \tilde{v}_o/R_{load}$. Equation (2.15b) is the differential equation for the converter output voltage. To determine the differential equations for the phase currents, the voltage equations for the circuit loops around each phase may be written as:

$$(V_{in} + \tilde{v}_{in}) = (I_{Lin} + \tilde{i}_{Lin})R_{in} + L_{Lin}\frac{d(I_{Lin} + \tilde{i}_{Lin})}{dt} + L_a\frac{d(I_a + \tilde{i}_a)}{dt} - L_m\frac{d(I_b + \tilde{i}_b)}{dt} - \tilde{d}_aV_o + (V_o + \tilde{v}_o)(1-D_a) \quad (2.16a)$$

$$(V_{in} + \tilde{v}_{in}) = (I_{Lin} + \tilde{i}_{Lin})R_{in} + L_{Lin}\frac{d(I_{Lin} + \tilde{i}_{Lin})}{dt} + L_b\frac{d(I_b + \tilde{i}_b)}{dt} - L_m\frac{d(I_a + \tilde{i}_a)}{dt} - \tilde{d}_bV_o + (V_o + \tilde{v}_o)(1-D_b) \quad (2.16b)$$

By substituting $I_{Lin} + \tilde{i}_{Lin} = (I_a + \tilde{i}_a) + (I_b + \tilde{i}_b)$ and separating the steady-state and the small-signal terms on each side of Equations (2.16a) and (2.16b), Equations (2.17a) to (2.18b) can be found:

$$V_{in} = I_{Lin}R_{in} + V_o(1-D_a) \quad (2.17a)$$

$$\tilde{v}_{in} = (L_{Lin} + L_a)\frac{d\tilde{i}_a}{dt} + (L_{Lin} - L_m)\frac{d\tilde{i}_b}{dt} + R_{in}\tilde{i}_a + R_{in}\tilde{i}_b - V_o\tilde{d}_a + (1-D_a)\tilde{v}_o \quad (2.17b)$$

$$V_{in} = I_{Lin}R_{in} + V_o\left(1 - D_b\right) \tag{2.18a}$$

$$\tilde{v}_{in} = \left(L_{in} + L_b\right)\frac{d\tilde{i}_b}{dt} + \left(L_{in} - L_m\right)\frac{d\tilde{i}_a}{dt} + R_{in}\tilde{i}_a + R_{in}\tilde{i}_b - V_o\tilde{d}_b + \left(1 - D_b\right)\tilde{v}_o \tag{2.18b}$$

Once more, assuming steady-state conditions, $D_a = D_b = D$, Equations (2.17a) and (2.18a) may be written as:

$$V_{in} = I_{Lin}R_{in} + V_o\left(1 - D\right) \tag{2.19}$$

whilst Equations (2.17b) and (2.18b) can be expressed as:

$$\tilde{v}_{in} = \left(L_{Lin} + L_a\right)\frac{d\tilde{i}_a}{dt} + \left(L_{Lin} - L_m\right)\frac{d\tilde{i}_b}{dt} + R_{in}\tilde{i}_a + R_{in}\tilde{i}_b - V_o\tilde{d}_a + \left(1 - D\right)\tilde{v}_o \tag{2.20a}$$

$$\tilde{v}_{in} = \left(L_{in} + L_b\right)\frac{d\tilde{i}_b}{dt} + \left(L_{in} - L_m\right)\frac{d\tilde{i}_a}{dt} + R_{in}\tilde{i}_a + R_{in}\tilde{i}_b - V_o\tilde{d}_b + \left(1 - D\right)\tilde{v}_o \tag{2.20b}$$

From Equation (2.19) the conversion ratio of the converter when the input inductor resistance is included may be derived by substituting Equation (2.15a) into Equation (2.19):

$$\frac{V_o}{V_{in}} = \frac{\left(1 - D\right)}{\left(1 - D\right)^2 + R_{in}/R_{load}} \tag{2.21}$$

It is evident that if the ratio of the input inductor resistance to the load resistance is sufficiently small, in other words $R_{in} << R_{load}$, Equation (2.21) will reduce to Equation (2.1).

Moreover, rearranging Equations (2.20a) and (2.20b) into two first-order differential equations for $\tilde{i}_a$ and $\tilde{i}_b$, yields:

$$\frac{d\tilde{i}_a}{dt} = \frac{V_o(\mathrm{L}_{in}+\mathrm{L}_c)}{L_{Tot}}\tilde{d}_a - \frac{V_o(\mathrm{L}_{in}+\mathrm{L}_c)}{L_{Tot}}\tilde{d}_b - \frac{(1-\mathrm{D})(\mathrm{L}_m+\mathrm{L}_c)}{L_{Tot}}\tilde{v}_o - \frac{R_{in}(\mathrm{L}_m+\mathrm{L}_c)}{L_{Tot}}\tilde{i}_a - \frac{R_{in}(\mathrm{L}_m+\mathrm{L}_c)}{L_{Tot}}\tilde{i}_b \tag{2.22a}$$

$$\frac{d\tilde{i}_b}{dt} = \frac{V_o(\mathrm{L}_{in}+\mathrm{L}_c)}{L_{Tot}}\tilde{d}_b - \frac{V_o(\mathrm{L}_{in}+\mathrm{L}_c)}{L_{Tot}}\tilde{d}_a - \frac{(1-\mathrm{D})(\mathrm{L}_m+\mathrm{L}_c)}{L_{Tot}}\tilde{v}_o - \frac{R_{in}(\mathrm{L}_m+\mathrm{L}_c)}{L_{Tot}}\tilde{i}_a - \frac{R_{in}(\mathrm{L}_m+\mathrm{L}_c)}{L_{Tot}}\tilde{i}_b \tag{2.22b}$$

where $L_{Tot} = 2L_{in}\left(L_c + L_m\right) + \left(L_c^2 - L_m^2\right)$, $L_a = L_b = L_c$ and $\tilde{v}_{in} = 0$. Furthermore V_o can be expressed in terms of V_{in} using the voltage conversion ratio of the converter shown in Equation (2.1) under the assumption that $R_{in} << R_{load}$. Using Equations (2.15), (2.22a) and (2.22b), the small-signal model of the converter can be represented in state-space form as:

$$\dot{\tilde{\mathbf{x}}} = \mathbf{A}_{av}\tilde{\mathbf{x}} + \mathbf{B}_{av}\tilde{\mathbf{u}} \tag{2.23}$$

where the state vector, $\tilde{\mathbf{x}}$, comprises the small-signal components of the phase currents flowing through the IPT windings and the voltage across the output capacitor: $\tilde{\mathbf{x}} = \begin{bmatrix} \tilde{i}_a & \tilde{i}_b & \tilde{v}_o \end{bmatrix}^T$; the input vector, $\tilde{\mathbf{u}}$, contains the control inputs of each phase and the load disturbance current: $\tilde{\mathbf{u}} = \begin{bmatrix} \tilde{d}_a & \tilde{d}_b & \tilde{i}_z \end{bmatrix}^T$. Moreover, if the small ac perturbations of the input voltage are included in the development of the model, the vector $\tilde{\mathbf{u}}$ will contain a fourth variable $\tilde{v}_{in}$. The matrices $\boldsymbol{A_{av}}$ and $\boldsymbol{B_{av}}$ in Equation (2.23) may be expressed by Equations (2.24) and (2.25):

$$\mathbf{A}_{av} = \begin{bmatrix} -\dfrac{R_{in}(L_c+L_m)}{L_{Tot}} & -\dfrac{R_{in}(L_c+L_m)}{L_{Tot}} & -\dfrac{(1-D)(L_c+L_m)}{L_{Tot}} \\ -\dfrac{R_{in}(L_c+L_m)}{L_{Tot}} & -\dfrac{R_{in}(L_c+L_m)}{L_{Tot}} & -\dfrac{(1-D)(L_c+L_m)}{L_{Tot}} \\ \dfrac{(1-D)}{C_o} & \dfrac{(1-D)}{C_o} & -\dfrac{1}{R_{load}C_o} \end{bmatrix} \tag{2.24}$$

$$\mathbf{B}_{av} = \begin{bmatrix} \dfrac{V_{in}(L_{in}+L_c)}{L_{Tot}(1-D)} & -\dfrac{V_{in}(L_{in}-L_m)}{L_{Tot}(1-D)} & 0 \\ -\dfrac{V_{in}(L_{in}-L_m)}{L_{Tot}(1-D)} & \dfrac{V_{in}(L_{in}+L_c)}{L_{Tot}(1-D)} & 0 \\ -\dfrac{V_{in}}{2R_{load}C_o(1-D)^2} & -\dfrac{V_{in}}{2R_{load}C_o(1-D)^2} & \dfrac{1}{C_o} \end{bmatrix} \tag{2.25}$$

By the use of the Laplace-transformation the transfer functions of the state-space model were obtained. These are listed in Table 2.2 and their corresponding algebraic expressions are shown in Table 2.3. The procedure to find the transfer functions was carried out with the assistance of the software Mathematica, which allows the reduction of symbolic algebraic expressions. From the mathematical development of these expressions, it was found that the transfer functions for each of the converter phases are identical,

$$G_{daia}(s) = G_{dbib}(s) \tag{2.26}$$

$$G_{daib}(s) = G_{dbia}(s) \tag{2.27}$$

$$G_{davo}(s) = G_{dbvo}(s) \tag{2.28}$$

$$G_{izia}(s) = G_{izib}(s) \tag{2.29}$$

which is expected as the two phases of the converter are identical. Moreover, the transfer functions $G_{daib}(s)$ and $G_{dbia}(s)$, Equation (2.27), confirm the existence of a cross-coupling between the control input of one phase and the phase-current of its counterpart.

Table 2.2. Transfer functions of the small-signal averaged model of the dual interleaved boost converter with IPT.

	$\tilde{i}_a(s)$	$\tilde{i}_b(s)$	$\tilde{v}_o(s)$
$\tilde{d}_a(s)$	$G_{daia}(s) = \left.\frac{\tilde{i}_a(s)}{\tilde{d}_a(s)}\right\|_{\tilde{d}_b(s)=0;\ \tilde{i}_z(s)=0}$ *Phase-a control-to-phase-a current*	$G_{daib}(s) = \left.\frac{\tilde{i}_b(s)}{\tilde{d}_a(s)}\right\|_{\tilde{d}_b(s)=0;\ \tilde{i}_z(s)=0}$ *Phase-a control-to-phase-b current*	$G_{davo}(s) = \left.\frac{\tilde{v}_o(s)}{\tilde{d}_a(s)}\right\|_{\tilde{d}_b(s)=0;\ \tilde{i}_z(s)=0}$ *Phase-a control-to-output voltage*
$\tilde{d}_b(s)$	$G_{dbia}(s) = \left.\frac{\tilde{i}_a(s)}{\tilde{d}_b(s)}\right\|_{\tilde{d}_a(s)=0;\ \tilde{i}_z(s)=0}$ *Phase-b control-to-phase-a current*	$G_{dbib}(s) = \left.\frac{\tilde{i}_b(s)}{\tilde{d}_b(s)}\right\|_{\tilde{d}_a(s)=0;\ \tilde{i}_z(s)=0}$ *Phase-b control-to-phase-b current*	$G_{dbvo}(s) = \left.\frac{\tilde{v}_o(s)}{\tilde{d}_b(s)}\right\|_{\tilde{d}_a(s)=0;\ \tilde{i}_z(s)=0}$ *Phase-b control-to-output voltage*
$\tilde{i}_z(s)$	$G_{izia}(s) = \left.\frac{\tilde{i}_a(s)}{\tilde{i}_z(s)}\right\|_{\tilde{d}_a(s)=0;\ \tilde{d}_b(s)=0}$ *Disturbance current-to-phase-a current*	$G_{izib}(s) = \left.\frac{\tilde{i}_b(s)}{\tilde{i}_z(s)}\right\|_{\tilde{d}_a(s)=0;\ \tilde{d}_b(s)=0}$ *Disturbance current-to-phase-b current*	$G_{izvo}(s) = \left.\frac{\tilde{v}_o(s)}{\tilde{i}_z(s)}\right\|_{\tilde{d}_a(s)=0;\ \tilde{d}_b(s)=0}$ *Disturbance current-to-output voltage*

In contrast to previous works [6,7], this averaged small-signal model has been developed for the boost converter and takes into consideration the small ac perturbation in each control input independently. This advantage is fully exploited in Chapter 4 where the model of the converter using digital average-current control is introduced, which includes the effects of the interleaved operation of the phases. The following sections will explain in more detail the implementation of the small-signal model in MATLAB and its validation using simulations carried out in SABER.

Table 2.3. Transfer functions of the small-signal averaged model of the dual interleaved boost converter with IPT.

$$G_{daia}(\mathrm{s}) = \mathrm{G}_{dbib}(\mathrm{s}) = \frac{\dfrac{(L_c+L_{\mathrm{in}})V_{\mathrm{in}}}{(1-\mathrm{D})L_{\mathrm{Tot}}}\left(s^2 - \dfrac{\left((3L_c+2L_{\mathrm{in}}+L_m)L_{\mathrm{Tot}}+2C_o(L_c+2L_{\mathrm{in}}-L_m)(L_c+L_m)R_{\mathrm{in}}R_{\mathrm{load}}\right)}{2C_o\ L_{\mathrm{Tot}}R_{\mathrm{load}}(L_c+L_{\mathrm{in}})}s + \dfrac{(L_c+2L_{\mathrm{in}}-L_m)(L_c+L_m)\left(R_{\mathrm{in}}+(1-\mathrm{D})^2R_{\mathrm{load}}\right)}{C_o\ L_{\mathrm{Tot}}R_{\mathrm{load}}(L_c+L_{\mathrm{in}})}\right)}{s\left(s^2 + \dfrac{\left(L_{\mathrm{Tot}}+2C_o(L_c+L_m)R_{\mathrm{in}}R_{\mathrm{load}}\right)}{C_oL_{\mathrm{Tot}}R_{\mathrm{load}}}s + \dfrac{2(L_c+L_m)\left(R_{\mathrm{in}}+(1-\mathrm{D})^2R_{\mathrm{load}}\right)}{C_oL_{\mathrm{Tot}}R_{\mathrm{load}}}\right)}$$

$$G_{dbia}(\mathrm{s}) = G_{daib}(\mathrm{s}) = \frac{-\dfrac{(L_{\mathrm{in}}-L_m)V_{\mathrm{in}}}{(1-\mathrm{D})L_{\mathrm{Tot}}}\left(s^2 - \dfrac{\left((L_c-2L_{\mathrm{in}}+3L_m)L_{\mathrm{Tot}}-2C_o(L_c+2L_{\mathrm{in}}-L_m)(L_c+L_m)R_{\mathrm{in}}R_{\mathrm{load}}\right)}{2C_oL_{\mathrm{Tot}}R_{\mathrm{load}}(L_{\mathrm{in}}-L_m)}s + \dfrac{(L_c+2L_{\mathrm{in}}-L_m)(L_c+L_m)\left(R_{\mathrm{in}}+(1-\mathrm{D})^2R_{\mathrm{load}}\right)}{C_o\ L_{\mathrm{Tot}}R_{\mathrm{load}}(L_{\mathrm{in}}-L_m)}\right)}{s\left(s^2 + \dfrac{\left(L_{\mathrm{Tot}}+2C_o(L_c+L_m)R_{\mathrm{in}}R_{\mathrm{load}}\right)}{C_oL_{\mathrm{Tot}}R_{\mathrm{load}}}s + \dfrac{2(L_c+L_m)\left(R_{\mathrm{in}}+(1-\mathrm{D})^2R_{\mathrm{load}}\right)}{C_oL_{\mathrm{Tot}}R_{\mathrm{load}}}\right)}$$

$$G_{davo}(\mathrm{s}) = G_{dbvo}(\mathrm{s}) = \frac{-\dfrac{V_{\mathrm{in}}}{2C_o(1-\mathrm{D})^2R_{\mathrm{load}}}\left(s^2 - \dfrac{(L_c+L_m)\left(-R_{\mathrm{in}}+(1-\mathrm{D})^2R_{\mathrm{load}}\right)}{L_{\mathrm{Tot}}}s - \dfrac{(L_c+L_m)^2\left((1-\mathrm{D})^2-R_{\mathrm{in}}^2\right)}{2\ L_{\mathrm{Tot}}^2}\right)}{s\left(s^2 + \dfrac{\left(L_{\mathrm{Tot}}+2C_o(L_c+L_m)R_{\mathrm{in}}R_{\mathrm{load}}\right)}{C_oL_{\mathrm{Tot}}R_{\mathrm{load}}}s + \dfrac{2(L_c+L_m)\left(R_{\mathrm{in}}+(1-\mathrm{D})^2R_{\mathrm{load}}\right)}{C_oL_{\mathrm{Tot}}R_{\mathrm{load}}}\right)}$$

$$G_{izia}(\mathrm{s}) = G_{izib}(\mathrm{s}) = -\frac{(1-\mathrm{D})(L_c+L_m)}{C_oL_{\mathrm{Tot}}\left(s^2 + \dfrac{\left(L_{\mathrm{Tot}}+2C_o(L_c+L_m)R_{\mathrm{in}}R_{\mathrm{load}}\right)}{C_oL_{\mathrm{Tot}}R_{\mathrm{load}}}s + \dfrac{2(L_c+L_m)\left(R_{\mathrm{in}}+(1-\mathrm{D})^2R_{\mathrm{load}}\right)}{C_oL_{\mathrm{Tot}}R_{\mathrm{load}}}\right)}$$

$$G_{izvo}(\mathrm{s}) = \frac{\left(s^2 + \dfrac{2(L_c+L_m)R_{\mathrm{in}}}{L_{\mathrm{Tot}}}s - \dfrac{(L_c+L_m)^2\left((1-\mathrm{D})^2-R_{\mathrm{in}}^2\right)}{L_{\mathrm{Tot}}^2}\right)}{C_o\left(s^2 + \dfrac{\left(L_{\mathrm{Tot}}+2C_o(L_c+L_m)R_{\mathrm{in}}R_{\mathrm{load}}\right)}{C_oL_{\mathrm{Tot}}R_{\mathrm{load}}}s + \dfrac{2(L_c+L_m)\left(R_{\mathrm{in}}+(1-\mathrm{D})^2R_{\mathrm{load}}\right)}{C_oL_{\mathrm{Tot}}R_{\mathrm{load}}}\right)}$$

2.4. Simulation models of the converter

2.4.1. MATLAB/Simulink averaged small-signal ac model

The implementation of the small-signal ac model of the DIBC has two main sections: a script developed in MATLAB and a block diagram developed in Simulink. The script allows the user to set up the model parameters such as input voltage, quiescent duty-ratio, values of the converter passive elements and quiescent values of the state-variables.

This information was then used to calculate a numerical representation of the state-space matrices of the system. This script can be found in Appendix B.1. The data generated by the script was then employed in Simulink using the block diagram illustrated in Figure 2.7 to solve the system and plot its transient response. Finally, an additional script was generated in MATLAB to export the data obtained in Simulink and to compare it against the simulation results obtained with SABER.

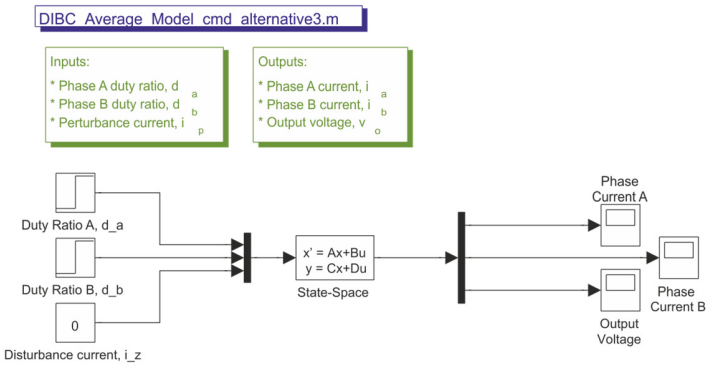

Figure 2.7. MATLAB/Simulink small-signal ac model.

2.4.2. SABER switched model

This model was created to verify the correct operation of the converter and as the first stage of a more complex model which incorporates the digital current control. Figure 2.8 depicts the schematic diagram of the dual interleaved boost converter with IPT developed in SABER. In this diagram all the elements employed are standard SABER models provided with the simulation software. The circuit is divided into two sections.

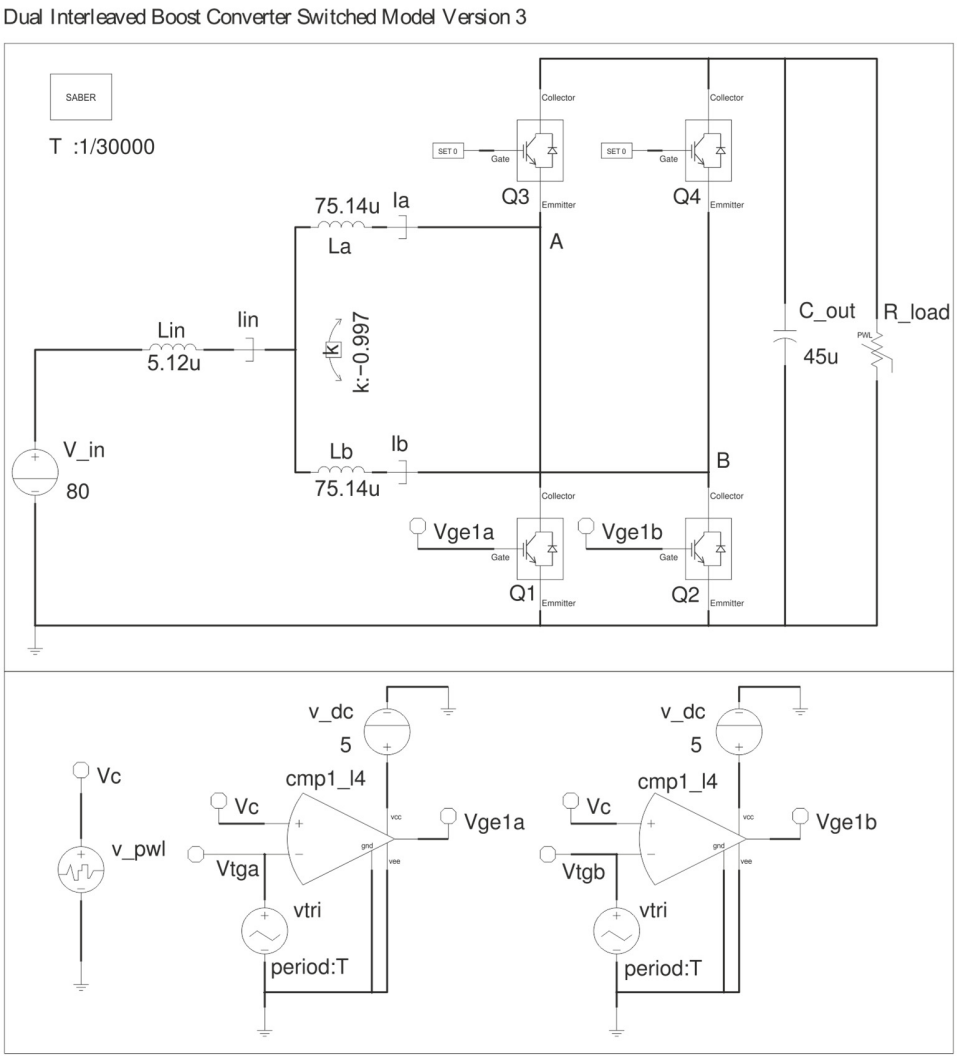

Figure 2.8. SABER switched model of the dual interleaved boost converter with IPT.

The first section includes the power circuit components. An ideal dc voltage source is used to power the low-voltage side of the converter. Two ideal capacitors are employed at the low-voltage and high-voltage ends of the converter with no equivalent series resistance. The input inductor is modelled by an ideal inductor with inductance of *5.12 µH* and an equivalent series resistance equal to *29 mΩ*. The IPT windings were modelled using coupled inductors where, in SABER, the coupling coefficient between two target inductors can be set. The attributes of these elements are *75.14 µH* for the self-inductance of the coupled inductors and *0.997* for the coupling coefficient. The values of these elements were obtained from a prototype of the converter, which is introduced in Section 3.2, Chapter 3.

Finally, the devices that comprise the switching legs consist of a simple switch connected in anti-parallel with a piecewise linear diode. The switch model is controlled by a digital gate-signal that toggles the device on and off. The on-resistance, turn-on and turn-off rise times of the device can be selected by the user. In this particular application *0.1 μΩ*, *10 ns* and *10 ns* were used for these properties respectively. These values were set to be very small to prevent switch related losses from affecting the correspondence between the simulation and the small-signal model and to reproduce ideal conditions. Additionally, a digital buffer is employed to drive the switch gate signal. By means of this buffer the propagation delay generated by the gate-drivers and the IGBT's turn-on and turn-off delays in the practical circuit are modelled. The delay set in this buffer equals *520 ns* and it corresponds to the practical value measured from the converter prototype in Section 3.6.3, Chapter 3.

The piecewise linear diode is modelled by a very high-resistance when the device is reverse-biased emulating an open circuit. Conversely, when the device is forward-biased the resistance between its terminals drops to the user specified value. The value employed for the simulations was *0.1 μΩ*. No forward voltage drop was considered in this model.

The second section of the diagram contains the PWM generators used to provide the driving signals for the bottom transistors in the converter legs. Each generator comprises an analogue comparator, a *5 V* dc voltage source and a voltage waveform generator. The waveform generators connected to the inverting input of the comparators were programmed to produce trailing-edged saw-tooth carrier waveforms with identical amplitude and frequency, but phase-shifted from each other by *180 degrees*. The non-inverting inputs of the comparators are supplied with the modulating signal. This signal is produced by an additional dc voltage source which is common to the two phases.

2.4.3. SABER averaged model

The SABER averaged model, depicted in Figure 2.9, was created to provide further validation for the small-signal ac model of the converter developed in Section 2.2. This model, unlike the switched model, has no ripple in the current waveforms allowing the average values of the waveforms to be compared directly by superimposing the results.

The schematic shares practically the same structure as the one depicted in Figure 2.8, but unlike the switched model, the switch networks of each boost cell have been replaced with an averaged PWM switch network, which is available in the component library of SABER. The duty ratio of each averaged PWM switch network is controlled by two dc voltage sources located at the bottom of the schematic. Whilst being similar to the

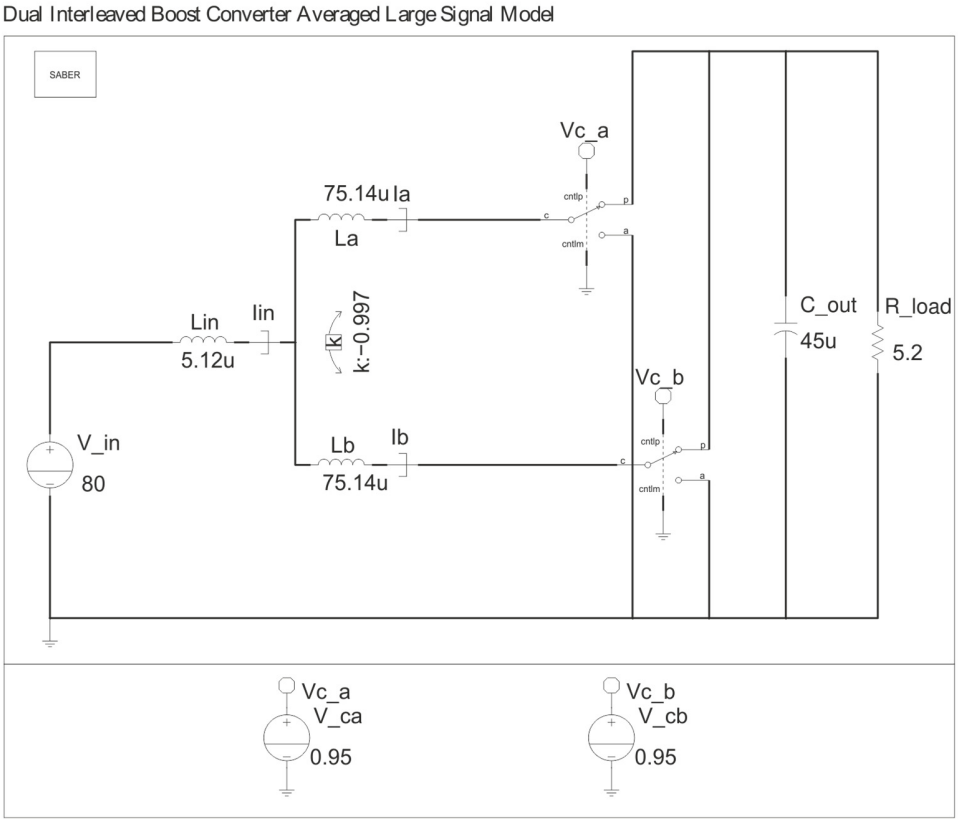

Figure 2.9. SABER averaged large-signal model of the dual interleaved boost converter with IPT.

averaged switch modelling described in Section 2.3.1, no linearization or removal of steady-state components has been undertaken.

2.5. Simulation results

The simulation results obtained using the SABER switched model, SABER average model and the small-signal model of the converter are presented in this section. The parameters of the converter employed for these simulations are listed in Table 2.4 and they were obtained from a prototype of the converter which is described in Chapter 3. The

results are organized in two sections. The first section will demonstrate the operation of the SABER switched model and SABER averaged model in CCM. For this purpose three steady-state operating points are examined.

Table 2.4. Simulation parameters for the validation of the small-signal model of the DIBC with IPT.

Parameter	Value
Input inductance at 60 kHz, L_{in}	*5.12 µH*
Input inductor stray resistance, R_{Lin}	*29 mΩ*
IPT windings self-inductance at 30kHz, L_a, L_b	*75.14 µH*
Coupling coefficient of the IPT windings, k	*0.997*
Output capacitance, C_o	*45 µF*
Load Resistance, R_{load}	*5.2 Ω*

The second section will be used to validate the small-signal ac model implemented in MATLAB. To this end, the step response and the response to small-sinusoidal perturbations are compared against those obtained using the models developed in SABER.

2.5.1. Verification of the SABER switched and SABER averaged simulation models

The simulation results of the SABER switched model and the SABER averaged model introduced in Sections 2.4.2 and 2.4.3 are shown in Figures 2.10, 2.11 and 2.12. These results depict the steady-state waveforms of the converter for the operating points *D = 0.25*, *D = 0.5* and *D = 0.75* respectively, using an input voltage of *80 V* and a load resistance of *5.2 Ω*. The waveforms of both simulation models are displayed on top of each other and in the same order as the theoretical waveforms sketched in Figure 2.2, Section 2.2. In addition, the theoretical voltage and current levels as well as the ripple magnitudes were calculated for all the operating points shown using Equations (2.1) to (2.4) and those listed in Table 2.1. The results of these calculations together with the measurements on the simulation waveforms are summarized in Table 2.5 for the purpose of comparison.

The first graph in Figures 2.10, 2.11 and 2.12 displays the transistor driving signals $v_{ge1a}(t)$ and $v_{ge1b}(t)$. The duty-ratio of these waveforms was measured to ensure that the SABER switched model was at the desired operating point. As seen in Figures 2.10, 2.11 and 2.12, the rest of the converter waveforms are delayed with respect to the driving signals

due to the propagation delay introduced in the ideal switch to model the turn-on and turn-off delay of the IGBTs and gate-drivers.

Table 2.5. Comparison of the theoretical and simulation waveforms for *D = 0.25*, *D = 0.5* and *D = 0.75*.

Parameter	Theoretical			SABER switched model		
	D=0.25	***D = 0.5***	***D = 0.75***	***D= 0.25***	***D = 0.5***	***D = 0.75***
Input inductor voltage amplitude $V_{Lin(pkpk)}$ [V]	*53.3*	*0*	*160*	*53.4*	*0*	*160*
Differential peak to peak voltage $V_{diff(pkpk)}$ [V]	*213.3*	*320*	*640*	*213.9*	*320.6*	*650*
Average input current I_{Lin} [A]	*27.3*	*61.5*	*246.1*	*26.9*	*61.6*	*250*
Input current ripple ΔI_{Lin} [A]	*43.4*	*0*	*130.2*	*43*	*0*	*130*
Differential current ripple ΔI_{diff} [A]	*2.9*	*8.8*	*8.8*	*2.9*	*8.8*	*8.9*
Phase current large-ripple ΔI_{alrg}, ΔI_{blrg} [A]	*24.6*	*8.8*	*73.9*	*24*	*9*	*73*
Average output voltage V_o [V]	*106.6*	*160*	*320*	*110*	*160*	*320*

In the second graph $v_{Lin}(t)$ is displayed. The shape of the SABER switched model waveform exhibits the voltage levels expected from Figure 2.2. However, in contrast to the theoretical estimation, the lowest voltage level of $v_{Lin}(t)$ is not constant for *D = 0.25* and *D = 0.75* as the ripple of the output voltage is reflected in this waveform. For the particular case when *D = 0.5*, the $v_{Lin}(t)$ waveform is not completely smooth as expected. This was attributed to the switching delays in the device models resulting in slightly different switching instants in the two legs.

The third to the seventh graphs in Figures 2.10, 2.11 and 2.12 depict the differential voltage, $v_{diff}(t)$, the input inductor current $i_{Lin}(t)$, the differential current, $i_{diff}(t)$, and the phase-currents, $i_a(t)$ and $i_b(t)$, respectively. The shapes of the SABER switched model results for all these waveforms are in agreement with the theoretical ones, Figure 2.2. Moreover, the amplitude and average values measured from the simulation results match the

theoretical values calculated, Table 2.5. Here the SABER averaged model presents discrepancies in the average values of the waveforms $i_{Lin}(t)$, $i_a(t)$ and $i_b(t)$ in contrast to the switched model. These discrepancies are more evident at $D = 0.75$ and the relative error between the SABER averaged model and the SABER switched model and was found to be 1.2% for the phase currents and 0.6% for the input inductor current. These slight differences in the current were attributed to the differences in the circuit parameters, for example, the switch characteristics which are not taken into account in the averaged model.

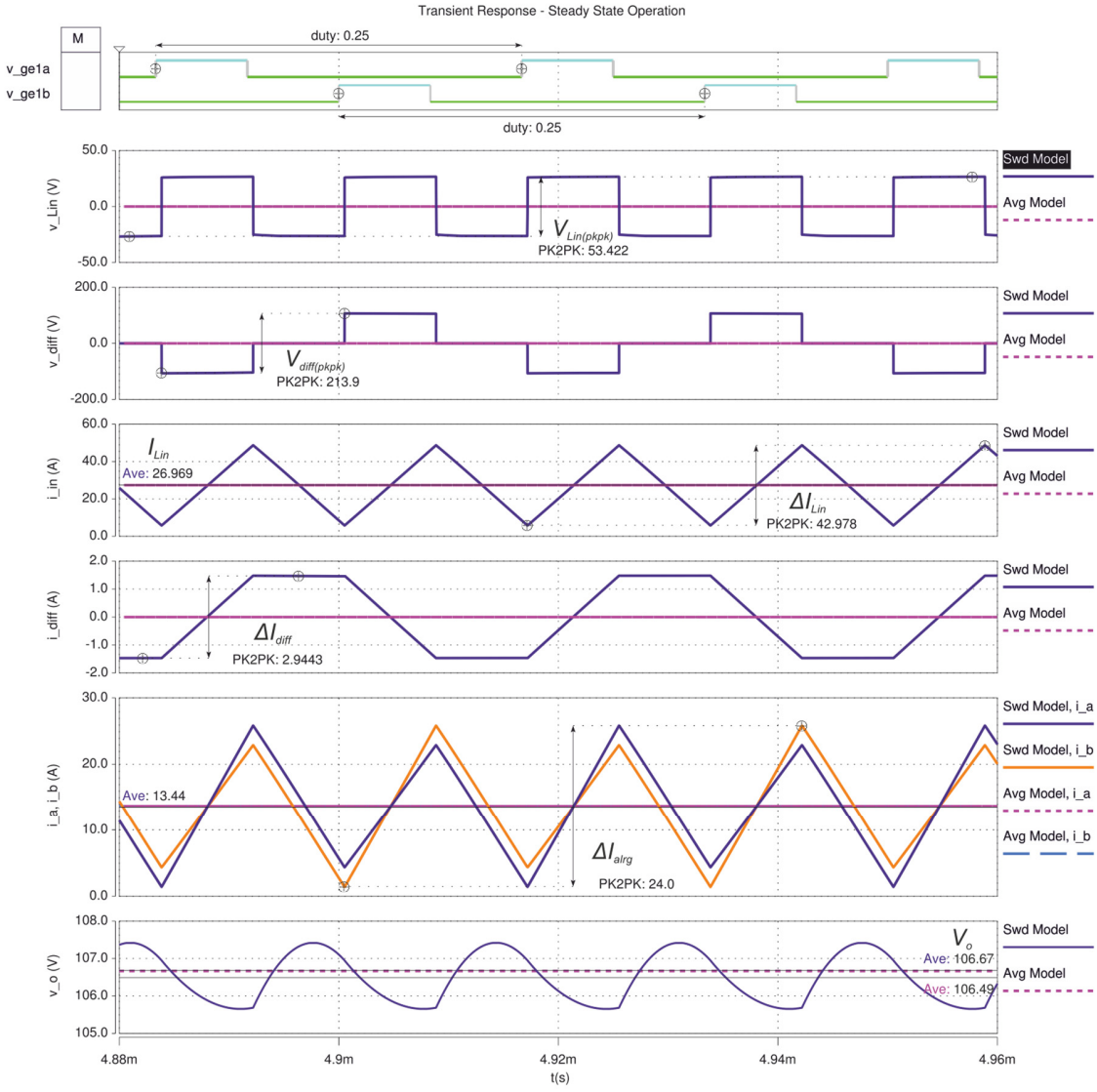

Figure 2.10. Steady state simulation results of the open loop switched model and the average model developed in SABER. *D = 0.25; V_{in} = 80 V; R_{Load} = 5.2 Ω.*

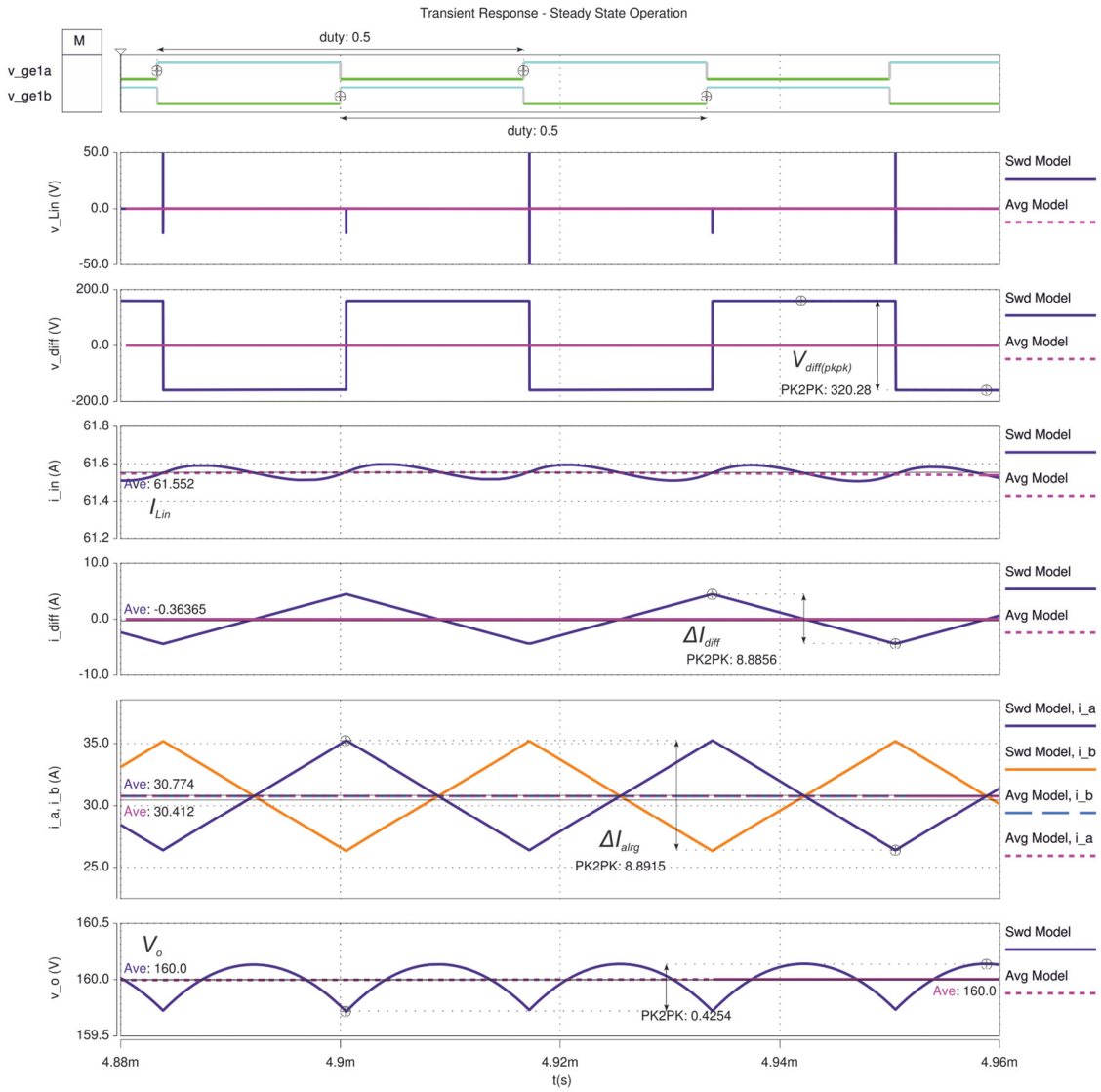

Figure 2.11. Steady state simulation results of the open loop switched model and the average model developed in SABER. *D = 0.5; V_{in} = 80 V; R_{Load} = 5.2 Ω.*

In conclusion, the SABER switched model operates correctly according to the theoretical analysis of the converter carried out in Section 2.2. Moreover, the SABER averaged model provides an accurate prediction of the average value of the waveforms.

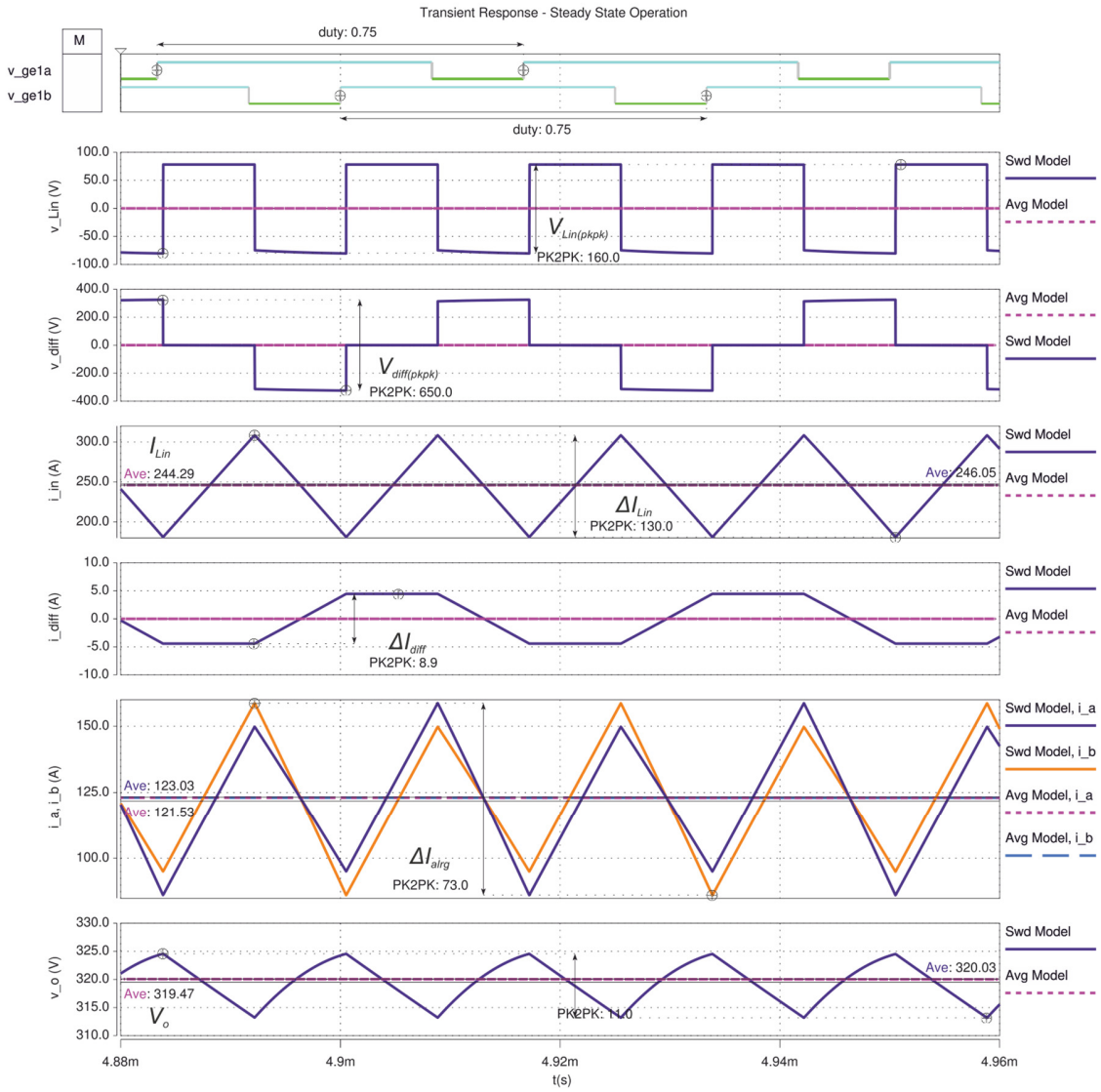

Figure 2.12. Steady state simulation results of the open loop switched model and the average model developed in SABER. *D = 0.75; V_{in} = 80 V; R_{Load} = 5.2 Ω.*

2.5.2. Validation of the small-signal ac model

In this section, the step response and the response to small sinusoidal perturbations of the small-signal model developed in Section 2.2 are compared against those obtained using the SABER averaged model and the SABER switched model.

2.5.2.1. Dynamic response

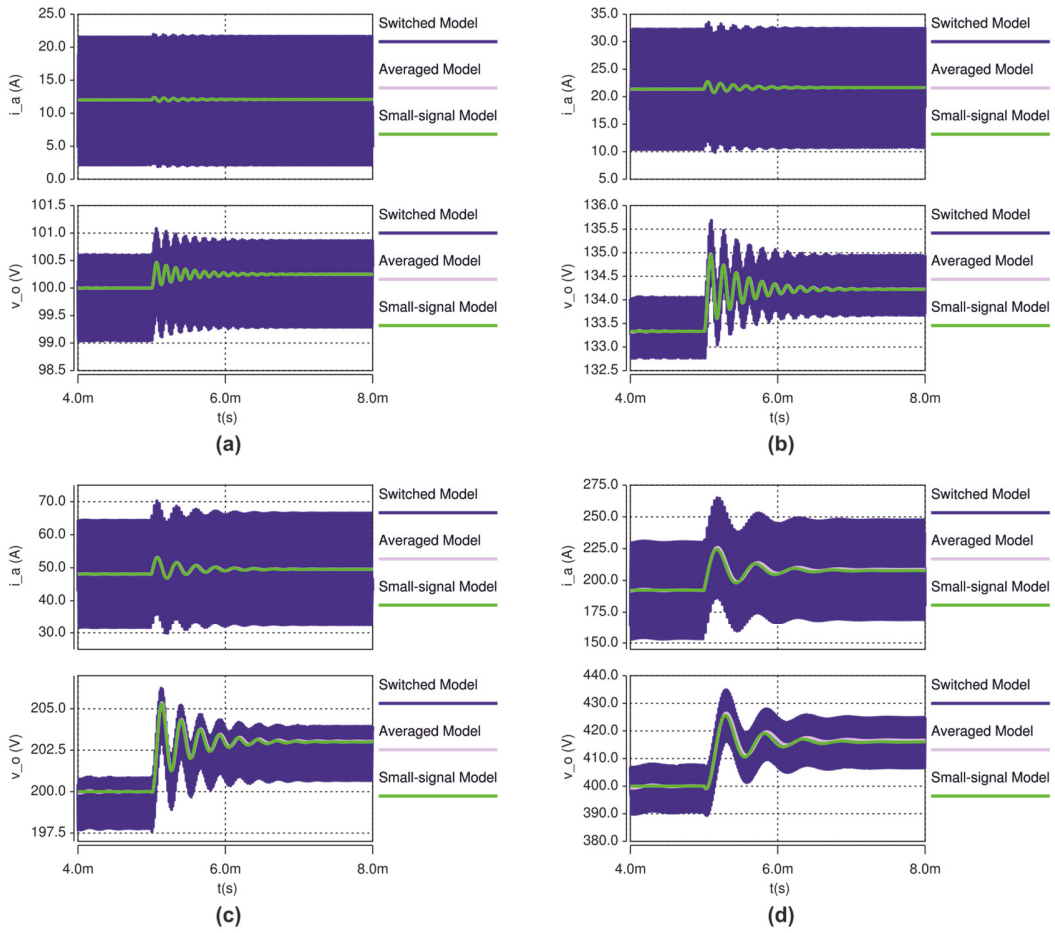

Figure 2.13. Transient response of the converter models for a synchronous 1% step increment in the duty ratio of both phases. *V_{in} = 80 V; R_{load} = 5.2 Ω.* (a) *$D_a = D_b = 0.2$;* (b) *$D_a = D_b = 0.4$;* (c) *$D_a = D_b = 0.6$; (d) $D_a = D_b = 0.8$.*

The transient response of the converter phase-currents and output voltage to a 1%, 3% and 5% step increment in the duty-ratio are illustrated in Figures 2.13, 2.14 and 2.15 respectively. The step increment was performed simultaneously at the control inputs at *t = 5 ms*. In these Figures the simulation results of the SABER switched model, the SABER

averaged model and the small-signal model are superimposed. The Figures are subdivided into four plots showing the response at different operating points. The operating points included are (a) *D= 0.2*, (b) *D = 0.4*, (c) *D = 0.6* and (d) *D = 0.8*. The switching frequency was *30 kHz.* The waveforms included on each plot are the phase-a current, $i_a(t)$, and the output voltage, $v_o(t)$. The phase-b current, $i_b(t)$, is not included since its behaviour is exactly the same as $i_a(t)$ for this particular case where both duty ratios are excited synchronously and with the same amplitude.

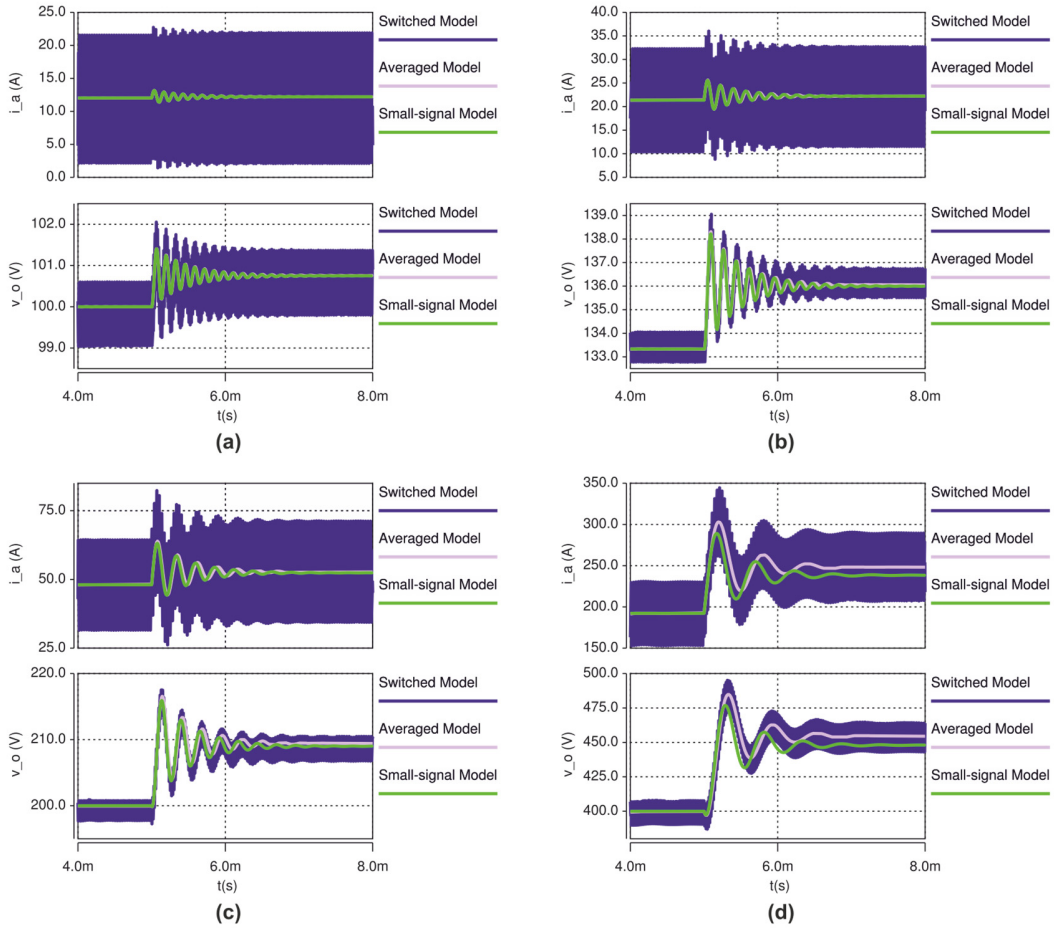

Figure 2.14. Transient response of the converter models for a synchronous 3% step increment in the duty ratio of both phases. *V_{in} = 80 V; R_{load} = 5.2 Ω.* (a) *$D_a = D_b = 0.2$;* (b) *$D_a = D_b = 0.4$;* (c) *$D_a = D_b = 0.6$; (d) $D_a = D_b = 0.8$.*

As seen in the graphs, the results show that the waveforms of the SABER averaged model follow closely the oscillation envelope of the switched model waveforms for any condition or step increment. At the same time, the small signal model shows an acceptable

accuracy with the 1% step for all the operating points examined, Figure 2.13. However, the small-signal model fails to predict accurately the current and voltages for the 3% and 5% step increments with *D* above *0.5*, Figures 2.14(c), 2.14(d), 2.15(c) and 2.15(d). This is expected, as larger disturbances take the model away from the steady-state operating point, where the assumptions of the linearization process become less accurate.

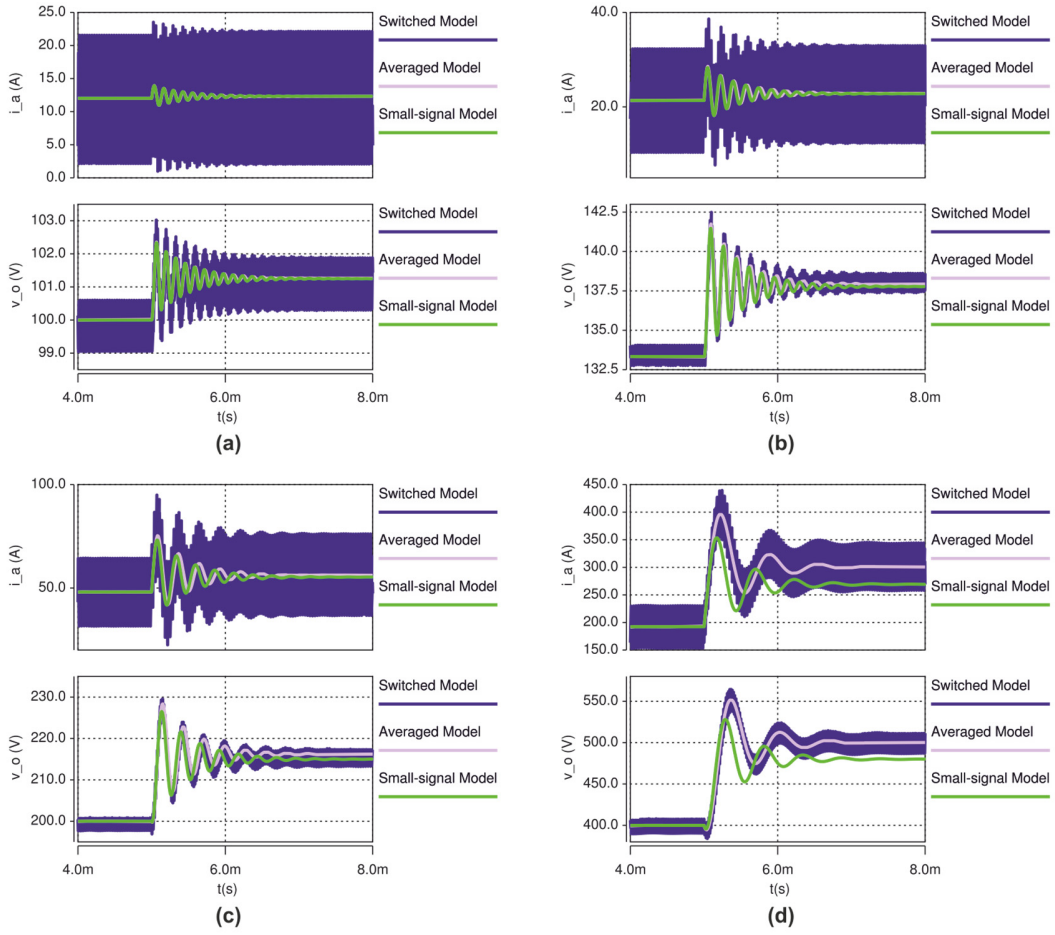

Figure 2.15. Transient response of the converter models for a synchronous 5% step increment in the duty ratio of both phases. *V_{in} = 80 V; R_{load} = 5.2 Ω*. (a) *$D_a = D_b = 0.2$*; (b) *$D_a = D_b = 0.4$*; (c) *$D_a = D_b = 0.6$*; *(d) $D_a = D_b = 0.8$.*

In order to quantify the accuracy of the small-signal model, the final average-value of $i_a(t)$ and $v_o(t)$ after the step-increment was measured and the relative error between the small-signal model and the average-values of the SABER switched model were calculated. The relative errors calculated for *D* ranging from *0.1* to *0.9* are summarized in the graphs shown in Figure 2.16. As seen from these graphs, the small-signal model has a maximum error of 1% for $v_o(t)$ and 2.5% for $i_a(t)$ when the system undergoes a 1% step-increment in

the duty-ratio. Furthermore, the maximum relative error for 3% and 5% step-increments in the duty-ratio is found to go well beyond 5% for values of D above 0.7, but remain less than 10% for duty-ratios up to 0.8.

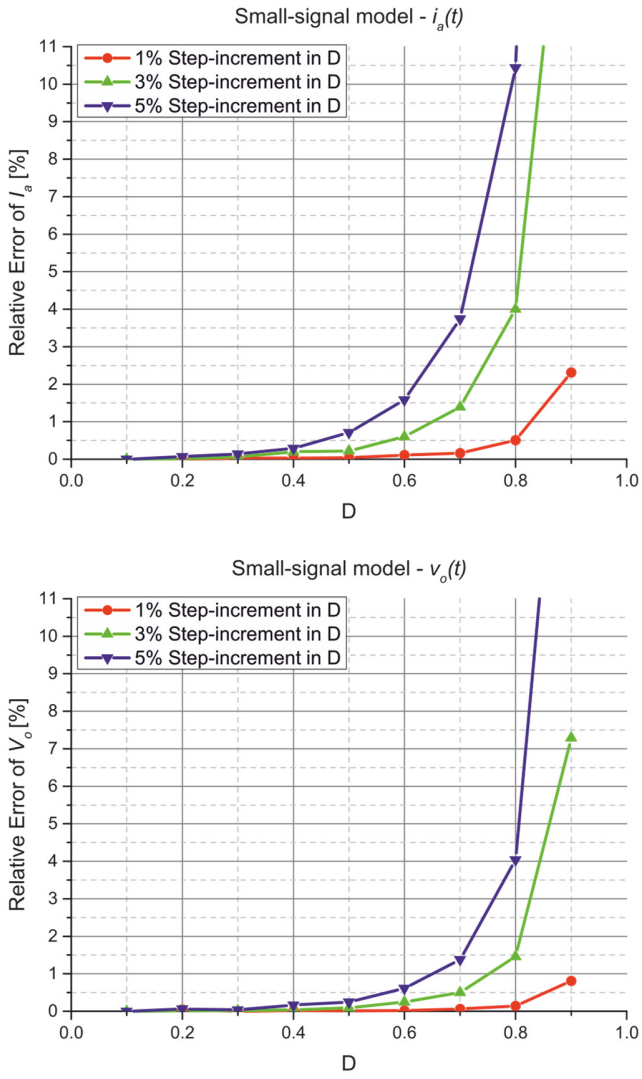

Figure 2.16. Relative error of the final average-value of $i_a(t)$ and $v_o(t)$ predicted by the small-signal averaged model after a small step-increment in the duty-ratio. The relative error was calculated with respect to the value predicted by the SABER switched model.

2.5.2.2. Response to small-sinusoidal perturbations

This section presents the results of small sinusoidal perturbations in the averaged small-signal model implemented in MATLAB and the SABER averaged model. The results of this analysis are superimposed in the plots of Figure 2.17 verifying the validity of the small-

signal ac model. The following paragraphs will explain the methodology employed to plot these results and how they are organized.

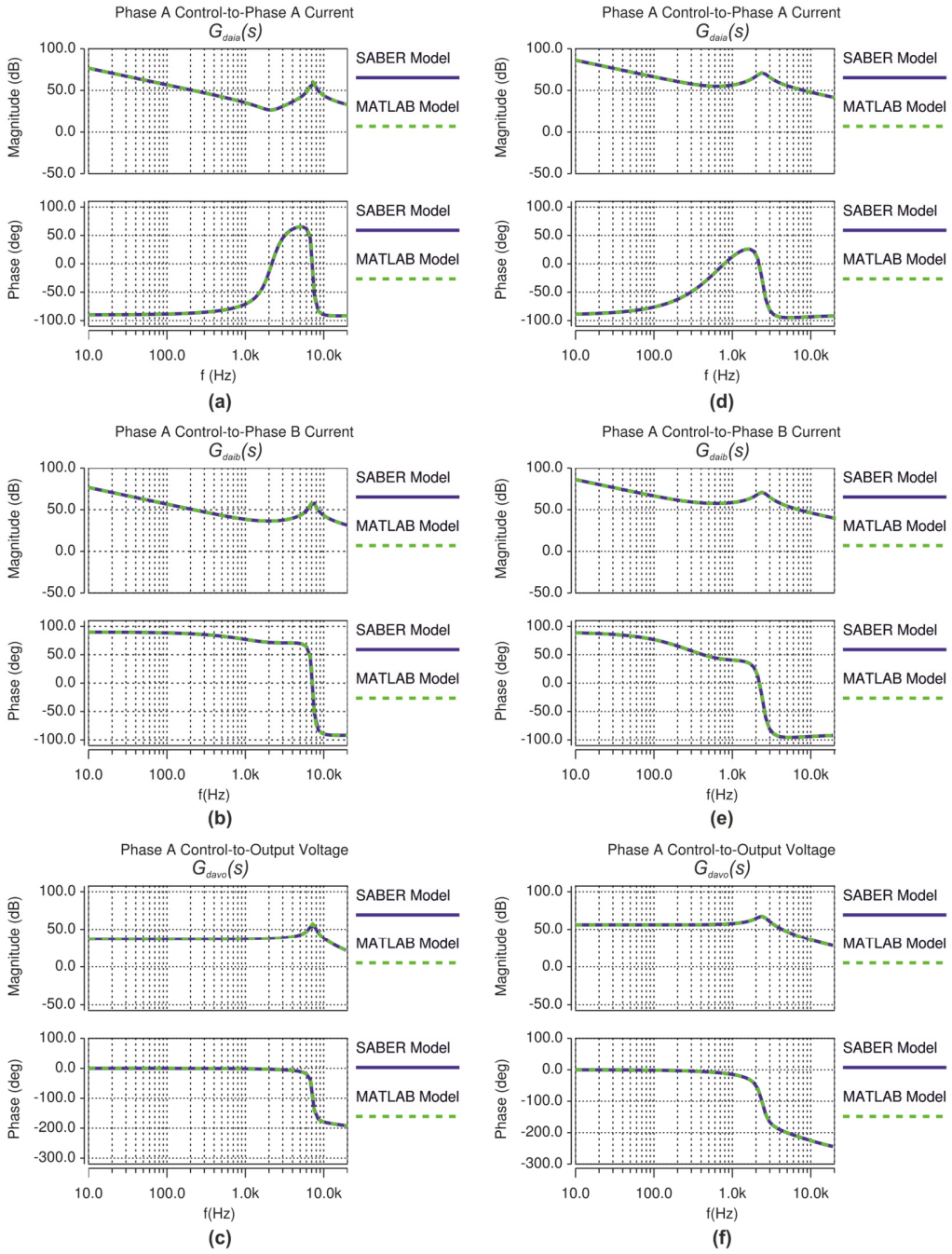

Figure 2.17. Magnitude and phase response of the small-signal averaged model and the SABER averaged model to small-sinusoidal perturbations in the duty-ratio. (a),(b)&(c) *D = 0.25; (d),(e)&(f) D = 0.75. V_{in} = 80 V, R_{load} =5.2 Ω.*

The numerical state-space representation of the small-signal model of the converter was found using the MATLAB script developed in Section 2.4.1. This MATLAB script was

extended to compute the transfer functions in the Laplace-domain. For this study only the transfer functions relating the control inputs, $\tilde{d}_a(s)$ and $\tilde{d}_b(s)$, to the states of the system, $\tilde{i}_a(s)$, $\tilde{i}_b(s)$ and $\tilde{v}_o(s)$ were computed. These six transfer functions are denoted $G_{daia}(s)$, $G_{dbib}(s)$, $G_{daib}(s)$, $G_{dbia}(s)$, $G_{davo}(s)$ and $G_{dbvo}(s)$ and it was demonstrated in Section 2.3 that they reduce to only three transfer functions as $G_{daia}(s) = G_{dbib}(s)$, $G_{daib}(s) = G_{dbia}(s)$, $G_{davo}(s) = G_{dbvo}(s)$. Finally, the magnitude and phase response of these transfer functions to small sinusoidal perturbations were plotted using MATLAB.

The response to small sinusoidal perturbations of the SABER averaged model was obtained employing the small-signal ac analysis tool included with the software. Prior to the small-signal ac analysis, a DC analysis on the circuit was run to obtain the quiescent operating point of all the variables. The data collected was then used to calculate the small-signal response due to the variations at the control input of phase-a. The rest of the system inputs were set to zero.

Figure 2.17(a), 2.17(b) and 2.17(c) depict the frequency responses of transfer functions $G_{daia}(s)$, $G_{daib}(s)$ and $G_{davo}(s)$ respectively, for the operating point $D = 0.25$. The data collected from both models is superimposed in the graphs shown where the results of the SABER averaged model and the small-signal model are plotted with a solid and a dashed line respectively. Likewise, Figures 2.17(d), 2.17(e) and 2.17(f) illustrate the same plots for the operating point $D = 0.75$. The results plotted show that the frequency responses of the SABER averaged model and the small-signal transfer functions have virtually no difference, confirming the validity of the state-space representation of the small-signal model.

2.6. Digital current control with uniformly-sampled PWM for the dual interleaved boost converter with IPT

In this section the implementation of the digital current control with uniformly sampled PWM [8-10], will be analysed for its use in the dual interleaved boost converter with IPT. The principles of this strategy are reviewed in detail in Chapter 1, Section 1.3.2.1.

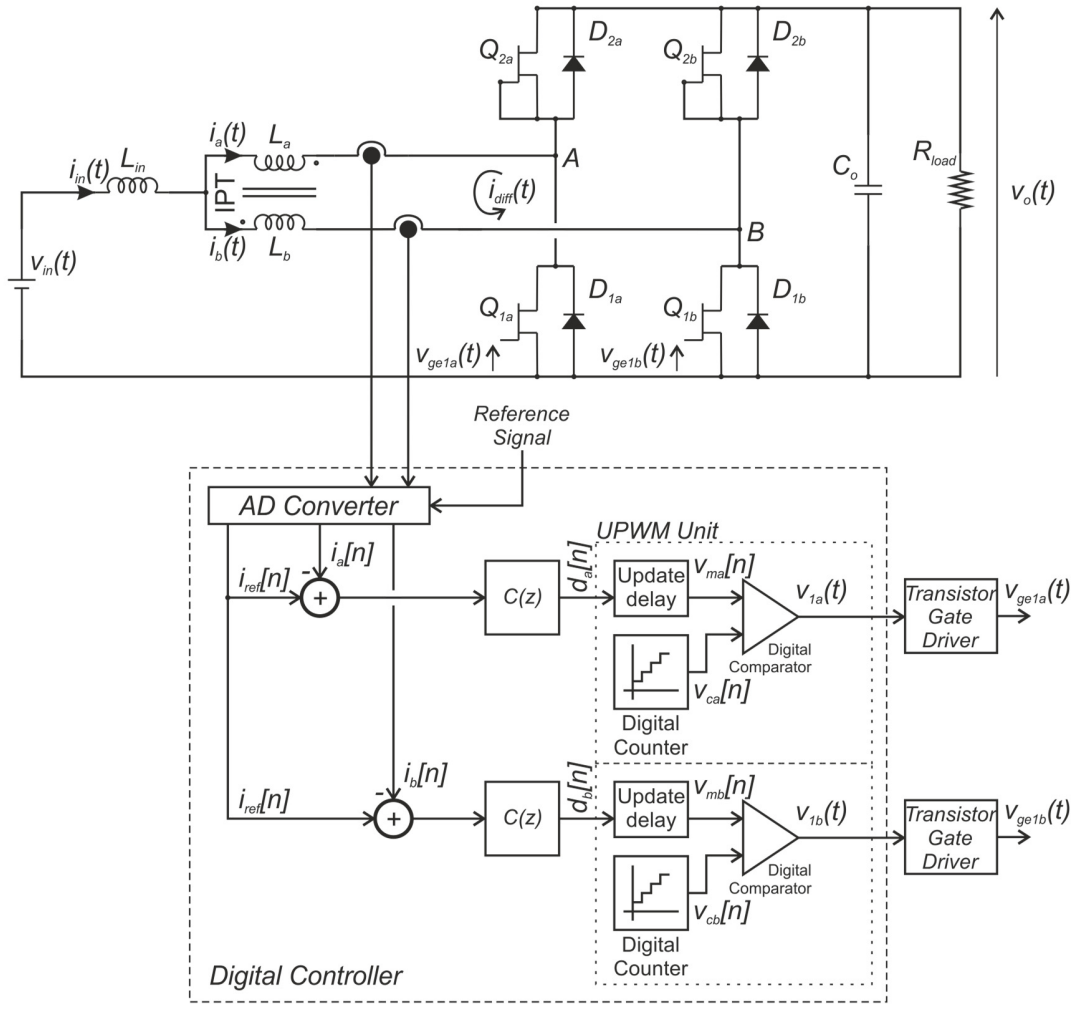

Figure 2.18. Functional block diagram of the digital current control with UPWM for the dual interleaved boost converter with IPT.

Figure 2.18 shows a schematic diagram of the converter with uniformly-sampled PWM. The diagram is divided in two sections. The top part illustrates the power-circuit whilst the bottom section depicts the current feedback loop implemented using a digital controller. The diagram is simplified by omitting the signal conditioning stages that would be needed in a practical system.

The digital controller regulates the current flowing through each phase of the converter using two individual current feedback loops operated in an interleaved manner. As the individual control loops share the same reference input, this topology ensures an equal distribution of the input current between the IPT windings. The PWM waveforms generated by the controller pass through gate-drivers to the converter transistors.

The digital controller comprises two Digital Pulse-Width Modulators, DPWMs, and an Analogue-to-Digital Converter, ADC. The DPWM modules operate in a similar way as their analogue counter-part: a digital counter, which is analogous to a carrier waveform, is constantly compared against a reference-register by means of a digital comparator. The reference-register stores the value of the desired duty-ratio and is analogous to the modulating waveform of the analogue PWM.

When the digital counter crosses the value contained in the reference-register, the output of the comparator is toggled high or low depending on its configuration. Furthermore, the comparator can be configured to toggle its output state whenever its digital counter reaches either maximum or minimum count. The digital counters of each DPWM are phase-shifted by *180 degrees*, thereby generating phase-shifted PWM waveforms. The ADC sampling is linked to the operation of the DPWM counters and can be requested whenever they are either at their maximum or at their minimum count.

The operation of the digital control loops will be explained with the aid of the diagram of Figure 2.18 and the waveforms depicted in Figure 2.19. The waveforms of Figure 2.19 were sketched for the particular case where the DPWM counters operate in up-count mode and are reset to zero every time they reach their maximum value, V_{cmax}, which is known as leading-edge modulation. These waveforms are valid for any $D < 0.5$ when the converter is in CCM only, and illustrate non-periodic waveforms to show the repercussion that slight variations on the duty-ratio have on the currents of each phase.

The first plot in the waveforms shows the instantaneous phase currents $i_a(t)$ and $i_b(t)$ in solid and dashed lines respectively. The second plot shows, the reference-register waveform, $v_{ma}(t)$, and the counter waveform, $v_{ca}(t)$, of the phase-a DPWM module. The third plot shows the reference-register waveform, $v_{mb}(t)$, and the counter waveform, $v_{cb}(t)$. The fourth plot shows the sampling instants of the phase-a and the phase-b current waveforms. Finally, the last graph shows the PWM waveforms at the output of the DPWM modules, $v_{1a}(t)$ and $v_{1b}(t)$, in solid and dashed lines respectively. It is important to point out that in these illustrations even though $v_{ca}(t)$ and $v_{cb}(t)$ are generated by a digital counter, they are sketched as continuous instead of stepped waveforms.

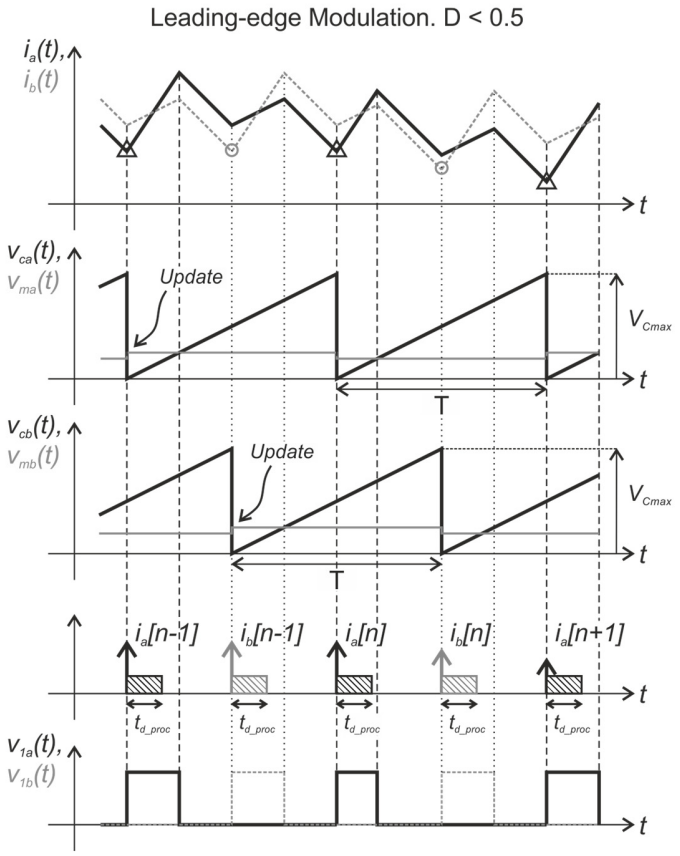

Figure 2.19. Waveforms of the digital current control with uniformly-sampled pulse-width modulation from the dual interleaved boost converter with IPT. Leading-edge modulation strategy. Valid for CCM and $D \leq 0.5$.

At the beginning of Figure 2.19 the phase-a DPWM counter is set to zero. At this instant three events take place: $v_{1a}(t)$ is set on, $v_{ma}(t)$ is updated and $i_a[n-1]$ and $i_{ref}[n-1]$ are acquired by sampling $i_a(t)$. The waveforms show that the sample $i_a[n-1]$ corresponds to the minimum-current or the valley-current. Meanwhile the phase-b DPWM counter, $v_{cb}(t)$, is increasing, as it is phase-shifted *180 degrees* with respect to the phase-a DPWM counter.

Immediately after $i_a(t)$ is sampled, the CPU of the controller compares $i_a[n-1]$ against $i_{ref}[n-1]$ to calculate the error, $i_{ea}[n-1]$, which is then fed into a digital controller, $C(z)$, to re-calculate the new duty-ratio, $d_a[n]$. This process is illustrated in Figure 2.18 in block diagram form and the length of time that the CPU dedicates to it will be referred to as the processing delay, t_{d_proc}. t_{d_proc} is illustrated in Figure 2.19 just after the sampling instants $i_a[n-1]$. The DPWM reference-register will not be updated with $d_a[n]$ until the beginning of the next cycle, therefore $v_{ma}(t)$ will be constant for the rest of the cycle.

At the same time as the CPU handles the sampled current of phase-a, $v_{ca}(t)$ will continue increasing until it equals $v_{ma}(t)$. At this moment $v_{1a}(t)$ will be turned off until the beginning of the next switching cycle where the DPWM counter of phase-a is reset. This process is completely independent from the CPU of the digital controller as it is carried out in the DPWM module, leaving the CPU free of tasks. The phase-b process is identical but is delayed behind phase-a by half a switching cycle $T/2$.

The waveforms show that the leading-edge modulation strategy results in the regulation of the valley-current. Secondly, as the processing of the sampled currents of both phases is shared by the same CPU, t_{d_proc} cannot be longer than half of a switching period, in other words $t_{d\_proc} \leq T/2$. Finally, since the calculated duty-ratio is held and not updated until the beginning of the next switching-cycle, a delay of a sampling period will always be present in the control response.

To overcome some of the limitations of the leading-edge modulation strategy, the following section reviews two other alternative approaches.

2.6.1. Analysis of the leading-edge, trailing-edge and triangular carrier modulations for the DIBC with IPT

Figure 2.20 depicts the principal waveforms for the three different current sampling schemes of the dual interleaved boost converter with IPT. The waveforms were sketched assuming instantaneous operation of the components, are valid for the converter operating in CCM and illustrate non-periodic waveforms to show the repercussion that slight variations on the duty-ratio have on the currents of each phase. The graphs are arranged in two groups. Figures 2.20(a), 2.20(c) and 2.20(e) are valid for $D \leq 0.5$. They illustrate the main waveforms of leading-edge modulation (as in Figure 2.19), trailing-edge modulation, and triangular-carrier modulation with symmetric on-time respectively. Likewise, Figures 2.20(b), 2.20(d) and 2.20(f) depict the waveforms of these modulation schemes for $D > 0.5$.

Each figure is arranged in a similar way to Figure 2.19. The first graph shows the currents $i_a(t)$ and $i_b(t)$ before and after a perturbation in the phase-a duty ratio, $d_a[n]$. $d_b[n]$ is assumed to be constant during the whole illustration. In the second graph $v_{ma}(t)$ and $v_{ca}(t)$ are illustrated. $v_{mb}(t)$ and $v_{cb}(t)$ are similar to those of phase-a, but delayed by half a cycle.

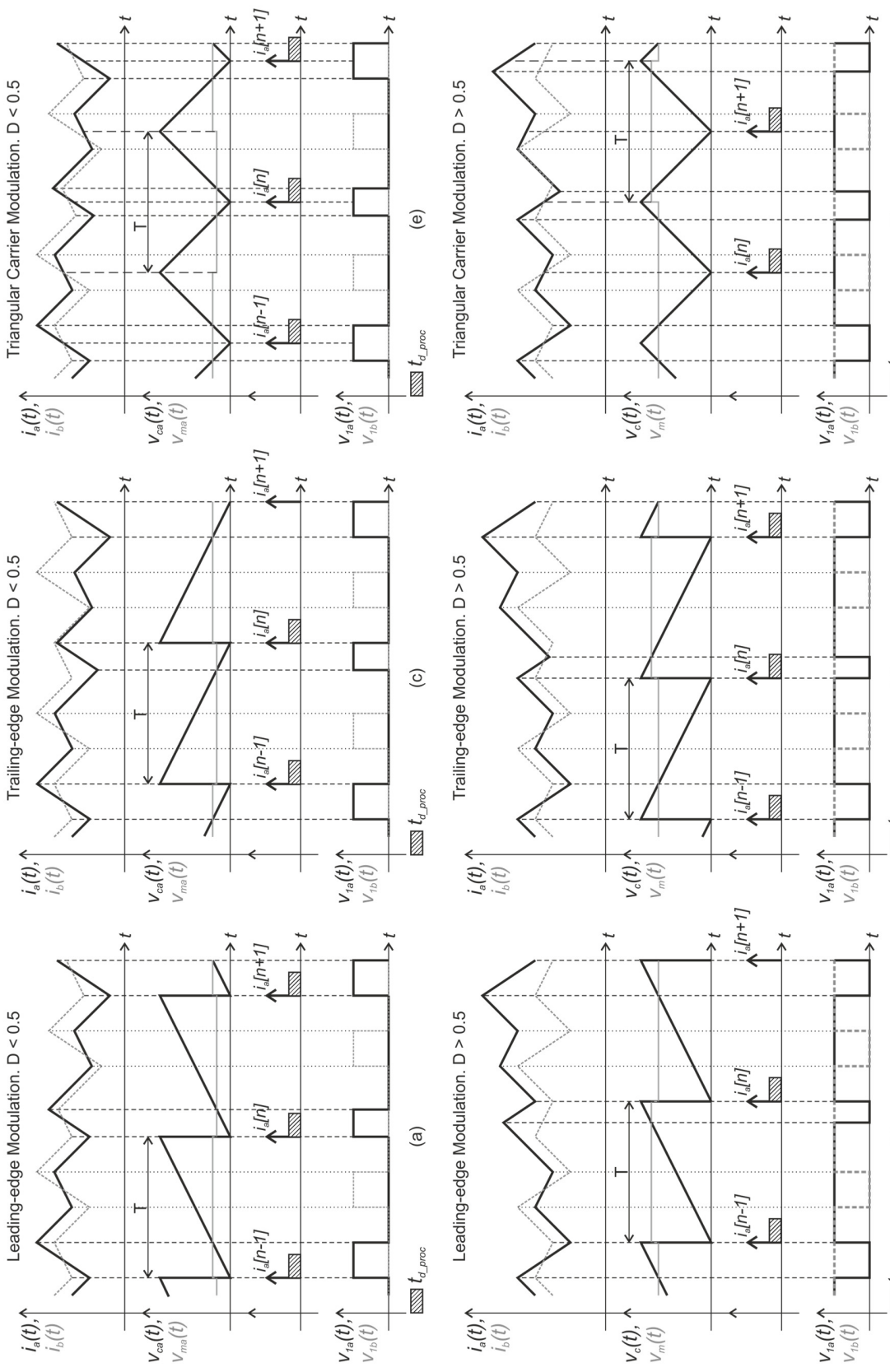

Figure 2.20. Analysis of the digital current control modulation schemes for the dual interleaved boost converter with inter-phase transformer.

The third graph depicts the sampled values of the phase-a current waveform $i_a[n]$ and the length of the processing time t_{d_proc}. Finally, the bottom plot shows $v_{ge1a}(t)$ and $v_{ge1b}(t)$.

As seen in Figures 2.20(a) and 2.20(b) for the leading-edge modulation, the DPWM counters are configured in count up mode, $v_{1a}(t)$ and $v_{1b}(t)$ are switched on when their respective DPWM counters are reset to zero, and the sampled current will be the valley-current for both $D < 0.5$ and $D > 0.5$. For the trailing-edge modulation, Figures 2.20(c) and 2.20(d), the DPWM counters are configured in count down mode, $v_{1a}(t)$ and $v_{1b}(t)$ are switched off when their respective DPWM counters are reset to zero, and the sampled current will be the peak-current for both $D < 0.5$ and $D > 0.5$.

Finally Figures 2.20(e) and 2.20(f), illustrate the waveforms for the case where the DPWM counters are configured in up-down count mode. As seen in these figures, $v_{1a}(t)$ is switched on whenever $v_{ca}(t)$ is counting down and it crosses $v_{ma}(t)$. Conversely, $v_{1a}(t)$ is switched off every time $v_{ca}(t)$ is counting up and it crosses $v_{ma}(t)$. Unlike the leading-edge and the trailing-edge modulations where the sampling of $i_a(t)$ occurs at the same time as the update of $v_{ma}(t)$, in this modulation strategy these events occur at different times. $i_a(t)$ is sampled every time its DPWM counter reaches zero and $v_{ma}(t)$ is updated when its counter is at maximum count. This particular configuration has two advantages. First, the on-time of $v_{1a}(t)$ is always symmetrical with respect to the sampling instant $i_a(t)$, thereby the name triangular carrier modulation with symmetric on-time. Second, unlike the previous modulation strategies where the update of $v_{ma}(t)$ and $v_{mb}(t)$ has a delay of one sampling period, T, in this modulation the update delay is reduced to $T/2$.

A close look at Figure 2.20(e) and 2.20(f) reveals that the sampling instants are strategically positioned in the middle of the transistors on-state intervals. This strongly suggests that if the symmetry of the phase current waveforms is preserved over a switching period, the sampled value will be close to the local average of the waveforms. Figure 2.21 will be employed to demonstrate this. In this figure, the phase-a current waveform, $i_a(t)$, and the transistor driving signals $v_{1a}(t)$ and $v_{1b}(t)$ are sketched for $D < 0.5$ under the assumption that the converter is in steady-state operation, and the on-state intervals of $v_{1a}(t)$ and $v_{1b}(t)$ are denoted $d_{b,n}T$ and $d_{a,n}T$ respectively, where the subindex n indicates the

corresponding switching interval and i_{a0} is the steady state average-value of the phase current at the beginning of the switching cycle and is defined in Table 2.7.

By inspection of Figure 2.21, $i_a(t)$ may be divided into five line segments, $i_{a1}(t)$ to $i_{a5}(t)$, which are defined as shown in Table 2.6. The slopes of $i_{a1}(t)$ to $i_{a5}(t)$, namely m_1 to m_5, are found in Table 2.7 and were calculated for each line segment using the derivative of Equation (2.3):

$$\frac{di_a(t)}{dt} = \frac{1}{2}\frac{di_{in}(t)}{dt} - \frac{di_{diff}(t)}{dt} \tag{2.30}$$

According to Figure 2.21, the sampling instant of $i_a(t)$ occurs at $T/2$, which is located in the interval corresponding to $i_{a3}(t)$. Therefore, in order to find the value of the sampled current, it is necessary to find $i_{a3}(T/2)$. Under the assumption that the converter is in steady-state conditions and that $d_{a,n} = d_{b,n} = d_{b,n+1} = D$, $i_{a3}(t)$ can be defined for any $D < 0.5$ employing the equations of Table 2.6 and Table 2.7 as shown in Equation (2.31).

$$i_{a3}(t) = m_3\left(t - \frac{1-D}{2}T\right) + m_2\left(\frac{1-D}{2}T - \frac{D}{2}T\right) + m_1\left(\frac{D}{2}T + \frac{D}{2}T\right) + i_{a0} \tag{2.31}$$

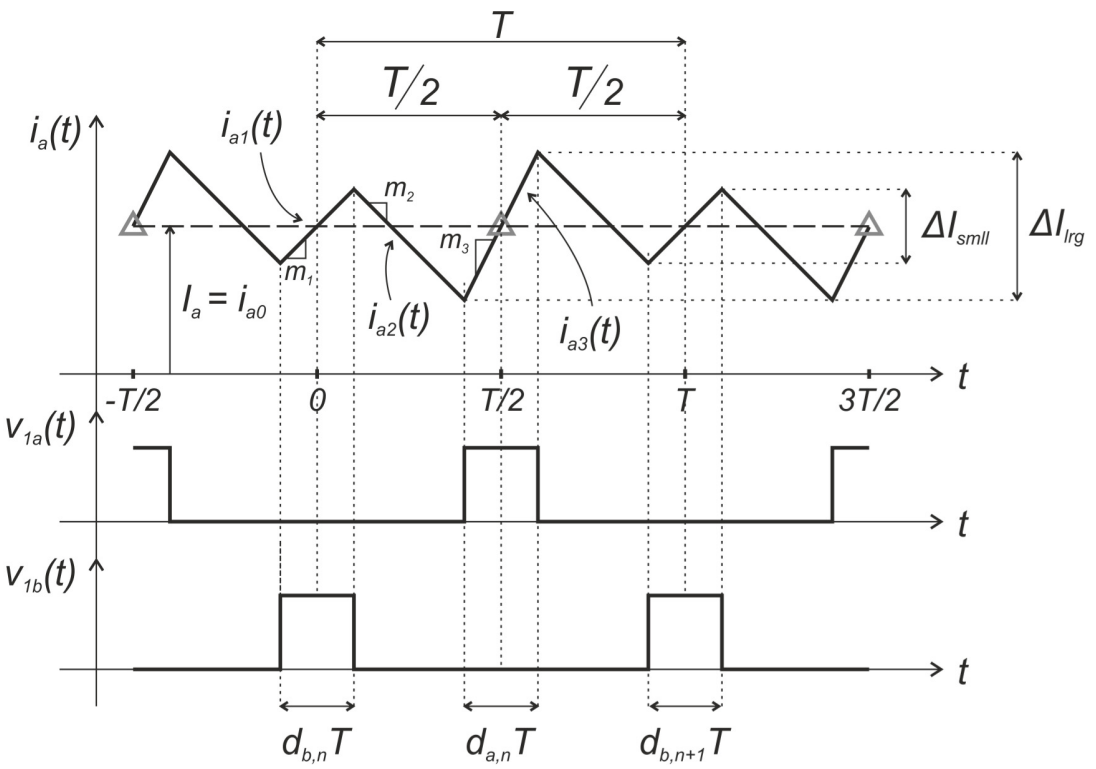

Figure 2.21. Sampled value of the phase-a current waveform when the sampling instants are located in the middle of the transistors on-intervals. *D < 0.5*.

Table 2.6. Equations of the line segments comprising $i_a(t)$ valid for D < 0.5 (Figure 2.19).

Function	Equation	Interval
$i_{a1}(t)$	$m_1\left(t+\frac{d_{b,n}T}{2}\right)+i_{a0}$	$\left(0,+\frac{d_{b,n}T}{2}\right)$
$i_{a2}(t)$	$m_2\left(t-\frac{d_{b,n}T}{2}\right)+i_{a1}\left(\frac{d_{b,n}T}{2}\right)$	$\left(+\frac{d_{b,n}T}{2},+\left(\frac{1}{2}-\frac{d_{a,n}}{2}\right)T\right)$
$i_{a3}(t)$	$m_3\left(t-\left(\frac{1}{2}-\frac{d_{a,n}}{2}\right)T\right)+i_{a2}\left(\left(\frac{1}{2}-\frac{d_{a,n}}{2}\right)T\right)$	$\left(\left(\frac{1}{2}-\frac{d_{a,n}}{2}\right)T,\left(\frac{1}{2}+\frac{d_{a,n}}{2}\right)T\right)$
$i_{a4}(t)$	$m_4\left(t-\left(\frac{1}{2}+\frac{d_{a,n}}{2}\right)T\right)+i_{a3}\left(\left(\frac{1}{2}+\frac{d_{a,n}}{2}\right)T\right)$	$\left(\left(\frac{1}{2}+\frac{d_{a,n}}{2}\right)T,\left(1-\frac{d_{b,n+1}}{2}\right)T\right)$
$i_{a5}(t)$	$m_5\left(t-\left(1-\frac{d_{b,n+1}}{2}\right)T\right)+i_{a4}\left(\left(1-\frac{d_{b,n+1}}{2}\right)T\right)$	$\left(\left(1-\frac{d_{b,n+1}}{2}\right)T,T\right)$

Table 2.7. Slopes of the line segments comprising $i_a(t)$.

Slope	Equation D < 0.5	Equation D > 0.5
i_{a0}*	$I_a-\frac{\Delta I_{smll}}{2}=\frac{I_{in}}{2}-\frac{V_{in}-V_o/2}{4L_{in}}DT+\frac{V_o}{2L_{diff}}DT$	$I_a-\frac{\Delta I_{lrg}}{2}=\frac{I_{in}}{2}-\frac{V_{in}-V_o/2}{4L_{in}}DT-\frac{V_o}{2L_{diff}}DT$
m_1	$\frac{V_{in}-V_o/2}{2L_{in}}-\frac{V_o}{L_{diff}}$	$\frac{V_{in}-V_o/2}{2L_{in}}+\frac{V_o}{L_{diff}}$
m_2	$\frac{V_{in}-V_o}{2L_{in}}$	$\frac{V_{in}}{2L_{in}}$
m_3	$\frac{V_{in}-V_o/2}{2L_{in}}+\frac{V_o}{L_{diff}}$	$\frac{V_{in}-V_o/2}{2L_{in}}-\frac{V_o}{L_{diff}}$
m_4	m_2	m_2
m_5	m_1	m_1

* ΔI_{smll} and ΔI_{lrg} as defined in Table 2.1

Equation (2.31) can be simplified, yielding:

$$i_{a3}(t)=m_3\left(t-\frac{1-D}{2}T\right)+m_2\left(\frac{T}{2}-DT\right)+m_1DT+i_{a0} \tag{2.32}$$

Substituting i_{a0} from Table 2.6 and evaluating Equation (2.32) at $T/2$ yields:

$$i_{a3}\left(\frac{T}{2}\right)=\frac{1}{2}\left(\frac{V_{in}-V_o/2}{2L_{in}}+\frac{V_o}{L_{diff}}\right)DT+\frac{1}{2}\left(\frac{V_{in}-V_o}{2L_{in}}\right)T-\left(\frac{V_{in}-V_o}{2L_{in}}\right)DT+ \quad \ldots$$
$$+\left(\frac{V_{in}-V_o/2}{2L_{in}}-\frac{V_o}{L_{diff}}\right)DT+I_a-\left(\frac{V_{in}-V_o/2}{4L_{in}}-\frac{V_o}{2L_{diff}}\right)DT \qquad (2.33)$$

Simplifying Equation (2.33), results in:

$$i_{a3}\left(\frac{T}{2}\right)=\frac{1}{2}\left(\frac{V_{in}-V_o}{2L_{in}}\right)T+\left(\frac{V_o}{4L_{in}}\right)DT+I_a \qquad (2.34)$$

Equation (2.34) can be further simplified using the conversion ratio of the converter, Equation (2.1), resulting in:

$$i_{a3}\left(\frac{T}{2}\right)=-\frac{V_{in}DT}{4L_{in}(1-D)}+\frac{V_{in}DT}{4L_{in}(1-D)}+I_a=I_a \qquad (2.35)$$

Equation (2.35) demonstrates that sampling in the middle of the transistors' on-state intervals when the triangular carrier modulation is employed, will acquire the average-

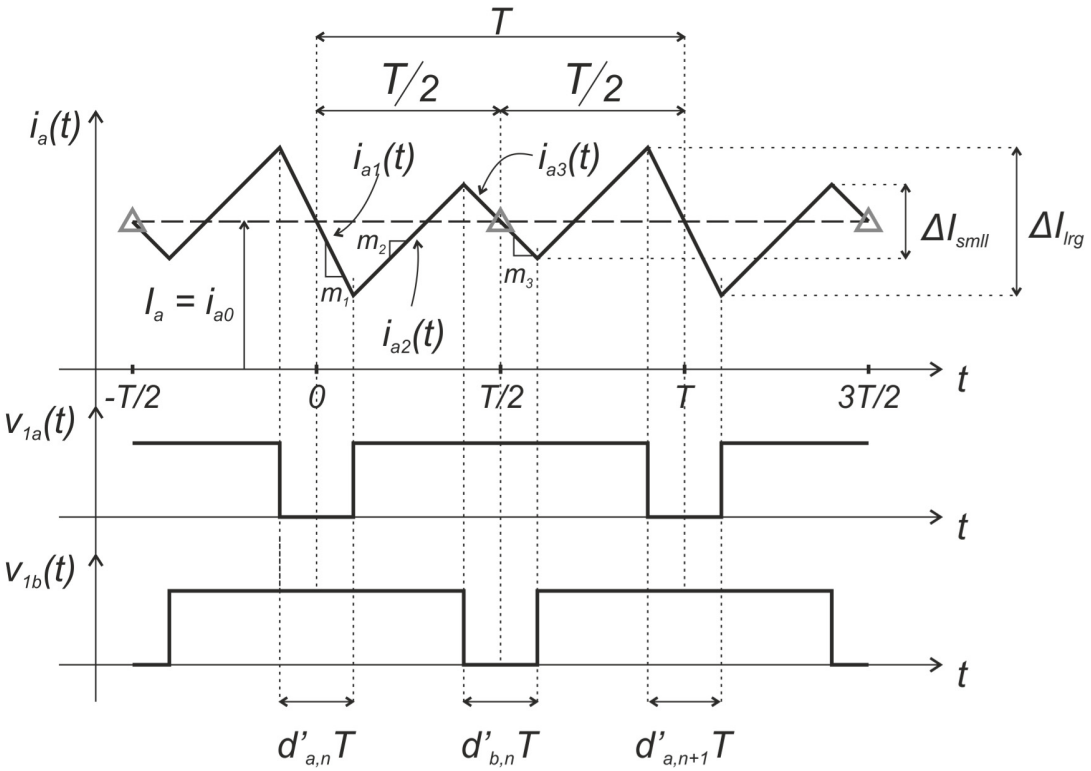

Figure 2.22. Sampled value of the phase-a current waveform when the sampling instants are located in the middle of the transistors on-intervals. *D > 0.5*.

value of the phase-current. A similar procedure can be undertaken for *D > 0.5* using Figure 2.22 and the corresponding equations from Table 2.7 and 2.8, leading to the same conclusion.

Table 2.8. Equations of the line segments comprising $i_a(t)$ valid for *D < 0.5* (Figure 2.20).

Function	Equation	Interval
$i_{a1}(t)$	$m_1\left(t+\frac{d'_{a,n}T}{2}\right)+i_{a0}$	$\left(0,+\frac{d'_{a,n}T}{2}\right)$
$i_{a2}(t)$	$m_2\left(t-\frac{d'_{a,n}T}{2}\right)+i_{a1}\left(\frac{d'_{a,n}T}{2}\right)$	$\left(+\frac{d'_{a,n}T}{2},+\left(\frac{1}{2}-\frac{d'_{b,n}}{2}\right)T\right)$
$i_{a3}(t)$	$m_3\left(t-\left(\frac{1}{2}-\frac{d'_{b,n}}{2}\right)T\right)+i_{a2}\left(\left(\frac{1}{2}-\frac{d'_{b,n}}{2}\right)T\right)$	$\left(\left(\frac{1}{2}-\frac{d'_{b,n}}{2}\right)T,\left(\frac{1}{2}+\frac{d'_{b,n}}{2}\right)T\right)$
$i_{a4}(t)$	$m_4\left(t-\left(\frac{1}{2}+\frac{d'_{b,n}}{2}\right)T\right)+i_{a3}\left(\left(\frac{1}{2}+\frac{d'_{b,n}}{2}\right)T\right)$	$\left(\left(\frac{1}{2}+\frac{d'_{b,n}}{2}\right)T,\left(1-\frac{d'_{a,n+1}}{2}\right)T\right)$
$i_{a5}(t)$	$m_5\left(t-\left(1-\frac{d'_{a,n+1}}{2}\right)T\right)+i_{a4}\left(\left(1-\frac{d'_{a,n+1}}{2}\right)T\right)$	$\left(\left(1-\frac{d'_{a,n+1}}{2}\right)T,T\right)$

2.7. Summary

Starting with a review of the steady-state waveforms for the dual interleaved boost converter with IPT, an averaged small-signal model was derived by substitution of the converter switch networks by the averaged PWM switch model. In contrast with previous models, the small-signal model accounts for the small-ac perturbation of each control input independently. This characteristic is exploited in Chapter 4 where the model is further developed to predict the stability issues that arise from the interleaved interaction of the converter phases.

The accuracy of the small signal model has been established through detailed comparison with both a switched and large signal averaged simulations using SABER software. Excellent agreement was found for duty-ratio disturbances of up to *5 %*, except at very high duty-ratio values (*D = 0.8*), where noticeable discrepancies occurred, and this was attributed to the assumptions of the linearization analysis becoming invalid. However,

with duty-ratio disturbances of up to *5 %* the error in the small signal model remained less than approximately *10 %*.

By analysing the main digital current-control strategies that employ uniformly-sampled pulse-width modulation, the sampling strategies of the trailing and the leading edge modulations were seen to result in the valley and the peak current of the converter being sampled. Finally, the triangular carrier modulation with symmetric on-time was shown to result in the sampled value of the phase currents being equal to the average value of the phase current waveforms when the system is in steady-state conditions. This approach is therefore well-suited to the control of the dual interleaved converter, providing a straight-forward method of ensuring current-balance between two phases.

2.8. References

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Chapter 3
Digital control platform and algorithm implementation

3.1. Introduction

In the previous Chapter, three digital control methodologies based on the uniformly-sampled pulse-width modulation were discussed for the dual-interleaved boost converter: valley-current, peak-current and average-current control. To investigate the practical advantages and disadvantages of these control strategies, a control platform containing a digital signal processor and all the necessary components to interface it with a prototype dual-interleaved converter was developed. In this Chapter the construction of this control platform, the implementation of the control algorithms and the practical and simulation results obtained are presented and discussed.

The first and second sections discuss the design, component selection and construction details of the digital control platform. The third section covers the implementation of the valley-current, peak-current and average-current control algorithms in the Digital Signal Controller, DSC. Also, in this section a variation of the average-current control strategy is proposed and implemented. The fourth section presents a short discussion of the SABER simulation models developed to investigate the behaviour of the control strategies. Finally, the last two sections present a discussion of the experimental and simulation results obtained with the control strategies and demonstrate the validity of the simulation models.

3.2. Prototype of the dual-interleaved boost converter with inter-phase transformer

Figure 3.1 shows a converter circuit diagram with the control platform, which indicates the input/output signals that will drive the converter under current control mode. The DIBC prototype is a *25 kW* high-density bi-directional version based on the requirements of a small fuel-cell based vehicle power train. This converter has been developed within the Power Conversion Group by Dr Gerardo Calderon-Lopez as part of a separate research project. The prototype has an input voltage range of V_{in} *= 75 V to 150 V*; an output voltage range, V_o *= 220 V to 275 V*; an individual-phase switching frequency, f_s *= 30 kHz*; and it has a maximum power capability, P_o *= 25 kW*.

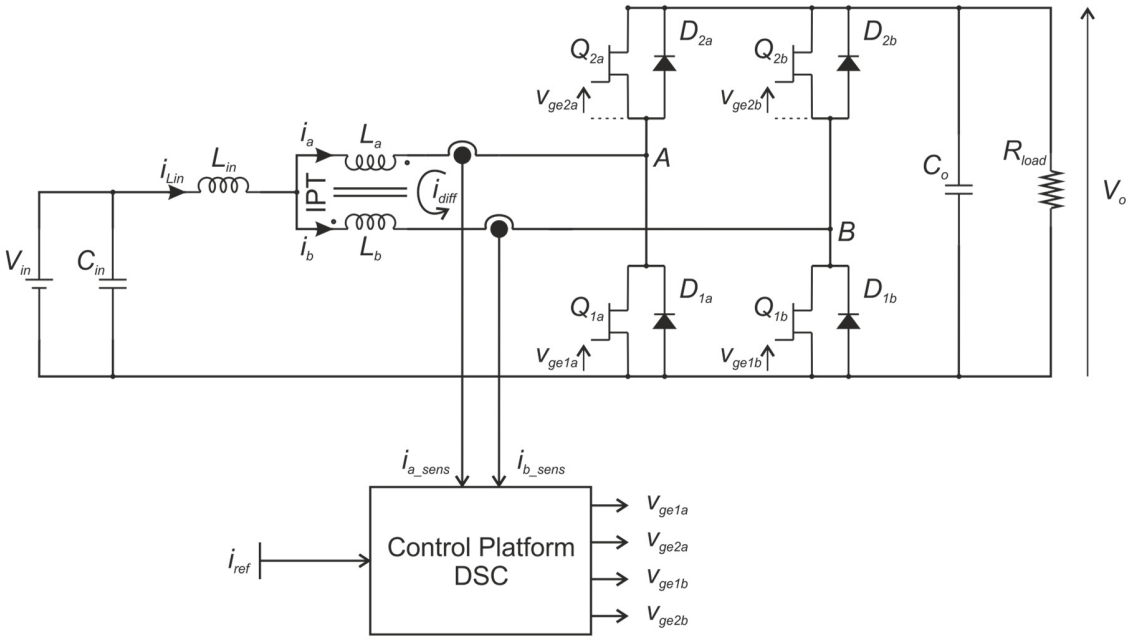

Figure 3.1. DIBC topology and control platform.

The input inductor was designed to give an overall input ripple current of approximately *114 A* peak-to-peak under worst-case conditions (*Vin = 75 V, Vo = 275 V*), whilst the IPT was designed to have a maximum peak-to-peak differential current of approximately *8 A* under worst case conditions (*D <= 0.5*). The output capacitance was calculated to obtain a maximum output voltage ripple of *2 %* at maximum voltage conditions. In order to reduce the parasitic inductance of the switching paths and prevent

large over-voltage transients, the components and devices are interconnected using planar bus bars. For the thermal management, the half-bridge semiconductor modules and magnetic component cases are mounted onto a liquid-cooled heat sink. Table 3.1 presents a summary of the prototype details whilst a picture of the converter is shown in Figure 3.2.

Table 3.1. Parameters of the DIBC prototype.

Operation Ratings		Device Specifications	
Maximum power, P_o	*25 kW*	**Input capacitance, C_{in}**	*22.4 µF*
Input voltage range, V_{in}	*75 V – 150 V*	**Output capacitance, C_o**	*45 µF*
Output voltage range, V_o	*220 V – 275 V*	**Input inductance, L_{in}**	*5.12 µH*
Operating frequency f	*30 kHz*	**Inter-Phase Transformer**	
Maximum input current, I_{Lin}*	*330 A*	**Winding self-inductance, L_a, L_b**	*75.14 µH*
Maximum output current, I_o*	*114 A*	**Mutual inductance, L_m**	*74.9 µH*
		Differential inductance, L_{diff}	*299.7 µH*
		Coupling coefficient, k	*0.997*
		Active Devices	
		IGBT Module	*CM300DU-21NFH*

* Calculated assuming operation at maximum power.

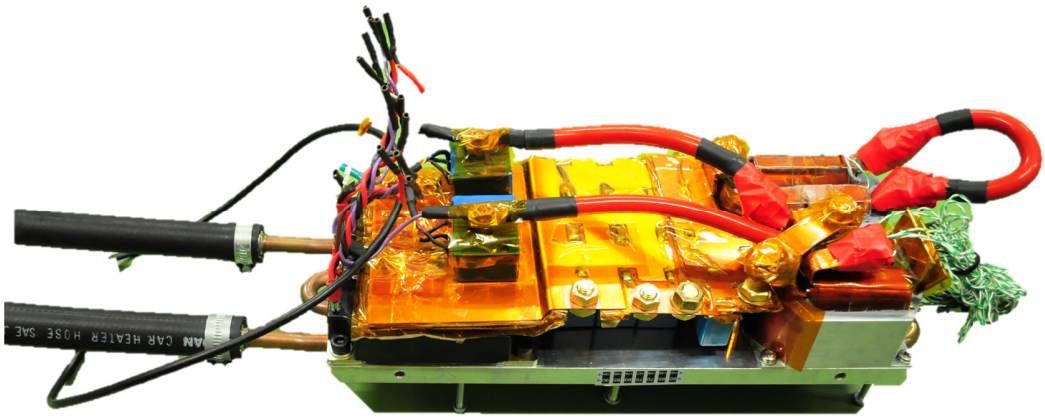

Figure 3.2. Prototype of the dual-interleaved boost converter with inter-phase transformer.

3.3. Digital control platform prototype

The control platform was created as an interface between the DSC and the converter prototype. This platform consists of several stages which are represented in the block diagram form in Figure 3.3. The functionality of these stages will be described next. The block located at the top right of the diagram represents the interleaved converter. The transistors of the converter are driven by four gate-to-emitter signals which are represented as inputs to the functional block: v_{ge1a}, v_{ge1b}, v_{ge2a} and v_{ge2b}; these signals range from *-5 V* to *+15 V*. The converter output voltage, v_o, load current, i_{load}, and phase currents, i_a and i_b respectively, are represented as output signals. The range of i_a and i_b was determined under the assumption that the input current, i_{Lin}, divides equally between the phases. Employing the maximum value of i_{Lin} from Table 3.1, the maximum value of i_a and i_b was determined to be approximately *175 A*.

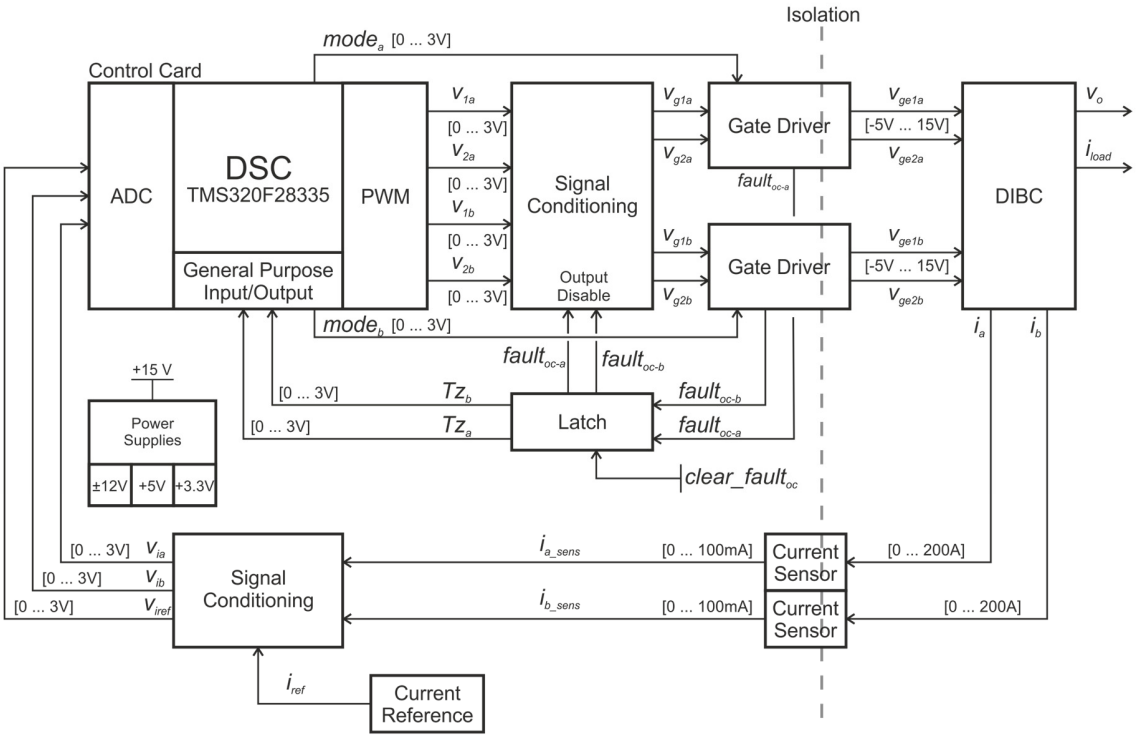

Figure 3.3. Functional block diagram of the digital control platform.

Two hall-effect current sensors, as depicted by the block diagram, were employed to measure the phase-currents. These transducers generate two current signals i_{a_sens} and

i_{b_sens} proportional to i_a and i_b respectively. The generated signals have a conversion ratio, K_N, of *1:2000 and* range between *0 mA to 100 mA*. These current signals representing the phase currents are fed into a conditioning stage where they are converted into voltage signals ready to be read by the ADC. These signals are denoted v_{ia} and v_{ib} in the diagram. Additionally a third signal designated v_{iref} is generated in this stage. This signal allows the user to set the target or reference phase-current for the converter by means of a potentiometer.

The control card, which is the next block in the diagram, is divided into three main parts: the ADC module which samples the signals v_{ia}, v_{ib} and v_{iref}; the PWM module which generates the driving signals v_{1a}, v_{1b}, v_{2a} and v_{2b}; and the General Purpose Input/Outputs, GPIOs, which are used to generate the control signals $mode_a$ and $mode_b$ and to read the fault signals $fault_{oc\text{-}a}$ and $fault_{oc\text{-}b}$. All the signals generated from the DSC range from *0* to *3 V*. The driving signals v_{1a}, v_{1b}, v_{2a} and v_{2b} are passed through a buffer/conditioning stage, as depicted in the diagram, where their voltage level is adjusted to be compatible with the gate drivers. Finally the gate drivers, generate the isolated gate-emitter driving signals v_{ge1a}, v_{ge1b}, v_{ge2a} and v_{ge2b} for the converter transistors. Additionally these devices are capable of two modes of operation: half-bridge mode or direct mode. In half-bridge mode, v_{ge1a} follows v_{1a} and v_{ge1b} follows the complement of v_{1a}; v_{1b} is used to enable/disable the gate-driver outputs. In direct mode, v_{ge1a} and v_{g1b} follow the driving signals v_{1a} and v_{1b}. The mode of operation is selected by the $mode_a$ and $mode_b$ signals generated in the GPIOs of the DSC.

Two over-current fault signals, $fault_{oc\text{-}a}$ and $fault_{oc\text{-}b}$, are set by the gate drivers in the event of a transistor over-current. These signals are latched and stop the PWM generation in the processor until the user clears the fault manually using a push-button provided in the control platform, $clear\_fault_{oc}$. The board is powered by a single external power supply of *+15 V* and incorporates additional dc-dc converters to generate *+12 V, -12 V, +5 V* and *+3.3 V*. Having established the functionality of all the stages in the control platform, the following sections will address the device selection and design for each.

3.3.1. Digital Signal Controller (DSC)

The control platform developed in this project was designed to interface a Delfino TMS320F28335 digital signal controller from Texas Instruments with the converter prototype [1]. This floating-point, digital signal controller was chosen as it was one of the fastest processors available at that time in the market. The processor is provided in an industry-standard DIMM-form-factor control card, shown in Figure 3.4, which is a complete board-level module incorporating all the necessary components to power up and code the processor using a standard 100-pin DIMM interface.

Figure 3.4. Delfino TMS320F28335 Control Card.

Table 3.2. Principal Features of the Texas Instruments TMS320F28335 [2].

CPU	C28x
Million Multiply Accumulate Cycles per Second, MMACS	150 MAC
FPU	Yes
Master Clock Frequency	150 MHz
RAM	68 Kb
Flash	512 kB
DMA	1 x 6-Channels DMA
PWM	9 Modules, 18 Outputs
Analog to Digital Converter, ADC	1 x 16-Channels 12-Bit Pipelined
ADC Conversion Time	80 ns
Inter-Integrated Circuit protocol, I2C	1
Universal Asynchronous Receiver Transmitter, UART (SCI)	3
Serial Port Interface, SPI	1
CAN,	2
Timers	3 32-Bit CPU,1 WD
General Port Input Output, GPIO	88

The processor incorporates a 12-bit analogue-to-digital converter, ADC, with a minimum conversion time of *80 ns* per sample and is capable of sampling up to 16 multiplexed channels. It also contains nine digital pulse width modulation modules with a

minimum resolution of *6.66 ns*. The maximum processor clock frequency is f_{clk} = *150 MHz.* Table 3.2 provides a summary of the processor's main characteristics [2].

3.3.2. Current sensors and conditioning for the measured signals

Figure 3.5 shows a detailed diagram of the current sensors and associated conditioning stage. The current transducers employed to measure the phase currents in the converter were the *LA 200-P* manufactured by LEM which have a conversion ratio, K_N, of *1:2000* [3]. A measurement resistor, R_m, of *10 Ω* is connected to the output of the current transducer to generate *5 mV per Ampere* of current measured. The voltage generated across R_m is then scaled using an operational amplifier configured as a level shifter. The gain of the amplifier is set by the resistors R_a, R_b, R_c and R_d as shown in Equation (3.1):

$$A_{AV} = \frac{R_B}{R_A} \tag{3.1}$$

where $R_A = R_a = R_c$ and $R_B = R_b = R_d$. The level-shifting function provided by the voltage V_{ref} connected to R_d enables the ADC, which only accepts positive inputs, to read both positive and negative phase currents. The gain of the level shifter, A_{AV}, was set to 1.5 and the zero-current reference on the level-shifter was established as *1.5 V*. This allowed the measurement of phase-currents ranging from *–200 A* to *+200 A* using a voltage range from *0 V* to *3 V* at the ADC input. An OPA2343UA amplifier was used in the level shifter [4]. This is a rail-to-rail amplifier specially designed to drive A/D converters.

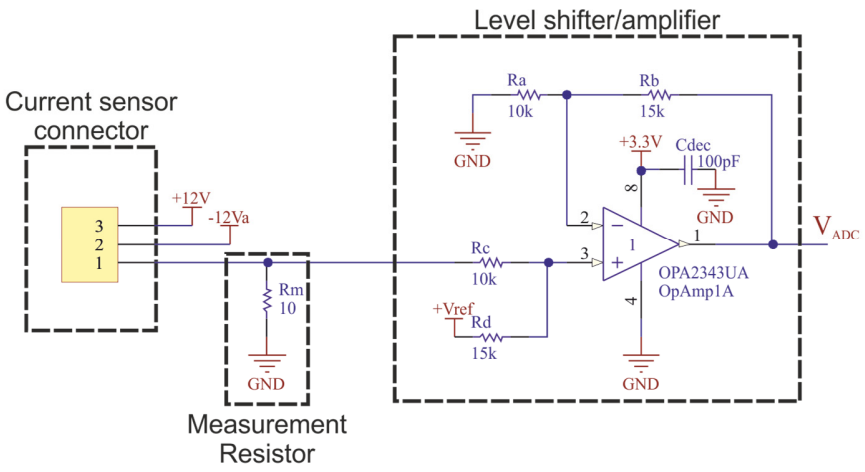

Figure 3.5. Current sensor and signal conditioning for the ADC.

Finally, the voltage delivered to the ADC per Ampere of current measured can be calculated using Equation (3.2):

$$v_{ix}(t) = \left(\frac{i_x(t)}{K_N} R_m \right) \frac{R_B}{R_A} + 1.5 = 1.5 \left(\frac{i_x(t)}{200} + 1 \right) \tag{3.2}$$

The full schematic diagram of the conditioning stage of the control platform can be found in Figure F.1, Appendix F.

3.3.3. Signal conditioning for transistor driving signals and gate drivers

The following paragraphs will describe how the gate drivers were used in combination with the DSC. For this purpose Figure 3.6 shows a simplified functional block diagram of this stage. A detailed diagram showing all the components employed in the design can be found in Figure F.3, Appendix F.

The gate drivers employed were the 2SC0435T manufactured by CONCEPT [5, 6]. These circuits provide a dual channel IGBT/MOSFET driver capability which is fully isolated and has short-circuit protection through v_{ce} monitoring.

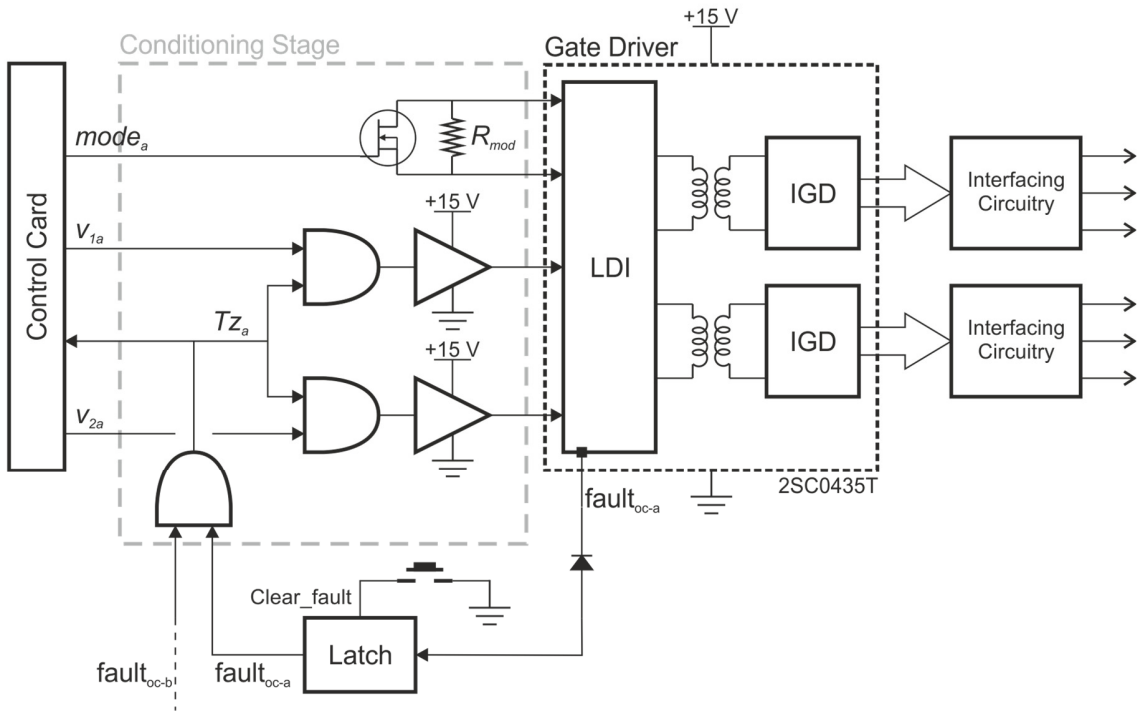

Figure 3.6. Functional block diagram of the signal conditioning for the transistor driving signals and the gate drivers.

According to Figure 3.6, the transistor driving-signals produced by the PWM module on the controller, v_{1a} and v_{2a} respectively, are taken to an array of AND logic gates. This array provides a way to interrupt the propagation of v_{1a} and v_{2a} in the event of an over-current failure and notifies the processor of the fault by means of the signal Tz_a. An UCC37324 MOSFET-driver was used to interface the TTL logic signals with the gate drivers which requires 15 V input. The over-current signals, $fault_{oc\text{-}a}$ and $fault_{oc\text{-}b}$, are pulled down when a fault occurs and held in this state by a latch circuit. The fault must be cleared manually using an external push button to re-enable operation of the system.

Additionally, an external N-Channel MOSFET driven directly by the DSC is connected in parallel to a mode selector resistor, R_{mod}. This arrangement enables the DSC to control the mode of operation of the gate drivers. When this MOSFET is turned off, the gate drivers operate in bridge mode, when is turned on they operate in direct mode. Finally the block shown at the right hand side of the CONCEPT driver denoted as interface circuitry includes the IGBT gate drive resistors.

3.3.3. Construction Details

A double-sided PCB with ground planes was created to accommodate the control platform circuitry. The complete schematic diagrams of this platform are found in Appendix F. The layout is shown in Figure 3.7 and was produced using Altium Designer. The control card is located on the top layer whilst the gate drivers are located on the bottom layer. Figure 3.8 shows a picture of the control platform.

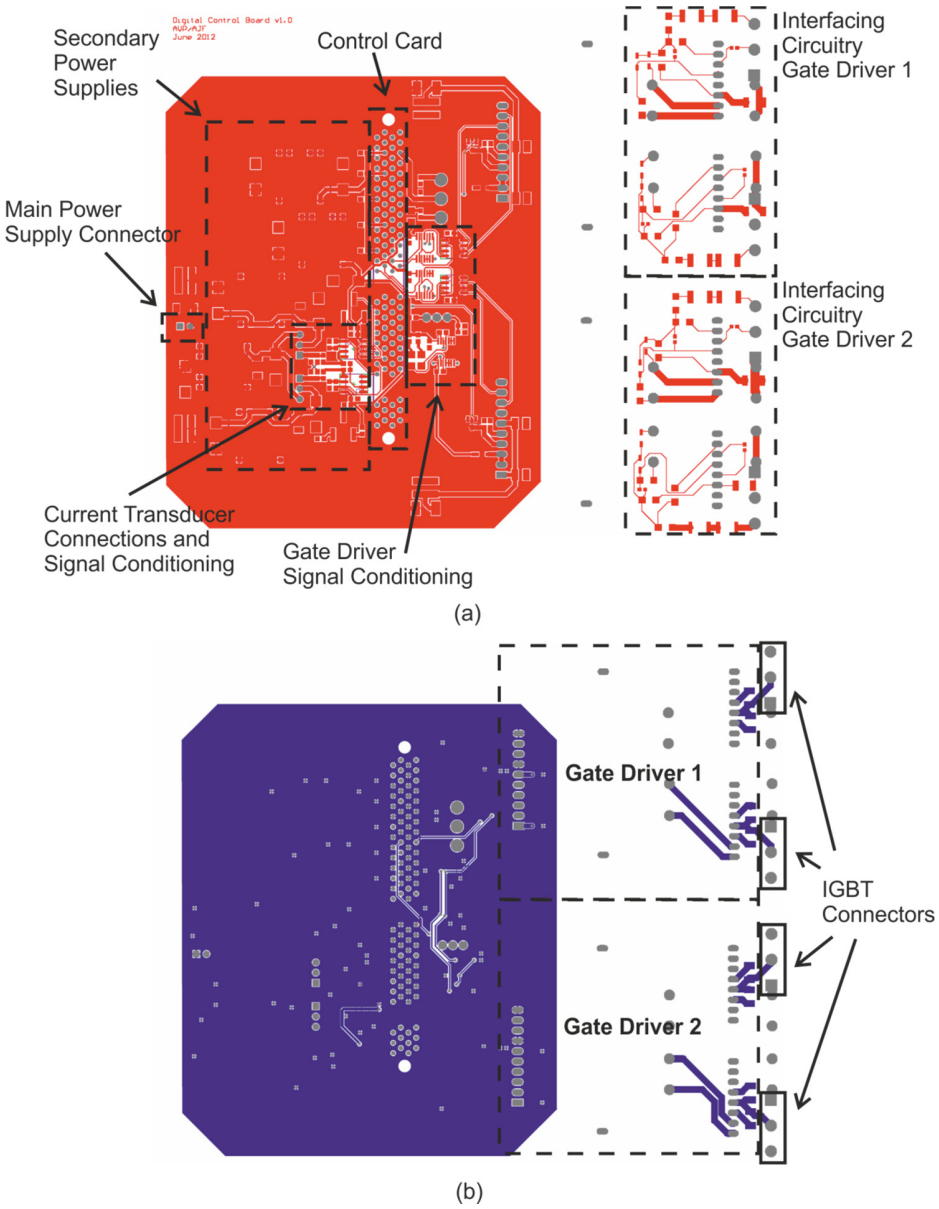

Figure 3.7. Printed circuit board of the digital control platform. (a) Top layer; (b) Bottom layer.

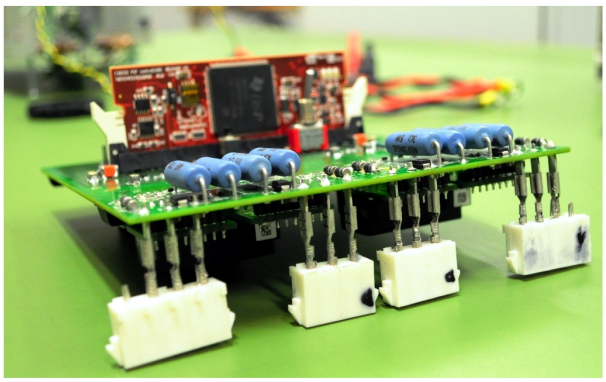

Figure 3.8. Digital control platform.

3.4. Implementation of the digital current-control algorithms on the DSC

The DSC was programmed using MATLAB Simulink and MATLAB Embedded Coder to create a block diagram which was compiled into C code and then into assembly files using Code Composer Studio. The assembly files were downloaded into the DSC flash memory by means of a docking station for the control card [7]. The Simulink diagrams generated can be found in Appendix D.

In the following sections the implementation of the valley-current, peak-current and average-current control strategies described in Section 2.6, Chapter 2, are discussed. Also, a variation of the average-current control strategy is investigated, which has not been reported before. In this variation the DPWM modules are updated immediately after the calculation of the duty-ratio, thereby enabling a reduction in the processing delay of the system. The algorithms for these control strategies share the same foundation. The only difference between them is the configuration of the DPWM modules and the location of the current-sampling instants which can be easily modified in the Simulink diagram.

3.4.1. Configuration and synchronization of the DSC modules

In this section, the configuration of the DSC is explained using the diagram of Figure 3.9 and the waveforms of Figure 3.10(a) and 3.10(b). In Figure 3.9, the functionality of the modules employed in the DSC and their inter-connections are represented using a block diagram. This diagram consists of four blocks: the analog-to-digital converter module, *ADC*, the ADC Interrupt Service Routine, *ADC_ISR*, and the digital pulse-width modulators, *DPWM A* and *DPWM B*.

The *ADC* was programmed to sample three signals in the following sequence: the phase-a current, v_{ia}, first, the phase-b current, v_{ib}, second, and the reference-current, v_{iref}, third. The sampled-data is stored in separate registers. The contents of these registers are labelled in Figure 3.9 as $v_{ia}[n]$, $v_{ib}[n]$ and $v_{iref}[n]$ respectively and can be calculated using Equation (3.3):

$$v_{ix}[\mathrm{n}] = 2^{N_{ADC}} \frac{v_{ix}(t)}{V_{ADC\max}} = (2^{12}) \frac{v_{ix}(t)}{3} \tag{3.3}$$

where N_{ADC} is the effective resolution of the ADC in bits, V_{ADCmax} is the maximum reference voltage of the ADC and v_{ix} is the sampled voltage in the corresponding channel. At the end of the sampling sequence, the ADC sets a flag to signal to the CPU the end of conversion. This flag will be referred to as EOC.

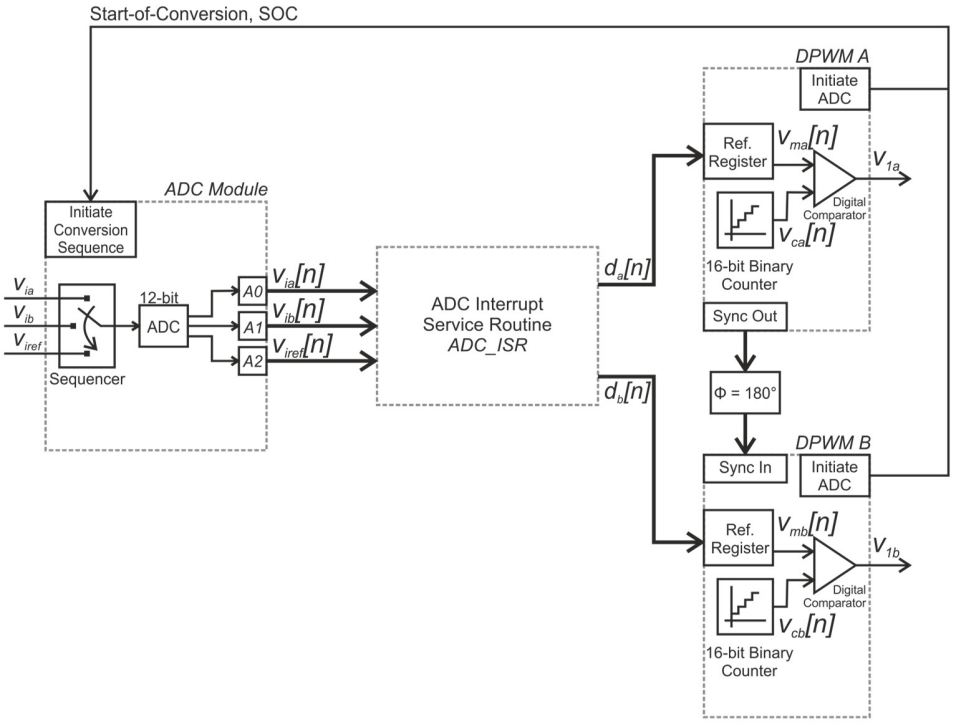

Figure 3.9. Functional block diagram of the DSC modules.

The *ADC_ISR* was programmed to be serviced by the CPU when the EOC flag is detected. This routine executes the control algorithm for the converter phases. A detailed discussion of the algorithms implemented in this service-routine is undertaken in the next section. To summarize, the service routine employs the sampled-data acquired by the *ADC* to calculate the duty-ratio of the converter transistors, $d_a[n]$ and $d_b[n]$.

As determined in Chapter 2, the binary-counters of the DPWM modules were programmed in count up mode to achieve valley-current control, in count down mode to achieve peak-current control, and count up-down mode to achieve average-current control. The strategic sampling for these control schemes was attained by programming the DPWM modules to initiate an ADC conversion sequence whenever their binary-counters reached zero.

Also, the reference-registers of the DPWM modules were programmed to be updated at the maximum count of the binary-counters. Finally, to achieve the generation of the interleaved PWM waveforms for the converter transistors, the binary-counters of these modules were synchronized and phase-shifted by 180 degrees.

The maximum count of the binary counters was determined using Equation (3.4) for the count up and the count down mode, and using Equation (3.5) for the count up-down mode:

$$v_{c\max} = \frac{f_{clk\_DPWM}}{f_{sw}} = \frac{150MHz}{30kHz} = 5000 \tag{3.4}$$

$$v_{c\max} = \frac{1}{2}\left(\frac{f_{clk\_DPWM}}{f_{sw}}\right) = 2500 \tag{3.5}$$

where f_{clk_DPWM} is the frequency of the DPWM clock, and f_{sw} is the switching frequency of the converter transistors. In the block diagram of Figure 3.9, the signal that initiates the ADC conversion is denoted as the start-of-conversion flag, SOC, and it interconnects the DPWM modules with the ADC.

The waveforms depicted in Figure 3.10(a) and 3.10(b) will be employed to discuss the synchronization of the blocks of Figure 3.9 when the DPWM counters are configured in count up mode and count up-down mode. The count down mode waveforms are not illustrated as they can be easily deduced from the ones in Figure 3.10(a). In the first and second plots of these figures the *DPWM A* and *DPWM B* counters are sketched respectively. The third and fifth plots illustrate the timing diagrams of the Start-of-Conversion flag, SOC, and the End-of-Conversion flag, EOC. Finally, the fourth and sixth graphs illustrate the timing diagrams corresponding to the ADC and CPU tasks respectively.

Initially in Figure 3.10(a), the *DPWM A* counter is reset to zero. At this instant the SOC flag is set by the *DPWM A* initiating an ADC conversion-sequence. The duration of the ADC conversion is depicted in the ADC timeline. Once the ADC conversion sequence is finished, the EOC flag is set by the ADC which requests the execution of the *ADC_ISR*. The *ADC_ISR* is then serviced by the CPU, which calculates the new duty-ratio $d_a[n]$. The time duration of *ADC_ISR* is illustrated in the CPU timeline. After $d_a[n]$ has been loaded into the

DPWM A registers, the CPU remains idle until the *DPWM B* counter is reset to zero. At this point, a new ADC conversion-sequence is requested and the routine is executed for phase-b. The synchronization of the DSC modules for the count up-down mode of operation, Figure 3.10(b), follows the same principle as described for the leading-edge modulation.

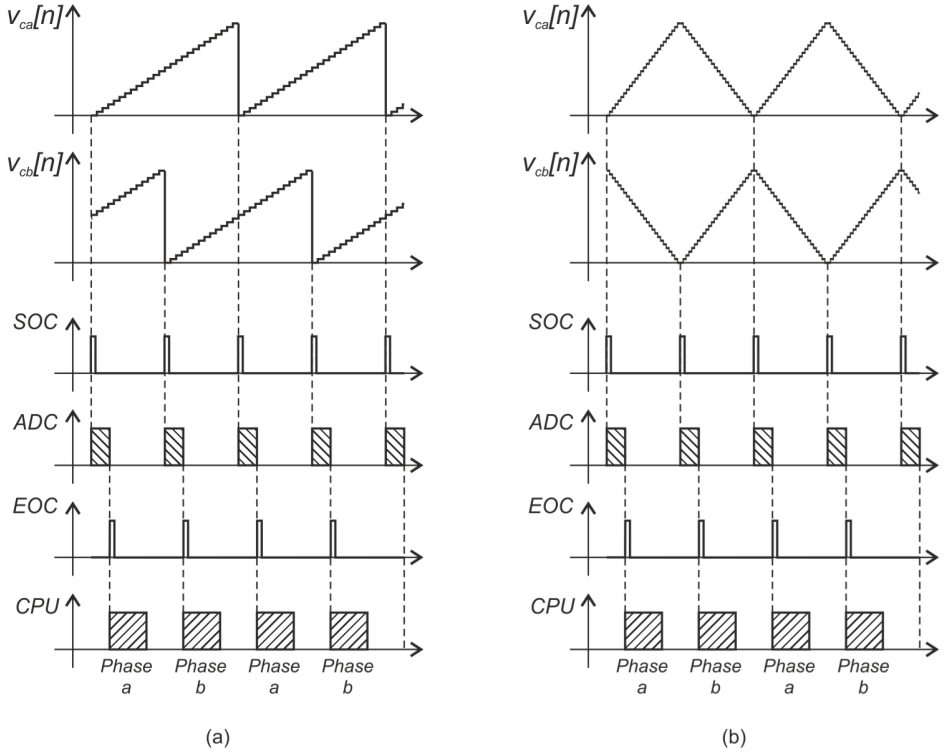

Figure 3.10. (a) Synchronization of the DSC modules for leading-edge modulation (valley-current control); (b) Synchronization of the DSC modules for triangular carrier modulation with symmetric on-time (average-current control).

3.4.2. ADC interrupt service routine, *ADC_ISR*

The scaling and control-loop compensation algorithm is executed during the ADC interrupt service routine. A flowchart of this algorithm is depicted in Figure 3.11(a), and it will be referred to as the normal-update control algorithm. The first task executed by the algorithm is to read the sampled-data acquired by the ADC module: $v_{ia}[n]$, $v_{ib}[n]$ and $v_{iref}[n]$. Followed by this, it determines which DPWM module triggered the ADC conversion and decides which phase has to be updated in the current cycle. Once the phase-in-turn has been identified, the routine carries out the scaling and compensation calculation which determines the new duty-ratio, $d_a[n]$ or $d_b[n]$. Finally, the last task of the control algorithm

is to load the new duty-ratio into the registers of its corresponding DPWM module and return to the main program.

The scaling and compensation process carried out by the control algorithm is illustrated in the block diagram of Figure 3.11(b), and it has identical structure for both phases. In this diagram, the data read from the ADC registers, $v_{iref}[n]$ and $v_{ix}[n]$ is first transformed back into Amperes. This is accomplished using Equation (3.6), which is found by substituting Equation (3.2) into Equation (3.3) and solving for i_x:

$$i_x[n] = \frac{K_N R_A}{R_m R_B}\left(\frac{V_{ADC\max}}{2^{ADCbits}} v_{ix}[\mathrm{n}] - 1.5\right) = \left(97.656e^{-3}\right) v_{ix}[\mathrm{n}] - 200 \tag{3.6}$$

The phase-current and the reference-current, $i_x[n]$ and $i_{ref}[n]$, are then compared in order to obtain the error-current, $i_{ex}[x]$, which is passed on to a digital compensation network that calculates the new duty-ratio, $d_x[n]$. Finally, $d_x[n]$ is multiplied by the modulator gain, K_{PWM}, and is loaded into the DPWM module.

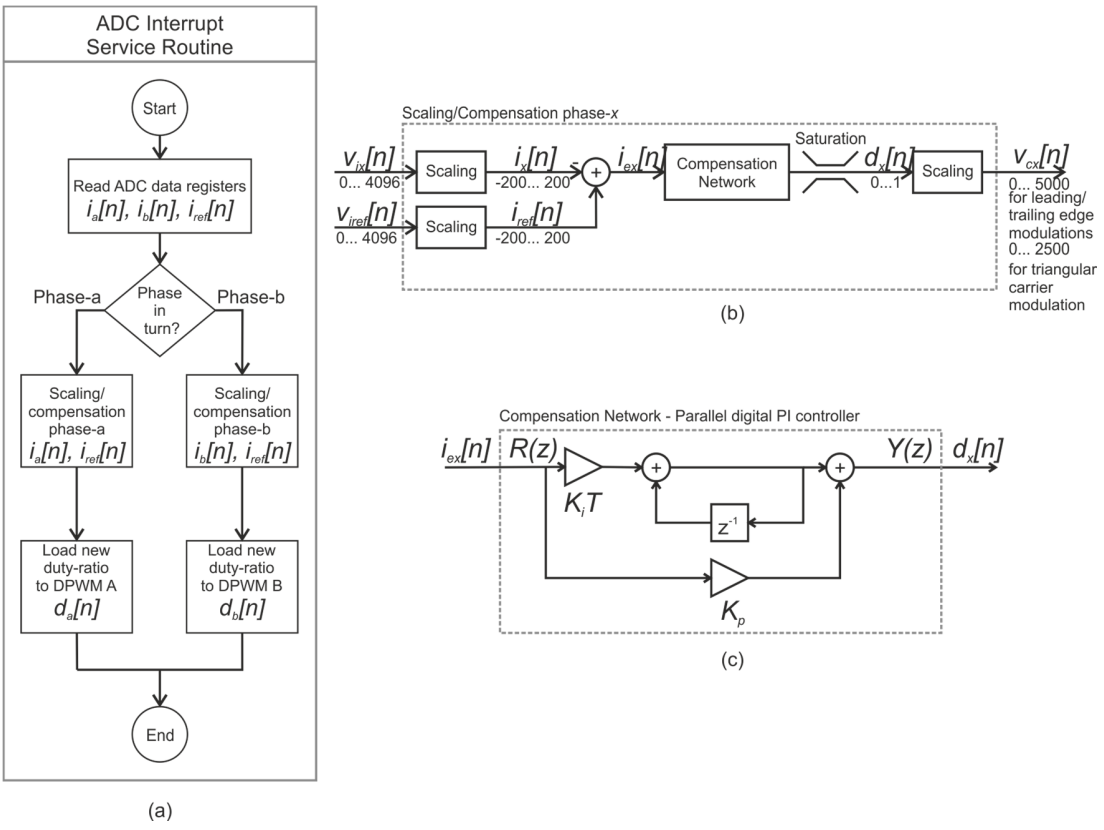

Figure 3.11. Valley-current, peak-current and average-current control algorithm. (a) Flow chart of the algorithm executed during the ADC interrupt service routine. (b) Scaling and compensation of the control-loops. (c) Compensation network: Backward-Euler proportional–integral compensator in parallel form.

In this thesis, a proportional-integral compensator implemented using the backward Euler integration method is adopted as the compensation network. The transfer function of this digital compensator is as shown in Equation (3.7), and its block diagram representation in parallel form is shown in Figure 3.10(c).

$$\frac{Y(z)}{R(z)} = K_p + K_i T \frac{1}{1 - z^{-1}} = \frac{\left(K_p - K_i T\right) z - K_p}{z - 1} \tag{3.7}$$

3.4.3. Detailed timing of the control algorithms

In Section 3.4.2 the synchronization of the DSC modules was discussed assuming the instantaneous switching of the converter transistors and neglecting the propagation delay caused by the conditioning stages of the control platform and gate-drivers.

In this section, the sampling and the control algorithm timing is analysed together with the transistor switching waveforms to determine the effects of the non-zero switching times and the propagation delays in the performance of the control algorithms. For this purpose, Figure 3.12, shows a magnification of the turn-on instant of the Q_{1a} transistor when the leading-edge modulation (valley-current control) is employed. A similar analysis can be carried out for the trailing-edge modulation (peak-current control) algorithm during the turn-off instant of Q_{1a}. The first plot of Figure 3.12 shows the transistor driving signal, v_{1a}, which is generated at the output of the DPWM modules. The second plot illustrates the gate-to-emitter voltage, v_{ge1a}. The third plot shows the collector current i_{c1a}. The fourth plot illustrates the phase-a current, i_a. The fifth plot illustrates the timing of the ADC sampling-sequence. The sixth plot shows the timing of the conversion and encoding process of the ADC module. Finally, the last plot illustrates the timing of the CPU tasks that are involved in the execution of the control algorithms.

Initially in Figure 3.12, v_{1a} is set to a high value by its corresponding *DPWM* module. The time delay from the moment where v_{1a} is set high to the moment where the phase-current is fully conducted by the transistor Q_{1a} is denoted t_{dQ}. In the figure, t_{on} is defined as the sum of the gate-driver propagation delay, t_{p_gd}, the transistor turn-on delay, $t_{d(on)}$, and the transistor current rise-time, $t_{r(on)}$:

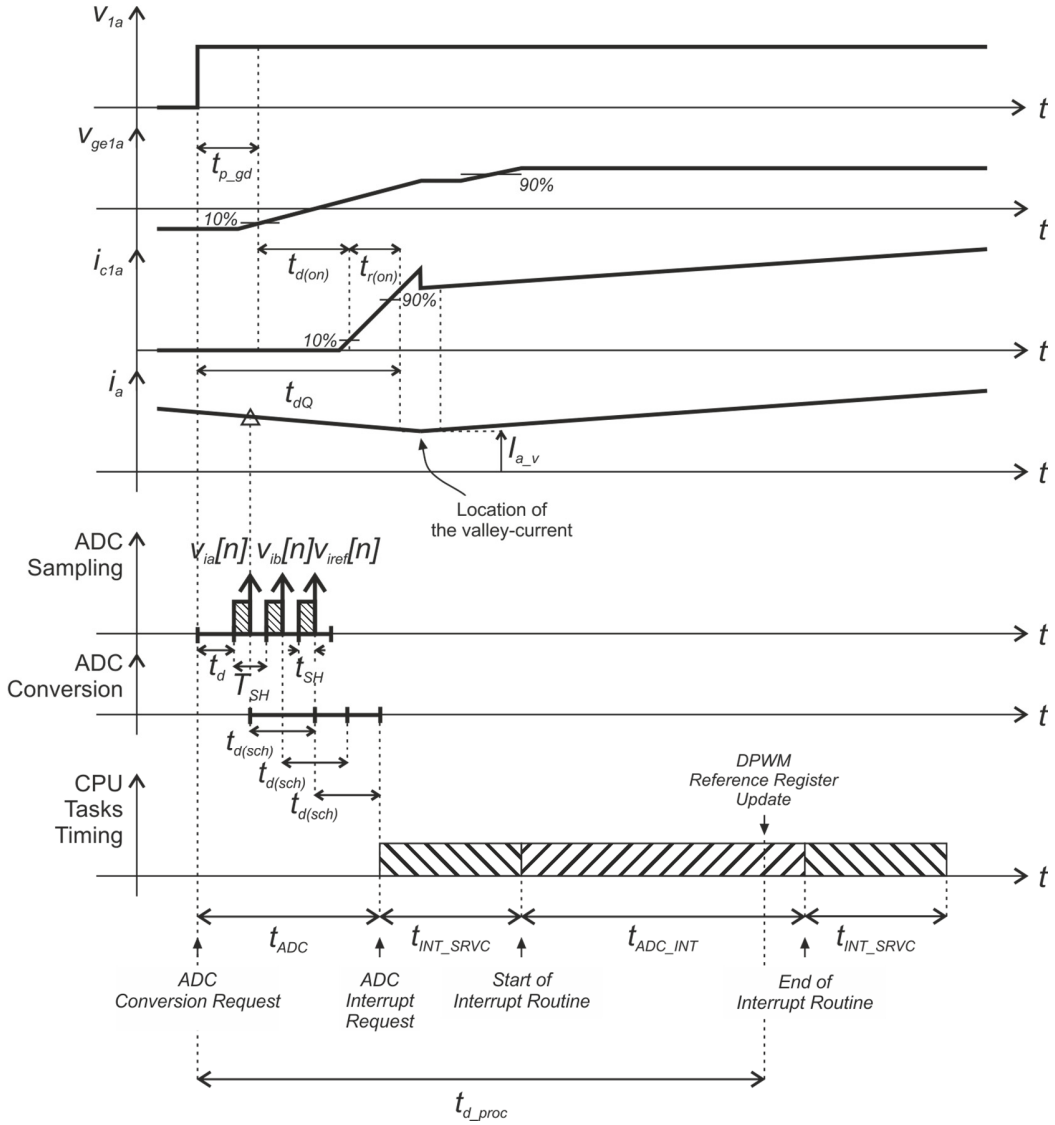

Figure 3.12. Timing diagram of the turn-on instant of the Q_{1a} transistor and the DSC modules for leading edge modulation or valley-current control.

$$t_{dQ} = t_{p\_gd} + t_{d(on)} + t_{r(on)} \tag{3.8}$$

At the same time as v_{1a} is set high, an ADC conversion-sequence is requested. The time delay from the moment that this request takes place to the start of the sampling-sequence is denoted t_d. During the sampling-sequence, each signal is sampled and coded with a uniform sampling period T_{SH} and an acquisition window of t_{SH}. The latency for the results of each conversion to appear in the registers of the ADC is denoted $t_{d(sch)}$. The total time taken by the ADC to complete the conversion-sequence is defined as the ADC conversion time, t_{ADC}, and may be calculated from Figure 3.12 as:

$$t_{ADC} = t_d + 2.5T_{SH} + t_{d(sch)} \tag{3.9}$$

Once the last result of the conversion is loaded into the result registers, the ADC module requests an interruption to the CPU which takes the necessary steps to run the ADC service routine. During this time, denoted t_{INT_SRVC}, the processor receives and determines the source of the interrupt request, approves the interrupt, executes context saving and prepares for the interrupt service routine [8]. The ADC interrupt service routine has a duration of t_{ADC_INT} seconds. During this time the new duty ratio of the corresponding phase is determined and loaded in the DPWM register. The duration of t_{ADC_INT} depends directly on the complexity of the controller compensation calculation. The length of time from the request of the ADC conversion sequence to the moment where the new duty-ratio is loaded in the DPWM registers is defined as the processing time delay, t_{d_proc}. After the ADC interrupt is finished, the CPU carries out the necessary steps to exit the service routine and to return to the main program. The length of time spent on these tasks is equal to t_{INT_SRVC} [8]. A list of the values of the times identified in Figure 3.12 can be found in Table 3.3.

Table 3.3. Value of the timings shown in Figure 3.11.

Parameter	Value
t_{p_gd}*	*85 ns*
$t_{d(on)}/t_{d(off)}$**	*350 ns/700 ns*
$t_{r(on)}/t_{f(off)}$**	*150 ns*
t_{dQ}	*585 ns*
t_d***	*100 ns*
T_{SH}***	*80 ns*
t_{SH}***	*40 ns*
$t_{d(sch)}$***	*160 ns*
t_{ADC}	*460 ns*
t_{INT_SRVC}****	Not specified
t_{ADC_INT}	Length depends on the complexity of the operations
$t_{d\_proc} = t_{ADC} + t_{INT\_SRVC} + t_{ADC\_INT}$	*460 ns* + $t_{INT\_SRVC} + t_{ADC\_INT}$

* As indicated in the gate-driver datasheet [5].
** As indicated in the CM300DU-12NFH IGBT datasheet [9].
*** As indicated in the TMS320F28335 manual [2].
**** [2, 8]

From Figure 3.12, it is evident that the sampling of the phase currents will not occur at the location of the valley-current due to the delayed turn on of the transistor Q_{1a} causing

a constant error which will not be detected by the control-loops. The magnitude of the error is variable and depends on the slope of the current waveform.

3.4.4. Average-current control with immediate DPWM update

In this variation of the average-current control, the configuration of the DPWM modules was modified to provide immediate access to the contents of the registers that contain the value of the duty-ratio in the DPWM modules. Employing this modification a new duty-ratio can be loaded immediately into the reference-register, eliminating the delay of the control loop caused by the DPWM module. However, the use of this mode of operation may generate spurious PWM waveforms under certain conditions.

For instance, consider the particular case illustrated in Figure 3.13(b) where the value of the duty-ratio calculated by the control algorithm in the n^{th}-*cycle* is smaller than the actual value of the DPWM counter. Under these circumstances, the counter will not cross over the value in the reference-register during the first half of the cycle. As a consequence v_{1a} will not be set-low causing an over-current fault. A simple way to prevent this issue is illustrated in the waveforms of Figure 3.13(c). Here, the minimum value of the duty-ratio is constrained to values that are higher than the value of the counter at the update instant. From Figure 3.13(c) it is evident that the value for the minimum constraint is directly related to the processing time of the control algorithm and the switching period of the converter, as shown by Equation (3.8):

$$D_{\min} = 2\frac{t_{d\_proc}}{T_{sw}} = \frac{4.2\mu s}{33.33\mu s} = 0.252 \approx 25\% \tag{3.8}$$

However, it is clear that this solution imposes a limit in the minimum range of operation that the converter can achieve, making it less attractive for applications where the converter is required to operate over the full-range of the duty-ratio, when the ratio of the processing time to the switching period is not small enough to meet the application requirements, or when a large number of converter phases is used.

Also, after testing this new configuration in conjunction with the control algorithm introduced in Section 3.4.3, an unexpected over-current fault was detected for duty-ratios

around *79 %*. A close-look at the fault-instants revealed that the transistor control-signals were being latched-on for a couple of switching cycles. Further analysis showed that these fault events occurred when a new duty-ratio was loaded into the DPWM modules at the same time instant that the other phase was changing state.

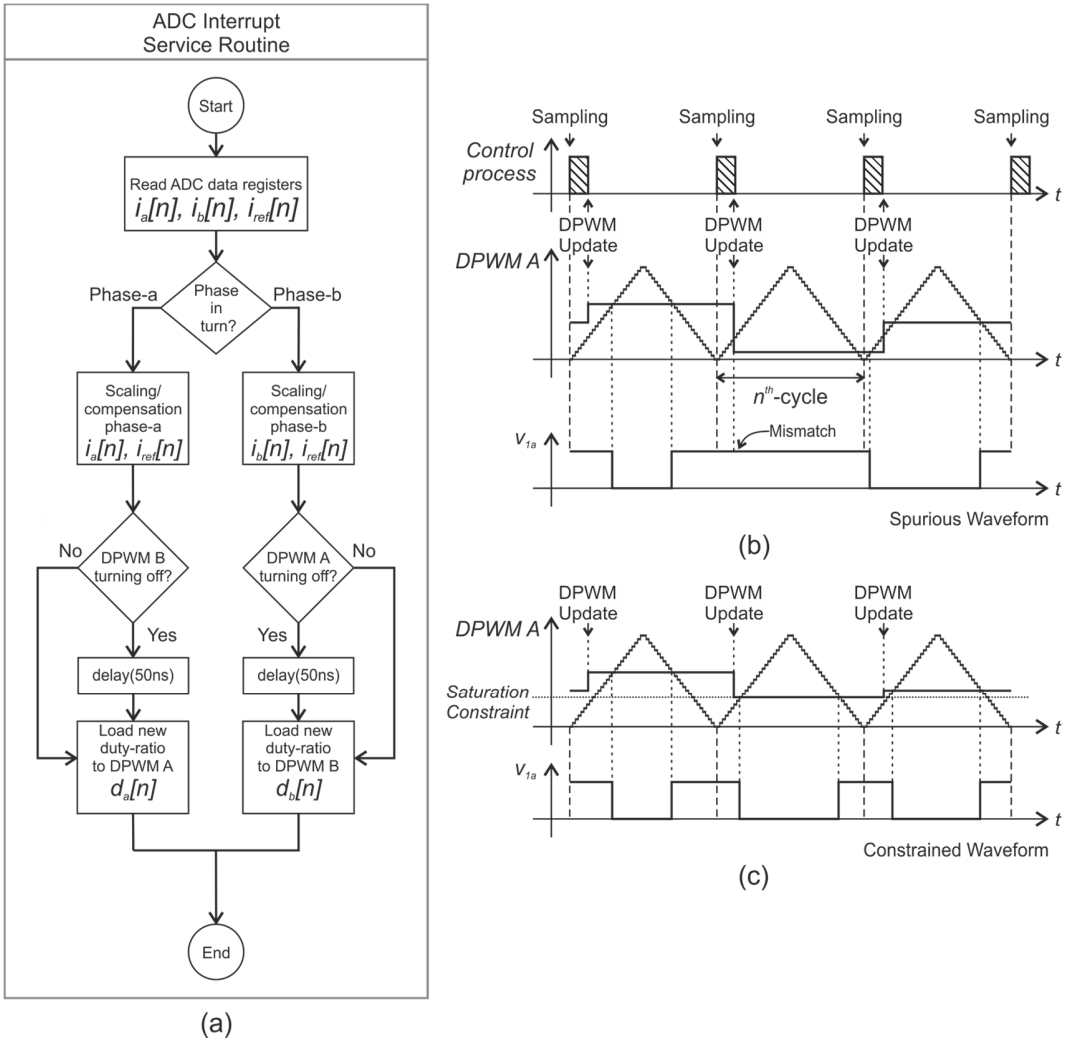

Figure 3.13. Average-current control with immediate DPWM update. (a) Control algorithm executed during the ADC interrupt service routine. (b) Time diagram illustrating the generation of spurious waveforms and how to avoid this issue by constraining the minimum value of the duty-ratio.

To overcome this issue, an "anti-glitch" stage was added to the control algorithm of Figure 3.11(a). The flowchart of this algorithm is illustrated in Figure 3.13(a). Compared with the normal-update version of the average-current control algorithm, this version includes a stage that prevents the DPWM reference register of one phase being updated at the same time as the opposite phase is being turned off. After performing this modification

the immediately updated PWM mode algorithm was able to operate correctly as demonstrated experimentally in Section 3.7.

3.5. SABER simulation models

Three simulation models were developed in SABER to investigate the behaviour of the DIBC with IPT in conjunction with the valley-, peak- and average-current control methodologies. These simulation models are based on the SABER switched model of the converter introduced in Chapter 2, Sections 2.4.2. To achieve an accurate simulation, the functionality of the modules employed in the DSC was rigorously replicated employing the functional blocks provided by SABER and also by programming special blocks specific for this application. The advantage of these models is that they accurately predict the behaviour of the control algorithms including the quantization effects of both the ADC and the DPWM modules, but at the cost of long simulation times, for instance a *100 ms* simulation will take about *40 min* to be completed. The SABER schematics of these models are depicted in Figures C.1 to C.6, Appendix C.

A fourth simulation model was specifically developed for the average-current control methodology. This simulation model makes use of the SABER average model of the converter developed in Chapter 2, Section 2.4.3. The control loops implemented in this model do not account for the quantization effects of the ADC and DPWM modules, thereby allowing a dramatic improvement in the simulation times at the cost of reduced accuracy, for example, a *100 ms* simulation will take about *3 min* to be completed. The SABER schematics of this model are depicted in Figures C.7 and C.8, Appendix C.

3.6. Results of the digital valley-current and peak-current control

The performance and operation of the control algorithms and control platform were verified using the converter prototype described in Sections 3.2. For all the experiments performed, the converter was powered using a *15 kW* dc power supply with maximum output voltage of *100 V* and maximum output current of *150 A*. A *48 kW* resistive load with selectable values of *2.6 Ω*, *3.8 Ω*, *5.2 Ω* and *10.4 Ω* was employed as the load. The gains of

the proportional integral current controller were selected by trial and error and were $K_p = 30T$ and $K_i = 1$ for both control strategies.

The simulation results presented were obtained using the SABER switched models developed for valley-current and peak-current control. The simulation parameters are listed in Table 3.4.

Table 3.4. Simulation parameters for valley-current and peak-current control.

Power Converter	
Input inductance at *60 kHz*, L_{in}	*5.12 µH*
Input inductor winding resistance at *60 kHz*, R_{in}	*0.029 Ω*
IPT windings self-inductance at *30 kHz*, L_a, L_b	*75.14 µH*
Coupling coefficient of the IPT windings, *k*	*0.997*
Output capacitance, C_o	*45 µH*
Load resistor, R_{load}	*5.2 Ω*
Switching delay, t_{dQ}*	*520 ns*
Digital Signal Controller	
Master clock frequency, f_{clk}	*150 MHz*
DPWM counters configuration	*Count up mode/Count down mode accordingly*
DPWM counter maximum value, v_{cmax}	*5000*
Sampling delay phase-a	*140 ns*
Sampling delay phase-b	*220 ns*
Processing delay, t_{d_proc}	*3.52 µs*
DPWM update delay	*One-cycle*

* As measured in Section 3.6.3. Includes the gate driver propagation delay, IGBT turn-on/turn-off delay, and the IGBT rise/fall time: $t_{dQ} = t_{p\_gd} + t_{d(on)} + t_{r(on)}$.

3.6.1. Steady-state operation of valley-current control strategy

Figures 3.14(a) and 3.14(b) show a comparison of the experimental and simulation results obtained using the valley-current control algorithm at the points of operation $D = 0.43$ and $D = 0.62$ respectively. The point of operation $D = 0.5$ was unattainable with this control strategy due to the non-linear behaviour of the phase-current ripple amplitude [10]. This issue is discussed with more detail in Section 3.6.4.

The waveforms plotted in these figures are the phase-a and phase-b switching signals, v_{1a} and v_{1b} respectively, the converter phase-a and phase-b currents, i_a and i_b respectively, the input inductor current, i_{Lin}, calculated as $i_{Lin} = i_a + i_b$ and the differential

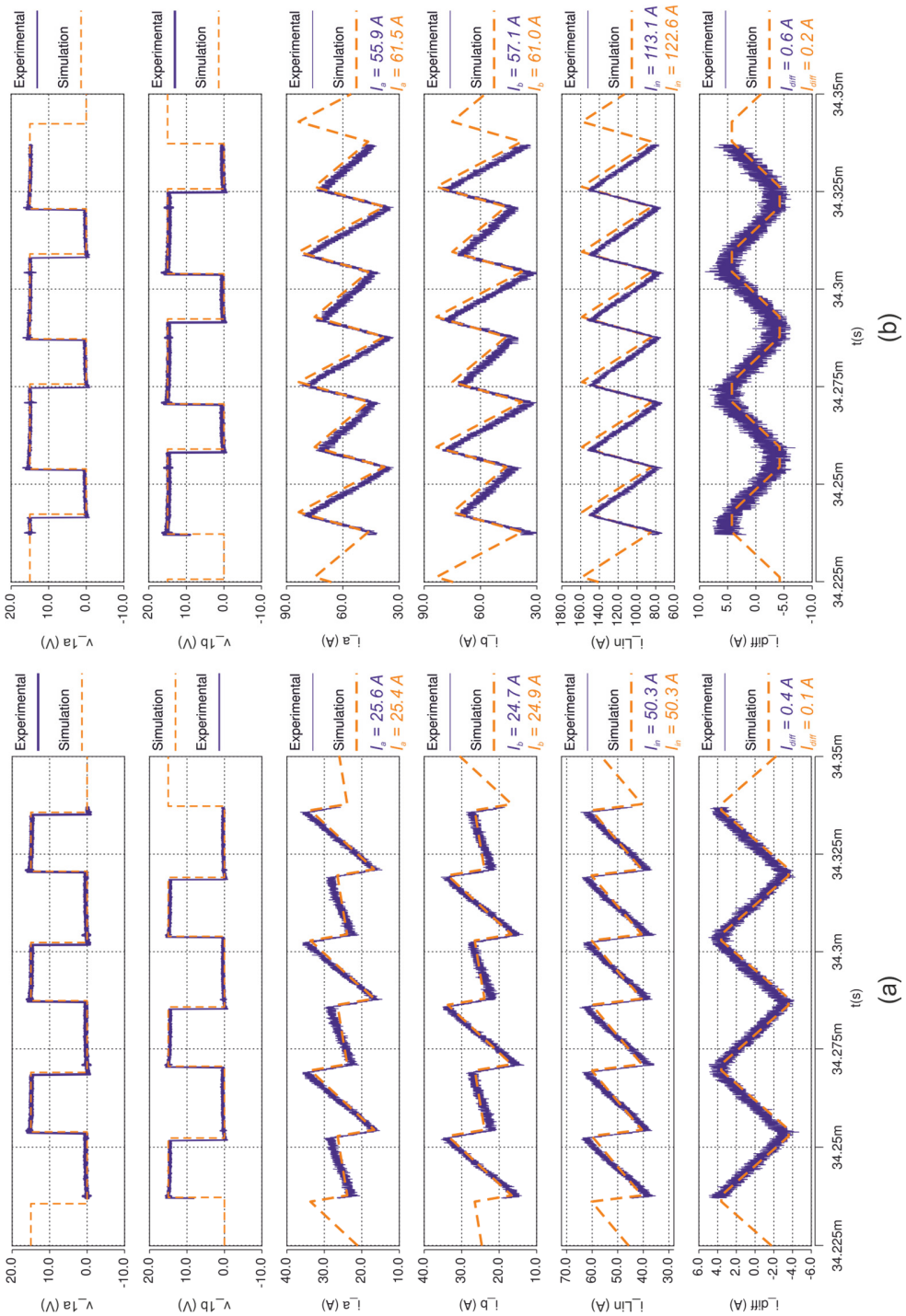

Figure 3.14. Experimental and simulation waveforms of the dual interleaved boost converter with IPT in steady state operation obtained employing the valley-current control algorithm. (a) I_{ref} = 20 A, D = 0.43; (b) I_{ref} = 40 A, D = 0.62. System conditions: V_{in} = 80 V; R_{load} = 5.2 Ω.

current, i_{diff}, calculated as $i_{diff} = \frac{1}{2}(i_a - i_b)$. Also, the average-values of the current waveforms presented are included below the legends of each plot. The results shown were obtained using a load resistance R_{load} of *5.2 Ω*, an input voltage V_{in} of *80 V* and a reference-current of *20 A* and *40 A*, Figures 3.14(a) and 3.14(b) respectively.

The experimental and the simulation results correspond closely and are in agreement with the theoretical waveforms presented in Figure 2.2, Chapter 2. A discrepancy in the duty-ratio of the experimental and the simulation waveforms can be observed. To quantify this difference, the duty-ratio of the driving signals were measured and summarized in Table 3.5. From this table the difference between the experimental and the simulation results was found to be of *2 %* for *D = 0.43* and *3 %* for *D = 0.62*. This discrepancy is attributed to delays in the control loop that were not taken into account in the simulation model, such as measurement delays of the current transducers for example.

Table 3.5. Comparison of the duty-ratio of the experimental and simulation results of the valley-current control algorithm (Figure 3.13).

Point of Operation	Reference valley-current	Experimental duty-ratio	Simulation duty-ratio	Experimental and simulation difference
D < 0.5	*20 A*	*43 %*	*45 %*	*2 %*
D > 0.5	*40 A*	*62 %*	*65 %*	*3 %*

Table 3.6 shows a comparison of the valley-current measured from both the experimental and simulation results of Figure 3.14(a) and 3.14(b). The relative error of these measurements with respect to the reference-current was calculated and is also included in this table. It is observed that the valley-current from both the experimental and the simulation results is generally smaller than the desired reference-current.

Table 3.6. Phase-current measurements of the experimental and simulation results of the valley-current control algorithm. (Figure 3.14).

Point of Operation	Reference valley-current	Experimental		Simulation	
		Phase-a I_{a_v} / %Err	Phase-b I_{b_v} / %Err	Phase-a I_{a_v} / %Err	Phase-b I_{b_v} / %Err
D < 0.5	*20 A*	*14.2 A / 28 %*	*16.7 A / 16 %*	*16.6 A / 17 %*	*16.6 A / 17 %*
D > 0.5	*40 A*	*33.8 A / 15 %*	*36.3 A / 9 %*	*37.8 A / 5.5 %*	*37.8 A / 5.5 %*

As explained in Section 3.5.2, this is attributed mainly to the turn-on delay of the transistors which produces a mismatch between the sampling instants and the location of the valley-current. Moreover, the errors from both the simulation and the experimental results are much smaller at high-current profiles since the difference between the valley-current and the desired reference-current is very similar over the whole range of operation.

A close look at the experimental data of Table 3.6 reveals an imbalance of *2.5 A* in the phase currents that is not evident in the simulation results. This is thought to be caused by the difference in the parameters of the switching devices which are likely to cause different delays in the turn-on instants. Also, other factors such as mismatch between the current sensor parameters may contribute as well. The current imbalance is reflected as a dc offset of approximately *-1 A* in the differential current.

Finally, from the data of Table 3.6, it is possible to observe that the error of the experimental results is generally larger than the error obtained with the simulation. This may be attributed to the tolerance of the components forming the conditioning stages and a variation of their parameters due to environmental conditions, mainly temperature.

3.6.2. Steady-state operation of the peak-current control strategy

In a similar way as in the previous section, Figure 3.15(a) and 3.15(b) show a comparison of the experimental and simulation results obtained with the peak-current control algorithm during steady-state operation. These figures show the waveforms obtained for the points of operation $D = 0.25$ and $D = 0.61$ respectively, with $R_{load} = 5.2\ \Omega$ and $V_{in} = 80\ V$. The reference-current was programmed at *25 A* in Figure 3.15(a), and *70 A* in Figure 3.15(b). The simulation parameters are listed in Table 3.4. The point of operation $D = 0.5$ was also unattainable with this control algorithm.

The simulation and experimental waveforms are in agreement with the theoretical waveforms in Chapter 2. In a similar way as in the previous section, Table 3.7 shows a comparison of the duty-ratios measured from the experimental and the simulation results, whilst Table 3.8 summarizes the peak-current measurements for the experimental and simulation waveforms and the relative error with respect to the reference-current.

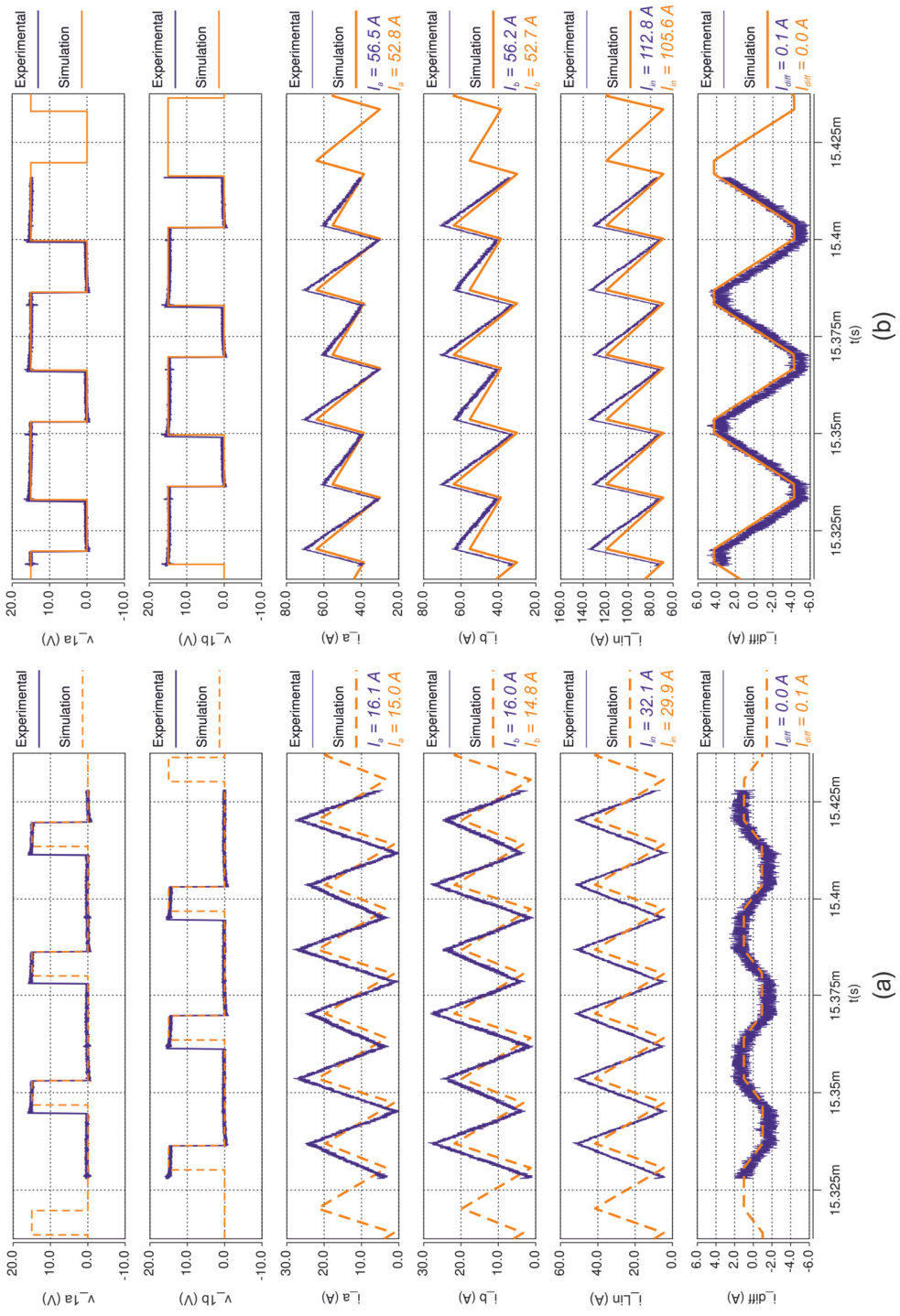

Figure 3.15. Experimental and simulation waveforms of the dual interleaved boost converter with IPT in steady state operation obtained employing the peak-current control algorithm. (a) I_{ref} = 20 A, D = 0.25; (b) I_{ref} = 60 A, D = 0.61. System conditions: V_{in} = 80 V; R_{load} = 5.2 Ω.

Table 3.7. Comparison of the duty-ratio of the experimental and simulation results of the peak-current control algorithm (Figure 3.15).

Point of Operation	Reference peak-current	Experimental duty-ratio	Simulation duty-ratio	Experimental and simulation difference
D < 0.5	*20 A*	*25 %*	*18 %*	*6 %*
D > 0.5	*60 A*	*61 %*	*60 %*	*1 %*

Table 3.8. Phase-current measurements of the experimental and simulation results of the peak-current control algorithm. (Figure 3.14).

Point of Operation	Reference peak-current	Experimental		Simulation	
		Phase-a I_{a_p} / %Err	Phase-b I_{b_p} / %Err	Phase-a I_{a_p} / %Err	Phase-b I_{b_p} / %Err
D < 0.5	*20 A*	*25.9 A / 29 %*	*26.8 A / 34 %*	*22.1 A / 10 %*	*21.5 A / 7.5 %*
D > 0.5	*60 A*	*69.0 A / 15 %*	*69.4 A / 15 %*	*62.6 A / 4.3 %*	*63.4 A / 5.6 %*

From Table 3.7 a difference in the experimental and simulation results of *6%* for *D = 0.25* and *1%* for *D = 0.61* is observed. From the data of Table 3.8, the peak-current obtained is generally larger than the reference-current, whilst the relative error shows a tendency to be smaller for the simulations. These results are consistent with the results obtained for the valley-current control algorithm shown in Table 3.6. Once again, the difference between the peak-current and the desired reference-current can be explained by the mismatch between the location of the sampling instants and the peak-current, which also have a repercussion in the duty-ratio discrepancy observed in Table 3.7. The imbalance between the phase currents was found to be approximately *1 A* for *D = 0.25* and for *D = 0.61*.

3.6.3. Timing of the control algorithms

To examine the processing time, t_{d_proc}, of the control algorithms and to estimate the location of the sampling instants on the phase-current waveforms, a digital output port of the DSC was programed to be set high at the start of the ADC interrupt service routine and to be cleared low when the new calculated duty-ratio was loaded into the DPWM registers. The square waveform generated by this port provides a way to measure the length of the interrupt service routine and will be denoted v_{timing}.

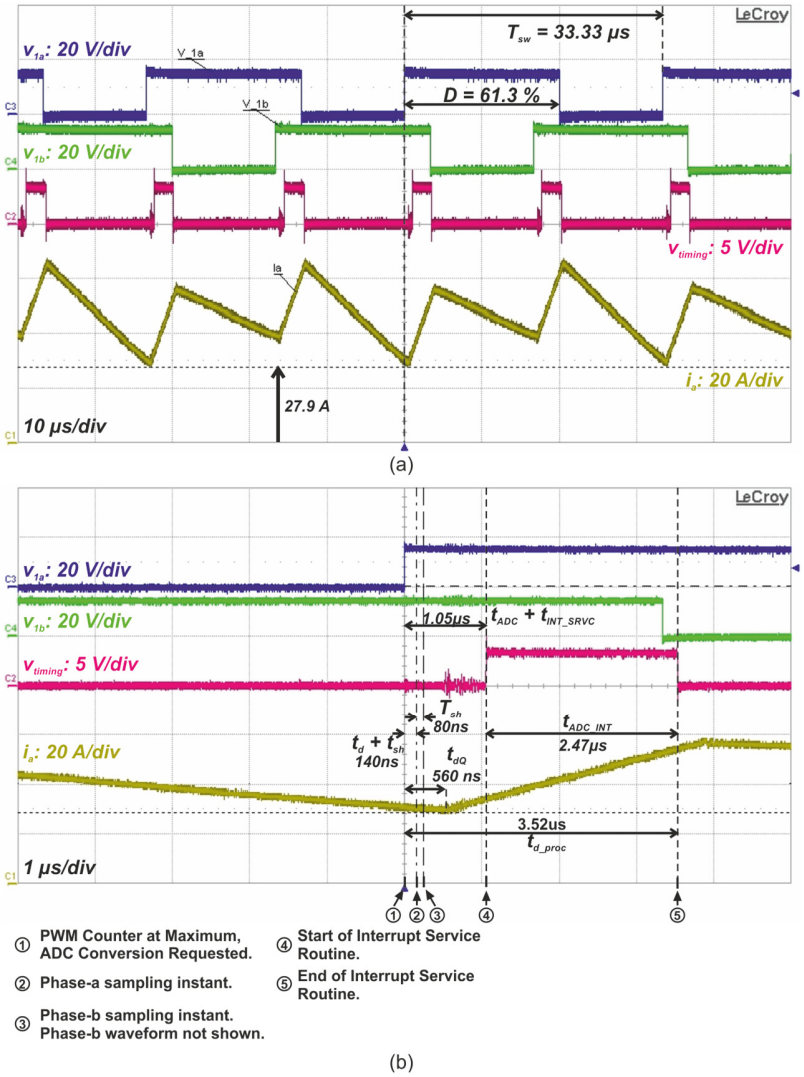

Figure 3.16. Experimental measurement of the processing time of the valley-current control. System conditions: V_{in} = 80 V; R_{load} = 5.2 Ω; D = 0.613, I_{Lin} = 101 A, V_o = 217 V. (a) Two complete cycles. (b) Expansion of the waveforms at the v_{1a} rising edge.

Figures 3.16 and 3.17 present the experimental waveforms measured for the valley-current and the peak-current control respectively. The results shown were acquired under steady-state operation by gradually adjusting the reference-current to achieve an average input current of *100 A*, which corresponds to a duty-ratio of approximately *63.1 %.* The system conditions employed were V_{in} = *80 V* and R_{load} = *5.2 Ω.* Each of these figures show two screen captures where four waveforms are depicted in the following order: the transistor driving signals, v_{1a} and v_{1b} respectively, v_{timing} and the phase-a current, i_a. The waveforms were arranged in a similar way to the theoretical waveforms shown in Figure 3.12, which were employed to analyse the timing of the control algorithms in Section 3.4.3.

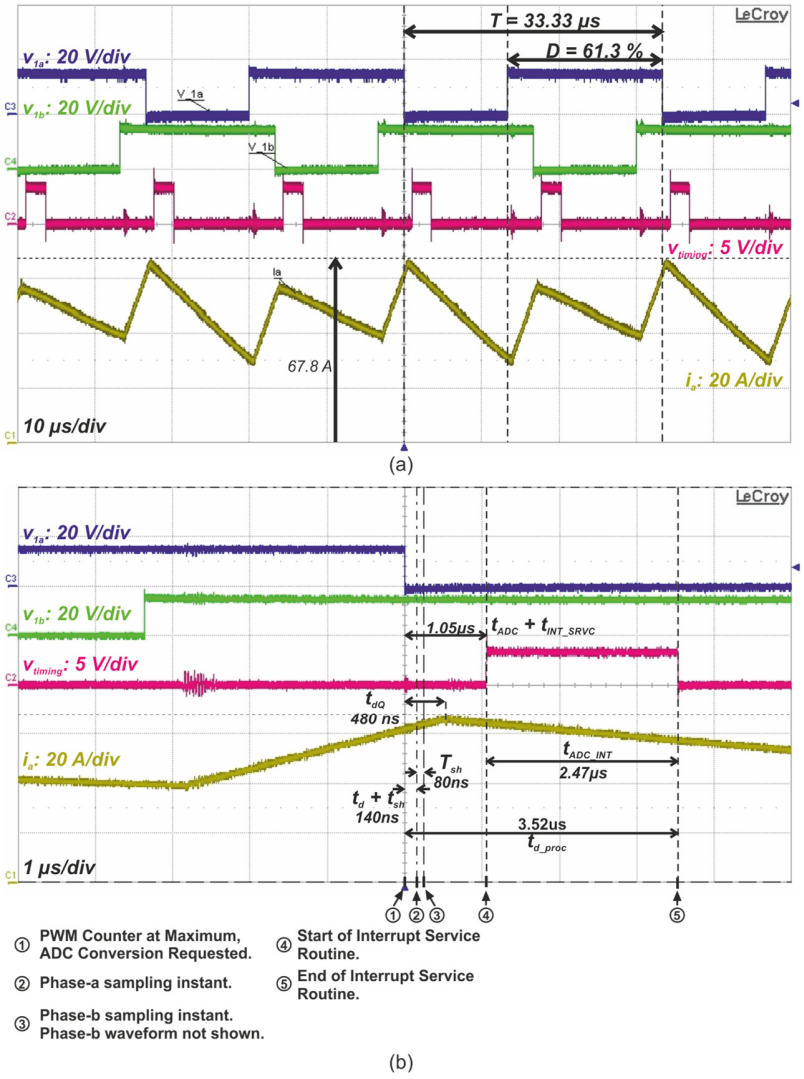

Figure 3.17. Experimental measurement of the processing time of the peak-current control. System conditions: V_{in} = 80 V; R_{load} = 5.2 Ω; D = 0.613, I_{Lin} = 101 A, V_o = 217 V. (a) Two complete cycles. (b) Expansion of the waveforms at the v_{1a} falling edge.

For the valley-current control algorithm, Figure 3.16(b) shows the waveforms at the turn-on instant of v_{1a}. Conversely for the peak-current control algorithm, Figure 3.17(b) shows an expansion of the waveforms at the turn-off instant of v_{1a}. The main events of the control process are denoted at the bottom of these figures with respect to the rising-edge or the falling-edge of v_{1a} accordingly. The sampling instants of the phase-a and phase-b currents denoted timing '2' and timing '3' were obtained from the DSC manual and occur at *140 ns* and 220 *ns* respectively, Table 3.3. From v_{timing} it is seen that the interrupt service routine starts at *1.05 µs* and that the calculated duty-ratio is loaded into the DPWM

registers at *3.52 µs*. The values of the principal timings in these figures are listed in Table 3.9. From the data collected it is seen that the total processing time, t_{d_proc}, is *3.5 µs* and is identical for both control algorithms as expected. Finally, the delay on the switching of the converter transistor, t_{dQ}, was measured to be approximately of *560 ns* for the turn-on and *480 ns* for the turn-off instants. From these measurements the mean value was calculated as *520 ns* and it is used to model both the turn-on and the turn-off delays of the ideal switches employed in the SABER switched model of the converter, Chapter 2.

Table 3.9. Experimental timings of the valley-current and the peak-current control algorithms.

Parameter	Time
$t_{ADC} + t_{INT\_SRVC}$	*1.05 µs*
t_{ADC}*	*460 ns*
t_{INT_SRVC}	*590 ns*
t_{comp}	*2.4 µs*
t_{d_proc}	*3.5 µs*
t_{dQ} **(Valley-current)**	*560 ns*
t_{dQ} **(Peak-current)**	*480 ns*

* As specified in the TMS320F28335 manual [2].

3.6.4. Range of operation

The range of operation of the valley-current and peak-current control algorithms was verified by gradually increasing the reference-current from *15 A* to the maximum value allowed by the power supply. This test revealed an uncontrollable region or dead-zone around the point of operation *D = 0.5*. To investigate further this characteristic, a set of simulations was run to evaluate the capability of the system to track a gradually increasing ramp reference-current. Since the control platform was not designed to follow arbitrary reference-currents, the study was carried out employing the SABER switched simulation models.

Each graph shown in Figure 3.18 depicts a comparison of the reference current, i_{ref}, and the phase-a current, i_a, on the first plot; a comparison of the sampled phase-a current, i_a*, and the sampled reference-current, i_{ref}* on the second plot; and the phase-a error-current, defined as i_{ea}* = i_{ref}* - i_a*, in the third plot. Figures 3.18(a), 3.18(b) and 3.18(c) were obtained employing the valley-current control strategy whilst the graphs shown in Figures 3.18(d), 3.18(e) and 3.18(f) were obtained using the peak-current control strategy.

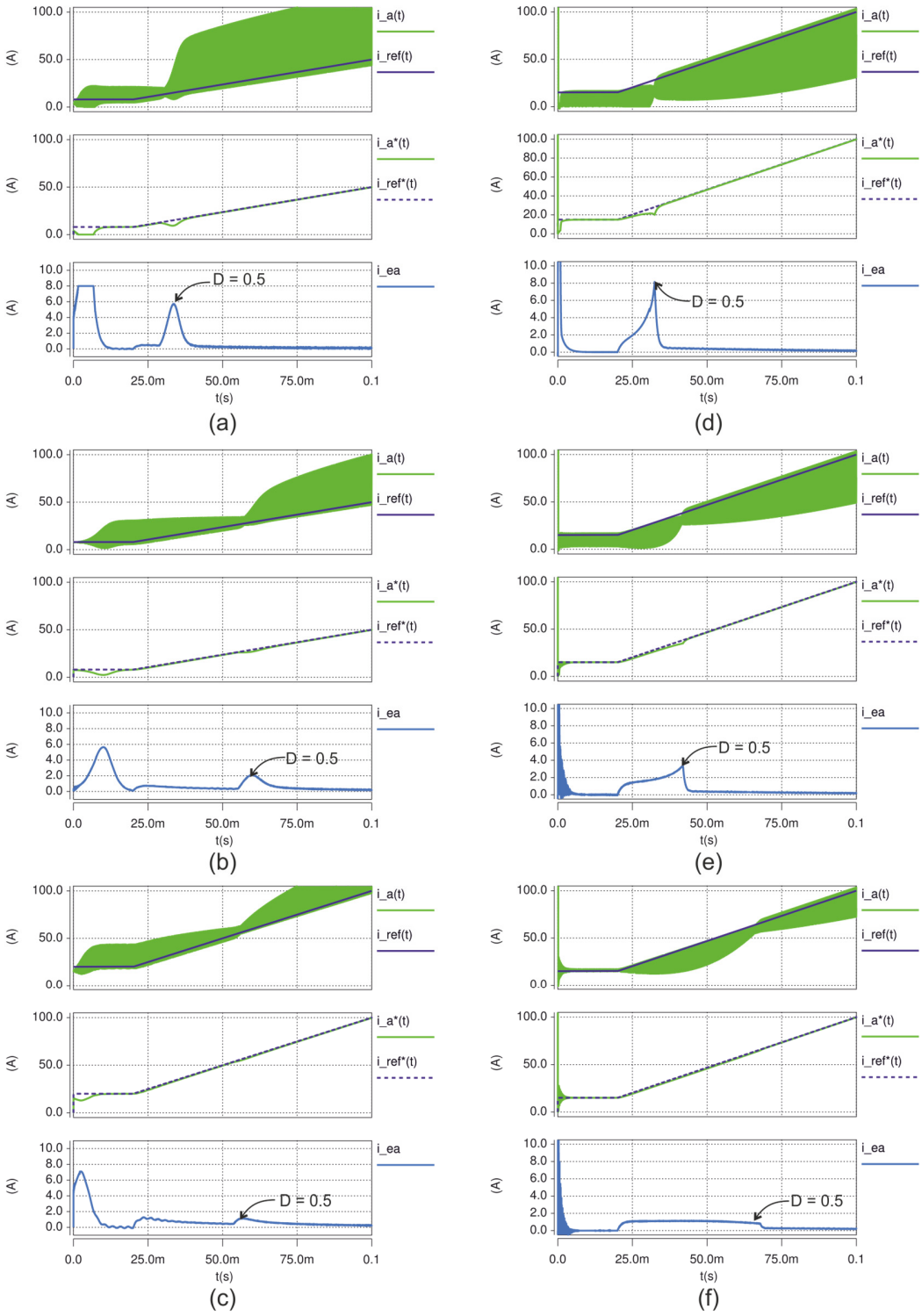

Figure 3.18. Response of the valley and peak current control algorithms to a ramp reference-current obtained by simulation. (a), (b) and (c) Valley-current control algorithm for R_{load} of *10.3 Ω, 5.2 Ω* and *2.6 Ω* respectively. (d), (e) and (f) Peak-current control algorithm for R_{load} of *10.3 Ω, 5.2 Ω* and *2.6 Ω* respectively. V_{in} = *80 V*.

As expected, all the plots show a constant error between the ramp-reference and the valley-current/peak-current, which is caused by the mismatch of the sampling instants caused by switching delay. However, it is also observed from i_{ea}* that the calculated error-current exhibits an increment for points or operation around *50%* of the duty-ratio (where the phase-current ripple is minimum). These uncontrollable regions are caused by the non-linear behaviour of the current-ripple and it is seen that they are reduced when the load is increased, Figures 3.18(c) and 3.18(f).

3.6.5. Dynamic performance

The experimental results presented in this section were gathered to evaluate the capability of the control algorithms to regulate and balance the phase-currents during a step-change in the reference-current and a step-change in the load. The results are organized as follows. For the valley-current control algorithm, Figures 3.19 and Figure 3.20 show the transient response of the system to a step-change in the reference-current and to a step-change in the load respectively. Likewise, Figures 3.21 and 3.22 show the transient responses of the system employing the peak-current control algorithm. Figures 3.19 to 3.22 comprise three scope-screen captures denoted (a), (b) and (c) respectively. (a), shows an overview of the transient response, (b) shows a magnification of the increasing current transient and (c) shows a magnification decreasing current transient. The relevant waveforms presented are the output voltage, v_o; the phase-a and phase-b currents shown one on top of the other, i_a and i_b respectively; and the differential current calculated as $i_{diff} = \frac{1}{2}(i_a - i_b)$. All the results were obtained with $V_{in} = 80\ V$. In addition, Figures 3.19 and 3.21, include an extra waveform plotted in green that was employed to synchronize the scope with the step-changes in the reference-current.

During the step-reference tests of the valley-current control algorithm, Figure 3.19, R_{load} was fixed to $5.2\ \Omega$ whilst i_{ref} was toggled between *20 A* and *40 A*. Conversely, during the step-load tests, Figure 3.21, i_{ref} was fixed at *40 A* whilst the load resistance was switched between $2.6\ \Omega$ and $5.2\ \Omega$. For the step-reference tests of the peak-current control, Figure 3.21, R_{load} was fixed to $5.2\ \Omega$ whilst i_{ref} was toggled between *20 A* and *70 A*, whilst for

the step-load tests i_{ref} was programmed at *60 A* and the load resistor was switched between *2.6 Ω* and *5.2 Ω*.

The results show in general a satisfactory performance. The differential and the phase-current waveforms show no evidence of saturation of the magnetic components and demonstrate the capability of the control strategies to maintain balanced currents in the converter phases even in transitory conditions. The transient times of the valley-current control were of approximately *30 ms* for the step-reference increment and *25 ms* for the step-reference decrement, whilst the transient times of the peak-current control were approximately of *25 ms* for the step-reference increment and *35 ms* for the step-reference decrement. The transient speeds are similar in both algorithms as the PI compensators used to regulate the current loops are equal for both control methodologies.

Finally, the step-load tests of both control algorithms, the phase current waveforms show a particular feature where the current seems to evolve in stages which is attributed to the non-instantaneous switching of the resistor bank.

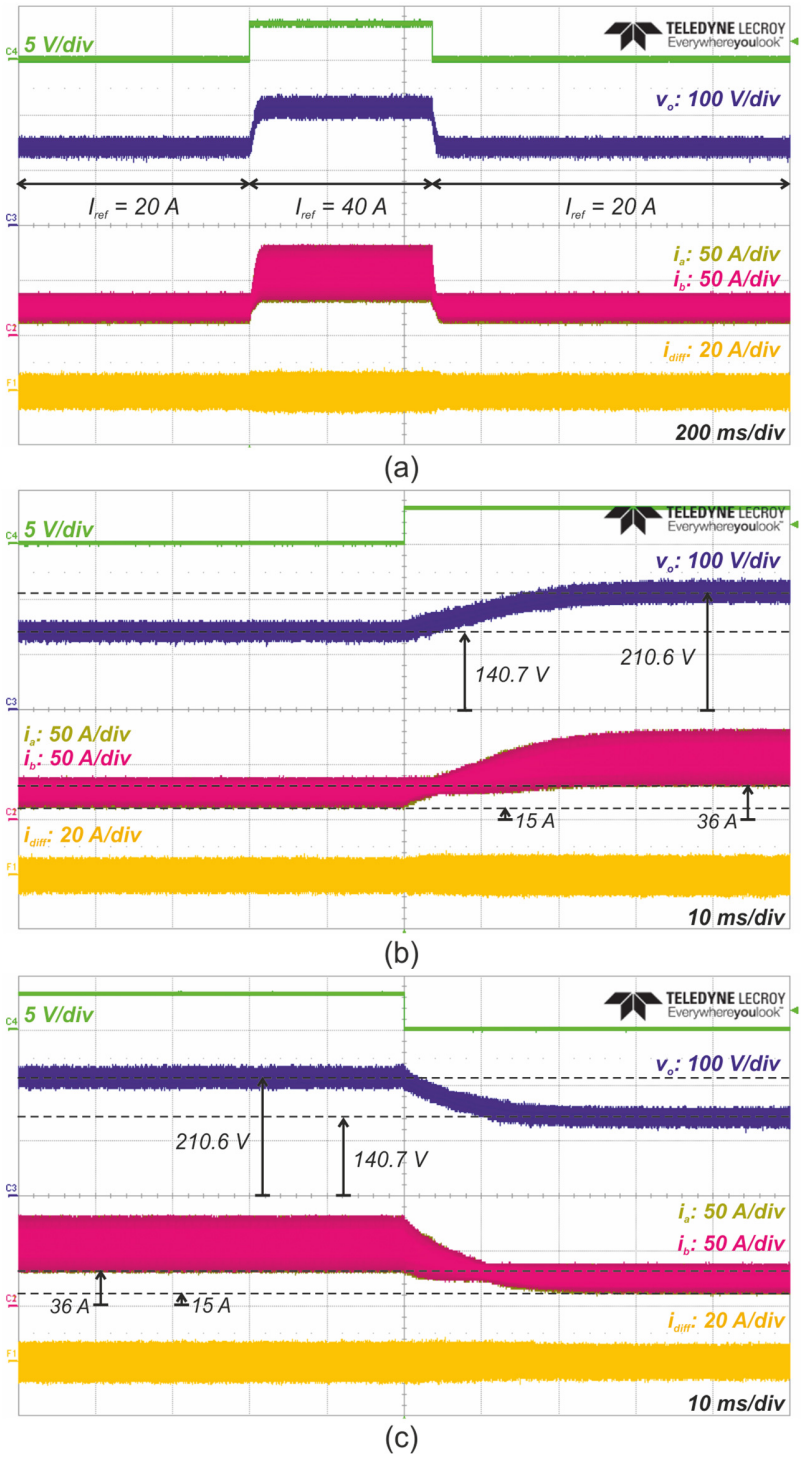

Figure 3.19. Experimental results of the step-reference response of the valley-current current control. System conditions: I_{ref1} = 20 A, I_{ref2} = 40 A, V_{in} 80 V, R_{load} = 5.2 Ω. (a) Overview of the test. (b) Magnification of the step-up transient. (c) Magnification of the step-down transient.

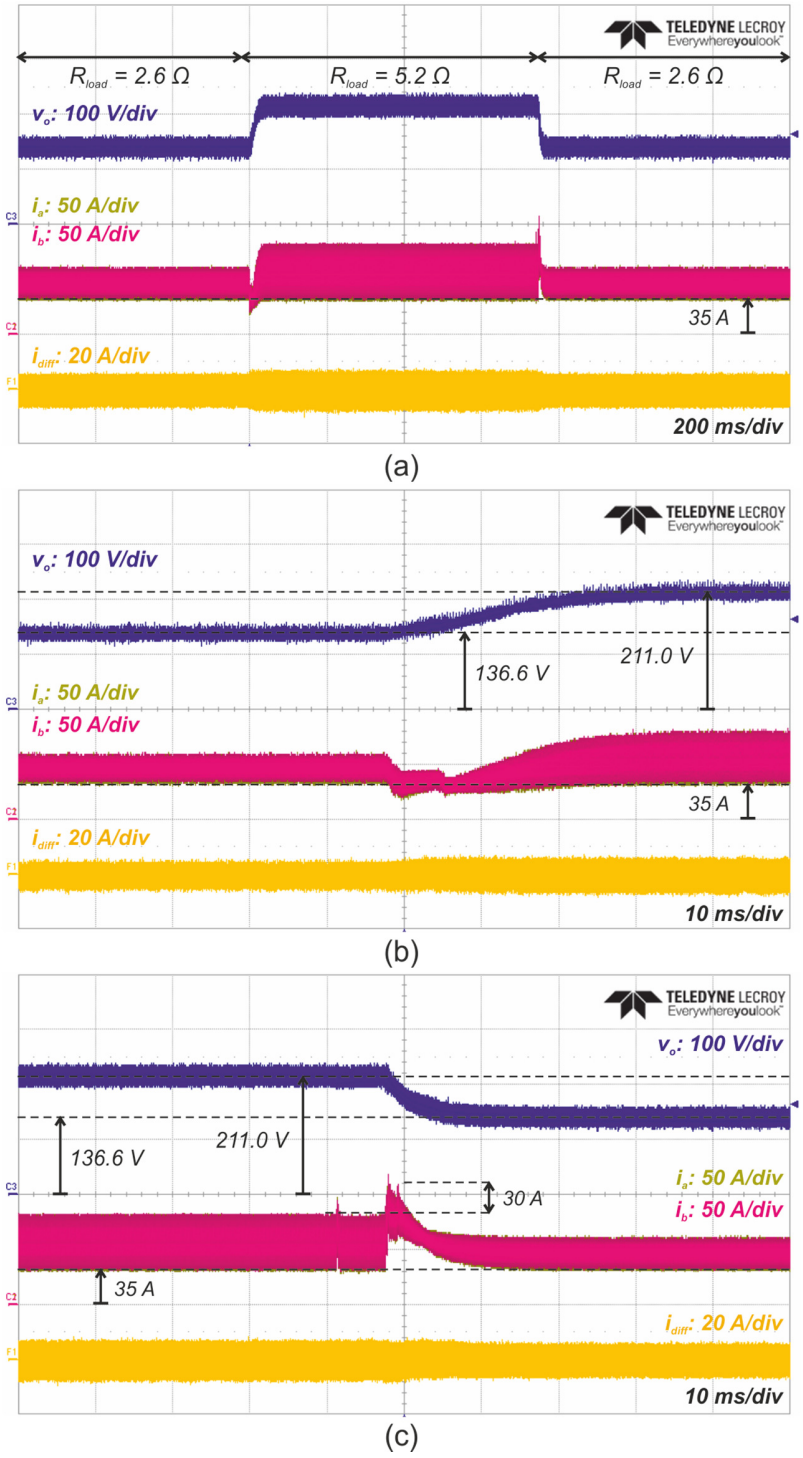

Figure 3.20. Experimental results of the step-load response of the valley-current current control. System conditions: I_{ref} = 40 A, V_{in} 80 V, R_{load1} = 2.6 Ω, R_{load2} = 5.2 Ω. (a) Overview of the test. (b) Magnification of the step-up transient. (c) Magnification of the step-down transient.

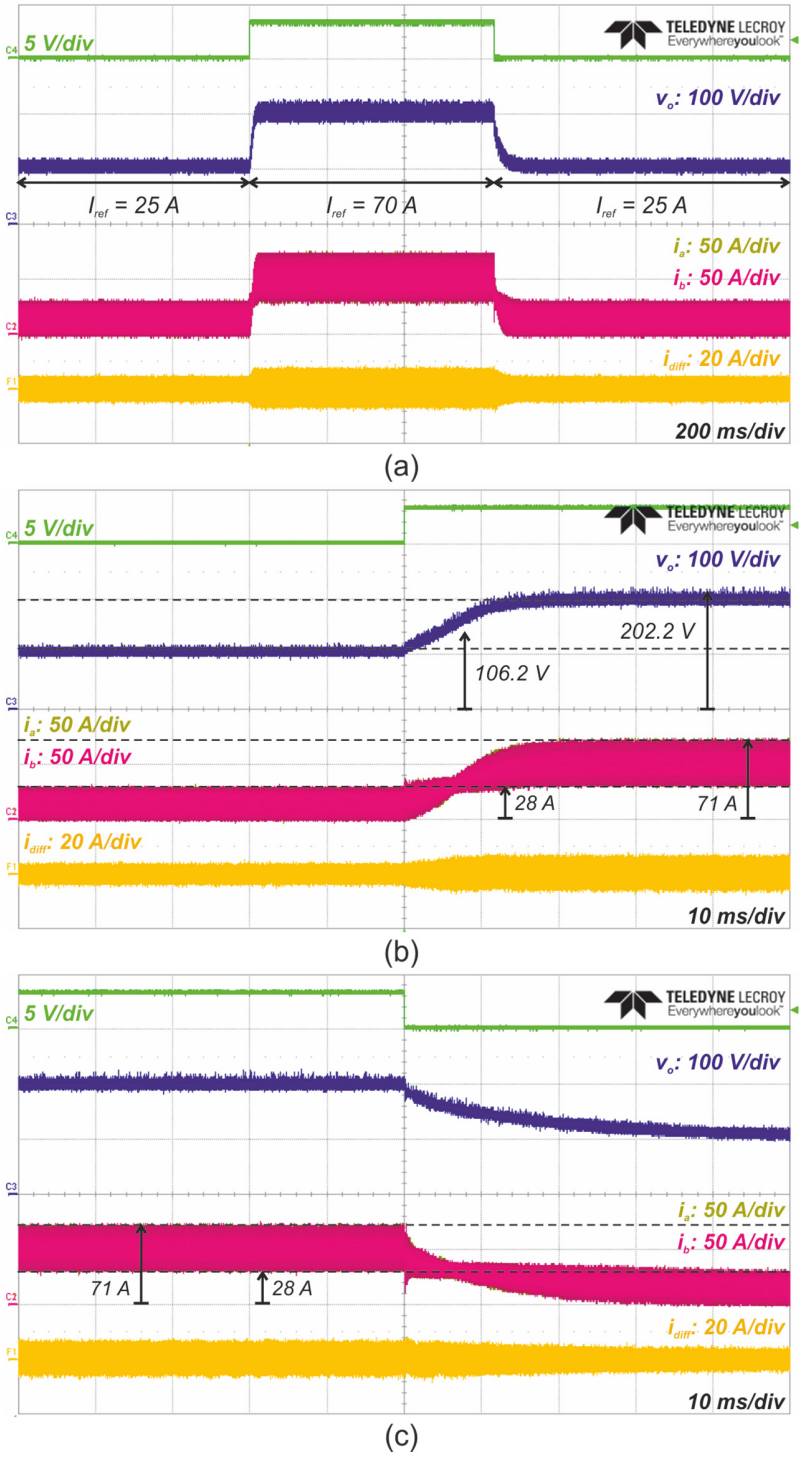

Figure 3.21. Experimental results of the step-reference response of the peak-current current control. System conditions: I_{ref1} = 20 A, I_{ref2} = 60 A, V_{in} 80 V, R_{load} = 5.2 Ω. (a) Overview of the test. (b) Magnification of the step-up transient. (c) Magnification of the step-down transient.

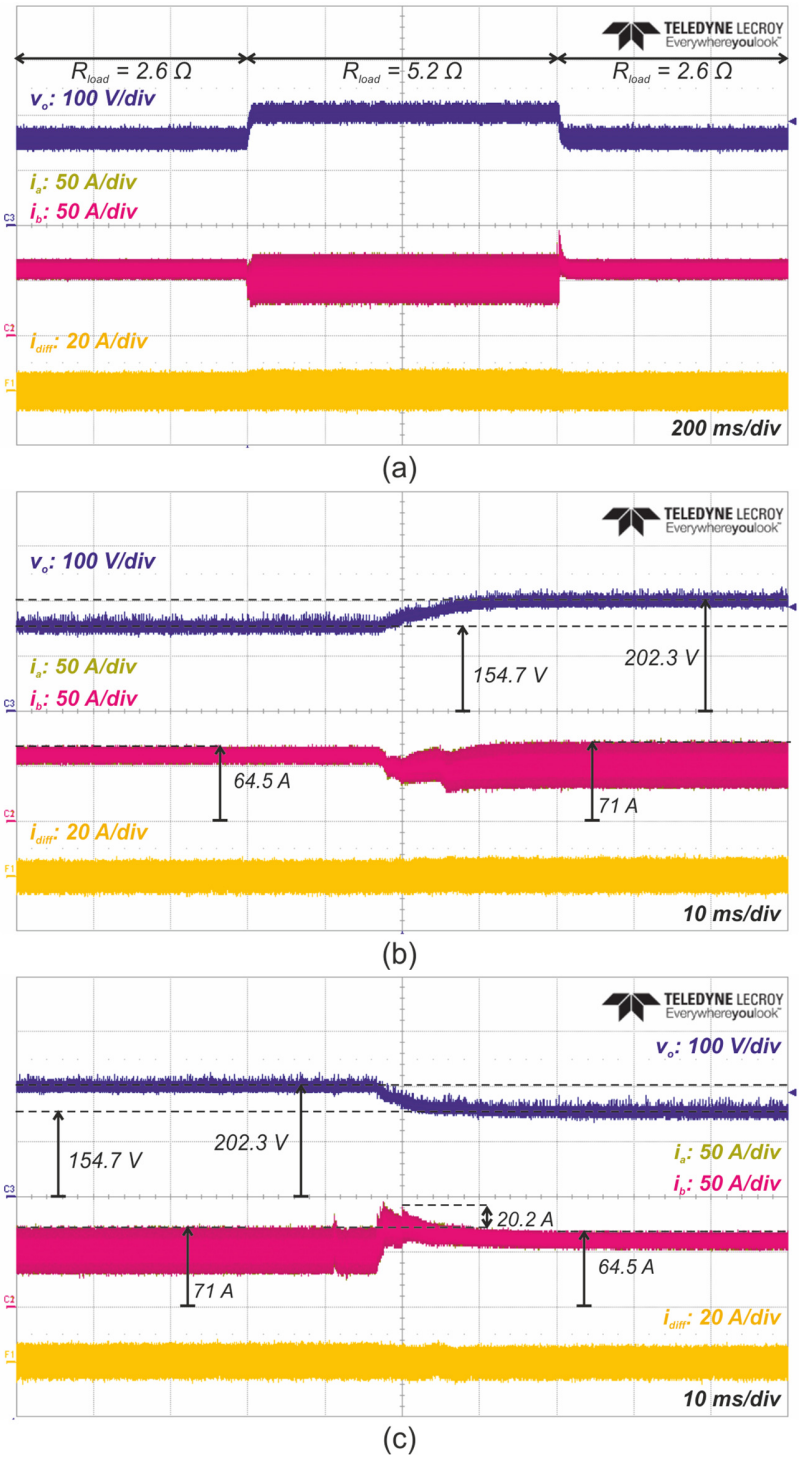

Figure 3.22. Experimental results of the step-load response of the peak-current current control. System conditions: I_{ref} = 60 A, V_{in} 80 V, R_{load1} = 2.6 Ω, R_{load2} = 5.2 Ω. (a) Overview of the test. (b) Magnification of the step-up transient. (c) Magnification of the step-down transient.

3.7. Results of the digital average-current control strategies with normal and immediate update

In this section, the performance and operation of the average-current control with normal update and with immediate update are presented. The experimental results were obtained employing the converter prototype and the control platform previously introduced in Sections 3.2 and Section 3.3. The simulation results were obtained using the SABER switched model developed for triangular-carrier modulation and the parameters listed in Table 3.10.

Table 3.10. Simulation parameters average-current control.

Power Converter	
Input inductance at *60 kHz*, L_{in}	*5.12 µH*
Input inductor winding resistance at *60 kHz*, R_{in}	*0.029 Ω*
IPT windings self-inductance at *30 kHz*, L_a, L_b	*75.14 µH*
Coupling coefficient of the IPT windings, *k*	*0.997*
Output capacitance, C_o	*45 µH*
Load resistor, R_{load}	*5.2 Ω*
Switching delay, t_{dQ}*	*520 ns*
Digital Signal Controller	
Master clock frequency, f_{clk}	*150 MHz*
DPWM counters configuration	*Count up-down mode*
DPWM counter maximum value, v_{cmax}	*2500*
Sampling delay phase-a	*140 ns*
Sampling delay phase-b	*220 ns*
Processing delay, t_{d_proc}	*4.2 µs*
DPWM update delay	*Half-cycle for normal update algorithm* *None for immediate update algorithm*

* As measured in Section 3.6.3. Includes the gate driver propagation delay, IGBT turn-on/turn-off delay, and the IGBT rise/fall time: $t_{dQ} = t_{p\_gd} + t_{d(on)} + t_{r(on)}$.

The converter power stage was powered using a *15 kW* dc power supply with maximum output voltage of *100 V* and maximum output current of *150 A*. A resistor bank of *48 kW* with selectable values of *2.6 Ω*, *3.8 Ω*, *5.2 Ω* and *10.4 Ω* was employed as the load. The gains of the digital PI compensator employed during the experiments were $K_p = 30T$ and $K_i = 1$ for the normal update algorithm and $K_p = 30T$ and $K_i = 10$ for the immediate update algorithm. These gains were selected using the simplified non-interleaved model of the converter described in Chapter 4 in conjunction with SISO tool in MATLAB to guarantee the

stability of the converter. The integral gain selected was the maximum possible before the system became unstable, however, these values were not properly designed and may affect how much better the immediate update method appears.

3.7.1. Steady-state operation

The results obtained with the average-current control algorithm with normal update and the variation employing immediate update showed virtually no difference in the steady-state results. For this reason, only the results obtained for the control algorithm with immediate update are presented in this section. Figures 3.23(a), 3.23(b) and 3.24 show a comparison of the measured experimental waveforms and the simulation results of the converter operating in continuous conduction mode and with $V_{in} = 80\ V$ and $R_{load} = 5.2\ \Omega$. Figures 3.23(a) and 3.23(b) show the results obtained for the points of operation $D = 0.43$ and $D = 0.61$, which were obtained by programming i_{ref} to $20\ A$ and $60\ A$ respectively. Figure 3.24 shows the results at $D = 0.5$. This particular point of operation was achieved by gradually increasing the reference-current until the system reached the desired duty-ratio. The waveforms plotted in these figures are the gate-driver signals, v_{1a} and v_{1b}, the phase currents, i_a and i_b, the input current, i_{Lin}, and finally the differential current, i_{diff}. In a similar way as for the valley and peak control strategies, Table 3.11 and 3.12 summarize the key aspects of the experimental and simulation waveforms.

Table 3.11. Comparison of the duty-ratio of the experimental and simulation results of the average-current control algorithm with immediate update (Figures 3.23 and 3.24).

Point of Operation	Reference peak-current	Experimental duty-ratio	Simulation duty-ratio	Experimental and simulation difference
D < 0.5	*20 A*	*43.9 %*	*39.2 %*	*4.7 %*
D = 0.5	*≈ 30 A*	*50.1 %*	*49.8 %*	*0.2 %*
D > 0.5	*50 A*	*61.8 %*	*61.3 %*	*0.7 %*

In general, the experimental and simulation results show a good correlation. The waveforms measured are in agreement with the theoretical expectation presented in Figure 2.2, Chapter 2. The practical values of the duty-ratio are slightly larger than those obtained in the simulation. From the measurements of Table 3.11 it is seen that the maximum difference between the experimental and the simulation duty-ratios is about *4.7 %* and it

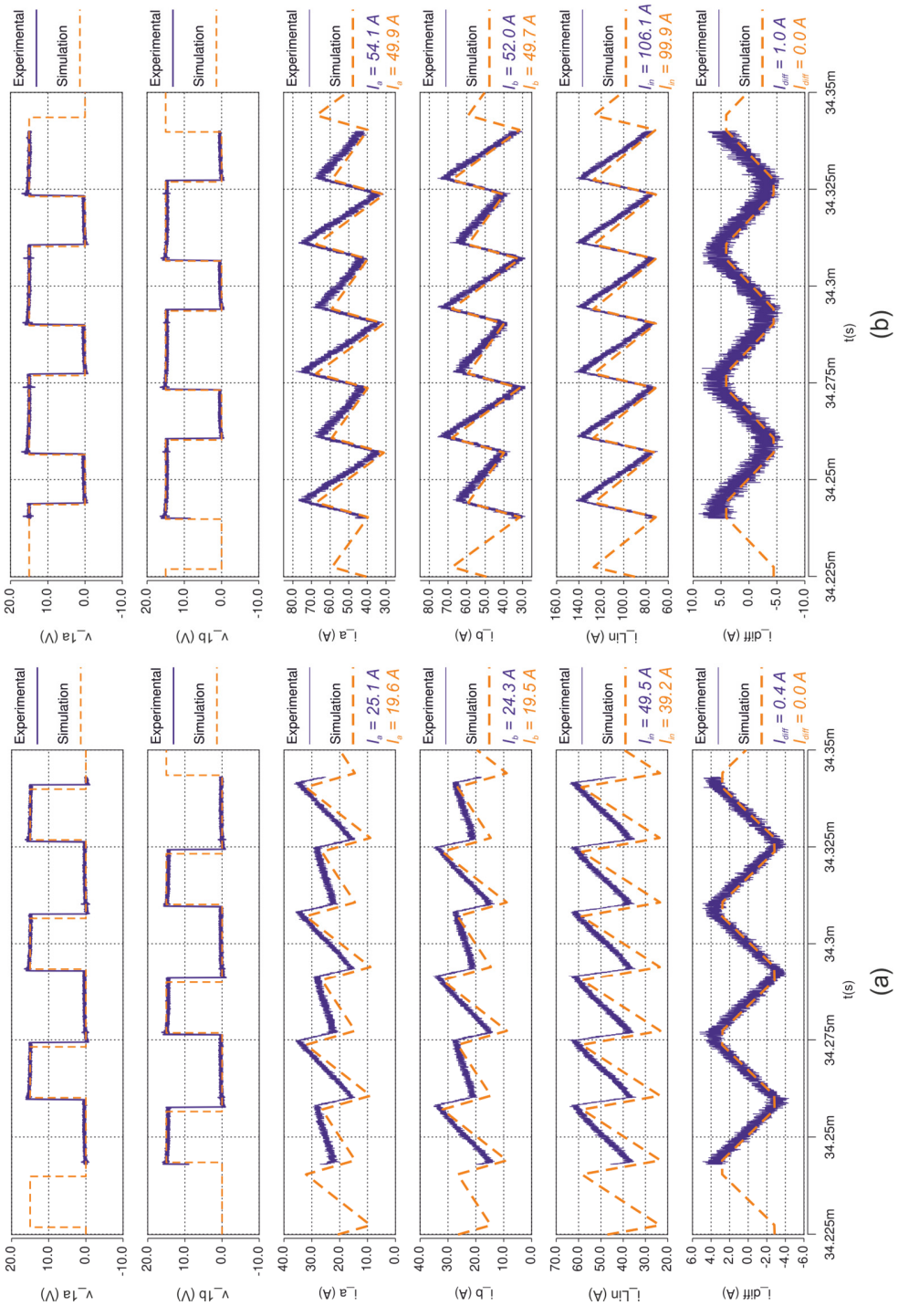

Figure 3.23. Experimental and simulation waveforms of the dual interleaved boost converter with IPT in steady state operation obtained employing the immediate update average-current control algorithm. (a) I_{ref} = 20 A, D = 0.43; (b) I_{ref} = 50 A, D = 0.61. System conditions: V_{in} = 80 V; R_{load} = 5.2 Ω.

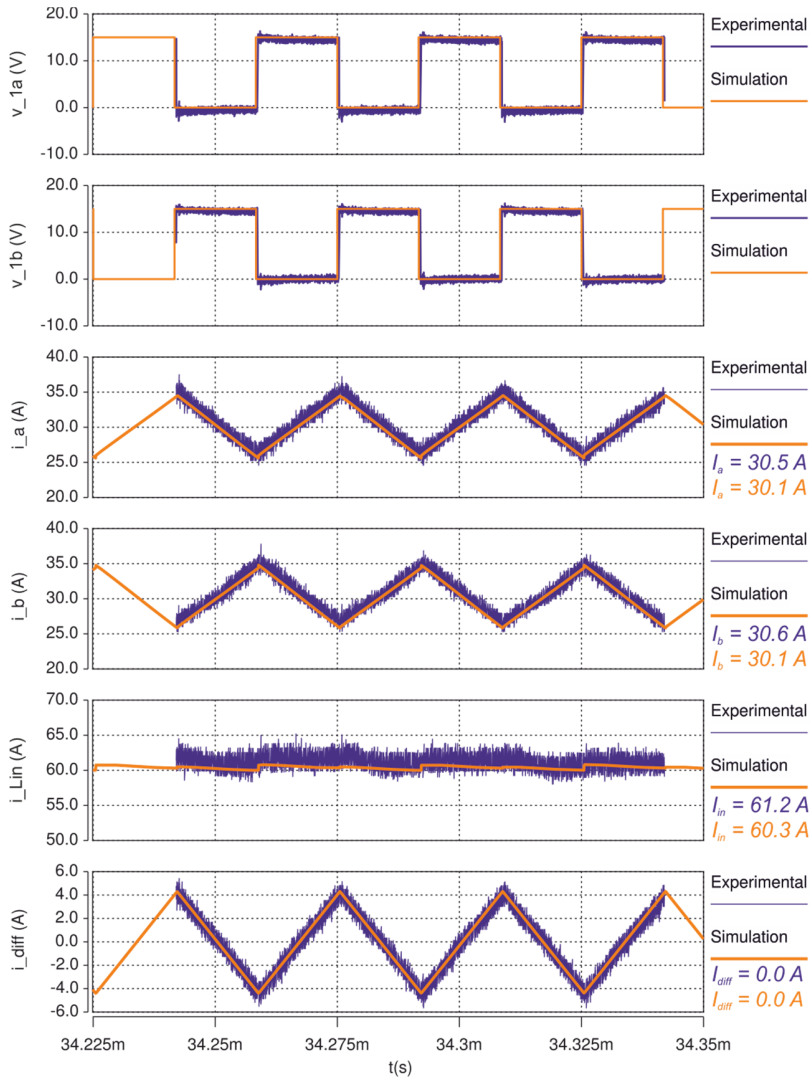

Figure 3.24. Experimental and simulation waveforms of the dual interleaved boost converter with IPT in steady state operation obtained employing the immediate update average-current control algorithm. I_{ref} = 30 A. D = 0.5. Svstem conditions: V_{in} = 80 V: R_{load} = 5.2 Ω.

seems to diminish as the duty-ratio is increased (the value at *D = 0.5* is the smallest as the reference-current was adjusted to set the converter in that point of operation). This difference is attributed to the slight mismatches in component parameters, and non-ideal elements of the converter as well as the turn-on and turn-off delays of the transistors.

The practical average level of the phase-currents is generally above the value obtained with the simulations, Table 3.12. The difference found was of about *5 A* between the experimental and simulation values. Once more this is attributed to the mismatch between the sampling instants and the actual point where the average-current is located which are a consequence of the delay in the control signals and the switching devices.

From Table 3.12, an imbalance in the average-value of the phase current waveforms is observed of about *1 A* for *D = 0.43* and *2 A* for *D = 0.61*. This is reflected as a dc offset of *0.4 A* and *1 A* respectively in the differential current of the system. The cause of this imbalance is likely to be related to the mismatches in the parameters of the converter and control platform and stray parasitic elements.

Table 3.12. Phase-current measurements of the experimental and simulation results of the average-current control algorithm with immediate update. (Figures 3.23 and 3.24).

Point of Operation	Reference peak-current	Experimental		Simulation	
		Phase-a I_{a_p} / Err	Phase-b I_{b_p} / Err	Phase-a I_{a_p} / Err	Phase-b I_{b_p} / Err
D < 0.5	*20 A*	*25.1 A / 25 %*	*24.3 A / 21 %*	*19.6 A / 2 %*	*19.5 A / 2 %*
D = 0.5	*≈ 30 A*	*30.5 A / 1.6%*	*30.6 A / 2 %*	*30.1 A / 0.3 %*	*30.1 A / 0.3 %*
D > 0.5	*50 A*	*54.1 A / 8 %*	*52.0 A / 4 %*	*49.9 A / 0.2 %*	*49.7 A / 0.3 %*

In conclusion, the results obtained confirm the correct operation of the control algorithms in steady-state and validate the correct operation of the SABER switched simulation model.

3.7.2. Timing of the control algorithms

Figures 3.25 and 3.26 illustrate the waveforms used to measure the processing time, t_{d_proc}, and estimate the location of the sampling instants for the average-current control algorithm with normal update and with immediate update. The waveforms shown in these figures correspond to the point of operation *D = 63.1%*. The system conditions were V_{in} = *80 V* and R_{load} = *5.2 Ω*. The waveforms displayed in these figures are the transistor driving signals v_{1a} and v_{1b}, the signal used to measure the processing time, v_{timing}, and the phase-a current i_a. The main events of the control process are denoted at the bottom of these figures. The sampling instants of the phase-a and phase-b currents denoted timing '2' and timing '3' were obtained from the DSC manual and occur at *140 ns* and 220 *ns* respectively, Table 3.3.

Table 3.13 summarizes the key measurements from the waveforms. For the average-current control algorithm with normal update, the computation time of the control algorithm was found to be of *2.3 μs* and the total processing time was *3.35 μs* which is

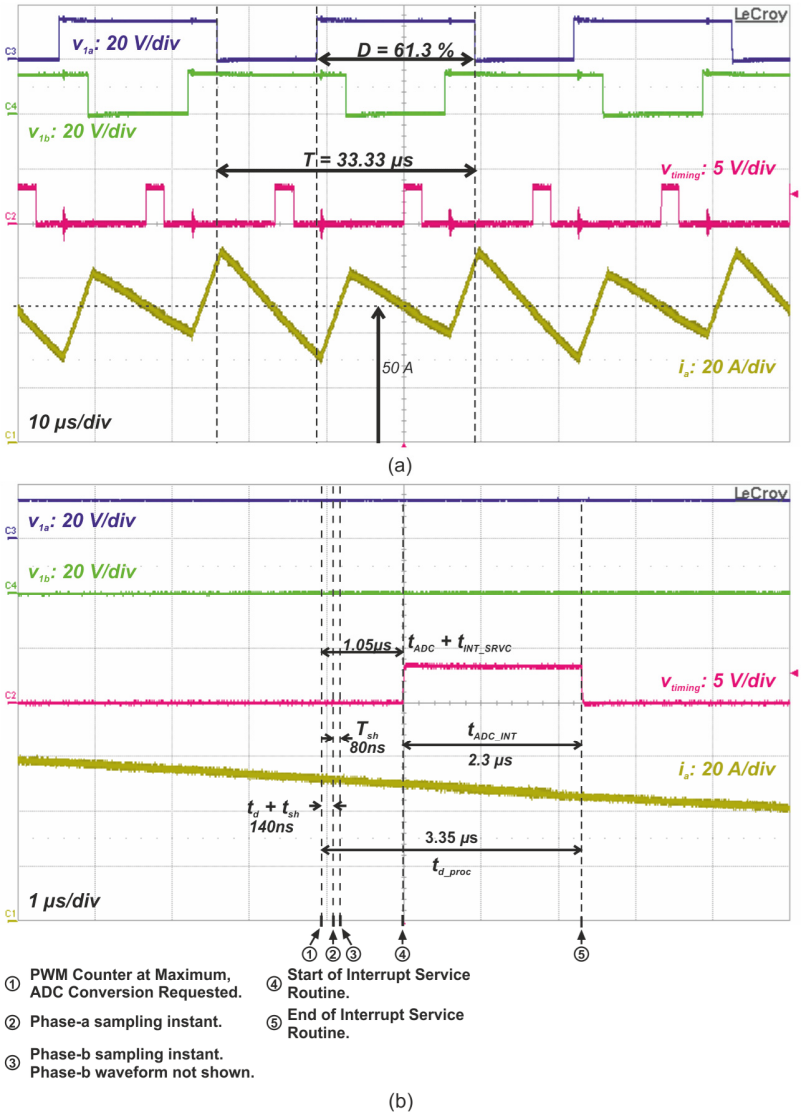

Figure 3.25. Experimental measurement of the processing time of the average-current control with normal update. System conditions: V_{in} = 80 V; R_{load} = 5.2 Ω; D = 0.613, I_{Lin} = 101 A, V_o = 217 V. (a) Two complete cycles. (b) Expansion of the waveforms at the v_{timing} rising edge.

Table 3.13. Experimental timings of the average-current control algorithm with normal and immediate update.

Parameter	Time
t_{ADC} + t_{INT_SRVC}	1.05 µs
t_{ADC}*	460 ns
t_{INT_SRVC}	590 ns
t_{comp} (normal algorithm)	2.3 µs
t_{d_proc} (normal algorithm)	3.35 µs
t_{comp} (immediate algorithm)	3.15 µs
t_{d_proc} (immediate algorithm)	4.2 µs

* As specified in the TMS320F28335 manual [2].

170 ns shorter than that of the valley-current and peak-current algorithms, Table 3.9. On the other hand, the computation time for the algorithm with immediate update was found to be *3.15 μs*, which is approximately *1 μs* longer than the normal update algorithm, as expected, due to the extra-tasks carried out for the anti-glitch scheme described in Section 3.4.4. Consequently, the total processing time of the immediate update algorithm was found to be *4.2 μs*.

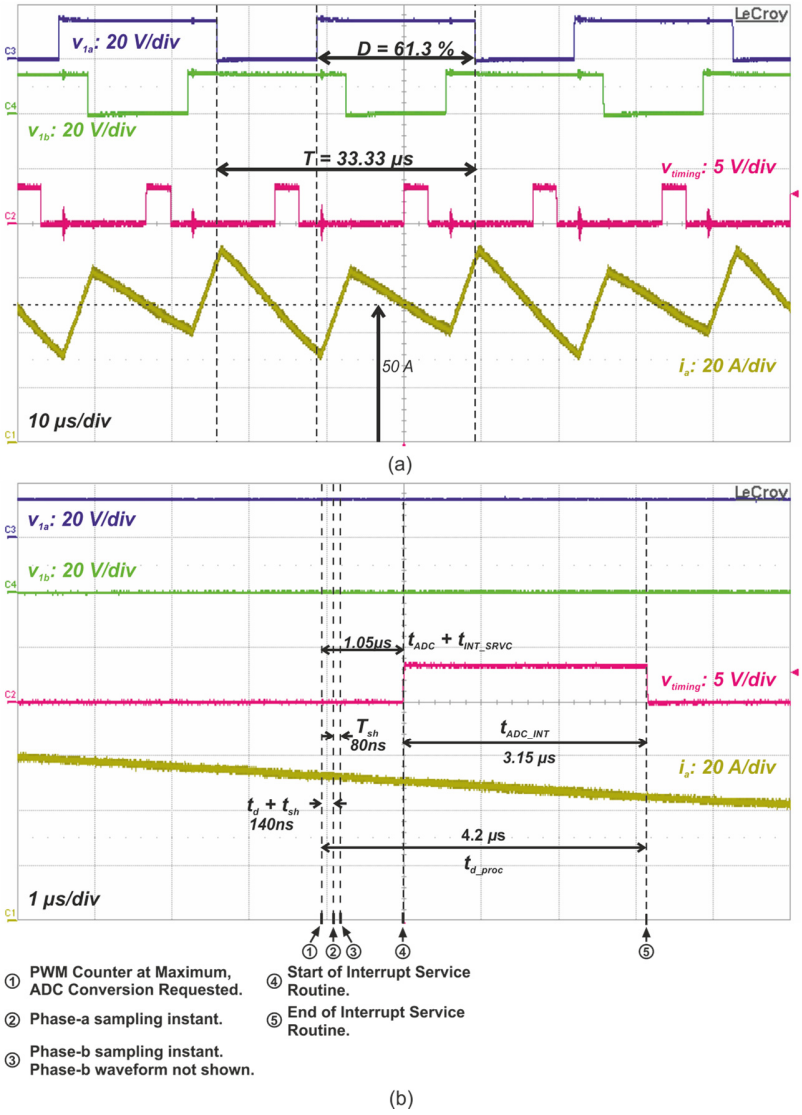

Figure 3.26. Experimental measurement of the processing time of the average-current control with immediate update. System conditions: V_{in} = 80 V; R_{load} = 5.2 Ω; D = 0.613, I_{Lin} = 101 A, V_o = 217 V. (a) Two complete cycles. (b) Expansion of the waveforms at the v_{timing} rising edge.

3.7.3. Dynamic performance

This section presents the experimental results for the average-current control algorithms with normal and immediate update for both a step-change in the reference-current and a step-change in the load. The results are arranged in a similar way as those presented for the valley-current and the peak-current control algorithms in Section 3.6.4. The figures presented display an overview of the transient response, a magnification of the increasing current transient and a magnification of the decreasing current transient. The waveforms displayed are the output voltage, v_o; the phase-a and phase-b currents shown one on top of the other, i_a and i_b respectively; and the differential current calculated as $i_{diff} = \frac{1}{2}(i_a - i_b)$. All the results were obtained with $V_{in} = 80\ V$. In addition, Figures 3.26 and 3.28, include an extra waveform plotted in green that was employed to synchronize the scope with the step-changes in the reference-current.

Figures 3.27 and Figure 3.28 show the step-reference and step-load results with normal update, whilst Figures 3.29 and 3.30 depict the transient response of the system with immediate update. During the step-reference tests R_{load} was $5.2\ \Omega$ whilst i_{ref} was switched between $20\ A$ and $50\ A$. Conversely, during the step-load tests i_{ref} was $50\ A$ whilst the load resistance was switched between $2.6\ \Omega$ and $5.2\ \Omega$.

Both control algorithms provided satisfactory regulation of the phase-currents. The average value of the phase-currents shows a steady-state error with respect to the reference-current of approximately $4\ A$ for $D > 0.5$ and $2\ A$ for $D < 0.5$ which is consistent with the steady-state tests of Section 3.7.1.

The two sets of results confirm the orderly operation of both control algorithms, with the phase currents remaining well-balanced throughout. Furthermore the results illustrate the much more rapid response that is obtained with the immediate update algorithm; the transient times of the phase currents are reduced by almost an order of magnitude, having values of around $2\ ms$. The improvement in speed is due to the use of a ten times larger integral gain in the immediate update system, which was made possible by the extended stability limits, which in turn were due to the reduced computation time.

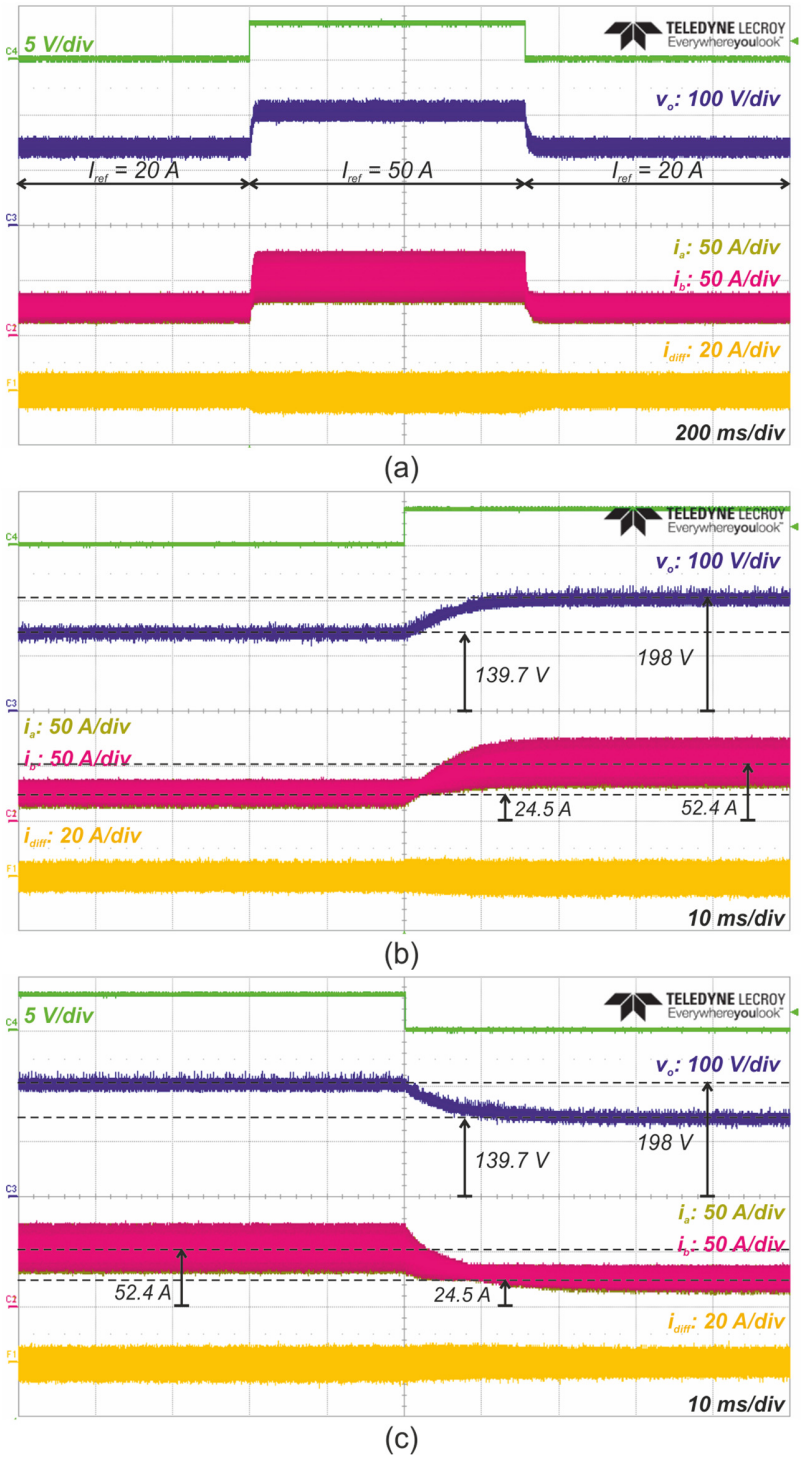

Figure 3.27. Experimental results of the step-reference response of the average-current current control with normal update. System conditions: I_{ref1} = 20 A, I_{ref2} = 50 A, V_{in} 80 V, R_{load} = 5.2 Ω. (a) Overview of the test. (b) Magnification of the step-up transient. (c) Magnification of the step-down transient.

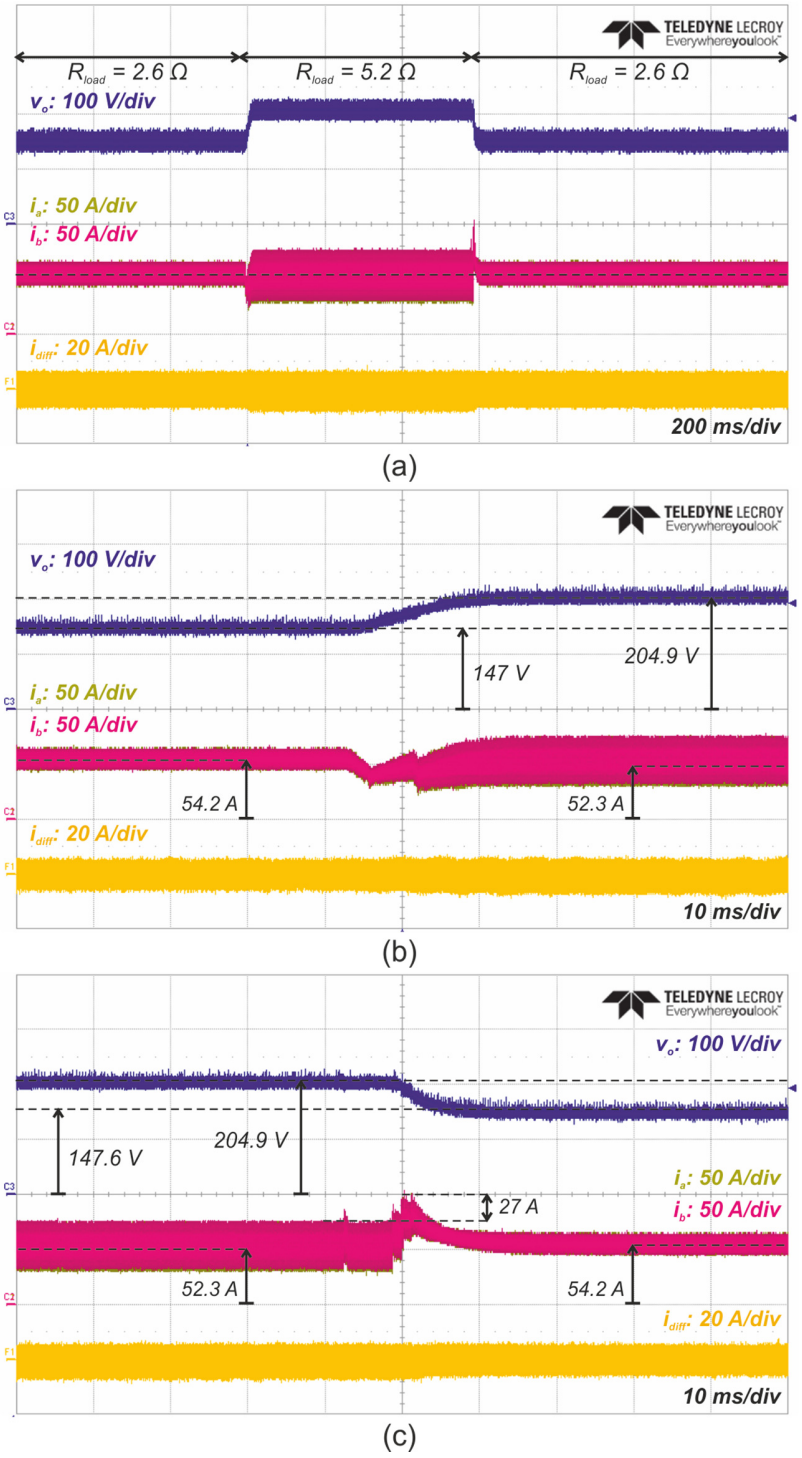

Figure 3.28. Experimental results of the step-load response of the average-current current control with normal update. System conditions: I_{ref} = 50 A, V_{in} 80 V, R_{load1} = 2.6 Ω, R_{load2} = 5.2 Ω. (a) Overview of the test. (b) Magnification of the step-up transient. (c) Magnification of the step-down transient.

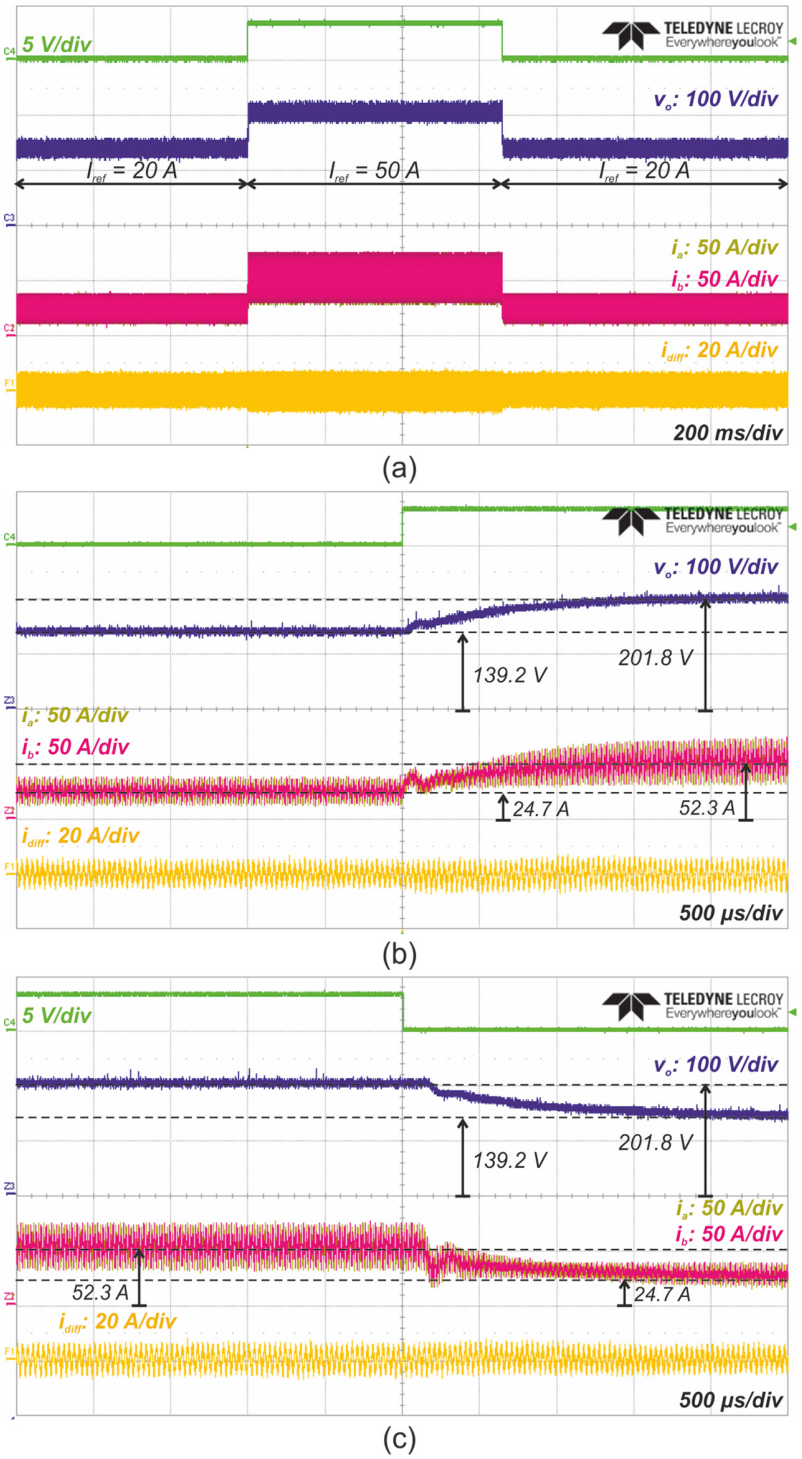

Figure 3.29. Experimental results of the step-reference response of the average-current current control with immediate update. System conditions: I_{ref1} = 20 A, I_{ref2} = 50 A, V_{in} 80 V, R_{load} = 5.2 Ω. (a) Overview of the test. (b) Magnification of the step-up transient. (c) Magnification of the step-down transient.

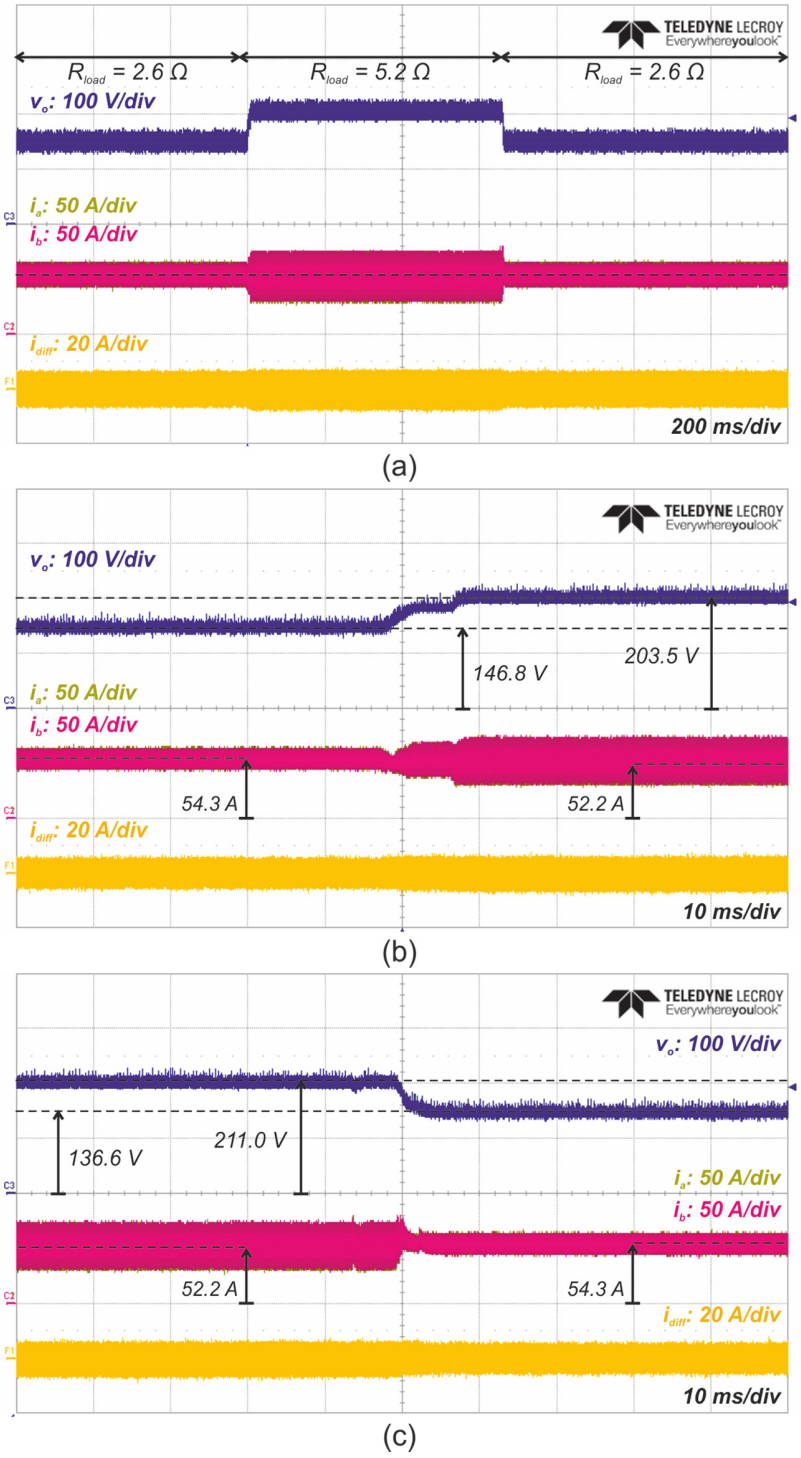

Figure 3.30. Experimental results of the step-load response of the average-current current control with immediate update. System conditions: I_{ref} = 50 A, V_{in} 80 V, R_{load1} = 2.6 Ω, R_{load2} = 5.2 Ω. (a) Overview of the test. (b) Magnification of the step-up transient. (c) Magnification of the step-down transient.

3.8. Summary

The design, component selection and construction of a digital control platform to interface a Texas Instruments TMS320F28335 digital signal controller with a *25 kW* of a dual interleaved converter prototype has been presented. Also the implementation of three digital control strategies for phase-current regulation have been described employing uniformly-sampled PWM with valley-current, peak-current and average-current control. In addition, a variant of the average-current control has been developed where the update delay caused by the DPWM operation is eliminated allowing the stability range of the converter to be extended and therefore enabling a faster response to be achieved. The correct operation of the control strategies was verified experimentally for a range of tests and compared against detailed SABER simulation results.

Although providing orderly operation of the converter and balanced phase-currents, both the valley-current and the peak-current algorithms were shown to be of limited value for this converter since uncontrollable regions were identified for duty-ratios in the region of *0.5*. Both forms of the average-current control algorithm allowed the converter to operate over the full range of duty-ratios whilst maintaining balanced phase currents. A maximum mismatch between the phase currents of *2 A* in *50 A* or *4 %* was observed, resulting in a *1 A* dc-offset in the IPT differential current.

Throughout detailed analysis of the processing delays, the immediate update version of the average-current control was developed, allowing the phase-current to be sampled and the duty-ratio to be updated within a switching period, but with the constraint of a minimum duty-ratio of *0.25.* Also, special measures were devised to prevent the generation of erroneous switching signals by the digital modulator. The immediate update algorithm provided transient times of around *2 ms*, however more detailed investigation of the control parameter settings and stability limits is considered in the following chapters.

3.9. References

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Chapter 4
Modelling phase interactions in dual interleaved converters

4.1. Introduction

In this Chapter, multirate discrete-data systems theory is used to extend the converter model developed in Chapter 2 to incorporate the interleaved operation of the phases, specifically when feedback is used to regulate the individual phase currents. The small-signal closed-loop transfer functions of the system in the z-domain are determined for two cases: when the interleaved operation of the converter is taken into account, termed the non-synchronous model, and when this interleaved interaction is disregarded, referred to as the synchronous model. The models are then compared with each other to examine their differences and against other switched and averaged models in order to provide validation. Finally, the predicted stability limits are compared with those from the practical system.

4.2. Representation of the converter in the control diagram form

Figure 4.1 shows a diagram of the average-current controlled dual interleaved boost converter with an inter-phase transformer and a digital signal controller. The DSC operates in an interleaved manner to regulate the average-current flowing through each phase of the converter using two individual current feedback loops, which share the same reference to ensure an equal distribution of the input current between the IPT windings.

In this diagram, the current-feedback signals $i_a(t)$ and $i_b(t)$ have transducer gains $H_a(s)$ and $H_b(s)$ respectively. These signals are sampled at a uniform rate by the analogue-to-digital converter, ADC. The sampling of $i_a(t)$, $i_b(t)$ and $i_{ref}(t)$ is represented by two

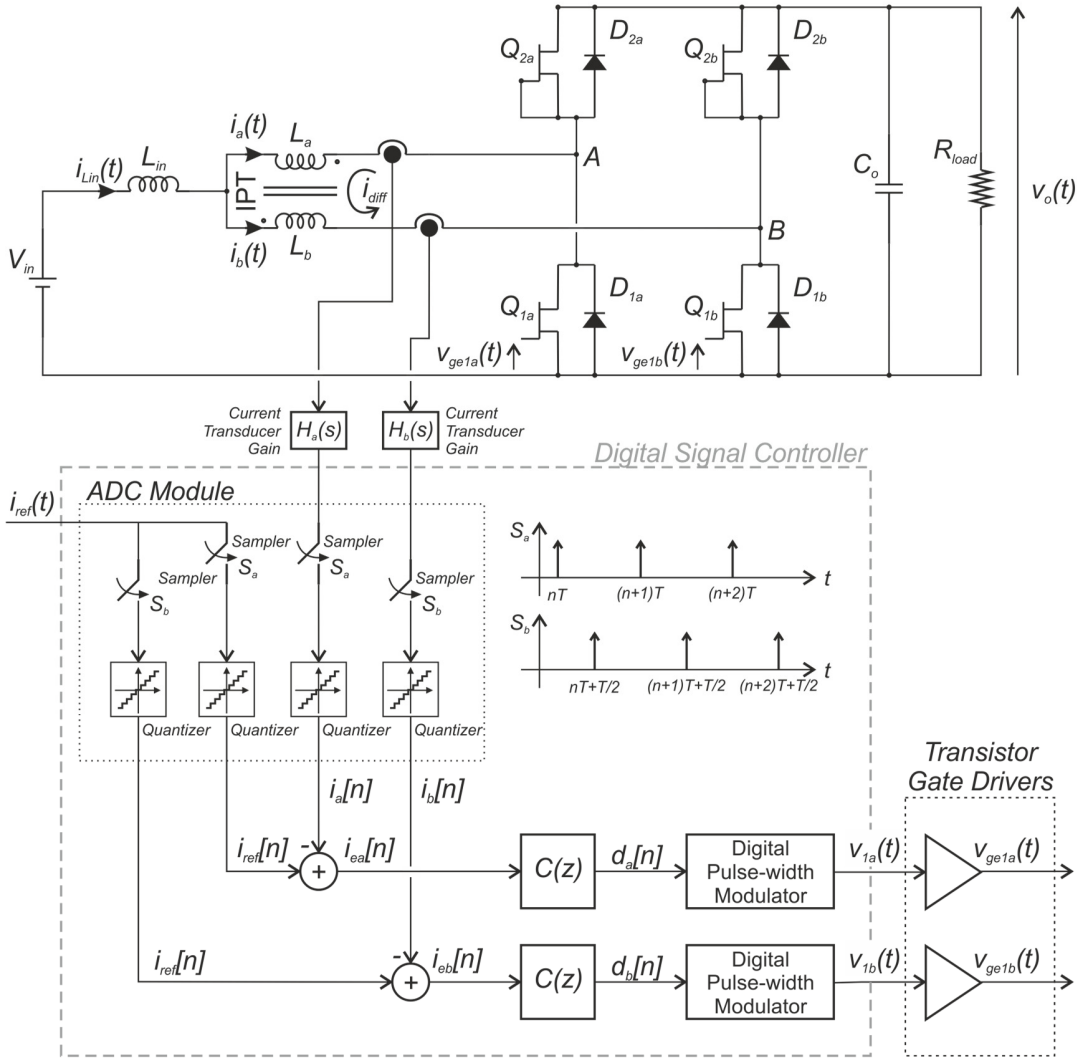

Figure 4.1. Digital feedback loop for regulation of the average phase-current of the dual-interleaved boost converter with inter-phase transformer.

samplers, S_a and S_b, with the sampled signals denoted $i_a[n]$, $i_b[n]$ and $i_{ref}[n]$ respectively and are employed to calculate the error signals $i_{ea}[n]$ and $i_{eb}[n]$. The samplers S_a and S_b share the same sampling period, T, but the sampling instants of the sampler S_b are delayed behind those of S_a by half a sampling period. The error signals, $i_{ea}[n]$ and $i_{eb}[n]$, in the two control loops are passed through a controller transfer function $C(z)$ before being passed on to the DPWM modules which generate the driving signals for the converter transistors.

4.2.1. Small-signal block diagram modelling

Figure 4.2(a) shows the system of Figure 4.1 represented as a standard closed-loop, block diagram in the Laplace-domain. In this diagram and in convention with the digital

control theory notation, the Laplace-domain representation of the time-domain pulse signals produced by the sampling devices are denoted by an asterisk. This representation is a variation of the Laplace transformation, commonly known as the starred transformation, which is defined by Equation (4.1), [1,2]:

$$f^*(s) = \left[f(s) \right]^* = \sum_{k=-\infty}^{+\infty} f(kT) e^{-kTs} \tag{4.1}$$

where *k* is the sample index and *T* is the sampling period.

In the system block diagram of Figure 4.2(a), the small-signal dynamics of the dual-interleaved boost converter are represented by the four Laplace-domain transfer functions determined in Chapter 2, Section 2.3, that relate the small changes in the transistor duty-ratios, $\tilde{d}_a(s)$ and $\tilde{d}_b(s)$, to the small changes in the converter phase-currents, $\tilde{i}_a(s)$ and $\tilde{i}_b(s)$, as shown in Equations (4.2) and (4.3):

$$\tilde{i}_a(s) = G_{daia}(s)\tilde{d}_a(s) + G_{dbib}(s)\tilde{d}_b(s) \tag{4.2}$$

$$\tilde{i}_b(s) = G_{daib}(s)\tilde{d}_a(s) + G_{dbib}(s)\tilde{d}_b(s) \tag{4.3}$$

where $G_{daia}(s) = G_{dbib}(s)$ *and* $G_{dbia}(s) = G_{daib}(s)$.

The current transducers of the control loops are represented by their respective transfer functions $H_a(s)$ and $H_b(s)$, whilst the analog-to-digital conversion process is modelled by the sampler devices S_a and S_b. For the sake of simplicity, the quantization non-linearity of the ADC and the delays associated with the measurements and the conditioning stages of the system are disregarded in this work.

The transfer function of the digital compensation network used in the control loops is represented by the blocks *C(z)*, whilst its associated computation delay, t_{d_proc}, is included with the DPWM modules. The DPWM modules are represented by a ZOH extrapolator connected in cascade with the associated processing delay of the compensation network, t_{d_proc}. As described in Chapter 1, Section 1.5.1.2, this is the simplest way to represent a DPWM, but may be replaced by the more elaborated models, [3], to enhance the accuracy in future research.

As shown in Chapter 3, Section 3.7, when average-current control is employed, the DPWMs can be updated immediately after the calculation of the new duty ratio or have a constant delay of *T/2*. In the former case, the processing time is $t_{d\_proc} < T/2$ and it is referred to as the immediate update mode. In the latter case the processing time can be defined as $t_{d\_proc} = T/2$ and is referred to as the normal update mode. Summarizing, the update delay of the DPWM modules can be represented as:

$$\Delta PWM(s) = \begin{cases} e^{-s(td\_\mathrm{proc})} & \forall \quad t_{d\_proc} < T/2 \\ e^{-s(T/2)} & \forall \quad t_{d\_proc} = T/2 \end{cases} \tag{4.4}$$

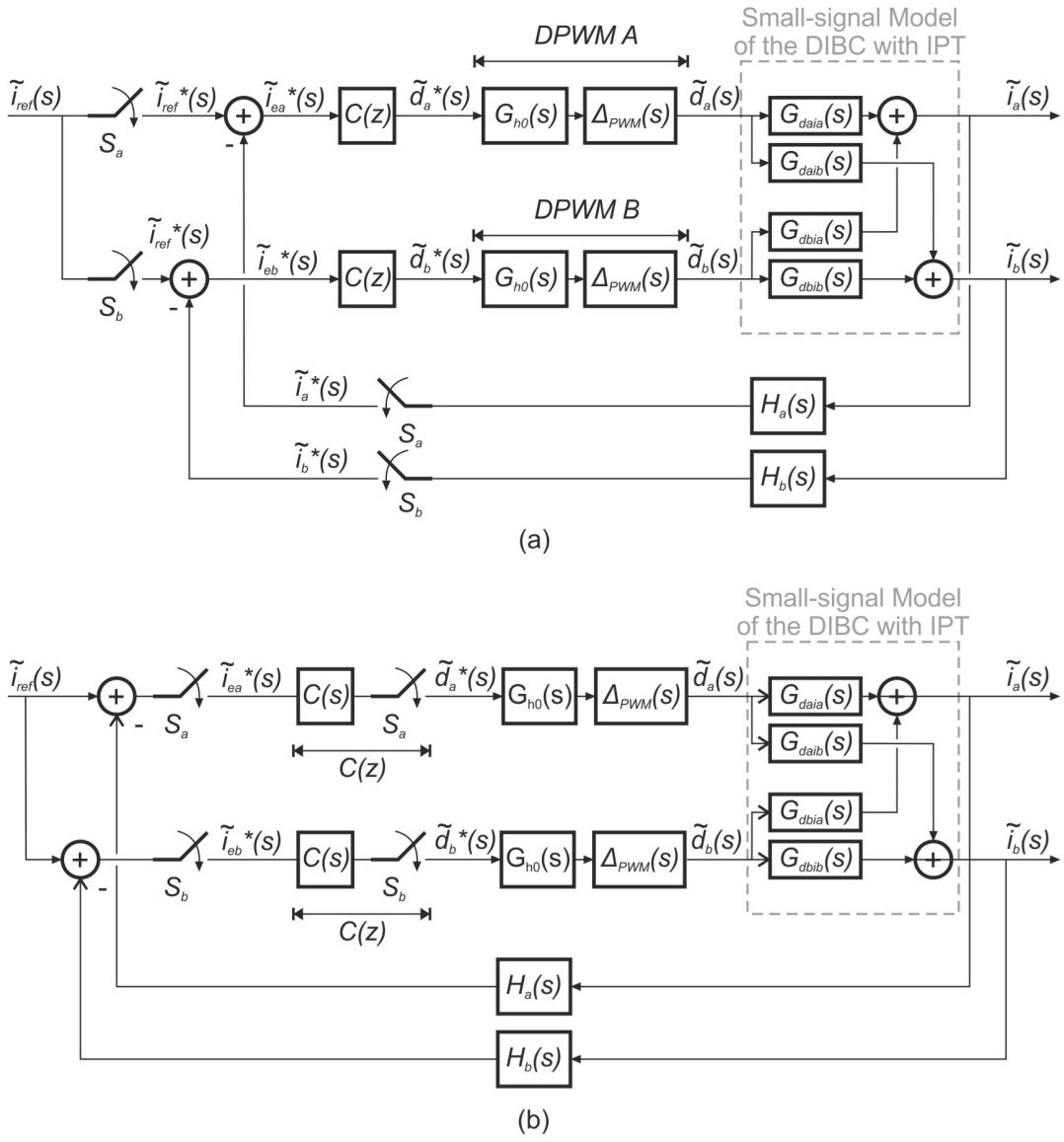

Figure 4.2. Functional control block diagram of the digital feedback loop for regulation of the average phase-currents of the DIBC with IPT. (a) Complete system; (b) Simplified system.

Finally, the model of Figure 4.2(a) can be simplified by moving S_a and S_b after the feedback summing junctions resulting in the diagram of Figure 4.2(b).

As described in Chapter 1, Section 1.6, previous work has neglected the interleaved sampling operation of the two phases. Therefore a key objective in this thesis is to devise a way of including the interleaved sampling and to examine its impact on controller design and converter stability.

4.3. Modelling of the interaction of the digital current control loops

To analyse the system stability and design an appropriate compensation network, analytical equations are required that relate the small changes in the reference-current input to small changes in the phase-currents. Therefore the closed-loop transfer functions $\tilde{i}_a(z)/\tilde{i}_{ref}(z)$ and $\tilde{i}_b(z)/\tilde{i}_{ref}(z)$, also denoted $G_{iairef}(z)$ and $G_{ibiref}(z)$, will be found employing multirate sampled-data systems theory.

4.3.1. The sampler-decomposition method

The sampler-decomposition [1,2] is used to model the effects of interleaved sampling. This methodology was chosen over other methods, such as the fictious-sampler

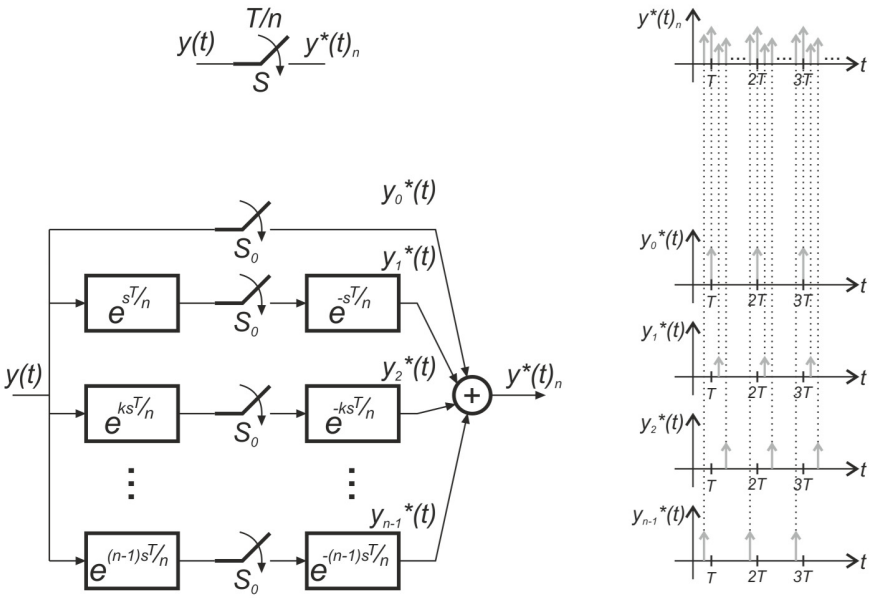

Figure 4.3. Decomposition of the sampler S with sampling rate *T/n* into *n* synchronized sub-samplers S_0 with sample rate *T*, [2].

method or the infinite-series representation, as it can be easily incorporated into the system model and it does not require a complex mathematical development. Moreover, owing to its versatility it is easily extendable to interleaved converters with two or more phases.

In this method, a sampler with sampling rate *T/n*, where *n* is an integer and *T* is the sampling period, can be decomposed into *n* parallel-connected, synchronized sub-samplers with sampling rate *T* using time advance and time delay units as illustrated in Figure 4.3. In this figure, the sampler *S* with sampling rate *T/n* is decomposed into *n* synchronized sub-samplers, S_0, which allocate the information corresponding to each sampling instant encompassed in the period *T*. Using the time advance and time delay units on each branch, the sampled data at different time instants is determined and relocated in such a way that all the interactions occur simultaneously in time and are finally combined in a single output $y^*(t)_n$. From the diagram of Figure 4.3, $y^*(t)_n$ may be expressed as:

$$y^*(t)_n = y_0^*(t) + \sum_{p=1}^{n-1} y_p^*(t) \tag{4.5}$$

4.3.2. Implementation of the sampler decomposition method in the digital average-current control loop

Considering the closed loop system depicted in Figure 4.2(b) and making use of the sampler decomposition method, S_b can be represented with respect to S_a as a single branch with time advance and time delay units equal to $e^{+sT/2}$ and $e^{-sT/2}$ as shown in Figure 4.4(a). Furthermore, the starred transform representation of the discrete-time signals of Figure 4.2(a) may be substituted directly by their z-domain representations owing to the link between the starred transform and the z-transform definitions. Equation (4.7) shows the definition of the z-transform, which can be derived from the starred transform definition, Equation (4.3), by replacing the term e^{-sT} with the *z* operator.

$$f(z) = \sum_{k=0}^{\infty} f(kT) z^{-k} \tag{4.7}$$

The resultant system block diagram is shown in Figure 4.4(b), where two fictious samplers were added at the outputs of the block diagram to allow the derivation of the

input-output relations of the system in the *z*-domain and where $G_M(s)$ is defined by Equation (4.6):

$$G_M(s) = G_{h0}(s)\Delta PWM(s) \tag{4.6}$$

This model is referred to as the non-synchronous small-signal model the DIBC with IPT.

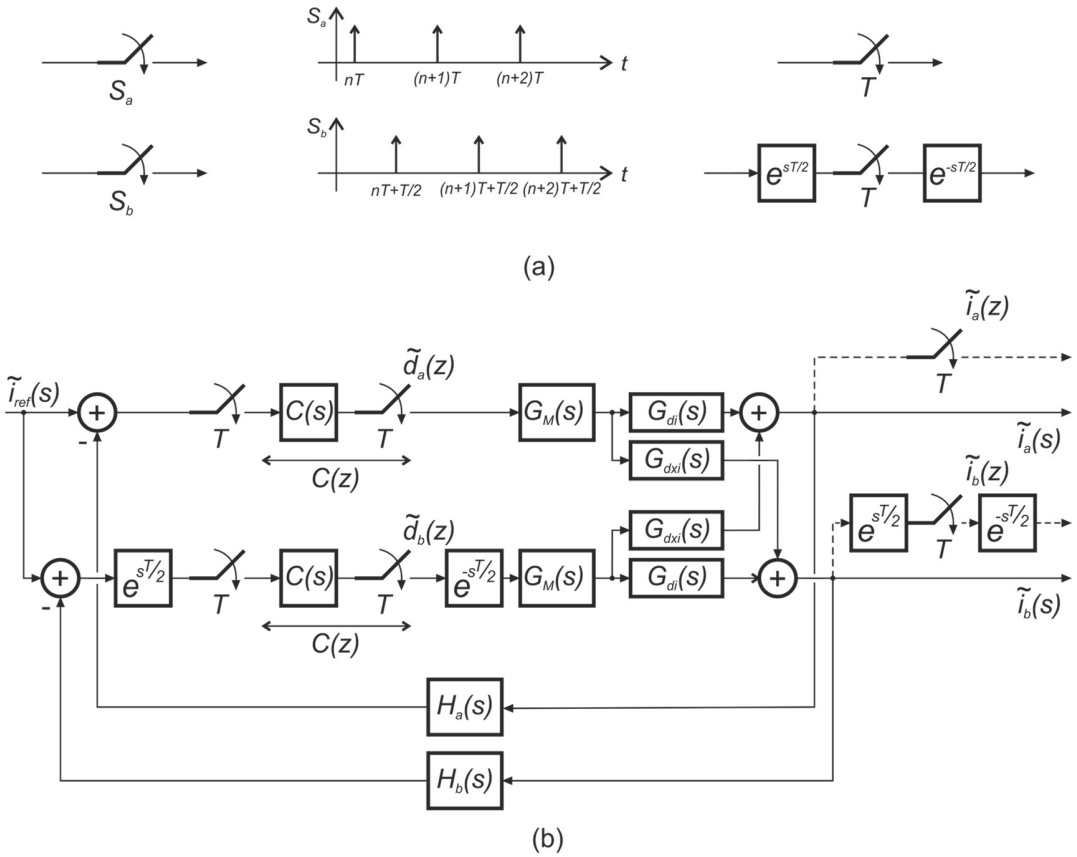

Figure 4.4. Implementation of the sampler decomposition method to model the average-current feedback loop of the DIBC with IPT: (a) Equivalent representation of the samplers S_a and S_b by a sampler with sampling period T. (b) Block diagram of the system with synchronous samplers.

4.3.3. Derivation of the closed-loop transfer functions $G_{iairef}(z)$ and $G_{ibiref}(z)$

In the following paragraphs, the closed-loop transfer functions $G_{iairef}(z)$ and $G_{ibiref}(z)$ will be derived from Figure 4.4(b) for the case where $t_{d\_proc} < T/2$, in other words, for the immediate DPWM update mode.

By analysis of the block diagram of Figure 4.4(b) the following relations can be written:

$$\tilde{d}_a(\mathrm{z}) = C(\mathrm{z})\mathcal{Z}\left[\tilde{i}_{ref}(\mathrm{s})\right] - C(\mathrm{z})\tilde{d}_a(\mathrm{z})\mathcal{Z}\left[G_M(\mathrm{s})\mathrm{G}_{di}(\mathrm{s})\mathrm{H}_a(\mathrm{s})\right] - C(\mathrm{z})\tilde{d}_b(\mathrm{z})\mathcal{Z}\left[e^{-sT/2}G_M(\mathrm{s})\mathrm{G}_{dxi}(\mathrm{s})\mathrm{H}_a(\mathrm{s})\right] \quad (4.8a)$$

$$\tilde{d}_b(\mathrm{z}) = C(\mathrm{z})\mathcal{Z}\left[e^{sT/2}\tilde{i}_{ref}(\mathrm{s})\right] - C(\mathrm{z})\tilde{d}_b(\mathrm{z})\mathcal{Z}\left[G_M(\mathrm{s})\mathrm{G}_{di}(\mathrm{s})\mathrm{H}_b(\mathrm{s})\right] - C(\mathrm{z})\tilde{d}_a(\mathrm{z})\mathcal{Z}\left[e^{sT/2}G_M(\mathrm{s})\mathrm{G}_{dxi}(\mathrm{s})\mathrm{H}_b(\mathrm{s})\right] \quad (4.8b)$$

$$\tilde{i}_a(\mathrm{z}) = \tilde{d}_a(\mathrm{z})\mathcal{Z}\left[G_M(\mathrm{s})\mathrm{G}_{di}(\mathrm{s})\right] + \tilde{d}_b(\mathrm{z})\mathcal{Z}\left[e^{-sT/2}G_M(\mathrm{s})\mathrm{G}_{dxi}(\mathrm{s})\right] \quad (4.8c)$$

$$\tilde{i}_b(\mathrm{z}) = \tilde{d}_b(\mathrm{z})\mathcal{Z}\left[G_M(\mathrm{s})\mathrm{G}_{di}(\mathrm{s})\right] + \tilde{d}_a(\mathrm{z})\mathcal{Z}\left[e^{sT/2}G_M(\mathrm{s})\mathrm{G}_{dxi}(\mathrm{s})\right] \quad (4.8d)$$

The z-transforms found in Equations (4.8a) to (4.8d) are listed in Table 4.1 and are redefined in a compact notation for this particular case-study where $t_{d\_proc} < T/2$, in other words, $\Delta PWM(s) = e^{-s(td\_\mathrm{proc})}$. Upon substitution of the compact notation of the constituent z-transforms into Equations (4.8a) to (4.8d), Equations (4.9a) to (4.9d) are found:

Table 4.1. Constituent transfer functions of the digital average-current controlled DIBC with IPT in the z-domain.

Z-transform identified	Modified z-transform	Compact notation
$\mathcal{Z}\left\{e^{sT/2}\tilde{i}_{ref}(s)\right\}$	$\mathrm{z}\tilde{i}_{ref}(\mathrm{z},1/2)$	$\tilde{i}_{ref\theta}(\mathrm{z})$
$\mathcal{Z}\left\{G_M(s)G_{di}(s)H_A(s)\right\}$	$\mathcal{Z}\left\{G_{h0}(s)\Delta PWM(s)G_{di}(s)H_A(s)\right\} = = G_{di}H_A\left(z,1-t_{d\_proc}\right)$	$G_{di}H_A(z)$
$\mathcal{Z}\left\{G_M(s)G_{di}(s)H_B(s)\right\}$	$\mathcal{Z}\left\{G_{h0}(s)\Delta PWM(s)G_{di}(s)H_B(s)\right\} = G_{di}H_B\left(z,1-t_{d\_proc}\right)$	$G_{di}H_B(z)$
$\mathcal{Z}\left\{e^{-sT/2}G_M(s)G_{dxi}(s)H_A(s)\right\}$	$\mathcal{Z}\left\{e^{-sT/2}G_{h0}(s)\Delta PWM(s)G_{dxi}(s)H_A(s)\right\} = = G_{dxi}H_A\left(z,1-(1/2+\mathrm{t}_{d\_proc})\right)$	$G_{dxi\phi}H_A(z)$
$\mathcal{Z}\left\{e^{sT/2}G_M(s)G_{dxi}(s)H_B(s)\right\}$	$\mathcal{Z}\left\{e^{sT/2}G_{h0}(s)\Delta PWM(s)G_{dxi}(s)H_B(s)\right\} = = zG_{dxi}H_B\left(z,\left(1/2-t_{d\_proc}\right)\right)$	$G_{dxi\theta}H_B(z)$
$\mathcal{Z}\left\{G_M(s)\mathrm{G}_{di}(s)\right\}$	$\mathcal{Z}\left\{G_{h0}(s)\Delta PWM(s)\mathrm{G}_{di}(s)\right\} = = G_{di}\left(z,1-t_{d\_proc}\right)$	$G_{di}(z)$
$\mathcal{Z}\left\{e^{-sT/2}G_M(s)\mathrm{G}_{dxi}(s)\right\}$	$e^{-sT/2}\mathcal{Z}\left\{G_{h0}(s)\Delta PWM(s)\mathrm{G}_{dxi}(s)\right\} = = G_{dxi}\left(z,1-\left(1/2+t_{d\_proc}\right)\right)$	$G_{dxi\phi}(z)$
$\mathcal{Z}\left\{e^{sT/2}G_M(s)\mathrm{G}_{dxi}(s)\right\}$	$\mathcal{Z}\left\{e^{sT/2}G_{h0}(s)\Delta\mathrm{PWM}(s)\mathrm{G}_{dxi}(s)\right\} = = zG_{dxi}\left(z,\left(1/2-t_{d\_proc}\right)\right)$	$G_{dxi\theta}(z)$

$$\tilde{d}_a(z) = C(z)\tilde{i}_{ref}(z) - C(z)\tilde{d}_a(z)G_{di}H_a(z) - C(z)\tilde{d}_b(z)G_{dxi\phi}H_a(z) \quad (4.9a)$$

$$\tilde{d}_b(z) = C(z)\tilde{i}_{ref\theta}(z) - C(z)\tilde{d}_b(z)G_{di}H_b(z) - C(z)\tilde{d}_a(z)G_{dxi\theta}H_b(z) \quad (4.9b)$$

$$\tilde{i}_a(z) = \tilde{d}_a(z)G_{di}(z) + \tilde{d}_b(z)G_{dxi\phi}(z) \quad (4.9c)$$

$$\tilde{i}_b(z) = \tilde{d}_b(z)G_{di}(z) + \tilde{d}_a(z)G_{dxi\theta}(z) \quad (4.9d)$$

As $i_{ref}(t)$ can be considered to be constant over a sampling period, it is possible to assume $\tilde{i}_{ref}(z) = \tilde{i}_{ref\theta}(z)$. Under this assumption, $\tilde{d}_a(z)$ can be found by solving Equation (4.9a) for $\tilde{d}_b(z)$ and substituting it into Equation (4.9b):

$$\tilde{d}_a(z) = C(z)\tilde{i}_{ref}(z)\left\{\frac{1 + C(z)\left[G_{di}H_b(z) - G_{dxi\phi}H_a(z)\right]}{\left[C(z)G_{di}H_a(z)+1\right]\left[C(z)G_{di}H_b(z)+1\right] - C^2(z)G_{dxi\phi}H_a(z)G_{dxi\theta}H_b(z)}\right\} \quad (4.10a)$$

In a similar way, solving Equation (4.9b) for $\tilde{d}_a(z)$ and substituting it into Equation (4.9a), $\tilde{d}_b(z)$ is obtained:

$$\tilde{d}_b(z) = C(z)\tilde{i}_{ref}(z)\left\{\frac{1 + C(z)\left[G_{di}H_a(z) - G_{dxi\theta}H_b(z)\right]}{\left[C(z)G_{di}H_a(z)+1\right]\left[C(z)G_{di}H_b(z)+1\right] - C^2(z)G_{dxi\phi}H_a(z)G_{dxi\theta}H_b(z)}\right\} \quad (4.10b)$$

Finally, substituting Equations (4.10a) and (4.10b) into (4.9c), the closed-loop transfer function $G_{iairef}(z)$ can be derived as:

$$\frac{\tilde{i}_a(z)}{\tilde{i}_{ref}(z)} = C(z)\left\{\frac{G_{di}(z) + G_{dxi\phi}(z) + C(z)\left\{G_{di}(z)\left[G_{di}H_b(z) - G_{dxi\phi}H_a(z)\right] + G_{dxi\phi}(z)\left[G_{di}H_a(z) - zG_{dxi\theta}H_b(z)\right]\right\}}{\left[C(z)G_{di}H_a(z)+1\right]\left[C(z)G_{di}H_b(z)+1\right] - C^2(z)G_{dxi\phi}H_a(z)G_{dxi\theta}H_b(z)}\right\} \ldots$$

…(4.11a)

In a similar way, substituting Equations (4.10a) and (4.10b) in (4.9d), $G_{ibiref}(z)$ can be found:

$$\frac{\tilde{i}_b(z)}{\tilde{i}_{ref}(z)} = C(z)\left\{\frac{G_{di}(z) + G_{dxi\theta}(z) + C(z)\left\{G_{di\theta}(z)\left[G_{di}H_a(z) - zG_{dxi\theta}H_b(z)\right] + G_{dxi}(z)\left[G_{di}H_b(z) - G_{dxi\phi}H_a(z)\right]\right\}}{\left[C(z)G_{di}H_a(z)+1\right]\left[C(z)G_{di}H_b(z)+1\right] - C^2(z)G_{dxi\phi}H_a(z)G_{dxi\theta}H_b(z)}\right\} \ldots$$

…(4.11b)

To further simplify Equations (4.11a) and (4.11b) it can be assumed that the current transducers have unity gain $H_a(s) = H_b(s) = 1$, resulting in:

$$G_{iairef}(z) = \frac{\tilde{i}_a(z)}{\tilde{i}_{ref}(z)} = \frac{C(z)G_{di}(z) + C(z)G_{dxi\phi}(z) + C^2(z)\left[G_{di}^{\ 2}(z) - G_{dxi\phi}(z)G_{dxi\theta}(z)\right]}{1 + 2C(z)G_{di}(z) + C^2(z)\left[G_{di}^{\ 2}(z) - G_{dxi\phi}(z)G_{dxi\theta}(z)\right]} \tag{4.12a}$$

$$G_{ibiref}(z) = \frac{\tilde{i}_b(z)}{\tilde{i}_{ref}(z)} = \frac{C(z)G_{di}(z) + C(z)G_{dxi\theta}(z) + C^2(z)\left[G_{di}^{\ 2}(z) - G_{dxi\phi}(z)G_{dxi\theta}(z)\right]}{1 + 2C(z)G_{di}(z) + C^2(z)\left[G_{di}^{\ 2}(z) - G_{dxi\phi}(z)G_{dxi\theta}(z)\right]} \tag{4.12b}$$

Equations (4.12a) and (4.12b) are the closed-loop transfer functions of the DIBC with IPT which account for the interleaved operation of the converter phases, specifically when digital average-current control is employed. The characteristic equation of these transfer functions can be identified as:

$$1 + 2C(z)G_{di}(z) + C^2(z)\left[G_{di}^{\ 2}(z) - G_{dxi\phi}(z)G_{dxi\theta}(z)\right] = 0 \tag{4.13}$$

Also, a quick inspection of Equations (4.12a) and (4.12b) reveals that they do not have an obvious open-loop transfer function, making it very difficult to employ methods such as Bode-plots to evaluate the system stability and/or design a compensator.

Following a similar method as that above described, the closed-loop transfer functions may also be determined assuming the synchronous operation of S_a and S_b, resulting in:

$$\frac{\tilde{i}_a(z)}{\tilde{i}_{ref}(z)} = \frac{\tilde{i}_b(z)}{\tilde{i}_{ref}(z)} = \frac{C(z)\left[G_{di}(z) + G_{dxi}(z)\right]}{1 + C(z)\left[G_{di}(z) + G_{dxi}(z)\right]} \tag{4.14}$$

The resulting transfer-functions are greatly simplified and are identical for both phases. Furthermore, Equation (4.14) has the standard structure of a SISO unity-feedback, closed-loop system, where the characteristic equation may be identified as:

$$1 + C(z)\left[G_{di}(z) + G_{dxi}(z)\right] = 0 \tag{4.16}$$

and the open-loop transfer function of the system is:

$$T(z) = C(z)\left[G_{di}(z) + G_{dxi}(z)\right] \tag{4.17}$$

This is a significant advantage over the interleaved small-signal model, Equations (4.12a) and (4.12b), as it enables the design of a compensation network and the analysis of the system by the use of standard methods. The derivation of Equation (4.14) can be found in Appendix A.2.

Finally, the closed-loop transfer functions for both the synchronous and the non-synchronous models may also be derived assuming the normal update operation of the DPWM, or in other words, assuming $t_{d\_proc} = T/2$. The transfer functions obtained are particular cases of the immediate update transfer functions and are summarized in Table 4.2, as Equations (4.18a), (4.18b) and (4.19).

Table 4.2. Closed-loop transfer functions of the digital average-current controlled DIBC with IPT in the z-domain.

Immediately updated DPWM ($t_{d\_proc} < T/2$)

Non-Synchronous Samplers (Case I)*	$\frac{\tilde{i}_a(z)}{\tilde{i}_{ref}(z)} = \frac{C(z)G_{di}(z) + C(z)G_{dxi\phi}(z) + C^2(z)\left[G_{di}^2(z) - G_{dxi\phi}(z)G_{dxi\theta}(z)\right]}{1 + 2C(z)G_{di}(z) + C^2(z)\left[G_{di}^2(z) - G_{dxi\phi}(z)G_{dxi\theta}(z)\right]}$	(4.12a)
	$\frac{\tilde{i}_b(z)}{\tilde{i}_{ref}(z)} = \frac{C(z)G_{di}(z) + C(z)G_{dxi\theta}(z) + C^2(z)\left[G_{di}^2(z) - G_{dxi\phi}(z)G_{dxi\theta}(z)\right]}{1 + 2C(z)G_{di}(z) + C^2(z)\left[G_{di}^2(z) - G_{dxi\phi}(z)G_{dxi\theta}(z)\right]}$	(4.12b)
Synchronous Samplers (Case II)*	$\frac{\tilde{i}_a(z)}{\tilde{i}_{ref}(z)} = \frac{\tilde{i}_b(z)}{\tilde{i}_{ref}(z)} = \frac{C(z)\left[G_{di}(z) + G_{dxi}(z)\right]}{1 + C(z)\left[G_{di}(z) + G_{dxi}(z)\right]}$	(4.14)

Normally updated DPWM ($t_{d\_proc} = T/2$)

Non-Synchronous Samplers (Case III)**	$\frac{\tilde{i}_a(z)}{\tilde{i}_{ref}(z)} = \frac{z^{-1}C(z)G_{di}(z) + z^{-1}C(z)G_{dxi\phi}(z) + C^2(z)\left[z^{-2}G_{di}^2(z) - z^{-1}G_{dxi\phi}(z)G_{dxi\theta}(z)\right]}{1 + 2z^{-1}C(z)G_{di}(z) + C^2(z)\left[z^{-2}G_{di}^2(z) - z^{-1}G_{dxi\phi}(z)G_{dxi\theta}(z)\right]}$	(4.18a)
	$\frac{\tilde{i}_b(z)}{\tilde{i}_{ref}(z)} = \frac{z^{-1}C(z)G_{di}(z) + C(z)G_{dxi\theta}(z) + C^2(z)\left[z^{-2}G_{di}^2(z) - z^{-1}G_{dxi\phi}(z)G_{dxi\theta}(z)\right]}{1 + 2z^{-1}C(z)G_{di}(z) + C^2(z)\left[z^{-2}G_{di}^2(z) - z^{-1}G_{dxi\phi}(z)G_{dxi\theta}(z)\right]}$	(4.18b)
Synchronous Samplers (Case IV)**	$\frac{\tilde{i}_a(z)}{\tilde{i}_{ref}(z)} = \frac{\tilde{i}_b(z)}{\tilde{i}_{ref}(z)} = \frac{z^{-1}C(z)\left[G_{di}(z) + G_{dxi}(z)\right]}{1 + z^{-1}C(z)\left[G_{di}(z) + G_{dxi}(z)\right]}$	(4.19)

* Constituent transfer functions as defined in Table 4.1
** Constituent transfer functions as defined in Table A.1, Appendix A

4.3.4. Implementation of the models in MATLAB

The closed-loop transfer functions of the non-synchronous model, Equations (4.12a) and (4.12b), and the synchronous model, Equation (4.14), were determined numerically employing a script developed in MATLAB. This script can be found in Appendix B.1.

In the first stage of this script, the parameters of the converter and initial conditions of the system are defined. In the second stage, the s-domain control-to-output transfer functions that describe the small-signal dynamics of the converter, Equations (4.1) and (4.2), are determined using the small-signal averaged model of the DIBC with IPT developed in Chapter 2, Section 2.4.1. The resulting transfer functions of this stage are represented as the ratio of two s-domain polynomials with numerical coefficients and are necessary to calculate the constituent transfer functions of the closed-loop model of the converter. In the third stage, the constituent transfer functions shown in Table 4.1 are calculated. Finally, in the last stage, the closed-loop transfer functions shown in Table 4.2 are calculated employing the constituent transfer functions previously determined in the third stage. The resulting transfer functions are represented as the ratio of two polynomials in the z-domain with numerical coefficients. The results presented in the following sections were obtained employing this script.

4.4. Validation of the closed-loop models

In this section the closed-loop models are validated and compared in three different ways: using their transient response to small step-reference changes, considering the response to small sinusoidal disturbances and finally by examining the stability range predicted by the models when a proportional-integral compensator is employed. To this end the small-signal models introduced in the previous section were implemented in MATLAB, and the results are compared against those from the simulation of both the switched and the averaged SABER models. The results presented were obtained assuming that the immediate-update control algorithm, described in Chapter 3, is used. The MATLAB scripts employed can be found in Appendix B. The SABER models employed are those previously introduced in Chapter 3, Section 3.7, which were validated using the converter prototype.

4.4.1. Transient response

Figure 4.5 shows the transient response of the models to a *5%* step increase in the reference-current of the digital control-loops. The system conditions employed were V_{in} = *80 V* and R_{load} = *5.2 Ω* and the PI compensator gains used are K_p = *30T* and K_i = *10* which are identical to those employed for the experimental results shown in Chapter 3 and were selected using the simplified non-interleaved model of the converter described by Equations (4.14) and in conjunction with SISO tool in MATLAB to guarantee the stability of the converter. An appropriate design methodology for this PI gains is later described in Chapter 5 of this Thesis. The graphs are divided into three groups. Figure 4.5(a) shows the results obtained for *D = 0.25*, Figure 4.5(b) for *D = 0.5*, and finally Figure 4.5(c) for *D = 0.75*. In each group, two sets of three graphs are shown. The top set provides an overview of the complete transient whilst the bottom set shows a time expansion at the start of the transient.

The parameters of the converter and the DSC unit employed in the SABER simulations are listed in Table 4.3. The transient responses of the mathematical models were obtained by applying the MATLAB *step()* command to the numerical solution of the transfer functions determined with the MATLAB script of Appendix B.1.

Table 4.3. Attributes of the converter and the DSC employed for the simulations.

Power Converter	
Input inductance at 60 kHz	*5.12 µH*
IPT windings self-inductance at 30kHz	*75.14 µH*
Coupling coefficient of the IPT windings	*0.997*
Output capacitance	*45 µF*
Load Resistance	*2.8 Ω, 5.2 Ω*
Input Voltage	*80 V*
Transistor turn-on/off delay*	*520 ns*
Switching frequency	*30 kHz*
Digital Signal Controller	
Master clock frequency*	*150 Mhz*
ADC sampling delay*	*140 ns* phase-a, *220 ns* phase-b
Compensation network	Digital PI, Backward-Euler implementation

* SABER switched model only.

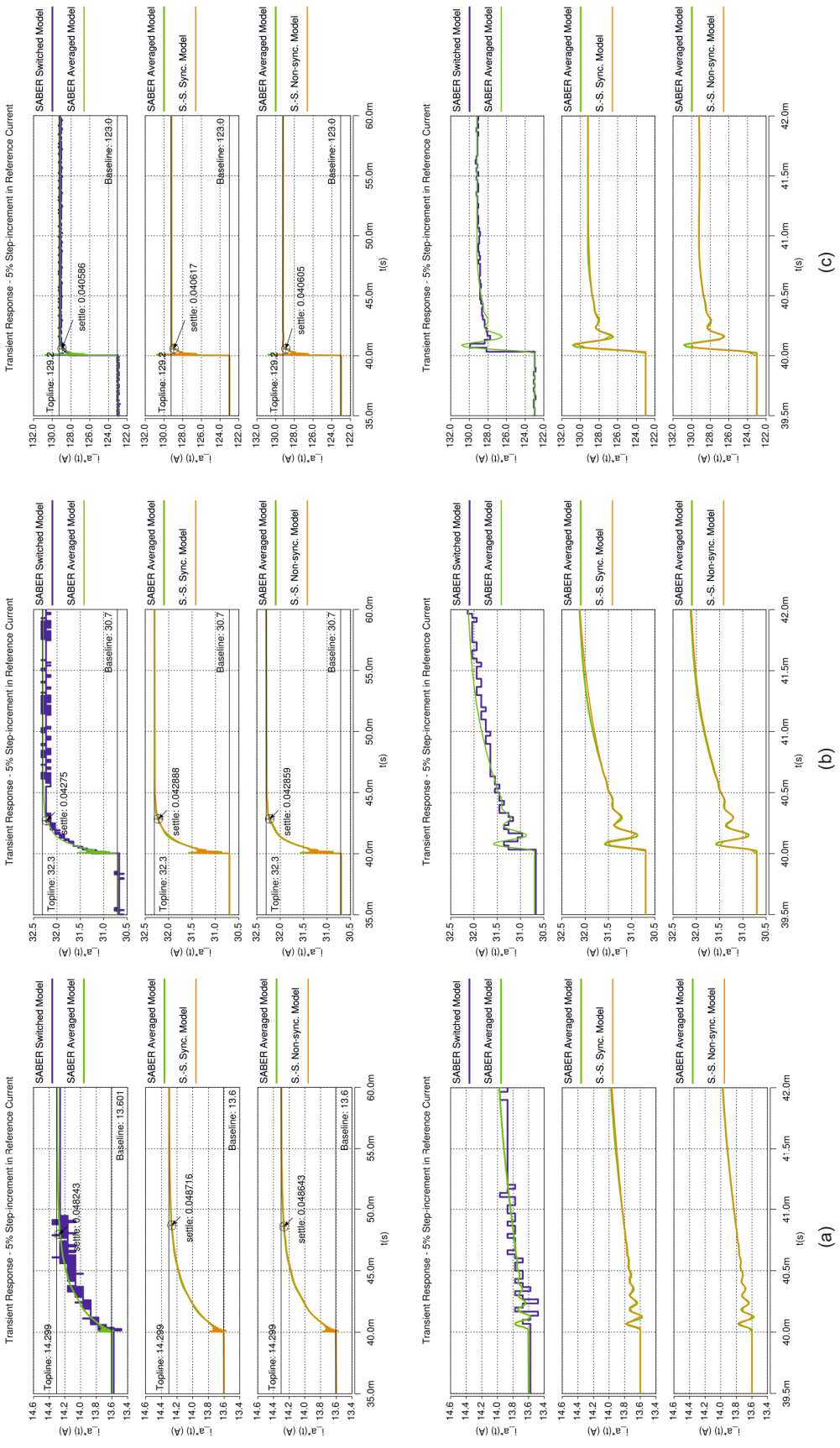

Figure 4.5. Closed-loop transient response of the sampled average-current $i_a^*(t)$ to a 5% step-increment in the reference-current input $i_{ref}(t)$. SABER switched model, SABER averaged model, small-signal synchronous model and small-signal non-synchronous model. Compensator: Digital PI with $K_p = 30T$ and $K_i = 10$; $R_{load} = 5.2\ \Omega$; $V_{in} = 80\ V$. (a) $I_{ref1} = 13.6\ A$, $I_{ref2} = 14.3\ A$, $D = 0.25$; (b) $I_{ref1} = 30.7\ A$, $I_{ref2} = 32.3\ A$, $D = 0.5$; (c) $I_{ref1} = 123\ A$, $I_{ref2} = 129.2\ A$, $D = 0.75$.

The waveform shown for the comparison of the models is the sampled phase-a current, $i_a^*(t)$. This current is shown instead of $i_a(t)$ as the large ripple of the SABER switched model would obscure the details of the response. In the first graph of each set, the transient-response of the SABER switched model is compared to that obtained from the SABER averaged model. The second graph depicts the transient-response of the small-signal synchronous model, Equation (4.14), which is compared against that of the SABER averaged model. Finally, in the last graph, the transient response of the non-synchronous model, Equation (4.12a), is superimposed on that of the SABER averaged model.

The results of the SABER switched model show bursts of random looking oscillations throughout the waveforms, however these oscillations have no more than *1 A* of amplitude. This behaviour was attributed to limit-cycle oscillations, LCOs, caused by quantization effects within the control loops, in particular the interaction produced by the resolutions of the ADC and the DPWM generators [4,5]. This was confirmed by increasing the resolution of the DPWM modules by a factor of four in the SABER switched model and the step response was re-simulated. The results from the SABER switched model employing a clock frequency of *150 MHz* and a clock frequency of *600 MHz* are superimposed in the graph of Figure 4.6, where the amplitude of the oscillations is reduced by about *75 %*.

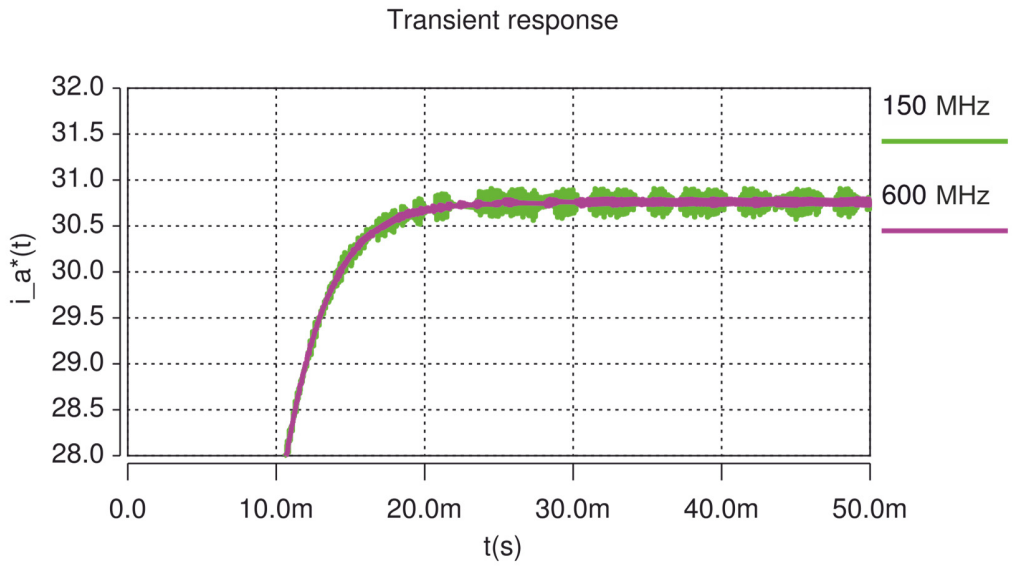

Figure 4.6. Comparison of transient responses of the SABER switched model using a *150 MHz* DPWM clock or a resolution of *6.66 ns* and using a *600 MHz* DPWM clock or a resolution of *1.66 ns*. V_{in} =80 V, R_{load} = 5.2 Ω, I_{ref} = 30.7 A, D = 0.5. Immediate update mode, $t_{d\ proc}$ = (0.21)T = 4.2 µs.

Going back to the results of Figure 4.5, the SABER averaged model follows closely the transient oscillations of the SABER switched model. The difference in the frequency of the oscillations is thought to be caused by parameters not considered in the averaged modelling such as non-zero switching times of the transistors and quantization effects of the ADC and PWM module. A difference in the steady-state value of the SABER averaged model and the SABER switched model of *0.1 A* can be noticed in Figure 4.5(a), this might be caused by the presence of LCOs. For the other cases examined, the difference in the steady-state value is negligible compared to the level of current.

The results obtained for the synchronous and non-synchronous models depicted for all the cases, correspond closely to the results of the SABER averaged model. No significant difference was noticed in the results. However, a close-inspection of the time-expansions reveals that the non-synchronous model predicts with more accuracy the amplitude of the sampled current, but the difference is not very significant.

4.4.2. Frequency response to small sinusoidal perturbations

In this section, the frequency response of the small-signal synchronous model, Equation (4.14), and the small-signal non-synchronous model, Equation (4.12a) and (4.12b), are compared against that of the SABER averaged model. The closed-loop transfer functions were calculated using the MATLAB program in Appendix B.1. The system parameters used in the MATLAB script are shown in Table 4.3.

In order to undertake this analysis in SABER, the Time Domain System Analyser tool, TDSA, was employed. This tool emulates the operation of a network analyser allowing the user to measure the magnitude and phase response of a system to small-sinusoidal perturbations. The parameters used to obtain the results for the SABER averaged model are listed in Table 4.4. The signal generator of the TDSA was connected to the reference-current input of the control loops whilst the phase-a current was converted into a voltage signal and fed-back into the measuring port of the TDSA tool. The parameters of the converter and the DSC unit in SABER are as shown in Table 4.3.

Table 4.4. Parameters of the TDSA tool employed in SABER to obtain the frequency response of the model to small-sinusoidal perturbations.

Parameter Name	Value
fbegin	*10*
fend	*20k*
ampl	*1*
Offset	*200*
npoints	*logswp*
Mode	*0.01*
Max_err	*0.01*
Max_nper	*100*
Min_nper	*5*
Min_tspp	*100*
a0	*1*
q0	*80*
Filter	*yes*
ac	*mag=1, phase=0*

Figures 4.7(a), 4.7(b) and 4.7(c) show the magnitude and phase response of the closed-loop transfer functions in the frequency domain for the points of operation $D = 0.25$, $D = 0.5$ and $D = 0.75$ from *10 Hz* to *20 kHz*. The system conditions employed were $V_{in} = 80\ V$, $R_{load} = 5.2\ \Omega$ and the DPWM modules were updated in normal mode, in other words, $t_{d\_proc} = (0.5)T$. Furthermore the PI controller gains were $K_p = 30T$ and $K_i = 10$. The results shown are only valid up to half of the switching frequency of the converter, or *15 kHz*, as stated by Nyquist.

In the first two graphs of Figures 4.7(a), 4.7(b) and 4.7(c), the magnitude and phase response of the SABER averaged model and the small-signal synchronous model, Equation (4.14), are compared. In the third and fourth graphs the magnitude and phase response of the phase-a current obtained with the SABER average model and the small-signal non-synchronous model, Equation (4.11a), are plotted. Finally, in the fifth and sixth graphs, the magnitude and phase response of the phase-b current obtained with the SABER averaged model and the small-signal non-synchronous model, Equation (4.11b), are shown.

The magnitude response of the small-signal synchronous model and the small-signal non-synchronous model show a close correspondence with the response of the SABER averaged model before the resonant peak. The maximum absolute difference between the

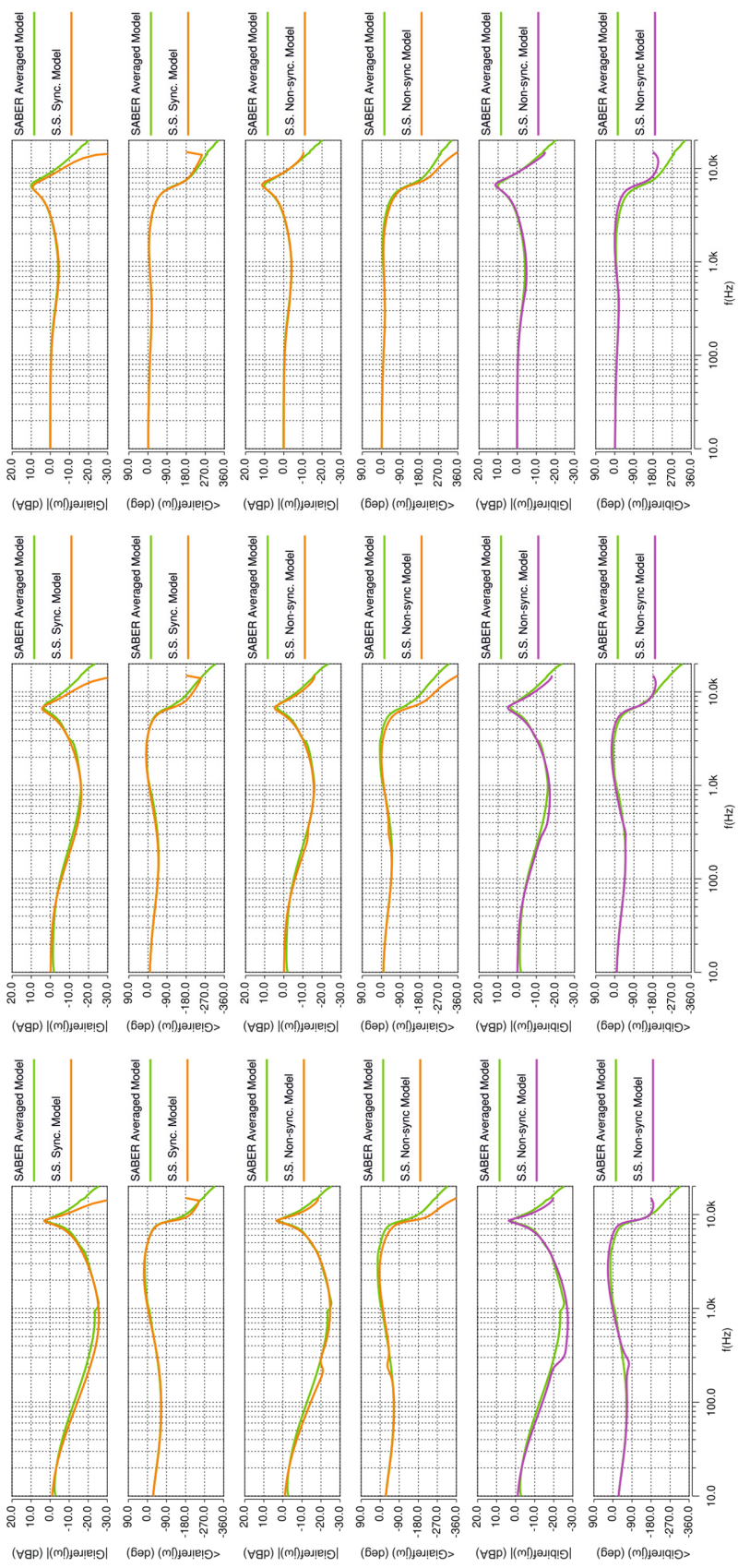

Figure 4.7. Frequency response of the closed-loop transfer function $G_{idiref}(s)$ for the SABER averaged model, the small-signal synchronous model and the small-signal non-synchronous model. Normal update mode, $t_{d\_proc} = (0.5)T = 16.66\ \mu s$. $V_{in} = 80\ V$, $R_{load} = 5.2\ \Omega$. *(a)* $I_{ref} = 13.6\ A$, $D = 0.25$; *(b)* $I_{ref} = 30.7\ A$, $D = 0.5$; *(c)* $I_{ref} = 123\ A$, $D = 0.75$.

signals in this range was found to be no more of *3 dBA* approximately for the phase-a current in all the range of operation. However, the magnitude of the phase-b current exhibits a drop of approximately *6 dBA* between *250 Hz* to *1 kHz* which is thought to be due to the interleaved interaction of the converter phases.

The magnitude and location of the resonant-peak frequency was measured for all the models and is presented in Table 4.5. As seen in the measurements, both the magnitude and the location of the resonant-peak are in close agreement for all the models. Similarly, the phase response of all the models below the resonant-peak frequency shows a close agreement with a difference of no more than *10 degrees*.

Table 4.5. Comparison of the magnitude and frequency location of the resonant peak in the frequency-response of the SABER averaged model, the small-signal synchronous model and the small-signal non-synchronous models.

Point of Operation	SABER averaged model	Small-signal synchronous model	Small-signal non-synchronous model
	Magnitude [dBA]		
***D = 0.25*, Figure 4.7(a)**	2.09	3.16	3.43
***D = 0.5*, Figure 4.7(b)**	3.50	4.30	4.83
***D = 0.75*, Figure 4.7(c)**	11.42	9.25	10.10
	Frequency [kHz]		
***D = 0.25*, Figure 4.7(a)**	8.63	8.59	8.59
***D = 0.5*, Figure 4.7(b)**	6.86	6.76	6.76
***D = 0.75*, Figure 4.7(c)**	6.60	6.42	6.69

Some of the differences observed in the synchronous and the non-synchronous models might be also produced by the discretization method employed to obtain the z-domain transfer functions of the model. The method employed was the ZOH method, which is known to discretize a system with high accuracy in the time-domain only for stair-case inputs [1,2]. Other methodologies exist, such as the Tustin approximation or the Zero-Pole Matching method, which can be employed to obtain a better approximation of the response of the system in the frequency domain.

For frequencies above the resonant frequency, the magnitude of the small-signal synchronous model drops with a steeper slope than the SABER averaged model in all the points of operation considered. Meanwhile, the magnitude of the non-synchronous model corresponds closely to the magnitude of the SABER averaged model. Conversely, the phase response of the synchronous model shows close agreement with the predictions of the SABER averaged model, whilst the non-synchronous model shows an increased phase-shift in the response of phase-a and a reduced phase shift in the response of phase-b. This is attributed to the time-delay and the time-advance units employed to model the interleaved sampling operation of the converter phases.

4.4.3. Stability range with a digital PI compensator

In this section the stability of the transfer functions $G_{iairef}(z)$ and $G_{ibiref}(z)$ obtained using the small-signal synchronous model, Equation (4.14), and the small-signal non-synchronous model, Equations (4.11a) and (4.11b), is compared when the control-loops are compensated with a digital PI controller. The MATLAB script found in Appendix B.2 was used to determine the stability of $G_{iairef}(z)$ and $G_{ibiref}(z)$ at a specific point of operation by evaluating the location of the poles for several combinations of proportional gain, K_p, and integral gain, K_i. For each iteration the data obtained was stored in a file together with the corresponding values of K_p and K_i and was plotted using ORIGINLAB. The analysis was undertaken for several points of operation to ensure the consistency of the data and the predictions of the small-signal models.

The graphs depicted in Figures 4.8 and 4.9 summarize the data acquired for four of the different points of operation examined employing the normal-update mode of the DPWM modules, in other words, $t_{d\_proc} = 0.5(T)$. Once more, the parameters of the converter are listed in Table 4.3. In the graphs, the results of the synchronous model are plotted in green whilst the ones corresponding to the non-synchronous model are plotted in orange. The stability range in these graphs is the shadowed region bound by the maximum values of K_p and K_i for which the system poles are stable and the minimum K_p and K_i values that were tested ($K_p = 0.005(T)$ and $K_i = 0.01$). To map out the stability region K_p and K_i were increased logarithmically up to $100(T)$ and 100 respectively.

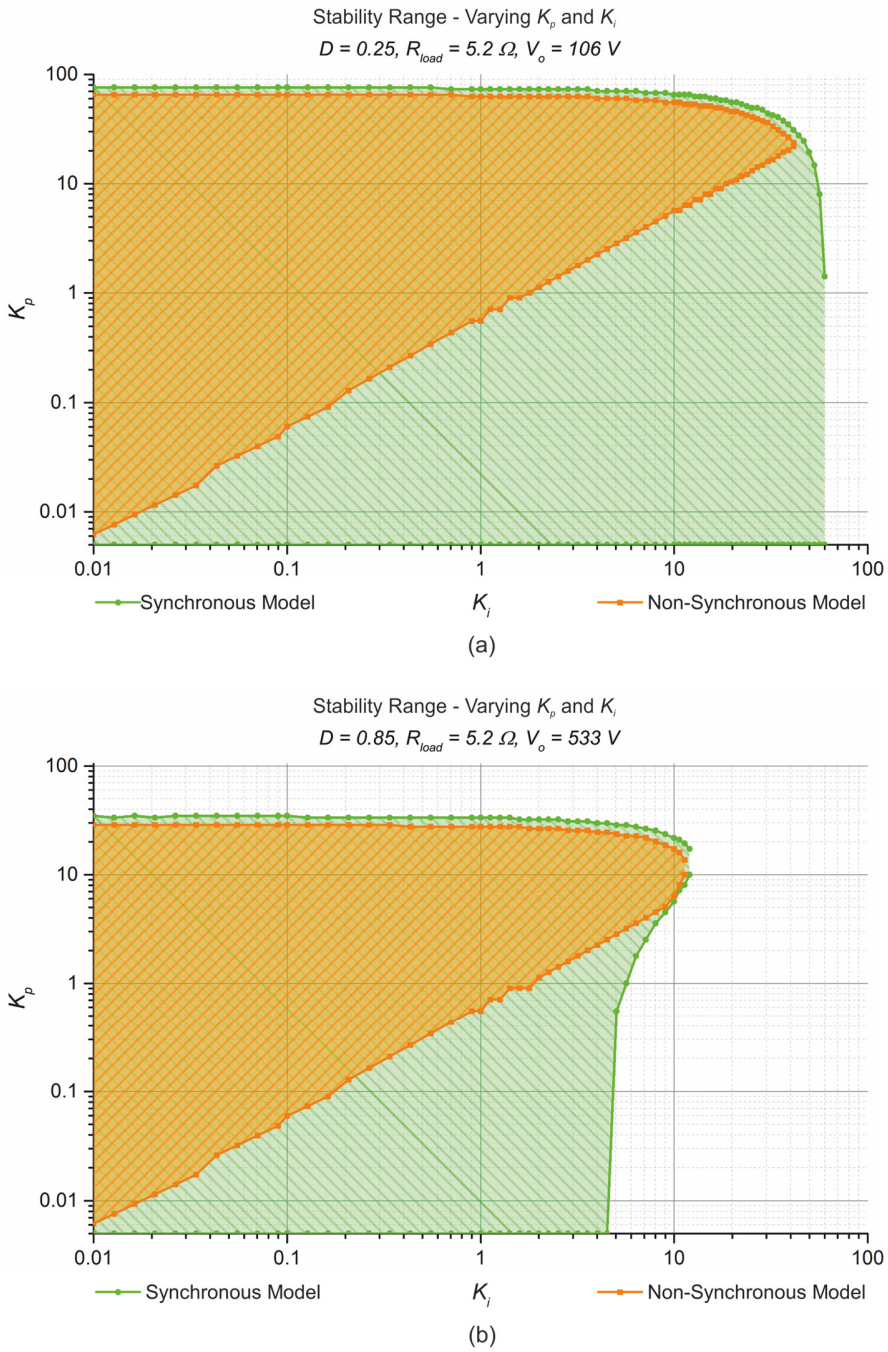

Figure 4.8. Stability-range predicted by the synchronous model and the non-synchronous model of the converter employing a digital PI controller. Normal update mode, $t_{d\_proc} = (0.5)T = 16.66\ \mu s$. (a) $R_{load} = 5.2\ \Omega$, $D = 0.25$, $I_{in} = 27.34\ A$, $V_{in} = 80\ V$; (b) $R_{load} = 5.2\ \Omega$, $D = 0.85$, $I_{in} = 246\ A$, $V_{in} = 80\ V$.

Figures 4.8(a) and 4.8(b) depict the results obtained employing $V_{in} = 80\ V$ and $R_{load} = 5.2\ \Omega$ for the points of operation $D = 0.25$ and $D = 0.85$. These results show the evolution of the stability range as the duty ratio is increased. Similarly, the graphs depicted in Figures 4.9(a) and 4.9(b) depict the results obtained using the conditions $V_{in} = 80\ V$ and $R_{load} = 2.8$

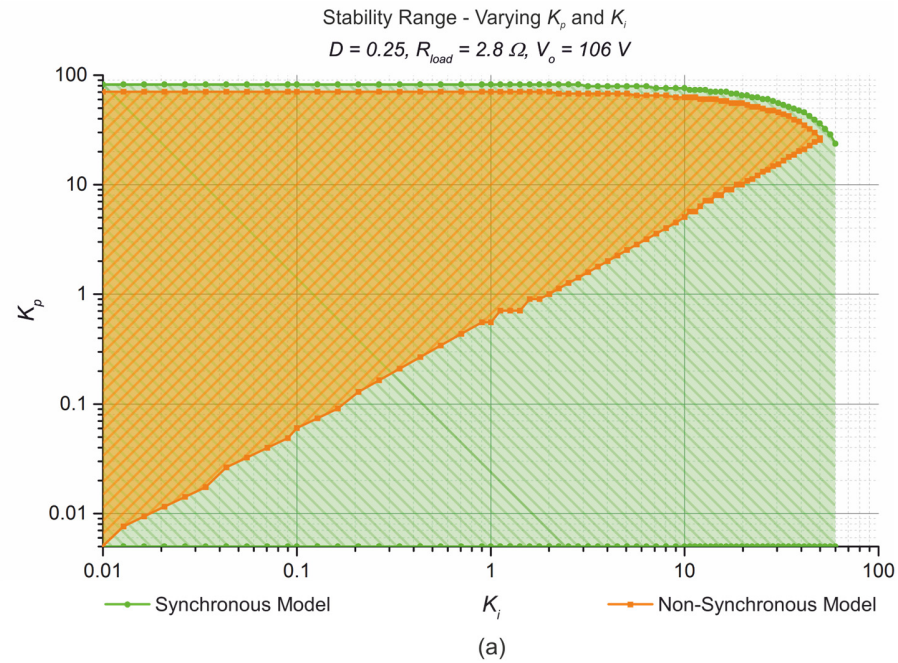

Figure 4.9. Stability-range predicted by the synchronous model and the non-synchronous model of the converter employing a digital PI controller. Normal update mode, $t_{d\_proc} = (0.5)T = 16.66\ \mu s$. (a) $R_{load} = 2.8\ \Omega$, $D = 0.25$, $I_{in} = 50.6$ A, $V_{in} = 80$ V; (b) $R_{load} = 2.8\ \Omega$, $D = 0.85$, $I_{in} = 457$ A, $V_{in} = 80$ V.

Ω for $D = 0.25$ and $D = 0.85$. From the graphs, it is evident that there is a clear difference in the lower stability limit predicted by the models. The K_p and K_i stability region is approximately rectangular using the synchronous model, whereas the region is almost halved with the non-synchronous model. In particular with low values of K_p and higher

values of K_i the synchronous model suggests the system will be stable whereas the non-synchronous model predicts the opposite. The results also show that the $K_p \backslash K_i$ stability region reduces at higher duty-ratio, but is only slightly affected by a reduced load resistance.

Figure 4.10, shows a similar graph to those found in Figure 4.8 and 4.9. In this graph, the stability range of the non-synchronous model with immediate update mode, $t_{d\_proc} = 0.1(T)$, is compared against the one with half-cycle delayed update, $t_{d\_proc} = 0.5(T)$. The point of operation where this graph was obtained is for the conditions $V_{in} = 85$ V, $R_{load} = 5.2\ \Omega$, $D = 0.5480$, $I_{in} = 80$ A, which was chosen as an example amongst several other points of operation that were evaluated as a similar pattern was observed. As seen from the graph, the stability range of the system is significantly increased when the PWM module is immediately updated after the duty ratio calculations.

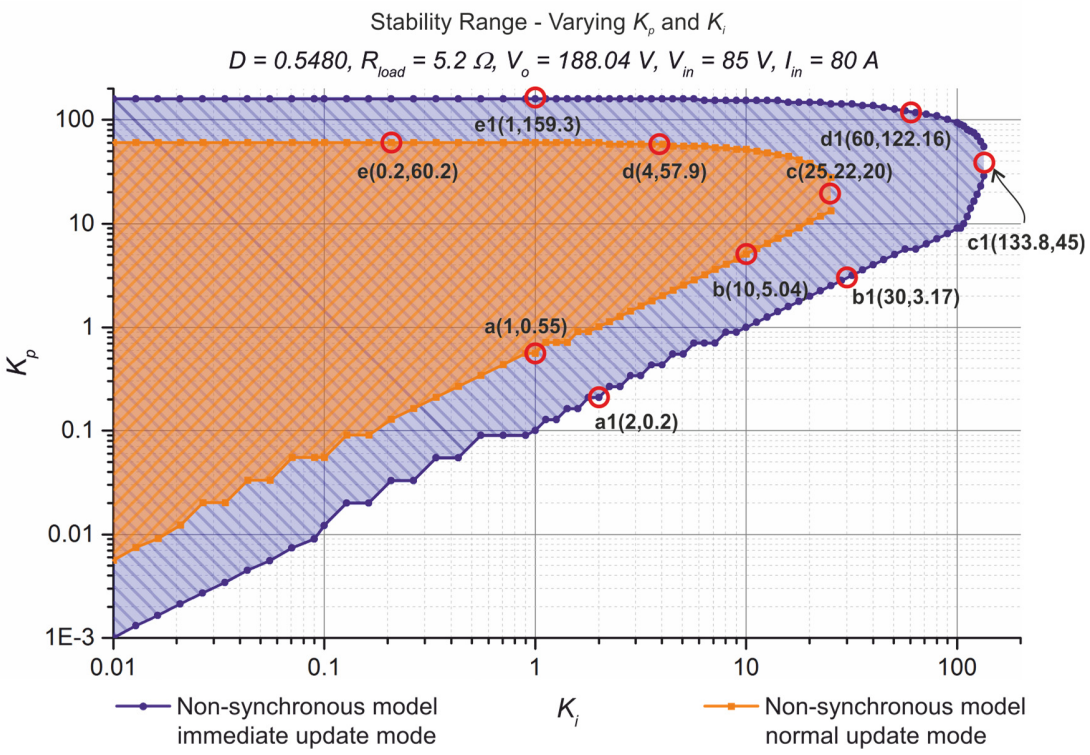

Figure 4.10. Comparison of the stability-range predicted by the non-synchronous model with immediate update mode, $t_{d\_proc} = (0.1)T = 3.33\ \mu s$, and the small-signal non-synchronous model with normal update mode, $t_{d\_proc} = (0.5)T = 16.66\ \mu s$. Compensator: digital PI controller, Backward-Euler implementation. $V_{in} = 85$ V; $R_{load} = 5.2\ \Omega$, $D = 0.5480$, $I_{in} = 80$ A.

To check the stability limit predicted by the small-signal non-synchronous model, a number of points around the parameter combinations, denoted points *a-e* and *a1-e1* in

Figure 4.10, were examined using the SABER averaged model. To run these simulations, the system was first taken to the desired point of operation with $K_p = 30(T)$ and $K_i = 20$. Once the system reached the steady state, K_p and K_i were switched to the values required and the system was perturbed employing a 5% step-increment in the reference-current. For every point identified in the graphs of Figure 4.10, two points in the surrounding points were selected and simulated.

The points evaluated are summarized in Table 4.6 and the simulation results obtained for each of the points of operation can be found in Figures E.1 to E.4 of Appendix E. As seen in Table 4.6, the predictions of the non-synchronous model are in agreement with the stability range observed using the SABER averaged model. The small difference in the predictions was attributed to the size of the step in the proportional gain when the $K_p \backslash K_i$ stability region graphs were generated.

Table 4.6. Comparison of the stability limits predicted by the non-synchronous model and the SABER averaged model. (Figure 4.10).

Non-synchronous model $(K_i, K_p(T))$	**SABER averaged model** $(K_i, K_p(T))$	
a(1,0.55(T))	*(1,0.7(T)) – Stable*	*(1,0.4(T)) - Unstable*
b(10,5.04(T))	*(10,6(T)) - Stable*	*(10,4(T)) - Unstable*
c(25.22,20(T))	*(24,20(T)) - Stable*	*(26,20(T)) - Unstable*
d(4,57.9(T))	*(4,60(T)) - Unstable*	*(4,56(T)) - Stable*
e(0.2,60.2(T))	*(0.2,63(T)) - Unstable*	*(0.2,58(T)) - Stable*
a1(2,0.2(T))	*(2,0.4(T)) - Stable*	*(2,0.2(T)) - Unstable*
b1(30,3.17(T))	*(30,4(T)) - Stable*	*(30,2(T)) - Unstable*
c1(133.8,45(T))	*(131,45(T)) - Stable*	*(135,45(T)) - Unstable*
d1(60,122.16(T))	*(60,124(T)) - Unstable*	*(60,121(T)) - Stable*
e1(1,159.3(T))	*(1,163(T)) - Unstable*	*(1,157(T)) - Stable*

4.4.4. Experimental validation of the stability range

To evaluate experimentally the stability region of the converter, the system described in Section 3.7, Chapter 3, was started-up with a programmed reference phase-current of *40 A* and with a set of initial values for K_p and K_i. The initial values for K_p and K_i were *10(T)* and *1* for the normal update algorithm and *12.5(T)* and *1* for the immediate

update algorithm. Once the converter reached the steady-state operation, the initial values of K_p and K_i were replaced by the required values for the evaluation.

The DSC was programmed to evaluate six different discrete values of K_p per experiment, which were selected employing the potentiometer that in previous experiments was used to select the reference-current. To range K_i the DSC had to be reprogrammed. The additional code to generate this program created an extra delay in the processing time which will have an impact on the stability range of the immediate update algorithm. The t_{d_proc} measured was of 4.9 µs, or 0.*147(T)*, compared with the *4.2* µs measured in Section 3.7.2, Chapter 3, when no extra-tasks other than controlling the converter phase-currents are undertaken by the DSC.

Figure 4.11(a) and 4.11(b) depict a comparison of the stability range predicted by the small-signal non-synchronous model and the stability limit observed using the converter prototype. Figure 4.11(a) corresponds to the normal update algorithm whilst Figure 4.11(b) corresponds to the immediate update algorithm. The point of operation evaluated corresponds to V_{in} *= 85 V,* R_{load} *= 5.2 Ω, D = 0.5480* and I_{in} *=80 A,* identical to that shown in the graphs of Section 4.3.3. The green shadowed area corresponds to the stability range predicted by the small-signal non-synchronous model, whilst the blue data-points represent the combination of K_p and K_i for which the practical system was stable and the red data-points correspond to the ones where instability was observed. To provide evidence of the experimental results, the highlighted points in the graphs were captured and included in Appendix E, Figures E.5 to E.8. In the experimental results shown, for any value of K_i, the precise position of the stability limit is somewhere between the last value of K_p that was found to be stable and the first where instability was observed.

The discrepancies observed might be attributed to several practical factors that were disregarded in the modelling procedure, such as the quantization non-linearity and limited resolution of both the ADC and the DPWM modules, non-zero switching transitions and non-linear behaviour of the switching devices, variations in the parameters of the current transducers and the components used to measure and condition the feedback signals, and small discrepancies in the parameters of the components integrating the converter phases, amongst others.

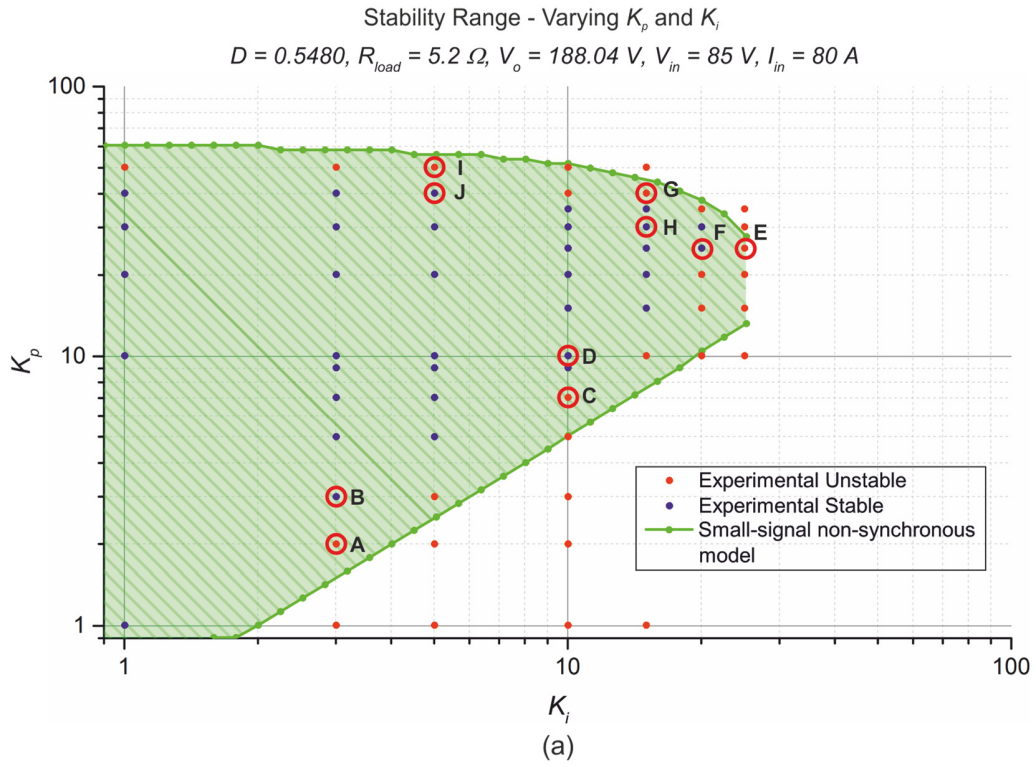

Figure 4.11. Comparison of the stability-range predicted by the non-synchronous model against the experimental stability-range measured with the converter prototype. (a) Normal update mode t_{d_proc} = (0.5)T = 16.66 µs (b) Immediate update mode, t_{d_proc} = (0.147)T = 4.9 µ, D = 0.5480, R_{load} = 5.2 Ω, V_{in} = 85 V, I_{in} = 80 A.

4.5. Summary

The sampler decomposition technique was used to model the interleaved sampling operation of the current feedback loops in an average-current controlled, dual-interleaved converter. The small-signal dynamics of the converter were represented using the small-signal averaged model developed in Chapter 2. The closed-loop, transfer functions that relate small-changes in the reference-current to small-changes in the phase-currents were derived for two cases: when the interleaved sampling is disregarded, synchronous model, and when the interleaved sampling is modelled. It was found that the transfer-functions for each phase are identical and greatly simplified when the interleaved sampling is disregarded. Conversely, when the interleaved sampling was taken into account, different transfer functions were found for each phase of the converter.

A comparison between the closed-loop transfer functions from the synchronous and the non-synchronous model was undertaken using time domain step-responses and frequency domain responses. Furthermore, to validate the models developed, these results were compared with simulation results from a switched and a large-signal averaged model implemented in SABER simulator.

The transient response of the models to *5 %* disturbances, showed an excellent agreement with the SABER simulations and the mathematical models showed no significant difference between their predictions. In the frequency domain, both models showed a good agreement with the simulation results presenting a deviation of no more than approximately *1 dBA* in the magnitude response over most of the operating range, but increasing at low power, and no more than *10 degrees* in the phase response for frequencies up to approximately *8 kHz*. However, for frequencies above *8 kHz* the transfer-functions of the non-synchronous model showed differences in the phase response, which are likely to be caused by the time-advance and time-delay units employed to model the interleaved interaction of the control-loops.

The stability-range comparison confirmed that the interleaved operation of the converter phases has a detrimental effect on the stability of the system and that the synchronous model fails to predict this behaviour. The stability range predicted by the non-

synchronous model was further validated by simulation and experimental results, showing an excellent agreement with the simulation results from the SABER averaged model and a good agreement with the pattern of stability observed in the experimental results.

4.6. References

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Chapter 5
Digital control loop: dynamics and design

5.1. Introduction

In the first section of this Chapter, the small-signal model of the DIBC developed in Chapter 4 is used to provide further insight into the system dynamics and stability limits by examining the loci of the system poles as the main parameters are changed. Several root-loci were generated with the aid of MATLAB to illustrate the trajectories of the poles when the quiescent duty-ratio is varied from *0.2* to *0.8* in steps of *0.05*. The sensitivity of the trajectories to the main system parameters are then examined in turn.

In the second section, the parameters of the digital PI compensator employed to regulate the system are selected based on the models and theory developed in this thesis. The objective was to ensure stability and minimum settling time to step-responses over a defined range of operation. The design exercise is performed using the small-signal non-synchronous model with immediate DPWM update developed in Chapter 4.

5.2. Sensitivity analysis via Root-locus

In this section, the sensitivity of the pole trajectories from the small-signal non-synchronous model developed in Chapter 4, Equations (4.12a) and (4.12b), to parameter variations is discussed. The root-loci generated are organized as shown in Table 5.1.

5.2.1. Varying load resistance with a proportional compensator

In Figure 5.1, the trajectories of the system poles are depicted when the duty-ratio and the load resistance are varied from *0.2* to *0.8* and from *1.4 Ω* to *10.4 Ω* respectively.

Table 5.1. Root-locus plots generated to analyse the behaviour of the closed-loop poles of the small-signal non-synchronous model.

	Section	Figure	Duty-ratio *D*	Input voltage V_{in}	Load resistance R_{load}	Proportional gain K_p	Integral gain K_i	Processing time t_{d_proc}
Proportional	5.2.1	5.1	*0.2 -> 0.8*	*80 V*	*1.4Ω, 2.6Ω, 5.2Ω, 10.4Ω*	*1(T)*	-	*0.5(T)*
	5.2.2	5.2	*0.2 -> 0.8*	*80 V*	*5.2 Ω*	*1(T), 5(T), 10(T), 20(T), 30(T), 40(T)*	-	*0.5(T)*
Proportional plus Integral	5.2.3	5.3	*0.2 -> 0.8*	*80 V*	*5.2 Ω*	*1(T), 5(T), 10(T), 20(T), 30(T), 40(T)*	*1* *10* *20*	*0.5(T)*
	5.2.4	5.4	*0.2 -> 0.8*	*80 V*	*10.4 Ω* *5.2 Ω* *2.6 Ω*	*1(T), 20(T), 40(T)*	*10*	*0.5(T)*
	5.2.5	5.5	*0.2 -> 0.8*	*80 V*	*5.2 Ω*	*20(T)*	*10*	*0.1(T), 0.3(T), 0.5(T)*
	5.2.6	5.6	*0.2 -> 0.8*	*50 V* *120 V*	*5.2 Ω*	*1(T), 20(T),40(T)*	*10*	*0.5(T)*

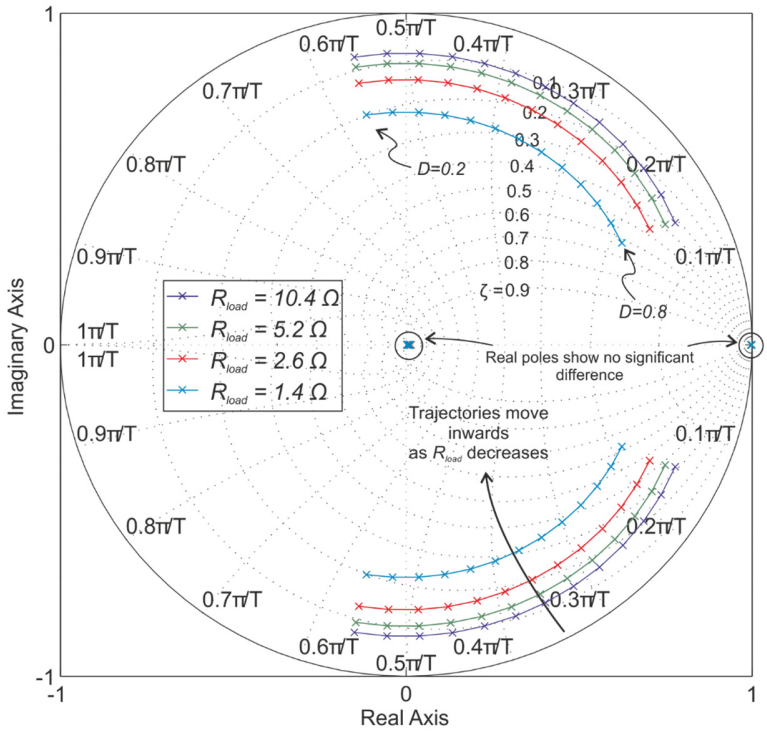

Figure 5.1. Root-locus of the poles of closed-loop transfer functions $G_{iairef}(z)$ and $G_{ibiref}(z)$ of the small-signal non-synchronous model. Compensator: digital proportional controller with $K_p = 1T$. Ranging *D* from *0.2* to *0.8* and R_{load} from *1.4 Ω* to *10.4 Ω*. V_{in} = *80 V*.

A proportional compensator of $K_p = 1T$ was used throughout in both phases. The root-locus comprises a pair of conjugated complex poles and three real-axis poles: one close to the *+1* point and two at the origin. As seen in the figure, the trajectory of the complex-conjugated poles moves around the unitary circle and towards the real positive axis as the duty ratio is increased, indicating a reducing natural frequency in the time-domain. If the load resistance is decreased, the trajectories are displaced concentrically towards the centre of the unit circle, increasing the damping of the poles. The three real-axis poles showed no significant movement over the range of the parameter variations.

5.2.2. Varying proportional gain of the proportional compensator

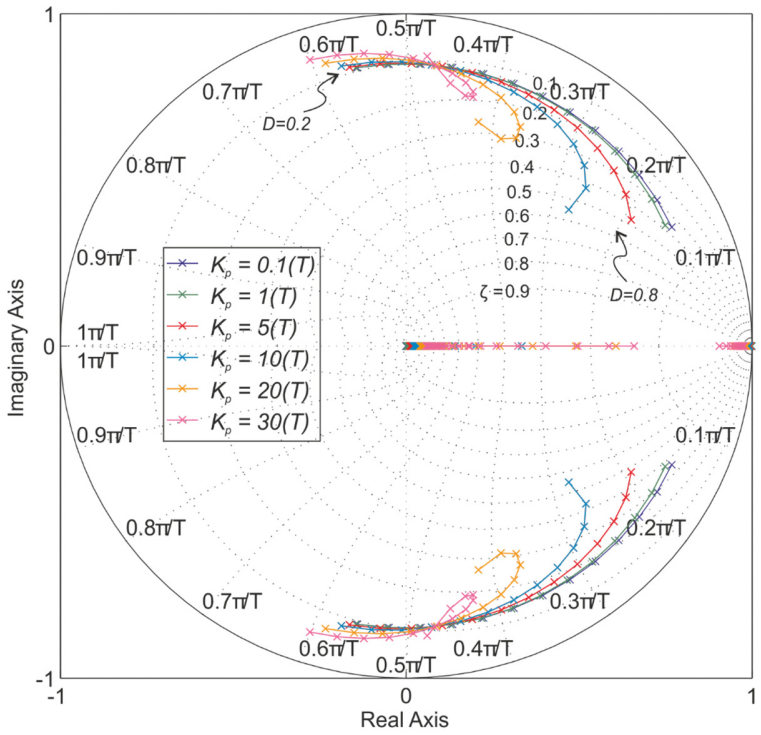

Figure 5.2. Root-locus of the poles of closed-loop transfer functions $G_{iairef}(z)$ and $G_{ibiref}(z)$ of the small-signal non-synchronous model. Compensator: digital proportional controller. *D = 0.2* to *0.8*; K_p = *0.1(T), 1(T), 5(T), 10(T), 20(T), 30(T)*; R_{load} = *5.2 Ω*; V_{in} = *80 V*.

Figure 5.2 depicts the root-locus of the system poles when the proportional gain is increased from *0.1(T)* to *30(T)*. In this plot, the load resistance was fixed to a value *5.2 Ω*. As seen in the plot, the trajectory of the complex poles curves initially towards the centre of the unit circle and then turns back on itself as K_p is increased. In addition, the real-axis

poles at the origin move to the right whilst the pole at the *+1* point moves to the left as K_p is increased.

5.2.3. Varying proportional gain and integral gain of the PI compensator

In the following sections the root-locus of the closed-loop system poles are examined when a digital proportional-integral compensator is employed to regulate the system. Similar to the previous sections, the group of plots in Figures 5.3 show the trajectories of the poles when the duty ratio is increased from 0.2 to 0.8 by 0.05 plus the evolution of these trajectories when K_p is varied from *1(T)* to *40(T)* and when K_i is equal to *1*, *5* and *10*. For each value of K_i examined, a general view of the unit circle and a magnified view of the poles located close to the *+1* point of the real axis are shown. Figures 5.3(a) and (b) depict the root-loci when the integral gain is fixed to $K_i = 1$; Figures 5.3(c) and (d) correspond to $K_i = 5$; and finally, Figures 5.3(e) and (f) correspond to $K_i = 10$.

The introduction of the PI compensator in the system generates an extra-pair of complex poles close to the real-axis and in the vicinity of the *+1* point. These poles will be referred to as the lower frequency complex conjugated poles from now on to distinguish them from the higher frequency pair of complex poles. It was found that the lower frequency complex poles determine the minimum K_p stability boundary that was observed in the stability-range graphs of Section 4.4.3. As the duty-ratio is increased the poles tend to move around the unit circle and away from the real-axis. Also in some cases, the trajectories of these poles lie outside the unit circle for small-values of K_p and move inwards as K_p is increased.

The movement of the higher frequency complex poles is similar to that observed in Figure 5.2, however as the duty-ratio increases the locus of some poles turns back on itself more sharply and moves outside the unit circle. This effect is stronger with larger values of K_i, Figures 5.3(c) and 5.3(e). The maximum K_p stability limit observed in the stability-range graphs of Section 4.4.3 was found to be directly related to these poles.

In summary, two main conclusions can be drawn, first, the maximum K_p stability limit which was identified in the stability-range plots of Section 4.4.3, is seen to be determined by the pair of high-frequency complex poles, and second, the minimum K_p stability limit is

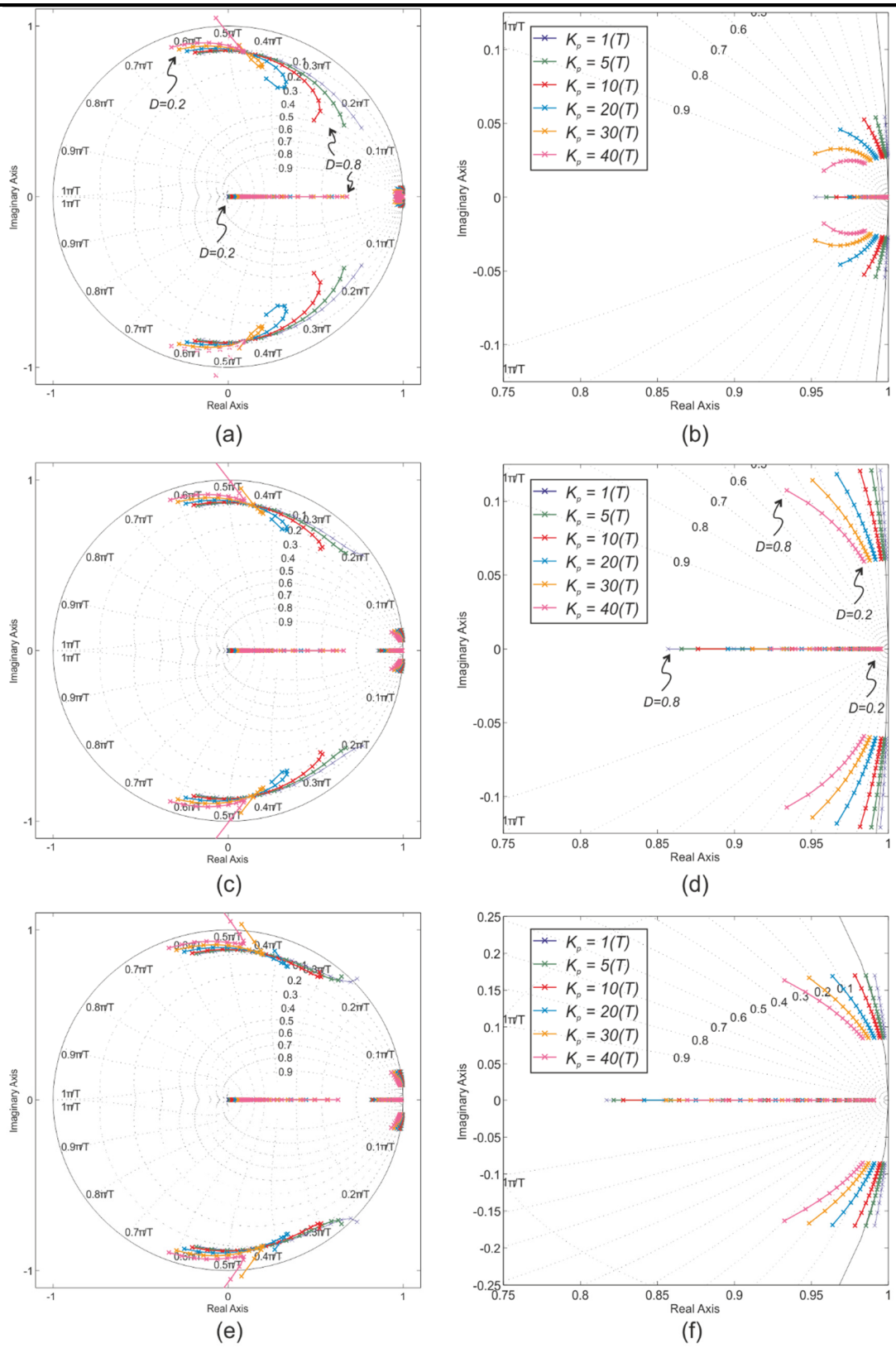

Figure 5.3. Root-locus of the poles of closed-loop transfer functions $G_{iairef}(z)$ and $G_{ibiref}(z)$ of the small-signal non-synchronous model. Compensator: digital PI controller. *D = 0.2* to *0.8; K_p = 1(T), 5(T), 10(T), 20(T), 30(T), 40(T); R_{load} = 5.2 Ω; V_{in} = 80 V*. (a)&(b) $K_i = 1$; (c)&(d) $K_i = 5$; (e)&(f) $K_i = 10$.

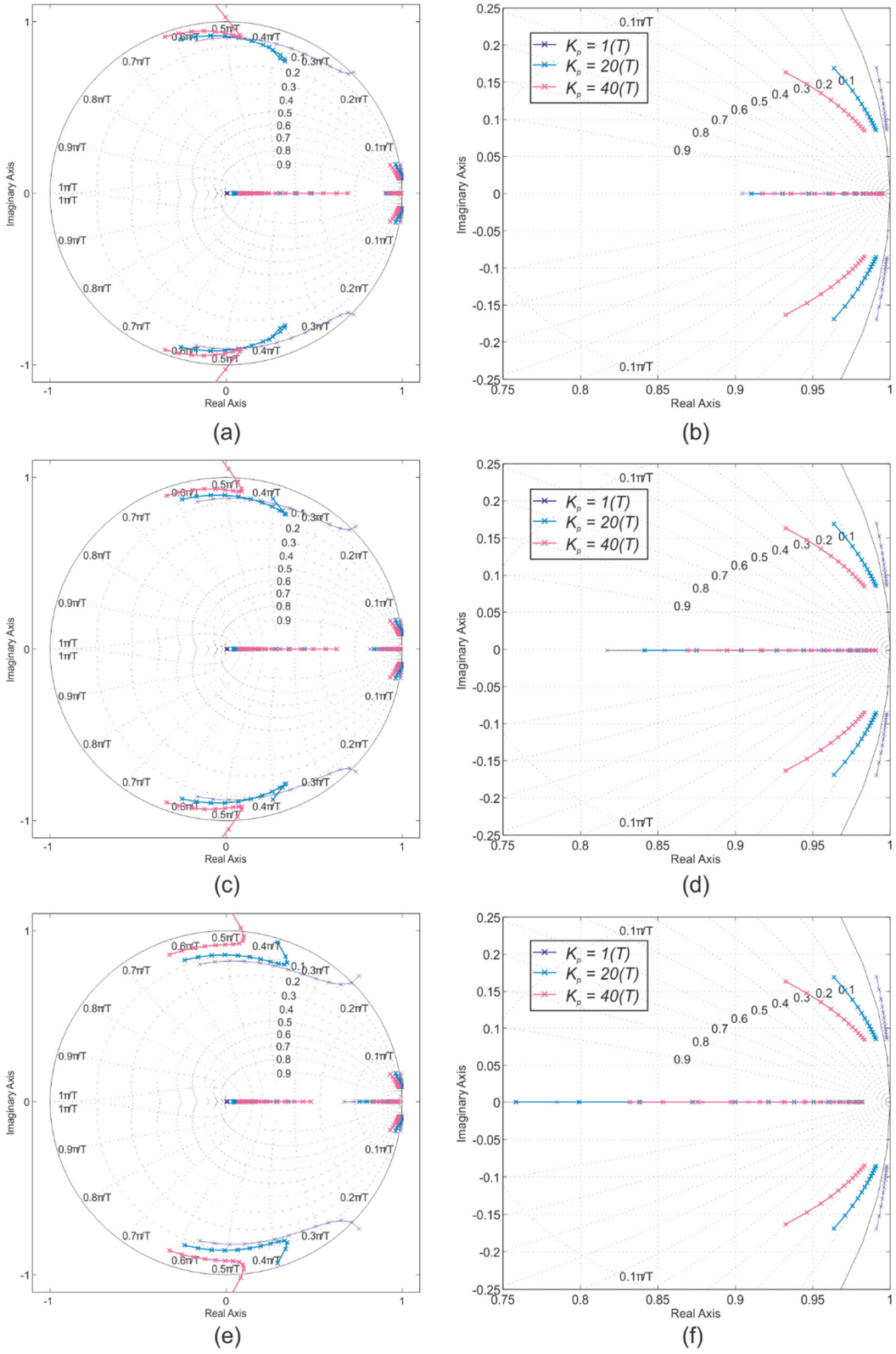

Figure 5.4. Root-locus of the poles of closed-loop transfer functions $G_{iairef}(z)$ and $G_{ibiref}(z)$ of the small-signal non-synchronous model. Compensator: digital PI controller. $D = 0.2$ to 0.8; $K_p = 1(T)$, $20(T)$ and $40(T)$; $K_i = 10$; $V_{in} = 80\ V$. (a)&(b) $R_{load} = 10.4\ \Omega$; (c)&(d) $R_{load} = 5.2\ \Omega$; (e)&(f) $R_{load} = 2.6\ \Omega$.

mainly determined by the pair of lower frequency complex poles which seem to be introduced by the PI compensator.

5.2.4. Varying load resistance with a PI compensator

Figure 5.4 depicts the trajectories of the system poles when *D* is increased from *0.2* to *0.8* in steps of *0.05* for different values of load resistance. The figures are arranged in a similar way to those presented in the previous section and they show a general view of the unit circle plus a close-up in the region of the *+1* point. For each value of resistance examined, the proportional gain was set to *1(T)*, *20(T)* and *40(T).* Figure 5.4(a) and (b) depict the trajectories for $R_{load} = 10.4\ \Omega$; Figure 5.4(c) and 5.4(d) correspond to $R_{load} = 5.2\ \Omega$; and Figure 5.4(e) and 5.4(f) correspond to $R_{load} = 2.6\ \Omega$. The integral gain was kept constant at $K_i = 10$ throughout.

The results show that the low frequency complex poles move outside the unit circle for the lowest value of K_p whereas the high frequency complex poles turn towards the unit circle and tend to cross over the circle as *D* increases, with the effect becoming more pronounced with lower values of load resistance, Figure 5.4(e).

5.2.5. Varying PWM update delay with a PI compensator

Figure 5.5 illustrates the root-locus of the system poles when t_{d_proc} is reduced from *0.5(T),* normal update mode of the DPWM, to *0.3(T)* and *0.1(T)*, immediate update mode of the DPWM. The point of operation selected to illustrate the pole trajectories was $R_{load} = 5.2\ \Omega$, $V_{in} = 80\ V$, $K_p = 20(T)$ and $K_i = 10$ with *D* ranging from *0.2* to *0.8* by *0.05*.

The plot of Figure 5.5(a) shows that a reduction of t_{d_proc} has a favourable impact on the position of the complex poles. The trajectories of the high frequency complex poles as *D* is increased turn towards the centre of the unit circle. In addition, the trajectories of the lower frequency complex poles also move further into the unit circle, Figure 5.5(b), although the movement is not as great as seen for the higher frequency poles. Once more, these results further illustrate the increase in stability-range depicted in the graph of Figure 4.10 with immediate update mode, Chapter 4, Section 4.4.3.

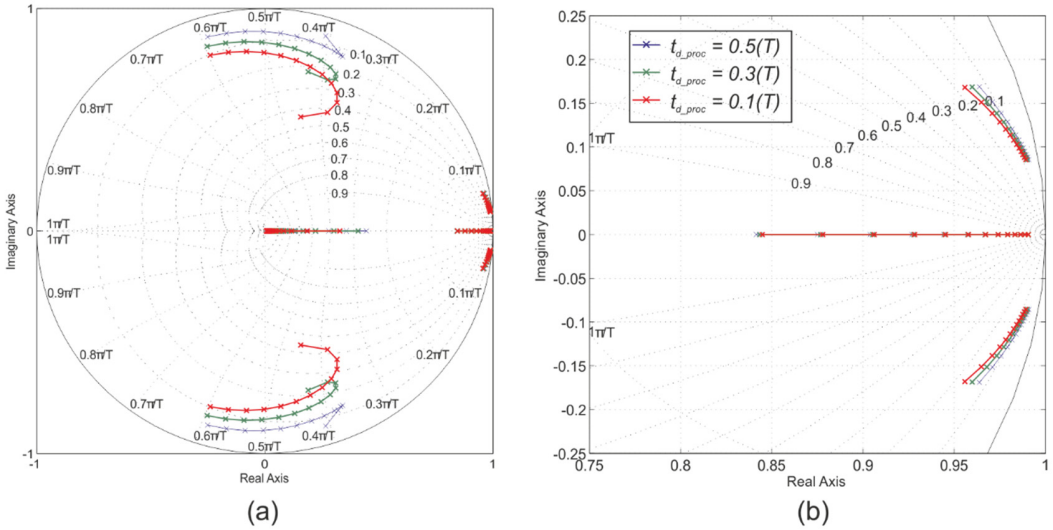

Figure 5.5. Root-locus of the poles of closed-loop transfer functions $G_{iairef}(z)$ and $G_{ibiref}(z)$ of the small-signal non-synchronous model. Compensator: digital PI controller. $D = 0.2$ to 0.8; $t_{d\_proc} = 0.1(T), 0.3(T), 0.5(T)$; $K_p = 20(T)$; $K_i = 10$; $R_{load} = 5.2\ \Omega$; $V_{in} = 80\ V$.

5.2.6. Varying input voltage with a PI compensator

Figure 5.6 illustrates the system pole trajectories for different values of input voltage. Figures 5.6(a) and 5.6(b) correspond to $V_{in} = 50\ V$ whilst Figures 5.6(c) and 5.6(d) correspond to $V_{in} = 120\ V$. Figures 5.4(c) and 5.4(d) can be used as a reference point when $V_{in} = 80\ V$. The fixed conditions that were used to obtain these plots are $R_{load} = 5.2\ \Omega$, $V_{in} = 80\ V$, $K_i = 10$. The trajectories of the poles are illustrated for values of K_p equal to $1(T)$, $20(T)$ and $40(T)$. From these graphs, it can be concluded that the stability-range of the system is reduced as the input voltage is increased since the trajectories of the poles tend to move outside the unitary circle. However, consistent with what has been seen previously, the lower frequency complex poles remain outside the unit circle for the lowest value of K_p, $K_p = 1(T)$.

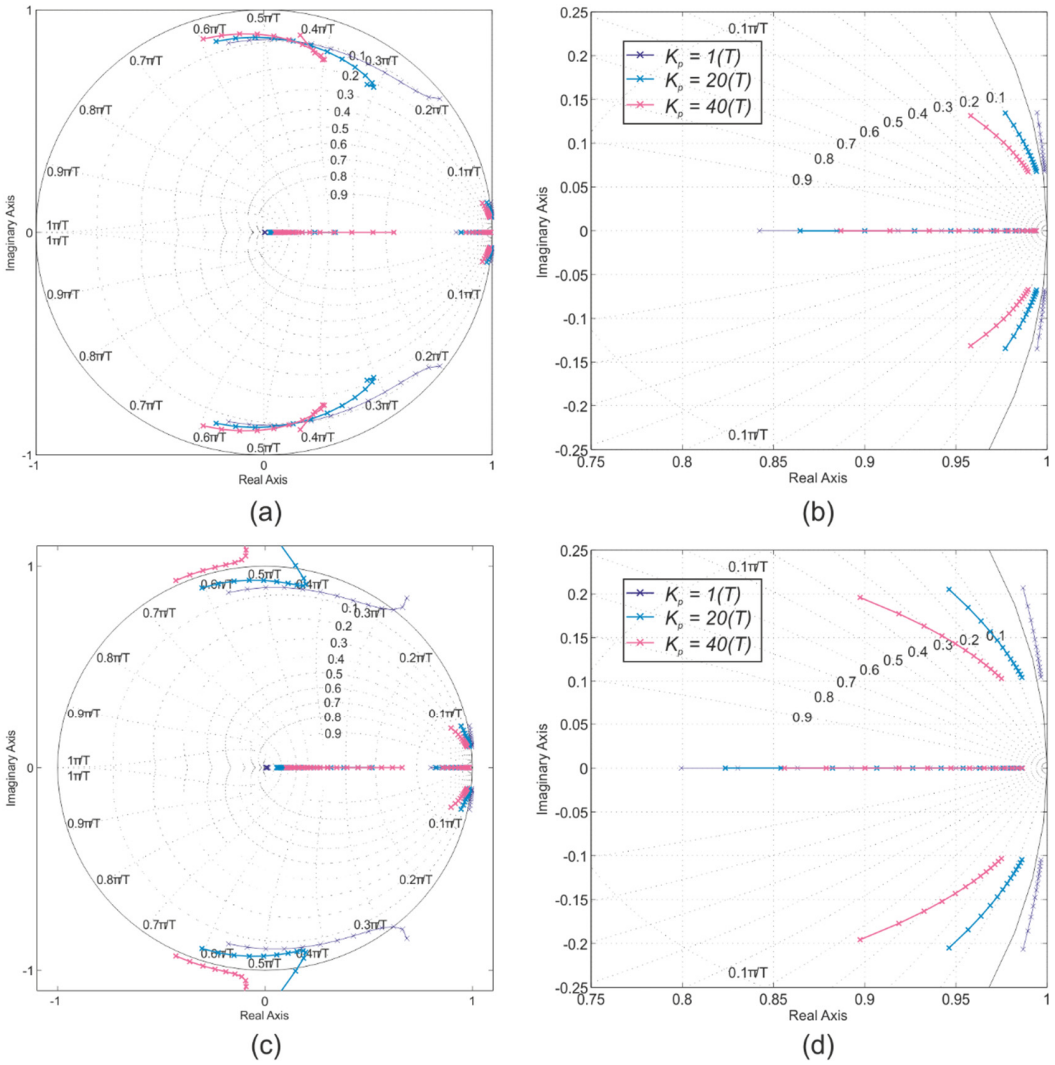

Figure 5.6. Root-locus of the poles of the closed-loop transfer functions $G_{iairef}(z)$ and $G_{ibiref}(z)$ of the small-signal non-synchronous model. Compensator: digital PI controller. *D = 0.2* to *0.8; K_p = 1(T), 20(T) and 40(T); K_i = 10; R_{load} = 5.2 Ω*. (a)&(b) *V_{in} = 50 V*; (c)&(d) *V_{in} = 120 V*.

5.3. Design of the PI compensator for digital average-current control with immediate update mode

The design method is based on the $K_p\backslash K_i$ stability-range plots introduced in Section 4.4.3, Chapter 4, as they offer an effective way to visualize the stability range of the system with a compensator. The transient performance of the system was evaluated using step responses generated from the non-synchronous model implemented in MATLAB.

The range of operation of the system, Table 5.2, was selected according to the maximum operating conditions of the converter prototype and the maximum ratings of the laboratory equipment that was readily available. In order to identify the necessary $K_p\backslash K_i$ plots to proceed with the design, the conditions of the system at the extremes of the operation range were identified and calculated. Table 5.3 summarizes these conditions.

Table 5.2. Range of operation of the converter for the design of the digital PI controller.

	Input Voltage	Input Current	Input Power	Output Voltage
Minimum	*50 V*	*60 A*	*3 kW*	*125 V*
Maximum	*100 V*	*120 A*	*12 kW*	*250 V*

Table 5.3. Extremes of operation for the design of the digital PI controller.

Parameter Name	Minimum input voltage/ Minimum input Current	Maximum input voltage/ Minimum input current
Input Voltage, V_{in}	*50 V*	*100 V*
Input Current, I_{in}	*60 A*	*60 A*
Load Resistance, R_{load}	*5.2 Ω*	*5.2 Ω*
Output Power, P_o	*3000 W*	*6000 W*
Output Voltage, V_o	*125 V*	*176 V*
Duty-ratio, D	*0.6*	*0.43*

Parameter Name	Minimum input voltage/ Maximum input current	Maximum input voltage/ Maximum input current
Input Voltage, V_{in}	*50 V*	*100 V*
Input Current, I_{in}	*120 A*	*120 A*
Load Resistance, R_{load}	*5.2 Ω*	*5.2 Ω*
Output Power, P_o	*6000 W*	*12000 W*
Output Voltage, V_o	*172 V*	*250 V*
Duty-ratio, D	*0.71*	*0.6*

The $K_p\backslash K_i$ stability-range plots of the converter were generated and compared for the four points of operation listed in Table 5.3, using the converter parameters shown in Table 5.4 and with the system operated in immediate update mode assuming a processing time of $t_{d\_proc} = 4.12\ \mu s$. The value of t_{d_proc} corresponds to the value measured using the converter prototype in Section 3.7.2, Chapter 3. The comparison revealed that the stability-range of the system at maximum power, *12 kW*, was enclosed by the stability-range of the other points of operation evaluated, indicating that the combination of maximum input voltage and maximum input current (maximum output power) yield the worst case of stability. Figure 5.7 illustrates the $K_p\backslash K_i$ stability-range for this point of operation, where the highlighted points, A1 - D3, show the combinations of proportional and integral gains chosen to evaluate the step performance of the system.

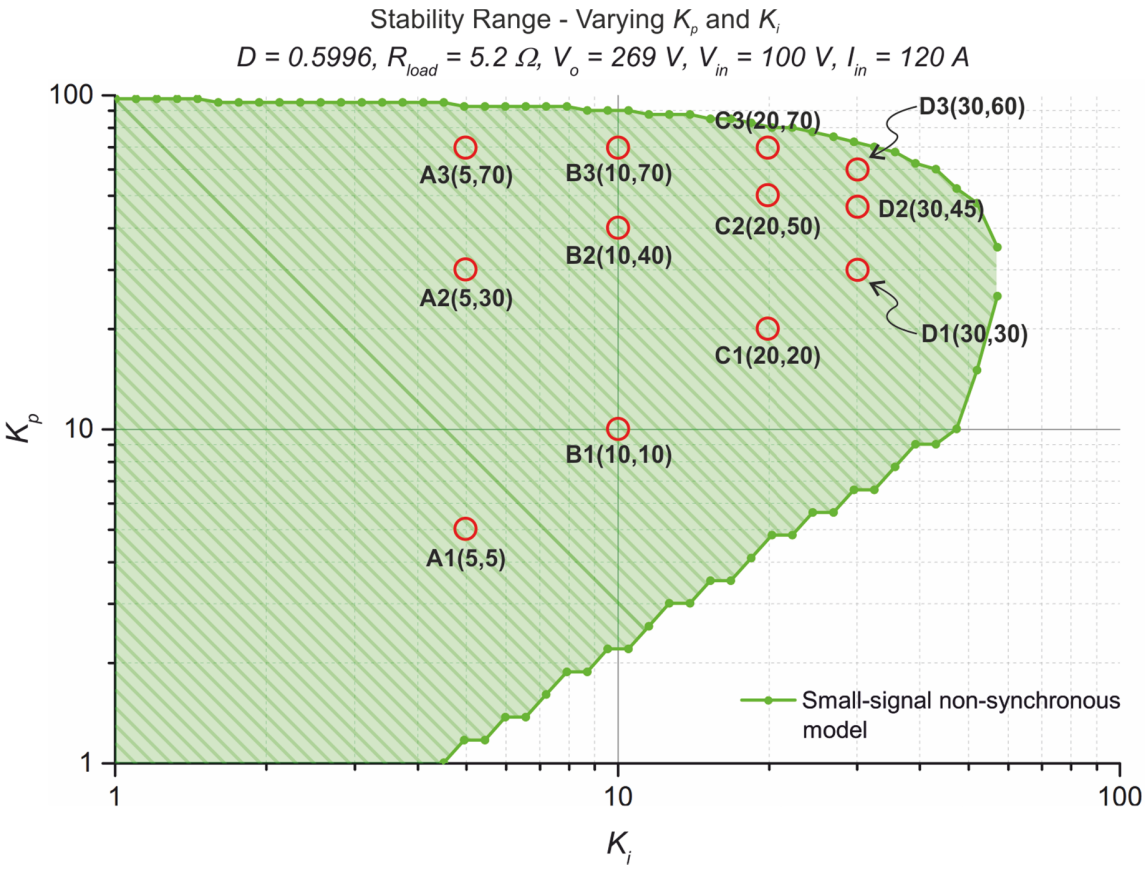

Figure 5.7. Stability-range predicted by the non-synchronous model for the design of the PI compensator. Immediate update mode, $t_{d\_proc} = (0.126)T = 4.12\ \mu s$. $D = 0.599$, $R_{load} = 5.2\ \Omega$, $V_{in} = 100$ V, $I_{in} = 120$ A. *(Worst case scenario for stability of the design).*

Table 5.4. Attributes of the converter and the DSC employed for the simulations.

Power Converter

Input inductance at 60 kHz	*5.12 µH*
IPT windings self-inductance at 30kHz	*75.14 µH*
Coupling coefficient of the IPT windings	*0.997*
Output capacitance	*45 µF*
Transistor turn-on/off delay*	*520 ns*
Switching frequency	*30 kHz*

Digital Signal Controller

Master clock frequency*	*150 Mhz*
ADC sampling delay*	*140 ns* phase-a, *220 ns* phase-b
Compensation network	Digital PI, Backward-Euler implementation

* SABER switched model only.

The results shown in Figures 5.8 and 5.9 show the transient response of the converter phase currents to a unit step-increment in the reference-current for the combinations *A1* to *D3* highlighted in Figure 5.7. In these figures an overview of the response is accompanied by a magnified view which details the initial oscillatory behaviour of the responses. The converter parameters used in MATLAB are shown in Table 5.4 and the point of operation employed for the evaluation corresponds to the maximum input voltage/maximum input current combination shown in Table 5.3.

Figures 5.8(a) and 5.8(b) depict the transient response when $K_i = 5$ and $K_p = 5(T)$, *30(T)* and *70(T)*, points A1 to A3 in Figure 5.7. Figures 5.8(c) and 5.8(d) correspond to $K_i = 10$ and $K_p = 10(T), 40(T)$ and *70(T)*, points B1 to B3 in Figure 5.7. Figures 5.8(e) and 5.8(f) correspond to $K_i = 10$ and $K_p = 20(T), 50(T)$ and *70(T)*, points D1 to D3 in Figure 5.7. Finally, Figures 5.9(a) and 5.9(b) correspond to $K_i = 10$ and $K_p = 30(T), 45(T)$ and *60(T)*, points E1 to E3 in Figure 5.7. In addition, Table 5.5 summarizes the maximum over-shoot and settling time measured for all the results depicted.

As expected from the root-locus analysis, two natural frequencies are evident in the responses, a lower frequency component which is related to the pair of complex z-domain poles close to the *+1* point and a higher frequency due to the second pair of complex poles. The lower frequency oscillation becomes more pronounced with lower values of K_p whilst the higher frequency component becomes more obvious with larger values of K_p.

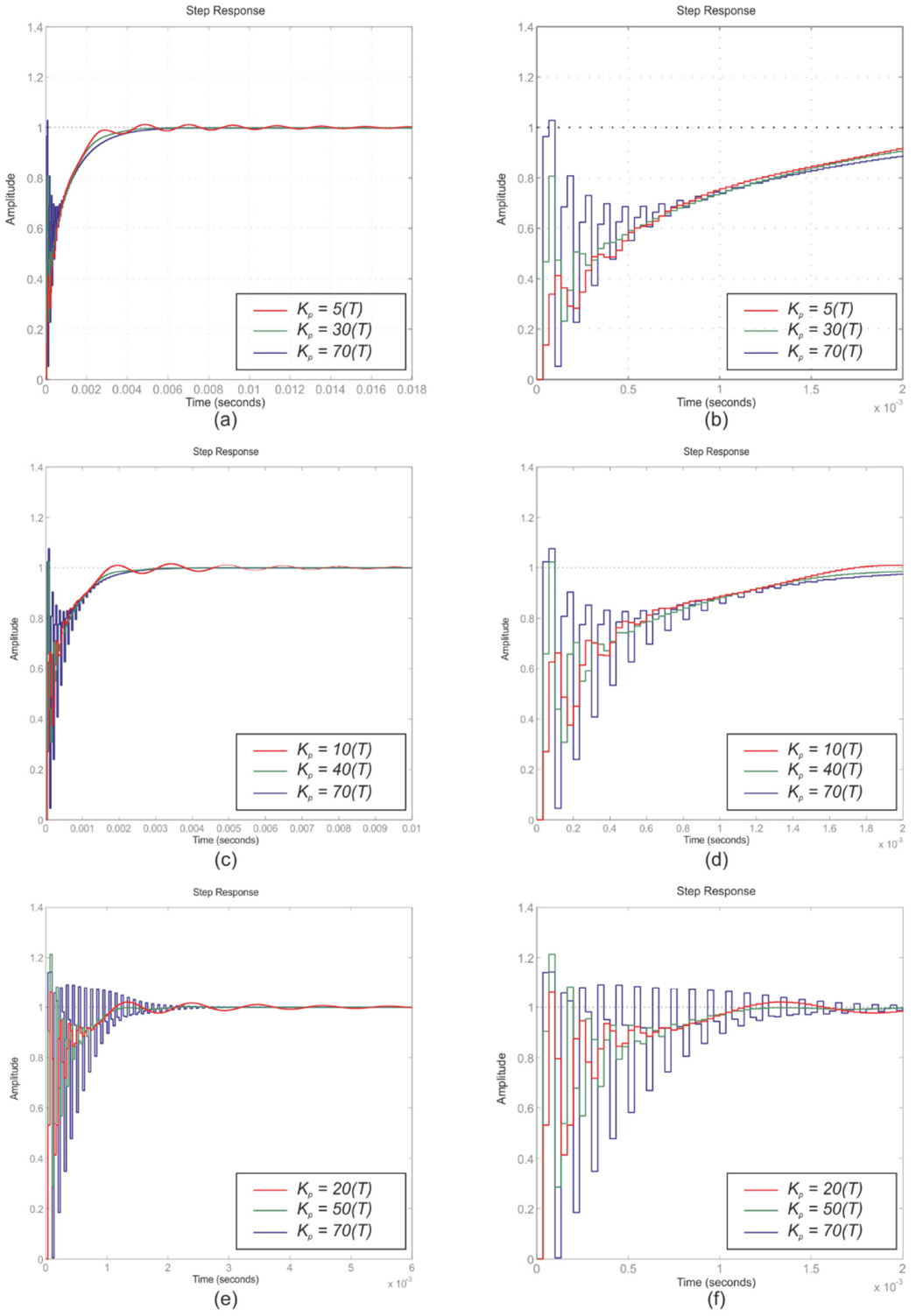

Figure 5.8. Transient-response of the closed-loop transfer function $G_{iairef}(z)$ to a 1 A step-increment in the reference-current. Small-signal non-synchronous model with immediate update mode. $t_{d\_proc} = (0.126)T = 4.12\ \mu s$. $D = 0.599$, $R_{load} = 5.2\ \Omega$, $V_{in} = 100$ V, $I_{in} = 120$ A. (a)&(b) $K_i = 5$, (c)&(d) $K_i = 10$, (e)&(f) K_i =20.

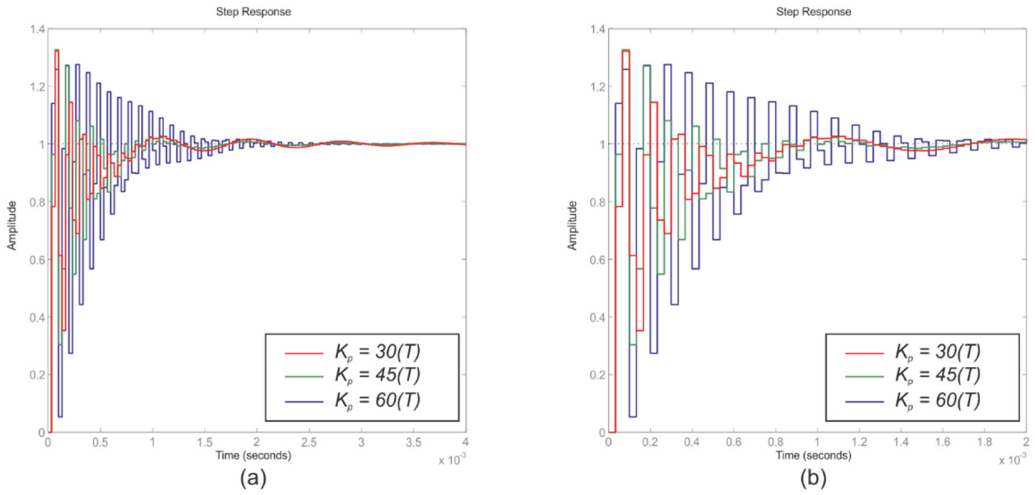

Figure 5.9. Transient-response of the closed-loop transfer function $G_{iairef}(z)$ to a 1 A step-increment in the reference-current. Small-signal non-synchronous model with immediate update mode. t_{d_proc} = (0.126)T = 4.2 µs. D = 0.599, R_{load} = 5.2 Ω, V_{in} = 100 V, I_{in} = 120 A. (a)&(b) K_i = 30.

From the results listed in Table 5.5, it is evident that the settling-time of the transient-response is reducing for higher values of K_i. However, the overshoot of the response is also increased. In addition, the reduction of the settling time is not very significant when K_i is ranged from *10* to *30*. From this analysis it is possible to conclude that the selection of the parameters of the PI compensator is a compromise between a fast settling-time and a low amplitude and frequency in the initial high-frequency oscillations. Therefore the final selection of K_p and K_i was *10(T)* and *10* respectively, which is highlighted in Table 5.5 and its associated transient response is seen in Figure 4.19(c).

Table 5.5. Performance of the step-response of the closed-loop transfer function $G_{iairef}(z)$. (Figure 5.8 and 5.9)

Figure	Point in Figure 5.7	K_i	K_p	Maximum over-shoot	Settling time
5.8(a) 5.8(b)	A1	5	5	1.2 %	3.9 ms
	A2		30	-	3.5 ms
	A3		70	2.8 %	4.1 ms
5.8(c) 5.8(d)	B1	10	10	1.5 %	2.7 ms
	B2		40	2.3 %	1.8 ms
	B3		70	7.5 %	2.1 ms
5.8(e) 5.8(f)	C1	20	20	6 %	1.9 ms
	C2		50	14.3 %	1.7 ms
	C3		70	21.3 %	1.0 ms
5.9(a) 5.9(b)	D1	30	30	32.2 %	1.0 ms
	D2		45	32.7 %	1.5 ms
	D3		60	27.5 %	1.7 ms

To further validate the step responses obtained with the small-signal model, the SABER switched model introduced in Chapter 3, Section 3.5, was used to plot the transient response of the system to a 5 % step- increment in the reference current. Figures 5.10(a) to 5.10(d) show a comparison of the sampled phase-a current, $i_a^*(t)$, obtained with the SABER switched model against that obtained with the small-signal non-synchronous model. Figure 5.10(a) shows the results obtained using the K_p and K_i combination corresponding to point A2 in Figure 5.7, Figure 5.10(b) corresponds to point B2, Figure 5.10(c) to point C2 and Figure 5.10(d) to point D3. The converter parameters used for these simulations are listed in Table 5.4 and the point of operation corresponds to the maximum output power conditions shown in Table 5.3. The schematic diagrams of the SABER switched model are given in Figures C.1 to C.3, Appendix C.

The results obtained showed no significant difference in the *5%* settling-times measured, the maximum error of the small-signal model with respect to the switched model was approximately *3.8%*, Figure 5.10(d). Also, the maximum over-shoot predicted by the switched model, stayed well within the ranges predicted by the small-signal model.

However, it is evident from Figures 5.10(c) and 5.10(d) that the small-signal model predicts a more lightly damped high frequency oscillation with higher values of $K_i \backslash K_p$ which are not predicted in the switched model results. This might be due to several factors that are included in the switched model but are not modelled in the small-signal one, such as non-linear switching characteristics of the devices in the converter, non-zero switching times of the transistors, and limited resolution of the ADC and DPWM modules which increase the overall damping effect of the system.

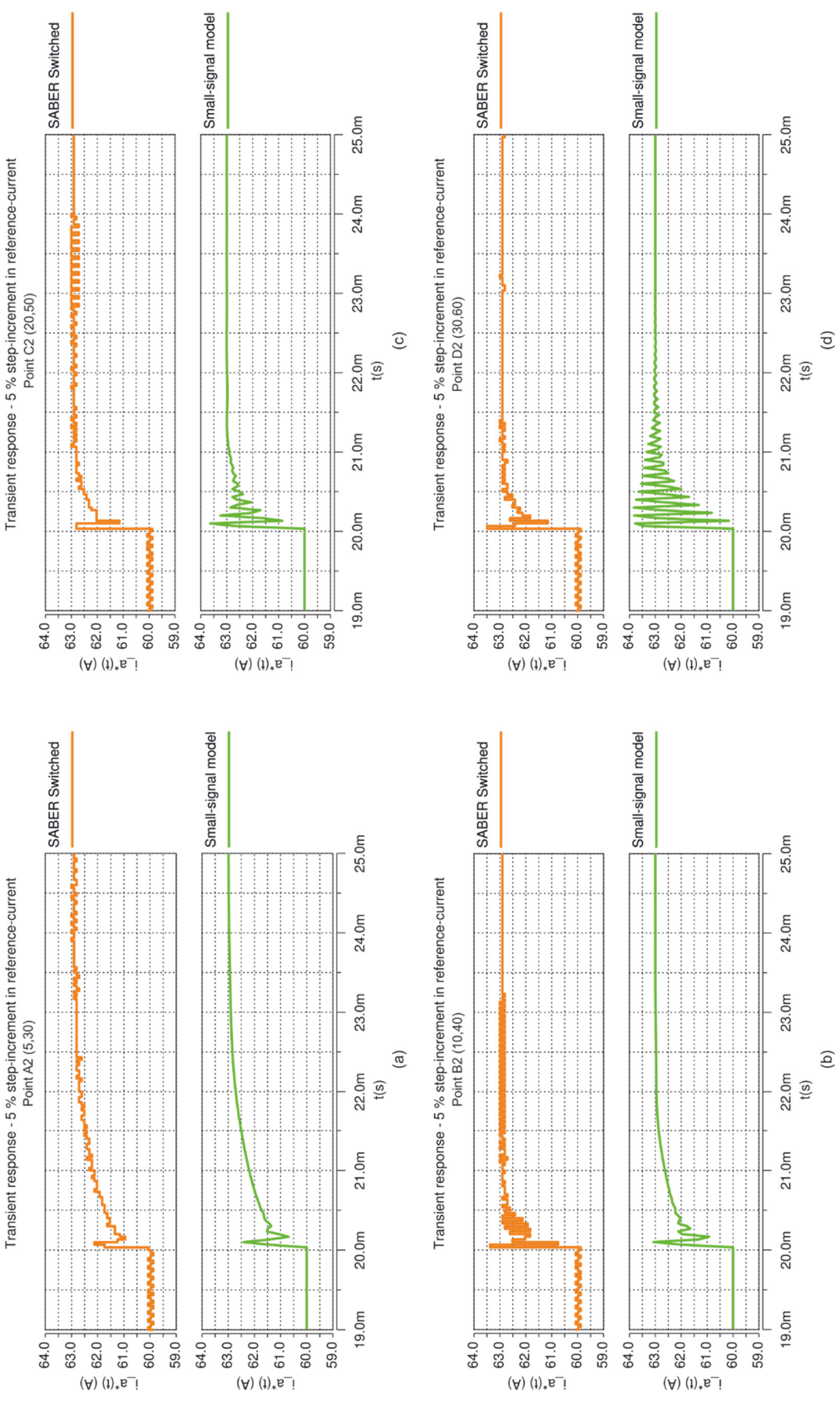

Figure 5.10. Comparison of the transient response of $i_a^*(t)$ to a 5 % step-increment in the reference-current obtained with the SABER switched model and the small-signal non-synchronous model of the converter. $t_{d\_proc} = (0.126)T = 4.2\ \mu s$, $D = 0.599$, $R_{load} = 5.2\ \Omega$, $V_{in} = 100\ V$, $I_{in} = 120\ A$, $I_{ref} = 60\ A$. (a) $K_p = 30T$, $K_i = 5$. (b) $K_p = 40T$, $K_i = 10$. (c) $K_p = 50T$, $K_i = 20$. (d) $K_p = 60T$, $K_i = 30$.

5.4. Performance evaluation of the designed PI compensator

5.4.1. Experimental evaluation to large step-increments

Figures 5.11(a), 5.11(b), 5.12(a) and 5.12(b) show the response of the converter phase current, $i_a(t)$, and the converter output voltage, $v_o(t)$, to a step-increment in the reference-current going from *30 A* to *60 A.* Each of these figures illustrate an overview of the transient response accompanied by a magnification of the event where several switching cycles are shown. The results shown were obtained using the SABER switched model and are compared against those obtained with the experimental prototype introduced in Chapter 3.

The reference-current values employed correspond to the extremes of operation of the design, Table 5.3, as they demand a minimum input current of *60 A* and a maximum input current of *120 A* respectively. The load resistance used was $R_{load} = 5.2\ \Omega$. The step-increment in the simulation was undertaken at *20 ms*, once the converter reached steady-state operation. In a similar way, the step-reference in the experimental tests was performed after the converter reached steady-state conditions. The converter parameters employed for the simulations are those listed in Table 5.4. Evidence of the experimental results shown is given in Appendix E, Figures E.9 and E.10.

The results of Figure 5.11(a) correspond to the case with the minimum input voltage, $V_{in} = 50\ V$ whilst those of Figure 5.12(a) depict the results obtained with the maximum input voltage, $V_{in} = 100\ V$. The values of the compensator gains used to obtain these results were $K_P = 10(T)$ and $K_i = 10$, as proposed in the previous section.

The results confirm the stability of the system over the operating region from *60 A* to *120 A*, Table 5.4. Moreover, the initial-transient oscillations are well controlled. The settling-time of the transient response is approximately *1.8 ms* for the minimum input voltage and *2.1 ms* for the maximum input voltage. Also a very good agreement between the simulation and the experimental results can be observed, further corroborating the validity of the SABER switched model. The noise shown in the experimental v_o trace that is consistent in all the results, is attributed to the use of a differential voltage probe which is susceptible to electro-magnetic interference.

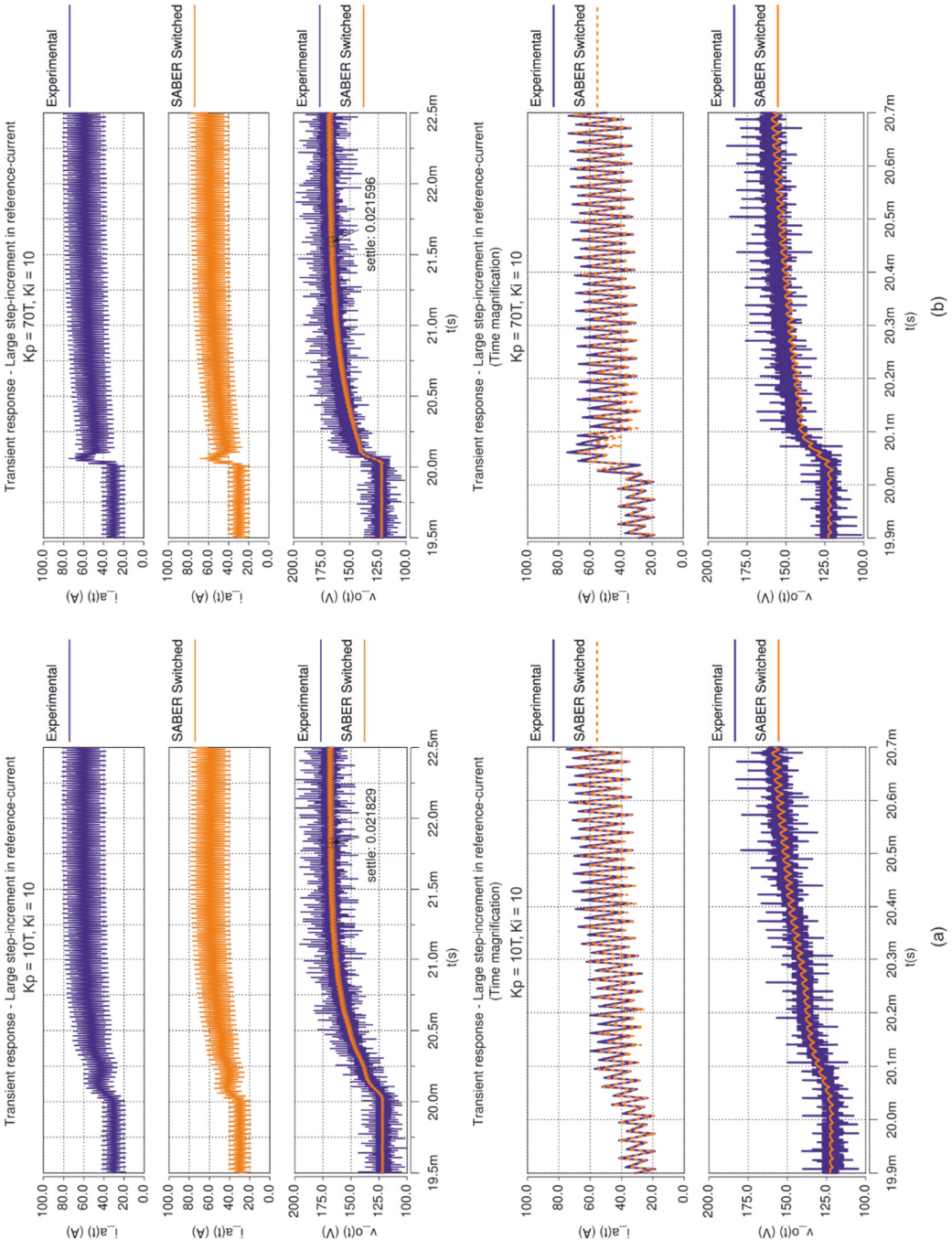

Figure 5.11. Transient response of the converter prototype and the SABER switched model to a large step-increment in the reference-current. V_{in} = 50 V, R_{load} = 5.2 Ω. Condition 1: I_{ref1} = 30 A; Condition 2: I_{re2} = 60 A. (a) K_p = 10(T) and K_i = 10; (b) K_p = 70(T) and K_i = 10.

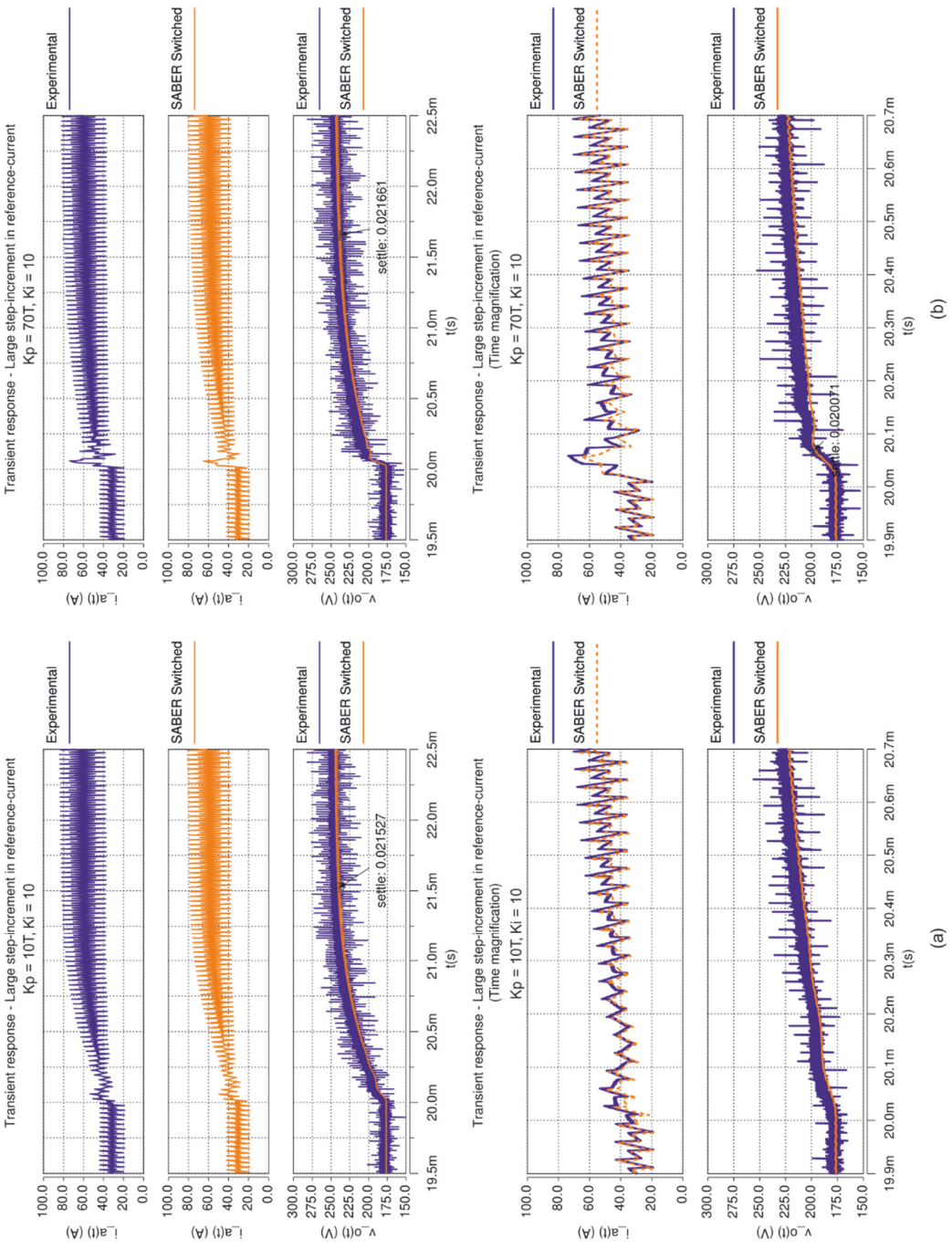

Figure 5.12. Transient response of the converter prototype and the SABER switched model to a large step-increment in the reference-current. V_{in} = 100 V, R_{load} = 5.2 Ω. Condition 1: I_{ref1} = 30 A; Condition 2: I_{re2} = 60 A. (a) K_p = 10(T) and K_i = 10; (b) K_p = 70(T) and K_i = 10.

To further corroborate the stability predicted by the small-signal non-synchronous model, the proportional gain was increased to *70(T)* where the converter is still expected to be stable. The results in Figure 5.11(b) and 5.12(b) with the new parameter of proportional gain are presented for $V_{in} = 50\ V$ and $V_{in} = 100\ V$ respectively and confirm the stability of the system. The settling time of the system at these points of operation was approximately *2.15 ms*.

5.4.2. Evaluation to small step-increments

Figures 5.13(a), 5.13(b), 5.14(a) and 5.14(b) show the transient response of the converter phase-current to a *5%* step-increment in the reference-current, which was obtained using the SABER switched model and the small-signal non-synchronous model. The switched model was used instead of the experimental prototype as the magnitude of the ripple in the prototype obscures the oscillations of the response, making it difficult to assess the validity of the small-signal model. The waveforms plotted in these figures are the phase-a current of the switched model, $i_a(t)$, and the sampled phase-a current of the switched model and of the small-signal model, $i_a^*(t)$. Once more, the parameters of the converter employed for the simulations are those listed in Table 5.4 and the load resistance used was *5.2 Ω*.

The points of operation evaluated correspond to the four extremes of operation of the design example shown in Table 5.3. Figure 5.13(a) and 5.13(b) show the response of the system for the cases with the minimum input current, $I_{in} = 60\ A$, and with minimum $V_{in} = 50\ V$ and maximum $V_{in} = 100\ V$ respectively. The results show a very good agreement between the switched model and the small-signal model. As expected some limit cycle oscillations are present along the switched model response. The settling-time measured is approximately *2.2 ms* with the exception of the response of the switched model in Figure 5.13(a), which is about *2.4 ms* which is caused by the LCOs. Finally, Figures 5.14(a) and 5.14(b) illustrate the responses for the case with maximum input current, $I_{in} = 120\ A$, and minimum and maximum input voltages respectively. These results also show an excellent agreement between the switched and the small-signal model results where the settling-

time measured was approximately *2.1 ms* in all the cases. The over-shoot measured in all the responses showed no significant difference.

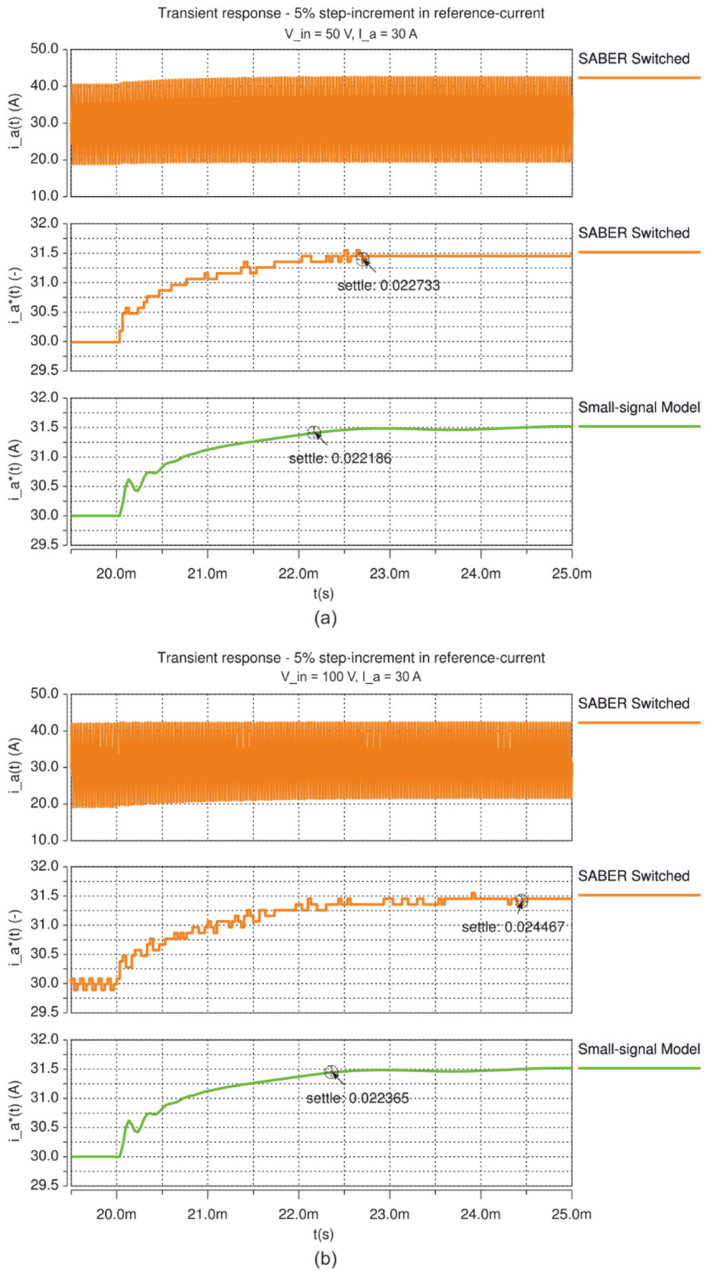

Figure 5.13. Transient response of the SABER switched model and the small-signal non-synchronous model to a 5% step-increment in the reference-current. $t_{d\_proc} = (1.2)T = 4.2\ \mu s$, $K_p = 10(T)$, $K_i = 10$, $R_{load} = 5.2\ \Omega$, $I_{ref1} = 30\ A$, $I_{re2} = 31.5\ A$. (a) $V_{in} = 50\ V$; (b) $V_{in} = 100V$.

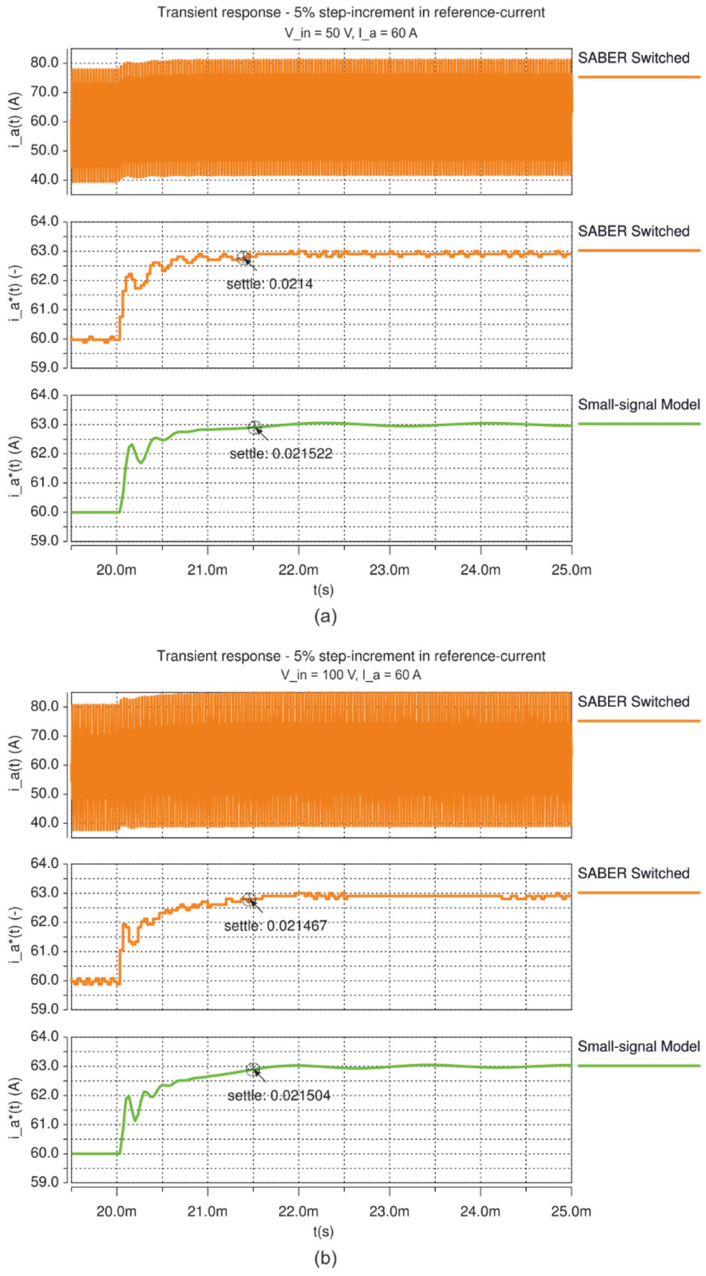

Figure 5.14. Transient response of the SABER switched model and the small-signal non-synchronous model to a 5% step-increment in the reference-current. $t_{d\_proc} = (1.2)T = 4.2\ \mu s$, $K_p = 10(T)$, $K_i = 10$, $R_{load} = 5.2\ \Omega$, $I_{ref1} = 60\ A$, $I_{re2} = 63\ A$. (a) $V_{in} = 50\ V$; (b) $V_{in} = 100V$.

5.5. Voltage control loop implementation and results

To verify the effectiveness of the digital average-current control loops in a voltage regulated system, an outer digital voltage control-loop was added to the SABER switched model. The voltage control-loop was included in the DSC unit and its block diagram can be found in Figure C.9, Appendix C.

The outer voltage control-loop compares the converter output voltage against a voltage-reference, the error between the two signals is passed through a PI compensator which calculates the current-reference for the inner average-current control loops. The parameters of the PI compensator employed for the inner current control loops used are those determined in the previous section: $K_p = 10(T)$ and $K_i = 10$. To select the parameters of the compensator for the voltage control-loop, a block diagram of the system was implemented in Simulink using the non-synchronous model developed in Chapter 4, Equation (4.14), which greatly simplifies the design. Using the Simulink control design tools, a digital PI backward-Euler compensator was automatically designed to regulate the voltage control-loop as to achieve the best transient performance and robustness of the system. For this example, the compensator was designed for the point of operation $V_{in} = 100\ V$, $V_o = 175\ V$, shown in Table 5.3.

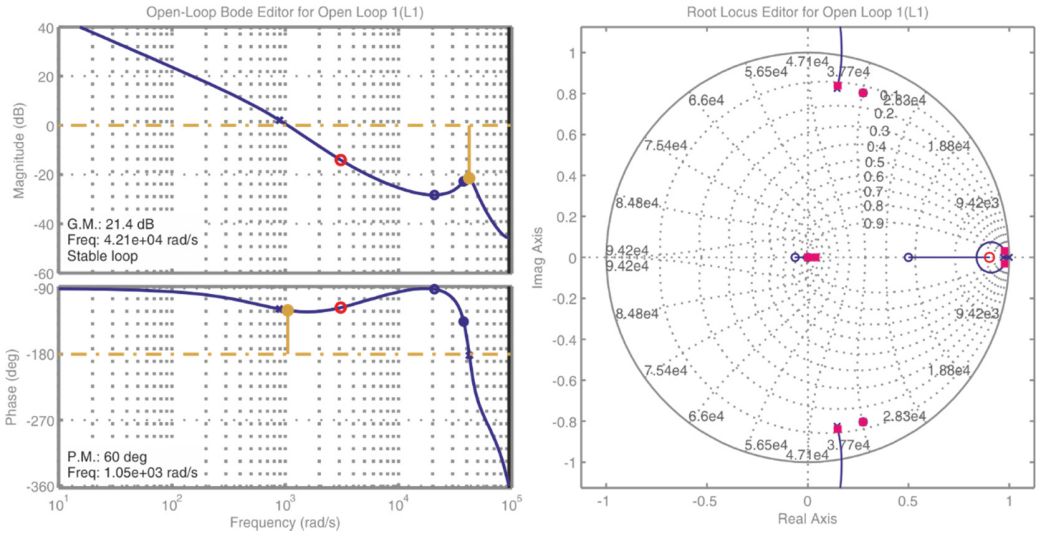

Figure 5.15. Bode plots and root-locus of the open, digital voltage control-loop using a PI compensator. Operating poing: $V_{in} = 100\ V$; $V_o = 175\ V$; $R_{load} = 5.2\ \Omega$; $t_{d\_proc} = (1.2)T = 4.2\ \mu s$.

Figure 5.15, shows the open-loop gain, phase and root-locus plots of the voltage control-loop that were used for the compensator design. It is possible to observe that the compensator has a real zero located at *0.902* in the z-plane, equivalent to a frequency of *493 Hz* or $3.1x10^3$ *rad/sec*. The expected transient performance of the output voltage to a unit step-change in the voltage-reference is illustrated in Figure 5.16, which main features are an over-shoot of *11.2 %* and a settling-time of *4.6 ms*.

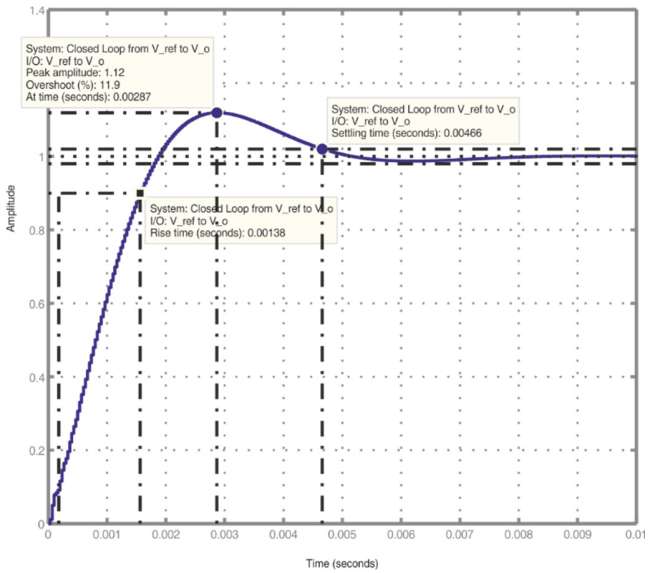

Figure 5.16. Transient response of the converter output voltage to a unit step-change in the voltage reference. Operating point: V_{in} = 100 V; V_o = 175 V; R_{load} = 5.2 Ω; t_{d_proc} = (1.2)T = 4.2 µs.

Figure 5.17 and 5.18 show the simulation results of the system with voltage regulation. The plots illustrated in these figures are as follows: in the first graph the converter output voltage, v_o, and the voltage reference, v_{ref}; in the second graph the sampled average value of the phase currents, i_a* and i_b*; and in the last graph the instantaneous phase currents, i_a and i_b.

Figure 5.17(a) shows the response of the system to a *10 %* step increase in the voltage reference at *20 ms*, which goes from *175 V* to *192.5 V*. The conditions of the system employed were using R_{load} = 5.2 Ω and V_{in} = 100 V. The overshoot and settle-time measured in the voltage waveform are *13 %* and *3.1 ms* approximately which correspond closely to those predicted by the model in Figure 5.21. The slight difference is attributed to the fact that a step increase is larger in the SABER simulation. Similarly, Figure 5.17(b) shows the

transient response of the system to a large step change in the voltage reference, going from *175 V* to *275 V*. The results show that the phase-currents have a complementary slow-frequency oscillation which amplitude decays slowly and that is due to the interaction of the converter phases.

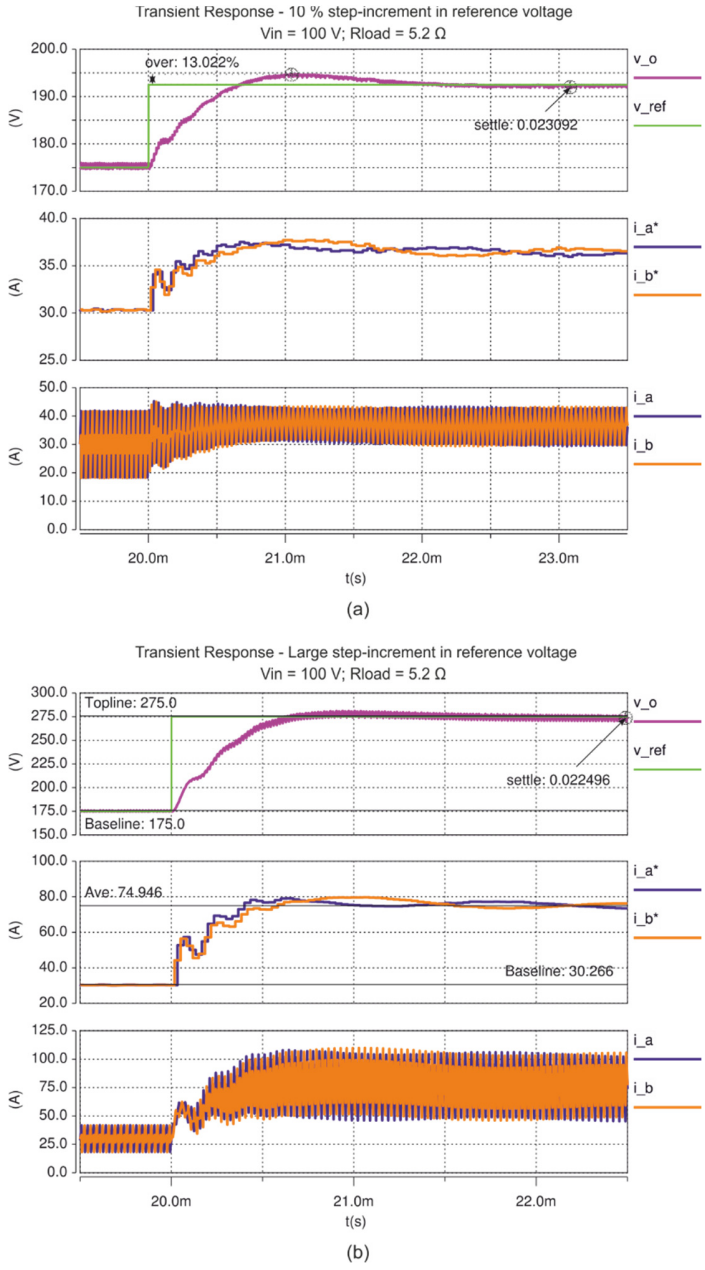

Figure 5.17. Transient response of the SABER switched model with voltage regulation to step-increments in the reference-voltage. $t_{d\_proc} = (1.2)T = 4.2\ \mu s$, $R_{load} = 5.2\ \Omega$, $V_{in} = 100\ V$. (a) $V_{ref1} = 175\ V$, $V_{ref2} = 192.5\ V$; (b) $V_{ref1} = 175\ V$, $V_{ref2} = 275\ V$.

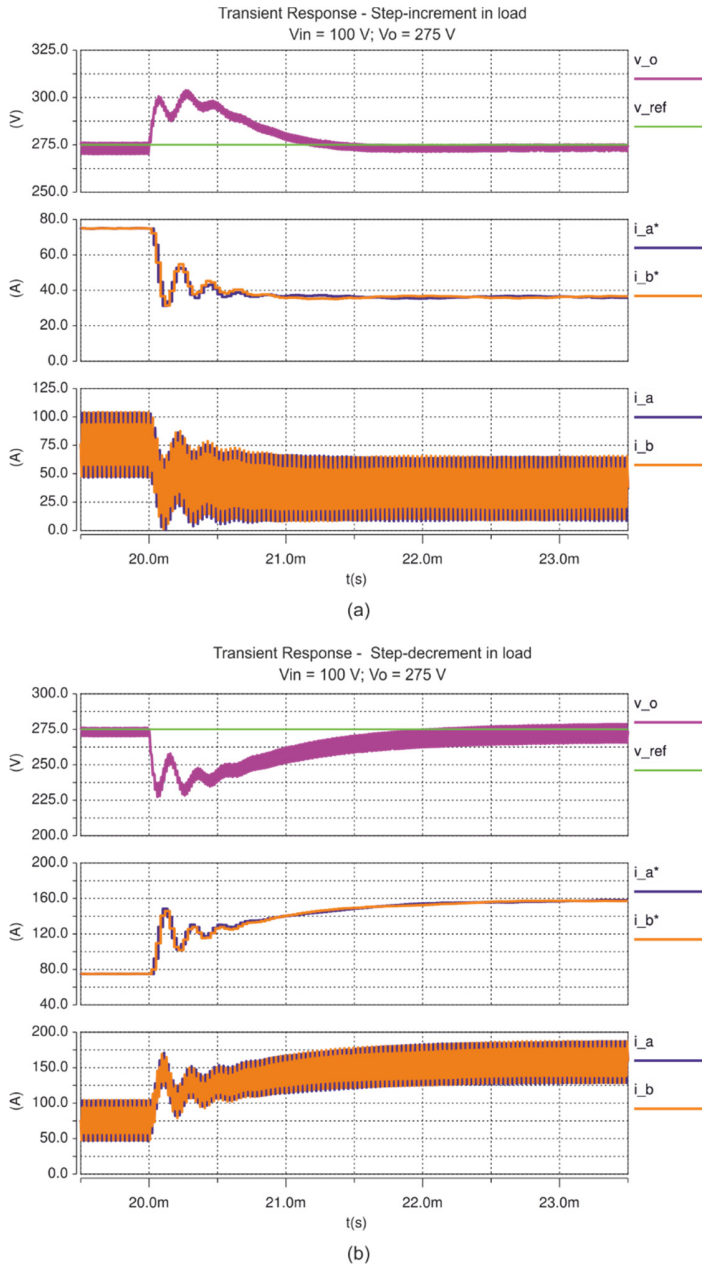

Figure 5.18. Transient response of the SABER switched model with voltage regulation to step-changes in the output load. t_{d_proc} = (1.2)T = 4.2 µs, V_{in} = 100 V, V_o = 275V. (a) R_{load} = 5.2 Ω, R_{load2} = 10.4 Ω; (b) R_{load} = 5.2 Ω, R_{load2} = 2.6 Ω.

Finally, Figures 5.18(a) and 5.18(b) show the transient performance of the system to step changes in the load resistor at *20 ms*, which go from *5.2 Ω* to *10.4 Ω* and from *5.2 Ω* to *2.6 Ω* respectively. The conditions used to obtain these results were V_{in} = *100 V* and V_{ref} = *275 V* which correspond to the maximum operating conditions for the design of the average-current control loops, see Table 5.3. The results confirm the capability of the

system to regulate the output voltage in several conditions. The system successfully regulates the step-load increase in approximately *2 ms* whilst the step-load decrease in approximately *3 ms*.

5.6. Summary

The sensitivity of the pole trajectories of the small-signal non-synchronous model to variations in the input voltage, output load, computational delay, proportional gain and integral gain was examined and discussed. The analysis revealed that the system is of order seven and contains a pair of high-frequency complex poles and a pair of low-frequency complex poles. The low-frequency complex poles are not present in the synchronous model of the converter and the study suggests that they are introduced by the PI compensator used to regulate the control loops. Moreover, the minimum K_p stability limit observed in the stability-range plots of Chapter 4, seems to be related to the location of the low-frequency complex poles whilst the maximum K_p stability limit is related to the location of the high-frequency complex poles.

Also, from this study, it was observed that variations in the output load and the input voltage seem to have no significant effect on the low-frequency complex poles, however the trajectories of the high-frequency poles are generally moved away from the centre of the unit circle as the load or the input voltage are increased. Finally, it was confirmed that the reduction of the computational delay has a favourable effect on the stability of the system as the trajectories of all the poles move towards the centre of the unit circle.

A design example to select the parameters of a PI compensator was carried out using the small-signal non-synchronous model developed in this thesis. The design aimed to guarantee the stable operation of the system over a defined range of operation and to ensure that the maximum response speed and the minimum overshoot to step-change transients were achieved. To this end, the stability-range plots of the system were used to select a number of proportional and integral gain combinations. The transient performance of the system was evaluated for each of the PI parameters selected, allowing a combination to be identified that meets the design requirements. The final design, $K_p = 10(T)$ and $K_i = 10$, was experimentally verified using *30 A* to *60 A* increments performed in the converter

prototype. The results confirmed the stability of the system over the intended range of operation and showed a maximum speed response of approximately *2.3 ms* with no over-shoot.

Finally, simulations results of the average-current controlled interleaved converter with voltage regulation were presented. To speed up the design process, the compensator of the outer voltage control-loop was designed using the non-interleaved model of the converter in combination with SIMULINK. The results demonstrated the capability of the system to regulate the converter output voltage in the presence of load disturbances and step-changes in the voltage reference. The maximum length of time that the system took to regulate the voltage was approximately *3 ms*.

Chapter 6
Conclusions and further research work

6.1. Introduction

This Chapter presents a summary of the achievements of the research work presented in this Thesis. The contributions to the field are highlighted and finally further research work opportunities are identified.

6.2. Summary of the thesis

6.2.1. Small-signal averaged modelling of the DIBC with IPT

A small-signal averaged model of the DIBC with IPT which accounts for the small ac perturbations of each control input independently was derived by replacing the switch networks of the converter with the averaged PWM switch model. By obtaining the transfer functions from the state-space representation of this model, transfer functions that describe the interaction between the control inputs and the converter phase-currents were identified.

Furthermore, the model was implemented in MATLAB and was thoroughly validated employing time-domain and frequency domain simulation results which were obtained from a switched and a large-signal averaged model developed in the SABER software. The results showed an excellent agreement at points of operation below *D = 0.7* and for duty-ratio disturbances of up to *5 %* where the error was found to be less than *4 %*. However, for very high duty-ratios, *D = 0.8* or more, which is a less common operating region, noticeable discrepancies occurred which were attributed to the assumptions of the

linearization analysis becoming inaccurate. Still, the error for duty-ratio disturbances up to *5 %* remained less than approximately *10 %* for the range $0.7 < D < 0.85$.

Finally, the frequency response of the transfer functions of the model showed virtually no difference compared to the simulation results, thereby further conforming their validity.

6.2.2. Analysis of the UPWM control techniques

The uniformly sampled PWM control of the DIBC with IPT was analysed for the leading-edge, trailing-edge and triangular carrier modulations by considering the steady-state waveforms of the converter. It was concluded that, similar to the single-phase boost converter, the leading-edge modulation and the trailing-edge modulation allowed the valley phase current and the peak phase current to be controlled respectively. Also, it was demonstrated analytically that by the use of the triangular carrier modulation, it is possible to control the average value of the converter phase currents.

6.2.3. Implementation of the control strategies and experimental validation

The valley-current, peak-current and average-current control strategies were implemented on a Texas Instruments DSC TMS320F28335 and verified experimentally employing a *25 kW, 30 kHz* prototype of the dual-interleaved converter with IPT.

Also, by examining the operation of the DPWM inbuilt in the DSC, an enhancement to the average-current control methodology was proposed which reduces the delay caused by the cycle-by-cycle update of the DPWM thereby allowing the bandwidth of the control loop to be extended. However, in order to avoid the generation of spurious waveforms using this strategy, the minimum duty-ratio has to be limited according to the computation time of the control algorithm, making the technique unsuitable for converters with high switching frequencies or with a high number of phases.

The steady-state and the dynamic operation of all the control techniques was evaluated by examining the transient response of the phase-currents to large step-reference changes and to step-load changes. The results revealed steady-state error in the phase-currents caused by the mismatched sampling instants which was attributed to the

propagation delay of the gate-drivers and the turn-on and turn-off delay of the converter transistors. Moreover, it was also revealed that the valley-current control and the peak-current control with UPWM are not suitable for this type of converter as the non-linear behaviour of the phase ripple-current causes an uncontrollable region around $D = 0.5$. It was observed that the size of the uncontrollable region was strongly dependent on the load resistor, being less significant for resistive loads below $R_{load} = 5\ \Omega$. In contrast, the average-current control methodologies showed no evidence of uncontrollable regions.

The system performance under large step-reference changes and to step-load changes further verified the correct regulation of the target control-current for all the control methodologies and the capability of the control loops to balance the phase-currents. It was found that even during transient events the phase currents were correctly balanced. The maximum current imbalance measured was found to be approximately *2 A* which was observed as a dc-offset of *1 A* in the differential current, the maximum peak phase-current being *70 A*.

6.2.4. Modelling of phase interactions in dual-interleaved converters

Using the sampler decomposition methodology, the small-signal, closed-loop transfer functions of the dual interleaved boost converter with IPT were determined for two cases: when the interleaved interaction of the converter phases is disregarded, synchronous model, and when the interleaved interaction is taken into account, non-synchronous model.

A comparison between the closed-loop transfer functions from the two models and the simulation results from a switched and a large-signal averaged model implemented in the SABER simulator was undertaken using time domain step responses and frequency domain responses. Identical PI controllers were used to regulate the phase currents. It was found that the transient response of the models to *5 %* disturbances, showed an excellent agreement with the SABER simulations and that the mathematical models showed no significant difference. In the frequency domain, both models showed a good agreement with the simulation results presenting a deviation of no more than approximately *1 dBA* in the magnitude response over most of the operating range, but increasing at low power.

Also, no more than *10 degrees* in the phase response for frequencies up to approximately *8 kHz*. However, for frequencies above *8 kHz* the transfer-functions of the non-synchronous model showed differences in the phase response, which are likely to be caused by the time-advance and time-delay units employed to model the interleaved interaction of the control-loops.

The stability range of the synchronous and non-synchronous models was determined by examining the location of the poles of the closed-loop transfer functions for several combinations of proportional and integral gains. The comparison confirmed that the interleaved operation of the converter phases has a detrimental effect on the stability of the system and that the synchronous model fails to predict this behaviour. The stability range predicted by the non-synchronous model was further validated by simulation and experimental results.

6.2.5. Stability analysis of the DIBC with IPT for digital average-current control via root-locus

The objective of this analysis was to study the impact that changes on the input voltage, load resistance, computational delay and the gains of a PI compensator have on the stability of the closed-loop transfer functions of the non-synchronous model.

It was found that with PI compensators two pairs of complex poles were present in the z-plane. A low frequency pair near to the *+1* point and a higher frequency pair. The low frequency complex poles were not present in the synchronous model of the converter and their location seemed to be related to the instability caused by the interleaved operation of the converter phases.

Also the results showed that increasing either the input voltage or the load, moves the system poles away from the centre of the unit circle reducing system stability. Conversely, it was found that reducing the processing time of the control algorithms has a favourable effect on stability as the closed-loop poles move towards the centre of the unit circle.

6.2.6. Design of a PI compensator for the current control loops

Aided by the stability-range plots generated using the closed-loop transfer functions of the non-synchronous model, the parameters of a PI compensator were selected. The design was made to ensure maximum response speed and minimum overshoot to step-change transients, and it was achieved by evaluating the step-response of the transfer-functions for a range of combinations of proportional and integral gains. The final design, K_p *=10(T)* and K_i *=10,* was validated using simulation and experimental results of the system to large-step transients which confirmed the stability for the intended operation region and showed a maximum settling time of *2.2 ms* with no over-shoot. The simulation and experimental results showed an excellent agreement.

6.3. Contributions of this research work

6.3.1. Small-signal averaged model of the dual interleaved boost converter with inter-phase transformer

By using the average PWM switch model, the modelling procedure of the converter accounting for small ac perturbations in the control inputs is fully described and the analytical expressions of the control-to-phase current, control-to-opposite phase current, control-to-output voltage, disturbance current-to-phase current and disturbance current-to-output voltage transfer functions are presented. Compared to similar models reported in the literature, [1-4], the model reported in this thesis has been developed for average-current control of a boost converter, it accounts for the inter-phase transformer, and has been thoroughly validated for a wide range of operation.

6.3.2. Comprehensive study of the uniformly sampled, valley-current, peak-current and average-current control for the DIBC with IPT.

The use of digital uniformly-sampled control techniques has been widely reported for interleaved dc-dc converters in low power applications, such as voltage regulation modules for microprocessors and communication systems, and in particular, digital average-current control is commonly employed in power factor correction systems. However, the use of digital uniformly-sampled control techniques is relatively new to the

field of high-power interleaved dc-dc converters and the study carried in this thesis has identified the most suitable form of this type of control for the dual interleaved boost converter.

6.3.3. Immediately updated DPWM operation for average-current control

By updating the DPWM registers immediately after the calculation of the new duty-ratio, it is possible to reduce the computational delay of the digital control-loops and therefore extend their bandwidth, increasing the response speed of the converter. Due to its simplicity, this technique is a straightforward alternative to improve the digital controller bandwidth in converters with a small number of phases and/or with a modest switching frequency since the minimum duty-ratio has to be limited to avoid the generation of spurious PWM waveforms. Despite being relatively simple to implement, this technique has not been reported in the literature to the best of the author's knowledge.

6.3.4. Modelling phase interactions in dual interleaved converters.

By means of the sampler decomposition technique, a methodology to account for the interleaved operation and the interaction of the phases in interleaved converters has been developed and validated. This methodology was employed in conjunction with an averaged small-signal model of the converter to derive the small-signal, closed-loop, control-to-output transfer functions of the dual interleaved boost converter with IPT, and it has been demonstrated that the interleaved interaction produces instability issues which cannot be predicted with a model that assumes the synchronized operation of the converter phases. To the best of the author's knowledge, the use of this methodology has not been reported in the field of dc-dc converters, and the effects of interleaved sampling in dc-dc converters have not been previously been analysed or understood.

6.3.5. Stability study of the converter

The stability of the converter has been analysed via root-loci and conclusions have been drawn on how parametric changes in the input voltage, load resistance, computational delay and proportional and integral gains of the compensator affect the stability of the converter. An analysis of this nature has not been found in the literature

and is an important contribution to the field as it provides a better understanding of the dynamics of interleaved converters and provides a sound basis for control loop design.

6.4. Further research opportunities

6.4.1. Simplification of the small-signal averaged state-space model of the converter

The state-space representation of the small-signal model of the converter developed in Chapter 2 contains a state-space matrix, $\mathbf{A_{av}}$, defined by three state variables: $\tilde{i}_a$, $\tilde{i}_b$ and $\tilde{v}_o$. However, the rank of $\mathbf{A_{av}}$ is two, which implies that at least two of the state variables are linearly dependent, therefore, it might be possible to eliminate one of these variables and further reduce the order of the system. Further research work could be carried out to verify this hypothesis which is of special interest as it might lead to a reduction of the order of the closed-loop transfer functions.

6.4.2. Generalization of the sampler decomposition technique for *n*-interleaved converters

The sampler decomposition method, introduced in Chapter 4, may be extended to model *n*-phase interleaved converters in order to obtain a generalized analytical closed-loop transfer function. This is of interest as it will provide further understanding of how the stability of the system is affected as the number of phases of the converter is increased. Also, this modelling methodology might be applied to other dc-dc converter topologies, such as the buck and the buck-boost converter.

6.4.3. Application of the sampler decomposition technique to model the dynamics of peak-current mode control

The sampler decomposition technique might be also employed in conjunction with the peak current control model proposed by Ridley to examine the instabilities caused by the interleaved operation of the converter phases. In contrast with data-sampled modelling methods, which have been already carried out for a DIBC, this methodology might lead to a simpler solution where analytical expressions can be determined. This is of special interest as peak-current control is widely employed in interleaved dc-dc converters due to its fast dynamic performance and inherent over-current protection.

6.4.4. Development of non-linear control methodologies

A further review of the literature identified a few publications on control systems with dual symmetrical control-loops such as those of the dual interleaved boost converter with digital average-current control considered in this thesis. These systems are termed multivariable symmetrical systems, [5-7], and formal non-linear control methodologies have been proposed to analyse their stability. However, the research work has been carried out using analogue controllers only and they do not account for the interleaved operation of the control loops. An opportunity for interdisciplinary research therefore arises, where non-linear control can be used in conjunction with the new closed-loop non-synchronous model of the converter proposed in this thesis to further analyse the system.

6.4.5. Digital implementation of bidirectional control for the dual interleaved converter

Operating the top transistors of the h-bridge that integrates the dual interleaved converter prototype allows the operation of the system in step-down mode and allows the current to flow in the opposite direction as when the bottom transistors are operated only. Developing a digital control strategy that allows the converter to be operated in both step-up and step-down modes is an interesting possibility with a wide range of applications.

6.4.6. Modelling and control of the dual interleaved converter for bidirectional operation

A similar modelling procedure as the one shown in this thesis might be employed to obtain a closed-loop model of the converter when it operates in step-down mode. It would then be possible to have a complete bidirectional model of the converter which can be employed to design a digital controller for bidirectional operation.

6.4.7. Symmetrical (double) sampling on immediate update control algorithm

When the triangular carrier modulation is used, it may be possible to acquire two samples of the average value of the phase-current per switching cycle by triggering a sampling sequence at both the minimum and the maximum values of the DPWM counters. This is of interest as it will allow to improve the control-loop bandwidth in a simple manner.

6.4.8. Implementation of digital control for converter with wide band gap devices

Further work could consider applying the digital control techniques developed in a converter that employs Silicon Carbide devices or other type of wide band gap devices. This is of interest as this devices are capable of higher switching speeds than common Silicon devices, which in consequence will allow to increase the switching frequency of the converter.

6.4.9. Implementation of other current-regulation methodologies

Other current-regulation methods such as predictive control techniques or dead-beat control may be implemented and designed using the model of the converter developed in this Thesis. This opens an opportunity of research as the use of predictive techniques has not been fully investigated for interleaved converters.

6.4.10. Implementation of alternative methods for balancing the IPT current

As mentioned in the literature review, the use of digital control opens the possibility to implement other type of current-regulation methodologies to ensure an adequate balancing of the phase-current in the IPT without the need of measuring the phase-currents. Some of these methods, such as the digital reconstruction of the phase currents employing a single dc-link current transducer, are of interest when the number of phases of the converter is large.

6.5. Conclusion

In this Thesis, the examination of digital uniformly-sampled current control techniques for a dual-interleaved boost converter has been undertaken using the converter steady-state waveforms and experimental results from a *25 kW*, *30 kHz* prototype. The results revealed that average-current control is the most suitable control technique for this type of converter. On this basis, a small-signal averaged model of the converter has been developed in conjunction with the sampler decomposition technique to account for the interleaved interaction and operation of the converter phases. The resulting closed-loop model demonstrated that the interaction of the converter phases has a detrimental effect

on the stability of the converter which cannot be predicted when the interleaved interaction of the phases is neglected. Further work is necessary to determine analytical expressions of the closed-loop, control-to-phase current transfer-functions for the converter, and to extend the proposed modelling methodology for *n*-interleaved dc-dc converters.

6.6. References

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Appendix A
Derivation of mathematical expressions

A.1. Derivation of equations for steady-state ripples

The following sections show the mathematical procedure used to obtain the equations found in Table 2.1, Chapter 2.

A.1.1. Input inductor current ripple for D < 0.5

The input inductor current ripple, ΔI_{Lin}, may be obtained for $D < 0.5$ from Figure 2.2(a) by integrating the positive volt-seconds applied to the input inductor:

$$\Delta I_{in} = \frac{1}{L_{in}} \int_0^{DT} v_{Lin}(t)\,dt = \frac{1}{L_{in}} \left(V_{in} - \frac{V_o}{2} \right) DT$$

The equation above can be expressed in terms of V_{in} employing the converter conversion ratio shown in Equation (2.1), $V_o = \frac{V_{in}}{(1-D)}$:

$$\Delta I_{in} = \frac{V_{in} DT}{2L_{in}} \left(\frac{1-2D}{1-D} \right) \tag{A.1}$$

A.1.2. Input inductor current ripple for D < 0.5

The input inductor current ripple may be obtained for $D > 0.5$ from Figure 2.2(c) by integrating the negative volt-seconds applied to the input inductor:

$$\Delta I_{in} = \frac{1}{L_{in}} \int_0^{(1-D)T} v_{Lin}(t)\,dt = \frac{1}{L_{in}} \left(\frac{V_o}{2} - V_{in} \right) (1-D)T$$

The equation above can be expressed in terms of V_{in} employing the converter conversion ratio shown in Equation (2.1), $V_o = \frac{V_{in}}{(1-D)}$:

$$\Delta I_{in} = \frac{V_{in}T}{2L_{in}}(2D-1) \tag{A.2}$$

A.1.3. Differential current ripple for D < 0.5

The differential current ripple, ΔI_{diff}, may be obtained for $D < 0.5$ from Figure 2.2(a) by integrating the positive volt-seconds between the terminals of the IPT, in other words:

$$\Delta I_{diff} = \frac{1}{L_{diff}} \int_0^{DT} v_{diff}(t)dt = \frac{1}{L_{diff}}(V_o)DT$$

The equation above can be expressed in terms of V_{in} employing the converter conversion ratio shown in Equation (2.1), $V_o = \frac{V_{in}}{(1-D)}$:

$$\Delta I_{diff} = \frac{V_{in}DT}{L_{diff}}\left(\frac{1}{1-D}\right) \tag{A.3}$$

A.1.4. Differential current ripple for D > 0.5

The differential current ripple may be obtained for $D > 0.5$ from Figure 2.2(c) by integrating the positive volt-seconds between the terminals of the IPT, in other words:

$$\Delta I_{diff} = \frac{1}{L_{diff}} \int_0^{(1-D)T} v_{diff}(t)dt = \frac{1}{L_{diff}}(V_o)(1-D)T$$

The equation above can be expressed in terms of V_{in} employing the converter conversion ratio shown in Equation (2.1), $V_o = \frac{V_{in}}{(1-D)}$:

$$\Delta I_{diff} = \frac{V_{in}T}{L_{diff}} \tag{A.4}$$

A.1.5. Large and small phase-current ripples

The large phase-current ripple can be expressed as the sum of two ripple magnitudes: the input inductor current ripple and the differential current ripple. Under the assumption that the input inductor current divides equally between the converter phases and that the IPT windings inductance is identical, the input inductor current ripple will be also equally divided between the phases, hence, the large phase-current ripple may be expressed as:

$$\Delta I_{lrg} = \frac{1}{2}\Delta I_{in} + \Delta I_{diff} \tag{A.5}$$

The small phase-current ripple may also be deduced similarly, and can be expressed as the difference between the input inductor current ripple and the differential current ripple:

$$\Delta I_{smll} = \frac{1}{2}\Delta I_{in} - \Delta I_{diff} \tag{A.6}$$

A.1.6. Large and small phase-current ripple for D < 0.5

Substituting Equations (A.1) and (A.3) in Equations (A.5), the large phase-current ripple for D < 0.5 can be obtained:

$$\Delta I_{lrg} = \frac{1}{2}\frac{V_{in}DT}{2L_{in}}\left(\frac{1-2D}{1-D}\right) + \frac{V_{in}DT}{L_{diff}}\left(\frac{1}{1-D}\right) = \frac{V_{in}DT}{(1-D)}\left(\frac{1-2D}{4L_{in}} + \frac{1}{L_{diff}}\right) \tag{A.7}$$

In a similar way, the small phase current ripple may be obtained by substituting Equations (A.1) and (A.3) in Equation (A.6):

$$\Delta I_{lrg} = \frac{1}{2}\frac{V_{in}DT}{2L_{in}}\left(\frac{1-2D}{1-D}\right) - \frac{V_{in}DT}{L_{diff}}\left(\frac{1}{1-D}\right) = \frac{V_{in}DT}{(1-D)}\left(\frac{1-2D}{4L_{in}} - \frac{1}{L_{diff}}\right) \tag{A.8}$$

A.1.7. Large and small phase-current ripple for D > 0.5

Substituting Equations (A.2) and (A.4) in Equations (A.5), the large phase-current ripple for *D > 0.5* can be obtained:

$$\Delta I_{lrg} = \frac{1}{2}\frac{V_{in}T}{2L_{in}}\left(2D-1\right)+\frac{V_{in}T}{L_{diff}} = V_{in}T\left(\frac{2D-1}{4L_{in}}+\frac{1}{L_{diff}}\right) \tag{A.9}$$

In a similar way, the small phase current ripple may be obtained by substituting Equations (A.2) and (A.4) in Equation (A.6):

$$\Delta I_{lrg} = \frac{1}{2}\frac{V_{in}T}{2L_{in}}\left(2D-1\right)-\frac{V_{in}T}{L_{diff}} = V_{in}T\left(\frac{2D-1}{4L_{in}}-\frac{1}{L_{diff}}\right) \tag{A.10}$$

A.2. Derivation of the closed-loop transfer functions $G_{iairef}(z)$ and $G_{ibiref}(z)$ with no interleaving

In the following paragraphs, the closed-loop transfer functions $G_{iairef}(z)$ and $G_{ibiref}(z)$ will be derived from Figure 4.4(b), Chapter 4, for the case where the samplers S_a and S_b operate synchronously and the DPWM module is updated immediately after the processing of the sampled current. From inspection of the block diagram of Figure 4.4(b), Chapter 4, the following relations can be written by ignoring the time advance and time delay units of the sampler S_b:

$$\tilde{d}_a(z) = C(z)\mathcal{Z}\left[\tilde{i}_{ref}(s)\right] - C(z)\tilde{d}_a(z)\mathcal{Z}\left[G_M(s)G_{di}(s)H_a(s)\right] - C(z)\tilde{d}_b(z)\mathcal{Z}\left[G_M(s)G_{dxi}(s)H_a(s)\right] \quad \text{(A.11a)}$$

$$\tilde{d}_b(z) = C(z)\mathcal{Z}\left[\tilde{i}_{ref}(z)\right] - C(z)\tilde{d}_b(z)\mathcal{Z}\left[G_M(s)G_{di}(s)H_b(s)\right] - C(z)\tilde{d}_a(z)\mathcal{Z}\left[G_M(s)G_{dxi}(s)H_b(s)\right] \quad \text{(A.11b)}$$

$$\tilde{i}_a(z) = \tilde{d}_a(z)\mathcal{Z}\left[G_M(s)G_{di}(s)\right] + \tilde{d}_b(z)\mathcal{Z}\left[G_M(s)G_{dxi}(s)\right] \quad \text{(A.11c)}$$

$$\tilde{i}_b(z) = \tilde{d}_b(z)\mathcal{Z}\left[G_M(s)G_{di}(s)\right] + \tilde{d}_a(z)\mathcal{Z}\left[G_M(s)G_{dxi}(s)\right] \quad \text{(A.11d)}$$

The constituent z-transforms found in Equations (A.11a) to (A.11d) are listed in Table A.1 and are redefined in a compact notation for this particular case-study where t_{d_proc} <

Table A.1. Constituent transfer functions of the digital average-current controlled DIBC with IPT in the z-domain assuming the synchronous operation of the samplers S_a and S_b.

Z-transform identified	Modified z-transform	Compact notation
$\mathcal{Z}\{G_M(s)G_{di}(s)H_A(s)\}$	$\mathcal{Z}\{G_{h0}(s)\Delta PWM(s)G_{di}(s)H_A(s)\} = = G_{di}H_A(z,1-t_{d\_proc})$	$G_{di}H_A(z)$
$\mathcal{Z}\{G_M(s)G_{di}(s)H_B(s)\}$	$\mathcal{Z}\{G_{h0}(s)\Delta PWM(s)G_{di}(s)H_B(s)\} = G_{di}H_B(z,1-t_{d\_proc})$	$G_{di}H_B(z)$
$\mathcal{Z}\{G_M(s)G_{dxi}(s)H_A(s)\}$	$\mathcal{Z}\{G_{h0}(s)\Delta PWM(s)G_{dxi}(s)H_A(s)\} = = G_{dxi}H_A(z,1-t_{d\_proc})$	$G_{dxi}H_A(z)$
$\mathcal{Z}\{G_M(s)G_{dxi}(s)H_B(s)\}$	$\mathcal{Z}\{G_{h0}(s)\Delta PWM(s)G_{dxi}(s)H_B(s)\} = = zG_{dxi}H_B(z,1-t_{d\_proc})$	$G_{dxi}H_B(z)$
$\mathcal{Z}\{G_M(s)G_{di}(s)\}$	$\mathcal{Z}\{G_{h0}(s)\Delta PWM(s)G_{di}(s)\} = = G_{di}(z,1-t_{d\_proc})$	$G_{di}(z)$
$\mathcal{Z}\{G_M(s)G_{dxi}(s)\}$	$\mathcal{Z}\{G_{h0}(s)\Delta PWM(s)G_{dxi}(s)\} = = G_{dxi}(z,1-t_{d\_proc})$	$G_{dxi}(z)$

T/2, in other words, $\Delta PWM(s) = e^{-s(td\_\mathrm{proc})}$. Upon substitution of the compact notation of the constituent z-transforms into Equations (A.11a) to (A.11d), Equations (A.12a) to (A.12d) are found:

$$\tilde{d}_a(\mathrm{z}) = C(\mathrm{z})\tilde{i}_{ref}(\mathrm{z}) - C(\mathrm{z})\tilde{d}_a(\mathrm{z})\mathrm{G}_{di}\mathrm{H}_a(\mathrm{z}) - C(\mathrm{z})\tilde{d}_b(\mathrm{z})\mathrm{G}_{dxi}\mathrm{H}_a(\mathrm{z}) \tag{A.12a}$$

$$\tilde{d}_b(\mathrm{z}) = C(\mathrm{z})\tilde{i}_{ref}(\mathrm{z}) - C(\mathrm{z})\tilde{d}_b(\mathrm{z})\mathrm{G}_{di}\mathrm{H}_b(\mathrm{z}) - C(\mathrm{z})\tilde{d}_a(\mathrm{z})\mathrm{G}_{dxi}\mathrm{H}_b(\mathrm{z}) \tag{A.12b}$$

$$\tilde{i}_a(\mathrm{z}) = \tilde{d}_a(\mathrm{z})\mathrm{G}_{di}(\mathrm{z}) + \tilde{d}_b(\mathrm{z})\mathrm{G}_{dxi\phi}(\mathrm{z}) \tag{A.12c}$$

$$\tilde{i}_b(\mathrm{z}) = \tilde{d}_b(\mathrm{z})\mathrm{G}_{di}(\mathrm{z}) + \tilde{d}_a(\mathrm{z})\mathrm{G}_{dxi}(\mathrm{z}) \tag{A.12d}$$

Solving Equation (A.12a) for $\tilde{d}_b(\mathrm{z})$ and substituting it into Equation (A.12b) yields:

$$\tilde{d}_a(\mathrm{z}) = \mathrm{C}(\mathrm{z})\tilde{i}_{ref}(\mathrm{z})\left\{\frac{1 + C(\mathrm{z})\left[\mathrm{G}_{di}H_b(\mathrm{z}) - G_{dxi}H_a(\mathrm{z})\right]}{\left[C(\mathrm{z})\mathrm{G}_{di}H_a(\mathrm{z}) + 1\right]\left[C(\mathrm{z})\mathrm{G}_{di}H_b(\mathrm{z}) + 1\right] - C^2(\mathrm{z})\mathrm{G}_{dxi}H_a(\mathrm{z})\mathrm{G}_{dxi}H_b(\mathrm{z})}\right\} \tag{A.13a}$$

In a similar way, by solving Equation (A.12b) for $\tilde{d}_a(\mathrm{z})$ and substituting it into Equation (A.12a), $\tilde{d}_b(\mathrm{z})$ is obtained:

$$\tilde{d}_b(\mathrm{z}) = \mathrm{C}(\mathrm{z})\tilde{i}_{ref}(\mathrm{z})\left\{\frac{1 + C(\mathrm{z})\left[\mathrm{G}_{di}H_a(\mathrm{z}) - G_{dxi}H_b(\mathrm{z})\right]}{\left[C(\mathrm{z})\mathrm{G}_{di}H_a(\mathrm{z}) + 1\right]\left[C(\mathrm{z})\mathrm{G}_{di}H_b(\mathrm{z}) + 1\right] - C^2(\mathrm{z})\mathrm{G}_{dxi}H_a(\mathrm{z})\mathrm{G}_{dxi}H_b(\mathrm{z})}\right\} \tag{A.13b}$$

Finally, substituting Equations (A.13a) and (A.13b) into (A.12c), the closed-loop transfer function $G_{iairef}(z)$ can be derived as:

$$\frac{\tilde{i}_a(\mathrm{z})}{\tilde{i}_{ref}(\mathrm{z})} = \mathrm{C}(\mathrm{z})\left\{\frac{G_{di}(\mathrm{z}) + \mathrm{G}_{dxi}(\mathrm{z}) + \mathrm{C}(\mathrm{z})\left\{\mathrm{G}_{di}(\mathrm{z})\left[G_{di}H_b(\mathrm{z}) - \mathrm{G}_{dxi}H_a(\mathrm{z})\right] + \mathrm{G}_{dxi}(\mathrm{z})\left[G_{di}H_a(\mathrm{z}) - z\,\mathrm{G}_{dxi}H_b(\mathrm{z})\right]\right\}}{\left[C(\mathrm{z})\mathrm{G}_{di}H_a(\mathrm{z}) + 1\right]\left[C(\mathrm{z})\mathrm{G}_{di}H_b(\mathrm{z}) + 1\right] - C^2(\mathrm{z})\mathrm{G}_{dxi}H_a(\mathrm{z})\mathrm{G}_{dxi}H_b(\mathrm{z})}\right\} \ldots$$

…(A.14a)

In a similar way, substituting Equations (A.13a) and (A.13b) into (A.12d), $G_{ibiref}(z)$ can be found:

$$\frac{\tilde{i}_b(\mathrm{z})}{\tilde{i}_{ref}(\mathrm{z})} = \mathrm{C}(\mathrm{z})\left\{\frac{G_{di}(\mathrm{z}) + \mathrm{G}_{dxi}(\mathrm{z}) + \mathrm{C}(\mathrm{z})\left\{\mathrm{G}_{di}(\mathrm{z})\left[G_{di}H_a(\mathrm{z}) - z\,\mathrm{G}_{dxi}H_b(\mathrm{z})\right] + \mathrm{G}_{dxi}(\mathrm{z})\left[G_{di}H_b(\mathrm{z}) - \mathrm{G}_{dxi}H_a(\mathrm{z})\right]\right\}}{\left[C(\mathrm{z})\mathrm{G}_{di}H_a(\mathrm{z}) + 1\right]\left[C(\mathrm{z})\mathrm{G}_{di}H_b(\mathrm{z}) + 1\right] - C^2(\mathrm{z})\mathrm{G}_{dxi}H_a(\mathrm{z})\mathrm{G}_{dxi}H_b(\mathrm{z})}\right\} \ldots$$

…(A.14b)

To further simplify Equations (A.14a) and (A.14b) it can be assumed that the current transducers have unity gain $H_a(s) = H_b(s) = 1$, resulting in:

$$G_{iairef}(z) = \frac{\tilde{i}_a(z)}{\tilde{i}_{ref}(z)} = \frac{C(z)\left[G_{di}(z) + G_{dxi}(z)\right]\left[1 + C(z)G_{di}(z) - C(z)G_{dxi}(z)\right]}{\left[1 + C(z)G_{di}(z)\right]^2 + C^2(z){G_{dxi}}^2(z)} \tag{A.15a}$$

$$G_{ibiref}(z) = \frac{\tilde{i}_b(z)}{\tilde{i}_{ref}(z)} = \frac{C(z)\left[G_{di}(z) + G_{dxi}(z)\right]\left[1 + C(z)G_{di}(z) - C(z)G_{dxi}(z)\right]}{\left[1 + C(z)G_{di}(z)\right]^2 + C^2(z){G_{dxi}}^2(z)} \tag{A.15b}$$

Appendix B
MATLAB Scripts

This appendix comprises the MATLAB scripts that were employed in this work to plot the results of the analytical closed-loop models of the DIBC with IPT presented in Chapter 4.

B.1. Calculation of the closed-loop transfer functions

The script shown at the end of this section was employed to calculate the numerical solution of the analytical closed-loop transfer functions of the DIBC with IPT shown in Chapter 4, Table 4.2.

_____MATLAB Script_____

```
%TITLE:     MODEL OF THE DIGITAL AVERAGE-CURRENT CONTROL LOOP FOR THE
%           DUAL INTERLEAVED BOOST CONVERTER WITH INTERPHASE TRASNFORMER
%FILE NAME: DIBC_DACC_NoDelay.m
%AUTHOR:    Alejandro Villarruel-Parra, alexvip_22@hotmail.com
%VERSION:   6.0 - DEC 2014, FINAL THESIS VERSION

clc;
clear;

Ts = 1/30000;
Tspha = [Ts];
Tsphb = [Ts (Ts/2)];

Kp = 10*Ts;
Ki = 20;

Delay_proc = (0.21*Ts);

L_c = 75.14e-6;
L = 5.12e-6;
M = L_c*(0.997);

LT = 2*L*(L_c + M) + ((L_c^2) - (M^2));

C = 45e-6;
%V_o = 220;
```

```
V_i = 100;
R_l = 5.2;
R_in = 0.029;
%P = 25000;
%Iin = P/V_i
Iin = 120;
D = 1 - sqrt((V_i/(R_l*Iin)))
%D = 0.63;
%V_i = (1-D)*V_o
%Iin = (V_i)/(R_l*((1-D)^2))
%V_o = V_i/(1-D);
Step_Duty = D*0.05;
Step_Iref = 1;

Aav = [((-R_in*(L_c+M))/LT) ((-R_in*(L_c+M))/LT) (-((1-
D)*(L_c+M))/(LT));((-R_in*(L_c+M))/LT) ((-R_in*(L_c+M))/LT) (-((1-
D)*(L_c+M))/(LT));((1-D)/C) ((1-D)/C) ((-1)/(R_l*C))];
Bav = [((V_i*(L+L_c))/((1-D)*LT)) (((-V_i)*(L-M))/((1-D)*LT)) 0;(((-
V_i)*(L-M))/((1-D)*LT)) ((V_i*(L+L_c))/((1-D)*LT)) 0;((-
V_i)/(2*R_l*C*((1-D)^2))) ((-V_i)/(2*R_l*C*((1-D)^2))) (1/C)];
Cav = [1 0 0;0 1 0;0 0 1];
Dav = [0 0 0;0 0 0;0 0 0];

X0 = [0;0;0];
X02 = [(V_i/(2*R_l*((1-D)^2)));(V_i/(2*R_l*((1-D)^2)));(V_i/(1-D))];

SSav = ss(Aav,Bav,Cav,0); %State Space of the Average Small-signal model.
TFav = tf(SSav);    %Individual transfer functions of all the state
space.

%TFav Distribution
%{
               +----------------------+
               |     |1.da |2.db |3.iz |
               |---- |-----|-----|-----|
               |1.Ia |Gdaia|Gdbia|Gizia|
               |---- |-----|-----|-----|
               |2.Ib |Gdaib|Gdbib|Gizib|
               |---- |-----|-----|-----|
               |3.vo |Gdavo|Gdbvo|Gizvo|
               +----------------------+
%}

%Tranfer Functions
Gdaia = TFav(1,1);
Gdaib = TFav(2,1);
Gdbia = TFav(1,2);
Gdbib = TFav(2,2);
Gdavo = TFav(3,1);
Gdbvo = TFav(3,2);
Gizia = TFav(1,3);
Gizib = TFav(2,3);
Gizvo = TFav(3,3);

[numGdaia,denGdaia] = tfdata(Gdaia,'v');
[numGdaib,denGdaib] = tfdata(Gdaib,'v');
[numGdbia,denGdbia] = tfdata(Gdbia,'v');
[numGdbib,denGdbib] = tfdata(Gdbib,'v');
```

```
Gdi =
minreal(absorbDelay(c2d(tf(numGdaia,denGdaia,'iodelay',(Delay_proc)),Ts,'
zoh')));
Gdxi =
minreal(absorbDelay(c2d(tf(numGdaib,denGdaib,'iodelay',(Delay_proc)),Ts,'
zoh')));

if (Delay_proc < (0.5*Ts))||(Delay_proc > (0.51*Ts))
    Gdxi_phi =
zpk(minreal(absorbDelay(c2d(tf(numGdaib,denGdaib,'iodelay',((Ts/2)+Delay_
proc)),Ts,'zoh'))));
    Gdxi_teta =
zpk(minreal(tf([10],1,Ts)*absorbDelay(c2d(tf(numGdaib,denGdaib,'iodelay',
(Ts-(Ts/2)+Delay_proc)),Ts,'zoh'))));
else
    Gdxi_phi =
zpk(minreal(tf(1,[10],Ts)*(c2d(tf(numGdaib,denGdaib),Ts,'zoh'))));
    Gdxi_teta = zpk(minreal(c2d(tf(numGdaib,denGdaib),Ts,'zoh')));
end

Comp = pid(Kp,Ki,0,0,Ts,'IFormula','BackwardEuler');
%Comp = zpk([],[1],Kp,Ts);

Num_IaIref = zpk(minreal(Comp*(Gdi + Gdxi)));
Den_IaIref = zpk(minreal(1 + Comp*(Gdi + Gdxi)));
IaIref = zpk(minreal((Num_IaIref/Den_IaIref)));
[numIaIref denIaIref] = tfdata(IaIref,'v');
CE_IaIref = zpk(minreal(Comp*(Gdi + Gdxi)));

A = minreal(Comp*((Gdi^2)-(Gdxi_phi*Gdxi_teta)));
B = minreal(2*Comp*Gdi);

Num_IaIref3 = minreal(zpk(Comp*(Gdi + Gdxi_phi + A)));
Den_IaIref3 = zpk(minreal(1 + B + minreal(Comp*A)));
IaIref3 = zpk(minreal((Num_IaIref3/Den_IaIref3)));
[numIaIref3 denIaIref3] = tfdata(IaIref3,'v');
CE_IaIref3 = zpk(minreal(B + minreal(Comp*A)));

Num_IbIref3 = zpk(minreal(Comp*(Gdi + Gdxi_teta + A)));
IbIref3 = zpk(minreal((Num_IbIref3/Den_IaIref3)));
[numIbIref3 denIbIref3] = tfdata(IbIref3,'v');

figure(1);
step(IaIref3);
hold on;
```

B.2. Stability range script

This script was employed to obtain the stability region plots shown in Chapter 4, employing the transfer functions listed in Table 4.2, Chapter 2. It operates by evaluating in an iterative manner the stability of the transfer-functions for different values of proportional and integral gains. The resulting data is stored in a *.txt* file which was plotted

employing ORIGINLAB. This program is comprised by two scripts. The outer-loop script defines the parameters and stores the data of each iteration whilst the Inner-loop script calculates the closed-loop transfer functions of the converter for each iteration.

_____MATLAB Script_____

```
%TITLE:     STABILITY RANGE PLOTS FOR THE AVERAGE-CURRENT CONTROL
%           OF THE DIBC WITH IPT (OUTER LOOP)
%FILE NAME: Stability_Analysis2
%AUTHOR:    Alejandro Villarruel-Parra, alexvip_22@hotmail.com
%VERSION:   2.0 - JAN 2015, FINAL THESIS VERSION

clc;
clear;

Ts = 1/30000;
Delay_proc = (0.5*Ts);

L_c = 75.14e-6;
L = 5.12e-6;
M = L_c*(0.997);

LT = 2*L*(L_c + M) + ((L_c^2) - (M^2));

C = 45e-6;
%V_o = 220;
V_i = 100;
R_l = 5.2;
R_in = 0.029;
%P = 25000;
%Iin = P/V_i
Iin = 120;
D = 1 - sqrt((V_i/(R_l*Iin)))
%D = 0.8;
%V_i = (1-D)*V_o
%Iin = (V_i)/(R_l*((1-D)^2))
V_o = V_i/(1-D)

file_name = '5R2_Iin120_Vin100_Sync_0Td5.txt';
fid = fopen(file_name,'w');
fprintf(fid,'R_load = %f\t',R_l);
fprintf(fid,'D = %f\t',D);
fprintf(fid,'\n');
fprintf(fid,['Ki\t','Kp_min\t','Kp_max\t']);
fprintf(fid,'\n');

file_name = '5R2_Iin120_Vin100_NonSync_0Td5.txt';
fid2 = fopen(file_name,'w');
fprintf(fid2,'R_load = %f\t',R_l);
fprintf(fid2,'D = %f\t',D);
fprintf(fid2,'\n');
fprintf(fid2,['Ki\t','Kp_min\t','Kp_max\t']);
fprintf(fid2,'\n');

handle_wait = waitbar(0,['Currently Evaluating Ki=',num2str(j)]);
```

```
%Res_Ki = [logspace(-2,log10(0.09),10),logspace(-
1,log10(0.9),10),logspace(0,log10(9),20),logspace(1,log10(60),30)];
%Res_Kp = [logspace(log10(0.005),log10(0.09),15),logspace(-
1,log10(0.9),10),logspace(0,log10(9),20),logspace(1,log10(100),60)];

%Res_Ki = [logspace(-2,log10(0.09),10),logspace(-
1,log10(0.9),10),logspace(0,log10(9),20),logspace(1,log10(90),20),logspac
e(2,log10(200),20)];
%Res_Kp =
[logspace(log10(0.0005),log10(0.009),7),logspace(log10(0.001),log10(0.09)
,10),logspace(-
1,log10(0.9),10),logspace(0,log10(9),20),logspace(1,log10(200),80)];

Res_Ki = logspace(0,log10(100),50);
Res_Kp =
[logspace(log10(0.1),log10(0.9),15),logspace(log10(1),log10(9),15),10:2.5
:200];

y = 1;
for j = Res_Ki
    waitbar((y/length(Res_Ki)),handle_wait,['Currently Evaluating
Ki=',num2str(j)]);
    Ki = j;
    x = 1;
    flag = 0;
    Stability_IaIref = nan(length(Res_Ki),2);
    Stability_IaIref3 = nan(length(Res_Ki),2);
    Stability_IbIref3 = nan(length(Res_Ki),2);
    for k = Res_Kp
        Kp = k*Ts;
        run Stability_Analysis;
        Stability_IaIref(x,1) = Ki;
        Stability_IaIref3(x,1) = Ki;
        Stability_IbIref3(x,1) = Ki;
        if isstable(IaIref)
            Stability_IaIref(x,2) = Kp/Ts;
        else
            Stability_IaIref(x,2) = NaN;
        end
        if isstable(IaIref3)
            Stability_IaIref3(x,2) = Kp/Ts;
        else
            Stability_IaIref3(x,2) = NaN;
        end
        if isstable(IbIref3)
            Stability_IbIref3(x,2) = Kp/Ts;
        else
            Stability_IbIref3(x,2) = NaN;
        end
        x = x+1;
    end

    [Val Index] = min(Stability_IaIref);
    StabilityRange(1,1:2) = Stability_IaIref(Index(1,2),:);
    [Val Index] = min(Stability_IaIref3);
    StabilityRange(1,3:4) = Stability_IaIref3(Index(1,2),:);
    [Val Index] = max(Stability_IaIref);
    StabilityRange(2,1:2) = Stability_IaIref(Index(1,2),:);
    [Val Index] = max(Stability_IaIref3);
```

```
    StabilityRange(2,3:4) = Stability_IaIref3(Index(1,2),:);

    fprintf(fid,'%f\t',Ki);
    fprintf(fid,'%f\t',StabilityRange(1,2));
    fprintf(fid,'%f\t',StabilityRange(2,2));
    fprintf(fid,'\n');

    fprintf(fid2,'%f\t',Ki);
    fprintf(fid2,'%f\t',StabilityRange(1,4));
    fprintf(fid2,'%f\t',StabilityRange(2,4));
    fprintf(fid2,'\n');
    y = y +1;
end
close(handle_wait);
fclose('all');
```

MATLAB Script

```
%TITLE:     STABILITY RANGE PLOTS FOR THE AVERAGE-CURRENT CONTROL
%           OF THE DIBC WITH IPT (INNER LOOP)
%FILE NAME: Stability_Analysis
%AUTHOR:    Alejandro Villarruel-Parra, alexvip_22@hotmail.com
%VERSION:   2.0 - JAN 2015, FINAL THESIS VERSION


Aav = [((-R_in*(L_c+M))/LT) ((-R_in*(L_c+M))/LT) (-((1-
D)*(L_c+M))/(LT));((-R_in*(L_c+M))/LT) ((-R_in*(L_c+M))/LT) (-((1-
D)*(L_c+M))/(LT));((1-D)/C) ((1-D)/C) ((-1)/(R_l*C))];
Bav = [((V_i*(L+L_c))/((1-D)*LT)) (((-V_i)*(L-M))/((1-D)*LT)) 0;(((-
V_i)*(L-M))/((1-D)*LT)) ((V_i*(L+L_c))/((1-D)*LT)) 0;((-
V_i)/(2*R_l*C*((1-D)^2))) ((-V_i)/(2*R_l*C*((1-D)^2))) (1/C)];
Cav = [1 0 0;0 1 0;0 0 1];
Dav = [0 0 0;0 0 0;0 0 0];

X0 = [0;0;0];
X02 = [(V_i/(2*R_l*((1-D)^2)));(V_i/(2*R_l*((1-D)^2)));(V_i/(1-D))];

SSav = ss(Aav,Bav,Cav,Dav); %State Space of the Average Small-signal
model.
TFav = tf(SSav);    %Individual transfer functions of all the state
space.

%Tranfer Functions
Gdaia = TFav(1,1);
Gdaib = TFav(2,1);
Gdbia = TFav(1,2);
Gdbib = TFav(2,2);
Gdavo = TFav(3,1);
Gdbvo = TFav(3,2);

[numGdaia denGdaia] = tfdata(Gdaia,'v');
[numGdaib denGdaib] = tfdata(Gdaib,'v');
[numGdbia denGdbia] = tfdata(Gdbia,'v');
[numGdbib denGdbib] = tfdata(Gdbib,'v');
```

```
Gdi =
minreal(absorbDelay(c2d(tf(numGdaia,denGdaia,'iodelay',(Delay_proc)),Ts,'
zoh')));
Gdxi =
minreal(absorbDelay(c2d(tf(numGdaib,denGdaib,'iodelay',(Delay_proc)),Ts,'
zoh')));

if (Delay_proc < (0.5*Ts))||(Delay_proc > (0.51*Ts))
    Gdxi_phi =
zpk(minreal(absorbDelay(c2d(tf(numGdaib,denGdaib,'iodelay',((Ts/2)+Delay_
proc)),Ts,'zoh'))));
    Gdxi_teta = zpk(minreal(tf([1
0],1,Ts)*absorbDelay(c2d(tf(numGdaib,denGdaib,'iodelay',(Ts-
(Ts/2)+Delay_proc)),Ts,'zoh'))));
else
    Gdxi_phi = zpk(minreal(tf(1,[1
0],Ts)*(c2d(tf(numGdaib,denGdaib),Ts,'zoh'))));
    Gdxi_teta = zpk(minreal(c2d(tf(numGdaib,denGdaib),Ts,'zoh')));
end

Comp = pid(Kp,Ki,0,0,Ts,'IFormula','BackwardEuler');

Num_IaIref = zpk(minreal(Comp*(Gdi + Gdxi)));
Den_IaIref = zpk(minreal(1 + Comp*(Gdi + Gdxi)));
IaIref = zpk(minreal((Num_IaIref/Den_IaIref)));
[numIaIref denIaIref] = tfdata(IaIref,'v');
CE_IaIref = zpk(minreal(Comp*(Gdi + Gdxi)));

A = minreal(Comp*((Gdi^2)-(Gdxi_phi*Gdxi_teta)));
B = minreal(2*Comp*Gdi);

Num_IaIref3 = minreal(zpk(Comp*(Gdi + Gdxi_phi + A)));
Den_IaIref3 = zpk(minreal(1 + B + minreal(Comp*A)));
IaIref3 = zpk(minreal((Num_IaIref3/Den_IaIref3)));
[numIaIref3 denIaIref3] = tfdata(IaIref3,'v');
CE_IaIref3 = zpk(minreal(B + minreal(Comp*A)));

Num_IbIref3 = zpk(minreal(Comp*(Gdi + Gdxi_teta + A)));
IbIref3 = zpk(minreal((Num_IbIref3/Den_IaIref3)));
[numIbIref3 denIbIref3] = tfdata(IbIref3,'v');
```

B.3. Root-loci plots

This script was employed to produce the root locus plots presented in Chapter 4, Section 4.5. This program is comprised by two scripts. The outer-loop script defines the evaluation parameters and plots the poles of the closed-loop transfer functions for each iteration. The Inner loop script calculates the closed-loop transfer functions of the converter for the parameters defined in the outer loop.

MATLAB Script

```
%TITLE:     ROOT LOCI OF THE DIGITAL AVERAGE-CURRENT CONTROLLED
%           DIBC WITH IPT (OUTER LOOP)
%FILE NAME: PZ_MAPS_2.m
%AUTHOR:    Alejandro Villarruel-Parra, alexvip_22@hotmail.com
%VERSION:   2.0 - FEB 2015, FINAL THESIS VERSION

clc;
clear;

Ts = 1/30000;
Tspha = [Ts];
Tsphb = [Ts (Ts/2)];

Kp = 40*Ts;
Ki = 10;

colorcito = color(6);

Comp = pid(Kp,Ki,0,0,Ts,'IFormula','BackwardEuler');
%Comp = Kp*Ts;
%Comp = zpk([],[1],Kp,Ts);

Delay_proc = (0.5*Ts);

L_c = 75.14e-6;
L = 5.12e-6;
M = L_c*(0.997);

LT = 2*L*(L_c + M) + ((L_c^2) - (M^2));

C = 45e-6;
V_i = 50;
R_l = 5.2;
R_in = 0.029;
%P = 4500;
%Iin = P/V_i
%Iin = (30.7*2);
%D = 1 - sqrt((V_i/(R_l*Iin)))
%D = 0.63;
%Iin = (V_i)/(R_l*((1-D)^2))
%V_o = V_i/(1-D)
%P = V_i*Iin
clpoles = [];
clpoles3 = [];
param = [];
x = 1;

for D = [0.2:0.05:0.8]
    PZ_MAPS;
    %Num_CE3 = (pole(IaIref))';
    Num_CE3 = (pole(IaIref3))';
    real_CE3 = real(Num_CE3);
    [CE3sortedreal,index] = sort(real_CE3);
    Num_CE3 = Num_CE3(index);
    imag_CE3 = imag(Num_CE3);
    [CE3sortedimag,index] = sort(imag_CE3);
    Num_CE3 = Num_CE3(index);
    param = [param;D];
    clpoles3 = [clpoles3;Num_CE3];
```

```
end

%General Plots To Establish the Context
hf1 = figure(1);
units = get(hf1,'Units');
set(hf1,'Units','inches');
set(hf1,'Position',[15,0.2,7,6.5]); set(hf1,'Units',units);
for x = 1:length(clpoles3(1,:))
    p_h = plot(real(clpoles3(:,x)),imag(clpoles3(:,x)),'x-');
    set(p_h,'Color',colorcito);
    hold on;
end
set(gca,'xtick',[-3,-2,-1,0,1]);
set(gca,'ytick',[-1,0,1]);
xlabel('Real Axis');
ylabel('Imaginary Axis');
title(sprintf('Root Locus - Poles of G_i_a_i_r_e_f(s) and
G_i_b_i_r_e_f(s)\n R_l_o_a_d = %5.1f; V_i_n = %5.1f',R_l,V_i));
zgrid;
grid;

hf2 = figure(2);
for x = 1:length(clpoles3(1,:))
    p_h = plot(real(clpoles3(:,x)),imag(clpoles3(:,x)),'x-');
    set(p_h,'Color',colorcito);
    hold on;
end
axis([0.75 1 -0.25 0.25]);
xlabel('Real Axis');
ylabel('Imaginary Axis');
title(sprintf('Root Locus - Poles of G_i_a_i_r_e_f(s) and
G_i_b_i_r_e_f(s)\n R_l_o_a_d = %5.1f; V_i_n = %5.1f',R_l,V_i));
zgrid;
grid;
```

MATLAB Script

```
%TITLE:     ROOT LOCI OF THE DIGITAL AVERAGE-CURRENT CONTROLLED
%           DIBC WITH IPT (INNER LOOP)
%FILE NAME: PZ_MAPS.m
%AUTHOR:    Alejandro Villarruel-Parra, alexvip_22@hotmail.com
%VERSION:   2.0 - FEB 2015, FINAL THESIS VERSION

Aav = [((-R_in*(L_c+M))/LT) ((-R_in*(L_c+M))/LT) (-((1-
D)*(L_c+M))/(LT));((-R_in*(L_c+M))/LT) ((-R_in*(L_c+M))/LT) (-((1-
D)*(L_c+M))/(LT));((1-D)/C) ((1-D)/C) ((-1)/(R_l*C))];
Bav = [((V_i*(L+L_c))/((1-D)*LT)) (((-V_i)*(L-M))/((1-D)*LT)) 0;(((-
V_i)*(L-M))/((1-D)*LT)) ((V_i*(L+L_c))/((1-D)*LT)) 0;((-
V_i)/(2*R_l*C*((1-D)^2))) ((-V_i)/(2*R_l*C*((1-D)^2))) (1/C)];
Cav = [1 0 0;0 1 0;0 0 1];
Dav = [0 0 0;0 0 0;0 0 0];

X0 = [0;0;0];
X02 = [(V_i/(2*R_l*((1-D)^2)));(V_i/(2*R_l*((1-D)^2)));(V_i/(1-D))];

SSav = ss(Aav,Bav,Cav,0); %State Space of the Average Small-signal model.
```

```
TFav = tf(SSav);    %Individual transfer functions of all the state
space.

%Tranfer Functions
Gdaia = TFav(1,1);
Gdaib = TFav(2,1);
Gdbia = TFav(1,2);
Gdbib = TFav(2,2);
Gdavo = TFav(3,1);
Gdbvo = TFav(3,2);
Gizia = TFav(1,3);
Gizib = TFav(2,3);
Gizvo = TFav(3,3);

[numGdaia,denGdaia] = tfdata(Gdaia,'v');
[numGdaib,denGdaib] = tfdata(Gdaib,'v');
[numGdbia,denGdbia] = tfdata(Gdbia,'v');
[numGdbib,denGdbib] = tfdata(Gdbib,'v');

Gdi =
minreal(absorbDelay(c2d(tf(numGdaia,denGdaia,'iodelay',(Delay_proc)),Ts,'
zoh')));
Gdxi =
minreal(absorbDelay(c2d(tf(numGdaib,denGdaib,'iodelay',(Delay_proc)),Ts,'
zoh')));

if (Delay_proc < (0.5*Ts))||(Delay_proc > (0.51*Ts))
    Gdxi_phi =
zpk(minreal(absorbDelay(c2d(tf(numGdaib,denGdaib,'iodelay',((Ts/2)+Delay_
proc)),Ts,'zoh'))));
    Gdxi_teta = zpk(minreal(tf([1
0],1,Ts)*absorbDelay(c2d(tf(numGdaib,denGdaib,'iodelay',(Ts-
(Ts/2)+Delay_proc)),Ts,'zoh'))));
else
    Gdxi_phi = zpk(minreal(tf(1,[1
0],Ts)*(c2d(tf(numGdaib,denGdaib),Ts,'zoh'))));
    Gdxi_teta = zpk(minreal(c2d(tf(numGdaib,denGdaib),Ts,'zoh')));
end

Num_IaIref = zpk(minreal(Comp*(Gdi + Gdxi)));
Den_IaIref = zpk(minreal(1 + Comp*(Gdi + Gdxi)));
IaIref = zpk(minreal((Num_IaIref/Den_IaIref)));
[numIaIref denIaIref] = tfdata(IaIref,'v');
CE_IaIref = zpk(minreal(Comp*(Gdi + Gdxi)));

A = minreal(Comp*((Gdi^2)-(Gdxi_phi*Gdxi_teta)));
B = minreal(2*Comp*Gdi);

Num_IaIref3 = minreal(zpk(Comp*(Gdi + Gdxi_phi + A)));
Den_IaIref3 = zpk(minreal(1 + B + minreal(Comp*A)));
IaIref3 = zpk(minreal((Num_IaIref3/Den_IaIref3)));
[numIaIref3 denIaIref3] = tfdata(IaIref3,'v');
CE_IaIref3 = zpk(minreal(B + minreal(Comp*A)));

Num_IbIref3 = zpk(minreal(Comp*(Gdi + Gdxi_teta + A)));
IbIref3 = zpk(minreal((Num_IbIref3/Den_IaIref3)));
[numIbIref3 denIbIref3] = tfdata(IbIref3,'v');
```

B.4. Export files for SABER Cosmo Scope

For the purpose of result comparisons, this script allows to save time-domain and frequency-domain data generated in MATLAB into *.txt* files which are compatible with SABER Cosmo Scope.

_____MATLAB Script_____

```
%TITLE:     Export to SABER
%FILE NAME: SABER_Export.m
%AUTHOR:    Alejandro Villarruel-Parra, alexvip_22@hotmail.com

ia = extract_portion(I_a,0,I_a(length(I_a)-1,1),(Ts),X02(1,1));
ib = extract_portion(I_b,0,I_b(length(I_b)-1,1),(Ts/2),X02(2,1));
ia3 = extract_portion(I_a3,0,I_a3(length(I_a3)-1,1),(Ts),X02(1,1));
ib3 = extract_portion(I_b3,0,I_b3(length(I_b3),1),(Ts/2),X02(2,1));

%vo = extract_portion(V_o,0,V_o(length(V_o),1),0,X02(3,1));
%iref = extract_portion(I_ref,0,I_ref(length(I_ref)-1,1),0,Iin/2);
%SimulinkExport = concatenate_simulink_arrays(ia,ib);

export_dwf_saber('SimExport_Iaz.txt',{'t`s','Ia`analog`-`real'},ia);
export_dwf_saber('SimExport_Ibz.txt',{'t`s','Ib`analog`-`real'},ia);
export_dwf_saber('SimExport_Ia3z.txt',{'t`s','Ia3`analog`-`real'},ia3);
export_dwf_saber('SimExport_Ib3z.txt',{'t`s','Ib3`analog`-`real'},ib3);

%ia = extract_portion(I_a,0,I_a(length(I_a),1),0,X02(1,1));
%ib = extract_portion(I_b,0,I_b(length(I_b),1),0,X02(2,1));
%vo = extract_portion(V_o,0,V_o(length(V_o),1),0,X02(3,1));
%Dab = extract_portion(D_ab,0,D_ab(length(D_ab),1),0,D);

%SimulinkExport = concatenate_simulink_arrays(ia,ib,vo,Dab);
%export_dwf_saber('SimExport.txt',{'t`s','Ia`analog`A`real','Ib`analog`A`
real','Vo`analog`V`real','D`analog`V`real'},SimulinkExport);
```

_____MATLAB Script_____

```
function export_dwf_saber(file_name,header,data)
%Author:    Alejandro Villarruel Parra
%           alexvip_22@hotmail.com
%Version:   1.0
%Date:      August  2014
%This function is used to create a file that contains the data of anarray
%of the form f(t,y(t)).  The format of the file created is suitable
%for SABER Cosmoscope.
%   *file_name is a string of the type filename.extension.
%
%   *header is a cell of string indicating the header for the saber file:
%       h{1} = 'tname''tunit'
%       h{2} = 'y1name''y1type''y1unit''y1datatype'
%       h{3} = 'y2name''y2type''y2unit''y2datatype'
%       ...
%       h{n} = 'ynname''yntype''ynunit''yndatatype'
```

```
%
%   *data is an array of the form f(t,y1(t),y2(t),...yn(t))
%
%   Example:
%       export_dwf_saber('input_current.txt',head,Ia);
%       where:
%       head = {'t''s','Ia''analog''A''t'};
%       Ia = [t,t^2];
[hx,hy] = size(header);
[dx,dy] = size(data);
fid = fopen(file_name,'w');
for x = 1 : hy
    fprintf(fid,'%s\t',header{x});
end
fprintf(fid,'\n');
for x = 1 : dx
    for y = 1 : dy
        fprintf(fid,'%f\t',data(x,y));
    end
    fprintf(fid,'\n');
end
fclose(fid);
beep on;
beep;
beep;
beep;
msgbox('File ready','Export Data Waveform to SABER txt file','help');
end
```

Appendix C
SABER simulation models

This appendix includes the schematic diagrams of the SABER models developed to simulate the digital current control strategies for the dual-interleaved boost converter. Three simulation models were developed and are described briefly in the following sections.

C.1. Switched model of the valley-current and peak-current control

The digital valley-current and digital peak-current control strategies were modelled employing the switched model of the DIBC with IPT introduced in Chapter 2, Section 2.4.2 and a special module referred to as DSC unit. This module reproduces the functional behaviour of the control algorithms implemented in the digital signal controller that was used to control the prototype of the DIBC introduced in Chapter 3.

Figure C.1 shows the schematic diagram of the switched model of the DIBC with IPT and the DSC unit employed to model the valley-current and the peak-current control strategies. Figure C.2 shows the complete schematic diagram of the DSC unit. The module operates using z-domain sampling-signals to speed-up the simulation time in SABER. Some of the elements found in this diagram were specifically designed for this application. These elements are shown with a uniform grey fill and the code developed can be found in the last section of this appendix.

As seen in Figure C.2, the DSC unit is organized in three main stages: the Master Clock Generator, the DPWM Counters and the Control Loops A and B. Figure C.3(a) shows a magnification of the DPWM A counter whilst Figure C.3(b) shows a magnification of the phase-a control loop.

C.2. Switched model of the average-current control with normal and immediate update

Figure C.4 shows the schematic diagram of the SABER switched model of the DIBC with IPT and the DSC unit employed to model the average-current control strategies with normal and immediate update of the DPWM. Figure C.5 shows the complete schematic diagram of the DSC unit developed for this control strategies. Figure C.6(a) shows a magnification of the DPWM A counter and Figure C.6(b) shows a magnification of the phase-a control loop.

C.3. Averaged model of the average-current control with normal and immediate update

In addition to the switched model the average-current control strategies were also simulated employing the average model of the DIBC with IPT introduced in Chapter 2, Section 2.4.3. Figure C.7 shows the schematic diagram of the SABER average model of the DIBC with IPT and the DSC unit employed to model the average-current control strategies with normal and immediate update of the DPWM units. In contrast to the DSC unit employed for the switched models introduced in the previous sections, the DSC unit employed in this simulation model does not contain DPWM modules and does not account for the quantization effects of the ADC conversion, thereby reducing considerably the simulation time. Figure C.8 shows the complete schematic diagram of the DSC unit employed.

C.4. SABER Scripts

C.4.1. Z-domain selector

```
#TITLE:     Selector, z-domain SABER
#AUTHOR:    Alejandro Villarruel-Parra
#VERSION:   1.0 - DEC 2012
#SUMMARY:   This template models a controllable two-input one-output
selector.

template Selector zin1 zin2 select zout = td
state nu zin1, zin2, zout, select
number td = 0
{
      when (event_on(zin1)¦event_on(zin2)) {
```

```
            if(select < 1) {
                  schedule_event(time, zout, zin1)
            }
            else {
                  schedule_event(time, zout, zin2)
            }
      }
}
```

C.4.2. Z-domain saturation

```
#TITLE:     Saturation, z-domain SABER
#AUTHOR:    Alejandro Villarruel-Parra
#VERSION:   1.0 - DEC 2012
#SUMMARY:   This template models a saturation in the z-domain.  The
maximum and minimum limits are user selectable.

template SaturationZ zin1 zout1 = lvlmax, lvlmin
state nu zin1, zout1
number lvlmax, lvlmin
{
      when (event_on(zin1)) {
            if(zin1 >= lvlmax){
                  schedule_event(time, zout1, lvlmax)
            }
            else if (zin1 <= lvlmin) {
                  schedule_event(time, zout1, lvlmin)
            }
            else {
                  schedule_event(time, zout1, zin1)
            }
      }
}
```

C.4.3. Z-domain event generator

```
#TITLE:     Event generator, z-domain SABER
#AUTHOR:    Alejandro Villarruel-Parra
#VERSION:   1.0 - DEC 2012
#SUMMARY:   This template generates a pulse when the difference between
the input signals are smaller than epsilon.

template EventGenerator zin1 zin2 dout = epsilon
state nu zin1, zin2
state logic_4 dout
number epsilon
{
state logic_4 out_state
      when (event_on(zin2)) {
            if( abs(INT(zin1)-INT(zin2)) < epsilon) {
                  out_state = l4_1
            }
            else {
                  out_state = l4_0
            }
            schedule_event(time, dout, out_state)
      }
```

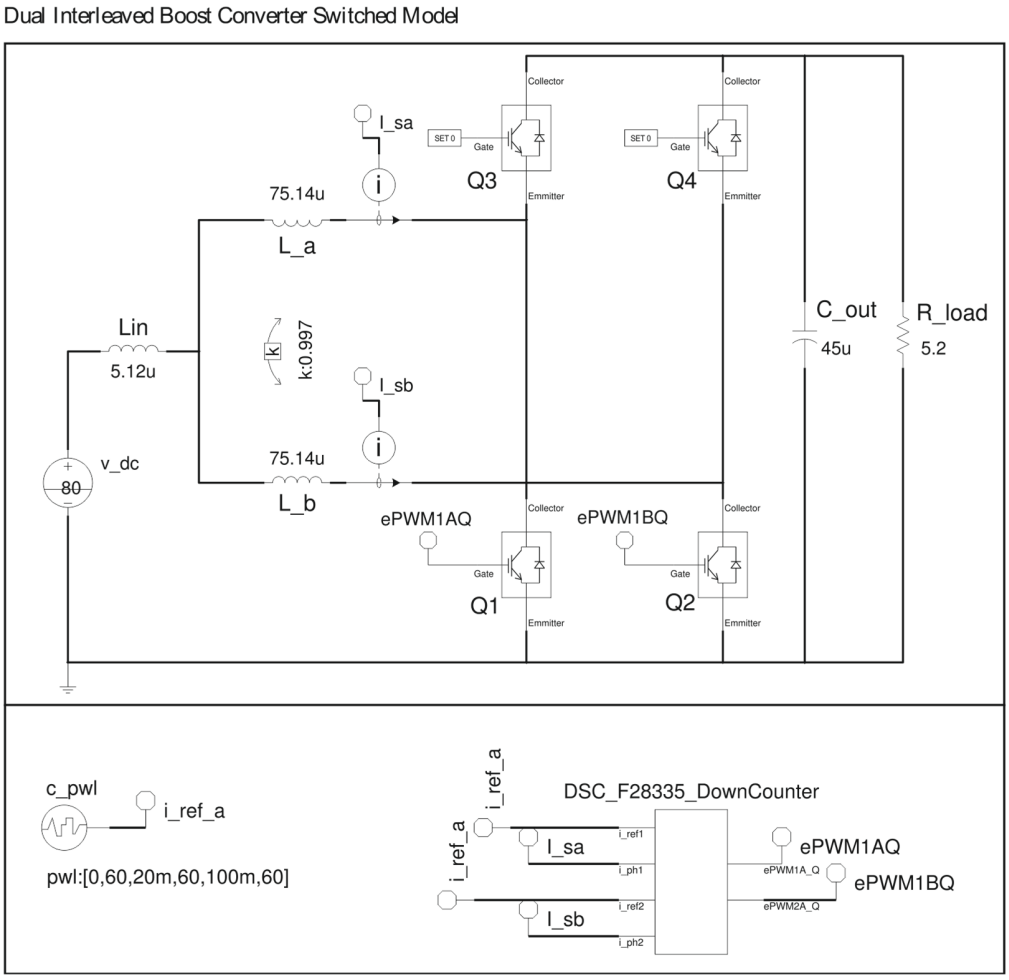


Figure C.1. SABER schematic diagram of the switched model of the DIBC with IPT and the DSC unit employed to simulate the valley-current and the peak-current control strategies.

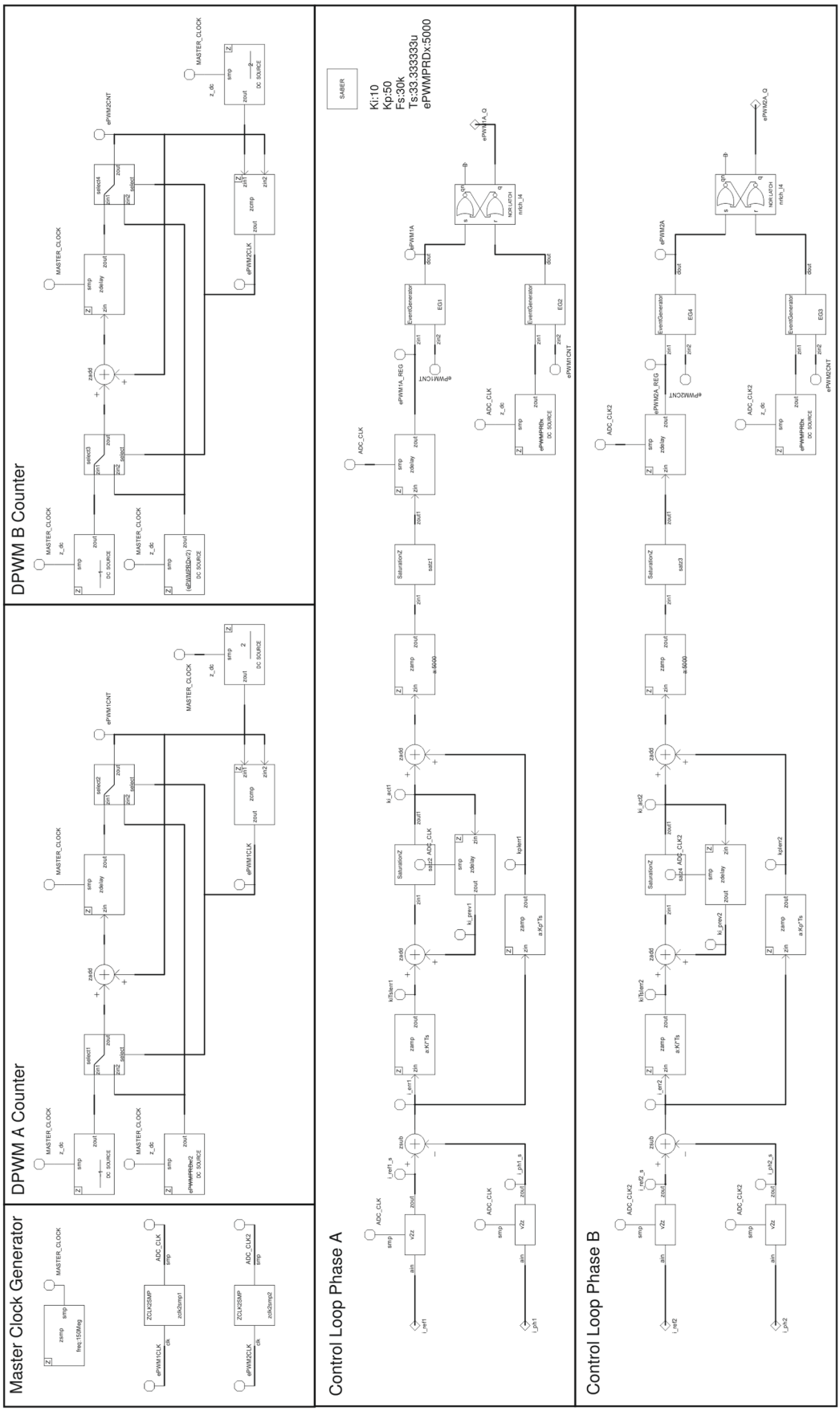


Figure C.2. SABER schematic diagram of the DSC unit employed to simulate the valley-current and the peak-current control strategies.

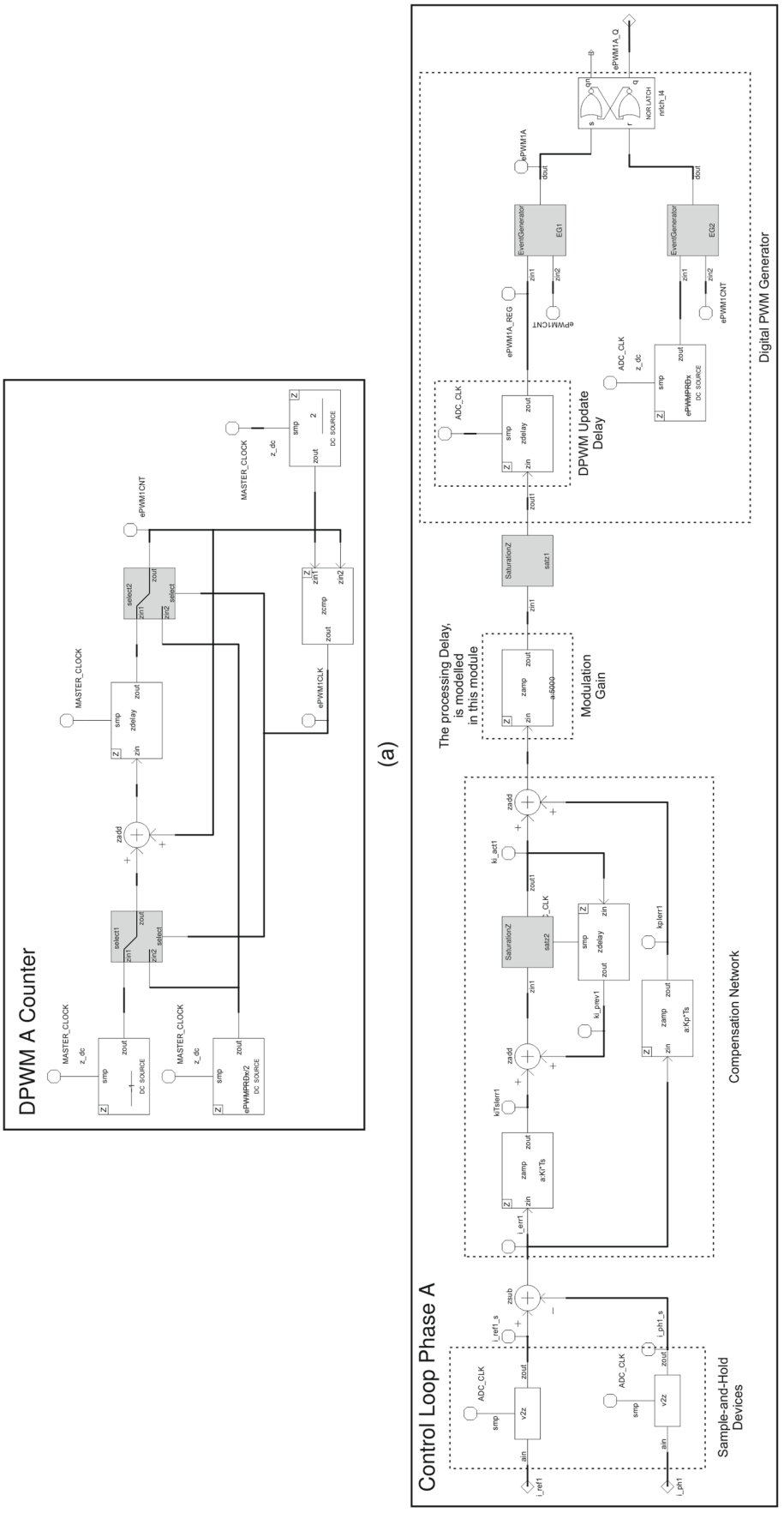


Figure C.3. SABER schematic diagram of the DSC unit employed to simulate the valley-current and the peak-current control strategies. (a) DPWM A counter; (b) Phase-a control loop.

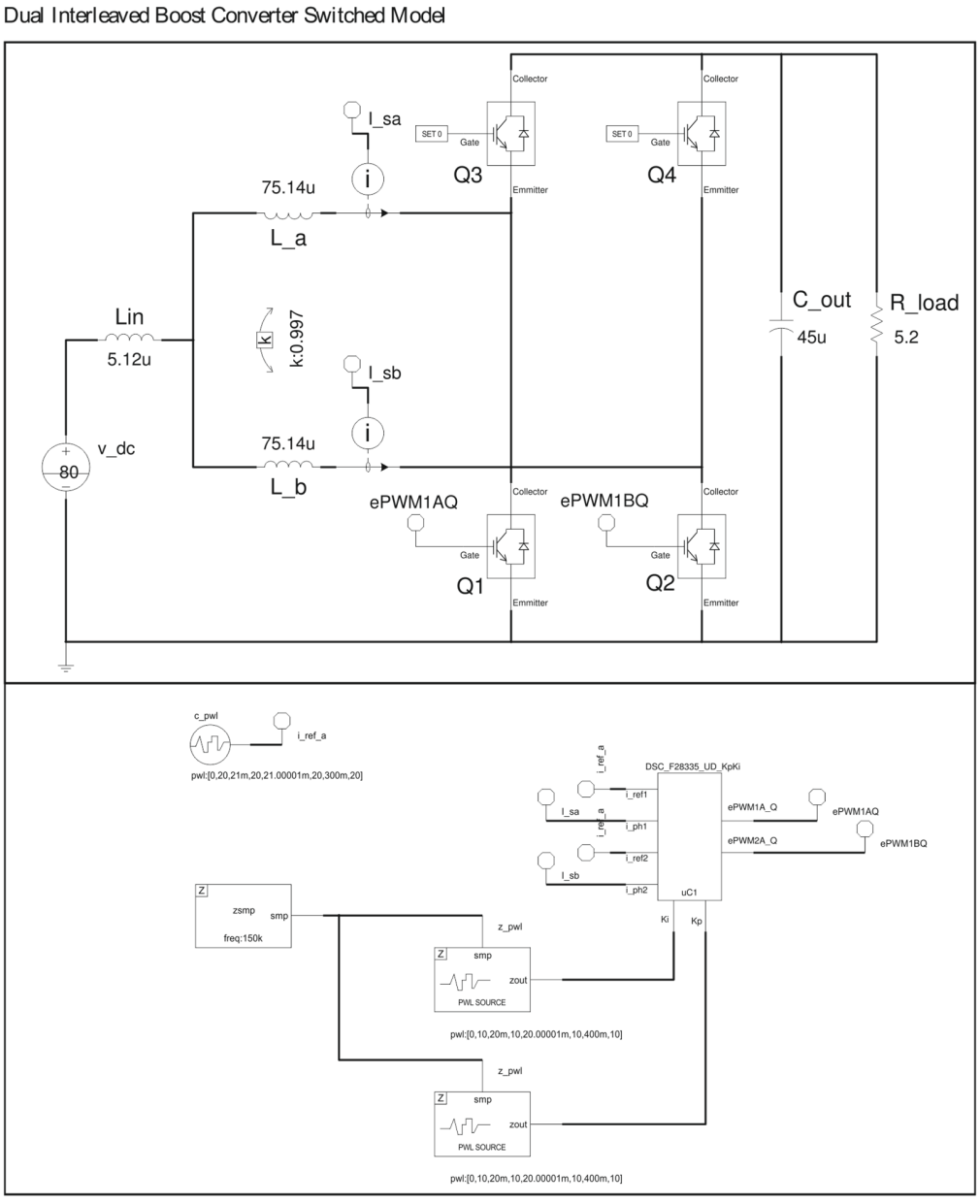


Figure C.4. SABER schematic diagram of the switched model of the DIBC with IPT and the DSC unit employed to simulate the average-current control strategies with normal and immediate update.

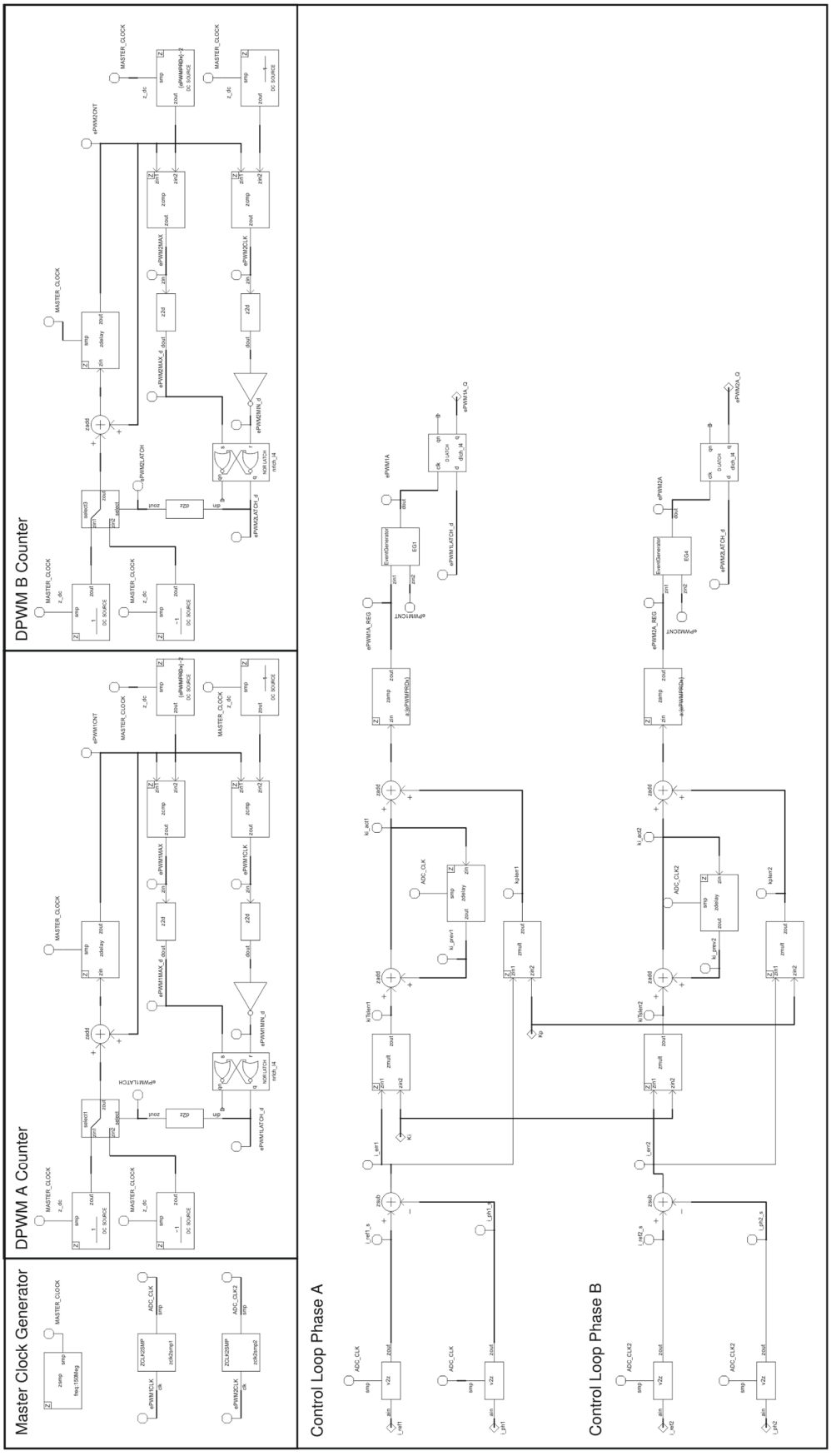


Figure C.5. SABER schematic diagram of the DSC unit employed to simulate the average-current control strategies with normal and immediate update.

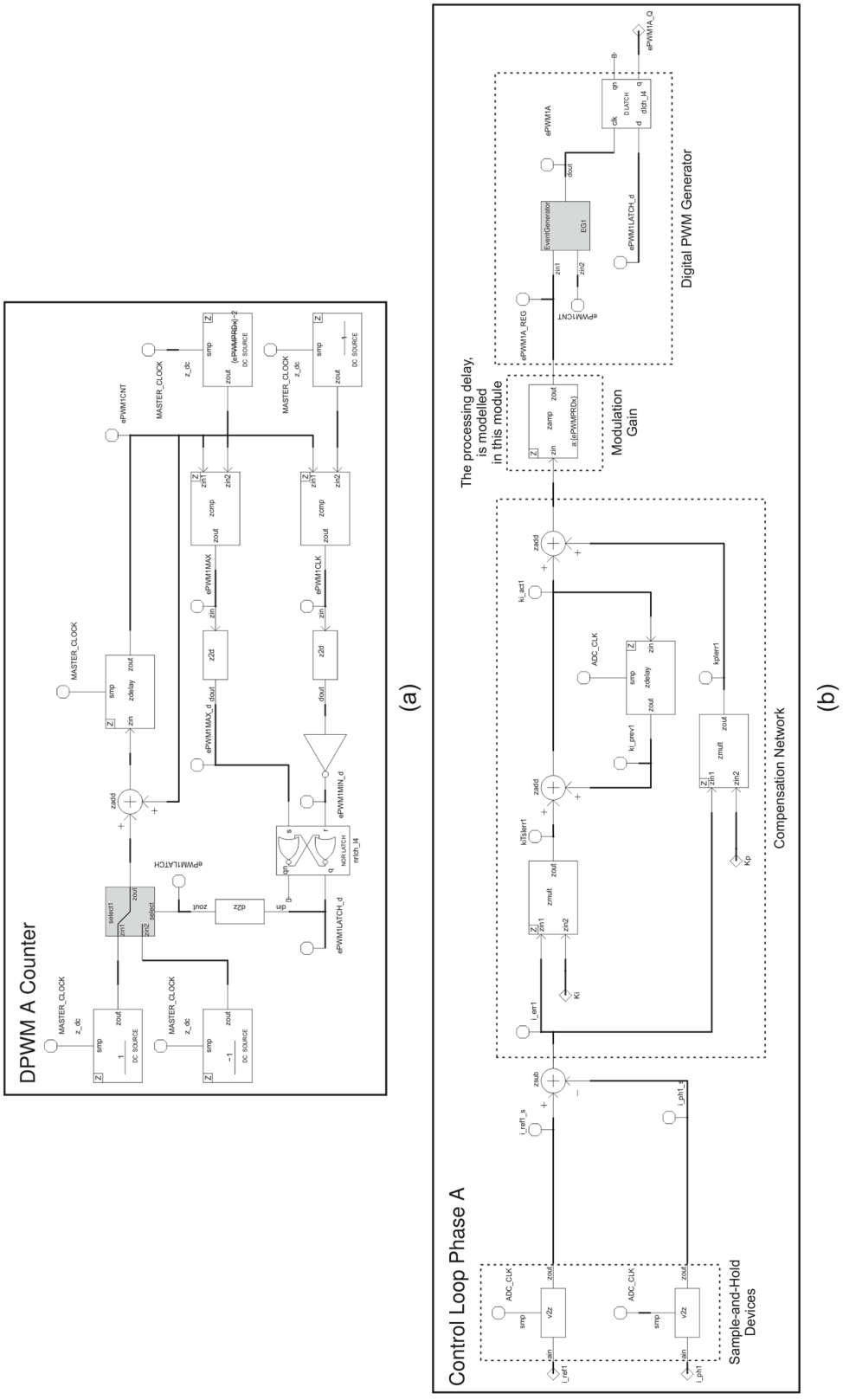


Figure C.6. SABER schematic diagram of the DSC unit employed to simulate the average-current control strategies with normal and immediate update. (a) DPWM A counter; (b) Phase-a control loop.

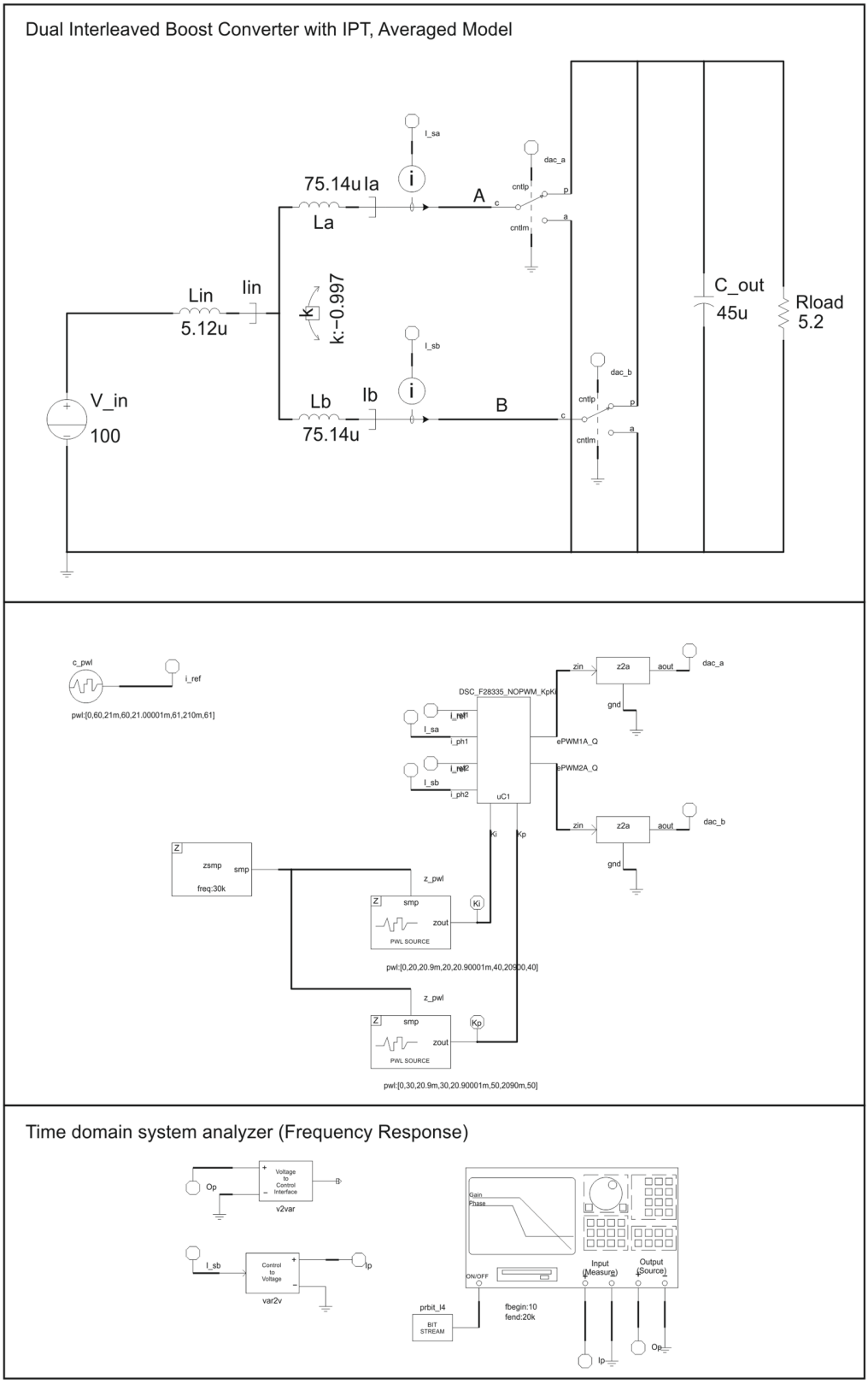


Figure C.7. SABER schematic diagram of the average model of the DIBC with IPT and the DSC unit employed to simulate the average-current control strategies with normal and immediate update.

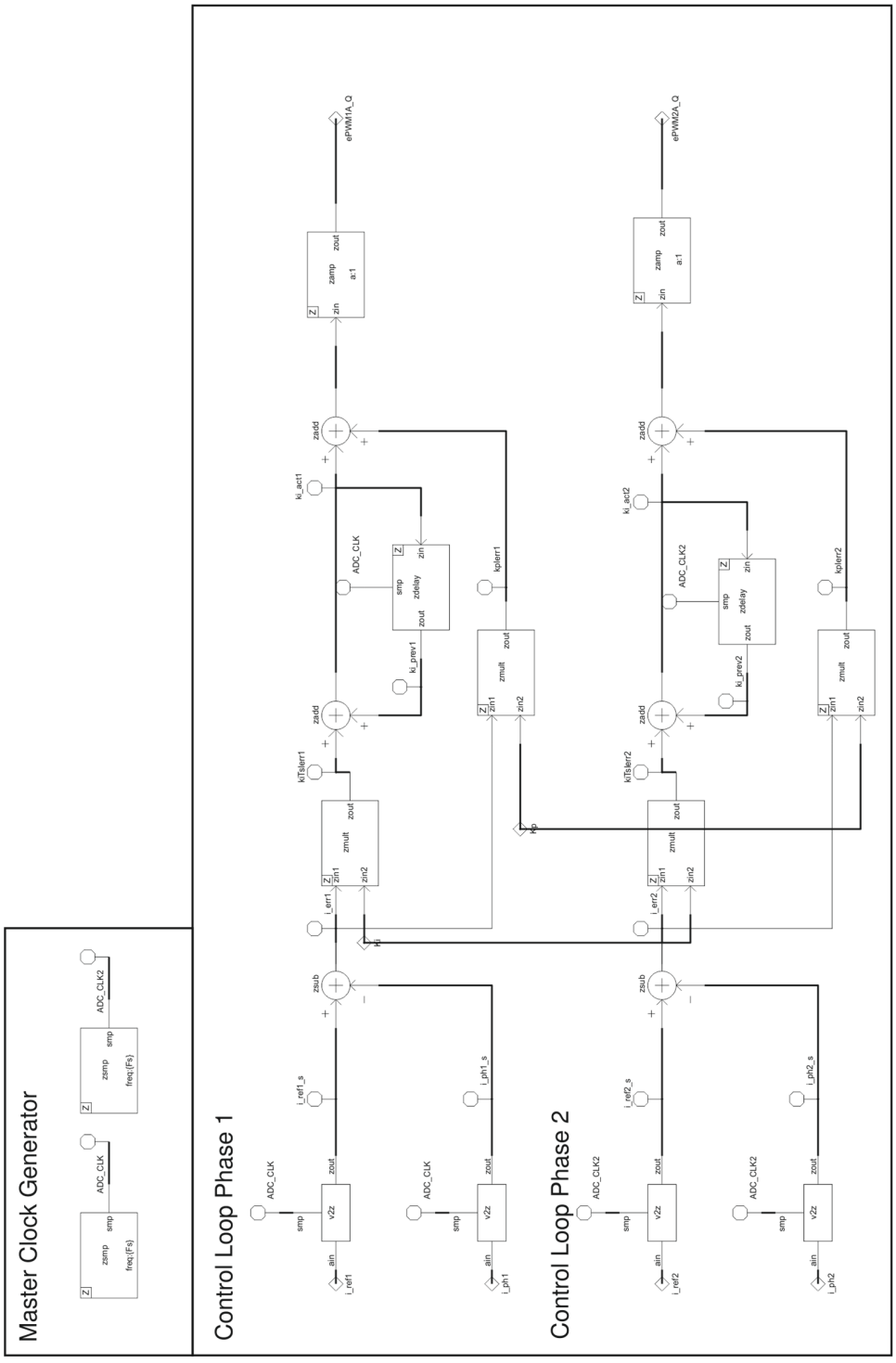


Figure C.8. SABER schematic diagram of the DSC unit employed to simulate the average-current control strategies with normal and immediate update.

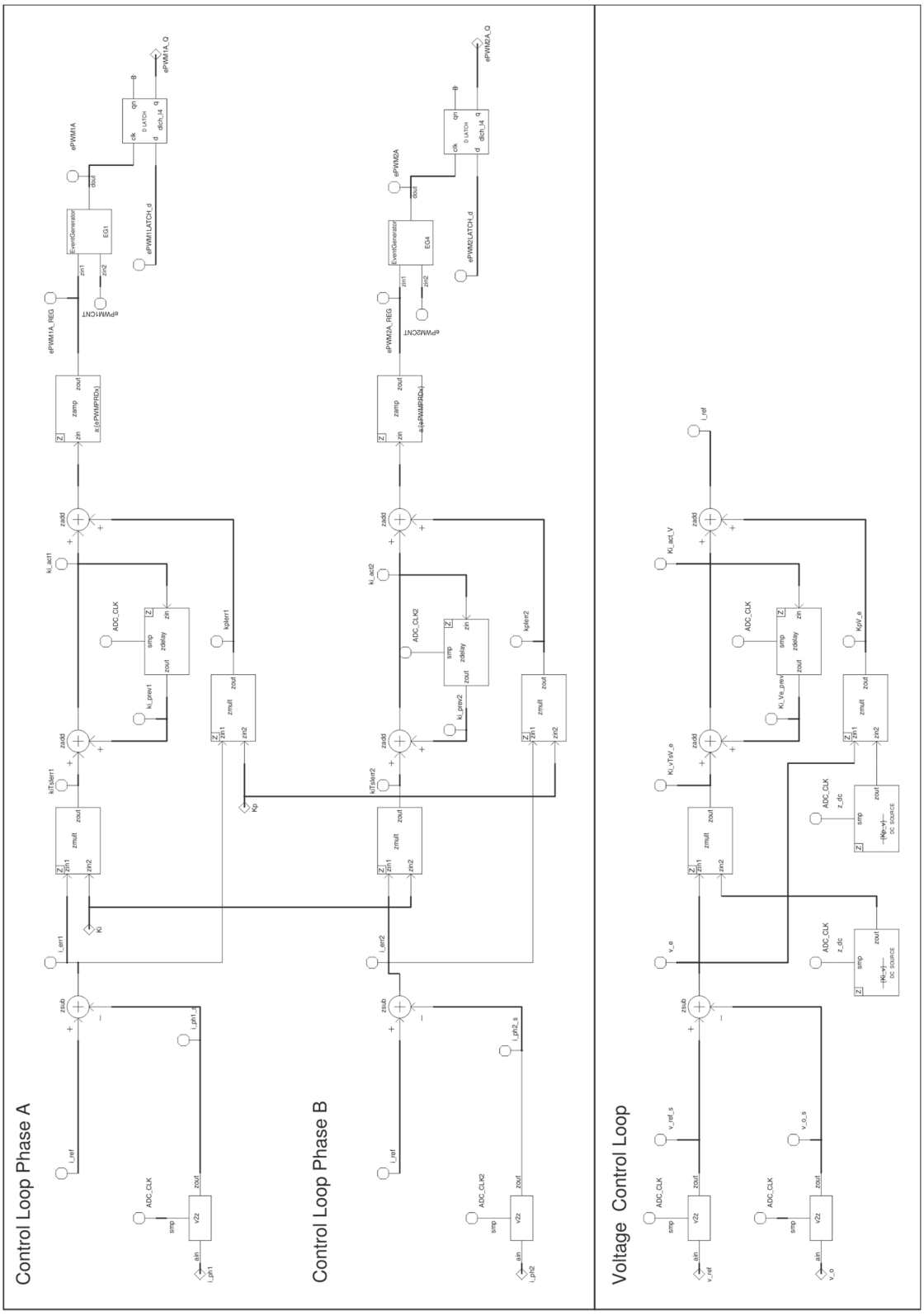


Figure C.9. SABER schematic diagram of the current and voltage control loops added to the DSC unit of Figure C.5.

Appendix D
Control implementation diagrams

In this appendix, the Simulink block diagrams employed to program the TMS320F28335 digital signal controller are shown and briefly explained.

D.1. Uniformly-sampled valley-current, peak-current and average-current control implementations

Figures D.1 and D.2 illustrate the hierarchical Simulink block diagrams that comprise the implementation of the control algorithms in the DSC. Figure D.1 groups the tasks that the DSC executes to initialize the system (System Start block, System Initialize block and Target preferences block), to enable/disable the DPWM modules operation (bottom left corner), and to handle the ADC interrupts (bottom right corner). Also, in this diagram it is possible to select the mode of operation of the gate drivers that interface the DSC with the interleaved converter prototype (upper right corner).

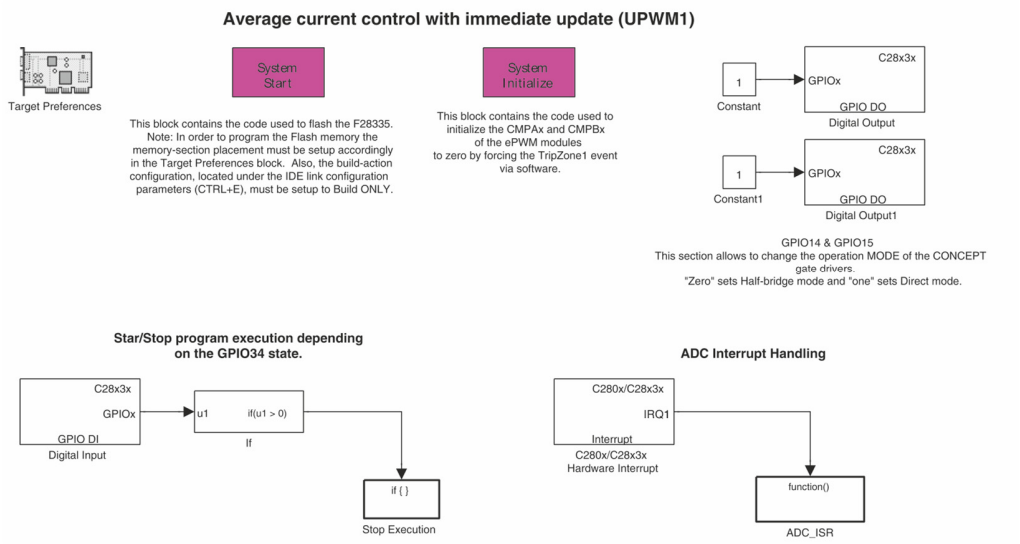


Figure D.1. Simulink diagram of the top-level tasks of the control algorithms.

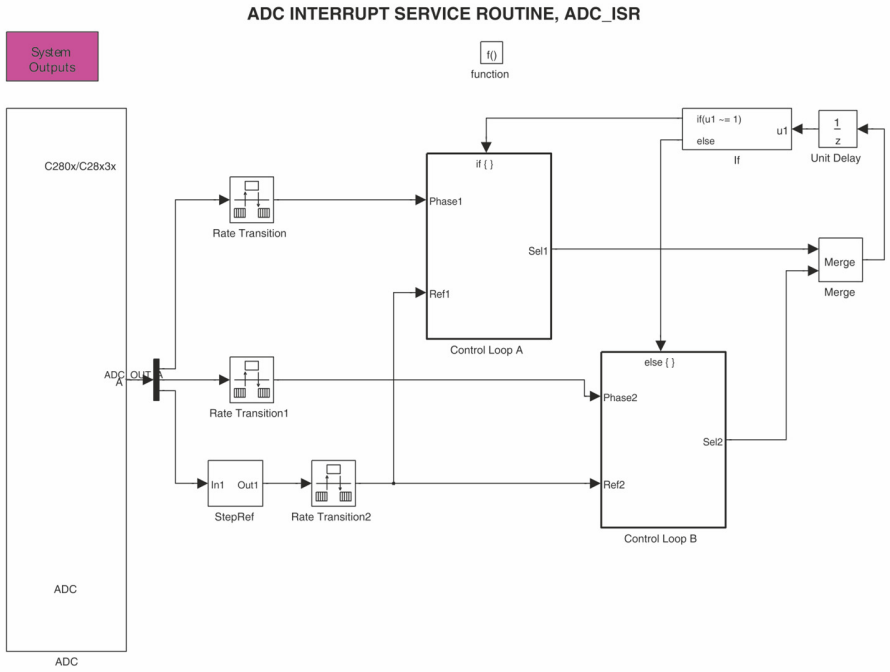


Figure D.2. Simulink diagram of the ADC interrupt service routine used for the normal DPWM update control algorithms.

Every time that the DSC is notified of an interrupt request from the ADC, the block diagram illustrated in Figure D.2(a) is executed. This section of the diagram performs the ADC interrupt service routine which reads the data acquired by the ADC (leftmost block), determines which control-loop has to be compensated (group of blocks at the rightmost side), and calculates new duty-ratio of the corresponding phase. The compensation of the control loops is executed by the blocks denoted Control loop A and Control loop B, which are respectively illustrated in Figure D.3. These sections of the algorithm are employed to scale the data read from the ADC, calculate the new duty-ratio of the corresponding phase, and to send the new duty-ratio to the registers of their corresponding DPWM modules. The block employed to scale the ADC data is shown in detail in Figure D.4.

Finally, the StepRef block which is connected to one of the output terminals of the ADC block, is employed to generate a step-increment or decrement in the reference-current of the control algorithms and is shown in detail in Figure D.5. The output of this block is connected to the control loop blocks.

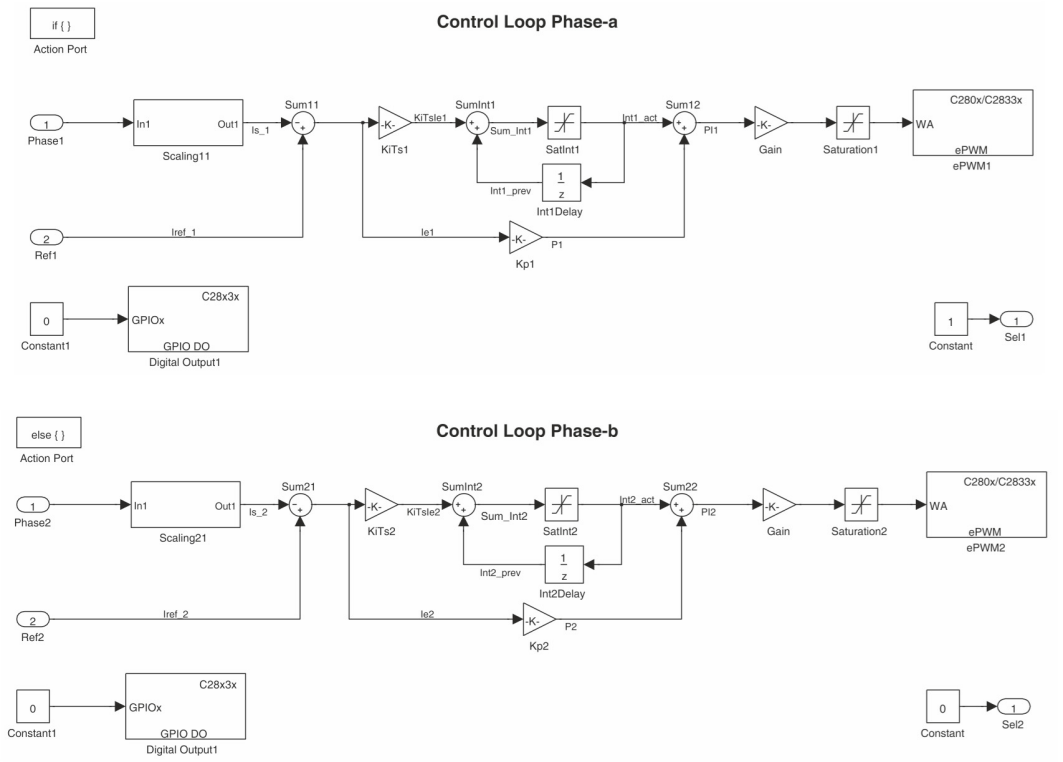


Figure D.3. Simulink diagrams of the current control-loops used for the normal DPWM update control algorithms.

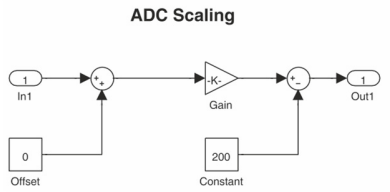


Figure D.4. Simulink diagram of the ADC scaling process.

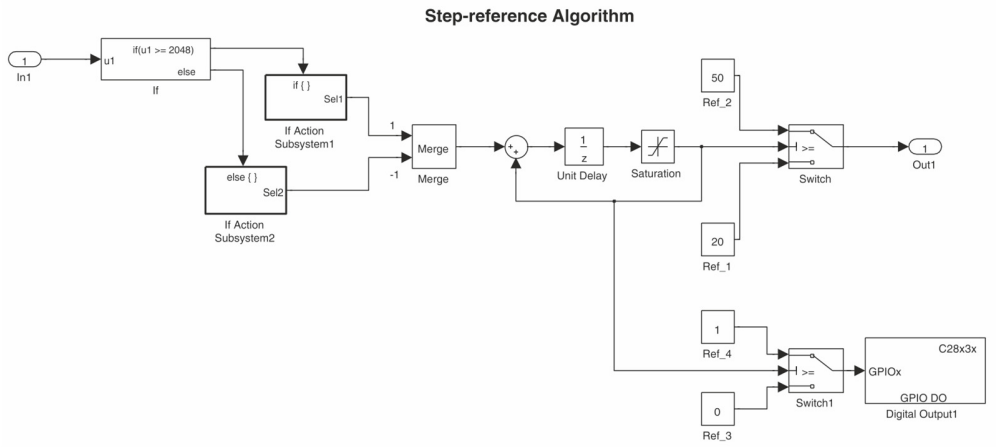


Figure D.5. Simulink diagram of the step-reference generator.

D.2. Uniformly-sampled average-current control with immediate DPWM update

Figures D.1 and D.6 illustrate the hierarchical Simulink block diagrams that comprise the implementation of the digital average-current control with immediate DPWM update in the DSC. Figure D.1 contains the tasks that the DSC executes to initialize the system, to enable/disable the DPWM modules operation, and to handle the ADC interrupts. This section of the block diagram is identical to the one employed for the control strategies with normal DPWM update shown in Appendix D.1.

Figure D.6 illustrates the section of the diagram that performs the ADC interrupt service routine. This diagram performs the ADC interrupt service routine which reads the data acquired by the ADC (leftmost block), determines which control-loop has to be compensated (group of blocks at the rightmost side), and calculates the new duty-ratio of the corresponding phase. The compensation of the control loops is executed by the blocks denoted Control loop A and Control loop B, which are respectively illustrated in Figure D.7. Compared to the control loop algorithms illustrated in Figure D.3, these control loops

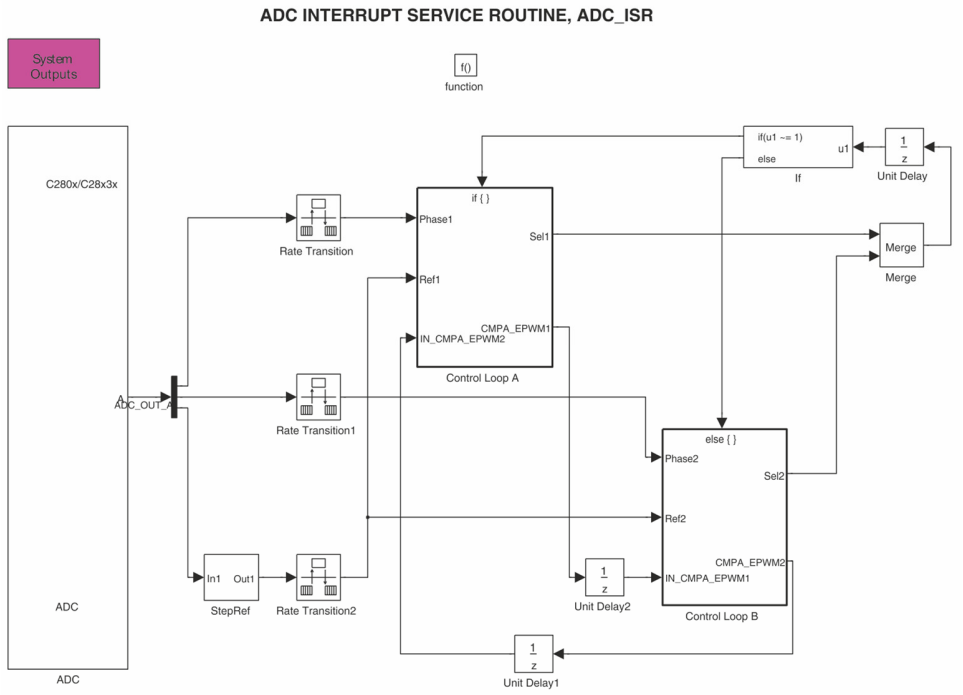


Figure D.6. Simulink diagram of the ADC interrupt service routine used for the immediate DPWM update control algorithm.

incorporate a building block called Anti-glitch, Figure D.8, which is used to avoid the issue described in Section 3.4.4, Chapter 3. The minimum duty-ratio constraint required to avoid the generation of spurious PWM waveforms, is implemented using the saturation blocks shown in the diagrams.

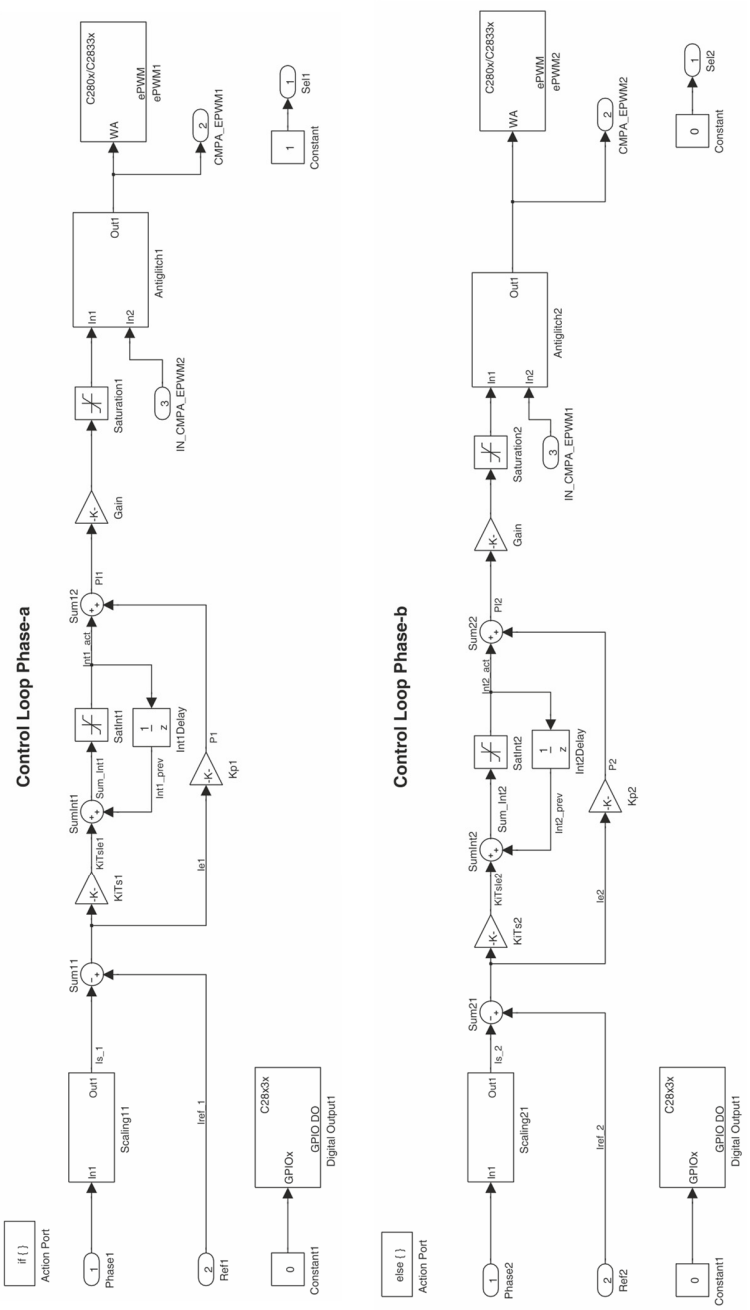


Figure D.7. Simulink diagrams of the current control-loops used for the immediate DPWM update control algorithm.

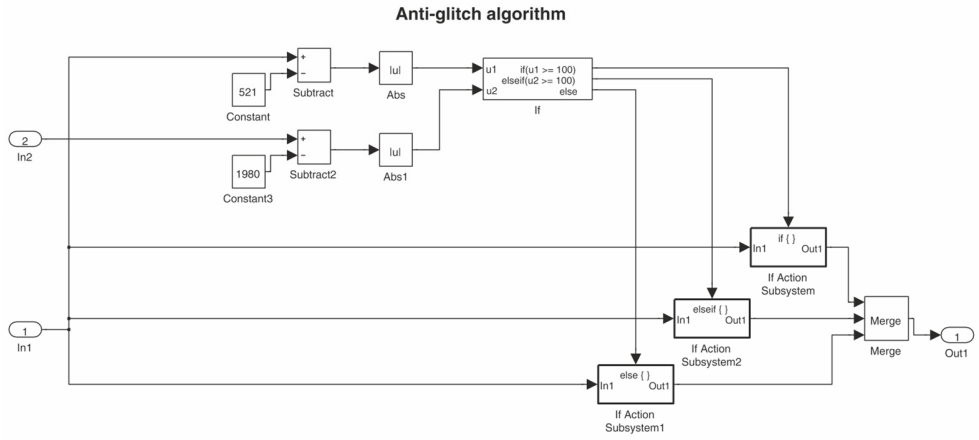


Figure D.8. Simulink diagram of the anti-glitch algorithm.

Appendix E
Simulation and experimental results

This appendix shows the simulation and experimental evidence of the stability-range plots presented in Figures 4.10 and 4.11 from Chapter 4, and the experimental results used to evaluate the converter performance PI compensator designed in Chapter 5 Section 5.4.1 (Figures 5.11 and 5.12).

Figures E.1 and E.2 present the simulation results obtained with the SABER averaged model when the system is operated with normal DPWM update mode, which supports the results shown in Figure 4.10(a). Similarly, Figures E.3 and E.4 present the simulation results obtained with the SABER averaged model when the system is operated with immediate DPWM update mode, which support the plot shown in Figure 4.10(b). The first plot of each figure shows the value of the proportional gain, K_p, and the integral gain, K_i, whilst the second plot shows the reference current, i_{ref}, and the sampled phase-a current, $i_a*(t)$.

The simulation was undertaken in three stages. First, the simulation was run until the system achieved stable steady-state operation. In the second stage, the proportional and integral gain values where changed for the values to be evaluated. Finally, *500 ns* after the second stage, a *5 %* step-increment was applied to the reference-current input. The system conditions can be found in the figure titles.

Figures E.5 and E.6 present the experimental results obtained when the system operates with normal DPWM update mode, which support the results of Figure 4.11(a). Similarly, Figures E.7 and E.8 show the experimental results obtained when the system operates with immediate DPWM update mode, which support the results of Figure 4.11(b).

In Figures E.5 to E.8 the first plot shows the transistor driving signal v_{1a}. However due to the size of the time scale and the amount of switching cycles, it is not possible to appreciate the waveforms on detail. The second plot, shows a PWM signal which was modulated using the proportional gain of the PI compensator. The purpose of this signal in these experiments was identify the value of the proportional gain that was being used during the experiments and to synchronize the scope to capture the evolution of the phase-a current when the proportional gain value was changed. Similar to the v_{1a} plot, due to the size of the time scale it is not possible to appreciate the details of this waveform. The third plot shows the phase-a current, i_a. Finally, the last plot illustrates the converter output voltage, v_o.

The procedure followed to obtain these results is similar to the one employed with the SABER simulator. First the converter was allowed to reach steady-state conditions using a combination of proportional and integral gains that allowed a stable operation of the system. Once the system reached steady-state operation, the proportional and integral gains were modified and the response of the phase-a current was captured. In some cases, despite that the oscillations of i_a were almost unnoticeable, the oscillation produced a constant audible noise.

Finally, Figure E.9 an E.10 show the experimental results obtained with the PI controller designed in Chapter 5, Section 5.4.1.

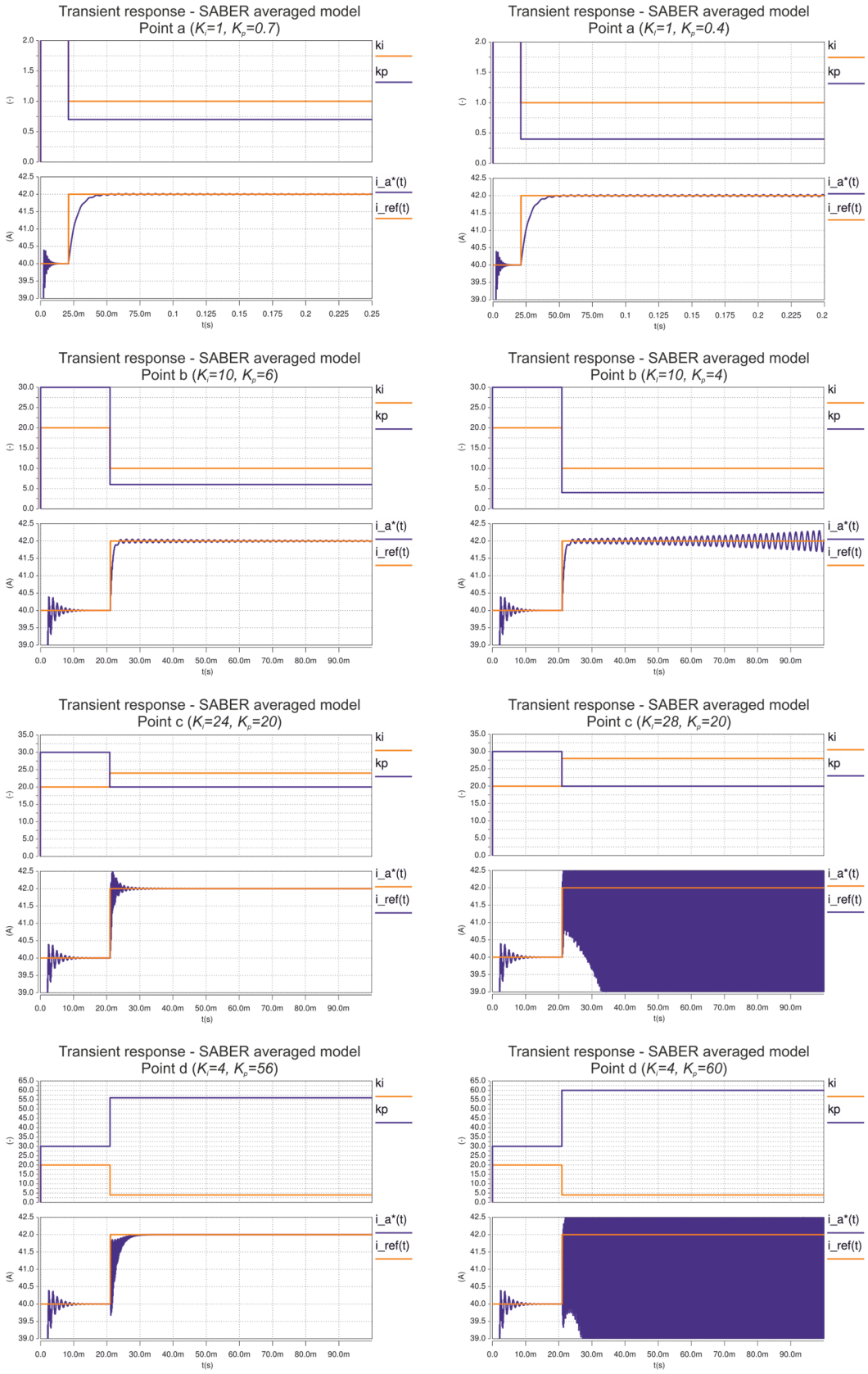


Figure E.1. Simulation results employed to validate the stability range predicted by the small-signal non-synchronous model illustrated in Figure 4.10, Chapter 4. Initial test conditions K_p = 30 K_i = 20. V_{in} = 85, R_{load} = 5.2 Ω, D = 0.5480.

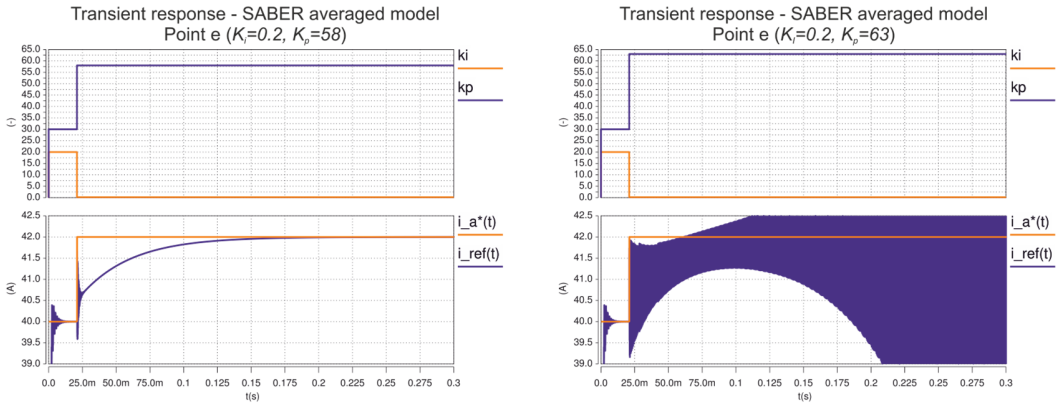


Figure E.2. Simulation results employed to validate the stability range predicted by the small-signal non-synchronous model illustrated in Figure 4.10, Chapter 4. Initial test conditions $K_p = 30$ $K_i = 20$. V_{in} = 85, R_{load} = 5.2 Ω, $D = 0.5480$.

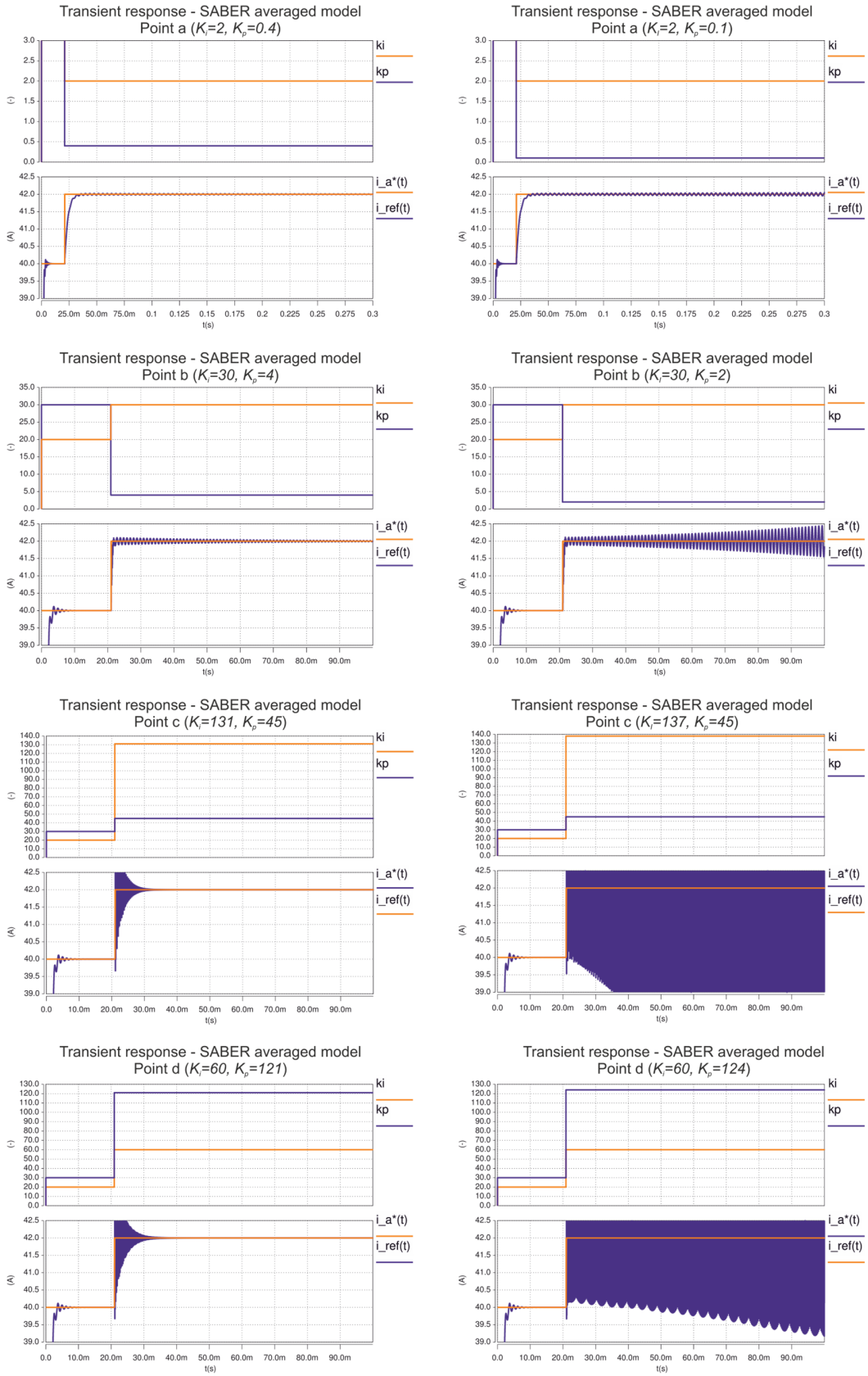


Figure E.3. Simulation results employed to validate the stability range predicted by the small-signal synchronous model illustrated in Figure 4.10, Chapter 4. Initial test conditions $K_p = 30$ $K_i = 20$. V_{in} = 85, R_{load} = 5.2 Ω, $D = 0.5480$.

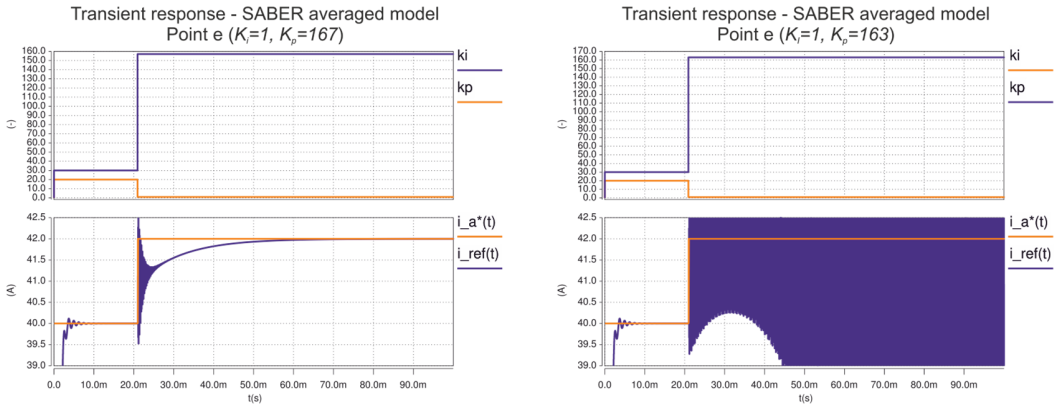


Figure E.4. Simulation results employed to validate the stability range predicted by the small-signal synchronous model illustrated in Figure 4.10, Chapter 4. Initial test conditions $K_p = 30$ $K_i = 20$. V_{in} = 85, R_{load} = 5.2 Ω, $D = 0.5480$.

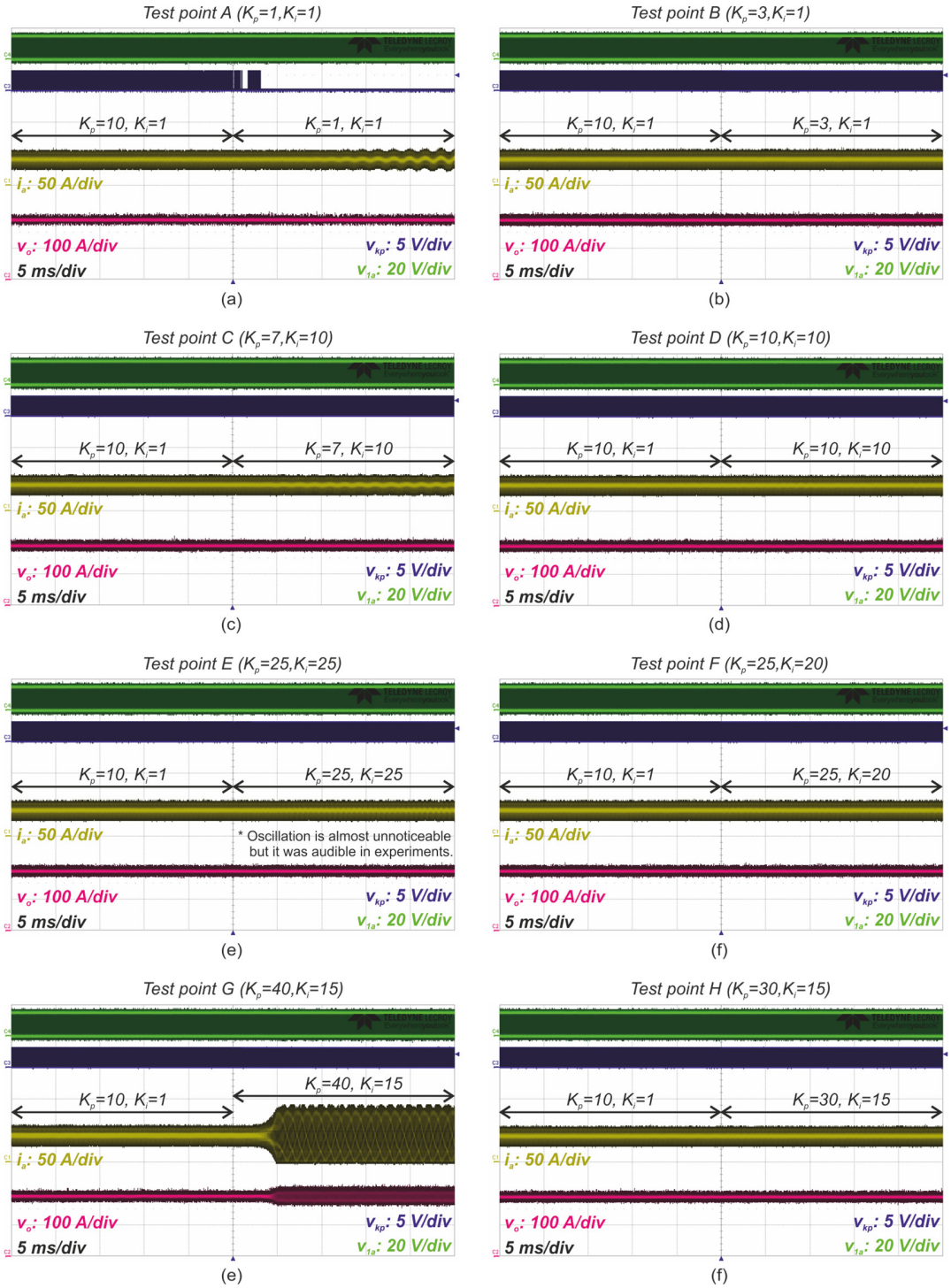


Figure E.5. Experimental results employed to validate the stability range predicted by the small-signal non-synchronous model with normal DPWM update mode found in Figure 4.11(a), Chapter 4. Initial test conditions $K_p = 10$ $K_i = 1$. V_{in} = 85, R_{load} = 5.2 Ω, $D = 0.5480$.

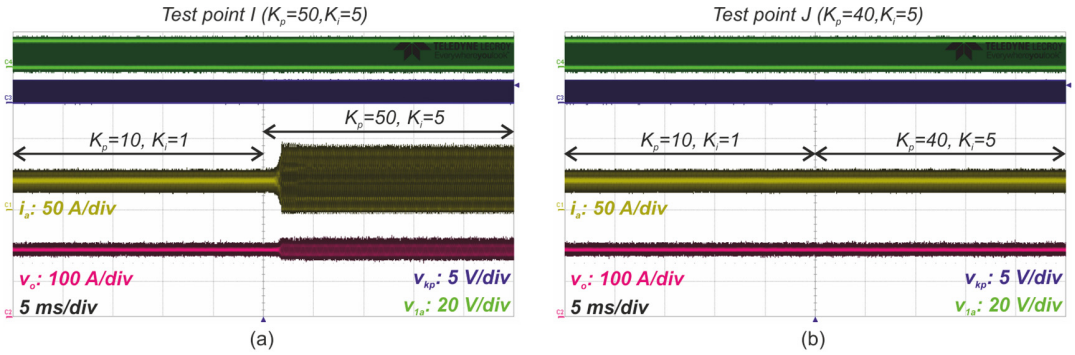


Figure E.6. Experimental results employed to validate the stability range predicted by the small-signal non-synchronous model with normal DPWM update mode found in Figure 4.11(a), Chapter 4. Initial test conditions $K_p = 10$ $K_i = 1$. V_{in} = 85, R_{load} = 5.2 Ω, $D = 0.5480$.

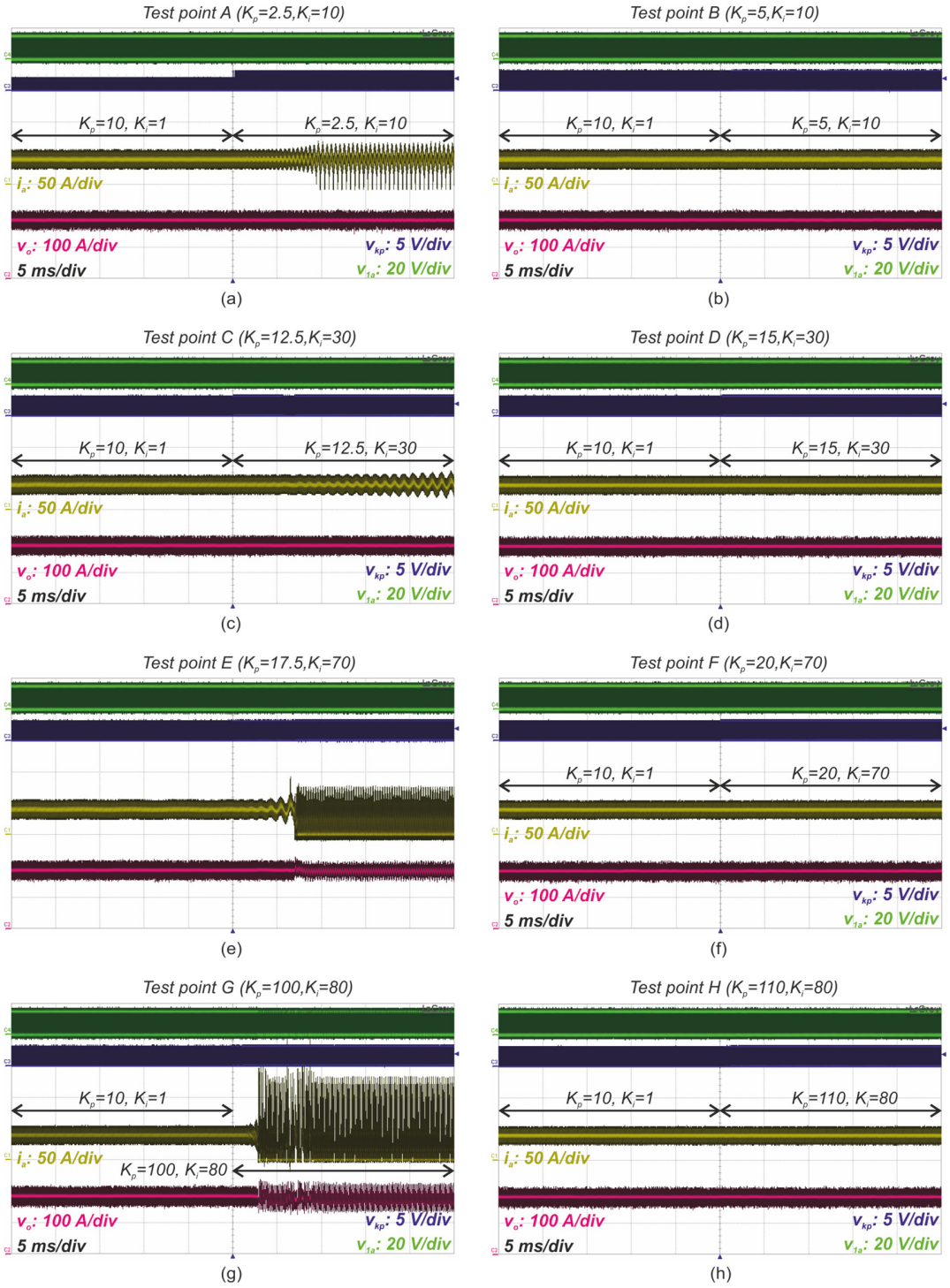


Figure E.7. Experimental results employed to validate the stability range predicted by the small-signal non-synchronous model with immediate DPWM update mode found in Figure 4.11(b), Chapter 4. Initial test conditions K_p = 10 K_i = 1. t_{d_proc} = (0.5)T, V_{in} = 85, R_{load} = 5.2 Ω, D = 0.5480.

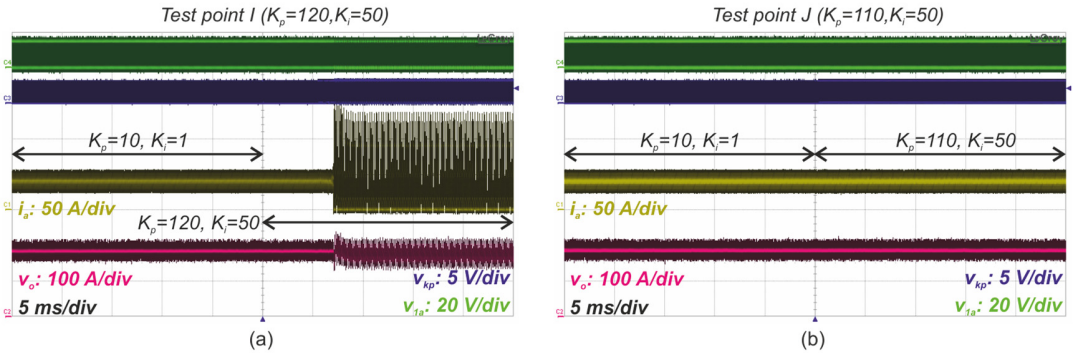


Figure E.8. Experimental results employed to validate the stability range predicted by the small-signal non-synchronous model with immediate DPWM update mode found in Figure 4.11(b), Chapter 4. Initial test conditions $K_p = 10$ $K_i = 1$. t_{d_proc} = (0.5)T, V_{in} = 85, R_{load} = 5.2 Ω, $D = 0.5480$.

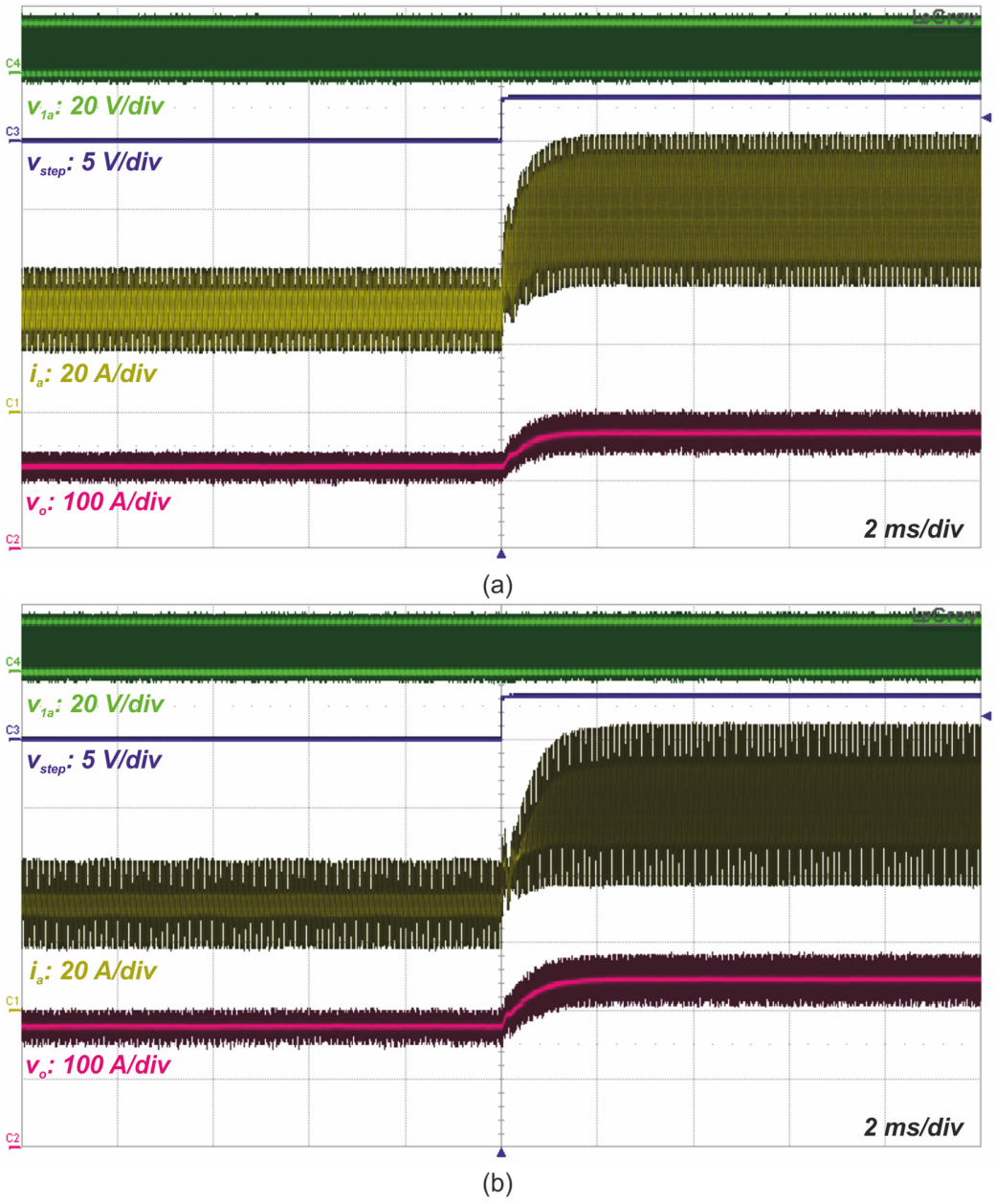


Figure E.9. Experimental results employed to validate PI design given in Chapter 5, Section 5.4. $K_p = 10T$ $K_i = 10$. $t_{d\_proc} = (0.12)T$, $R_{load} = 5.2\ \Omega$, $I_{ref1} = 30$ A, $I_{ref2} = 60$ A. (a) $V_{in} = 50$ V. (b) $V_{in} = 100$ V.

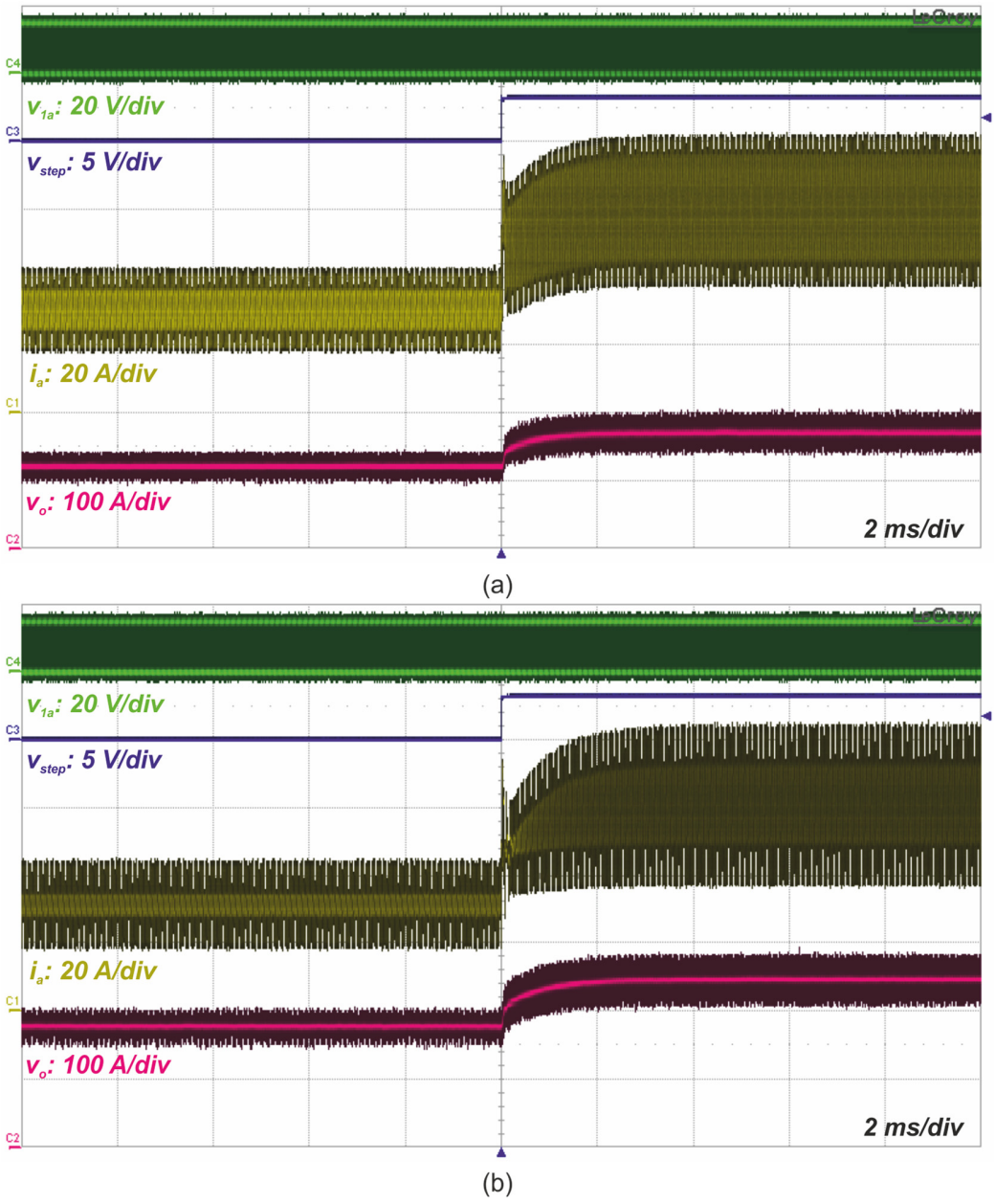


Figure E.10. Experimental results employed to validate PI design given in Chapter 5, Section 5.4. $K_p = 70T$ $K_i = 10$. $t_{d\_proc} = (0.12)T$, $R_{load} = 5.2\ \Omega$, $I_{ref1} = 30$ A, $I_{ref2} = 60$ A. (a) $V_{in} = 50$ V. (b) $V_{in} = 100$ V.

Appendix F
Control platform schematics

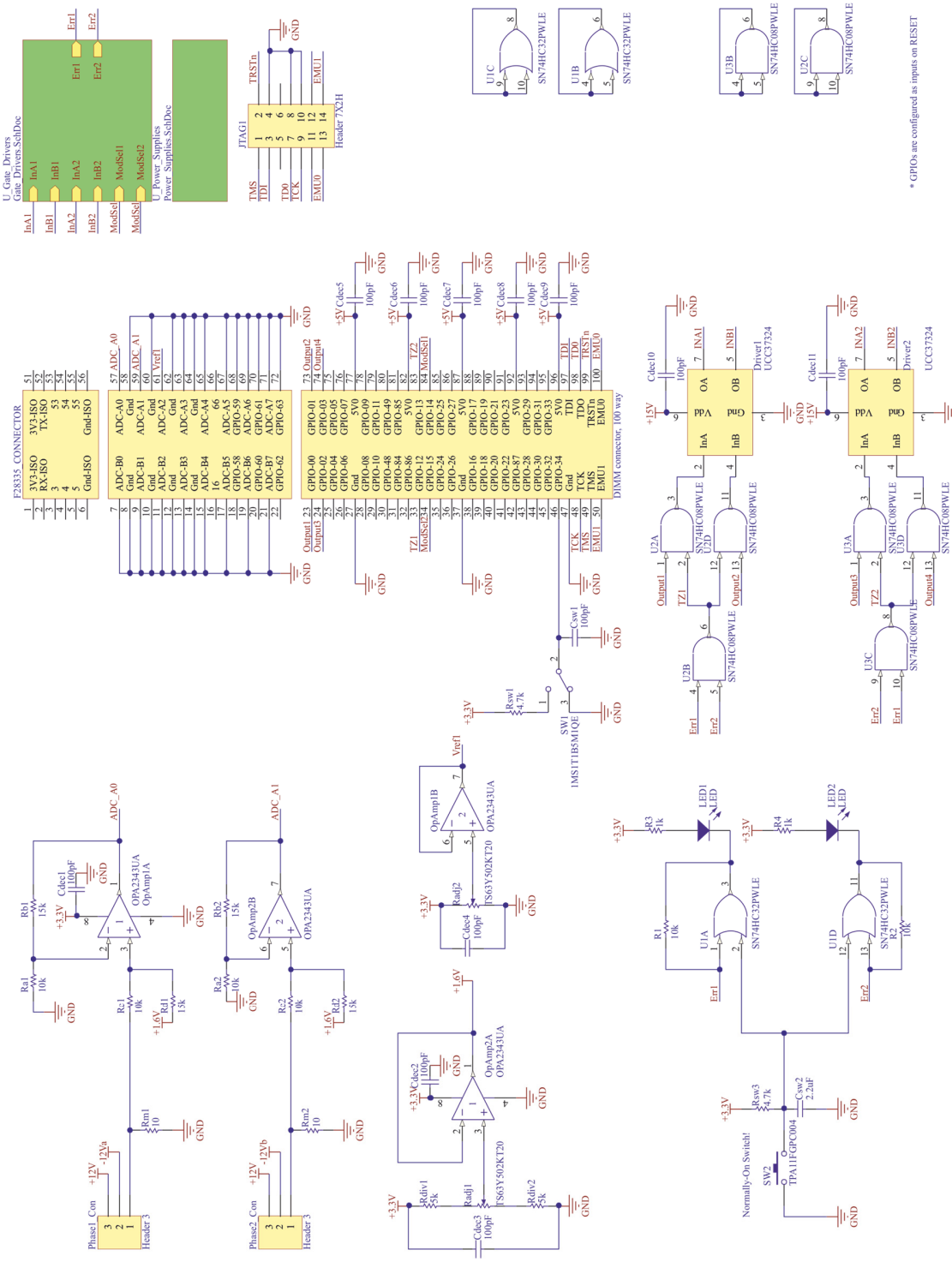


Figure F.1. Control platform schematics, scaling and conditioning stage.

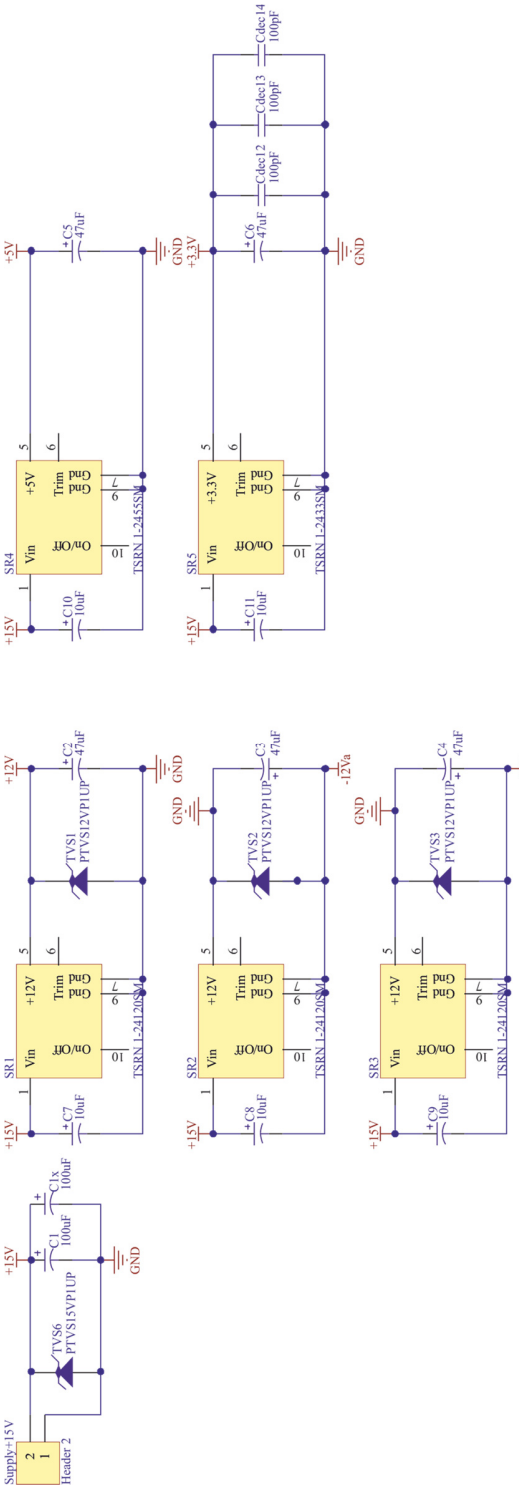
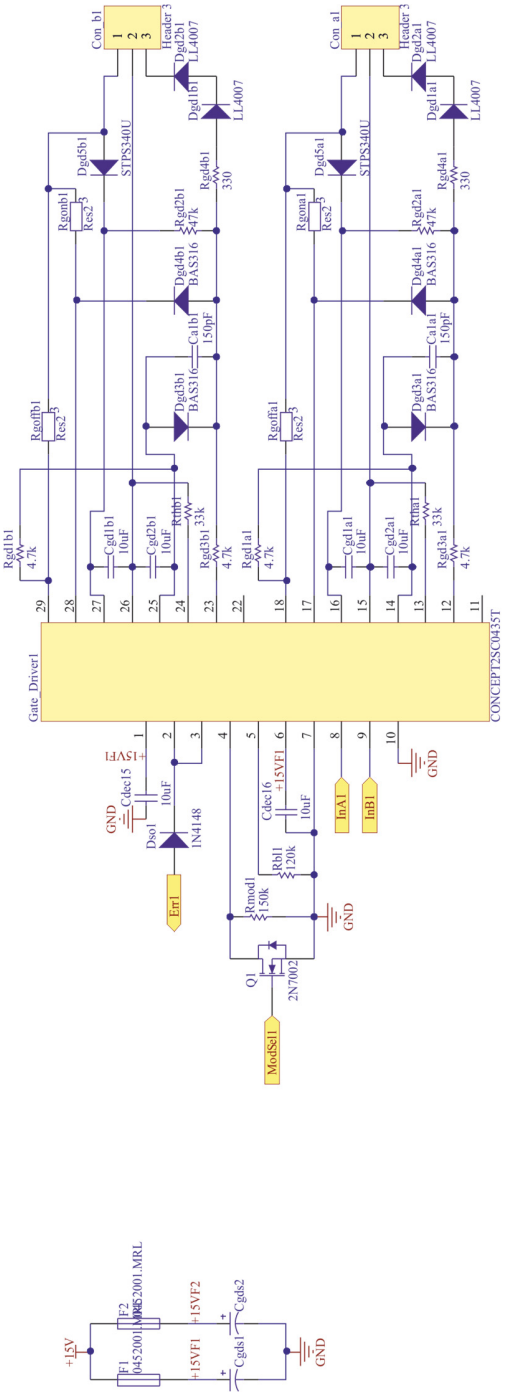


Figure F.2. Control platform schematics, power supplies.



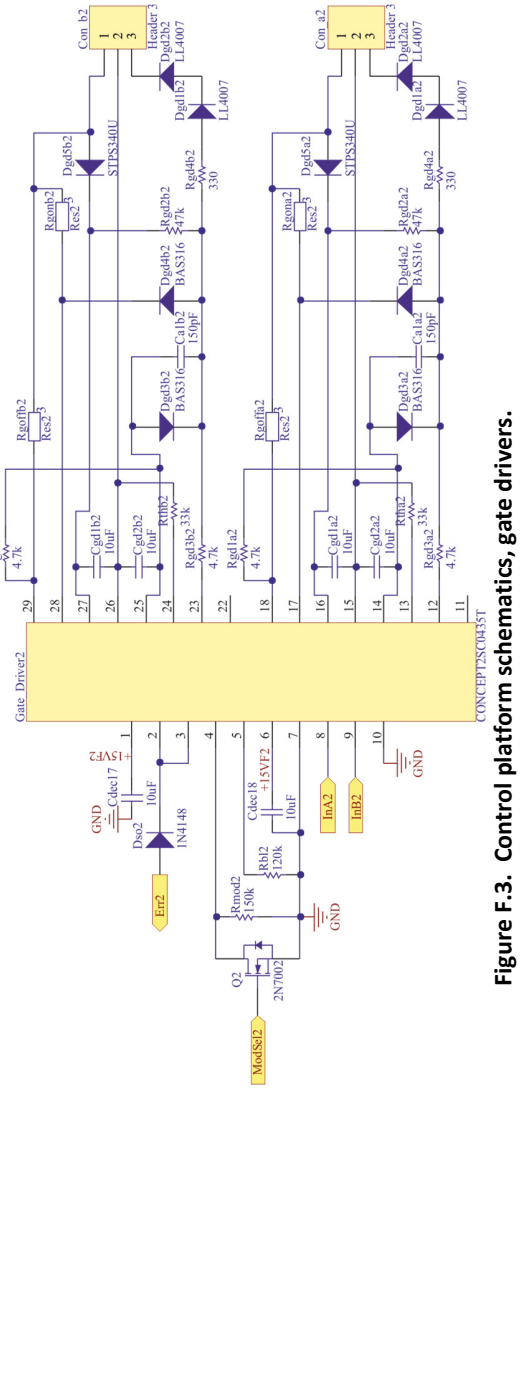


Figure F.3. Control platform schematics, gate drivers.