MODELLING AND DESIGN OF LOW NOISE AMPLIFIERS USING STRAINED InGaAs/InAlAs/InP pHEMT FOR THE SQUARE KILOMETRE ARRAY (SKA) APPLICATION

A thesis submitted to The University of Manchester for the degree of

Doctor of Philosophy

In the Faculty of Engineering and Physical Sciences

2012

NORHAWATI AHMAD

School of Electrical and Electronic Engineering

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES AND ILLUSTRATIONS

LIST OF ABBREVIATIONS

2DEG	Two-Dimensional Electron Gas
ADS	Advanced Design System
ASKAP	Australian SKA Pathfinder
ATA	Allen Telescope Array
CAD	Computer Aided Design
CMOS	Complementary Metal Oxide Semiconductor
CPW	Coplanar Waveguide
DC	Direct Current
HBT	Heterojunction Bipolar Transistor
HEMT	High Electron Mobility
ICCAP	Integrated Circuit Characterization and Analysis Program
IF	Intermediate Frequency
LNA	Low Noise Amplifier
MBE	Molecular Beam Epitaxy
MESFET	Metal Semiconductor Field Effect Transistor
MMIC	Monolithic Microwave Integrated Circuit
NF	Noise Figure
NF_{min}	Minimum Noise Figure

pHEMT	Pseudomorphic High Electron Mobility Transistor
PNA	General-purpose Network Analyser
RF	Radio Frequency
SKA	Square Kilometre Array
SOLT	Short-Open-Load-Thru
VLA	Very Large Array

ABSTRACT

The University of Manchester
Candidate: Norhawati Ahmad
Degree: Doctor of Philosophy (PhD)
Title: Modelling and design of Low Noise Amplifiers using strained InGaAs/ InAlAs/InP pHEMT for the Square Kilometre Array (SKA) application.
Date: 15th October 2012

The largest 21st century radio telescope, the Square Kilometre Array (SKA) is now being planned, and the first phase of construction is estimated to commence in the year 2016. Phased array technology, the key feature of the SKA, requires the use of a tremendous number of receivers, estimated at approximately 37 million. Therefore, in the context of this project, the Low Noise Amplifier (LNA) located at the front end of the receiver chain remains the critical block. The demanding specifications in terms of bandwidth, low power consumption, low cost and low noise characteristics make the LNA topologies and their design methodologies one of the most challenging tasks for the realisation of the SKA. The LNA design is a compromise between the topology selection, wideband matching for a low noise figure, low power consumption and linearity. Considering these critical issues, this thesis describes the procedure for designing a monolithic microwave integrated circuit (MMIC) LNA for operation in the mid frequency band (400 MHz to 1.4 GHz) of the SKA.

The main focus of this work is to investigate the potential of MMIC LNA designs based on a novel InGaAs/InAlAs/InP pHEMT developed for 1 μm gate length transistors, fabricated at The University of Manchester. An accurate technique for the extraction of empirical linear and nonlinear models for the fabricated active devices has been developed. In addition to the linear and nonlinear model of the transistors, precise models for passive devices have also been obtained and incorporated in the design of the amplifiers. The models show excellent agreement between measured and modelled DC and RF data.

These models have been used in designing single, double and differential stage MMIC LNAs. The LNAs were designed for a 50 Ω input and output impedance. The excellent fits between the measured and modelled S-parameters for single and double stage single-ended LNAs reflects the accurate models that have been developed. The single stage LNA achieved a gain ranging from 9 to 13 dB over the band of operation. The gain was increased between 27 dB and 36 dB for the double stage and differential LNA designs. The measured noise figures obtained were higher by ~0.3 to ~0.8 dB when compared to the simulated figures. This is due to several factors which are discussed in this thesis.

The single stage design consumes only a third of the power (47 mW) of that required for the double stage design, when driven from a 3 V supply. All designs were unconditionally stable. The chip sizes of the fabricated MMIC LNAs were 1.5 x 1.5 mm^2 and 1.6 x 2.5 mm^2 for the single and double stage designs respectively. Significantly, a series of differential input to single-ended output LNAs became of interest for use in the Square Kilometre Array (SKA), as it utilises differential output antennas in some of its configurations. The single-ended output is preferable for interfacing to the subsequent stages in the analogue chain. A noise figure of less than 0.9 dB with a power consumption of 180 mW is expected for these designs.

DECLARATION

No portion of the work referred to in the thesis has been submitted in support of an application for another degree or qualification of this or any other university or other institute of learning.

COPYRIGHT STATEMENT

1. The author of this thesis (including any appendices and/or schedules to this thesis) owns certain copyright or related rights in it (the "Copyright") and s/he has given The University of Manchester certain rights to use such Copyright, including for administrative purposes.

2. Copies of this thesis, either in full or in extracts and whether in hard or electronic copy, may be made only in accordance with the Copyright, Designs and Patents Act 1988 (as amended) and regulations issued under it or, where appropriate, in accordance with licensing agreements which the University has from time to time. This page must form part of any such copies made.

3. The ownership of certain Copyright, patents, designs, trademarks and other intellectual property (the "Intellectual Property") and any reproductions of copyright works in the thesis, for example graphs and tables("Reproductions"), which may be described in this thesis, may not be owned by the author and may be owned by third parties. Such Intellectual Property and Reproductions cannot and must not be made available for use without the prior written permission of the owner(s) of the relevant Intellectual Property and/or Reproductions.

4. Further information on the conditions under which disclosure, publication and commercialisation of this thesis, the Copyright and any Intellectual Property and/or Reproductions described in it may take place is available in the University IP Policy (see http://www.campus.manchester.ac.uk/-medialibrary/policies/intellectualproperty.pdf), in any relevant Thesis restriction declarations deposited in the University Library, The University Library's regulations (see http://www.manchester.ac.uk/library/aboutus-/regulations) and in The University's policy on presentation of Theses.

ACKNOWLEDGEMENTS

First and foremost, all praise is due to *Allah* the giver of all knowledge.

I would like to express my very great appreciation to my supervisor, Professor Mohamed Missous, for his enthusiastic encouragement and patient guidance. I would like to offer my special thanks to Dr. James Sexton for his extensive knowledge sharing, comments and ideas throughout the years.

I have furthermore to thank Dr. Shahzad Arshad and Dr. Boume Boudjelida for their guidance in operating the necessary equipment, and for useful discussions. I also would like to acknowledge Professor Eduardo Artal and his team from the University of Cantabria, Spain for their great help in the noise and S-parameter measurement.

I am much indebted to my beloved husband, Mr. Muammar Mohamed Isa who is also my research group member, for his support, encouragement, care and understanding. He has always been beside me to motivate me in my difficult moments. I doubt that I will ever be able to convey my appreciation fully, but I owe him my eternal gratitude. A special thanks to my wonderful children, Kaiyisah Anati and Safiyyah Anati whom, in their own ways, inspired me to complete this work.

This thesis would not have been possible without the financial support from my sponsors, the Ministry of Higher Education Malaysia and Universiti Malaysia Perlis (UniMAP).

Finally, this project would not be successful without the kind support and help of many more individuals and organisations. I would like to extend my sincere thanks to all of them.

PUBLICATIONS

1. **N. Ahmad**, M. Mohamad Isa and M. Missous, "Modelling, Design and Testing of novel InGaAs-InAlAs Low Noise Amplifier for Radio Astronomy applications'', in UK Semiconductor 2012 Conference, The University of Sheffield, 4-5 July 2012

2. **N. Ahmad**, M. Mohamad Isa and M. Missous "Modelling and Design of MMIC Low Noise Amplifier using an in-house InP-based Process", Postgraduate Poster Conference and Industrial Advisory Group Meeting, The University of Manchester, 30 Nov 2011

3. **N. Ahmad**, J. Sexton, Yan Lai and M. Missous, "Single and Double Stage MIC Low Noise Amplifiers for MUST Project", in UK Semiconductor 2011 Conference, The University of Sheffield, 6-7 July 2011

4. M. Mohamad Isa, **N. Ahmad**, M. Missous, Y. Lai, J. Sexton, and S. Boulay, "Fabrication of Low Noise InAlAs-InGaAs pHEMT for SKA application (300MHz to 2GHz)", in IMiEJS 2011 Conference, Athlone Institute of Technology (AIT), Ireland, 9-11 June 2011

5. **N. Ahmad**, S. Arshad and M. Missous, "New InP Based pHEMT Double Stage Differential to Single-ended MMIC Low Noise Amplifiers for SKA", in 8th International Conference on Advanced Semiconductor Devices & Microsystems, Smolenice, Slovakia, 25-27 October 2010, pages 305-308, IEEE: 10.1109/ASDAM.2010.56666366

6. **N. Ahmad**, S.Arshad and M. Missous, "New InP pHEMT Based Single ended and differential to single-ended MMIC Low Noise Amplifiers for SKA", in UK Semiconductor 2010 Conference, The University of Sheffield, 7-8 July 2010

7. S. Boulay, B. Boudjelida, S. Arshad, **N. Ahmad** and M. Missous, "Low Frequency Broadband InGaAs/InAlAs Low Noise Amplifiers for SKA", in

Wide Field Astronomy & Technology for the Square Kilometre Array, Chateau de Limelette, Belgium, 4-6 November 2009, p. 299

8. S. Arshad, B. Boudjelida, S. Boulay, **N. Ahmad** and M. Missous, "Sub-0.6 dB NF Low Power Differential to Single-Ended MMIC LNA Designs for the SKA using InGaAs/InAlAs/InP pHEMTs", in Wide Field Astronomy & Technology for the Square Kilometre Array, Chateau de Limelette, Belgium, 4-6 November 2009, p. 295

9. **N. Ahmad**, S. Arshad, B. Boudjelida, S. Boulay and M. Missous, "Wide-band Hybrid Single-Ended and Differential LNA Designs Using GaAs pHEMTs and Comparison with In-house InP pHEMT Based LNA Design", in Wide Field Astronomy & Technology for the Square Kilometre Array, Chateau de Limelette, Belgium, 4-6 November 2009, p. 287

CHAPTER 1

INTRODUCTION

1.1 INTRODUCTION

Astronomers continue to explore the universe learning about its amazing history, discovering the richness of its contents, and understanding the physical processes that take place in this astoundingly diverse environment. Today, astronomy expands knowledge, inspiring new generations to understand how the universe and how stars first came into being, life beyond the Earth or even the natural forces that control our universal destiny.

''We have explored the cosmos, not just by observing through the tiny visible window used by our eyes, but also by exploiting the entire electromagnetic spectrum, from radio waves with wavelengths larger than a house to gamma rays with wavelengths 1,000 times smaller than a proton. The universe has also been studied by using samples returned to Earth from comets and meteorites, and by detecting and analyzing high-energy particles that permeate space.'' Panel Reports—New Worlds, New Horizons in Astronomy and Astrophysics National Research Council, USA, 2010.

To the naked eye, the universe appears static, apart from the twinkling of starlight caused by the Earth's atmosphere. In fact, it is a place where dramatic events occur on timescales from a tiny fraction of a second to days or centuries. These dramatic discoveries came about through the application of modern technology and human desire to observe the sky. This thirst for knowledge resulted in a number of very large radio telescopes being built,, such as the Giant Metrewave Radio Telescope (GMRT) with parabolic dishes of 45 m diameter (total 30 dishes), spread over a distance of up to 25 km, and the Allen Telescope Array (ATA) which currently has 42 dishes, with the aim to expand to 350 dishes. To date, the world's largest and most sensitive radio telescope, the Square Kilometre Array (SKA), is already being planned [1].

"We are on the verge of confirming some of the most revolutionary theories of the last century and we need big machines to do that!" Michael Kramer, Director at the Max Planck Institute for Radio Astronomy.

1.2 RADIO TELESCOPES

The telescope was first introduced in 1609 by the great Italian scientist Galileo Galilei. He became the first man to discover sunspots, the four large moons of Jupiter, and the rings of Saturn [2]. Galileo's telescope was an arrangement of two glass lenses to magnify objects. In 1704, Sir Issac Newton announced a new concept in telescope design, whereby instead of glass lenses, a curved mirror could be used to gather light and reflect it back to a focal point. The reflector telescope that Newton designed opened the door to the magnification of objects millions of times, far beyond what could ever be achieved with a lens [3].

Radio telescopes have come a long way since 1937 when Grote Reber built the first one in his backyard. Reber built a telescope with a dish in the shape of a parabola [4]. Because radio waves are so large, about 100,000 times longer than visible light, astronomers therefore require a substantial telescope to collect them. In addition, radio telescopes require a large surface area so that they can capture more of the radio frequency radiation reaching the Earth. Building a single large telescope is not feasible, hence radio astronomers concentrate their efforts into building array instruments. Arrays are a series of smaller telescopes that work together as one large telescope. In 1980, the very large array (VLA) was built, which consisted of 27 radio telescopes.

In a radio telescope array, the further apart the individual dishes are, the greater is the resolution, or the ability to distinguish between two closer objects. However, when the individual dishes are placed closer together, the telescope array can obtain more information about celestial object characteristics such as their brightness and temperature. These concepts were applied to the building of future radio telescopes. The Australian Square Kilometre Array Pathfinder (ASKAP) is currently under construction and will be an important test bench for the Square Kilometre Array

(SKA). Figure 1-1 illustrates the development of telescopes and Table 1-1 summaries the specifications of current and planned radio telescope arrays

(a) Galileo Galilei's telescope, 1906

(b) Sir Issac Newton's telescope, 1704

(c) The VLA radio telescope, 1980

(d) The ATA radio telescope, under construction

(e) The ASKAP radio telescope, under construction

Figure 1-1 Pictures showing the development of telescopes.

Table 1-1 Table of specifications of current and planned radio telescope arrays

Radio Telescope	Very Large Array (VLA)	Allen Telescope Array (ATA)	Australian SKA Pathfinder (ASKAP)	Square Kilometre Array (SKA)
Bandwidth (GHz)	0.07-50	0.5-11	0.7-1.8	0.4-10
Number of Reflectors	27	350	36	~3000
Reflectors Diameters (m)	25	6	12	~15
Receiver Elements	54	700	~10 000	>10 000
Number of LNAs	54	700	~10 000	>10 000
Location	New Mexico, USA	Northeast San Francisco, California	Mid West, Western Australia	South Africa or Australia
Operation	1980	Under construction	Under construction	Under Planning

1.2.1 The Square Kilometre Array (SKA)

The Square Kilometre Array (SKA) will create a telescope with an effective collecting area equivalent to one square kilometre [5]. The SKA offers 50 times greater sensitivity and 100 times improvement in resolution over any other radio telescope array to date. Partners from 20 countries are involved in the ~ £1.3 billion project which is expected to be completed in 2024. The timeline for the SKA project is shown in Table 1-2. Competition to host the array was intense, and has been narrowed down to two strong sites in Western Australia and in the Northern Cape of South Africa. Both sites will now host the SKA.

Table 1-2 The timeline of the SKA project [6]

Timeline	
2024	Full operation
2019	First astronomical observations
2016	Initial construction
2013-15	Details designs and production engineering
2012-13	Site selection, funding approval for initial (10% SKA) construction, establish SKA organisation
2008-12	System design and costing
2006	Short listing of suitable site
1991	SKA concept

Three types of antennas will be used to provide continuous frequency coverage from 70 MHz to 10 GHz: 1) high-frequency dishes (1.2 to 10 GHz), 2) mid frequency (0.4 to 1.4 GHz), and 3) low frequency (70 to 450 MHz) aperture arrays. The antennas that cover these three regions are shown in Figure 1-2.

The sensitivity for each frequency range is shown in Figure 1-3 and is improved by increasing the relative collection area. To increase the collection area, the number of observation points needs to be increased. The phased array technique in the SKA uses multiple receivers to increase the number of observation points. The number of observation points can also be increased by enhancing the angular resolution using a radio telescope array with a large baseline, up to several hundred kilometres in length [7]. The sensitivity can also be increased by using an antenna array which has a large number of small collectors [8].

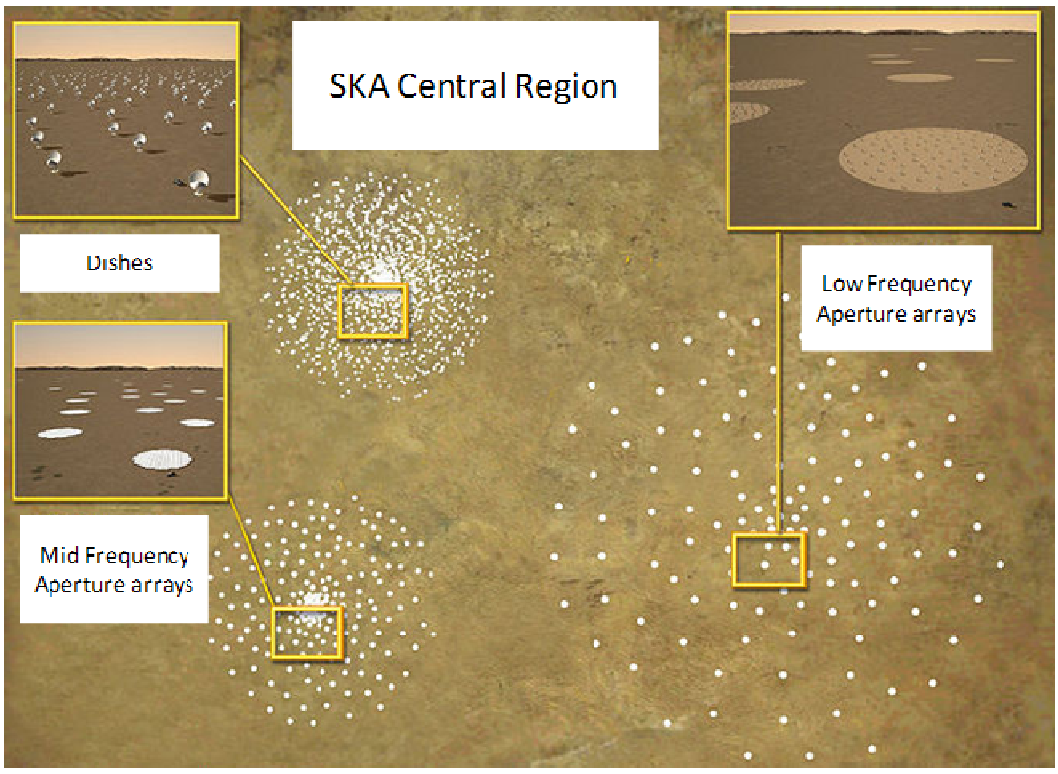


Figure 1-2 Picture of the central region of the SKA [9]

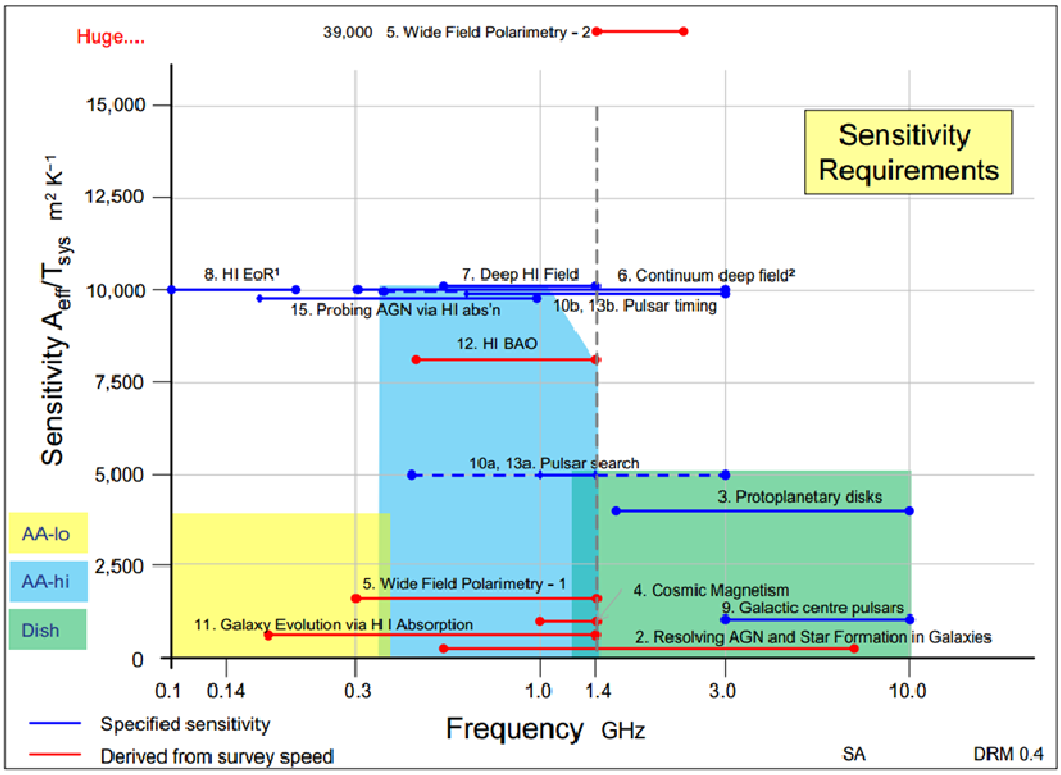


Figure 1-3 The Sensitivity of the SKA Radio Telescope [8]

1.3 LOW NOISE AMPLIFIER (LNA) TECHNOLOGY

The SKA project features phased array technology and will ultimately use a very large numbers of receivers, estimates are in the order of 250 x 150 000 (~37 million) LNAs in the 0.4 - 1.4 GHz mid frequency band [8]. This large number of receiving elements requires close attention to its cost to ensure the financial budget is kept under control. For this reason, the technology developed for the LNA is being assessed at room temperature, but inexpensive temperature control can also be used to improve uniformity and the noise temperature when needed.

According to Haus and Adler [10], it is impossible for any LNA to have a noise figure lower than that of the minimum noise figure of the best transistor inside the LNA. Therefore, to achieve the noise figure close to the device's minimum possible noise figure, not only a very low noise device an important factor, but an accurate model, biasing technique and circuit topology is also crucial. These requirements are explained and discussed in detail in subsequent chapters of this thesis.

Several different technologies, design topologies and noise measurement techniques of LNAs for the SKA have been proposed and analysed since the commencement of the project in 2000. Transistor technologies including GaAs mHEMT, GaAs pHEMT, SiGe HBT, InP pHEMT and CMOS have all been extensively studied and characterised at multiple institutes around the world [11]. The ability to scale down CMOS transistor size and produce f_{max} exceeding 200 GHz makes it a realistic alternative to III-V materials like GaAs and InP pHEMTs for some applications, but it has drawbacks and limitations at low frequencies [12].

In this project, a novel InP-based pHEMT technology was used to develop an LNA to operate between 0.4–1.4 GHz, and which was capable of meeting the mid frequency performance requirements of the SKA. Crucial to achieving this, the complete workflow is available at the University of Manchester, from material growth to circuit measurement, as shown in Figure 1-4.

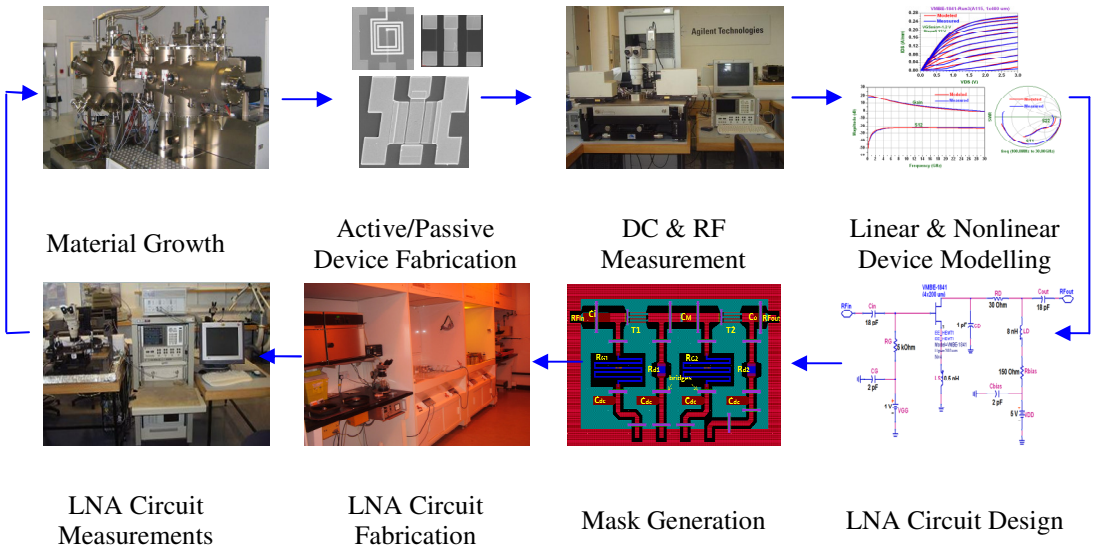


Figure 1-4 The complete workflow process at the University of Manchester

1.4 SCOPE OF THE THESIS

This thesis presents the development of low noise amplifier (LNA) designs using a new InP pHEMT technology to fulfil the requirements of the mid frequency (0.4-1.4 GHz) band of the Square Kilometre Array (SKA). The transistor used in this project employs a 1 µm gate length with multiple sized gate widths. The transistors were fabricated at the University of Manchester. The measurement of the transistors and the LNAs were carried out at room temperature. Therefore, no comparison could be made with other research at cryogenic temperatures. The proposed design is a Monolithic Microwave Integrated Circuit (MMIC) that combine high performance with low cost and avoids expensive and labour intensive external components (especially discrete inductors used for the input of the LNA).

1.5 STRUCTURE OF THE THESIS

Chapter 2 deals with pHEMT theory and the relevant semiconductor band structure background to this device. The history of the conventional pHEMT epitaxial structure is also discussed followed by discussion of the emergence of the pHEMT in the marketplace.

Chapter 3 discusses the conceptual understanding of two-port networks, where theoretical approaches are applied in the analysis of low noise amplifier performance. Figures of merit for the design such as noise, gain and stability are also included and analysed. The Scattering parameter technique is employed throughout the discussions for a thorough understanding of low noise circuits.

After a brief introduction to the selected device and its figures of merit used in this research, the thesis is then divided into two main sections: device modelling and LNA design and measurement.

The device modelling is discussed in ***Chapter 4*** and ***Chapter 5. Chapter 4*** highlights the theoretical background of HEMT device modelling. The discussion in ***Chapter 5*** concentrates on the device models used in this research. The details of ***Chapter 4*** and ***Chapter 5*** are as follows:

Chapter 4 addresses the necessary concepts for the development of empirical models of HEMT devices, which contribute to successful low noise amplifier design. The chapter begins with a discussion of biasing conditions and the correct selection for low noise application. These bias conditions are then introduced into the transistor linear model, followed by the nonlinear model. The chapter continues with a literature review of previously developed transistor noise models. The most appropriate model was then selected to model the noise of the in-house fabricated transistors.

Chapter 5 discusses the device modelling steps based on the empirical model derived in Chapter 4. The differences in the model between various device sizes from three different epitaxial layers are also presented in this chapter. The agreements between the modelled and measured parameters discussed in this chapter are then compared and analysed. At the end of the chapter, comprehensive studies on the device's noise characteristics are presented. The results of this provided guidance to the author in selecting the right device for the LNA circuit design.

The LNA theoretical concepts are discussed in ***Chapter 6*** and the designs are detailed in ***Chapter 7*** and ***Chapter 8***. The contents of each chapter are as follows:

Chapter 6 is used to examine the requirements of a complete system design. The chapter commences with a discussion of the Monolithic Microwave Integrated Circuit (MMIC). The specifications of the system design are then addressed, before the active device is selected. LNA theory is then explained and the performance compromises that arise in the design of circuit topologies, biasing networks and matching configurations are discussed.

Chapter 7 presents the design and analysis of the single input single-ended output, single and double stage LNAs, using all of the criteria discussed in Chapters 6. The LNAs are designed to match a 50 Ω input and output impedance. The measured and simulated S-parameters of the LNA are compared and analysed. The fabricated LNAs show excellent agreement with the simulations.

Chapter 8 demonstrates the improvement in the noise performance obtained via the differential to single-ended MMIC LNA. Several designs are proposed and analysed, to explore the effect of topology on noise and gain, and on the system as a whole.

Finally, ***Chapter 9*** summarises the work discussed in the earlier chapters and suggests some potential future research to further extend the work described in this thesis.

CHAPTER 2

PSEUDOMORPHIC HIGH ELECTRON MOBILITY TRANSISTOR: THEORY AND BACKGROUND

2.1 INTRODUCTION

For many applications, the most advanced technology is always a preferred option. In the early applications used in advanced military systems, the superior performance of pseudomorphic high electron mobility (pHEMT) technology outweighed the higher system cost. Therefore, the defence community in the United States made a very large investment in pHEMT materials, design and manufacturing capabilities in order to benefit from the superior performance of the device. This contributed towards the evolution of a cost effective pHEMT technology base. As a result, pHEMT technology is now routinely selected and used in commercial applications including mobile communications and wireless local area networks.

Having the advantages of an extremely high cut-off frequency, f_T and high transconductance, g_m, pHEMTs have become one of the primary choices for satellite communication applications. However, the low noise and high speed performance are not the only concerns for space applications, since stability and power consumption are also vital. Thus, there is always competition with pHEMT technology from SiGe, MESFET and conventional HEMTs [13, 14], due to their reasonably stable performance.

In this work, a novel InAlAs/InGaAs/InP pHEMT structure has been studied and investigated at the University of Manchester and is chosen as the active device for the design and implementation of low noise and broadband amplifier, mainly for the Square Kilometre Array (SKA), as it has potentially the lowest noise figures when compared to any alternative technologies, purely based on its superior material properties. The operating frequency range 0.4 GHz to 1.4 GHz corresponding to the mid-frequency array configuration of the SKA.

Before discussing the advantages of pHEMT devices, it is paramount to understand the underlying fundamental theory of semiconductor devices. Therefore this chapter provides a basic outline of the theory and mechanisms involved in the development of high electron mobility transistors. The chapter is arranged as follows: Firstly, the theoretical basis for heterostructures, lattice matching, pseudomorphism, band structures and quantum wells are discussed. This is followed by the conceptual description of metal-semiconductor contacts, including the theory of Schottky and Ohmic contacts. Finally, a conventional pHEMT epilayer structure is presented, followed by a literature review of the emergence of pHEMT in the marketplace.

2.2 HETEROJUNCTIONS AND HETEROSTRUCTURES

Heterojunctions are the fundamental building blocks of many of the most advanced semiconductor devices. A heterojunction is the interface between two dissimilar semiconductors. The combination of multiple heterojunctions in a device is called a heterostructure.

The idea of using heterostructures in semiconductor electronics emerged at the very dawn of electronics. W. Shockley proposed the application of a wide-gap emitter in his patent associated with p–n junction transistors [15]. At present, heterostructure-based devices are widely used for the development of advanced microwave electronic devices [16, 17] and are major components in consumer electronics. The molecular beam epitaxy (MBE) technique has grown into one of the most important technologies for the growth of high performance microwave heterostructures using III–V compounds, primarily through the pioneering work of A. Cho [18].

The HEMT and pHEMT utilise a heterojunction within their structure to improve their performance. The crucial characteristic of semiconductor heterojunctions is the interplay between their energy band gaps and lattice constants. Theoretically, an ideal heterojunction is one where the interface is free from structural and other crystalline defects such as dislocations and mechanical stresses. In this case, the heterojunctions are grown using lattice-matched semiconductors which have equal lattice constants.

2.2.1 Lattice-Matched Semiconductors

This section discusses the most important III-V compounds that can be used for the individual layer of the basic pHEMT structure. Figure 2-1 shows the lattice constant versus bandgap energy for the most widely used III-V semiconductors. The material bandgaps range from 0.17 eV (InSb) to 2.45 eV (AlP). The dotted lines in the graph represent the indirect bandgap. Two semi-insulating substrate materials that are available for epitaxial growth are GaAs and InP.

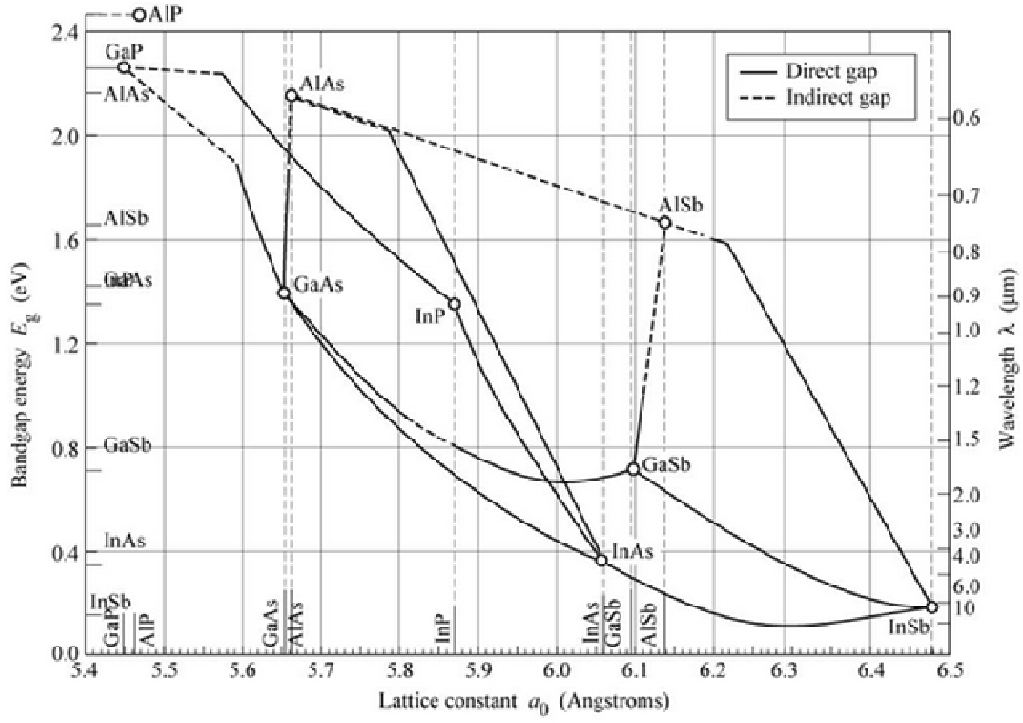


Figure 2-1 Lattice constant versus energy gap at room temperature for various III-V semiconductors and their alloys [19]

To minimise the disturbance at the heterointerface, the materials chosen must have very close lattice constants. This is often not the case across the various materials, thus Vegard's law [20] is used to synthesize new semiconductor materials to match the size of the crystal lattices. For example the lattice constant of a ternary alloy $A_xB_{(1-x)}Z$ is made up from two semiconductors AZ and BZ. Therefore the resulting lattice constant will obey Vegard's law:

$$a_{alloy}=xAZ+(1-x)BZ \quad (2\text{-}1)$$

This rule has been shown to be accurate for most semiconductors including AlGaAs [21] and InGaAs [22].

The AlAs, $Al_xGa_{(1-x)}As$, (for all values of x) and $In_{0.48}Ga_{0.52}P$ are examples of compound semiconductors lattice-matched to GaAs. For an InP substrate, the lattice-matched $In_{0.52}Al_{0.48}As$ is usually used as a buffer as it has a large band gap, resulting in improved insulation; and $In_{0.53}Ga_{0.47}As$ as a channel (due to its high mobility) followed by $In_{0.52}Al_{0.48}As$ as a barrier (large Delta E_v).

Enhancements in epitaxial growth techniques have enabled the possibility of growing lattice mismatched heterostructures [23, 24]. The crystalline defects are avoided if the lattice constants differ marginally and the growth of the mismatched layer is keep below a certain critical thickness limit [25, 26]. In this situation, the lattice atoms change abruptly between the two semiconductor materials with dissimilar energy band gaps and lattice constants [27]. This growth technique is known as *pseudomorphism* and will be further explained in the following section.

2.2.2 Pseudomorphic Materials

Pseudomorphism is a growth technique in which the lattice constant of the grown material becomes strained in order to fully align itself with the lattice constant of the base material. This high quality crystal growth can be produced with the help of advanced technology such as molecular beam epitaxy (MBE). The conceptual formation of pseudomorphic heterostructures with lattice mismatched materials is depicted in Figure 2-2. For lattice-matched materials, the overlayer lattice constant (a_L) is the same as the lattice constant of the substrate (a_S) as shown in Figure 2-2 (a). However, as seen in Figure 2 it is very rare for heteroepitaxial growth to be exactly lattice-matched. In most cases, the epitaxial layer has a lattice constant that is different from that of the substrate. Figure 2-2 (b) shows a semiconductor heterostructure in compressive strain ($a_L > a_S$) and Figure 2-2 (c) is when the semiconductor is in tensile strain ($a_L < aS$).

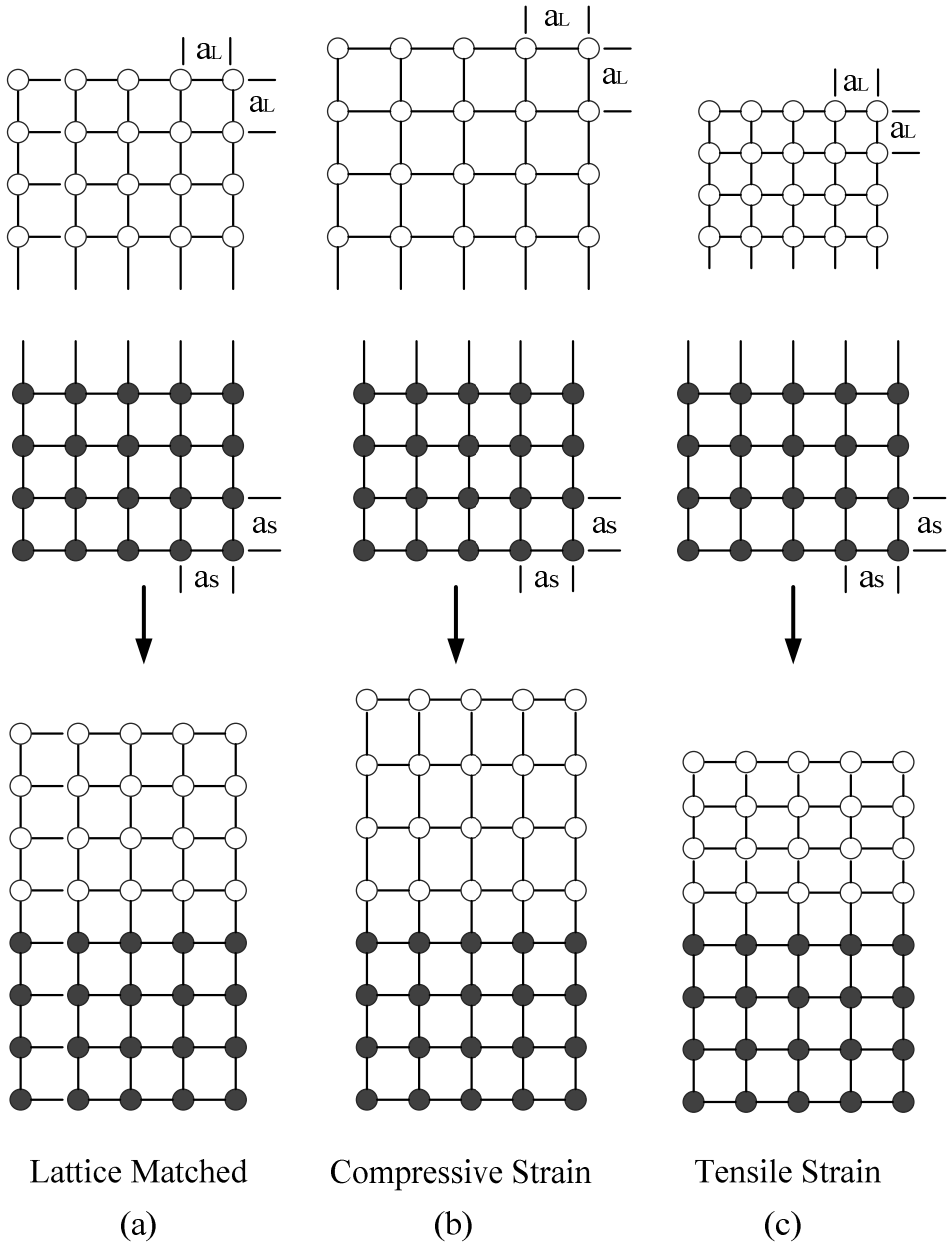


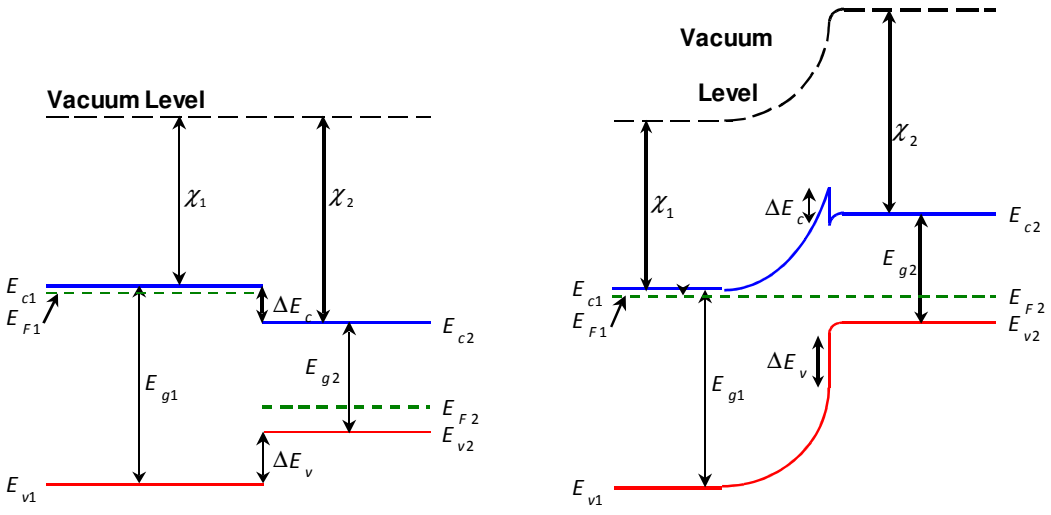
Figure 2-2 Conceptual formation of (a) Lattice-Matched, (b) Compressive Strain and (c) Tensile Strain

The main advantages of pHEMT technology are its enhanced electron mobility (because mobilities are always higher in Indium containing compounds) and improved carrier confinement at the AlGaAs/InGaAs heterointerface (as the Indium containing compounds have always lower band gaps). This high electron mobility and channel carrier density will provide higher transconductance compared to conventional AlGaAs/GaAs HEMTs [28].

2.2.3 Band Structure

The joining of two dissimilar semiconductors with different band gaps results in the formation of an energy difference at the interface This energy difference will result, in most instances, in an abrupt change in the energy band diagram of the heterostructure.

The notations of band alignment at the heterojunction are shown in Figure 2-3. E_C and E_V indicate the conduction and valence bands, E_g denotes the band gap, E_F the Fermi level, χ the electron affinity, and ΔE_C and ΔE_V represent the conduction and valence band discontinuities between the two materials [29]. Anderson [30] was the first to produce an energy-band model of an ideal, abrupt heterojunction, in which it was assumed that ΔE_c was equal to the difference in electron affinities χ as shown in equation (2-2) and (2-3).



(a) (b)

Figure 2-3 Energy band diagrams of wide and narrow band gap materials: (a) before and (b) after contact

$$\Delta E_c = \chi_1 - \chi_2 \qquad 2\text{-}2$$

Similarly, $$\Delta E_v = (E_{g2} - E_{g1}) - (\chi_1 - \chi_2) \quad \text{2-3}$$

Interestingly, depending upon the size of these discontinuities, and as a natural consequence of their existence, useful properties of heterojunctions such as quantum wells and two Dimensional Electron Gas (2DEG) formations occur.

2.2.4 Quantum Wells and 2DEG

The simplest configuration in which a quantum well can be formed is simply a thin layer of a narrow bandgap semiconductor (e.g. GaAs) sandwiched between two identical larger bandgap materials (e.g. $Al_xGa_{(1-x)}As$). As a result of the different band gaps, discontinuities in the conduction and valence band occur at the heterojunction interface and a quantum well is generated for both electron and hole carriers. Carriers in the quantum well can be supplied by dopant in the wider band-gap layers. As shown in Figure 2-4 if the bottom of the quantum well is below the Fermi level, the high energy electrons (from the donor atoms) can fall into the well and establish a quasi Two Dimensional Electron Gas (2DEG).

Due to the space charge, band bending occurs and consequently, a barrier is generated between $Al_xGa_{(1-x)}As$ and GaAs layers which eventually limits the carrier transfer. The 2DEG is free to move in the directions along the heterojunction interface [18] but not in the direction perpendicular to the interface. The 2DEG effectively improves carrier confinement.

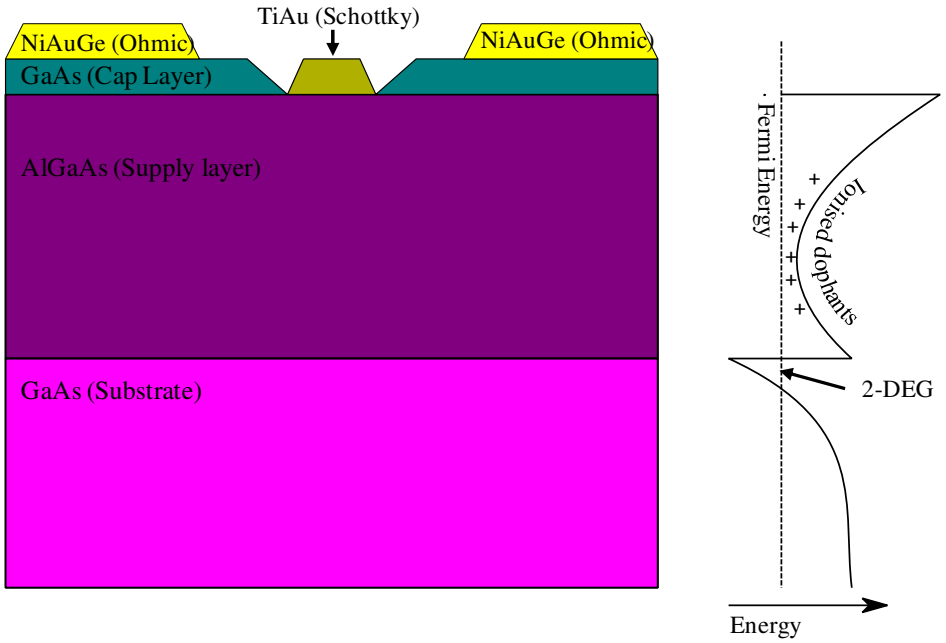


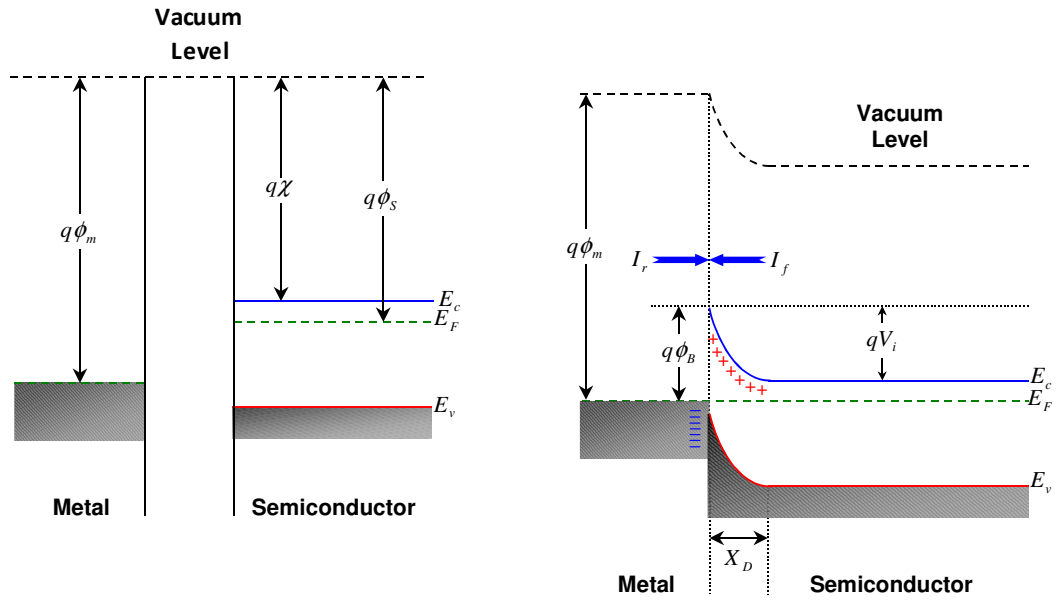
Figure 2-4 Typical epitaxial layer and energy band diagram of GaAs/AlGaAs HEMT

2.3 METAL-SEMICONDUCTOR CONTACTS

The basic knowledge of metal-semiconductor contacts is critically important for all semiconductor devices. There are two main types of metal-semiconductor contacts. The first is the 'Schottky' contact first identified and introduced by Schottky and Mott in 1938 [31]. Their model explained rectification in terms of electrons passing over a potential barrier through thermionic emission. The second type is the 'Ohmic' contact that provides a low resistance path between the semiconductor and the metal.

2.3.1 Schottky Contacts

Figure 2-5 shows a schematic band structure of an unbiased metal-semiconductor contact before and after contact according to the Schottky-Mott theory [32].



(a) (b)

Figure 2-5 Band diagram of Schottky contact (a) before contact and (b) after contact [33]

In the band diagram, ϕ_B is the contact barrier height, ϕ_m is the metal work function, χ is the electron affinity of the semiconductor, V_i is the built-in-voltage, E_c is the bottom of the conduction band, E_v is the top of the valance band, E_F is the Fermi level, I_f is the forward current and I_r is the reverse current.

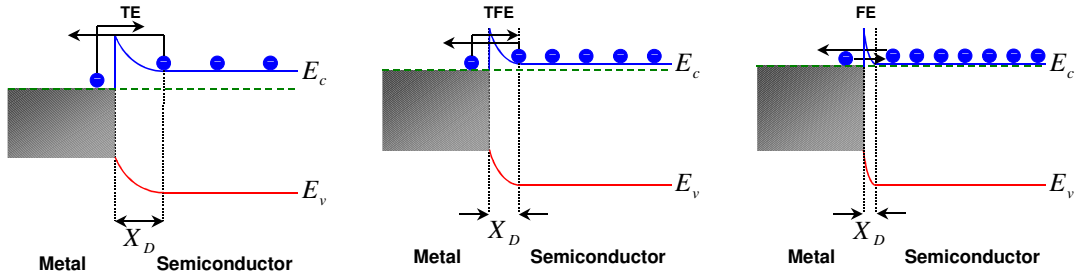
When metal and semiconductor are in contact, electrons flow from the semiconductor conduction band into the metal until an equilibrium condition is achieved, i.e. the Fermi levels align. The flow of electrons produces a depletion region (X_D) in the semiconductor near the junction, and results in upward bending of the energy bands as shown in Figure 2-5 (b). The band bending generates a barrier height ϕ_B and built-in voltage potential V_i that restricts further diffusion of electrons from semiconductor to metal. The barrier height ϕ_B is given by:

$$\phi_B = \phi_m - \chi \qquad 2\text{-}4$$

In the forward bias situation (V positive), the effective barrier (ϕ_B –V) is much lower and the depletion region X_D is smaller. Therefore, electrons can easily tunnel through the barrier resulting in a large current flow into the metal. In contrast, in the reverse condition (V negative), the effective barrier (ϕ_B –V) is much larger and X_D is increased, and this limits the current flows into the metal.

2.3.2 Ohmic Contacts

The Ohmic contact is a low resistance junction (non-rectifying) providing current conduction from metal to semiconductor and vice versa. These contacts have linear I-V characteristics in both directions. The purpose of the Ohmic contact is to provide an electrical path to the outside world without affecting the device characteristics. Figure 2-6 illustrates three conduction mechanisms that take place at different doping concentrations.



(a) Thermionic emission (TE): Carriers thermally excited over the barrier (**Low N_D**)

(b) Thermionic Field Emission (TFE): Carriers are thermally excited to an energy where the barrier is sufficiently narrow for tunnelling to take place (**Intermediate N_D**)

(c) Field Emission (FE): Carriers can tunnel through entire barrier (**High N_D**)

Figure 2-6 Depletion type contacts to n-type substrates with increasing doping concentration N_D: (a) Low N_D, (b) Intermediate N_D and (c) High N_D [33]

The most common method used to produce an Ohmic contact is to highly dope the layer directly beneath the metal (typically 1×10^{19} cm^{-3} or higher for n-type $In_{0.53}Ga_{0.47}As$) to enable tunnelling through the barrier [34].

2.4 pHEMT EPITAXIAL LAYER STRUCTURES

The emergence of the pHEMT resulted from the integration of the above concepts. In a pHEMT structure, a better carrier confinement in the 2DEG can be achieved from a pseudomorphic layer when compared to a lattice-matched material. Due to this unique feature, the device will have superior characteristics such as: a carrier-rich channel, high transconductance, and better output current. Figure 2-7 shows a 3D schematic structure of a pHEMT device.

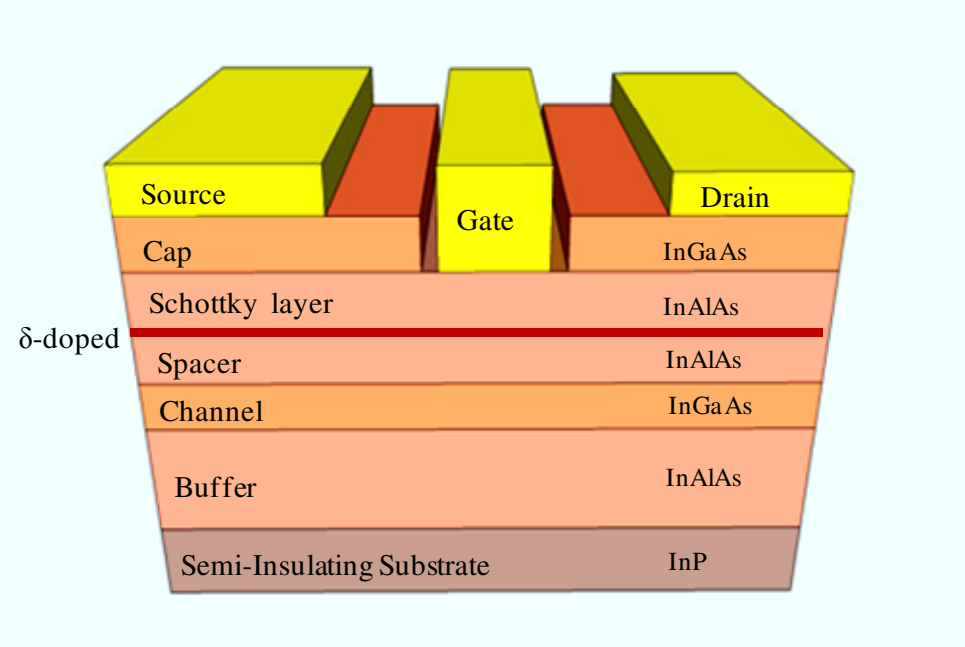


Figure 2-7 Epitaxial Layer of pHEMT device

The current flow is through the 2DEG channel from an Ohmic contact located at the source and drain terminals. This current flow is controlled via a depletion width induced by the gate bias. Here the gate contact is made from a metal-semiconductor Schottky contact. The uppermost layer in the pHEMT structure is a cap layer and is

used for the source and drain Ohmic contacts. The cap layer is a low band gap semiconductor which produces good Ohmic contacts. Below the cap layer is the Schottky barrier layer which is used as a wall to prevent thermally excited gate electrons entering the semiconductor channel as a leakage current. The thin-large bandgap spacer layer is used as an intermediate layer to enable electrons from the δ-doped layer to fall into the 2DEG channel (quantum well) and become trapped, and to increase the mobility by minimising remote carrier scattering.

The δ-doped layer can minimise the effect of parasitic parallel conduction which can be seen in the bulk doped layer. By referring to the δ-doped energy band diagram in Figure 2-8, E_1^{δ} is the quantised energy in the δ-doped region, whereas E_1 is the quantised energy in the quantum well. When E_1^{δ} is below the Fermi level, E_F, a parallel conductive channel is formed in the supply layer. If it is not fully depleted by the built-in and the applied voltages, this parallel channel will become an undesired portion of the 2DEG. Similarly, in bulk-doped structure, the parallel conduction will occur if the conduction band minimum in supply layer is lower than E_F.

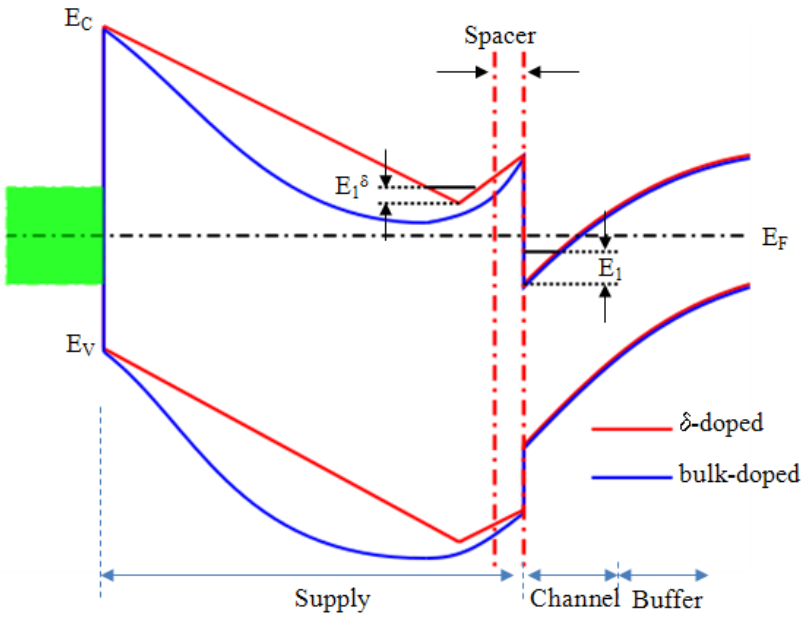


Figure 2-8 Band diagram and quantised carriers between δ-doped and bulk-doped heterostructures resulting similar 2DEG carrier densities [35]

Figure 2-8 also shows the band bending for both δ-doped and bulk-doped structures. As can be seen, a similar carrier concentration in the channel is obtained for both

structures despite the reduced doping in the δ-doped structure. As a consequence, a lower conduction band minimum in the supply layer is observed in bulk-doped layer. In other words, the δ-doping technique can provide higher 2DEG carrier densities as compared to similar bulk-doping levels, thus allowing for the incorporation of less dopants and avoid the unwanted parallel conduction.

Finally, by referring back to Figure 2-7, the thick buffer layer is used to reduce any growth defects, and to accumulate any impurities from the substrate interface that may degrade the performance of the 2DEG channel.

There are a number of reasons why the pHEMT offers performance advantages for both low noise and power applications over the conventional GaAs/AlGaAs HEMT: Firstly, the larger bandgap discontinuity between AlGaAs and InGaAs compared to that between AlGaAs and GaAs produces higher sheet carrier density (more charge transfer) and thus higher device current in the pHEMT compared to the HEMT. Secondly, the increased saturated electron velocity of InGaAs compared to GaAs results in elevated gain and improved high frequency performance. Thirdly, the improved carrier confinement in the InGaAs channel results in a lower output conductance. These advantages allow pHEMTs to produce higher gain, a better noise figure, and higher current (for power applications), when compared to HEMTs.

The performance of the pHEMT device is particularly dependent on the underlying epitaxial heterostructure, both in terms of the quality of the individual layers, and the quality of the overall layer structure (such as its composition and thickness). It is therefore important to ensure that the quality of the epitaxial layers is high before any device processing commences.

2.5 HOW THE pHEMT EMERGED

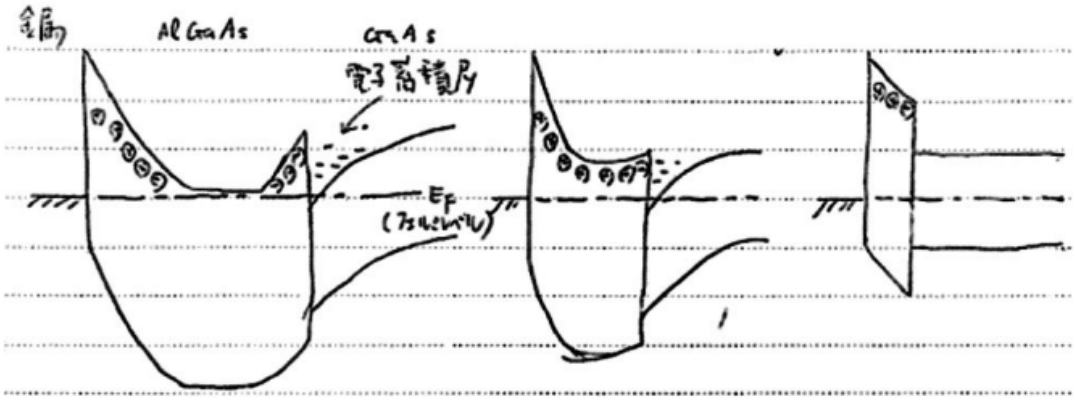
The milestones in pHEMT development are summarised in Table 2-1. Back in the 1950's, research was motivated by the first demonstration of a heterojunction device proposed by Shockley [15]. Since then, each decade saw significant work towards the development of the pHEMT. In 1969, Esaki and Tsu proposed the concept of the modulation-doped super-lattice. The knowledge of super-lattice behaviour [36] and

the application of MBE growth techniques [18, 37] led to the first patent by Dingle, *et al.* Inspired by the super-lattice structure, Mimura, *et al*. came up with the concept of using a field effect to modulate electrons at the interface of a heterostructure consisting of an un-doped GaAs and n-type AlGaAs pair. Figure 2-9 shows his original sketch depicting the device principle of HEMTs, which was patented in 1980 [38].

Table 2-1 Milestones in pHEMT development

Year Published	Development	Ref
1951	Heterojunction device proposed (Patent No: 2569347)	[15]
1969	Mobility enhancement in superlatttice heterojunction predicted for GaAs/AlGaAs system	[39]
1969	Molecular Beam Epitaxy demonstrated	[18, 37]
1978	Mobility enhancement in GaAs/AlGaAs demonstrated	[36]
1978	U. S. Patent for HEMT (Patent No: 4163237)	[40]
1980	First demonstration of HEMT device	[38, 41]
1985	Pseudomorphic HEMT introduced	[42, 43]
1986	Present InGaAs/AlGaAs pHEMT structure introduced	[44]
1987	Pulse-doped pHEMT demonstrated	[45]
1988	First InP pHEMT having highest f_T reported	[46]
1989	First pHEMT-based MMIC reported	[47]

The year 1985 is remembered as the year when the pHEMT was first introduced [42, 43]. After that, continuous work has been undertaken in device refinement and evolution from the basic pHEMT, to the pulse-doped pHEMT, to the fully functional pHEMT MMIC [44, 45, 47, 48]. The 1990's is the decade in which the pHEMT began to enter the marketplace.



(a) (b) (c)

Figure 2-9 Mimura original sketch on energy band diagrams explaining the operation principle of HEMTs: (a) Thick AlGaAs, (b) Medium AlGaAs and (c) Thin AlGaAs [38]

2.6 SUMMARY

This chapter presents the theory of the development of the pHEMT structure. It explains several factors which contribute to the superior characteristics of the device, which make it suitable for use in low noise applications such as radio telescopes. The heart of the device is the compressively strained $In_xGa_{(1-x)}As$ ($x > 0.7$) channel in which the two dimensional electron gas (2DEG) is confined. After that, the fundamental epitaxial layer of conventional pHEMT is discussed. Finally, this chapter gives an overview of how the pHEMT rose to prominence, from the heterostructure concept proposed in 1951, to the first pHEMT reported in 1985.

CHAPTER 3

TWO-PORTS NETWORK

3.1 INTRODUCTION

The simplest and most effective approach to describe the performance of a high-frequency design is though the use of a two-port network representation. This chapter defines and describes the properties of a two-port network in detail. Firstly, the concept of the two-port network is briefly discussed, followed by its key figures of merit:

1) Gain
2) Noise
3) Stability
4) Linearity

These parameters are important in the design of low noise amplifier. To make the circuit analysis simpler, the Scattering (S) parameter concept will be used throughout this chapter.

3.2 THE TWO-PORT NETWORK

Figure 3-1 shows a general representation of a two-port network. A two-port network describes the relationship between voltage, V_1 and current, i_1 at the input port and voltage, V_2 and current, i_2 at the output port.

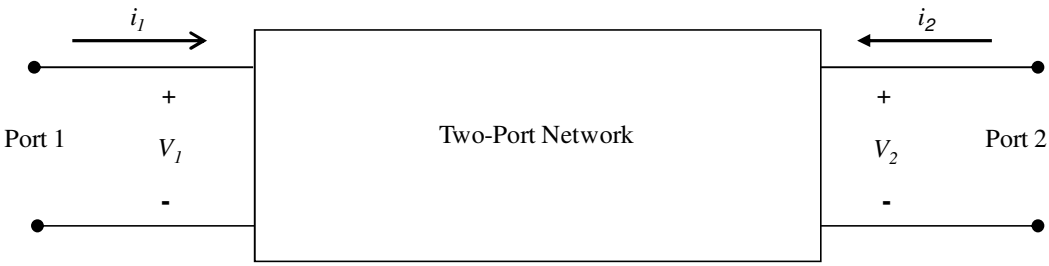


Figure 3-1 A general representation of two-port network model

At low frequencies, it is possible to characterise this two-port network by applying a test current or voltage at the input port whilst maintaining the output port as an open or short circuit. This is known as Z (impedance) and Y (admittance) characterisation as shown in equation (3-1) and (3-2):

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} \quad 3\text{-}1$$

$$\begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \quad 3\text{-}2$$

However, at RF and microwave frequencies, these characterisations become increasingly difficult to determine since open and short circuits of ac signals are notoriously difficult to implement [49]. Hence, another representation, known as Scattering parameters (S-parameters), is used to describe circuit performance, detailed in the next subsection.

3.2.1 Scattering Parameter

S-parameters are commonly defined as a set of parameters which relate to the transit of an incident wave, a_i or reflected wave, b_i through a transmission line when an n-port network is inserted into it. Figure 3-2 shows the S-parameter representation for a two-port network.

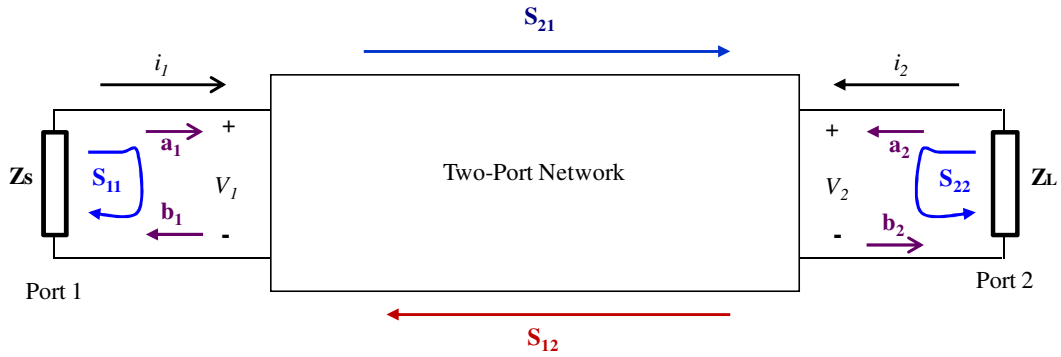


Figure 3-2 A diagram of S-parameter representation of two-port network

The S-parameter matrix for a two-port network is given as:

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \qquad 3\text{-}3$$

Where: S_{11} reflected signal at the input

S_{22} reflected signal at the output

S_{12} transmitted signal from the output to the input, known as reverse gain

S_{21} transmitted signal from the input to the output, known as forward gain

An S-parameter can be represented by the reflected wave over the incident wave, (assuming that the input or output is properly terminated). Expanding equation (3-3), the following expressions are defined:

$$S_{11} = \left.\frac{b_1}{a_1}\right|_{a2=0} \qquad 3\text{-}4$$

$$S_{22} = \left.\frac{b_2}{a_2}\right|_{a1=0} \qquad 3\text{-}5$$

$$S_{12} = \left.\frac{b_1}{a_2}\right|_{a1=0} \quad 3\text{-}6$$

$$S_{21} = \left.\frac{b_2}{a_1}\right|_{a2=0} \quad 3\text{-}7$$

Conveniently, S-parameters can be converted to Y (admittance), Z (impedance) and H (Hybrid) parameters. S-parameters are usually measured with the device inserted between a 50 Ω load and source. The maximum power handling capability of a particular transmission line is found at 30 Ω, while the lowest attenuation is found at 77 Ω. The ideal characteristic impedance, therefore, is 50 Ω which a compromise between these two values.

The characterisation of S-parameters can be applied to both linear and nonlinear networks. Once the network's parameters have been determined, its behaviour in any external environment can be predicted without regard to the contents of the network. Theoretically, S-parameter analysis is much simpler and more convenient and capable of providing a greater insight into a measurement or design problem.

3.3 GAIN OF TWO-PORT NETWORKS

There are many expressions used by a designer to describe the gain of a two-port network. The most commonly used expressions are: the voltage gain, A_v, the maximum available gain, G_A and the maximum stable gain, G_S [49]. The easiest way to derive these gain expressions is by using the signal flow graph of the two-port network as depicted in Figure 3-1. The construction of a signal flow graph is discussed in [50].

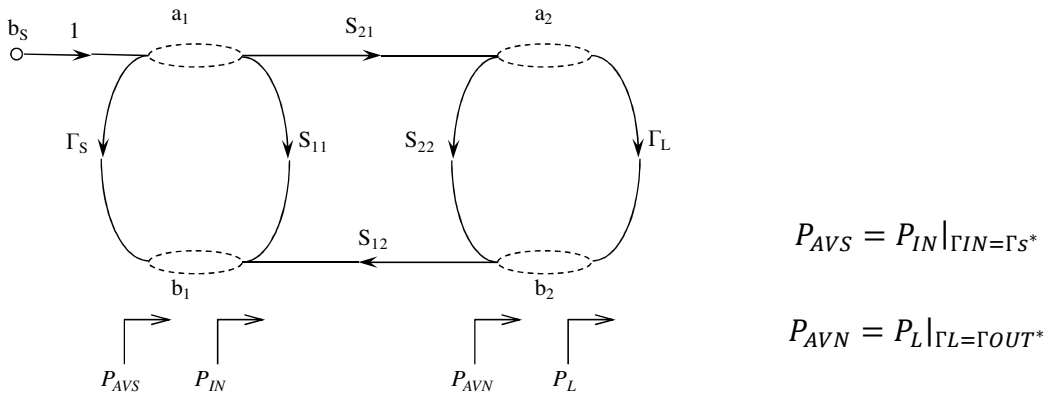


Figure 3-3 A diagram of signal flow graph of a two-port network

The voltage gain, A_v of the amplifier is defined as the ratio of the output voltage to the input voltage:

$$A_V = \frac{V_{OUT}}{V_{IN}} = \frac{a_2 + b_2}{a_1 + b_1} \qquad 3\text{-}8$$

where a_1 = The incident wave at port 1

a_2 = The incident wave at port 2

b_1 = The reflected wave at port 1

b_2 = The reflected wave at port 2

The complete derivation of voltage gain as written in Appendix A. The final derivation of the expression (3-8) can be written as:

$$A_V = \frac{S_{21}(1 + \Gamma_L)}{(1 - S_{22}\Gamma_L) + S_{11}(1 - S_{22}\Gamma_L) + S_{21}\Gamma_L S_{12}} \qquad 3\text{-}9$$

Where Γ_L and Γ_S are the load and source impedance respectively.

For the LNA design, the two most commonly used are the maximum available gain, G_A and maximum stable gain, G_S. G_A is given by:

$$G_A = \left|\frac{S_{21}}{S_{12}}\right| k - \sqrt{k^2 - 1} \qquad 3\text{-}10$$

Where k is the stability factor:

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} \qquad 3\text{-}11$$

Where Δ is the determinant of the scattering matrix, given by:

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| \qquad 3\text{-}12$$

The matching impedances necessary to achieve maximum stable gain may result in amplifier instability. The amplifier is unconditionally stable if $k > 1$ and leads to a definition of maximum stable gain:

$$G_S = \frac{|S_{21}|}{|S_{12}|} \qquad 3\text{-}13$$

3.4 NOISE IN A TWO-PORT NETWORK

Noise is an unwanted signal which can degrade the performance or quality of wanted data. In microwave designs, noise becomes the dominant issue and has been discussed thoroughly by many researchers [51-54].

A useful expression of the noise of a system is found by measuring its noise figure (F). In the 1940's, Harald Friis defined the noise figure of a network as the ratio of the signal-to-noise power ratio at the input to the signal-to-noise power ratio at the output [55]:

$$F = \frac{S_i/N_i}{S_O/N_O} \qquad 3\text{-}14$$

The noise figure, F also can be expressed in the form:

$$F = \frac{P_{No}}{P_{Ni}G_A} \tag{3-15}$$

Where P_{No} is the total available noise power at the output of the amplifier, P_{Ni} is the available noise power at the input and G_A is the available power gain given by:

$$G_A = \frac{P_{So}}{P_{Si}} \tag{3-16}$$

P_{Si} and P_{So} is the signal power at the input and output respectively.

Equations (3-15) and (3-16) are used to calculate the noise figure of single stage amplifier. However, equation (3-16) can be extended to express the noise figure of a double stage, or a two stage amplifier. The noise figure model of a double stage amplifier is depicted in Figure 3-4.

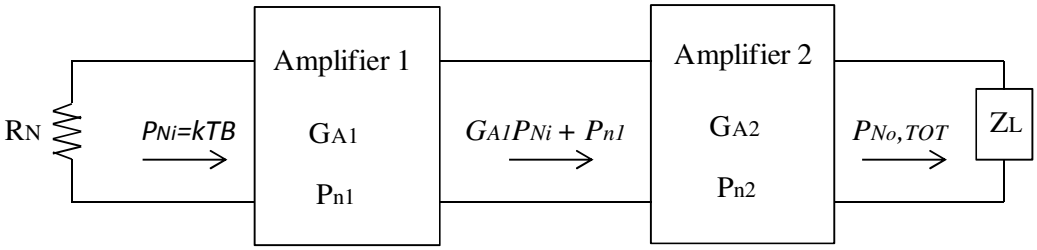


Figure 3-4 A noise figure model of a two stage amplifier

The total available noise power at the output $P_{No,TOT}$ is given by equation (3-17).

$$P_{No,TOT} = G_{A2}(G_{A1}P_{Ni} + P_{n1}) + P_{n2} \tag{3-17}$$

Where P_{n1} and P_{n2} is the noise power due to the first and second repeater respectively.

Therefore, the noise figure (F) of a double stage amplifier is given by:

$$F = \frac{P_{No,TOT}}{P_{Ni}G_{A1}G_{A2}} = 1 + \frac{P_{n1}}{P_{Ni}G_{A1}} + \frac{P_{n2}}{P_{Ni}G_{A1}G_{A2}} \tag{3-18}$$

Equation (3-18) can be written as:

$$F = F_1 + \frac{F_2 - 1}{G_{A1}} \quad 3\text{-}19$$

Where

$$F_1 = 1 + \frac{P_{n1}}{P_{Ni} G_{A1}} \quad 3\text{-}20$$

And

$$F_2 = 1 + \frac{P_{n2}}{P_{Ni} G_{A2}} \quad 3\text{-}21$$

In summary, the noise figure, F for a multistage system can be written in the form:

$$F_{total} = F_1 + \frac{F_2 - 1}{G_{A1}} + \frac{F_3 - 1}{G_{A1} G_{A2}} + \cdots + \frac{F_n - 1}{G_{A1} G_{A2} \ \ldots G_{A(n-1)}} \quad 3\text{-}22$$

Equation (3-22) was first introduced by Harald Friis in 1944 [55] and is now commonly referred to as the Friss Equation. Another important noise parameter is the minimum noise figure (F_{min}), which can be obtained if the design attains its optimal source impedance, that is when $\Gamma_S = \Gamma_O$. The expression for F_{min} is given by:

$$F_{min} = F - \frac{4 r_n |\Gamma_S - \Gamma_O|^2}{(1 - |\Gamma_S|^2)|1 + \Gamma_O|^2} \quad 3\text{-}23$$

Where r_n is the equivalent normalised noise resistance of the two-port network.

$$r_n = \frac{R_N}{Z_O} \quad 3\text{-}24$$

In modern usage, the quantity F in equation (3-14) is more often called the noise factor or sometimes the noise figure in linear terms. The term noise figure is usually applied to quantity *NF*, expressed in dB.

$$NF = 10 \log F \quad 3\text{-}25$$

3.5 STABILITY OF TWO-PORTS NETWORKS

The stability of an amplifier is a measure of its ability to resist any oscillations. This stability can be computed from the S-parameters, the input-output matching and the terminations. Figure 3-5 shows an illustration used to determine the stability of a two-port network.

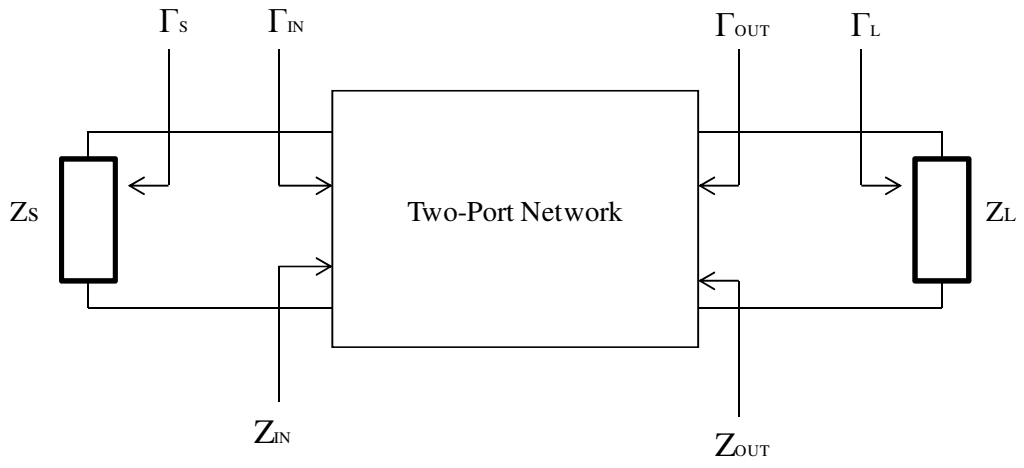


Figure 3-5 A diagram to calculate stability of a two-port network

Oscillation in a design will occur if $|\Gamma_{IN}| > 1$ or $|\Gamma_{OUT}| > 1$ or in term of S-parameters $|S_{11}| > 1$ or $|S_{22}| > 1$. Therefore, to achieve the optimum system performance, the amplifier must be insensitive to any oscillation. If this is the case, the system is said to be unconditionally stable. Unconditional stability refers to an amplifier that will not oscillate regardless of load or source impedance values. Equations (3-26) to (3-29) summarise the criteria for the circuit to be unconditionally stable.

$$|\Gamma_S| > 1 \tag{3-26}$$

$$|\Gamma_L| > 1 \tag{3-27}$$

$$|\Gamma_{IN}| = S_{11} < 1 \tag{3-28}$$

$$|\Gamma_{OUT}| = S_{22} < 1 \quad \text{3-29}$$

Another commonly used indicator of stability is the Rollett's K-factor [56]. A K-factor of 1.0 is the boundary condition for unconditional stability. If this factor is greater than zero but less than 1.0, the amplifier is only conditionally stable. The Rollett's stability K-factor is given by:

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} > 1 \quad \text{3-30}$$

Where $$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| < 1 \quad \text{3-31}$$

The K-factor is used throughout this thesis to indicate the stability of the designs.

3.6 LINEARITY

Linearity is another important factor in the design of amplifiers, especially power amplifiers. Ideally, the amplifier will behave linearly, so that the output signal corresponds proportionally to the input signal. There is a scenario where a possibly unwanted signal or cross-modulation may be present and mix with the amplified signal. This unwanted signal can usually be filtered out by the narrow bandwidth of the amplifier. However, there is tendency for this signal to mix and produce wideband noise if the amplifier behaves nonlinearly. Therefore, it will be extremely difficult to filter out this wideband noise.

The one-dB compression point, P_{1dB} and third-order interception point, IP3 are the figures-of-merit of the linearity of an amplifier, these are explained in the next subsections.

3.6.1 1-dB Compression Point

An amplifier behaves linearly when the output power is proportional to the input power. Above a certain input power, the output power will tend to saturate and

behave nonlinearly. The output power is therefore less than that predicted by the linear gain line, and hence the gain of the transistor decreases. Therefore, the 1-dB compression point indicates the power level that causes the gain to decrease by 1 dB from its small signal value and is denoted as P_{1dB}. Figure 3-6 shows this:

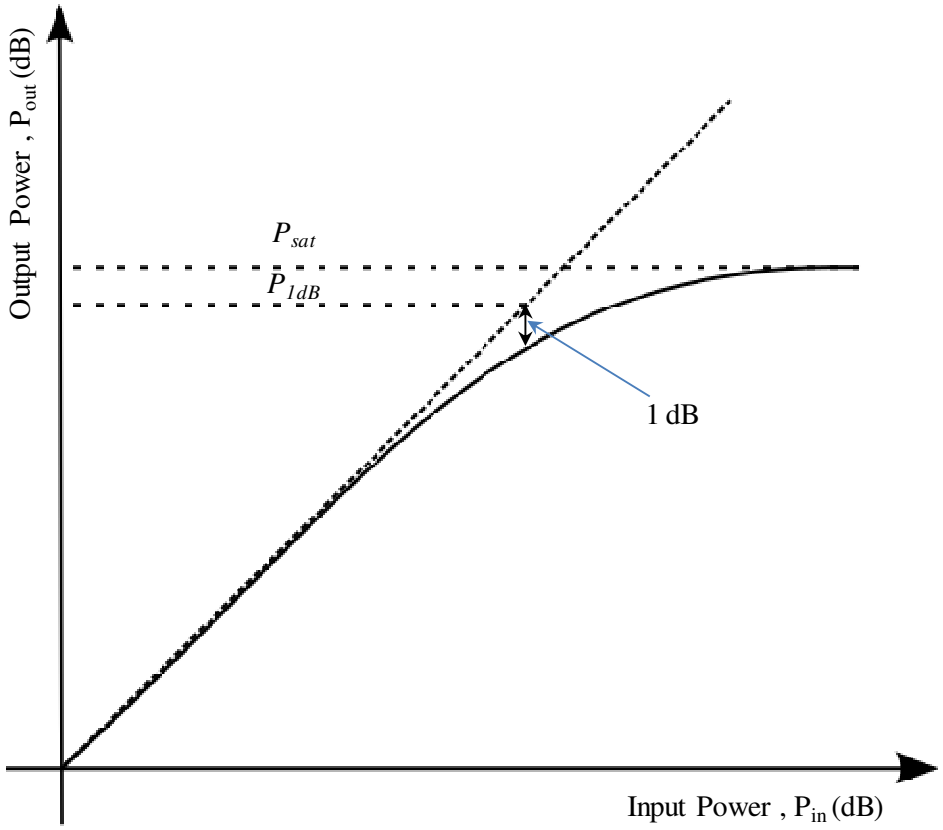


Figure 3-6 A graph of 1-dB gain compression point

3.6.2 Third Order Intercept and Intermodulation Distortion

Third order intercept point, IP3 is the input power point at which the first order and third order distortion output lines intercept, (assuming a linear system). Unfortunately, this intercept point is only theoretically calculated as this point is usually far greater than the output power of the device. Figure 3-7 shows the third order intercept point:

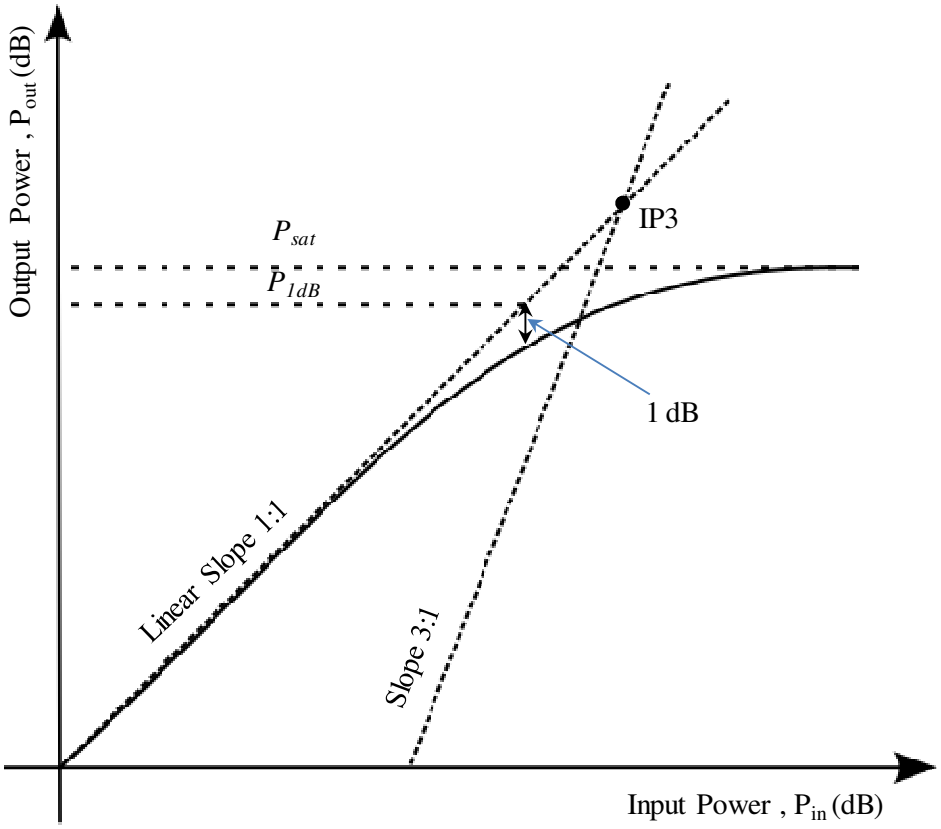


Figure 3-7 A graph of third order intercept point

The concept of third order intercept point, IP3, is more applicable to high power amplifiers. High power amplifiers create harmonic distortions where the harmonic appears as power loss in the fundamental (first order) frequency. For low noise amplifiers, the amplifiers produce the lowest distortion [57], hence the IP3 technique is less important. One of the simplest approaches to measure third-order distortion products is with a two-tone intermodulation test. The theory of the IP3 and the two-tone intermodulation test is discussed in detail in [49, 57].

3.7 SUMMARY

One of the most useful design analyses possible is the representation of the circuit as a two-port network system. A two-port network is depicted as a "box" with its properties specified by a matrix of numbers. This chapter discusses the design

requirements for two-port networks. These requirements are very important in order for an LNA to achieve its optimal performance. The S-parameters concept was introduced to describe the behaviour of microwave systems including LNAs. From Equation (3-22) it is clear that for a multistage system, the overall noise figure is dominated by that of the first stage. The noise figure of the second stage is reduced by the gain at the first stage, G_{A1}. Therefore the noise contribution of this second stage is small if G_{A1} is large. However, this higher gain can contribute to oscillation in un-optimised designs. Therefore, a compromise between noise figure and gain must be made. It is also shown that it is fairly challenging to measure the linearity of an amplifier using the concept of P_{1dB} and IP3 [49]. The simplest approach is to ensure that the amplifier is unconditionally stable. Therefore, the K-factor is the foremost characteristic used to determine the stability of an LNA, and it is relatively easy to measure using S-parameters.

In summary, designing broadband low noise amplifiers is very challenging, and requires consideration of the compromise between key factors that must be balanced to achieve optimal performance.

CHAPTER 4

DEVICE MODELLING: THEORY

4.1 INTRODUCTION

This chapter introduces the basic empirical modelling steps necessary to facilitate the design of a functioning low noise amplifier based on a single transistor model. The procedures used for the in-house pHEMT parameter extraction are also discussed in detail.

4.2 BIAS CONDITIONS

The correct bias point is essential to ensure that the transistor operates in the mode intended. Figure 4-1 shows the typical operating bias point for a FET, and indicates the four common operating bias points used for amplifiers [58]. For improved noise performance (Region I), the amplifier is biased at approximately V_{DS} = 1 V and 10 to 20% I_{dss}. I_{dss} is saturated drain current at V_{GS} = 0 V. Region II is used to bias the transistor for maximum gain, where V_{GS} is close to 0 V. Region III biases the transistor in the middle of I-V curves and allows the amplifier to work linearly. Region IV is biased for maximum efficiency with an increased V_{DS} and ~40% of I_{dss}. Since only a small amount of current is required for efficient biasing, this bias condition is a good choice in order to maintain low-power dissipation.

In this project, the transistor is biased in region I as noise is of primary importance. Therefore, the transistor models derived in the following section will be biased in this region.

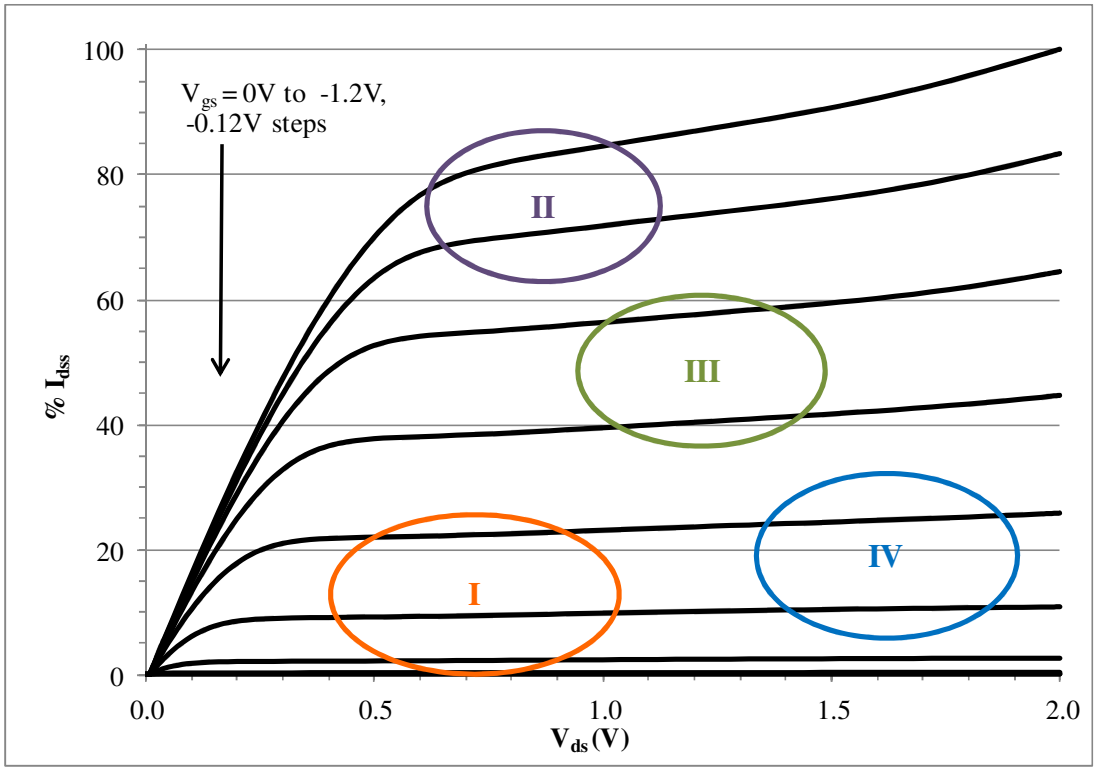


Figure 4-1 Graph of typical I-V characteristic and operating bias point for HEMT

4.3 TYPES OF MODELLING

There are two methods of device modelling:

1) Physical and
2) Empirical

Both modelling techniques can be used to represent a device, and selection of the appropriate model depends on the exact requirements of the particular application since each technique has its own advantages and limitations.

For physical modelling, the device is represented in terms of physical parameters, such as carrier transport, material properties and device geometry. Therefore, this model necessitates the need for detailed material property data, epitaxial structure design and manufacturing details, which are not always available from the device foundries. Additionally, simulation of a physical model typically requires more computational time and is heavily dependent on the user's ability to optimise the number of points used in the simulations and which models are required. SILVACO

is the example of software use for physical modelling [59]. The greater the number of points of the meshes used in the simulation, the more accurate the result will be, but the greater the required computational time. This model provides a physical insight into the device, and physical modelling for our in-house fabricated transistor has already been attempted by Shahzad Arshad, a former PhD student at Manchester University [60].

In contrast, empirical modelling is based on the mathematical representation of a device, from measurements over a specified voltage, current and frequency range. Therefore, this model is more efficient in terms of computation time and is normally used for circuit design. The empirical model is often referred to as 'black box' modelling since it relies only on measured data without considering the physical parameters of the device [61].

4.4 EMPIRICAL MODELLING

The empirical model of a transistor begins with the extraction of linear (small signal) parameters based on the measured DC and RF characteristics of the device. These parameters are then used in a large signal model, which includes the nonlinear behaviour of the transistor. This section will present empirical models for active device. These models are important for the accuracy of the LNA designs. Finally, noise models for a HEMT device are discussed as a starting point for successful LNA designs.

4.4.1 Linear Modelling

The linear model, also called the small signal model, consists only of linear elements known as intrinsic and extrinsic elements, and is based on the measured S-parameters of the device. There are several linear model circuit topologies described in [62-65]. The linear model presented in this work, developed by Dambrine *et al.* [64], is the most commonly used, and has been further extended by Shirakawa [66]

and Caddemi, *et al.* [67]. The extended technique has demonstrated an excellent match to the measured S-parameters over wide frequency bands.

The linear model can be physically correlated to pHEMT/HEMT devices as discussed in the next section.

4.4.1.1 Physical correlation of pHEMT/HEMT linear model

The physical origin of the pHEMT/HEMT linear equivalent circuit model is shown in Figure 4-2. This equivalent circuit model can be represented in a standard form as depicted in Figure 4-3. According to [64], the equivalent circuit model can be divided into two parts:

1) Extrinsic elements which are bias-independent and
2) Intrinsic elements which are bias-dependents

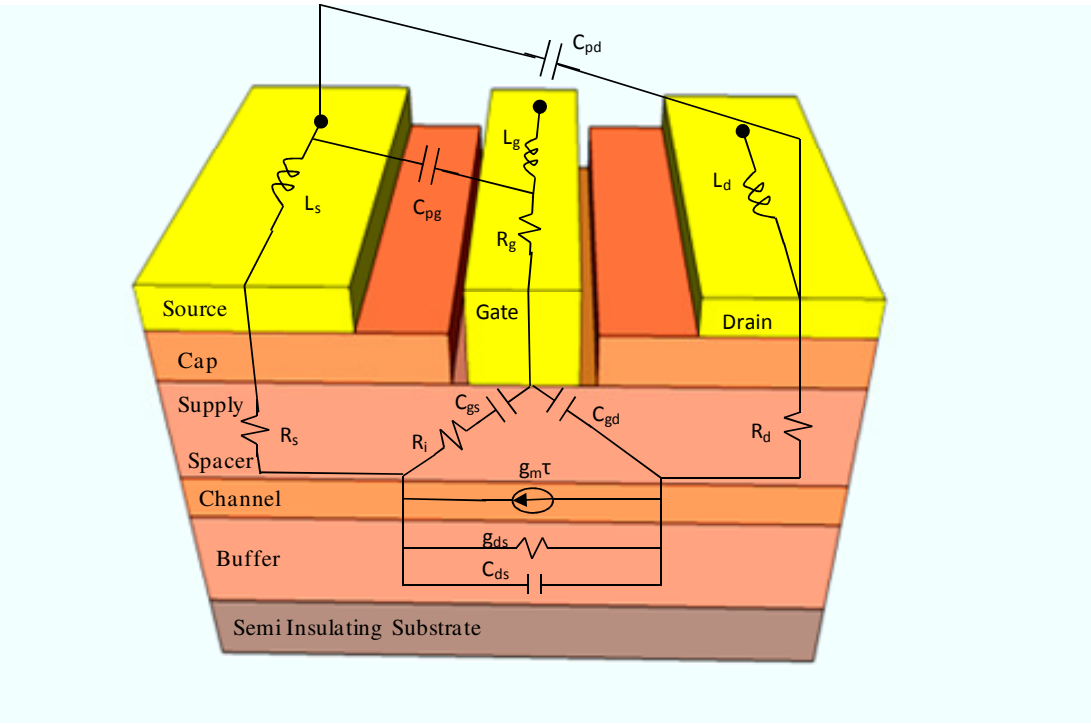


Figure 4-2 Physical origin of the pHEMT/HEMT linear equivalent circuit model

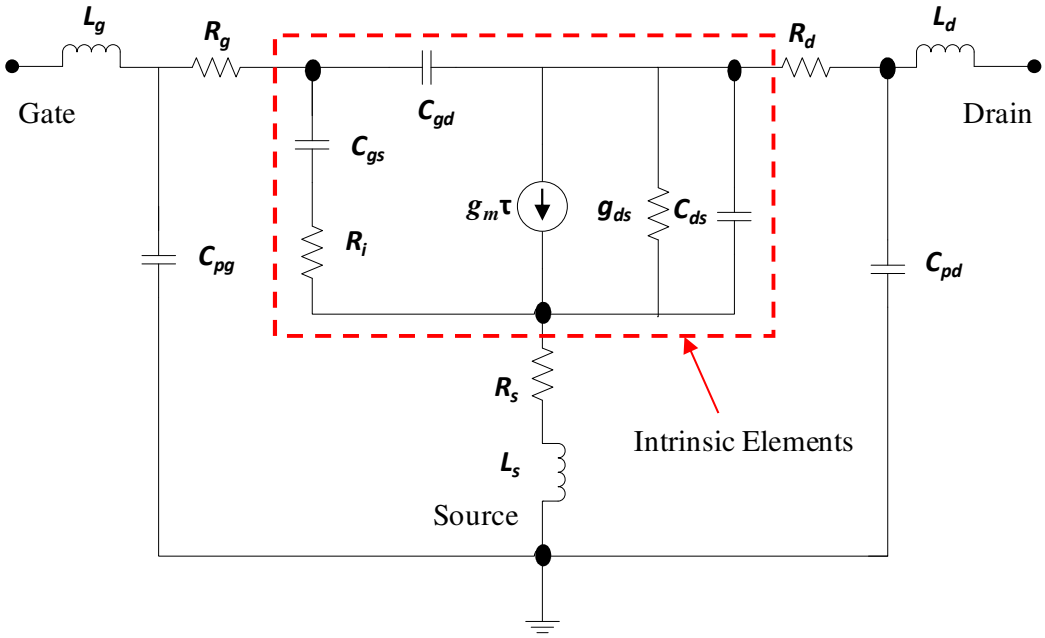


Figure 4-3 Standard form of pHEMT/HEMT linear equivalent circuit [64]

The eight extrinsic elements (R_s, R_d, R_g, L_s, L_d, L_g, C_{pd}, and C_{pg}) and seven intrinsic elements (g_m, R_i, τ, g_{ds}, C_{ds}, C_{gs}, and C_{gd}) in this model are described as follows:

Parasitic Inductances; L_s, L_d and L_g

L_s, L_d and L_g are the source, drain and gate inductances respectively. These inductances result from the metallisation of the contacts with the device surface. The gate inductance L_g is usually large for short gate length devices as shown in the equation below:

$$L_g = \frac{\mu_0 dW}{L_G} \qquad 4\text{-}1$$

Where μ_0 is the permeability of free space, d is the depletion depth, W is the gate width and L_G is the gate length.

Parasitic Resistances; R_s, R_d and R_g

R_s and R_d are the source and drain resistances respectively. These resistances exist due to the resistance of the Ohmic contacts, between the metal electrodes and the cap layer, and also include any bulk resistance to the active channel. R_g is the gate resistance which results from the metallisation of the Schottky contact at the gate terminal.

Capacitances; C_{gs}, C_{gd} and C_{ds}

The gate-source capacitance, C_{gs} and gate-drain capacitance, C_{gd} represent the variation of the depletion charge with respect to the gate-source and gate-drain voltages. The drain-source capacitance, C_{ds}, arises as a result of the capacitive effect between the drain and source electrodes.

Input Channel Resistance; R_i

R_i is the input channel resistance that exists under the gate, between the source and the channel. Normally, R_i will have a direct effect on the input reflection coefficient, S_{11} of the device.

Transconductance; g_m

The transconductance, g_m, is defined as the change in the drain current, I_{ds}, divided by the change in the gate-source voltage, V_{gs}. It is also a measure of how successfully the input voltage is converted to output current.

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}} \qquad 4\text{-}2$$

Output conductance; g_{ds}

Output conductance, g_{ds}, is defined as the change in the drain current, I_{ds}, divided by the change in the drain-source voltage, V_{ds}.

$$g_{ds} = \frac{\partial I_{ds}}{\partial V_{ds}} \quad 4\text{-}3$$

Transconductance Delay; τ

The transconductance delay, τ, is the delay time in the change in g_m that corresponds to a change in gate voltage. Alternatively it can be explained as the time taken for charges to re-arrange themselves upon variation of the gate voltage.

Bond Pad Capacitances; C_{pg} and C_{pd}

C_{pg} and C_{pd} are the bond pad capacitances at the gate and drain, respectively. These bond pads are required for probe measurement systems.

4.4.2 Linear Equivalent Circuit Parameter Extraction

The linear parameter extraction proposed in this project is based on S-parameters measurement of an in-house fabricated transistor. As stated in section 4.4.1, the most common technique used in this project is the linear model developed by Dambrine, *et al.* [64] and further extended by Shirakawa [66]. The linear equivalent circuit is commonly divided into two parts: the first is the extrinsic section which is outside the dashed line, and the second is the intrinsic section inside the dashed line as depicted in Figure 4-3. These extrinsic and intrinsic elements can be extracted using an optimisation technique [68] or analytical (direct) techniques [63, 67, 69]. The extraction technique used throughout this project is an analytical method. Finally an optimisation of parameters is performed to achieve an excellent fit between the modelled and measured data.

The extraction procedures begin with the extraction of extrinsic elements, followed by the extraction of intrinsic elements. These are explained in the next subsections.

4.4.2.1 Extrinsic elements extraction

The first step is the extraction of eight extrinsic elements from the measured pinched off or cold FET S-parameters. The cold FET measurements are taken at zero drain bias, V_{DS} = 0 V and gate voltage below the device pinch-off state, i.e. $V_{GS} < V_p$. Under this condition, there is no electron flow from source to drain, and therefore, g_m and g_{ds} are equal to zero. As a result, the three unknown values, g_m, g_{ds} and τ disappear. Moreover, the gate-source and gate-drain intrinsic circuits can be assumed to be equal due to the symmetry of the depletion region under the gate at V_{DS} = 0V [67]. Therefore, the final circuit has a Π-network configuration, which can be transformed into T-network to simplify the circuit analysis. The T-network for the equivalent circuit model of the device is shown in Figure 4-4:

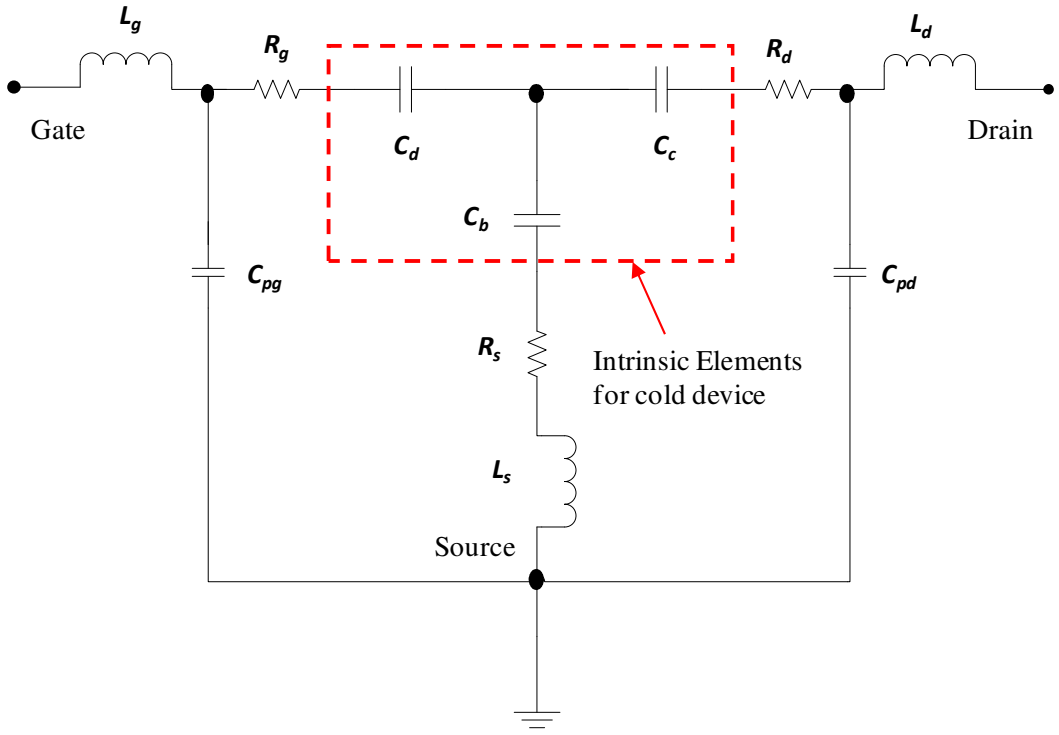


Figure 4-4 Schematic circuit of T network representation for linear equivalent circuit

Thus, the Z-parameters of the pinched off cold FET can be obtained:

$$Z_c = \begin{bmatrix} R_g + R_s + j\left[\omega\left(L_g + L_s\right) + \dfrac{1}{\omega C_{ab}}\right] & R_s + j\left[\omega L_s + \dfrac{1}{\omega C_b}\right] \\ R_s + j\left[\omega L_s + \dfrac{1}{\omega C_b}\right] & R_d + R_s + j\left[\omega\left(L_d + L_s\right) + \dfrac{1}{\omega C_{bc}}\right] \end{bmatrix} \quad 4\text{-}4$$

Where $C_{ab}^{-1} = C_a^{-1} + C_b^{-1}$, $C_{bc}^{-1} = C_b^{-1} + C_c^{-1}$ 4-5

The extrinsic equations are expressed as follows:

$$R_g = Re(Z_{c11} - Z_{c12}) \quad 4\text{-}6$$

$$R_s = Re(Z_{c11}) \quad 4\text{-}7$$

$$R_d = Re(Z_{c22} - Z_{c12}) \quad 4\text{-}8$$

$$\omega . Im(Z_{c11}) = \omega^2\left(L_g + L_s\right) - \frac{1}{C_{ab}} \quad 4\text{-}9$$

$$\omega . Im(Z_{c12}) = \omega^2 L_s - \frac{1}{C_b} \quad 4\text{-}10$$

$$\omega . Im(Z_{c22}) = \omega^2 (L_d + L_s) - \frac{1}{C_{bc}} \quad 4\text{-}11$$

Where *Re* ( ) is the real part and *Im* ( ) is the imaginary part.

The parasitic resistances, R_s, R_g and R_d, from equation (4-6) to equation (4-8), can be solved using the measured values of the Z-parameters from the cold device. All equations, from (4-9) to (4-11), represent a straight line plot for the measured ωIm (Z_{c11}), ωIm (Z_{c12}), and ωIm (Z_{c22}) versus ω^2. Taking the simplest equation, i.e. equation (4-10), the slope of the line will yield the inductance, L_s while the y-intercept of the line yields the capacitance, C_b. The values for inductances L_d and L_g can then easily be obtained.

Under pinch off bias condition, the resistances and inductances have no influence on the imaginary part of the Y parameters. This assumption is only valid for frequencies up to a few gigahertz [64]. The equations can now be simplified as:

$$Im\ (Y_{11}) = j\omega(C_{pg} + 2C_b) \quad 4\text{-}12$$

$$Im\ (Y_{12}) = Im(Y_{21}) = -j\omega C_b \quad 4\text{-}13$$

$$Im\ (Y_{22}) = j\omega(C_{pd} + C_b) \quad 4\text{-}14$$

The bond pad capacitances, C_{pg} and C_{pd}, from the equation (4-12) to equation (4-14) can be directly extracted since C_b was previously calculated.

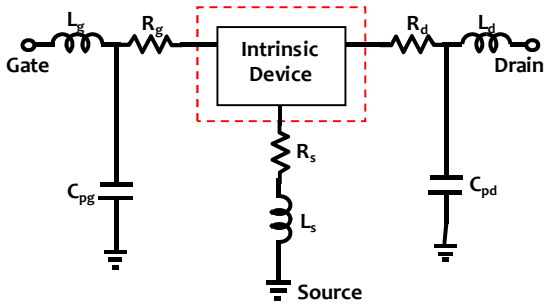
4.4.2.2 The intrinsic elements extraction

After extracting the eight extrinsic elements from the cold (pinched) device, the next procedure in linear parameter extraction is to extract the seven intrinsic elements from the measured S-parameters. According to Dambrine, the determination of the intrinsic admittance matrix (Y_{int}) can be carried out using simple matrix manipulations if the extrinsic elements are known. The extraction procedure carried out by Dambrine, *et. al*. is listed below [64]:

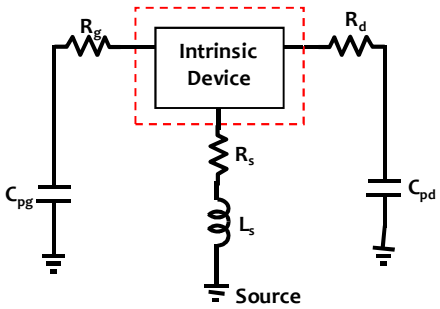
I. Measurement of the S-parameters of the extrinsic device
II. Transformation of the S-parameters to Z parameters and subtraction of L_g and L_d, which are series elements
III. Transformation of Z to Y parameters and subtraction of C_{pg} and C_{pd} ,which are in parallel
IV. Transformation of Y to Z parameters and subtraction of R_g, R_s, L_s,and R_s, which are in series
V. Transformation of Z to Y parameters which correspond to the desired matrix

Figure 4-5 shows the diagram for extracting intrinsic parameter as proposed by Dambrine, *et. al*.

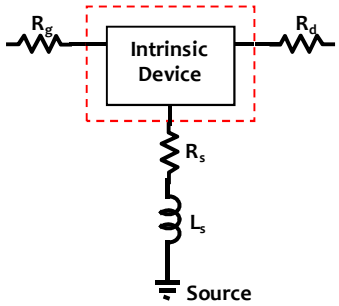
I $\begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix}$



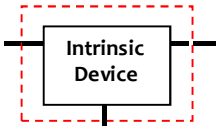
II $\begin{bmatrix} Z_{11} - j\omega L_g & Z_{12} \\ Z_{21} & Z_{22} - j\omega L_d \end{bmatrix}$



III $\begin{bmatrix} Y_{11} - j\omega C_{pg} & Y_{12} \\ Y_{21} & Y_{22} - j\omega C_{pd} \end{bmatrix}$



IV $\begin{bmatrix} Z_{11} - R_s - R_g - j\omega L_s & Z_{12} - R_s - j\omega L_s \\ Z_{21} - R_s - j\omega L_s & Z_{22} - R_s - j\omega L_s \end{bmatrix}$



V $(Y_{int}) = Z \rightarrow Y(Z_{int})$

Figure 4-5 Method for extracting the device intrinsic Y matrix [64]

The transformation of the Z matrix to the Y matrix is given in Appendix B.

The effects of extrinsic parameters are then subtracted from the measured hot (intrinsic) S-parameters to obtain the admittance ((Y_{int}), written as:

$$Y_{int} = \begin{bmatrix} \frac{R_i C_{gs}^2 \omega^2}{D} + j\omega\left(\frac{C_{gs}}{D} + C_{gd}\right) & -j\omega C_{gd} \\ \frac{g_m e^{-j\omega\tau}}{1 + j\omega R_i C_{gs}} - j\omega C_{gd} & g_{ds} + j\omega\left(C_{ds} + C_{gd}\right) \end{bmatrix} \quad 4\text{-}15$$

where
$$D = 1 + \omega^2 C_{gs}^2 R_i^2 \quad 4\text{-}16$$

The term $\omega^2 C_{gs}^2 R_i^2$ is less than 0.01 at frequencies below 5 GHz and hence D = 1 [64].

The expressions for all seven intrinsic parameters are expressed as [64]:

$$C_{gd} = Im(Y_{int21}) \quad 4\text{-}17$$

$$C_{gs} = \frac{Im(Y_{int11}) - \omega C_{gd}}{\omega}\left[1 + \frac{\{Re(Y_{int11})^2\}}{\{Im(Y_{int11}) - \omega C_{gd}\}^2}\right] \quad 4\text{-}18$$

$$R_i = \frac{Re(Y_{int11})}{\{Im(Y_{int11}) - \omega C_{gd}\}^2 + \{Re(Y_{int11})^2\}} \quad 4\text{-}19$$

$$\mathrm{g}_m = \sqrt{\{Re(Y_{int21})^2\} + \{Im(Y_{int21}) + \omega C_{gd}\}^2 D} \quad 4\text{-}20$$

$$\tau = \frac{1}{\omega} arcsin\left[\frac{-\omega C_{gd} - Im(Y_{int21}) - Re(Y_{int21})\omega C_{gs} R_i}{\mathrm{g}_m}\right] \quad 4\text{-}21$$

$$C_{ds} = \frac{Im(Y_{int22}) - \omega C\_gd}{\omega} \quad 4\text{-}22$$

And
$$R_{ds} = \frac{1}{Re(Y_{int22})} \quad 4\text{-}23$$

All of the equations for intrinsic and extrinsic parameter extraction explained in this work have been programmed in Advance Design System (ADS) software. This software reduces the possibility of errors in manual calculations. ADS also include an optimisation tool, in order to obtain the best performance from the linear model.

4.4.3 Nonlinear Modelling

An accurate nonlinear or large signal model of a transistor is an essential requirement for any circuit design. Therefore there is a continuous effort from circuit designers to produce efficient nonlinear models [70]. The first empirical nonlinear model, established in 1980, was developed by Curtice [62]. A decade later, several empirical nonlinear models had been developed in order to allow the model being extracted to use Computer Aided Design (CAD) tools [71]. McCamant*, et al*. [72] introduced a SPICE model for GaAs MESFET devices over a wide range of bias conditions. This model was achieved by modifying the model equations proposed by H. Statz *et al.*[73].

There are several CAD packages available for modelling devices in conjunction with the use of foundry modules in the design process [74]. Therefore, all designers have the freedom to choose any of the available CAD tools depending on whether the software has an accurate model built in.

Nonlinear models for microwave and millimetre wave devices are commonly based on DC and S-parameter measurements. The model used in this work was developed by Agilent, the EEsof EE-HEMT model in Advance Design System (ADS) [75]. The EE-HEMT is an empirical analytic model based on fitting of the measured electrical characteristics of HEMTs.

4.4.3.1 The EE-HEMT Model

This project made extensive use of Agilent's EE-HEMT large signal model for modelling the nonlinear behaviour of the active devices. The EE-HEMT equivalent

large signal model is depicted in Figure 4-6. The EE-HEMT model includes the following features [75]:

1) Accurate isothermal drain-source current model fits virtually all processes
2) Flexible transconductance formulation permits accurate fitting of g_m
3) Self-heating correction for drain-source current
4) Charge model that accurately tracks measured capacitance values
5) Dispersion model that permits simultaneous fitting of high-frequency conductances and DC characteristics
6) A breakdown model describes gate-drain current as a function of both V_{GS} and V_{DS}

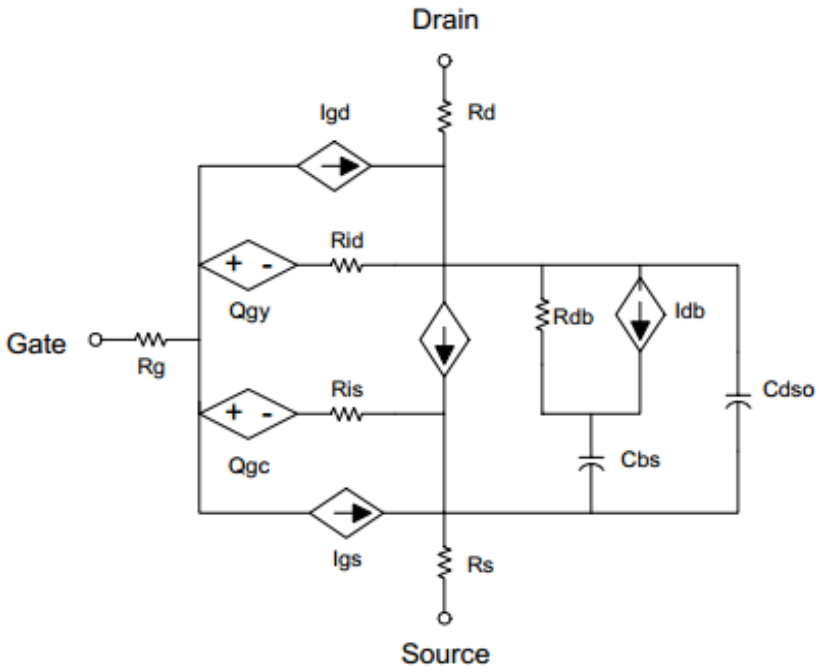


Figure 4-6 Schematic of EE-HEMT equivalent large signal model, reprinted from [75]

The EE-HEMT model equations were developed concurrently with parameter extraction techniques to ensure the model parameters was extractable from the measured data. Based on these specifications, the EE-HEMT model is classified into four (4) categories as discussed below:

Drain-source current parameters

This model enables the parameters to analytically express drain-source current, I_{ds}, transconductance, g_m and conductance, g_{ds} derivation. The drain-source current parameters are listed in Table 4-1. This model assumes that the device is symmetrical, i.e. V_{GS} is identical to V_{GD} and V_{DS} is identical to - V_{DS}.

Table 4-1 Table of Agilent EE-HEMT Model Drain-Source Current Parameters

Parameter	**Description**	**Units**	**Default**
Vto	Zero-bias threshold	V	-1.5
Gamma	Transconductance parameter	1/V	0.05
Vgo	Gate-source voltage where transconductance is a maximum	V	0.0
Vdelt	Parameter which controls linearization point	V	0.0
Vch	Gate-source voltage where Gamma no longer affects I-V curves	V	1.0
Gmmax	Peak transconductance	S	$70.0e^{-03}$
Vdso	Drain voltage where Vo dependence is nominal	V	2.0
Vsat	Drain-source current saturation	V	1.0
Kapa	Output conductance	S	1.0
Peff	Channel to backside self-heating (effective power compression)	W	2.0
Vtso	Subthreshold onset voltage	V	-10.0

g_m compression parameters

The g_m compression parameters are obtained from the measured DC characteristics and these parameters are stated in Table 4-2. These parameters are easily extracted from the g_m versus V_{gs} plot as illustrated in Figure 4-7.

Table 4-2 Table of Agilent EE-HEMT g_m Compression Parameters

Parameter	Description	Units	Default
Vco	Voltage where transconductance compression begins for $V_{ds}=V_{dso}$	V	10.0
Vba	Transconductance compression 'tail-off'	V	1.0
Vbc	Transconductance roll-off to tail-off transition voltage	V	1.0
Mu	Vo dependent to transconductance compression	None	1.0
Deltgm	Slope of transconductance compression characteristic	None	0.0
Alfa	Transconductance saturation to compression transition	V	$1.0e^{-3}$

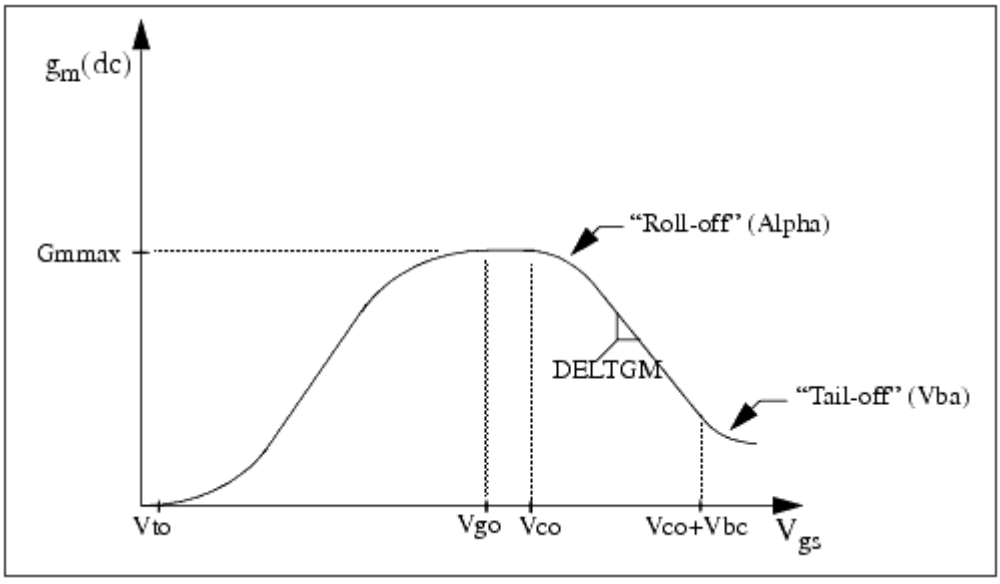


Figure 4-7 Graph of g_m versus V_{gs}, reprinted from [75]

Dispersion parameters

The dispersion parameters model the effects of dispersion current at high frequency, usually due to self-heating and charge-trapping. Therefore, for improved accuracy, pulsed I-V measurements are necessary to eliminate dispersion effects at high frequency. The model parameters for dispersion effects are provided in Table 4-3.

Table 4-3 Table of Agilent EE-HEMT Dispersion Parameters

Parameter	**Description**	**Units**	**Default**
Rdb	Dispersion source output impedance	Ohm	$1.0e^{+9}$
Cbs	Trapping-state capacitance	F	$1.6e^{-13}$
Gdbm	Additional d-b branch conductance at V_{ds} = Vdsm	None	0.0
Kdb	Dependence of d-b branch conductance with V_{ds}	None	0.0
Vdsm	Voltage where additional d-b branch conductance becomes constant	None	1.0
Vtoac	Zero-bias threshold (AC)	V	-1.5
Gammaac	V_{ds}-dependent threshold (AC).	1/V	0.05
Vdeltac	Parameter which controls linearization point (AC)	V	0.0
Gmmaxac	Peak transconductance (AC)	S	$60.0e^{-03}$
Kapaac	Output conductance (AC)	S	0.0
Peffac	Channel to backside self-heating (AC)	W	10.0

Gate Charge parameters

The Gate charge parameter model is observed from the effect of capacitances (obtained from measured Y-parameters). The gate charge parameters are listed in Table 4-4.

Table 4-4 Table of Agilent EE-HEMT Gate Charge Parameter

Parameter	Description	Units	Default
$C11_o$	Maximum input capacitance for V_{ds}=Vdso and Vdso>Deltds	F	$0.3e^{-12}$
$C11_{th}$	Minimum (threshold) input capacitance for V_{ds}=Vdso	F	$0.03e^{-12}$
V_{infl}	Inflection point in C11-V_{gs} characteristic	V	1.0
Deltgs	C11th to C11o transition voltage	V	0.5
Deltds	Linear region to saturation region transition	V	1.0
Lambda	C11-V_{ds} characteristic slope	1/V	1.0
C12sat	Input transcapacitance for V_{gs}=Vinfl and V_{ds}>Deltds	F	$0.03e^{-12}$
Cgdsat	Gate drain capacitance for Vds>Deltds	F	$0.05e^{-12}$
Ris	Source end channel resistance	Ohm	0.0
Rid	Drain end channel resistance	Ohm	0.0
Tau	Gate transit time delay	Sec	0.0
Cdso	Drain-source inter-electrode capacitance	F	$80.0e^{-15}$

All of the model parameters discussed above are commonly used to model the DC and RF characteristics of the transistors at room temperature, which is the specification for this project. The next section presents the source of noise in pHEMT followed by the techniques used to model this noise.

4.5 SOURCE OF NOISE IN pHEMTs

Noise is a random process associated with a variety of sources. The main sources of noise in a semiconductor device are thermal noise, shot noise and flicker noise.

4.5.1 Thermal Noise

Thermal noise, also known as Johnson noise, is generated by the random thermal motion of electrons due to the fluctuations of the electric current inside an electrical conductor [76, 77]. The thermal noise of the resistor is given by:

$$V_n = \sqrt{4kTR_n\Delta f}$$
$$\text{or} \qquad 4\text{-}24$$
$$I_n = \sqrt{4kT\Delta f / R_n}$$

Where V_n is the rms noise voltage source while I_n is the rms noise current source. T is the temperature in Kelvin, Δf is the bandwidth, k is Boltzmann's constant and R_n is the noise resistance in ohms. In pHEMTs, thermal noise is normally generated by the parasitic resistances of source, drain and gate.

4.5.2 Shot Noise

Shot noise is caused by the random fluctuation of the electrons in an electrical conductor. The shot noise is described as:

$$I_{ns}^2 = 2qI_o\Delta f \qquad 4\text{-}25$$

Based on equation (4-25), it is clear that, the shot noise is directly proportional to the magnitude of the DC current, I_o, of the device. Unlike thermal nose, this shot noise is independent of temperature. In pHEMTs, the shot noise is due to the reverse biased gate leakage current [78], therefore minimising this is essential.

4.5.3 Flicker Noise

Flicker noise is also known as 1/f noise since this noise varies inversely with the frequency. Flicker noise is caused by the random trapping and de-trapping of charges in the surface state [79]. Flicker noise is characterized by a corner (knee) frequency,

f_c, and usually occurs at frequencies lower than 1 MHz. Therefore, in pHEMTs, flicker noise is not generally important since the device is operated at microwave frequencies. However, flicker noise still exists in mixers and HEMT oscillators [78, 79] as it can be up-converted from lower frequencies to the operating microwave frequencies.

Other noise contributions in pHEMT are generation-recombination (G-R) noise and diffusion noise. Generation-recombination (G-R) noise is caused by fluctuations in the number of free carriers inside a two terminal sample, associated with random transitions of charge carriers between states of different energy bands [80]. The diffusion noise develops in portions of the semiconductor structure with an intense electric field, which produces heating of the electrons and a corresponding decrease in their mobility [81]. A distribution of the noise sources in pHEMT is depicted in the diagram in Figure 4-8.

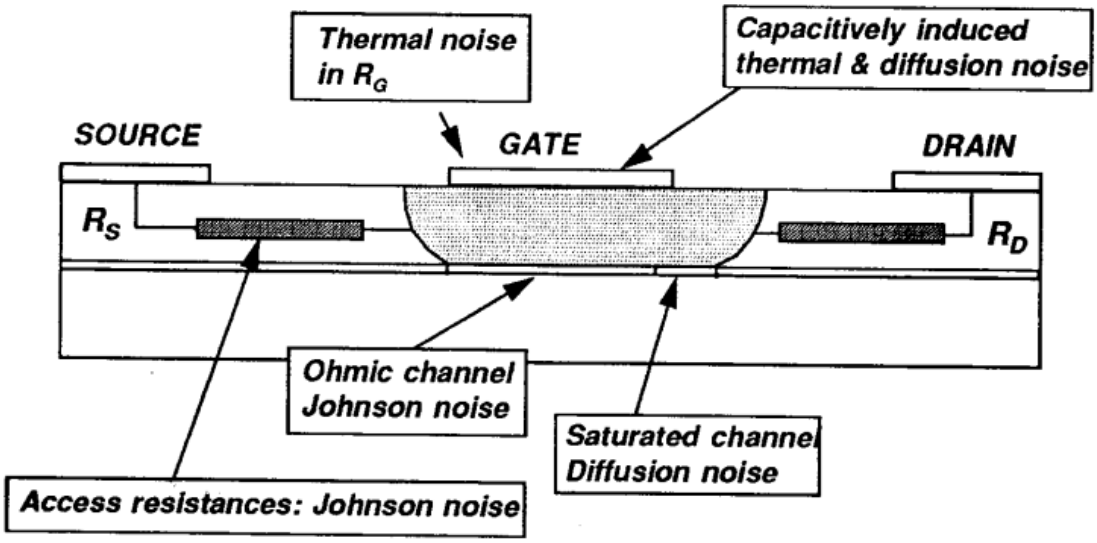


Figure 4-8 Distribution of noise sources in a pHEMT device, reprinted from [82]

4.6 FET/HEMT NOISE MODELLING

There have been many studies conducted by researchers to investigate the noise of semiconductor devices [53]. In 1960, Van der Ziel began to develop the first noise model to investigate the noise performance of an FET [51]. The work then continued with more detailed and refined methods by other researchers as described in the next section.

4.6.1 Fukui's Noise Model

Fukui's noise model was developed by Hatsuaki Fukui in 1979 [83]. This model described how the small signal parameters affect the noise performance of the devices, mainly GaAs MESFETs at the time. Figure 4-9 shows the equivalent circuit of a GaAs MESFET used by Fukui for noise analysis.

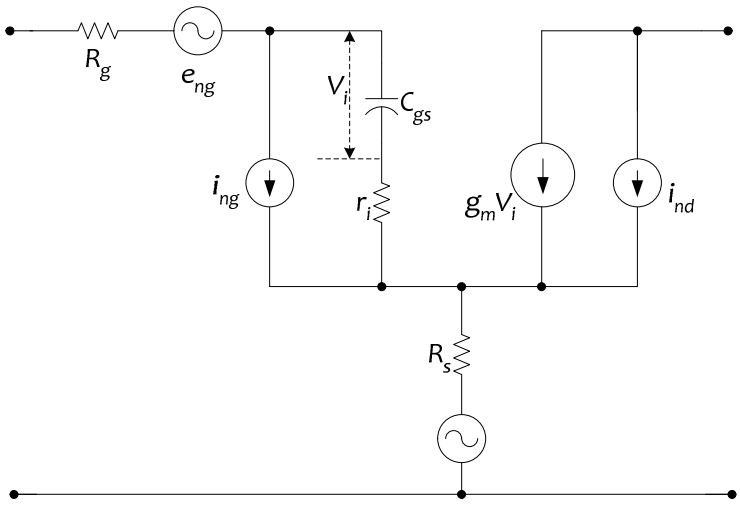


Figure 4-9 Fukui's Noise Model

In this model, the noise sources i_{ng}, i_{nd} e_{ng} and e_{ns}, represent the induced gate noise and drain-circuit noise. R_g and R_s are the thermal noise of the gate metallization

resistance and the thermal noise of the source resistance respectively. Fukui's expression for the minimum noise figure parameter is:

$$F_{min} = 1 + k_1 \frac{f}{f_T} \sqrt{g_m \left(R_s + R_g \right)} \qquad 4\text{-}26$$

Where, f_T is the unity current gain cut-off frequency given by:

$$f_T = \frac{g_m}{2\pi (C_{gs} + C_{gd})} \qquad 4\text{-}27$$

The other noise parameters are given by:

$$R_n = \frac{k_2}{g_m^2} \qquad 4\text{-}28$$

$$R_{opt} = k_3 \left(\frac{1}{4 g_m} + R_g + R_s \right) \qquad 4\text{-}29$$

and

$$X_{opt} = \frac{k_4}{f C_{gs}} \qquad 4\text{-}30$$

where, R_n = Noise resistance

R_{opt} = Optimum signal noise resistance

X_{opt} = Optimum signal noise reactance

k_1, k_2, k_3 and k_4 are the fitting factors chosen by Fukui [83, 84]:

$$k_1 = 0.016$$

$$k_2 = 0.030$$

$$k_3 = 2.2$$

$$k_4 = 160$$

All of the elements in Fukui's model are expressed in a simple analytical form. This makes it suitable for practical noise parameter extraction. This work, therefore,

adopted Fukui's model for pHEMT noise extraction. Similar to the linear and nonlinear modelling, this noise model is automated in ADS to reduce the complexity of noise the extraction technique.

Other prominent noise models were developed by Cappy [85] and Pospieszalski [86] which will be discussed briefly in this subsection.

4.6.2 Cappy's Noise Model

Cappy's noise model was developed by Alain Cappy in 1988 [85] and is similar to the Fukui's model. The noise parameters for Cappy's model are as follows:

$$F_{min} = 1 + 2\sqrt{P}\frac{f}{f_T}\sqrt{g_m\left(R_s + R_g\right)} \tag{4-31}$$

$$g_n = Pg_m\left(\frac{f}{f_T}\right)^2 \tag{4-32}$$

$$R_{opt} = \frac{1}{\omega C_{gs}}\sqrt{\frac{g_m\left(R_s + R_g\right)}{P}} \tag{4-33}$$

In the equation (4-31), term $2\sqrt{P}$ is comparable to Fukui's fitting factor, k_1 and given as:

$$P = \frac{I_{ds}}{\xi_c L_G g_m} \tag{4-34}$$

Where,

P = Dimensionless parameter close to 1-3 that depends on the device physical parameters and biasing conditions

I_{ds} = DC drain current

ξ_c = Critical electric field and

L_G = Gate length

4.6.3 Pospieszalski's Noise Model

Pospieszalski's noise model was developed by Marian W. Pospieszalski in 1989 [86]. This model was a new approach to Fukui's model since it was independent of noise sources. Figure 4-10 shows the Pospieszalski's model.

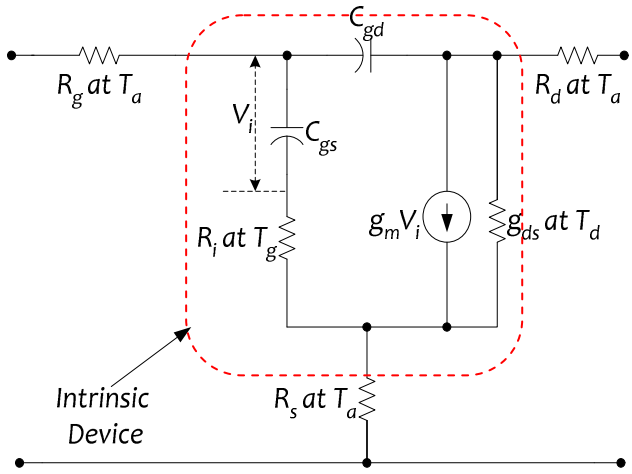


Figure 4-10 Pospieszalski's model

In this model, the noise parameters of the intrinsic device are expressed as a function of equivalent temperatures: T_g of R_i and T_d of g_d, while the noise properties of the Ohmic resistances, R_g, R_d and R_s are determined by the physical temperature T_a of the chip. The noise parameter expressions of this model are given as follows:

$$T_{min} = 2\frac{f}{f_T}\sqrt{g_{ds}R_i T_g T_d + \left(\frac{f}{f_T}R_i g_{ds} T_d\right)^2} + 2\left(\frac{f}{f_T}\right)^2 R_i g_{ds} T_d \qquad 4\text{-}35$$

$$R_n = \frac{T_g R_i}{T_a} + \frac{T_d}{T_a}\frac{g_{ds}}{g_m^2}\left(1 + w^2 C_{gs}^2 R_i^2\right) \qquad 4\text{-}36$$

$$R_{opt} = \sqrt{\left(\frac{f_T}{f}\right)^2 \frac{R_i}{g_{ds}}\frac{T_g}{T_d} + R_i^2} \qquad 4\text{-}37$$

And

$$X_{opt} = \frac{1}{\omega C_{gs}} \qquad 4\text{-}38$$

Fitting factors T_g and T_d are determined by measurement.

S. Arshad has proved that these models produced the same noise results as Fukui's noise model [60], with less than 0.1 dB difference. Therefore no noise comparison between the three models has been included in this project.

4.7 SUMMARY

In the LNA design process, accurate modelling for the active device is vital. Therefore, this chapter summarises the figures of merit for device modelling involved in designing a low noise amplifier (LNA). The models were discussed in detail since accurate models are necessary to realise well defined LNAs.

This chapter begins with the selection of appropriate biasing for active devices for low noise applications. The chapter then introduces the theoretical concept of the empirical linear and nonlinear models of a transistor. As the LNA designer is mainly concerned with absolute minimum noise, a detailed extracted transistor noise model used throughout this project is described. The results of linear and nonlinear modelling of the studied devices, as well as the selection of the epilayers will be discussed in Chapter 5.

CHAPTER 5

DEVICE FABRICATION AND MODELLING

5.1 INTRODUCTION

This chapter demonstrates the modelling of an in-house fabricated device based on the theoretical concepts explained in Chapter 3 and Chapter 4. The chapter begins with a description of the epitaxial layers that have been used in this work. Comparisons of the fabricated device's DC and RF characteristics of the selected epitaxial layers are then discussed. The chapter continues with modelling of the devices from the extracted parameters, where the linear and nonlinear models are presented and analysed. Figure 5-1 illustrates a workflow which summarises the steps involved in modelling a device.

A complete device modelling process begins with the selection of the epitaxial layer structure. This structure is then used for device fabrication, where large number processing steps are involved. After the devices have been through all of the processing steps, the DC and S-parameters measurements are performed to verify the device's performance. These parameter measurements are required for the next step of device modelling.

The device modelling task begins with the extraction of extrinsic and intrinsic parameters from the measured RF data. The initial linear model is then produced, after substitution of the measured extrinsic and intrinsic values, followed by tuning of the model's parameters until the S-parameters show an excellent agreement with the measured data. Next, the linear model is optimised in order to reduce the modelling error between measured and modelled data. After this, the nonlinear modelling is carried out, where the parasitic resistances from the linear model are substituted into the nonlinear model. The task continues with the fitting of DC and RF results with the measured data. During this process the nonlinear model is

constantly being optimised so that the modelling errors are reduced and finally the device model is completed.

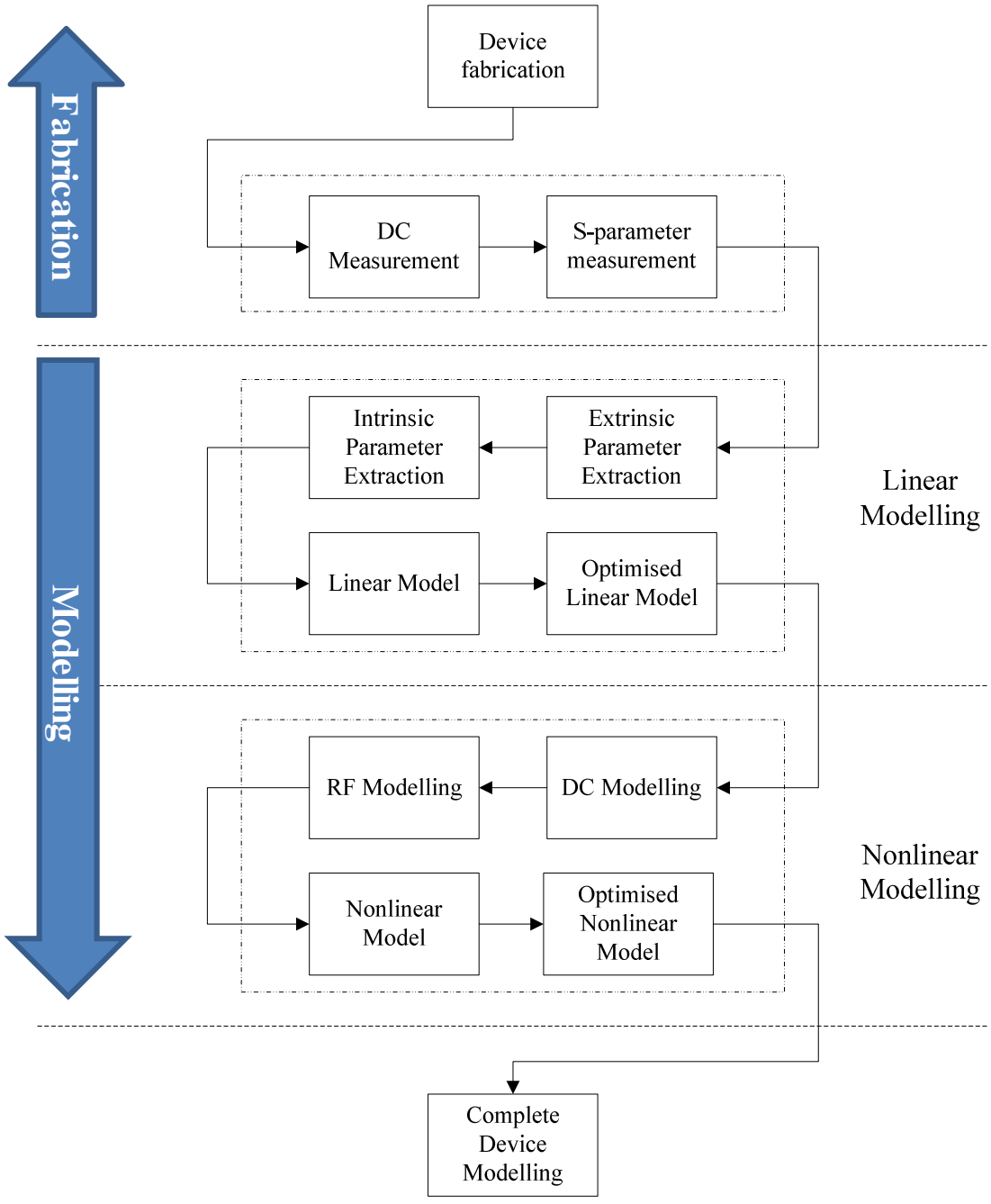


Figure 5-1 The complete flow of device modelling

5.2 EPITAXIAL STRUCTURES

In this work, a number of devices fabricated from three main types of epitaxial layer have been modelled for use in low noise applications. These devices can be divided into two main categories: (a) 1 μm gate length and (b) submicron (0.35 μm) gate length - to fulfil the low-noise requirements of SKA designs. Since the submicron devices were only recently developed and fabricated, the submicron discussion is limited to device modelling only. Thus, in this work, the 1 μm devices are the main subject of the discussions of LNA design. Three different epitaxial layers were investigated in this chapter, denoted as XMBE144, VMBE2100 and XMBE131.

All epitaxial layers were grown using in-house solid-source Molecular Beam Epitaxy (MBE) on RIBER V100H and V90H systems. The epitaxial structure with prefix VMBE indicates growth in the V90H system, whilst prefix XMBE denotes the growth was performed in the V100H system. These epitaxial layers were grown to improve the overall performance of the LNA through optimisation of the devices' epitaxial layers. Performance enhancement of XMBE144 and VMBE2100 was achieved through epitaxial layer improvements, resulting in low gate leakage and an improvement in the devices' thermal stability. Conversely, XMBE131 was grown to improve circuit low noise performance by means of gate scaling. The epitaxial structures are shown in Figure 5-2.

The epitaxial structures of XMBE 144 and VMBE2100 share almost the same epitaxy layers and thicknesses. The only different difference between the two materials is the that Schottky Barrier layer for VMBE2100 is made from highly strained, high band gap (~2.1 eV) material, which is advantageous for achieving a higher Schottky barrier height, and consequently leads to a lower gate leakage current. From these epitaxial layers, devices with 1 μm gate length (L_G) were fabricated.

Figure 5-2 also shows XMBE131, an epitaxial layer which was used for submicron devices. Its epilayers are made from a thin gate to channel distance and double δ-doped epilayer structures.

XMBE144	VMBE2100	XMBE131
(Cap) $In_{0.53}Ga_{0.47}As$ *50 Å*	(Cap) $In_{0.53}Ga_{0.47}As$ *50 Å*	(Cap) $In_{0.53}Ga_{0.47}As$ *50 Å*
(Barrier) $In_{0.52}Al_{0.48}As$ *300 Å*	(Barrier) $In_{0.3}Al_{0.7}As$ *300 Å*	(Barrier) $In_{0.52}Al_{0.48}As$ *150 Å*
δ	δ	δ1
(Spacer) $In_{0.52}Al_{0.48}As$ *100 Å*	(Spacer) $In_{0.3}Al_{0.7}As$ *100 Å*	(Spacer) $In_{0.52}Al_{0.48}As$ *100 Å*
(Channel) $In_{0.7}Ga_{0.3}As$ *140 Å*	(Channel) $In_{0.7}Ga_{0.3}As$ *160 Å*	(Channel) $In_{0.7}Ga_{0.3}As$ *160 Å*
(Buffer) $In_{0.52}Al_{0.48}As$ *4500 Å*	(Buffer) $In_{0.52}Al_{0.48}As$ *4500 Å*	(Spacer) $In_{0.52}Al_{0.48}As$ *100 Å* δ2 (Buffer) $In_{0.52}Al_{0.48}As$ *4500 Å*
(Substrate) InP Fe doped	(Substrate) InP Fe doped	(Substrate) InP Fe doped

Figure 5-2 Three different epitaxial layer structures for device under test

To minimise the undesired effects caused by device scaling, (such as channel length modulation), the aspect ratio between gate length and gate to channel distance must be greater than 5 [87]. The ratio between the 0.35 μm gate and gate to channel thickness for this epitaxial layer is shown in equation (5-1).

$$A = \frac{gate\ length}{gate\ to\ channel\ thickness} = \frac{350\ nm}{25\ nm} = 14 \qquad 5\text{-}1$$

Using the same formula, devices with gate lengths as small as 0.125 μm are still viable by using this epitaxial layer structure.

Double δ-doped structures also enhanced the carrier confinement in the quantum well, and additionally reduced the gate leakage to compensate for the thinner gate to channel thickness. The band structure and electron charge distribution for all three epitaxial layers structure was calculated using WinGreen simulator [88]. Parameters that need to be specified in WinGreen simulation tool are dielectric constant, Γ-valley electron effective mass, m_n^{Γ}, Γ-valley energy gap, E_g^{Γ}, hole effective mass and valence band discontinuity (ΔE_V) between heterojunctions. All these parameters were simulated under thermal equilibrium and varying biasing conditions. Results from the WinGreen simulation tool for all three epitaxial layers, at 0 V gate biasing, are shown in Figure 5-3, Figure 5-4 and Figure 5-5 respectively.

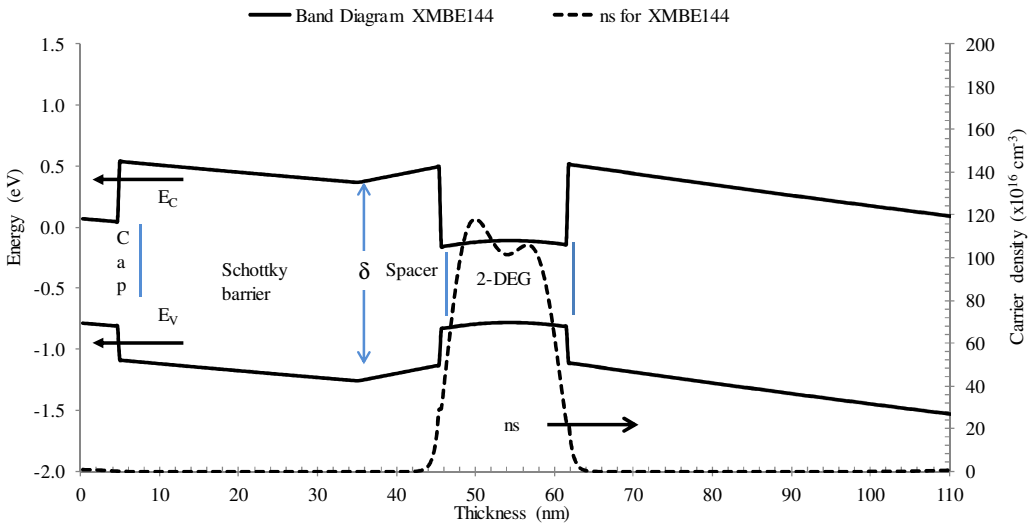


Figure 5-3 Energy band diagram and charge density for XMBE144

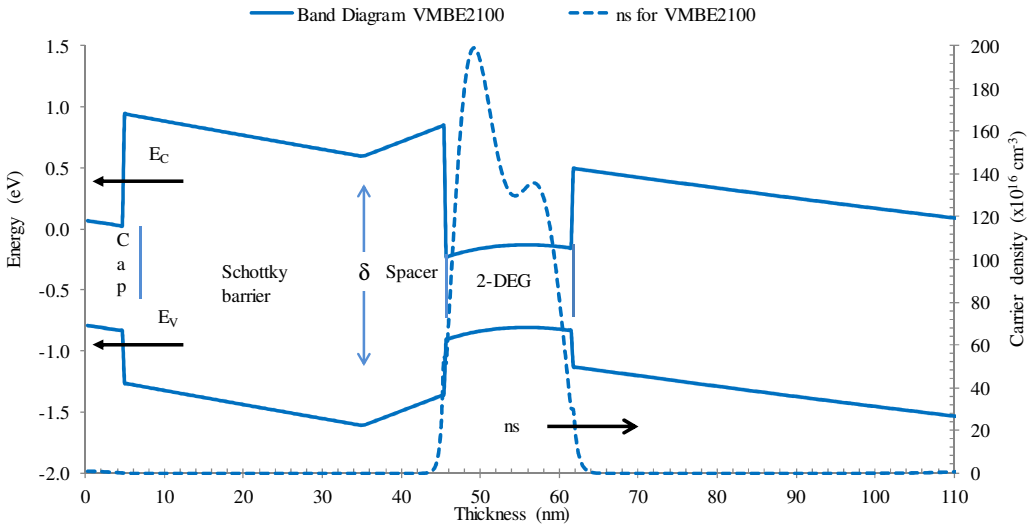


Figure 5-4 Energy band diagram and charge density for VMBE2100

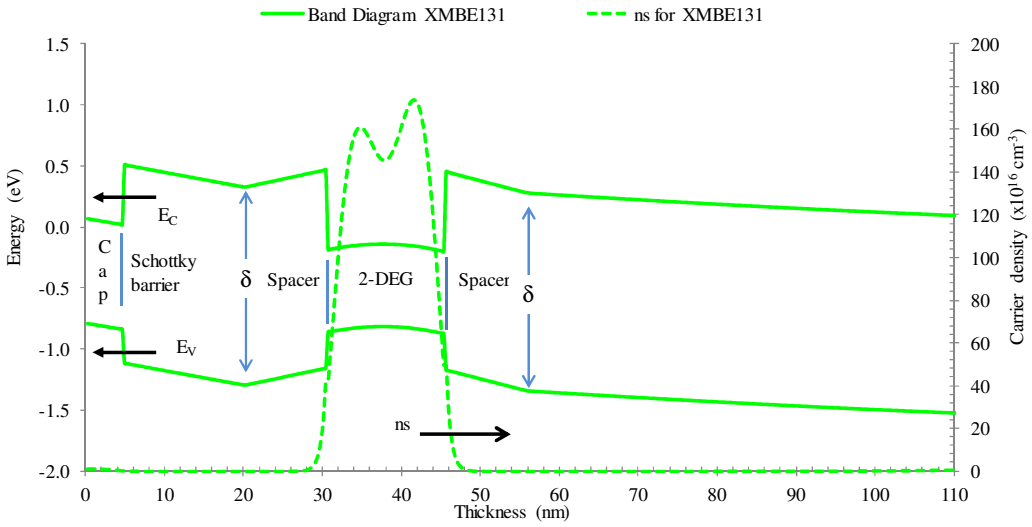


Figure 5-5 Energy band diagram and charge density for XMBE131

Comparing the energy band diagrams shown in Figure 5-3 and Figure 5-4, one can observe a significantly higher Schottky barrier height for the VMBE2100 epitaxial layer as compared to XMBE144. This results from utilising a very large band gap barrier layer to the highly tensile strained $In_{0.3}Al_{0.7}As$ materials. The carrier density of the 2DEG is significantly higher in VMBE2100 as a result of the higher spacer

layer potential barrier and the deeper quantum well. Therefore, the gate leakage in VMBE2100 devices will be notably lower than that of XMBE144, this is seen in the measured DC characteristics (see section 5.4)

By referring to Figure 5-3 and Figure 5-5, the barrier height for XMBE131 and XMBE144 are almost the same, since similar material is used for the Schottky barrier layer. However, XMBE131 is seen to have a thinner gate to channel distance, since the epitaxy layer is designed for submicron devices. Furthermore, the carriers are more confined in the quantum well, as a result of the double δ-doped structure.

The Hall measurement data at 300 K and 77 K for all epitaxial layers is shown in Table 5-1. From the table, the sheet carrier concentration is higher in VMBE2100 and XMBE131, as a consequence of better carrier confinement in both epitaxial layers. As previously mentioned, the carrier confinement in VMBE2100 is attained by using a deeper quantum well, resulting from the wider bandgap material at the Schottky and spacer layer. In the case of XMBE131, the carrier confinement is achieved by adapting the almost square-shaped quantum well, resulted from the double δ-doped structure.

Table 5-1 Hall measurement data at 300 K (room temperature) and 77 K

Hall Data	**XMBE144**	**VMBE2100**	**XMBE131**
Sheet Carrier Concentration (n_H) at 300 K / 77 K (x 10^{12} cm^{-2})	1.74 / 2.06	2.50 / 2.60	2.4 / 2.5
Hall Mobility (μ_H) at 300 K / 77 K (cm^2 / V.s)	12,850 / 48,800	12,982 / 46,390	13,896 / 47,829

From the Table 5-1, one can also observe that the carriers' mobilities are comparable with each other in all three epitaxial structures. This is predominantly due to the use of the same highly strained $In_{0.7}Ga_{0.3}As$ in the channel material. Referring back to Figure 5-2, the carriers in the 2DEG are separated by the same spacer thickness (100 Å) in all epilayer structures. Therefore the Columbic interaction between the electrons and ionised donor atoms at the δ-doped layer are almost the same, and consequently comparable carrier mobilities are recorded in all epitaxial layers.

Investigation of the advantages of each epitaxial layer, in terms of the variation of barrier height, carrier concentration and carrier confinement was completed by the fabrication of transistors with a range of device widths. Several devices with multiple gate fingers and with gate length of 1 μm (L_G = 1 μm) were fabricated on XMBE144 and VMBE2100 epitaxial layers, whereas submicron devices with L_G = 0.35 μm were fabricated using the XMBE131 epitaxial layer. The devices' DC and RF characteristics were then modelled, prior to their use in the Low Noise Amplifier (LNA) designs.

5.3 FABRICATION STEPS

The block diagram of the fabrication process for the pHEMT devices is shown in Figure 5-6. The diagram shows the general fabrication steps involved for both the 1 μm and 0.35 μm submicron gate devices.

However, there is one major difference between the 1 μm processing gate steps and the submicron gate processing steps. For the 1 μm gate, the gate opening is achieved through an optical lithography process using high grade AZnLOF 2070 resist, before the cap layer at the opening was etched away by a highly selective succinic acid etchant. Following this, the gate terminal was formed by a thermal evaporation process. An illustration of the fabrication steps for four gate fingered devices can be found in Appendix C.

More complicated processing steps are involved in the formation of the submicron gate length. In this process, the submicron-sized opening was realised by an optical lithography process, used to form the initial gate opening on 90 nm thick Silicon

Nitride layer covering the sample surface. The gate opening size was then further reduced by a soft reflow process, where an evaporated solvent vapour was used to soften, and at the same time reduce, the gate opening size. Next, the submicron footprint was formed by a dry etching process in a plasma etching chamber. The resist was then dried by baking the sample on a hot plate. This process consequently made the gate opening larger and formed a T-gate. A Ti/Au metal scheme was then deposited by a thermal deposition process. The remaining processing steps were similar to the conventional pHEMT processing steps.

A picture of 4 x 200 μm with L_G = 1 μm is shown in Figure 5-7, while Figure 5-8 shows an illustration of the submicron device with a T-gate structure.

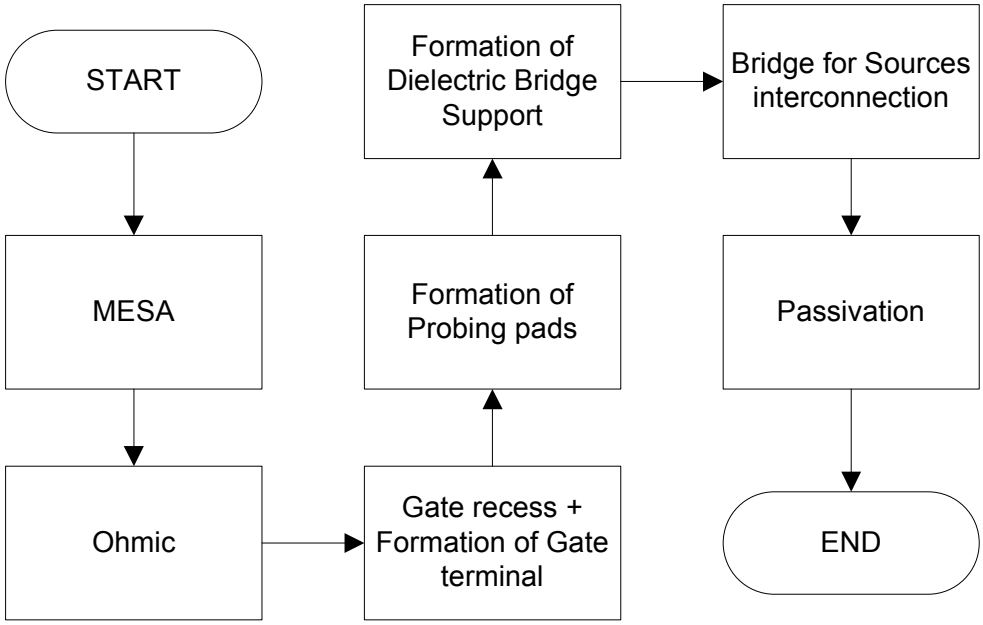


Figure 5-6 Fabrication process for conventional pHEMT process

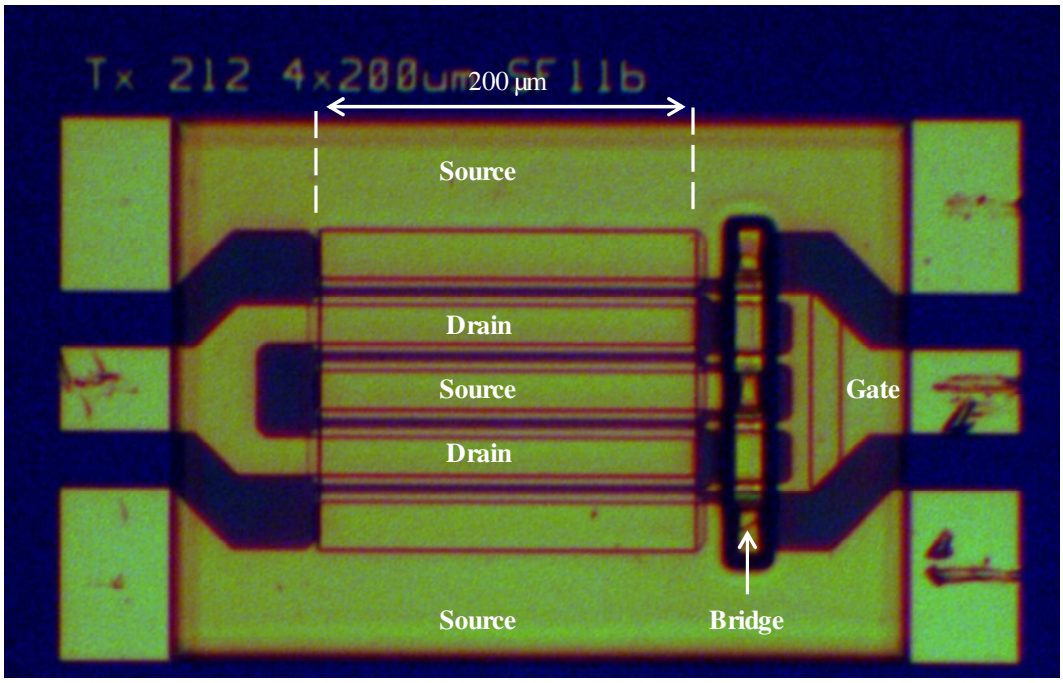


Figure 5-7 Picture of 4 x 200 µm gate width device with L_G = 1 µm.

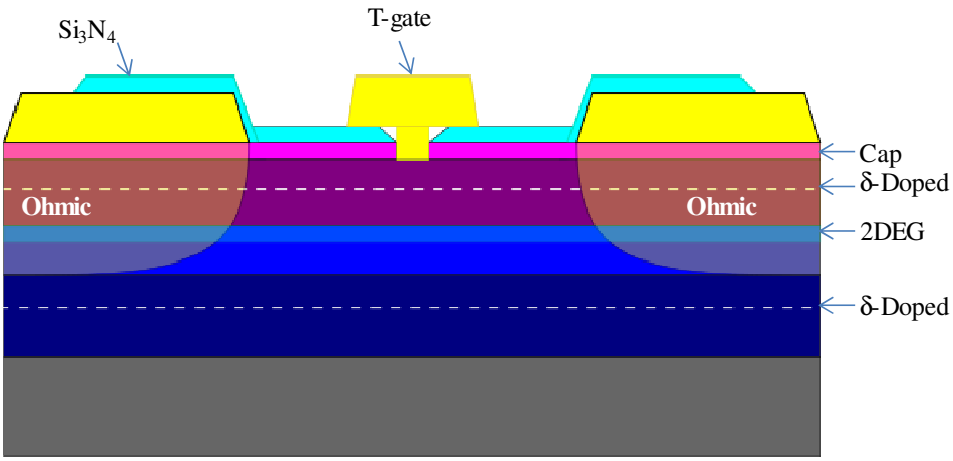


Figure 5-8 An illustration of a submicron device with a T-gate structure. The T-gate foot print is ~0.35 µm. (Thickness not to scale)

In this work, a very large number of devices were fabricated and characterised. The devices are summarised in Table 5-2. All devices have 5 µm source-to-drain (S-D) terminal distances. However, for presentation purpose, only a selected number of devices are detailed in this chapter. The remainder of the devices are shown only in

the summary of each section. Three types of devices, with two and four gate fingers, and with different gate widths, are shown for the XMBE144 epitaxial layer, whereas only 4 x 200 μm gate width devices were fabricated and modelled from VMBE2100. Conversely, devices with two gate widths are shown for XMBE131.

Table 5-2 Summary of the fabricated and modelled devices

W_T = Devices' total width and S-D = 5 μm

Epitaxial layer	Device width	Gate length	Note
XMBE144	2 x 50 μm (W_T = 100) 2 x 100 μm (W_T = 200) 4 x 200 μm (W_T = 800)	1.00 μm	Low gate leakage epitaxial layer
VMBE2100	4 x 200 μm (W_T = 800)	1.00 μm	Extremely low gate leakage epitaxial layer
XMBE131	2 x 50 μm (W_T = 100) 2 x 200 μm (W_T = 400)	0.35 μm	Submicron epitaxial layer

5.4 DC AND RF CHARACTERISTICS

In this section, the DC and RF characteristics from the devices fabricated on all three epitaxial layers are presented. As listed in

Table 5-2, six families of devices were successfully fabricated and measured. Thus, for data presentation purposes, only samples of the largest device from each epitaxial layer are discussed. For XMBE144 and VMBE 2100, only 4 x 200 μm devices are presented and 2 x 200 μm devices are selected from XMBE131. The emphasis on large gate width devices will become obvious when the design of broadband LNAs is undertaken; for broadband matching, a low noise resistance is needed, which require large gate width transistors. The measured parameters for these devices were extracted using the Agilent Integrated Circuit Characterisation and Analysis Program (ICCAP). ICCAP is a powerful program used to analyse device performance. It

provides a simple extraction module for DC-IV characteristic and S-parameters data [89].

5.4.1 On-state Leakage Currents

The on-state leakage for 4 x 200 µm devices using XMBE144 and VMBE2100 epitaxial layers are depicted in Figure 5-9.

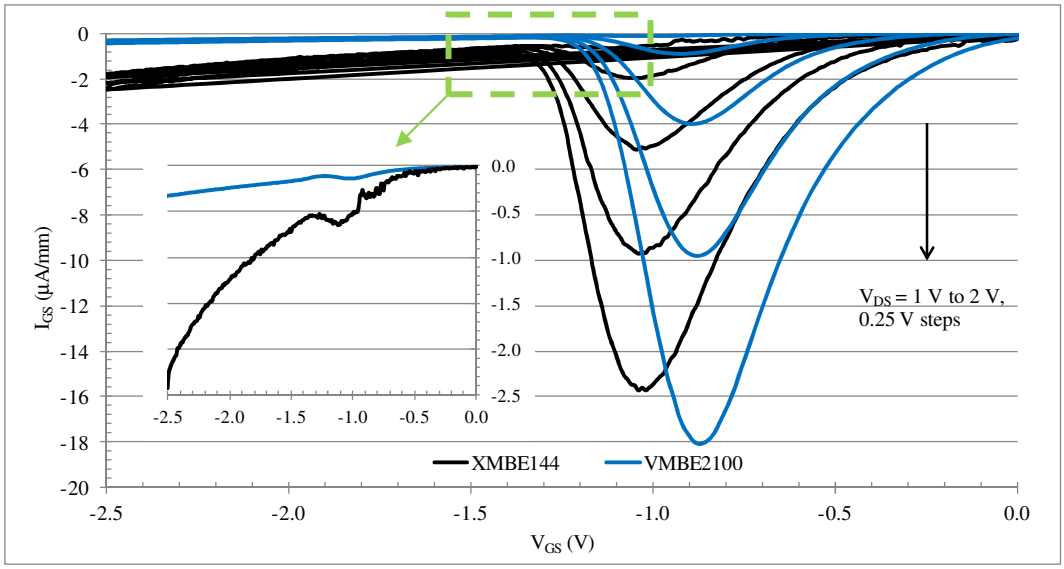


Figure 5-9 On-state leakage current for XMBE144 and VMBE2100. Inset is the on-state leakage current of V_{DS} = 1 V (4 x 200 µm devices)

In the Figure 5-9, one can observe gate leakage caused by tunnelling and impact ionisation. Below the threshold voltage (V_{th}), the device is OFF and the leakages are due to carriers tunnelling through the Schottky barriers. Above V_{th}, the devices are ON and the leakage is mainly due to impact ionisation, where carrier multiplication takes place and a bell-shaped current profile is measured. The V_{th} values for XMBE144 and VMBE2100 are approximately -1.3 V and – 1.2 V respectively.

From this figure, it is obvious that the VMBE2100 device's leakage current due to tunnelling is significantly reduced at all V_{DS} bias values through the adoption of a wider band gap material as the Schottky barrier layer. The gate leakage for a V_{DS} bias equal to 1 V at V_{GS} = -2.5 V is shown as inset in Figure 5-9. This is the V_{DS} biasing method that is used in all the LNA circuit designs described in this thesis.

Here, a small leakage current of -0.3 µA/mm is recorded for VMBE2100, whereas the gate leakage for XMBE144 has a higher value of -2.3 µA/mm.

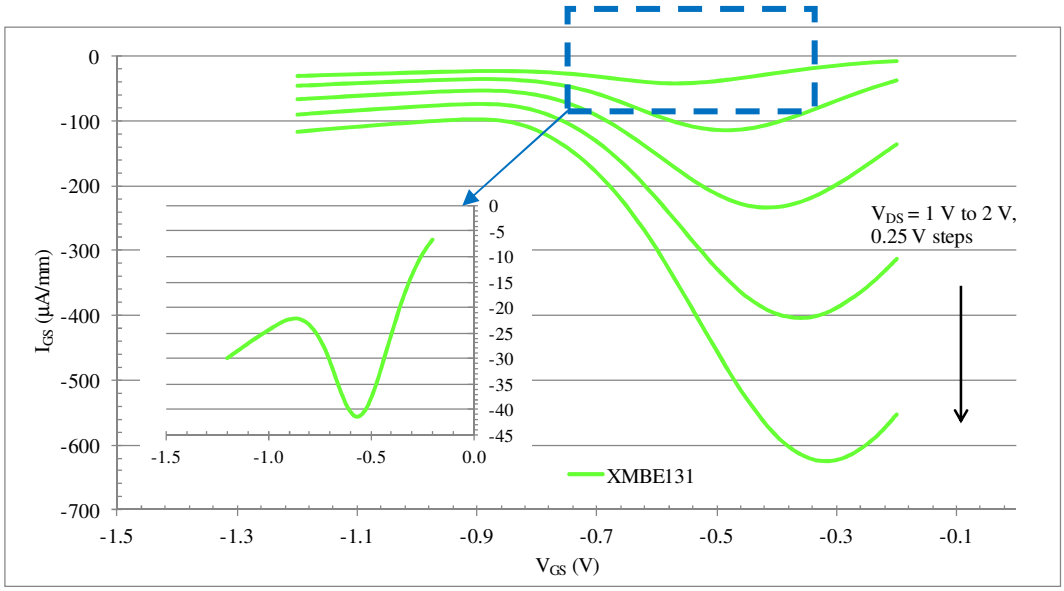


Figure 5-10 On-state leakage current for XMBE131. Inset is the on-state leakage current of V_{DS} = 1 V (2 x 200 µm devices)

Figure 5-10 depicts the bell-shaped on-state leakage current for the submicron device (L_G = 0.35 µm and W_T = 2 x 200 µm) using the XMBE131 epitaxial layer. Clearly, this device has a notably higher leakage current than either XMBE144 or VMBE2100. For example, at V_{DS} = 1 V, the maximum gate leakage due to impact ionisation is –43 µA/mm, more than 100 times higher than the maximum gate leakage of the XMBE144 or VMBE2100 samples. For other V_{DS} biasing levels, the maximum gate leakage is considerably higher. The high gate leakage is one of the disadvantages of this type of epitaxial layer when the gate to channel distance is very small.

The V_{th} for this epitaxial layer is also shifted to a more positive value, as expected. In this epitaxial layer, due to the thin Schottky barrier and spacer layers, the distance from gate to channel is shorter. Thus the depletion region under the gate terminal, which already exists when the gate bias is 0 V, will grow wider as the reverse bias

gate voltage is increased. As a result, a smaller negative gate voltage is needed to pinch the channel and consequently turn OFF the device. The V_{th} for XMBE131 is approximately -0.8 V.

5.4.2 Transconductance

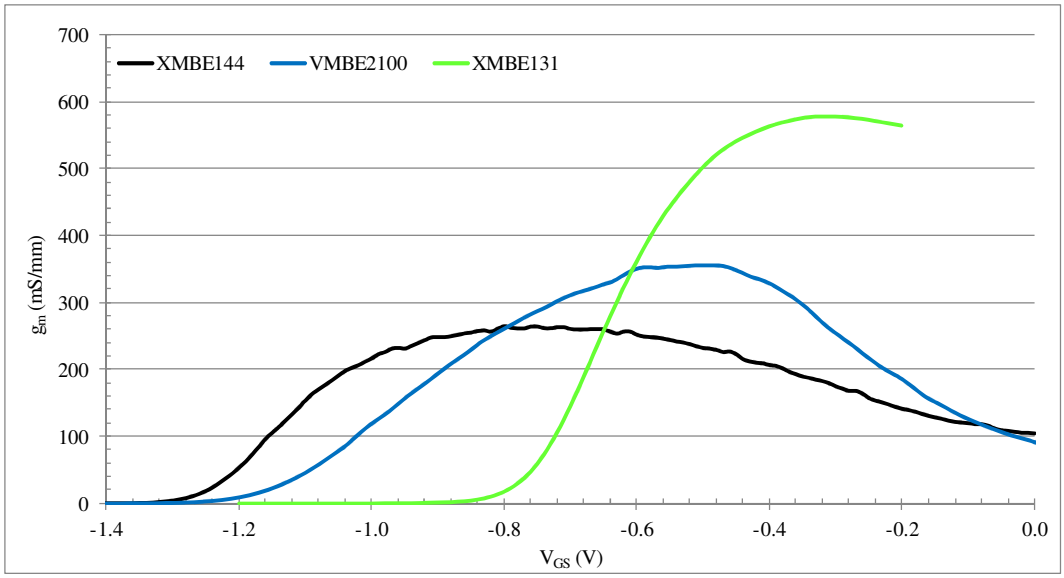


Figure 5-11 Comparison of transconductance for XMBE144 (4 x 200 µm) , VMBE2100 (4 x 200 µm) and XMBE131 (2 x 200 µm) at V_{DS} = 1 V

The variations in transconductance (g_m) between the devices at V_{DS} = 1 V are depicted as Figure 5-11. Comparing XMBE144 and VMBE2100, the peak g_m (g_{m_max}) for VMBE2100 is considerably higher. This is because, for the VMBE2100 sample, the carrier concentration is higher, which means more electrons are available for current conduction, and consequently the output current is increased. Since g_m is directly proportional to the rate of change of I_{DS}, VMBE2100's g_m is increased, as illustrated in Figure 5-11.

Another important finding in Figure 5-11 is the superior recorded g_m value for sample XMBE131. The increase of g_m is related to the increase in I_{DS} value due to the smaller L_G size and the smaller gate to channel distance. As previously stated, the I_{DS} current in both the linear and saturation region is inversely proportional to the device's gate length.

5.4.3 Output Characteristics

The output characteristics from these epitaxial layers (XMBE144, VMBE2100 and XMBE131) are shown in Figure 5-12, Figure 5-13 and Figure 5-14 respectively.

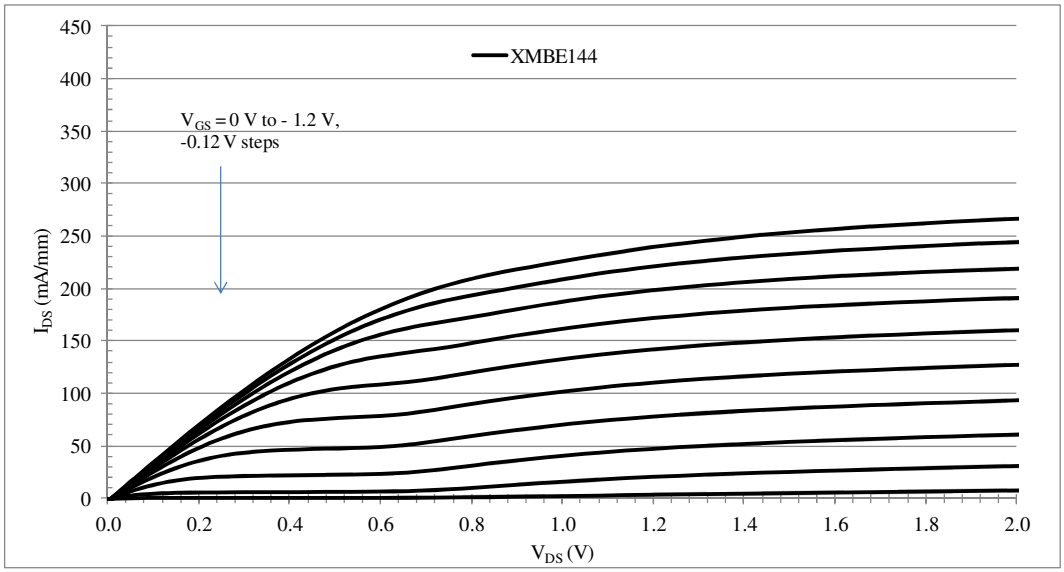


Figure 5-12 Output current characteristic for XMBE144, device 4 x 200 µm

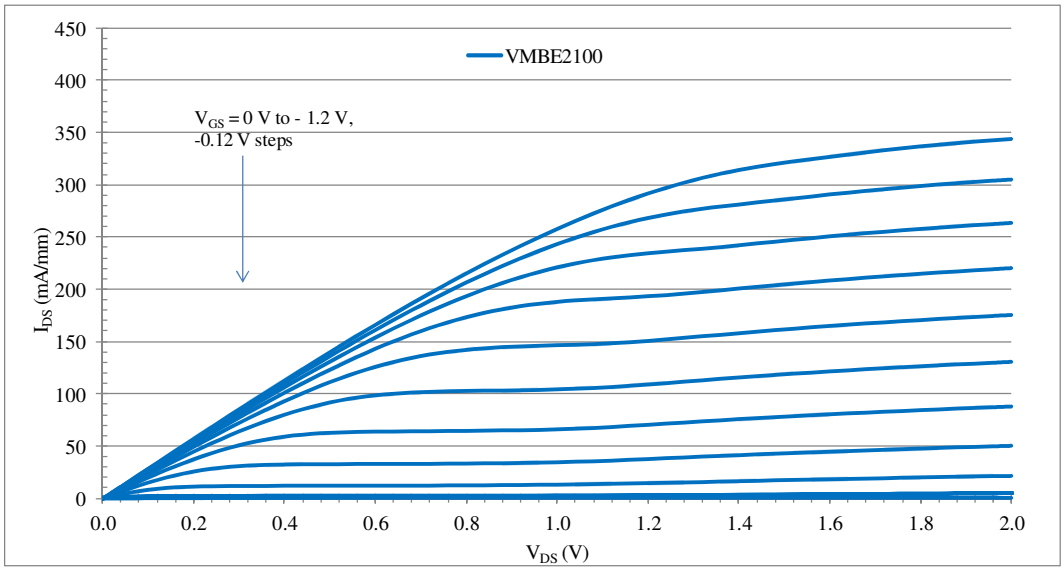


Figure 5-13 Output current characteristic for VMBE2100, device 4 x 200 µm

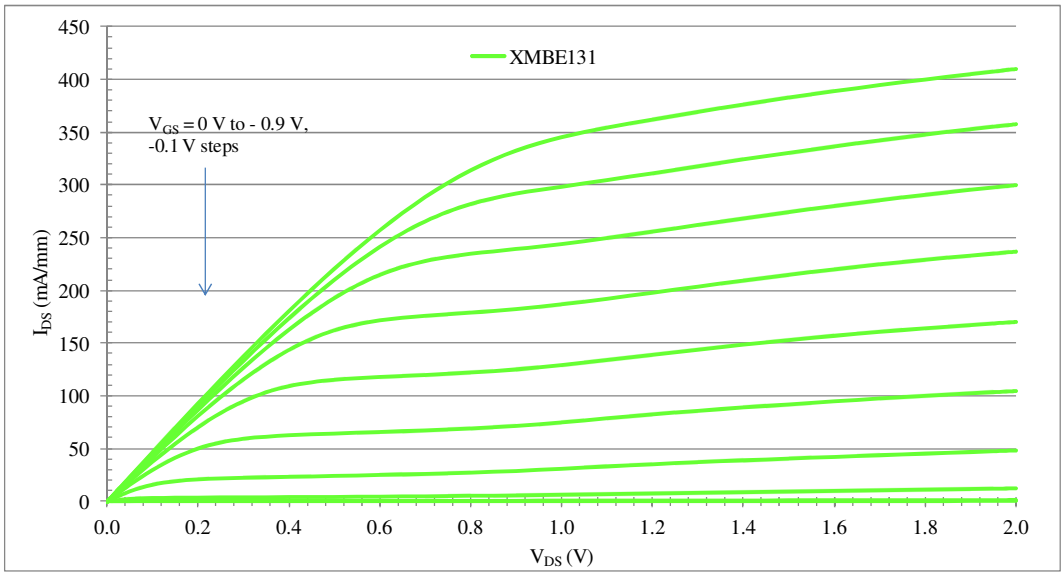


Figure 5-14 Output current characteristic for XMBE131, device 2 x 200 µm

From these figures, the XMBE144 sample has the lowest output current due to its lower carrier concentration. The output current from XMBE131 has the highest value because of its high carrier concentration in the channel, as well as its smaller device gate length. The maximum output currents at V_{DS} = 2 V are 266 mA/mm, 344 mA/mm and 410 mA/mm for XMBE144, VMBE2100 and XMBE131 respectively.

5.4.4 RF Characteristics

Figure 5-15 is a plot of the unity current gain (h21) versus frequency for the three devices. Their cut-off frequencies (f_T) are defined as the frequency at which the h21 plots cross the 0 dB line. In the figure, f_T for XMBE144 and VMBE2100 are ~ 21 GHz. Since f_T is inversely proportional to gate length (L_G), the submicron device shows superior RF performance - an f_T ~ 55 GHz is obtained. A high f_T device is a promising component for the LNA design as it will have a reduced noise figure.

The DC and RF data are now ready for use in the linear modelling stage (refer to Figure 5-1).

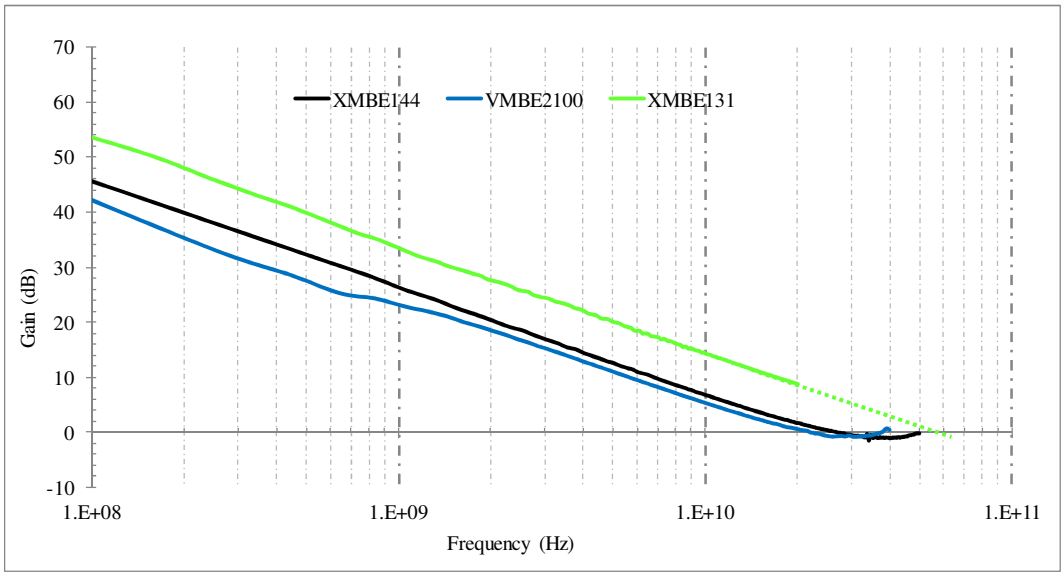


Figure 5-15 Unity current gain (h21) plot versus frequency at VDS = 1 V. The cut-off frequency (f_T) is obtained by the 0 dB crossing at x-axis (frequency)

5.5 DEVICE MODELLING

Extensive explanations and derivations of each part of the device's empirical model have been previously highlighted in Chapter 4, section 4.4. Therefore, this section will use these theoretical concepts to model the studied devices.

The device modelling can be divided into linear modelling and nonlinear modelling phases. The linear modelling phase begins with the extraction of extrinsic and intrinsic parameters from pinched and biased dependent S-parameter measurements, from which the initial linear model (non-optimised empirical model) is generated. This model is then optimised by fitting the modelled and measured S-parameters data. This will consequently reduce the modelling error. Nonlinear modelling of the devices is then performed; the DC and RF data are extracted, modelled and optimised. After the nonlinear model has been optimised, the complete model is ready to be used in circuit designs.

In this work, multiple device sizes from each epitaxial layer have been modelled. Since the model output data has a large number of parameters, only data from the

XMBE144 4 x 200 µm device are presented. However, the complete modelling data for the remaining devices are summarised at the end of this section.

5.5.1 Linear Modelling

The S-parameter measurements are firstly exported from the ICCAP to the ADS software, where the linear model is created. The configuration of the transistor's linear model begins with the extraction of extrinsic parameters, followed by the intrinsic parameters. The extrinsic parameters are obtained from the device's pinched (cold) S-parameters measurement. This measurement is made when the device's channel is totally pinched, and it is bias-independent. The ADS setup for the cold model is depicted in Figure 5-16.

Conversely, the intrinsic parameters extraction can be obtained from the bias dependent (hot) measurement. For example, the device is biased in the low power and low noise region, where V_{DS} = 1 V and I_{DS} = 10 % I_{DSS}. The biasing points for all of the studied devices are tabulated in Table 5-3. The setup for the hot model is illustrated in Figure 5-17.

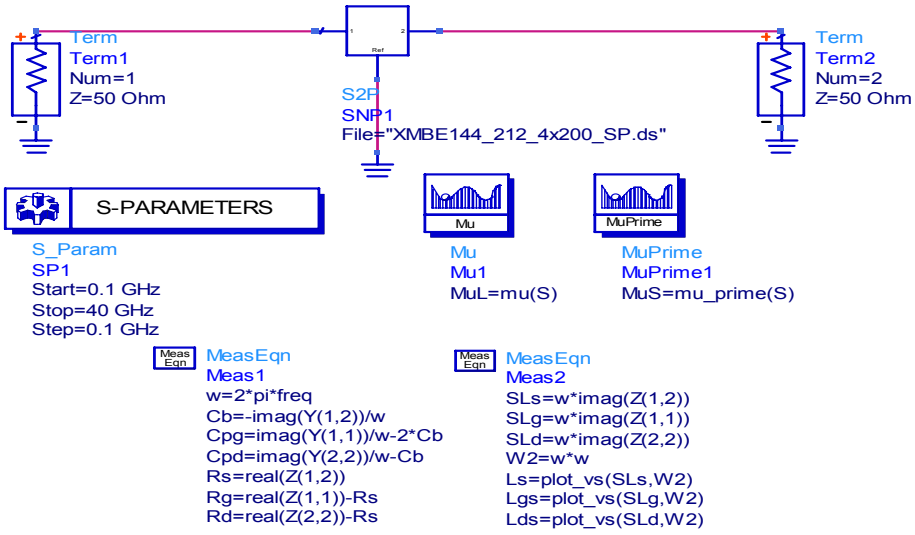


Figure 5-16 Parameter extraction for Cold measurement (XMBE144's 4 x 200 µm)

Table 5-3 Table of biasing point for devices on sample XMBE144, VMBE2100 and XMBE131

Epi. layer	Gate fingers x widths (μm)	V_{DS} (V)	I_{DS} (mA)	V_{GS}(V)
XMBE144	2 x 50	1	2	-0.72
	2 x 100	1	5	-0.81
	4 x 200	1	20	-0.75
VMBE2100	4 x 200	1	22	-0.92
XMBE131	2 x 50	1	4	-0.55
	2 x 200	1	15	-0.56

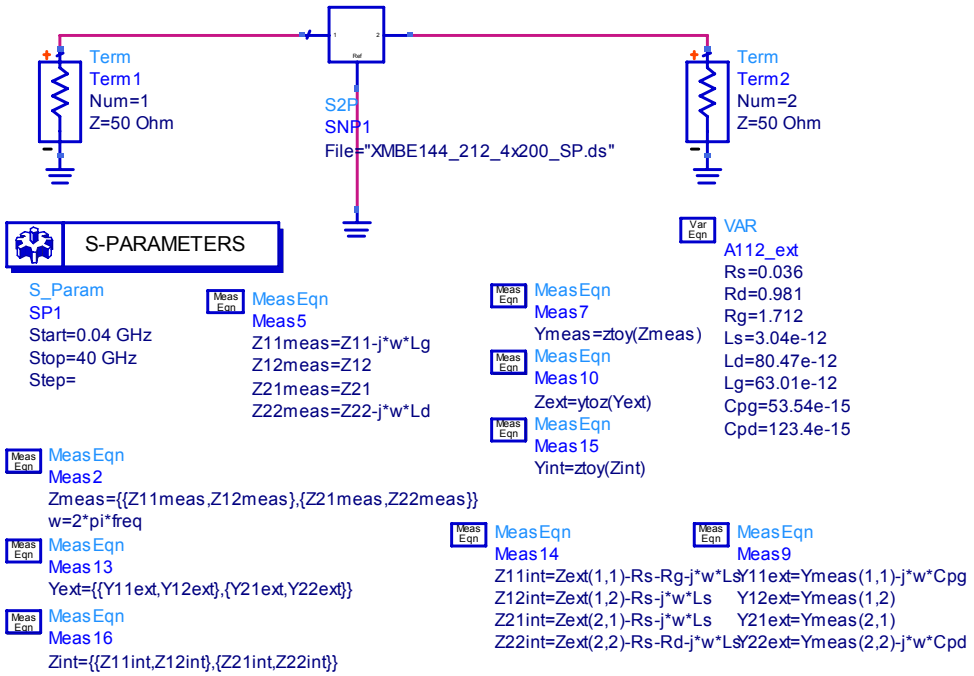


Figure 5-17 Parameter extraction for Hot measurement

(XMBE144's 4 x 200 μm device at V_{DS} = 1 V, 10 % I_{dss})

The extracted parameters were then substituted into the linear model to obtain the simulated S-parameters. The setup for the linear model is depicted in Figure 5-18.

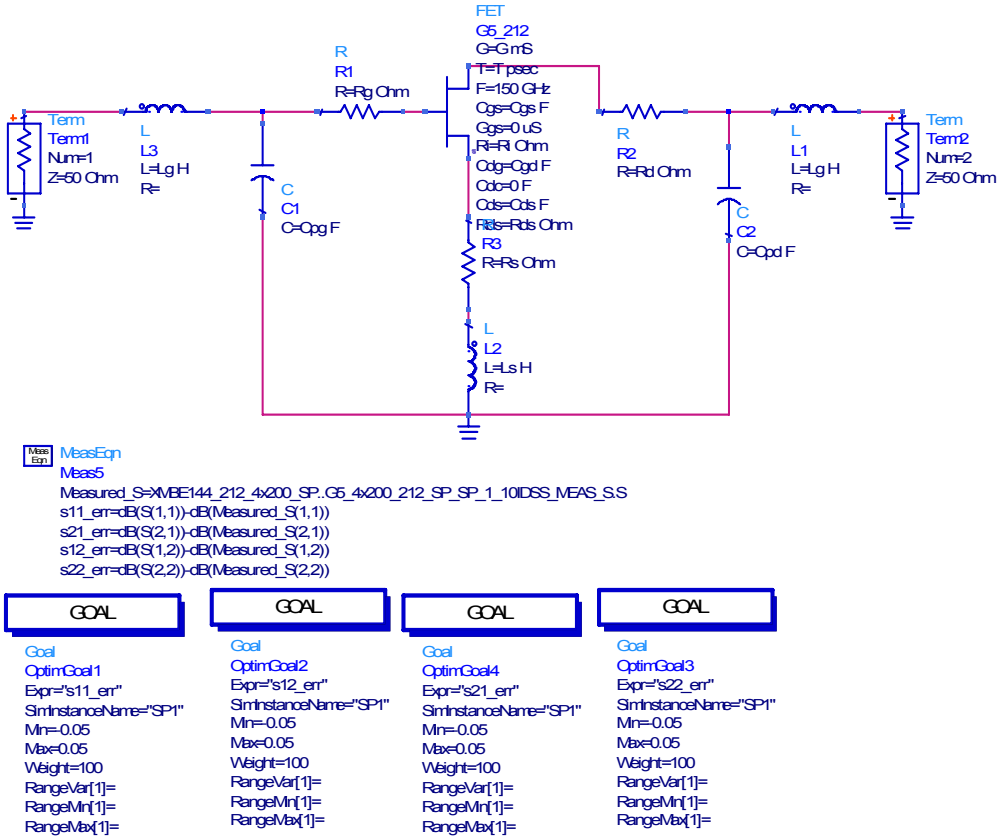


Figure 5-18 The setup for Linear Model for XMBE144's 4 x 200 µm device for V_{DS} = 1 V, 10 % I_{dss}

The simulated S-parameters are tuned to match the measured S-parameters. The model's S-parameters data are then fine tuned further using the ADS optimiser to reduce the errors in the parameters. The setup for the linear model optimisation is shown in Figure 5-19. As shown in the diagram, the setup is formed from a combination of several linear models, developed from several bias-dependent measurements as previously shown.

Following the linear model optimisation, the linear modelling process is complete. Figure 5-20 shows the empirical model with the optimised extrinsic and intrinsic values for the XMBE144 4 x 200 µm device. The S-parameter data is depicted in Figure 5-21, where the modelled data shows a good fit to the measured data up to a frequency of 10 GHz.

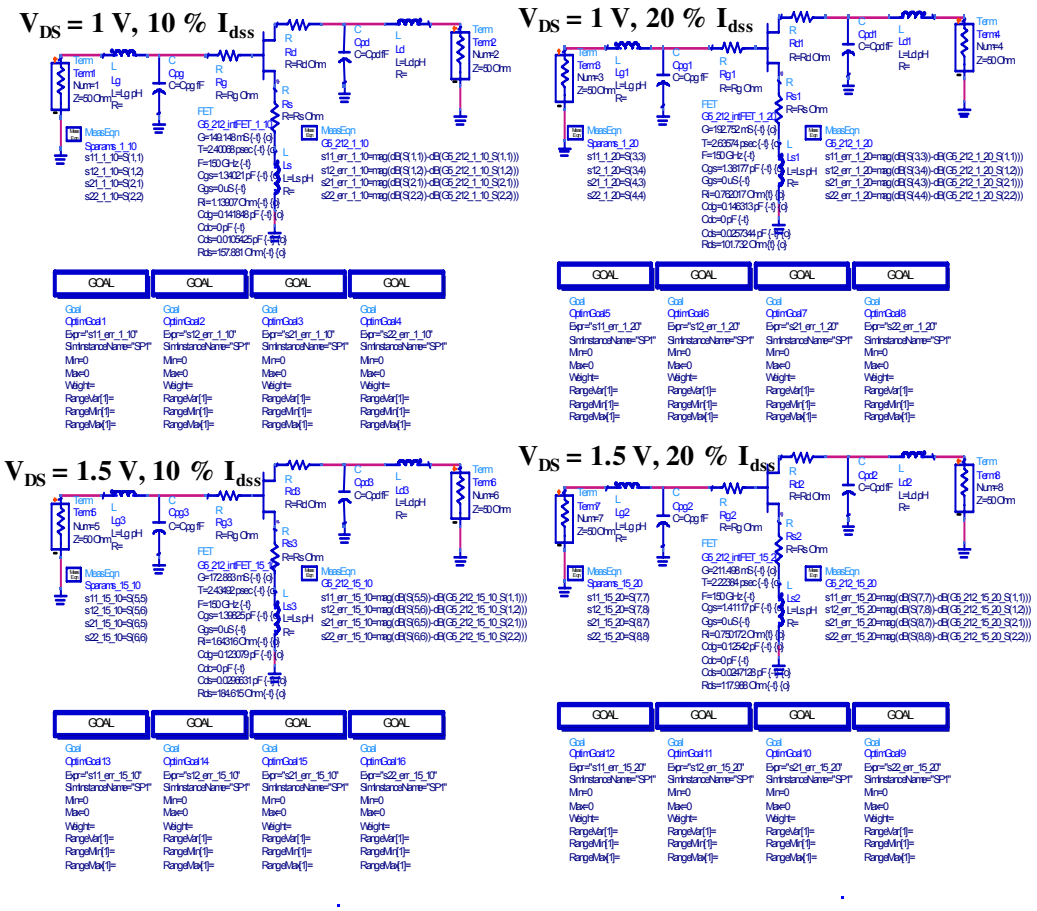


Figure 5-19 The optimisation setup for XMBE144's 4 x 200 µm Linear Model

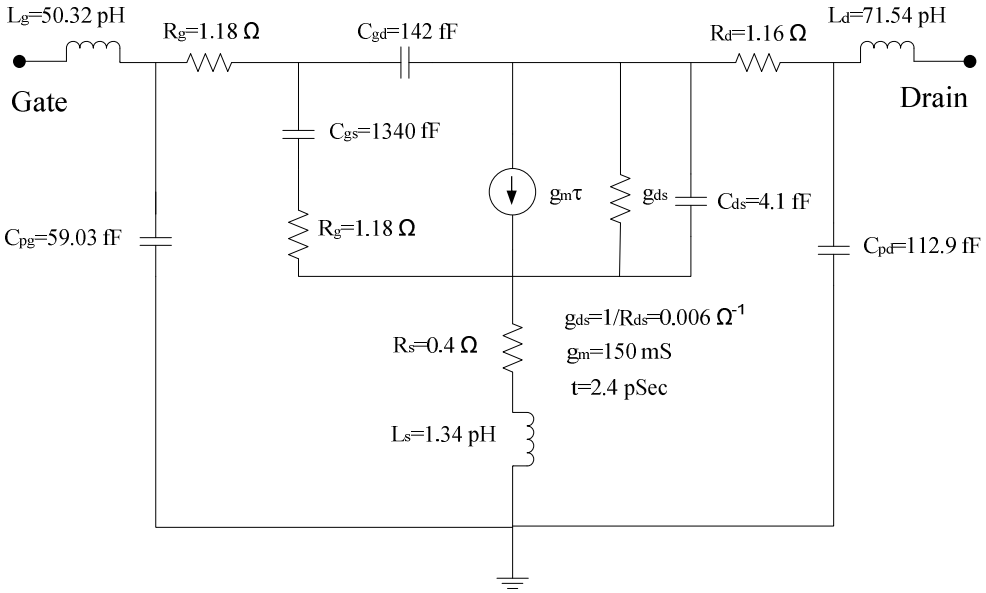
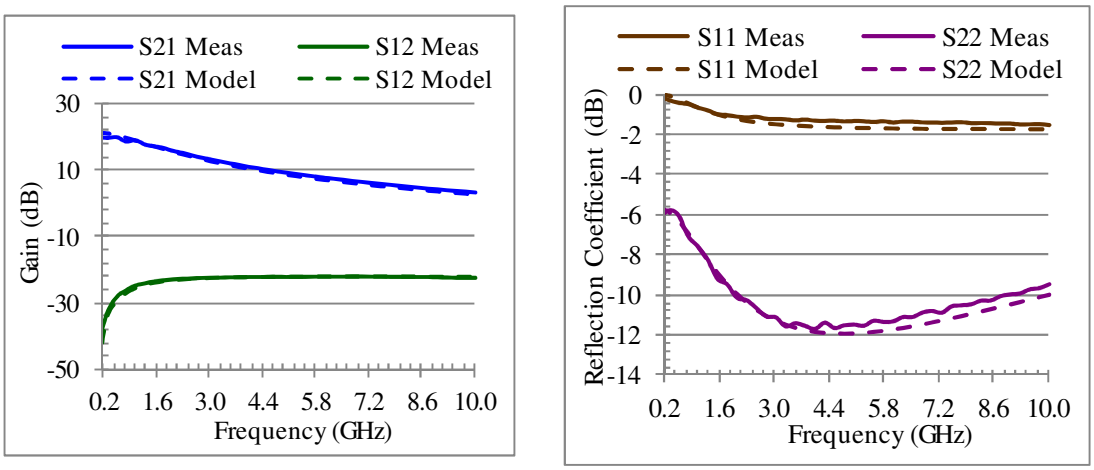


Figure 5-20 The optimised Linear Model (with extrinsic and intrinsic values) for the XMBE144 4 x 200 µm device



(a) (b)

Figure 5-21 The matched S-parameter data after Linear Model optimisation for XMBE144's 4 x 200 µm device. (a) S21 and S12 and (b) S11 and S22

Table 5-4 summarised the extrinsic parameters value for all devices involved in this work.

Table 5-4 Table of extrinsic parameters for all devices at V_{DS} = 1 V and 10% I_{dss}

Sample ID	Gate fingers x widths (µm)	C_{pg} (fF)	C_{pd} (fF)	R_s (Ω)	R_g (Ω)	R_d (Ω)	L_s (pH)	L_g (pH)	L_d (pH)
XMBE144	2 x 50	7.8	26.6	5.80	1.94	2.91	8.1	20.5	17.9
	2 x 100	13.7	37.9	1.99	1.44	1.38	3.9	26.7	56.1
	4 x 200	59.0	112.9	0.40	1.18	1.16	1.3	50.3	71.5
VMBE2100	4 x 200	40.1	155.6	0.53	1.56	1.43	2.0	79.7	111.6
XMBE131	2 x 50	9.0	38.1	0.50	1.53	0.60	1.9	34.0	93.2
	2 x 200	74.6	114.9	0.80	1.50	0.80	20.2	34.4	96.5

From the Table 5-4, one can see that the capacitance values increase as the total device width is increased. Since the capacitance value is proportional to the contact area, the capacitance increases as the contact pad areas become larger.

It can also be seen from Table 5-4, that the terminal resistances are also reduced as the device size is increased. As the gate width is increased, the total gate area will increase, and consequently it will decrease the terminal resistances. The submicron devices show comparable gate resistances due to the implementation of a T-gate structure as the gate terminal. For the same device width, the VMBE2100 device shows comparable data to the XMBE144 device.

The intrinsic parameters for all devices are shown in Table 5-5.

Table 5-5 Table of intrinsic parameters for all devices at V_{DS} = 1 V and 10% I_{dss}

Sample ID	Gate fingers x widths (μm)	g_m (mS)	τ (psec)	R_i (Ω)	R_{ds} (Ω)	C_{gs} (fF)	C_{ds} (fF)	C_{gd} (fF)
XMBE144	2 x 50	19	1.71	9.42	1318.9	150	1.7	22
	2 x 100	50	1.77	3.89	681.3	410	2.6	43
	4 x 200	150	2.40	1.14	157.9	1340	4.1	142
VMBE2100	4 x 200	170	1.17	2.42	179.0	1400	3.0	150
XMBE131	2 x 50	63	0.32	0.20	386.8	130	12.8	30
	2 x 200	230	0.81	1.26	65.0	700	194	210

The intrinsic parameters follow the same trend as the extrinsic values as the device width is increased. However, a significant reduction in R_{ds} values can be observed as the device width is increased. This resistance can also be viewed as the resistance in the channel between the Drain and Source terminals. As the device width is increased, the total area involved in parallel with the device width will be increased, and consequently the channel resistance is reduced.

At this stage, the linear model is complete and ready for the nonlinear model.

5.5.2 Nonlinear Modelling

The nonlinear modelling begins with the development of the DC and RF models. In this project, an Anritsu 37396 Vector network Analyser and an HP4142B modular DC Source/Monitor were used to characterise the DC and RF parameters. Both measurements were performed using the Agilent ICCAP [90] software.

5.5.2.1 DC Models

To develop the DC model, firstly the R_s, R_d and R_g resistances obtained from the linear model are substituted into the ADS EE-HEMT model. The drain-source parameters and g_m compression parameters are then extracted from the measured g_m versus V_{GS} value as illustrated in Figure 5-22. These parameters provide the starting point for the nonlinear device model. The parameters are then tuned for optimum fit between the measured and modelled DC characteristics. Figure 5-23 shows the modelling setup for the DC Model.

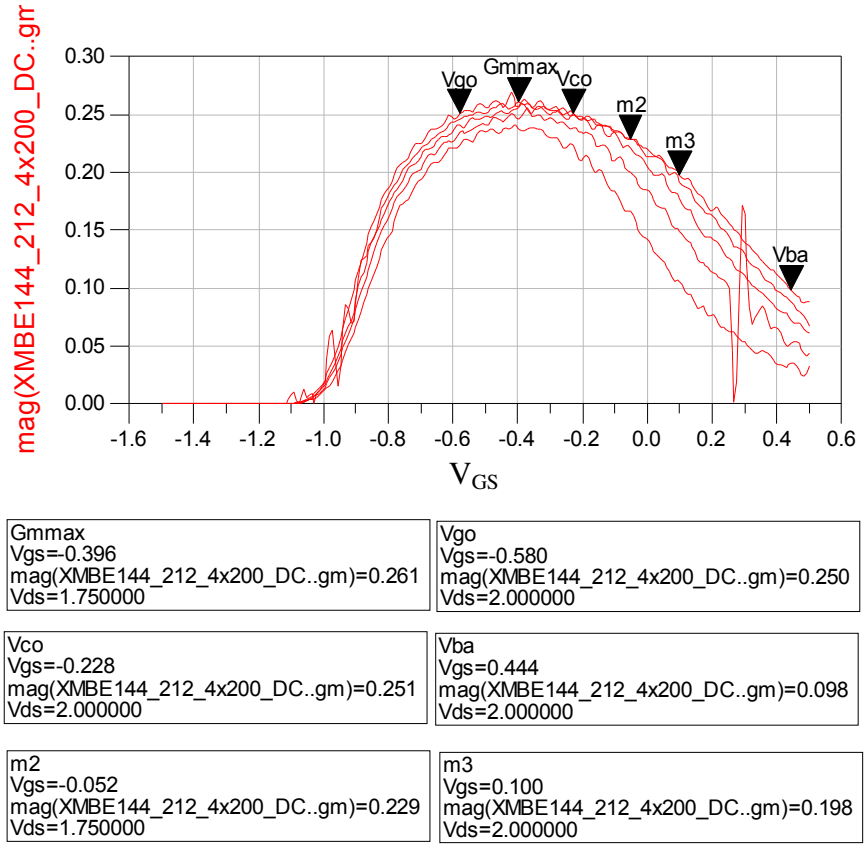


Figure 5-22 Graph of measured g_m versus V_{gs}

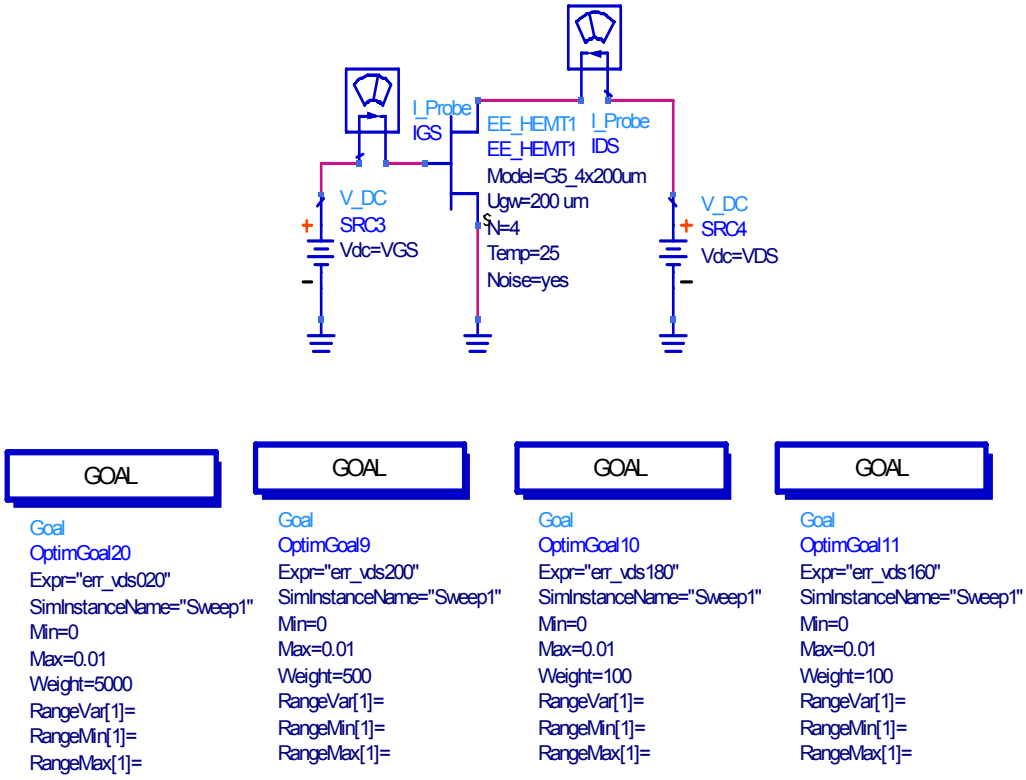
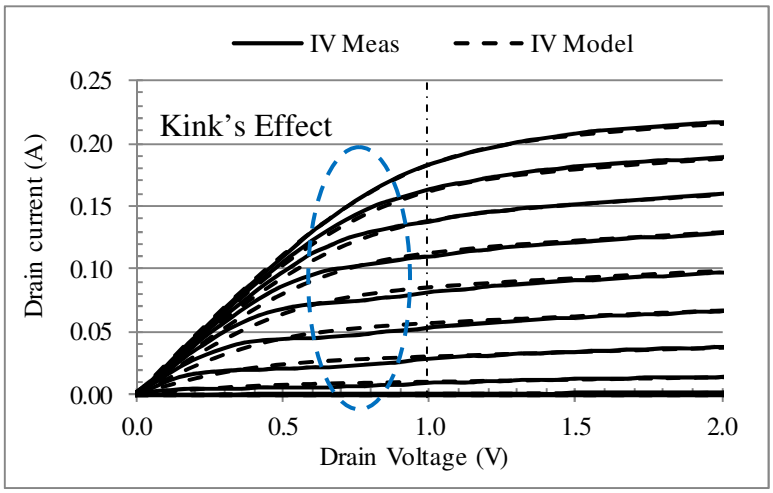
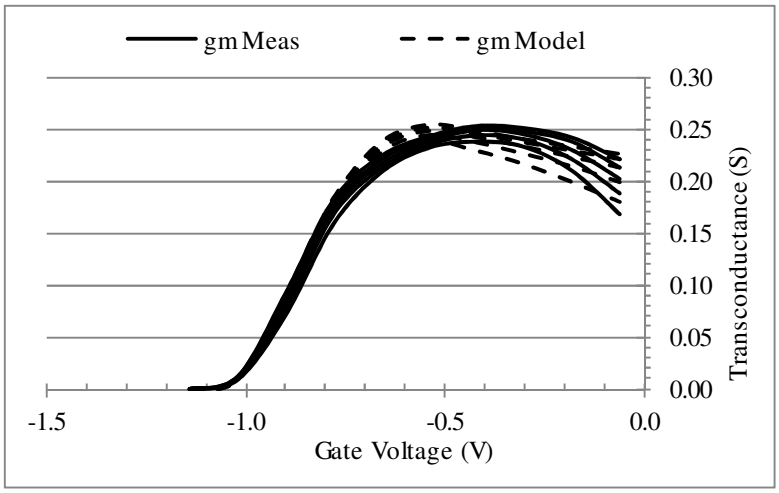


Figure 5-23 Modelling setup for DC Model (XMBE144, 4 x 200 µm)

In the DC modelling, two types of graph from the DC measurements are used: the I-V and transconductance (g_m) curves. Figure 5-24 (a) shows the comparison between the measured and modelled I-V characteristics. The graph shows excellent agreement between the two sets of data, except around the kink area. However, the difference between the two sets of data around the kink area is very small. Explanation of the kink effect is not included in this work due to the complexity in modelling it [75]. Nevertheless, for the bias conditions required, the low noise zone in this work (V_{DS} = 1 V) is safely outside the kink region. Figure 5-24 (b) shows the curve fitting between the measured and modelled transconductance, g_m. The model demonstrated good agreement between the two data at higher V_{GS}. Nonetheless, there is a marginal divergence at lower V_{GS} due to the limitations in the DC model [59].



(a)



(b)

Figure 5-24 DC Model curve fitting for 4 x 200 µm on XMBE144 (a) I-V curve fitting (b) Transconductance (g_m) curve fitting

Once good agreement is obtained between the modelled and measured data, the next stage of nonlinear modelling, the RF Modelling, can begin.

5.5.2.2 RF Models

In RF modelling, the same S-parameters fitting techniques were performed on the modelled and measured data. However, here the fitted components result in parameters that are totally different from the results of the intrinsic parameters fitting in the linear modelling work. Therefore, the S-parameter curve fitting in the RF model is a much more difficult task than the curve fitting in linear model.

Additionally the model is validated via modelling of the S-parameters over several bias points. Moreover, the drain-source currents (I_{DS}) for every bias point are also monitored because sometimes good matching of S-parameters data can be obtained, although a large difference between modelled and measured I_{DS} values still exists. These parameters are then tuned and optimised to obtain the optimum fitting between the measured and modelled S-parameters data. Figure 5-25 illustrated the modelling setup for the RF model.

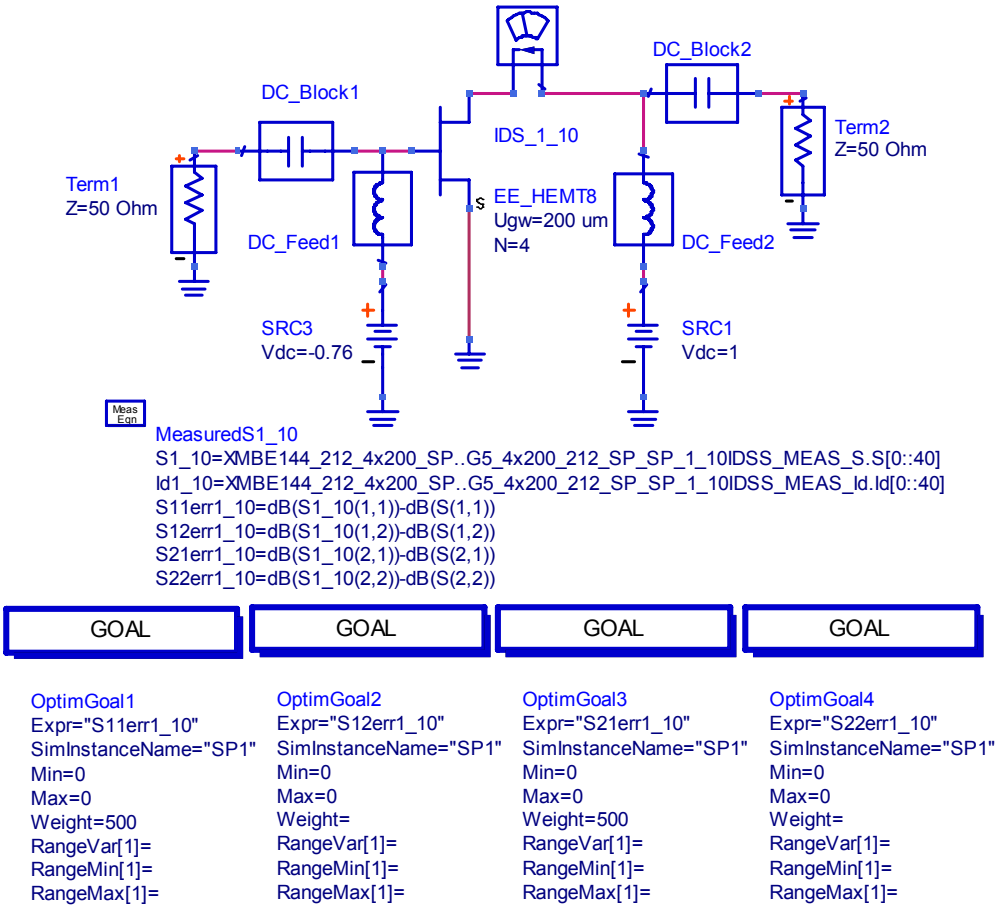
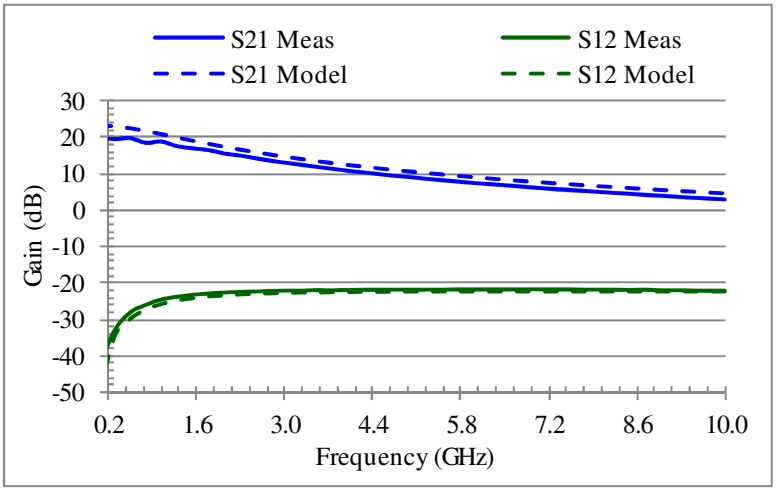
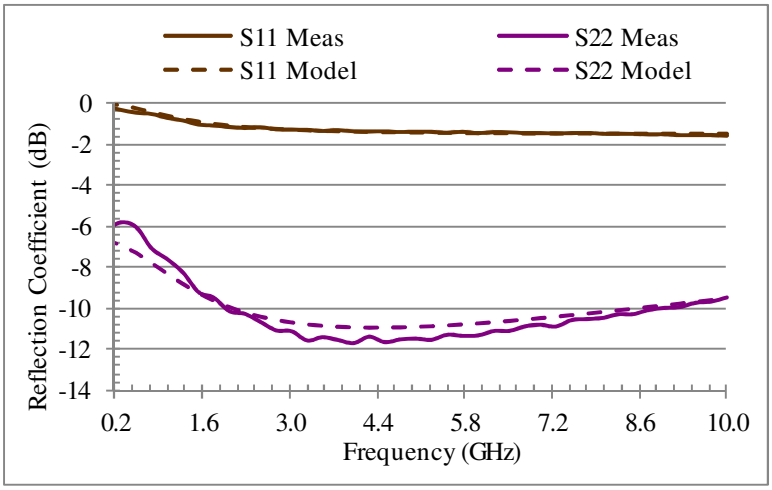


Figure 5-25 Modelling setup for RF Model (XMBE144, 4 x 200 µm)

Figure 5-26 (a) shows the curve fitting between the measured and modelled forward (S21) and reverse (S12) gain, whilst Figure 5-26 (b) shows the comparison between the measured and modelled input (S11) and output (S22) reflection coefficients. Both figures show excellent agreement between measured and modelled S-parameters.



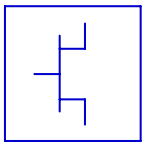
(a)



(b)

Figure 5-26 RF curve fitting for 4 x 200 µm on XMBE144. (a) Graph of gain against frequency and (b) Reflection coefficient against frequency

The transistor model is now complete and ready to be used in circuit designs. Figure 5-27 shows the transistor model (EE-HEMT Model) for XMBE144's 4 x 200 µm device.



EE_HEMT1_Model
G5_4x200um

Vto=-1.09982	Cdso=80 fF	Deltgs=0.0142162 V	Vba=0.549332 V
Gamma=0.00782293	Rdb=0.00245387 GOhm	Deltds=0.140589 mV	Vbc=460 mV
Vgo=-0.634847 V	Cbs=4.45784 fF	Lambda=0.000541507	Mu=1 m
Vch=0.772449 V	Vtoac=-1.1037654	C12sat=51.3941 fF	Deltgm=0.1278424
Gmmax=269.997 mH	Gammaac=0.007	Cgdsat=51.1595 fF	Deltgmac=0.18
Vdso=4.5619 V	Gmmaxac=0.271	Kbk=3.35e-008 m	Alpha=235.015 mV
Vsat=1.0073 V	Kapaac=247 mS	Vbr=12.04994	Tnom=25
Kapa=243.26 mS	Peffac=3	Nbr=1.49287	
Peff=2.76771	Vtsoac=-75	Idsoc=200.214 mA	
Vtso=-75.19896	Gdbm=7.46104 uF	Rd=1.16032 Ohm	
Is=1.22 nA	Kdb=128.301	Rs=0.40237 Ohm	
N=1.2	Vdsm=93.9742 V	Rg=1.185 Ohm	
Ris=0.24331 Ohm	C11o=0.610438 pF	Ugw=200 um	
Rid=0.167574 Ohm	C11th=1.74346 pF	Ngf=4	
Tau=1.55547 psec	Vinfl=80.5407 V	Voo=-0.257134 V	

Figure 5-27 A complete transistor model for XMBE144's 4 x 200 µm

Figure 5-28 to Figure 5-32 show the DC and RF fitting for the other five devices. The modelled data show excellent agreement with the measured data with very small percentage errors.

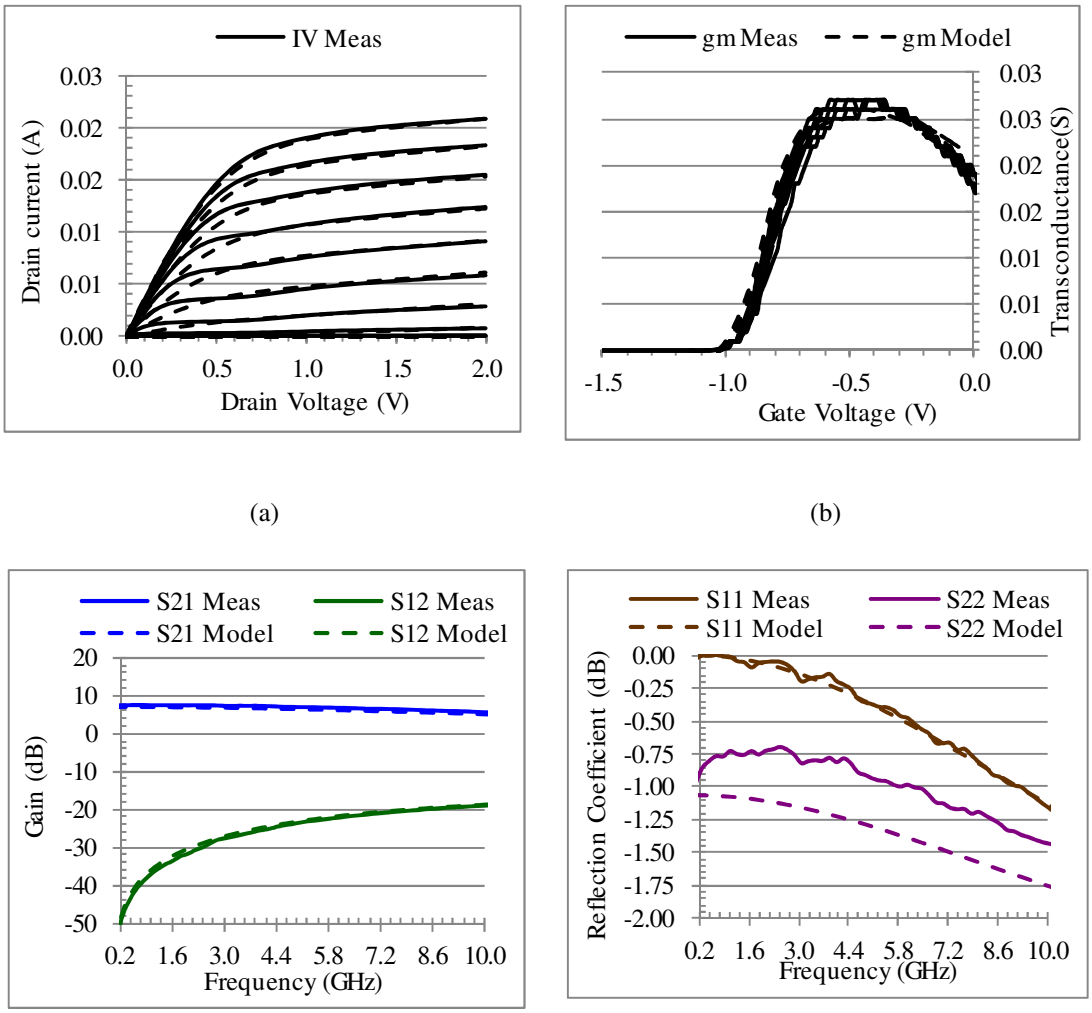


Figure 5-28 Summary of curve fitting for 2 x 50 µm on XMBE144 (a) I-V curve (b) Transconductance (c) Forward and reverse gain and (b) Reflection coefficient against frequency

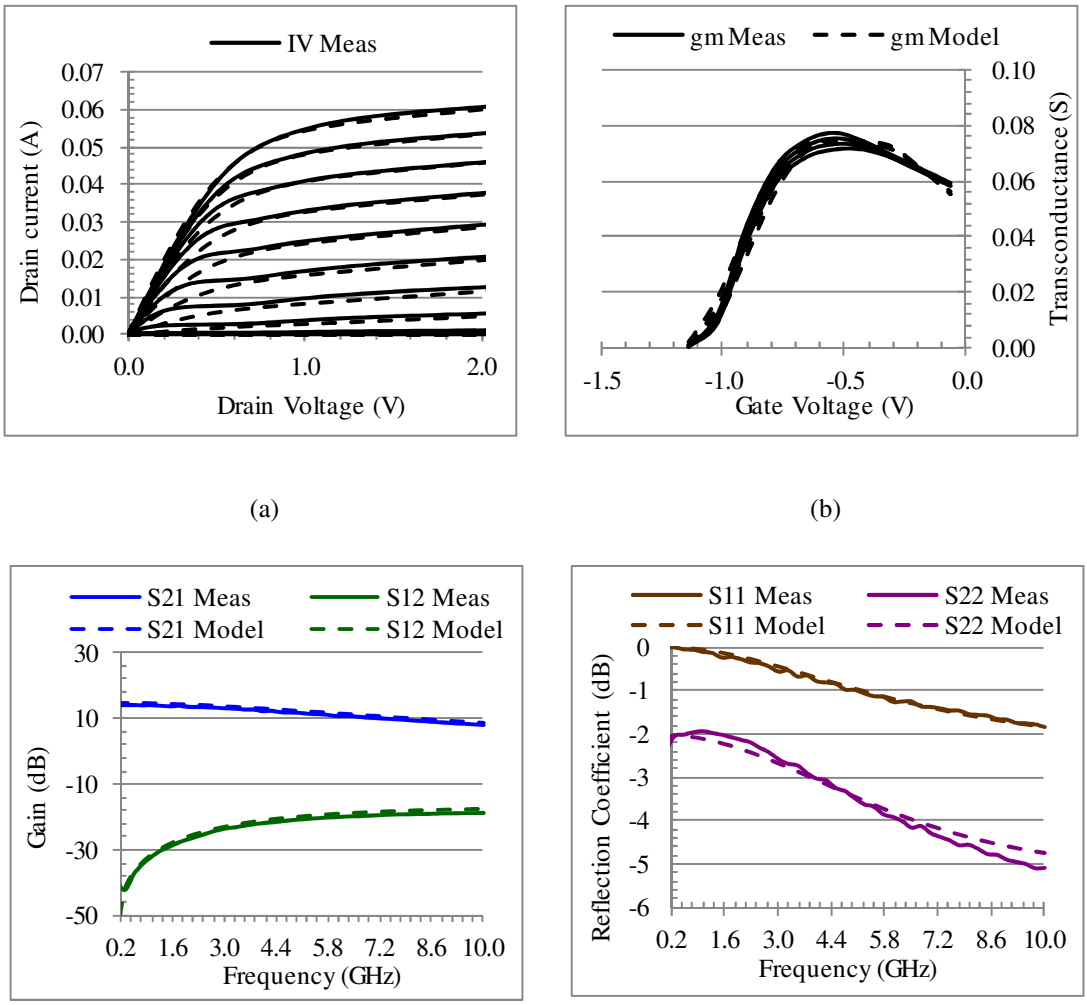
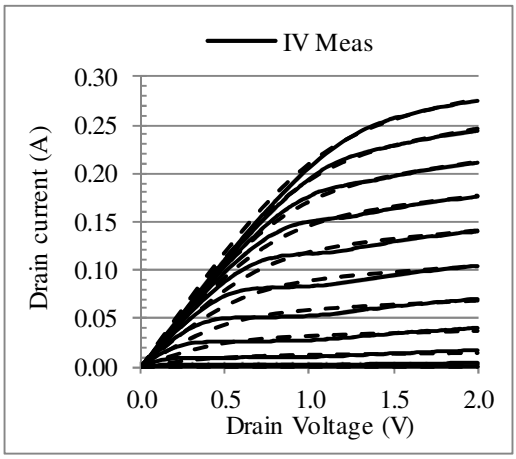
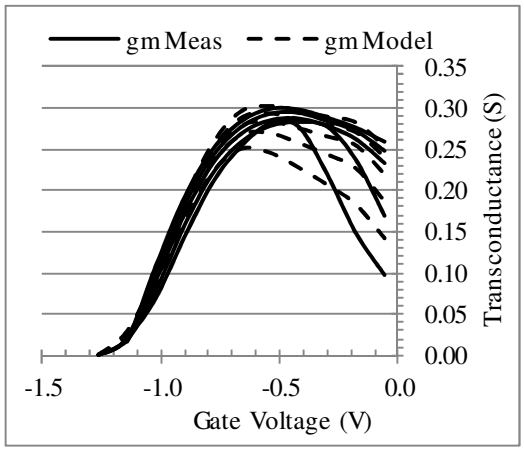


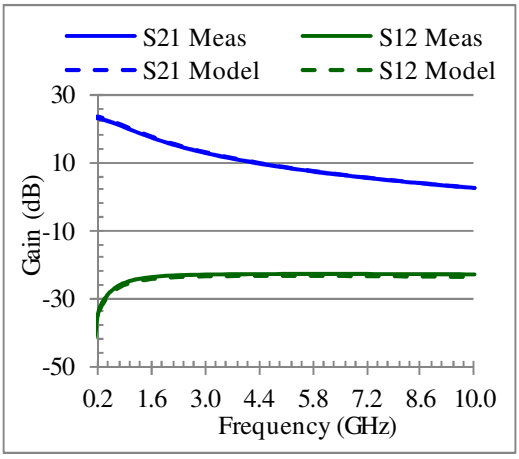
Figure 5-29 Summary of curve fitting for 2 x 100 µm on XMBE144 (a) I-V curve (b) Transconductance (c) Forward and reverse gain and (b) Reflection coefficient against frequency



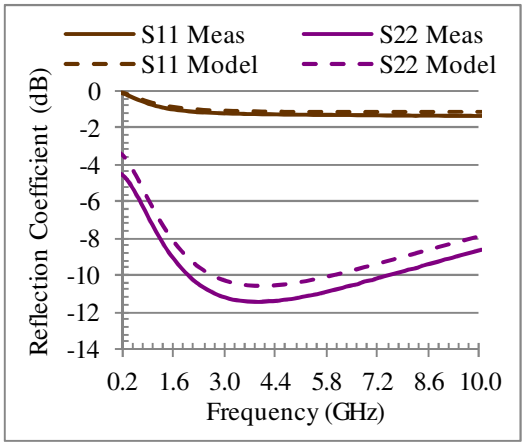
(a)



(b)



(c)



(d)

Figure 5-30 Summary of curve fitting for 4 x 200 µm on VMBE2100 (a) I-V curve (b) Transconductance (c) Forward and reverse gain and (b) Reflection coefficient against frequency

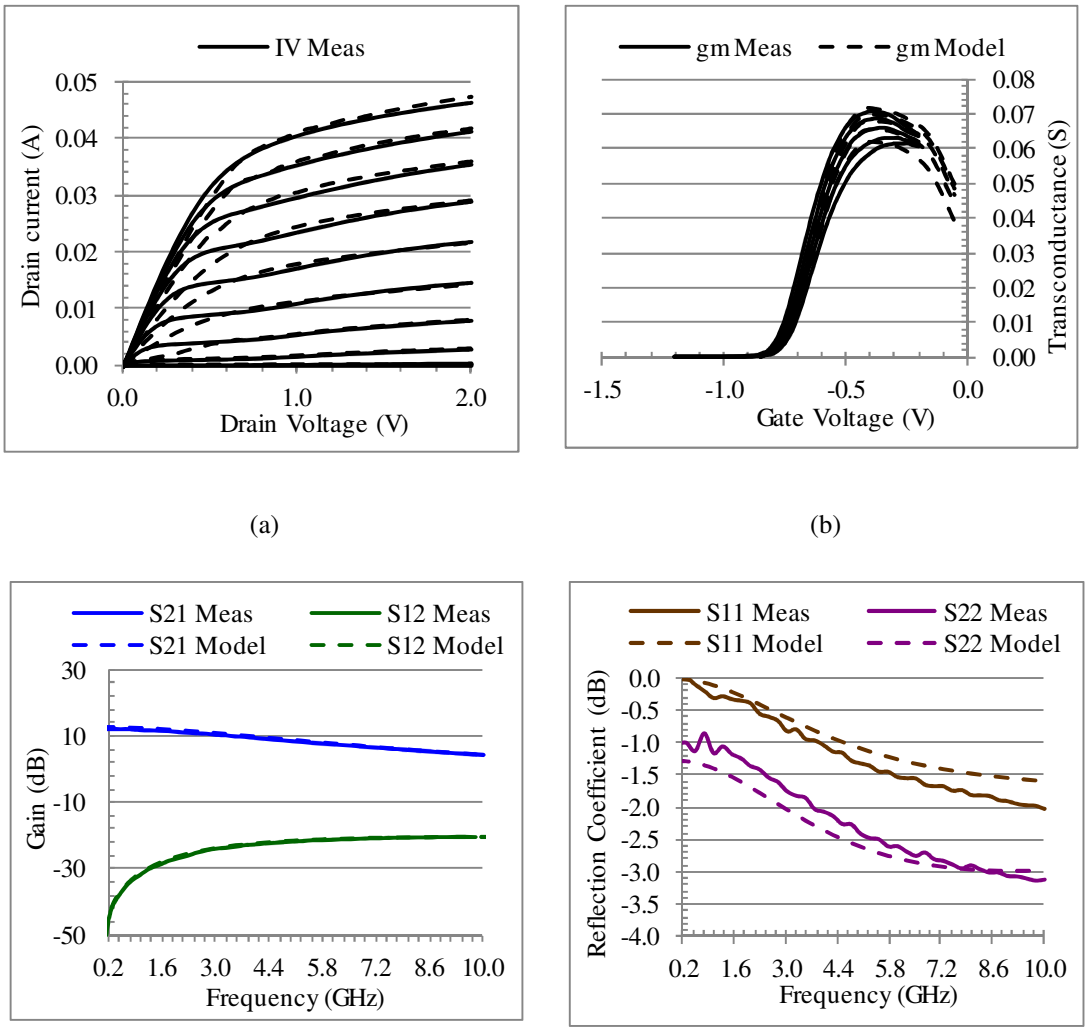
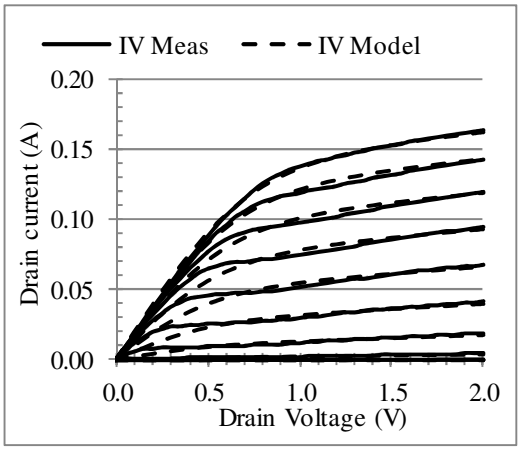
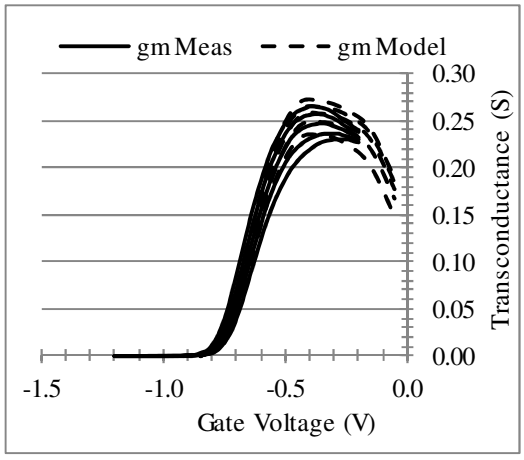


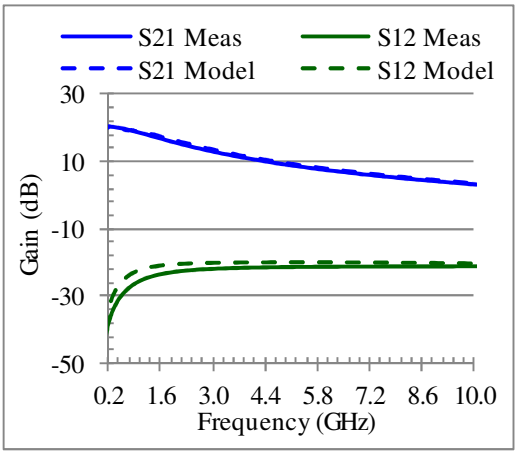
Figure 5-31 Summary of curve fitting for 2 x 50 µm on XMBE131 (a) I-V curve (b) Transconductance (c) Forward and reverse gain and (b) Reflection coefficient against frequency



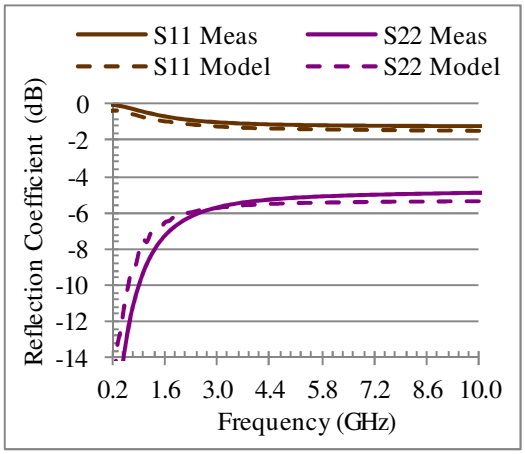
(a)



(b)



(c)



(d)

Figure 5-32 Summary of curve fitting for 2 x 200 µm on XMBE131 (a) I-V curve (b) Transconductance (c) Forward and reverse gain and (b) Reflection coefficient against frequency

5.6 NOISE MODEL

This section summarises the noise characteristics of the fabricated devices. The advantage of device scaling is seen when the device's minimum Noise Figure (NF_{min}) is plotted against device width at a certain frequency. NF_{min} can be viewed as the minimum Noise Figure (NF) that can be generated from the device if the device matching is at its optimum value. Thus, it is important to have optimum RF matching, as improper matching can make NF larger than NF_{min}.

Referring to Fukui's NF_{min} expression as written in equation (4-26), the noise characteristic of all devices can be examined. However, for convenience, Fukui's formula is re-written here as expressed in equation (5.2):

$$NF_{min} = 10 * \log\left(1 + k_1 \frac{f}{f_T} \sqrt{g_m(R_s + R_g)}\right) \quad 5\text{-}2$$

A constant, k_1 is equal to 3.5 [78]. The values of g_m, R_s and R_g can be obtained from the linear model. Figure 5-33 illustrated the plot of NF_{min} against transistor's width for all epitaxial layers under study at 2 GHz.

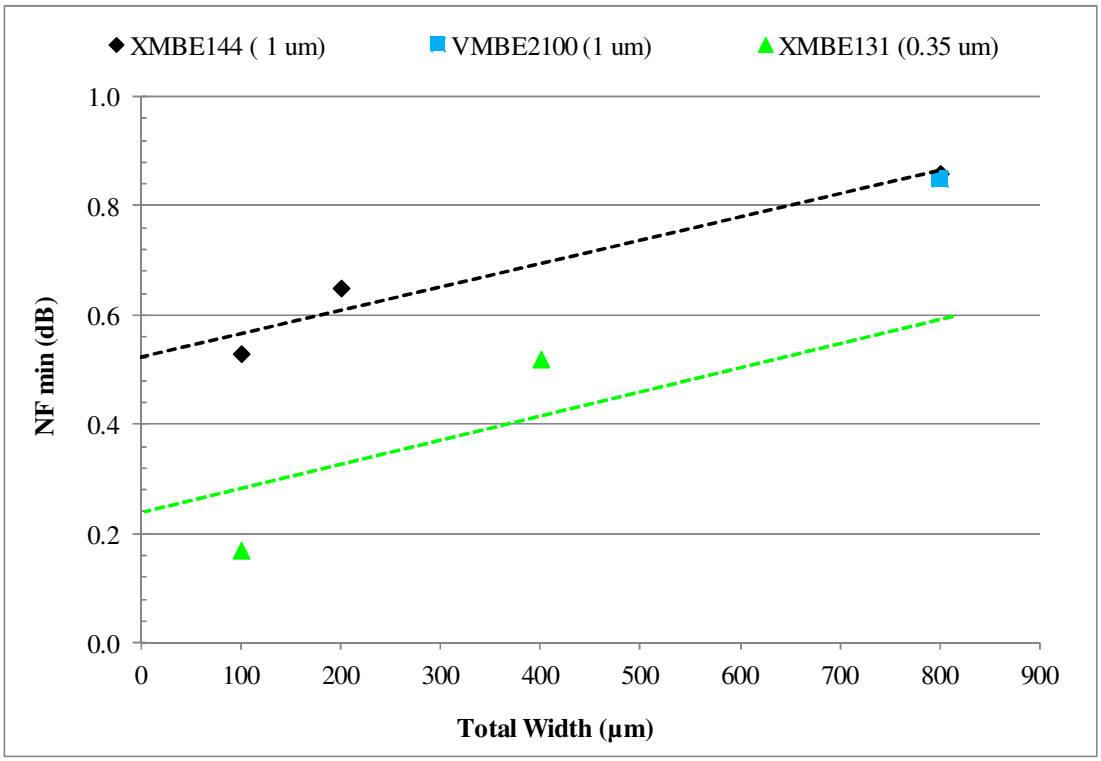


Figure 5-33 Plot of NF_{min} against device's width at f = 2 GHz. The devices from different epitaxial layers are distinguished by line colour

In the Figure 5-33, XMBE144 has three plotted data points, and it's NF_{min} for other device widths can be estimated by the trend line. The other epitaxial layers do not have enough data for the trend line to be plotted. However, VMBE2100 is estimated to have nearly the same NF_{min} as XMBE144 because it has a similar epitaxial layer as well as comparable extrinsic and intrinsic values when compared with XMBE144.

In the case of XMBE131, only two device widths are available which again permits the plot of its trend line. However, by assuming the trend line will follow XMBE144, we can estimate the NF_{min} for a larger device by plotting a line parallel to that for XMBE144.

In general, Figure 5-33 clearly shows that a larger device will exhibit higher NF_{min} characteristics. In the calculation of NF_{min}, the noise characteristic relies on knowledge of g_m and the summation of R_s and R_g values. From the extrinsic and intrinsic parameter extraction (see Table 5-4 and Table 5-5), the device's g_m increases with the increasing total device width. Conversely, the summation of R_s and R_g reduces, as the device's total width is increased. However, the increases in g_m outweigh the decrease in R_s and R_g values. Thus, NF_{min} follows the trend of the square root of $g_{m,}$ where larger values are obtained for larger devices.

Comparing the epitaxial layers, the 1 μm devices show higher noise characteristics than the submicron devices. Since the f_T for the submicron devices is more than double that of the 1 μm devices, from equation (5-2) , it is clear that the NF_{min} for submicron devices has been successfully reduced (including the larger device periphery). As can be observed from the Figure 5-33, the difference in NF_{min} between the 1 μm gate devices and 0.35 μm gate device is about 0.25 dB, a reduction of almost 50 %. This is an attractive characteristic for future low noise amplifier design.

Another important equation in discussing the noise characteristic is given by equation (5-3) [91, 92].

$$NF = NF_{min} + \frac{4R_n}{Z_o} * \frac{\left|\Gamma_S - \Gamma_{opt}\right|^2}{\left|1 + \Gamma_{opt}\right|^2 * (1 - |\Gamma_S|^2)} \qquad 5\text{-}3$$

For a system impedance (Z_o) = 50 Ω, the four noise parameters are:

Γ_S = complex source reflection coefficient,

Γ_{opt} = complex optimum refection coefficient,

NF_{min} = minimum noise figures when $\Gamma_S = \Gamma_{opt}$ in dB,

R_n = the noise resistance

Equation (5-3) relates the device *NF* with respect to the four noise parameters and can also be interpreted as the how far the *NF* value can deviate with respect to NF_{min}. In other words, if the four noise parameters are small, the second term in equation (5-3) will be small, thus *NF* will be closer to $NF_{min.}$ Importantly, the R_n value will change depending on the device widths. Figure 5-34 is a plot showing the decrease in R_n values as the device width is increased at 2 GHz for sample XMBE144. Thus, a large device periphery is preferable, not just because it can provide high circuit gain, but also because it gives better RF matching, resulting in *NF* being closer to NF_{min}.

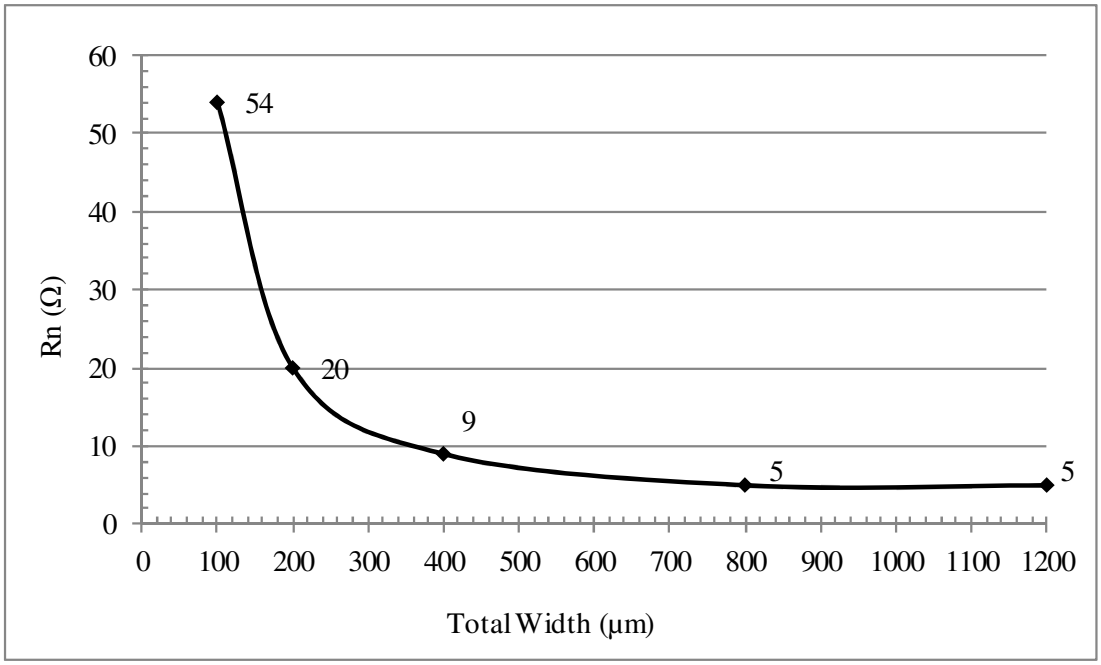


Figure 5-34 Plot of noise resistance R_n against device's width at f = 2 GHz for XMBE144

5.7 SUMMARY

In this chapter, complete sequences of device modelling steps are described. A comprehensive discussion of the advantages of three different epitaxial layers is shown. Comparisons between the modelled and measured devices from each epitaxial layer are also presented.

At the end of the chapter, a comparison between the noise characteristic of the three epitaxial layers is made. The submicron devices have shown the lowest NF_{min} values

when compared with the 1 μm devices. Practically, a reduction of 50% in NF_{min} can be observed by using the submicron gate device. Additionally a large device periphery is shown to be preferable, as a large device can provide wideband RF matching.

CHAPTER 6

MMIC LNA DESIGNS

6.1 INTRODUCTION

The low noise amplifier (LNA) is the key component in every communication system. It is used in the front end of a receiver to amplify the weak input signal, while minimising the introduction of additional noise. The LNA's performance is measured by a number of figures of merit as discussed in Chapter 3. This chapter also describes important considerations in the successful implementation of an LNA design.

To meet the stringent LNA performance requirements, a systematic procedure was introduced for the design of the LNA. This chapter focuses on the in-house fabricated pHEMT at the University of Manchester. However, there are various devices that are suitable for LNA applications including complementary metal–oxide–semiconductor (CMOS), metal semiconductor field effect transistor (MESFET) and Heterojunction Bipolar Transistor (HBT).

In this chapter, a theoretical study of preferred LNA circuit topologies will be described. The discussions begin with an appropriate Integrated Circuit (IC) design which is suitable for the miniaturisation of the circuit used in this research. Before the circuit design is further discussed, the design specifications and selection of the active device are be highlighted. This is followed by the concept of DC biasing at an appropriate operating point as explained in section 4.2. Furthermore, the DC bias points will depend on the circuit applications such as low noise, high gain or high power. Since noise is the primary concern in this project, the biasing network and impedance matching are defined so that the designs' system impedances are optimised, the circuits are stable, and, of particular importance, give the lowest possible noise characteristics.

In this project, the output and input impedance is matched to 50 Ω systems. The choice of transmission line is explained at the end of this chapter to conclude the design procedures for the successful implementation of LNA designs.

6.2 MMIC TECHNOLOGY

The integrated circuit technology selected for this research project is the Monolithic Microwave Integrated Circuit (MMIC). Monolithic come from the Greek word which means "as a single stone". This is the fundamental principle of MMIC design, where all of the passive and active components are fabricated on the same semiconductor substrate. The term 'Microwave' refers to the frequency range of 300 MHz to 300 GHz, and corresponds to a wavelength of 1 m to 1 mm. An 'Integrated Circuit (IC)' consists of both active (e.g. transistors) and passive components (such as capacitors and inductors) on the same circuit [58].

MMICs have been widely used due to their advantages over other microwave technologies. Due to their small size (from 1 mm^2 to 10 mm^2), thousands of MMICs can be produced on a single wafer, and therefore promise low unit cost for mass production [58]. Their small size and low mass make these MMICs suitable for many applications which require a compact design, such as mobile phones and smart cards [93]. Additionally, the broadband performance of MMICs is excellent due to the reduced number of parasitic elements caused by wire bonds and embedded active devices within the printed circuit. Moreover, the reproducibility is also excellent because all of the active and passive components are produced using the same photolithography masks.

Whilst it has many advantages, the MMIC technology also has drawbacks that need to be addressed. The MMIC manufacturing is time consuming and costly, since the correct functionality of the circuit can only be checked after the whole fabrication is completed. Therefore, the physical and electrical models for both active and passive element must be accurate before commencing the fabrication process. Furthermore, setting up an MMIC fabrication facility for mass production is expensive [58] and the choice of components (especially passives) are also limited due to the small chip area.

A successful MMIC circuit is a result of accurate models of active and passive devices. The modelling of the active device has been addressed in Chapter 5. Therefore, this chapter will detail the modelling and design of MMIC passive elements.

6.2.1 Passive Modelling

Accurate modelling of the passive elements in MMICs is crucial for good circuit performance. In MMIC design, the passive elements, such as inductors, capacitors and resistors, need to be integrated with the active elements using transmission line interconnection. This section focuses on the modelling of lumped-element passive components at microwave frequencies.

6.2.1.1 MMIC NiCr Resistor

MMIC resistors are usually fabricated from Tantalum Nitride (TaN) or Nickel Chromium (NiCr) [94]. However, NiCr resistors are widely used in circuit design due to their low temperature coefficient of resistance (TCR) and small parasitic value [95]. In this project, NiCr is used to produce MMIC resistors by following the approach of Sharma et al as outlined in [96]. The equivalent circuit model for a NiCr resistor is shown in Figure 6-1:

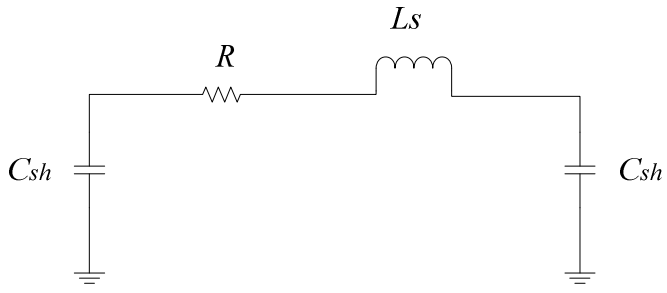


Figure 6-1 Schematic of equivalent circuit model for NiCr resistor [96]

R is the real value of resistance, L_s is the series inductance and C_{sh} is the shunt capacitance to ground. The structure is assumed to be symmetrical. The Y-

parameters for a two port network are applied to extract all of the values. The equations are listed as below:

$$Y_{11} + Y_{21} = j\omega C \quad 6\text{-}1$$

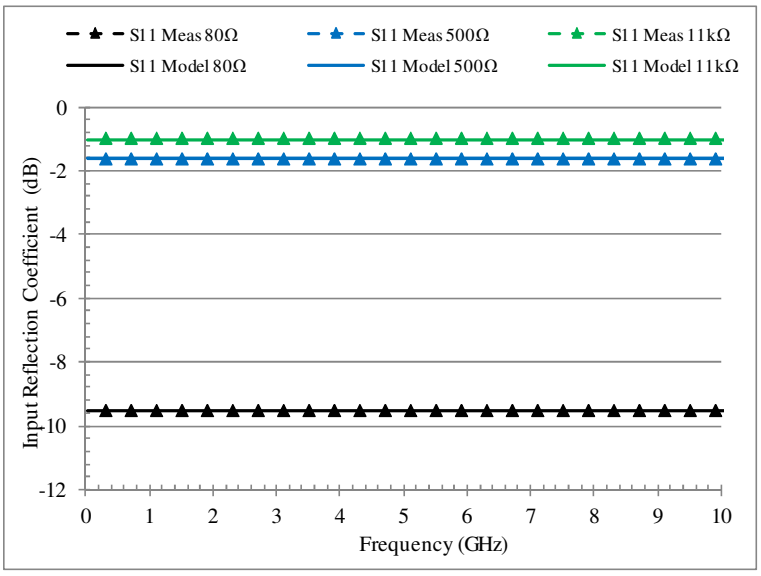
$$Y_{21} = -\frac{1}{(R + j\omega L_s)} \quad 6\text{-}2$$

Assuming $\omega^2 Ls^2 << R^2$ then,

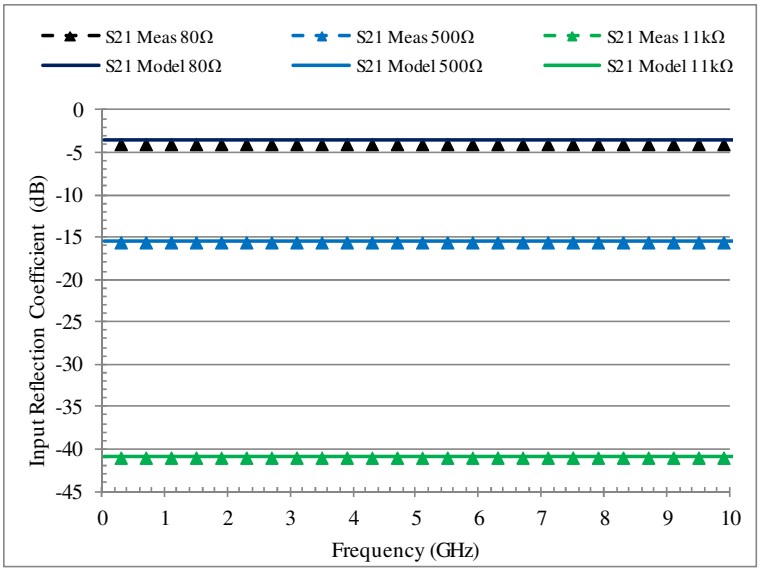
$$Re[Y_{21}] = -\frac{1}{R} \quad 6\text{-}3$$

$$Im[Y_{21}] = \frac{\omega L_s}{R^2} \quad 6\text{-}4$$

The equations (6-1) to (6-4) were modelled using the ADS software. Several modelled NiCr resistors were compared with measured data as depicted in Figure 6-2. The measured data shows excellent agreement with the modelled data for a wide frequency range, and hence the equivalent circuit model is validated for use in LNA designs.



(a)



(b)

Figure 6-2 Comparison graphs between measured and modelled S-parameters for NiCr resistors (a) S11 (b) S21

Figure 6-3 shows the in-house fabricated NiCr resistor. The resistance value (*R)* is 8 kΩ and *Ls* is 32 pH. The values for C_{sh} were very small and therefore can be neglected.

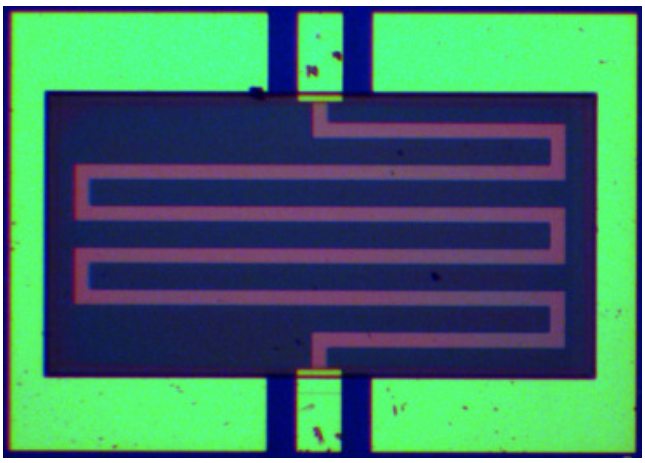


Figure 6-3 MMIC NiCr resistor fabricated at the University of Manchester (8 kΩ)

6.2.1.2 MMIC MIM Capacitor

Metal Insulator Metal (MIM) capacitors are formed by sandwiching a layer of dielectric between two metal plates. The dielectric layers are usually silicon nitride, polyimide or silicon dioxide [97]. In this project, silicon nitride was used as the dielectric material. The equivalent circuit model for the MIM capacitor is illustrated in Figure 6-4.

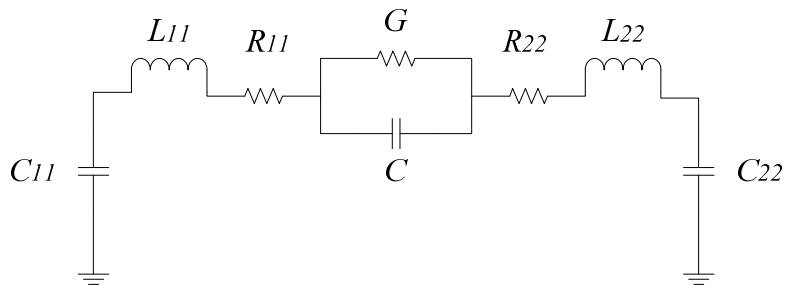


Figure 6-4 Schematic of equivalent circuit model for MIM capacitor [98]

R_{11} and R_{22} are the resistances for the top and bottom plates respectively. L_{11} is the series inductance of the top plate, and L_{22} is the series inductance for the bottom plate. C_{11} and C_{22} are the capacitances of the top and bottom plates respectively.

The main capacitor, C is calculated as:

$$C = \varepsilon_o \varepsilon_r \frac{WL}{t_d} \quad 6\text{-}5$$

Where ε_o is the free space permittivity, ε_r is the relative permittivity of the dielectric, t_d is the thickness of the dielectric material, and W and L are the width and length of the overlapped metal plates respectively.

The loss in conductance, G due to the capacitance of the dielectric is computed by calculating the product of the loss tangent ($tan\delta_d$).

$$G = \omega C tan\delta_d \quad 6\text{-}6$$

The metal plate loss resistances R_{11} and R_{22} are given by:

$$R_{11} = R_{22} = \frac{\rho L}{W t_p} \quad 6\text{-}7$$

Where ρ is the metal resistivity and t_p is the thickness of either the top or bottom plate.

The metal plate inductance and parallel capacitance can be obtained from [98]:

$$L_{11} = L_{22} = \frac{0.4545 Z_o L}{C} \quad 6\text{-}8$$

$$C_{11} = C_{22} = \frac{0.5 \varepsilon_{eff} L}{C Z_o} \quad 6\text{-}9$$

Where Z_o is the characteristic impedance = 50 Ω. The values of 0.4545 and 0.5 from equations (6-8) and (6-9) is the proposed model parameters.

All of the MIM capacitor equations were modelled using the ADS software. Figure 6-5 shows the graphical comparison between modelled and measured S-parameters for an 8 pF capacitor.

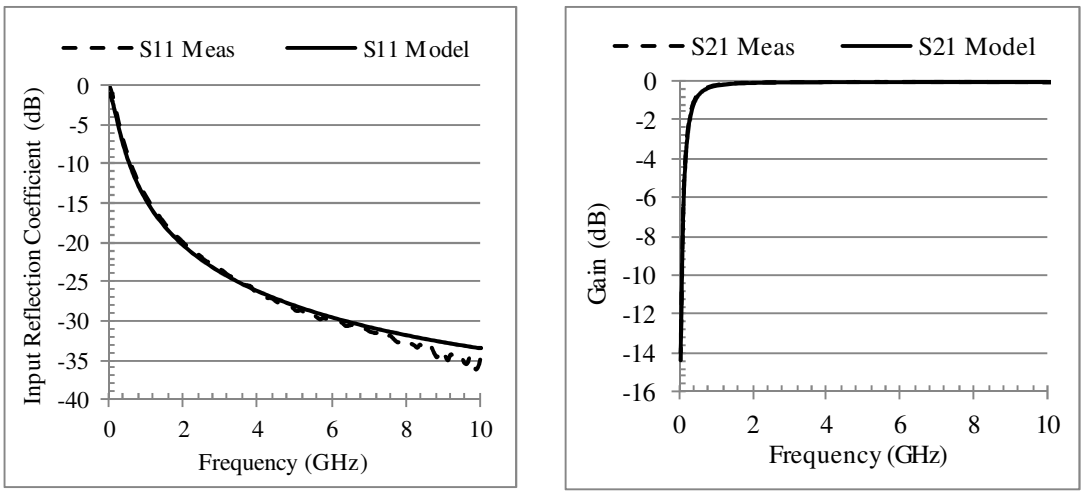


Figure 6-5 Comparison graphs between measured and modelled S-parameters for 8 pF MIM capacitor

The excellent fits between modelled and measured data validate the MIM capacitor model which will be used in the LNA designs. An in-house fabricated MIM capacitor (8 pF) is shown in Figure 6-6.

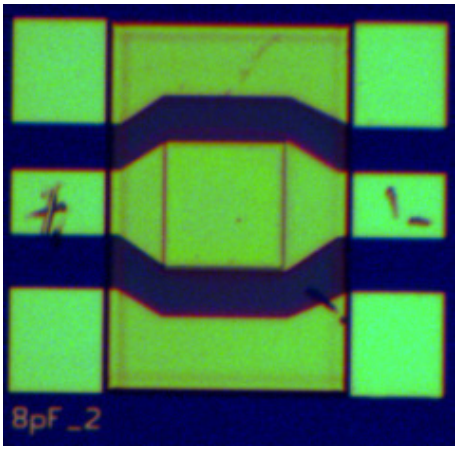


Figure 6-6 MMIC MIM capacitor fabricated at the University of Manchester

6.2.1.3 MMIC Spiral Inductor

The Spiral inductor requires at least two metal layers to prevent a shorted connection. A spiral inductor can be designed in the form of octagonal, circular or square shapes [99]. In this work, the square shape of a spiral inductor was used for ease of fabrication. Figure 6-7 shows the equivalent circuit model for the spiral inductor.

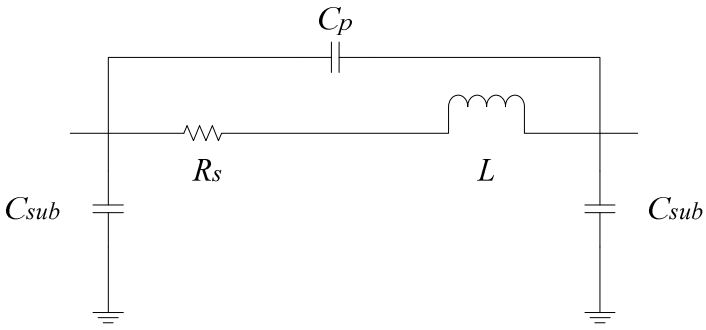


Figure 6-7 Schematic of equivalent circuit model for spiral inductor

The primary inductance is L which in series with the resistance R_s. C_p is the feedback capacitance and C_{sub} is the capacitance of the metal to ground.

The value for inductance, L is computed using equations (6-10) and (6-11).

$$L = 2.34 * \frac{\mu_0 {n_L}^2((D_L + d_L)/2))}{1 + 2.75\rho} \quad 6\text{-}10$$

and

$$\psi = \frac{D_L - d_L}{D_L + d_L} \quad 6\text{-}11$$

Where μ_o is the permeability of free space, n_L is no of turns, k_{L1} and k_{L2} are the processing dependent fitting factors and ψ is the ratio of the difference between outer diameter, D_L and inner diameter, d_L of the spiral inductor. Values for k_{L1} and k_{L2} are 2.34 and 2.75 respectively as reported in [99].

R_s, C_p and C_{sub} can be calculated using the equations listed below:

$$R_s = \frac{P_L \rho}{t_p W_L} \quad 6\text{-}12$$

$$C_p = n_L \varepsilon_r \varepsilon_o \left(\frac{W_L x L_L}{t_{p-dielectric}} \right) \quad 6\text{-}13$$

and

$$C_{sub} = \frac{W_L P_L C_o}{2} \quad 6\text{-}14$$

Where ρ is the metal resistivity, t_p is the metal thickness, $t_{p\text{-}dielectric}$ is the silicon nitride thickness, P_L is the length of metal, W_L is the width of the square metal and C_o is a process dependent fitting parameter. The parameters used in this project are summarised in Table 6-1.

Table 6-1 Table of parameter value used for in-house fabricated spiral inductor

Parameters	Value used
P	2. 44 e-8 Ω-m
t_p	-450 nm
$t_{p\text{-}dielectric}$	90 nm
ε_r	7.5
C_o	5e-6 F

A number of spiral inductors were fabricated at the University of Manchester to verify the equivalent circuit model which will be used for the LNA design. However, only one value, a 14 nH inductor, is included in this chapter as an example. The S-parameters comparison between measured and modelled data for the 14 nH spiral inductor is shown in Figure 6-8. The overlapped modelled and measured data indicates that the model is accurate over the intended frequency range of 300 MHz to 1.4 GHz and hence, can be used with confidence in the design process.

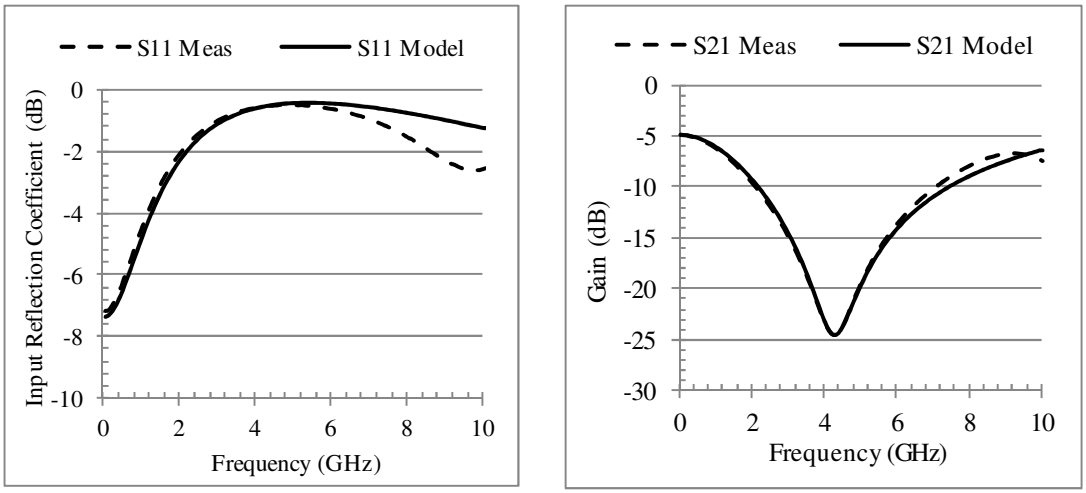


Figure 6-8 Comparison graphs between measured and modelled S-parameters for 14 nH spiral inductor

The in-house fabricated 14 nH spiral inductor is shown in Figure 6-9.

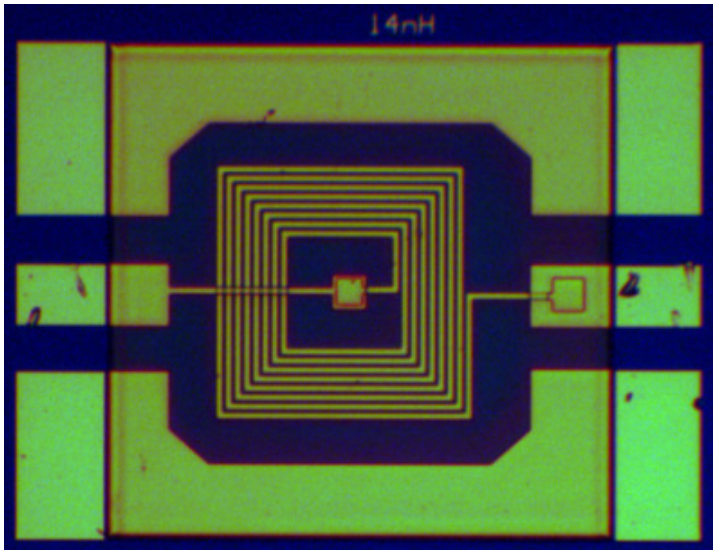


Figure 6-9 MMIC Spiral inductor fabricated at the University of Manchester

6.3 LNA SPECIFICATIONS

An important LNA specification that strongly influences the circuit design is the frequency range of interest. The choice of frequency range will also give affect other design specifications. In this project, the frequency is selected to be between 0.4 GHz and 1.4 GHz, to suit the application of the medium frequency range of the Square Kilometre Array (SKA), Global Positioning System (GPS), mobile communication and other medium frequency commercial applications.

The most critical parameter of a Low Noise Amplifier (LNA) is its Noise Figure (*NF*). The *NF* depends on the correct selection of active device, which will be further explained in section 6.4 . In this work, the *NF* is targeted to be better than 1 dB over a very wide range of frequencies in the band of interest. However, the final SKA specification for *NF* is further tightened, with a value of 0.5 dB being highly desirable, as lower *NF* will result in a smaller, more cost effective collector area. In simple terms, each 0.1 dB increase in *NF* adds significant cost, as the collecting area will need to be larger to compensate for the higher *NF*. Alternatively, every fraction of a dB gain in noise saves costs.

The LNA must also provide stable gain and small signal loss over the entire operating bandwidth. The LNA circuit gain in this project was chosen to be at a moderate range of around 25 dB to 35 dB. The upper gain value is to prevent the circuit from oscillating, which commonly happens in very high gain circuits. Input and output return loss is specified to be better than -5 dB.

For SKA applications, a wide collecting area automatically demands a large number of receiver circuits. Therefore, the system implementation also must have a constraint in terms of cost and power consumption [100]. Due to these requirements, the 1 µm gate LNAs were fabricated using relatively inexpensive optical lithography techniques, while delivering high production throughput, and also, more fundamentally, reasonable low noise behaviour. In addition to minimising the overall cost and complexity during their measurement, the LNAs are measured only at room temperature, where expensive cryogenic methods are not required. As such, the LNA must provide an exceptionally low noise performance at room temperature. This is one of the main specifications of the LNA, where cryogenic cooling for a large

number of elements would be impractical. The power consumption is set to be less than 150 mW and it is designed to be unconditionally stable over a wide frequency range for good linearity.

The LNA is designed for commonly used 50 Ω source and load impedance systems, allowing ease of testing and circuit interfacing to other components in the system.

6.4 SELECTION OF ACTIVE DEVICES

One of the most practical approaches for improving the overall performance of the LNA is by the selection of the most appropriate active device, which has an optimised epitaxial layer structure and optimised biasing conditions. In this project, the active device is selected from the novel high breakdown InGaAs/InAlAs/InP pHEMTs which have been developed and fabricated using conventional optical lithography at the University of Manchester [101]. The epitaxial layer structure has been presented in section 5.2 of Chapter 5.

Initially, the fabrication work was focussed on the XMBE144 epitaxial layer, from which relatively low gate leakage devices can be fabricated. However, the pHEMT structure was later further optimised and grown on a new VMBE2100 sample with better gate leakage performance, due to its wider bandgap material in the supply layer. VMBE2100 also showed better thermal stability when compared to XMBE144. To date, submicron devices have been produced using optical lithography and reflow processes, which will help the LNA design to meet the SKA's low noise requirement. However, the submicron device design is still under development and will not be included further in this thesis. Thus, LNA design from XMBE144 and VMBE2100 are the main discussion in this thesis.

The comparison of leakage current (I_{GS}) and transconductance (g_m) of the 4 x 200 µm devices between XMBE144 and VMBE2100 are shown in Figure 6-10 and Figure 6-11 respectively. The fabricated transistor on sample VMBE2100 demonstrated excellent performance with higher g_m and reduced leakage current when compared with XMBE144. These superior properties are fundamentally important for low noise applications, since increased g_m will automatically provide

improved RF performance (f_T) and hence reduce the noise figure (refer to Equation (4.26) and Equation (4.27)). The transistor on VMBE2100 also has a lower leakage current and therefore improved noise performance since leakage current is directly proportional to the noise as explained in [102].

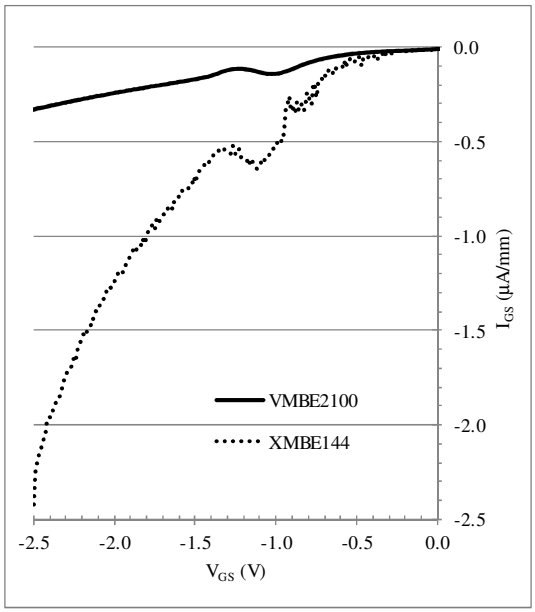


Figure 6-10 Graph of comparison on leakage current between fabricated transistor on sample XMBE144 VMBE2100 at V_{DS} = 1 V

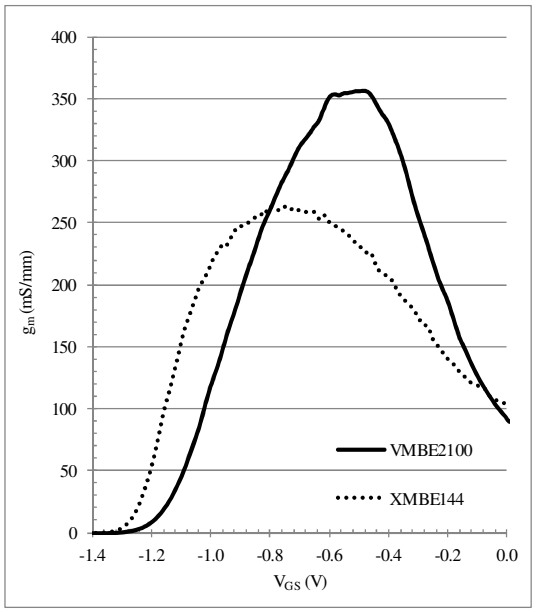
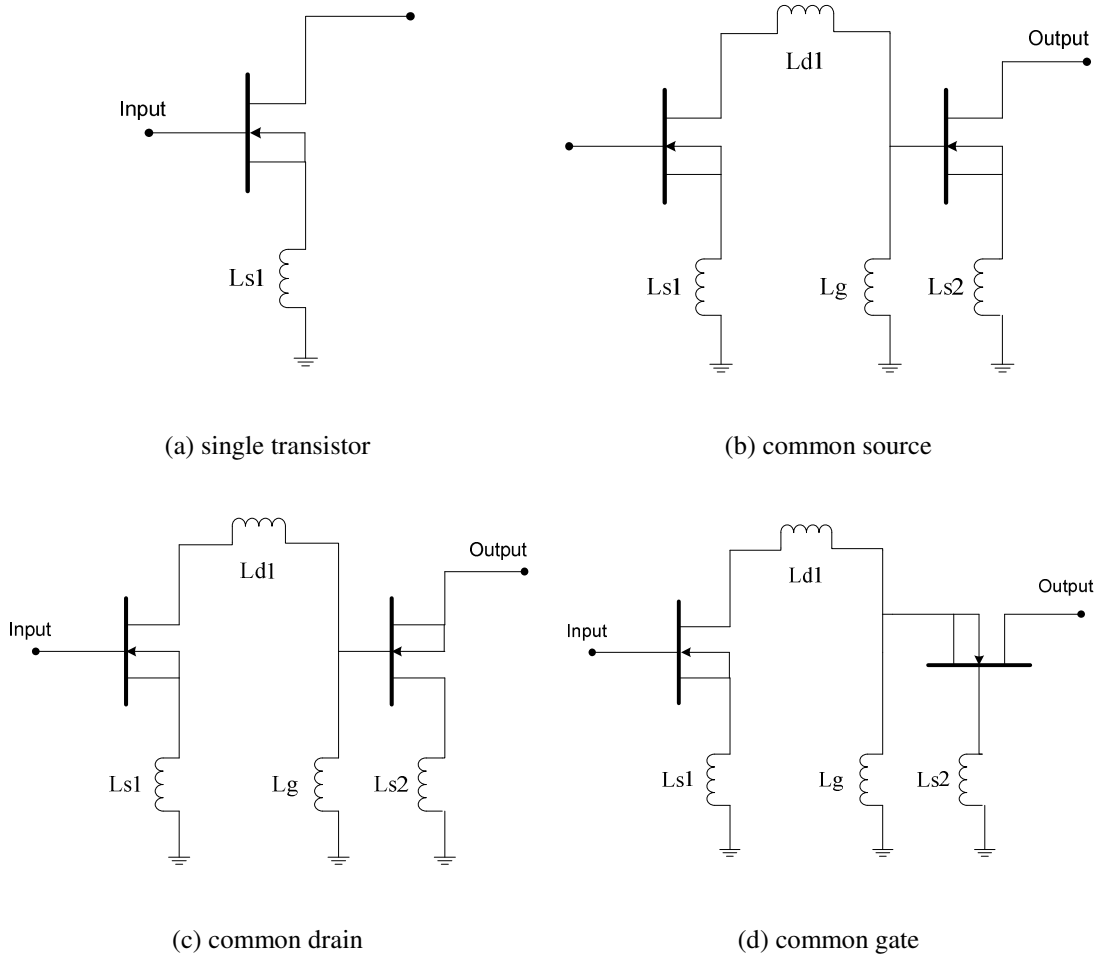


Figure 6-11 Graph of comparison on transconductance, g_m between fabricated transistor on sample XMBE144 VMBE2100 at V_{DS} = 1 V

6.5 CIRCUIT TOPOLOGY

Another important consideration in LNA implementation is the proper selection of network topology. An optimal LNA design must have low noise figure, high gain, wide bandwidth, low power dissipation, compact size and must be unconditionally stable over the desired frequency range. However, HEMT technologies alone cannot meet all of these requirements simultaneously [103]. Therefore, the circuit topology is selected to meet most of the system requirements.

The basic configurations of HEMT's LNA are similar to the FET's LNA theoretical network. The four basic configurations of FET amplifiers are depicted in Figure 6-12.



(a) single transistor (b) common source

(c) common drain (d) common gate

Figure 6-12 Schematic diagram of basic LNA topologies

The fundamental LNA network only requires a single transistor as illustrated in Figure 6-12 (a). This network is known as a single stage amplifier or single stage amplification path. The minimum noise for this configuration is the noise measure of the single transistor. The gain for this configuration is usually small. Therefore, to improve the gain, the second transistor is cascaded in series with the first, as shown in Figure 6-12 (b), (c) and (d). These networks are all referred to as double stage amplifiers.

There are three basic configurations of double stage amplifiers:

1) Common source
2) Common drain and
3) Common gate

The common source amplifier has a noise measure close to the transistor's minimum noise measure over the wide bandwidth [104]. The disadvantage of the common source configuration is that it suffers from a lack of gain flatness as the gain is very high at low frequency and tends to be very low at high frequency [103]. This disadvantage can be corrected by using a proper matching network in the LNA designs. The common drain is normally used for buffer amplifiers. It has low output resistance and is therefore capable of driving low impedance loads with little loss of gain. This topology can provide an advantage to digital circuits since the inherent impedance-buffering action can enhance the speed of circuit operations [105]. The common gate is use as a current buffer. This topology allows unity current gain with low input resistance [106].

Common drain and common gate topologies are more prone to oscillation than the common source network [94]. These configurations have a larger gain at high frequencies, but also a larger noise measure. Therefore, it has been decided to use a common source configuration in this project due to the smallest minimum noise measure over a wide band. Also the limitations in poor gain and gain flatness can be improved using a double stage design and a proper matching network.

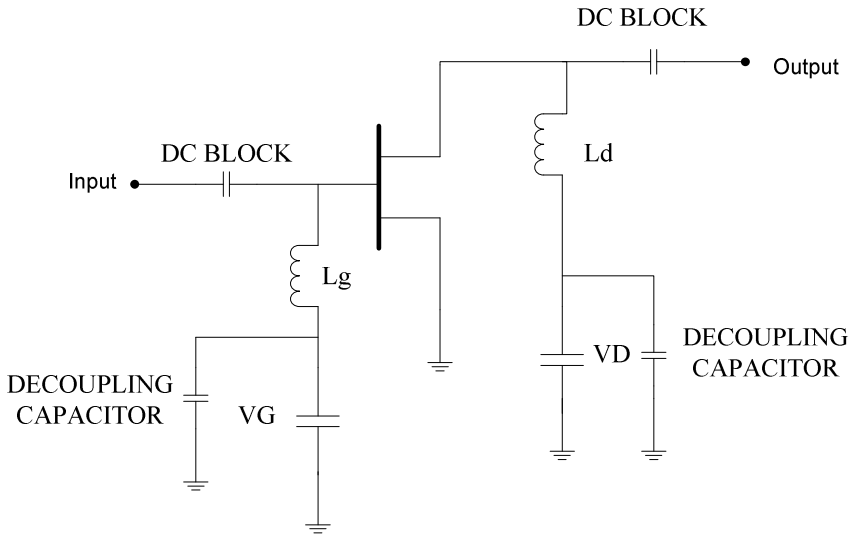
6.6 BIASING NETWORK

Up to this stage, the active device, circuit topology and DC bias point (as discussed in section 4.1) have already been selected for the LNA implementation. Another important decision is to select the correct biasing network, taking into consideration that not all bias networks can be matched to the modelled transistor. As a result of improper network biasing, the LNA will oscillate or the noise will increase.

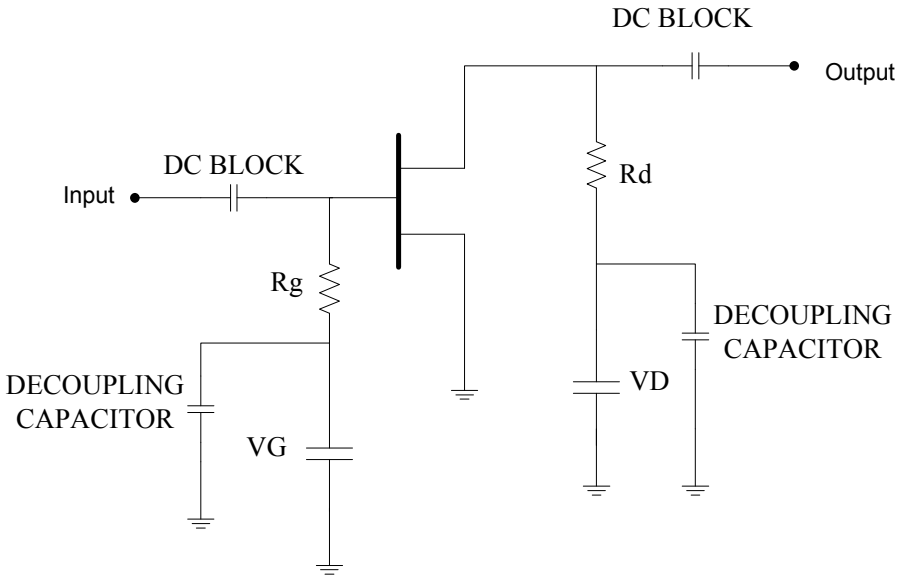
The RF circuit design begins with the use of DC blocking and decoupling capacitors. DC blocking capacitors are used at the input and output to isolate the bias. The

decoupling capacitors are used to prevent the leakage of RF signals into the power supplies. These DC blocking and decoupling capacitors are crucial, especially with regard to the circuit layout, since leakage from either the power supplies or RF signal can cause the circuit to behave incorrectly.

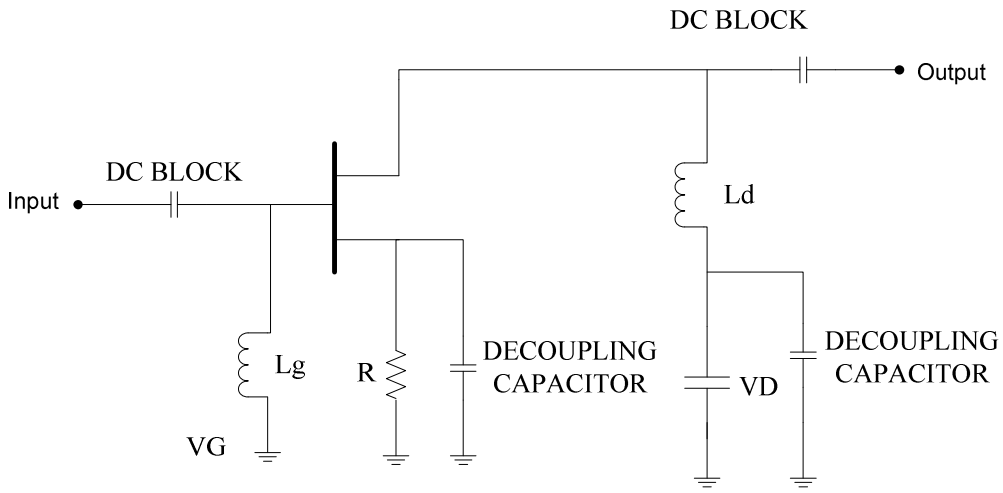
Figure 6-13 shows the bias network topology used in this research.



(a) Inductors as bias chokes



(b) High value resistor



(c) Self-biasing

Figure 6-13 Circuit diagram of different types of bias network

(a) Inductor as bias chokes (b) High value resistor and (c) Self-biasing

In Figure 6-13 (a), the inductors will act as bias chokes. The values of these inductors are usually large (~30 nH) and hence can consume the majority of the die area. The circuit in Figure 6-13 (b) uses a high value resistor for biasing the gate. This method is suitable since, ideally, the gate draws no current, and the high value gate resistor is used to stabilise the device. Therefore, this method is preferable to produce the unconditionally stable circuit as outlined in the specification. Figure 6-13 (c) shows an alternative circuit design biased from a single power supply, V_D. The gate is grounded at DC through either an inductor or resistor. The source is raised to positive voltage by a DC potential to the desired gate-source voltage and hence this is called self biasing. The disadvantage of this technique is that the amplifier is more sensitive to process variations such as changes in the transistor's pinch off voltage. The output parameters of the amplifier might be different from those expected since the bias is fixed during the circuit design. To overcome this problem, a number of different resistors are connected to the source, and the optimum one is selected during testing [94]. This technique, however, increases the circuit complexity especially in the layout design and also results in an increase in chip area.

6.7 MATCHING NETWORKS FOR SINGLE AND DOUBLE STAGES

The optimum matching network is another consideration in LNA design. In the single stage design, the bias network can act as an input and output matching network. In multistage design, the inter-stage matching network can counteract the gain roll off of the transistor, especially when the common source configuration is used, as explained in section 6.5 In some designs, the inter-stage matching network may only have one passive component [93], usually a capacitor. The input and output matching must provide a 50 Ω match over the desired frequency range for the amplifier to be unconditionally stable. A general representation of the two stage amplifier is shown in Figure 6-14.

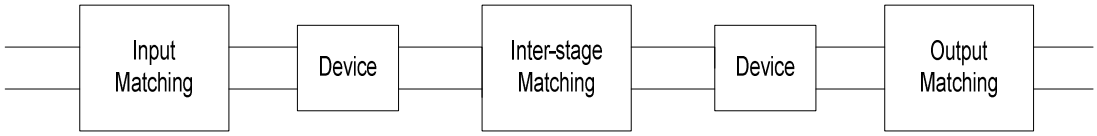


Figure 6-14 A general representation of two stage amplifier

Factors such as complexity, bandwidth, implementation and adjustability need to be considered in designing the matching network. In this project, Agilent's Advanced Design System (ADS) software with the aid of a Smith Chart is used to analyse the matching network of the LNA. This synthesis tools provide solutions to overcome the complex numerical analysis for designing the matching network. Figure 6-15 shows the example of input reflection coefficient (S11) line close to the 50 Ω (middle point) of the Smith chart. The diagram presents the expected plot for a well matched input network.

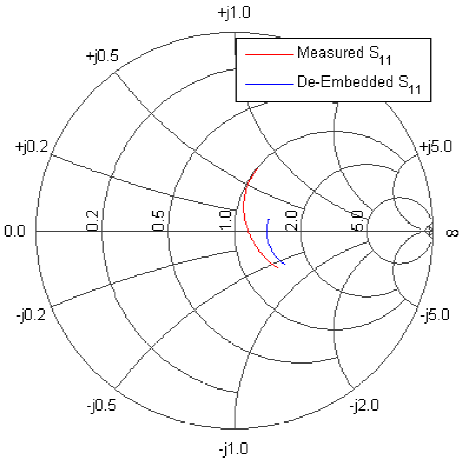


Figure 6-15 A smith chart represents the example of well matched input network [107]

6.8 COPLANAR WAVEGUIDE (CPW)

The final element in the MMIC LNA design concerns the isolation of transmission lines for the active and passive components. The most commonly used transmission line in MMIC designs are: slotline, coplanar strips and coplanar waveguide (CPW) [58]. Figure 6-16 shows the structure of a CPW transmission line. It consists of a signal conductor placed in between two ground plane.

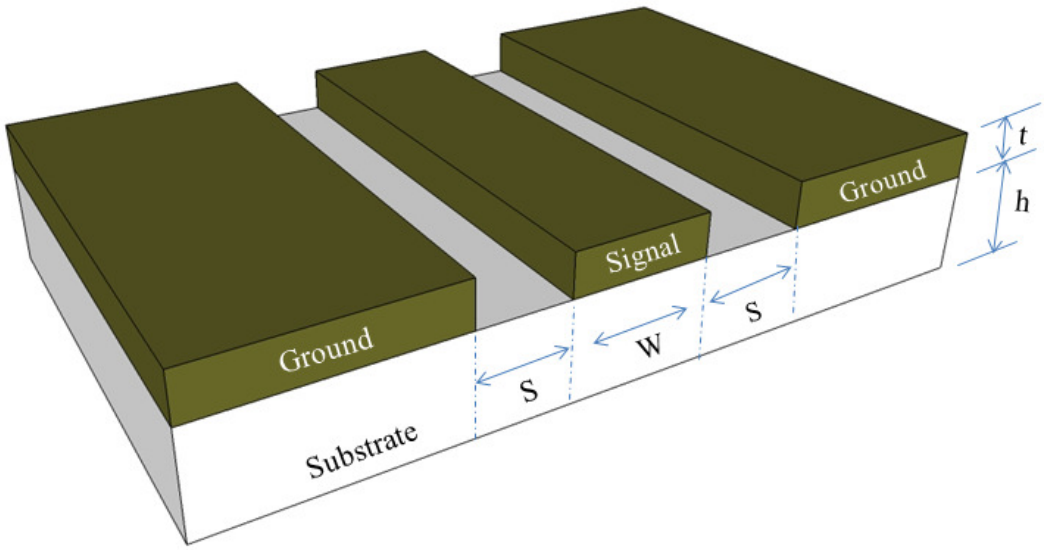


Figure 6-16 Structure of CPW transmission line

In MMIC design, CPW demonstrates circuit isolation due to the fact that the devices and components are always grounded between the traces. Other advantages of CPW are as follows [58, 108]:

In CPW, a device or component can be grounded without the use of via-holes, (compared to microstrip) since the ground-plane lies in the same plane. CPW also suffers from less dispersion effects than microstrip, making it suitable for millimetre wave circuits. The effect of finite dielectric substrate is negligible if the thickness of substrate, h exceeds W + 2S, where W is the metal width and S is the gap or separation. In this project, W = 55 μm, S = 40 μm and h = 300 μm. Moreover, to avoid field radiation in the air, it is also very important to use substrates with a high dielectric constant, ε_r with a recommended value greater than 10. In this project, the ε_r for InP substrate is 12.56. Additionally, a given characteristic impedance can be obtained with almost any track width and gap combination. This enables the design of unique CPW lines with particular impedance. In this project, the characteristic impedance is 50 Ω. However, with relatively thick substrate, CPW allows a wide range of impedance value from 20 Ω to 250 Ω. Finally, lumped elements exhibit less parasitic capacitance since metal back-plating is not required.

Recently, many computer aided design (CAD) packages have started offering CPW models in their libraries, therefore it is being extensively used in MMIC production.

Considering the benefits of CPW discussed in the literature [109-111], and the ease of design using CAD tools, the author decided to use CPW for the in-house MMIC LNA designs. In this work, Agilent ADS software is used for designing CPW transmission lines.

6.9 SUMMARY

As previously discussed, an accurate model for the active device alone is not sufficient as the LNA also consists of passive devices. Therefore, accurate passive models were developed within this project. Various amplifier topologies and DC biased networks which suit the in-house active device are described. The CPW transmission line has many advantages in MMIC design as previously discussed.

Therefore, CPW is chosen as the interconnection line between the active and passive components in this project. Design considerations, as well as matching networks based on the 50 Ω impedance system, are also discussed in this chapter.

From knowledge of optimal circuit topologies, active and passive devices, the complete LNA circuit can be designed for optimum low noise, high gain and unconditionally stable characteristics. The LNA designs are further discussed in Chapter 7 and Chapter 8.

CHAPTER 7

MMIC LNA: SINGLE AND DOUBLE STAGE LNA

7.1 INTRODUCTION

This chapter presents designs and performance measurements of single and double stage MMIC LNAs suitable for SKA applications. The MMIC LNAs described in this chapter employs the transistor model developed in Chapter 5, together with the passives models discussed in Chapter 6. The 4 x 200 µm device described in Chapter 5, fabricated from the VMBE2100 epitaxial layer, is chosen as the active device in the LNA designs.

7.2 LNA DESIGN

The LNAs described in this chapter employ the common source topology to minimise their noise figures; in addition, this topology is less prone to oscillation. The DC bias for these LNAs is optimised at low I_{DS} and $V_{GS,}$ as explained previously in Chapter 4 section 4.2. These biasing conditions provide the required low noise performance, and can also be used in low power applications. The DC bias network utilises a high gate resistor value, which is preferable, to achieve unconditional circuit stability. To reduce the complexity as well as to minimise chip area, the drain side of the LNA is designed to use only a single low value of inductor and resistor, without compromising the output return loss.

There are three types of LNA designs presented in this chapter. The LNA designs are:

1) Single stage single-ended MMIC LNA,
2) Double stage single-ended MMIC LNA (a design with inductor) and
3) Double stage single-ended MMIC LNA (a design without inductor)

The low cost and simple topology for the LNAs described in this chapter meets the project specifications of: high gain, unconditional stability, low power dissipation, small chip area, and most fundamentally, low noise.

7.2.1 Single Stage Single –Ended MMIC LNA

The single stage single-ended (SSLNA) MMIC LNA is shown in Figure 7-1. The LNA was designed for a frequency range of 0.4 GHz to 2.0 GHz, with optimum performance up to 1.4 GHz. The active device used was the 4 x 200 µm depletion mode pHEMT fabricated on sample VMBE2100. The active device T1 was biased at 1 V V_{DS}, 0.22 mA I_{DS} (10% I_{dss}) and -0.92 V V_{GS}. These biasing conditions were optimised for low noise applications as explain in section 4.2.

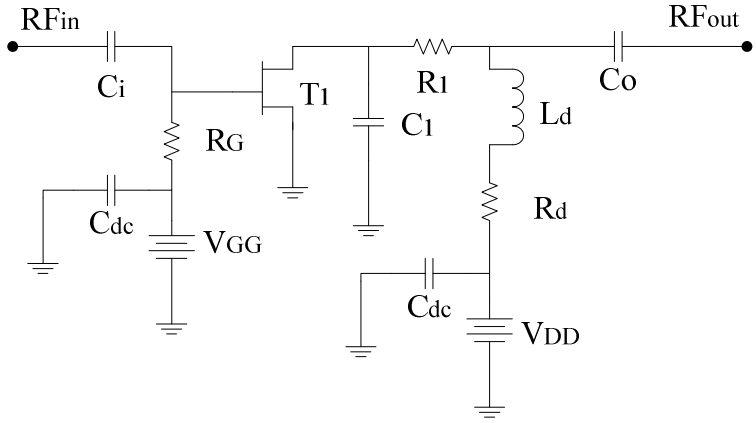


Figure 7-1 Schematic diagram of single stage single-ended MMIC LNA designed using 4 x 200 µm pHEMTs

The biasing for this LNA utilized the common source technique as described in section 6.5. This amplifier uses a high gate resistance (R_G = 3.3 kΩ) at the input terminal of the transistor. This topology prevents a large current flowing to the input gate of the transistor, and hence the optimum DC gate voltage is injected to the transistor (V_{GG} = -0.92 V). Therefore, the transistor was biased for optimum low

noise performance. The increased gate resistance can also minimise the oscillation at low frequency.

The series capacitor, Ci, acts as a DC-block to isolate the DC signal from the DC source, V_{GG}, to the RF input. The coupling capacitor, $C_{dc,}$ prevents RF leakage to the DC sources. The drain capacitor, C_1, was used to improve the input return loss, as well as to provide output matching for the amplifier. The resistor located at the drain side, R_1, prevents oscillations. Since this resistor is placed at the output side of the LNA, it will not affect the noise. However, it can slightly reduce the overall gain of the amplifier. Therefore, to minimise the gain loss, the value of R_1 was minimised. In the design, $R_1 = 60\ \Omega$.

The drain inductor, L_d, and drain resistor, R_d, were used to provide an adequate output match over the wide frequency band, and hence ensure the unconditional stability of the LNA. The use of spiral inductors at the source of an active device can improve the input return loss, yet, due to their resistance, the noise is degraded. For this reason, the use of spiral inductors was avoided for the critical paths.

The output capacitor, C_o, is a DC-block to the drain current, and behaves as an output matching network for the output return loss. The SSLNA mask layout is depicted in Figure 7-2

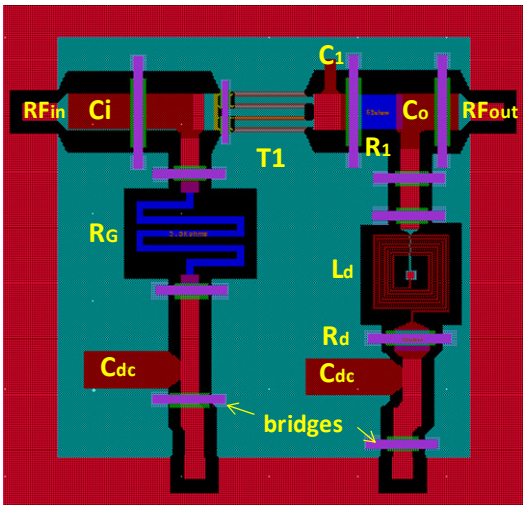


Figure 7-2 Mask layout of single stage single-ended MMIC LNA designed using 4 x 200 µm pHEMTs

7.2.2 Double Stage Single–Ended MMIC LNA

This section describes the two double staged single-ended (DSLNA) MMIC LNA:

1) Design with inductors and,
2) Design without inductors

A two stage topology was used to improve the gain and optimise the noise performance. Since the noise figure of the first stage dominates the noise performance of the entire design, as well as its sensitivity (See Chapter 3 Section 3.4), the first stage was designed to have the lowest possible noise figure. The second stage was used to increase the gain from the first stage and, therefore it was biased to optimise the gain [55].

The active devices used in these designs were based on the 4 x 200 µm pHEMTs with 1 µm gate length, fabricated on VMBE2100. Both LNAs were designed for 50 Ω input and output impedance. The measurements for these LNAs were performed at room temperature only, as required by the design specification.

7.2.2.1 Design with Inductors

This section presents the double stage single-ended MMIC LNA design with inductors as the matching network. The schematic diagram for this design is illustrated in Figure 7-3. In this design, a two single stage single-ended MMIC LNA, as described in section 7.2.1, was cascaded in series using a common source and high gate resistance topology.

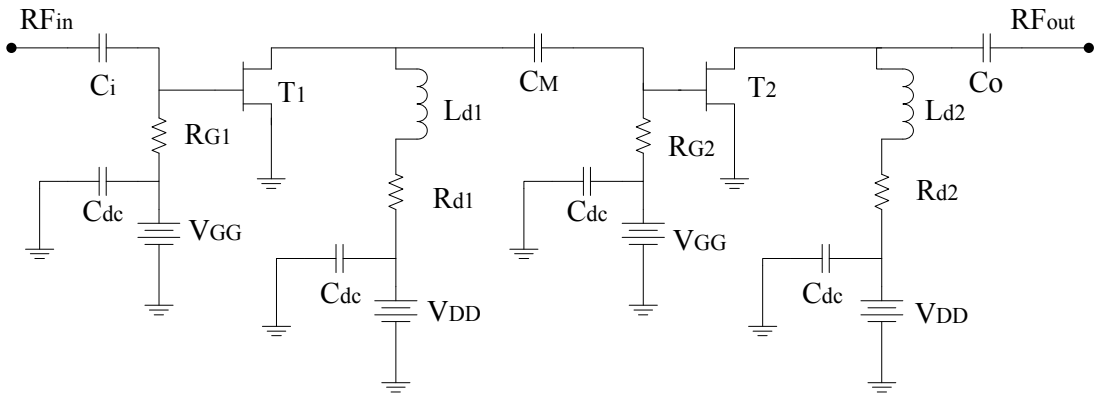


Figure 7-3 Schematic diagram of double stage single-ended MMIC LNA designed using 4 x 200 µm pHEMTs (Design with inductors)

The values for the passive elements in this LNA were adjusted to compensate for the presence of the inter-stage matching network. Therefore, the passive values for this LNA were not the same as those used in the single stage LNA, despite the fact that the circuit was adopted from the single stage design. The passive values were therefore optimised so that the LNA is biased for optimum low noise applications. The overall gain of the circuit is more than adequate, when biased for low noise, to meet the specification of the project. It was therefore unnecessary to alter the biasing of the second stage, which reduced the complexity of the layout. The additional noise benefit from not biasing for high gain was minimal as previously discussed.

Transistors T1 and T2 are biased at 1 V V_{DS}, 10% I_{dss} (~22 mA) and -0.92 V V_{GS}. To achieve these bias conditions, a high gate resistance (R_{G1} = 8 kΩ) was employed for the first stage design as explained previously in section 7.2.1. The capacitor (C_M), inductor (L_{d1}), and resistor (R_{d1}) act as the inter-stage matching network of the LNA. Additionally, C_M is used to isolate the gate DC supply of the second stage from the RF output of the first stage. The value of C_M is 20 pF. Components L_{d1} and R_{d1} improve the input and output return loss, and also improve the amplifier stability at higher frequencies.

The second stage amplifier enhanced the overall gain of the LNA. Due to the presence of the inter-stage matching network, C_M, L_{d1} and R_{d1}, the value of resistor R_{G2} is half that of R_{G1} (R_{G2} = 3.5 kΩ). This is to ensure that transistor T2 achieves the optimum noise bias conditions. L_{d2} and R_{d2} were used for the output matching

network of the amplifier, and also used to provide a good output return loss and to improve the stability of the amplifier.

The series capacitance Ci and Co acts as a DC-block and isolates the RF signal from DC sources V_{GG} and V_{DD}. The decoupling capacitors, C_{dc}, were used to prevent RF leakage into the DC sources. The DSLNA mask layout with inductors is depicted in Figure 7-4.

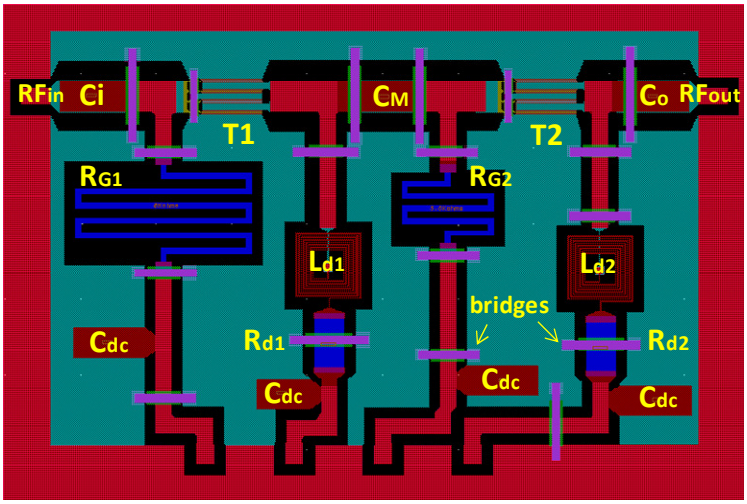


Figure 7-4 Mask layout of double stage single-ended MMIC LNA designed using 4 x 200 µm pHEMTs (Design with inductors)

7.2.2.2 Design without Inductors

For comparative purposes, a double stage single-ended MMIC LNA was also designed without inductors in the biasing network. The schematic diagram for this LNA is shown in Figure 7-5. This design is less complex when compared to the design in section 7.2.2.1 and hence the number of fabrication steps could be reduced.

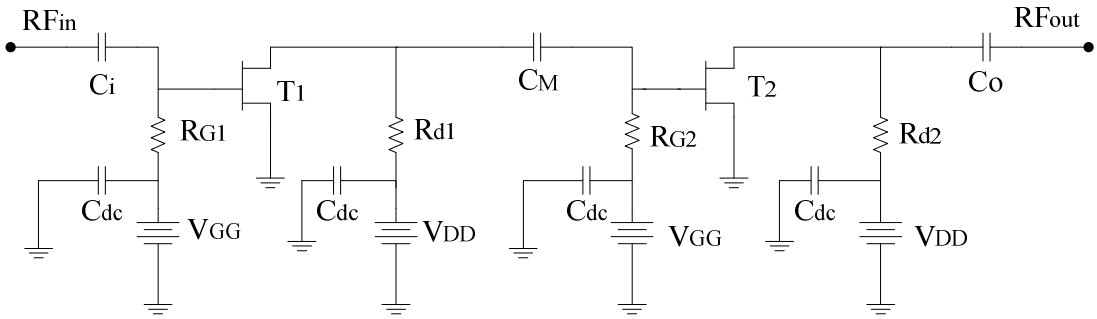


Figure 7-5 Schematic diagram of double stage single-ended MMIC LNA designed using 4 x 200 µm pHEMTs (Design without inductors)

The DC blocking capacitors, Ci and Co, are used to isolate the DC from the RF input and RF output respectively. To prevent the leakage of RF signals to the DC sources, the decoupling capacitors, $C_{dc,}$ are placed in parallel with supply voltages V_{GG} and V_{DD}. The intermediate capacitance, C_M, is used to isolate the gate DC supply of the second stage from the RF output of the first stage.

This design uses the common source configuration with increased gate resistance. The design is symmetrical, with R_{G1} equal to R_{G2}, and R_{d1} equal to R_{d2}. In this design, R_{G1} = 8 kΩ and R_{d1} = 40 Ω. Additionally, C_M and R_{d1} are used as the inter-stage matching network. These components improve the input and output return loss and also improve the stability of the circuit. This design also utilises a small value of C_M for excellent stability performance and R_{d2} provided the output matching of the LNA.

The DSLNA mask layout without inductor is depicted in Figure 7-6.

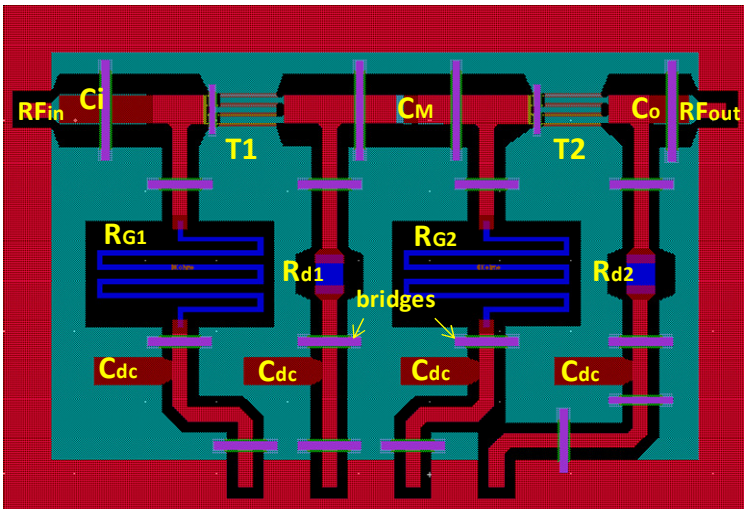


Figure 7-6 Mask layout of double stage single-ended MMIC LNA designed using 4 x 200 µm pHEMTs (Design without inductors)

7.3 SIMULATION AND MEASUREMENT RESULTS

The single stage and double stage LNAs fabricated on sample VMBE2100 are shown in Figure 7-7.

Figure 7-7 A final product of single stage and double stage InGaAs/InAlAs/InP pHEMT MMIC LNAs fabricated at The University of Manchester

The S-parameters measurements of the single stage LNA were carried out at the University of Manchester. However, due to the limitations of the available measurement equipment, the S-parameters measurements for the double stage LNA were performed at the University of Cantabria, Spain.

The noise figure measurements for all LNA designs were also performed at the University of Cantabria. The measurements were carried out in a 50 Ω environment at room temperature. The measurement frequency range was from 400 MHz to 4.2 GHz with a step of 10 MHz (401 points). The power of the General-Purpose Network Analyser (GPNA) generator is -20 dBm, with an intermediate frequency (IF) bandwidth of 1 kHz. A short-open-load-thru (SOLT) calibration standard with two ports was applied to the CS-5 substrate as depicted in Figure 7-8. A complete setup for noise figure measurement is illustrated in Figure 7-9.

The measured noise characteristics and S-parameters for all three designs are presented in the following sections.

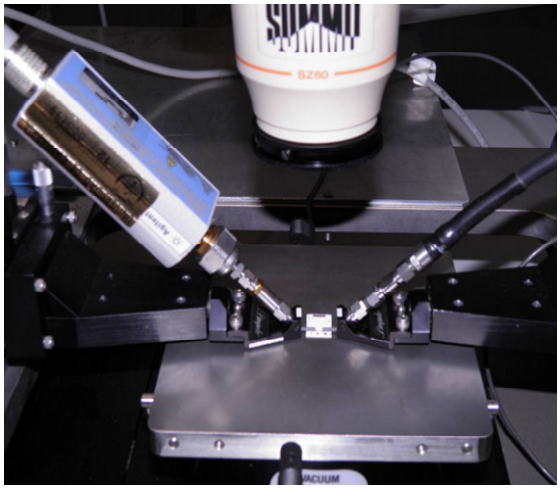


Figure 7-8 A calibration standard of two ports network (CS-5 substrate)

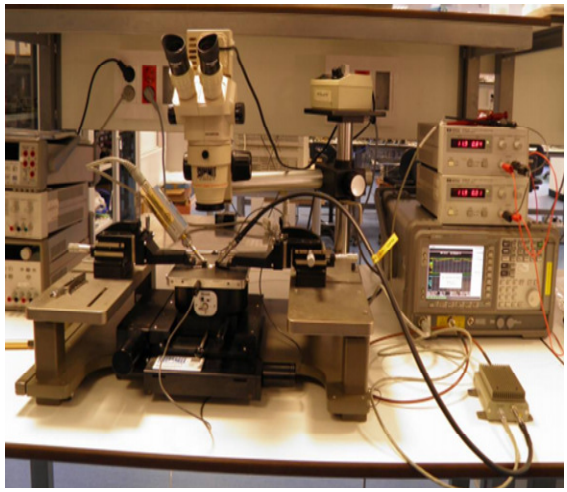


Figure 7-9 A complete setup for noise figure measurement

7.3.1 SSLNA: Simulation and Measurement Results

Firstly, the passive components needed to be replaced with real modelled passives as explained in section 6.2.1. Then, the complete LNA schematic was required to be

transformed into a layout for a mask to be generated before the fabrication process could be started. In this project, Agilent's ADS software was used for the layout designs. The simplified fabrication process flow is presented in Appendix D.

A comparison between modelled and measured S-parameters for a single stage, single-ended MMIC LNA is shown in Figure 7-10 to Figure 7-14 for sample VMBE2100. The data was compared over the frequency range of 0.4 GHz to 2 GHz. The measured S-parameters showed excellent agreement with the modelled data.

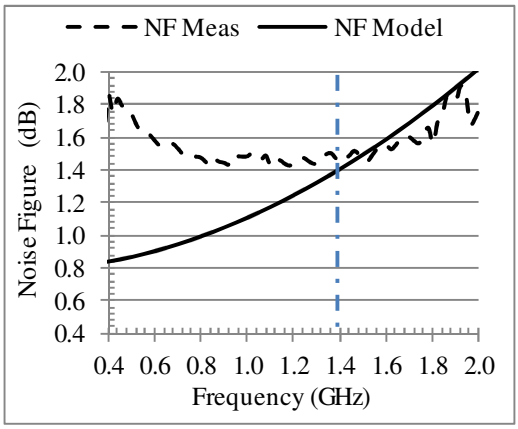


Figure 7-10 Graph of comparison between measured and modelled noise figure, *NF* against frequency

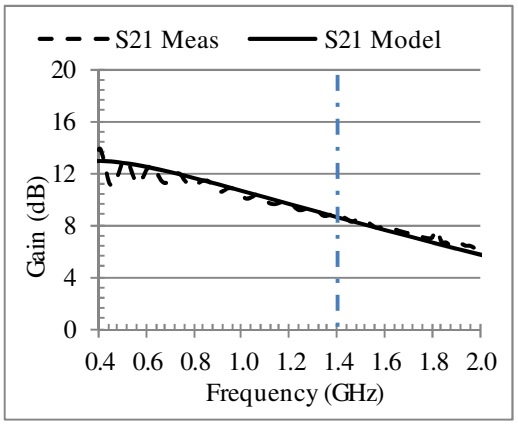


Figure 7-11 Graph of comparison between measured and modelled gain, S21 against frequency

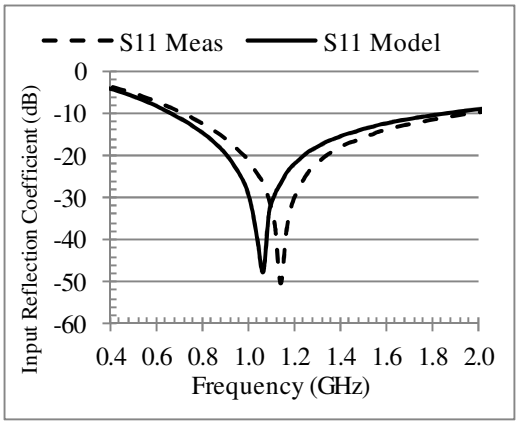


Figure 7-12 Graph of comparison between measured and modelled input reflection coefficient, S11 against frequency

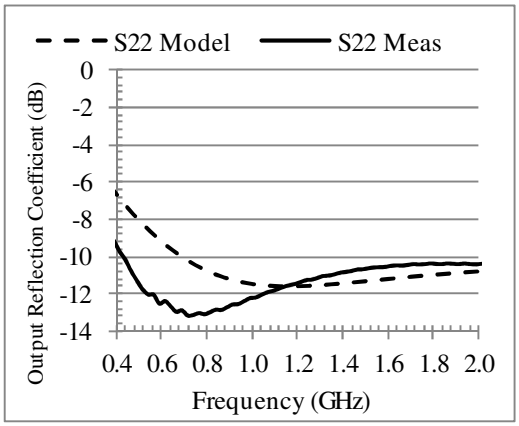


Figure 7-13 Graph of comparison between measured and modelled output reflection coefficient, S22 against frequency

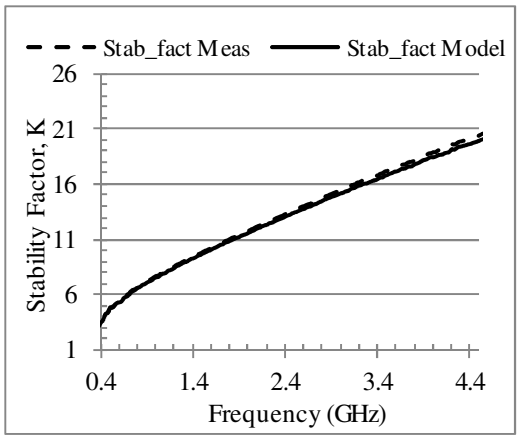


Figure 7-14 Graph of Rollet stability factor, K

The modelled gain perfectly overlaps the measured data over the frequency band of interest. The measured gain of 13 dB at 0.4 GHz and 9 dB at 1.4 GHz is considered small for the SKA and wireless applications. Hence the double stage LNAs are introduced to boost up the gain as discussed in section 7.3.2 and 7.3.3

The input and output reflection coefficients (S11 and S22) demonstrated a very good input and output match. There was a difference of only ~2 dB between the measured and modelled S22 at frequencies of less than 1 GHz, as depicted in Figure 7-13.

The LNA was unconditionally stable up to 10 GHz. However, for comparative purposes with other circuits, the stability factor, K is only shown up to 5 GHz (Figure 7-14).

Taking averages of the measured data, the noise figure (*NF*) shows a wider gap between measured and modelled values at low frequency, and begins to converge at higher frequency. The difference between the measured and modelled *NF* is ~1 dB at 0.4 GHz and 0.3 dB at 1 GHz. The degradation in noise performance was therefore investigated. This was correlated with both the effect of leakage in the pHEMT on the noise at low frequency [106], and mismatches due to the lumped passive elements used in the circuits. Since the circuit is relatively simple and has no matching network at the input, only the MIM capacitor (Ci) contributed to the noise. As explained in 6.2.1.2 , the MIM capacitor has series resistance due to the top and bottom plates. However, this series resistance is small and is already accounted for in the model. Therefore, it may not be the cause of the degradation in noise

performance. According to R. Simon [108], CPW suffer from dispersion at low frequencies. The CPW must maintain the same potential at both ground planes to prevent unwanted modes from propagating. If the grounds are at different potentials, the CPW mode will become uneven, with a higher field in one gap than the other, which might therefore affect the characteristics of the circuit. To overcome this problem, ground straps or bridges are used to connect the ground planes as illustrated in Figure 7-2, Figure 7-4 and Figure 7-6.

Another possible cause of mismatch is due to poor Q factor of the inductor. From the parasitic parameters extraction, the Q factor of the inductor can be calculated from Equation (7-1) which shows that the Q factor at low frequency (< 1 GHz) is less than 0. Typically, a good Q factor for an inductor is 10 [111]. One can therefore observe a large mismatched of noise at low frequency.

$$Q = \frac{2\pi f L}{R_s} = 1\ x\ 10^{-9} * f \qquad 7\text{-}1$$

The low Q value of the inductor can be corrected by using a large inductor value in the design. But a large inductor value will increase the chip area, which is therefore a trade-off in MMIC designs.

The final in-house fabricated, single stage single-ended MMIC LNA, designed using the 4 x 200 µm InGaAs/InAlAs/InP pHEMT, is shown in Figure 7-15. The chip size for this LNA is 1.5 x 1.5 mm^2. With V_{DD} = 3 V and a drain current of 15.6 mA, this LNA consumed only 47 mW of power.

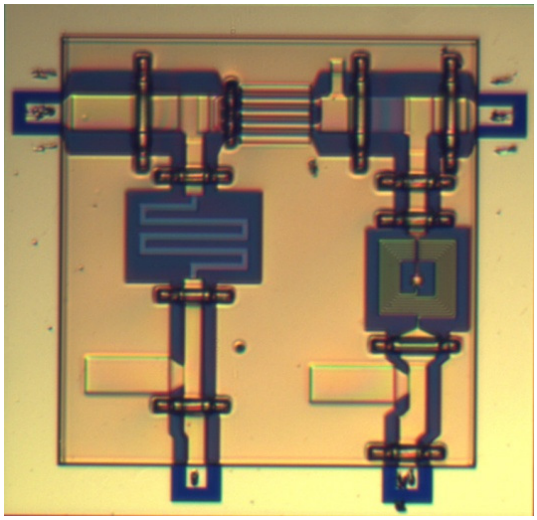


Figure 7-15 Picture of in-house fabricated single stage single-ended MMIC LNA designed using 4 x 200 µm pHEMTs

The excellent agreement between measured and modelled data obtained in this section verifies that the linear, nonlinear and passives models described in Chapter 5 are accurate.

7.3.2 DSLNA (with inductor): Simulation and measurement results

Figure 7-16 and Figure 7-17 shows measured versus modelled data of noise figure (*NF*) and gain (S21) respectively. The measured data was compared with the simulated data over the frequency range of 0.4 GHz to 2 GHz. The measured NF is 0.5 dB higher than the simulated value at the lower frequency and ~ 0.3 dB higher at the higher frequency. As explained in section 7.3.1, the difference between the modelled and measured NF could be due the leakage in the pHEMT, and the dispersive nature of CPW [106]. However, the most likely cause is the low Q factor of the inductor. Since this design uses two inductors as intermediate and output matching networks, the mismatches can be seen not only at low frequency but also at high frequency. To study the effect of the inductor in the circuit design, the next DSLNA, design without inductor is introduced and discussed in the section 7.3.3

The gain, on the other hand, shows excellent agreement between the measured and modelled data. The measured gain for this design was 36 dB at 0.4 GHz,

approximately 23 dB higher than the single stage design. At 2 GHz, the gain was 23 dB, whereas the single stage LNA had a gain of 6 dB

The reflection coefficients and stability factor for this amplifier are depicted in Figure 7-18 and Figure 7-19 respectively. There is no measured S-parameters data, hence no comparison to the modelled is made. However, the excellent agreements between measured and modelled data presented previously in the single stage design verified that the simulated data is accurate. The LNA demonstrated unconditional stability over 10 GHz with good input and output reflection coefficients.

With a 3 V DC supply and the collective current for both the stages is 41.6 mA, this LNA had a net power consumption of 125 mW.

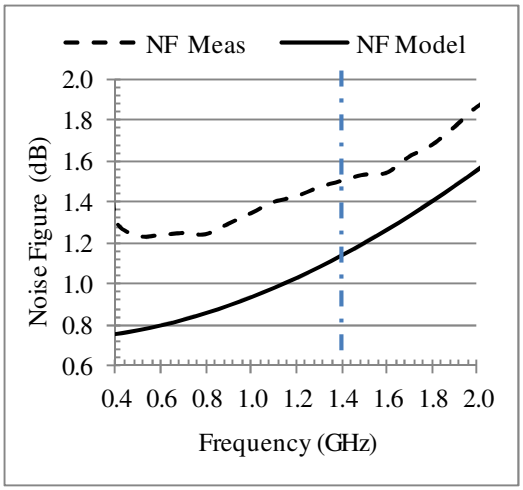


Figure 7-16 Graph of comparison between measured and modelled noise figure, *NF* against frequency

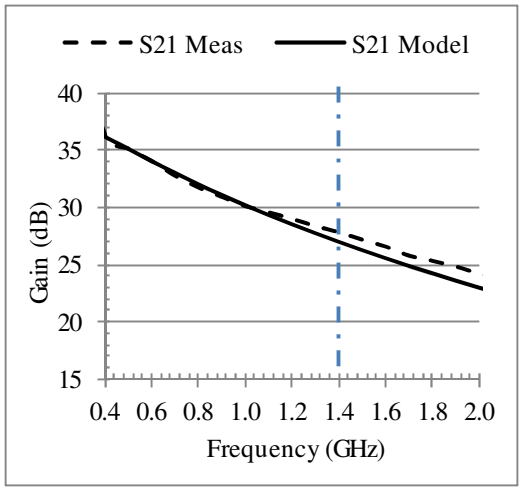


Figure 7-17 Graph of comparison between measured and modelled gain, S21 against frequency

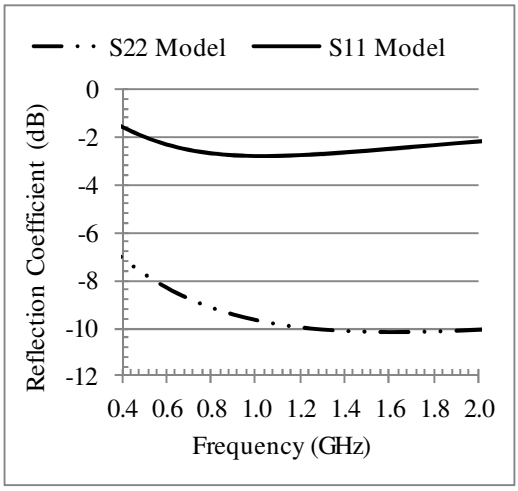


Figure 7-18 Graph of modelled input, S11 and output reflection coefficient, S22 against frequency

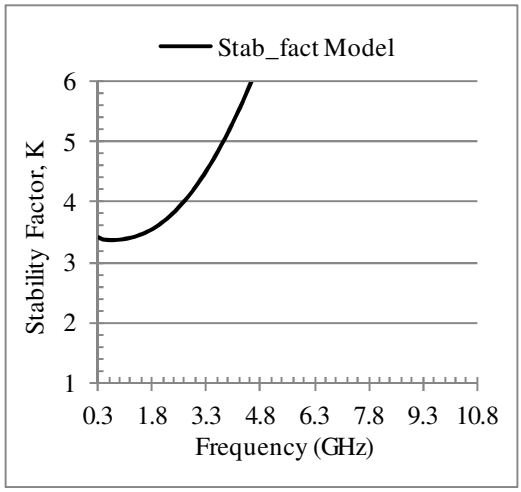


Figure 7-19 Graph of Rollet stability factor, K

The completed layout for the double stage, single-ended MMIC LNA (designed with inductors) is shown in Figure 7-4. The measured inductor size is 14 nH. The LNA is designed using a 4 x 2 00 µm InGaAs/InAlAs/InP pHEMT and the chip size is 1.6 x 2.5 mm^2. The fabricated LNA is illustrated in Figure 7-20.

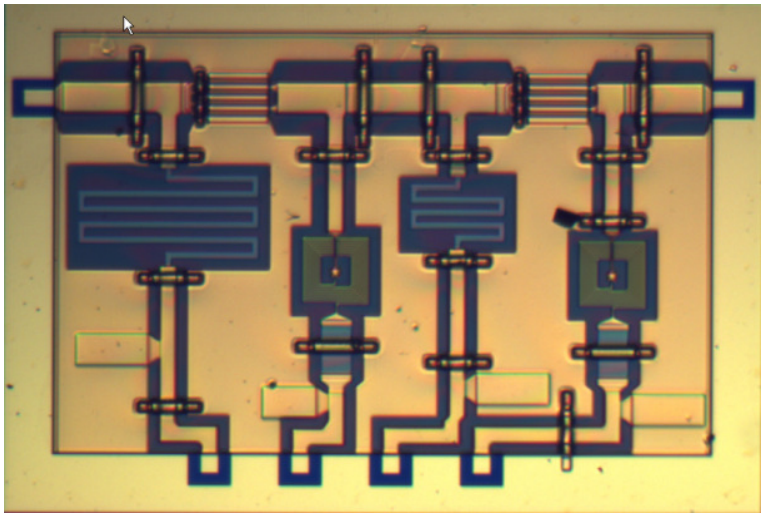


Figure 7-20 Picture of in-house fabricated double stage single-ended MMIC LNA designed using 4 x 200 µm pHEMTs (Design with inductors)

7.3.3 DSLNA (without inductor): Simulation and measurement results

This LNA design had no measured data for reflection coefficient or stability factor. Therefore, only *NF* and gain is compared with the measured data. Figure 7-21 shows the modelled and measured *NF* - this LNA design offered a noise figure performance comparable to the LNA designs with inductors. There are still discrepancies between measured and modelled *NF* of 0.4 dB even though no inductor is used in this design (therefore the low Q factor value of the inductor is not the reason for this *NF* mismatch).

Thus, further research has been carried out, which suggests that the difference between measured and modelled *NF* might be due to the capacitor's Q factor. The Q factor for capacitor is shown in equation (7-2).

$$Q = \frac{X_c}{ESR} \qquad 7\text{-}2$$

Q is the Quality Factor, ESR is the equivalent series resistance in ohm and X_c is the absolute value of the capacitance reactance in ohm.

Referring to section 6.2.1.2, the MIM capacitor model has its own parasitic series inductors and resistors. From parameter extraction, the 25 pF capacitor will introduce series inductances of 2 pH, series resistances of 2 Ω and a parallel transconductance of 1000 Ω^{-1}. Therefore, the total ESR will be 2 Ω. From calculations at 1 GHz, Q factor for C = 8 pF and 25 pF is 9.95 and 3.18 respectively. Smaller capacitor values tend to have higher Q factors [96]. Thus, by using smaller capacitor values, the low Q factor can be corrected. This is another design trade-off as a large value MIM capacitor is very important in MMIC LNAs to isolate the RF signal from the DC supply.

Figure 7-22 shows the modelled and measured gain. The gain specification for this design is moderate (~25 dB to 17 dB) as a precaution to reduce the effect of oscillation resulting from the higher gain obtained in the previous design. The gain achieved in the previous two stage design was ~36 dB to 23 dB over the frequency range of interest. In conclusion, the double staged designs fabricated at the University of Manchester are unconditionally stable and behave as simulated.

The input and output reflection coefficient was improved in this design as compared to the design in section 7.2.2.1. The LNA and is also unconditionally stable over 10 GHz with better Rollet stability factor, K.

The power consumption for this design is 132 mW, with 22 mA drain current at each stage and 3 V voltage supply. This drain current is higher when compared to the previous designs, and is due to the low resistance value of the output matching for both stages.

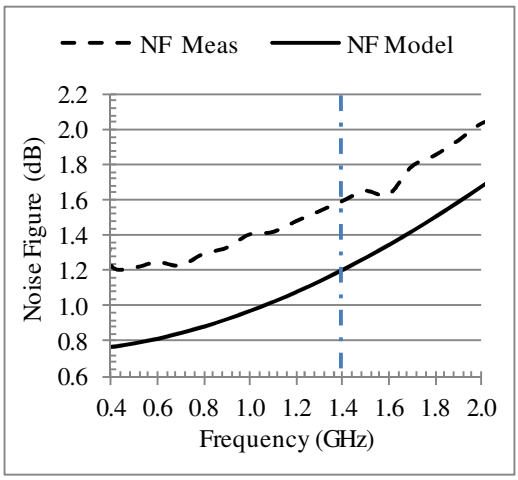


Figure 7-21 Graph of comparison between measured and modelled noise figure, *NF* against frequency

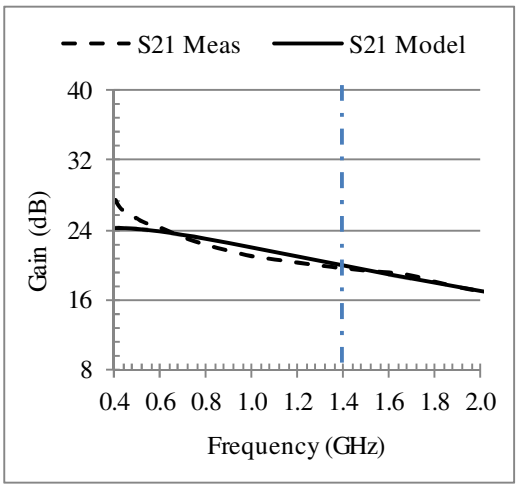


Figure 7-22 Graph of comparison between measured and modelled gain, S21 against frequency

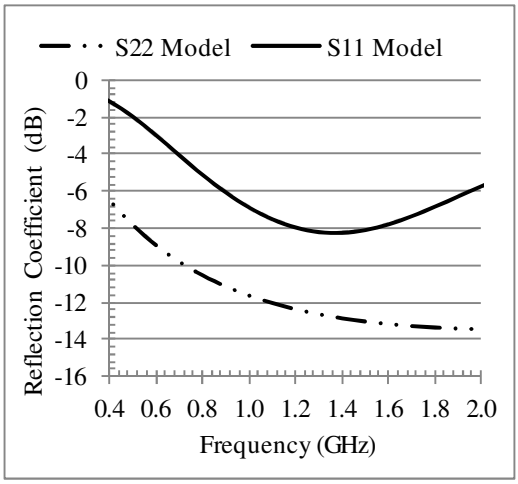


Figure 7-23 Graph of modelled input, S11 and output reflection coefficient, S22 against frequency

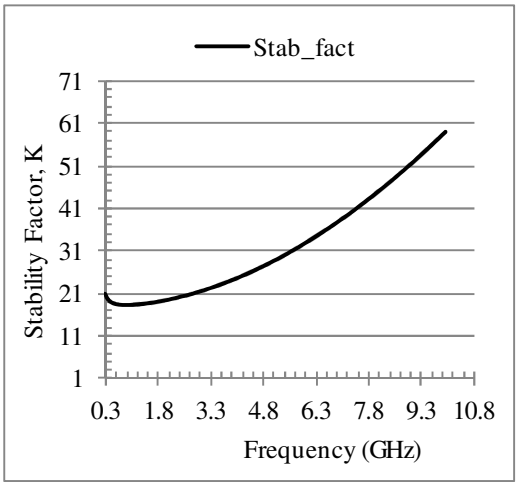


Figure 7-24 Graph of Rollet stability factor, K

The complete layout for the double stage single-ended MMIC LNA (design without inductor) is shown in Figure 7-4. The LNA was designed using the 4 x 200 µm InGaAs/InAlAs/InP pHEMT, with 1 µm gate length. The chip size was 1.8 x 2.7 mm^2. The fabricated LNA is illustrated in Figure 7-25.

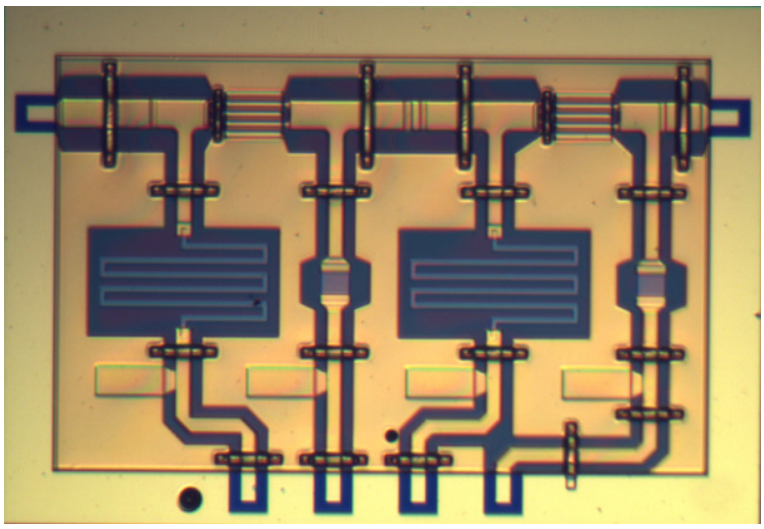


Figure 7-25 Picture of in-house fabricated double stage single-ended MMIC LNA designed using 4 x 200 µm InP pHEMTs (Design without inductors)

7.4 COMPARISONS WITH OTHER LNA DESIGNS

Table 7-1 shows a comparison of the in-house fabricated LNA with LNA designs from other researchers. These LNAs were designed for the same frequency range and thus meaningful comparisons can be made.

Firstly, using 0.2 µm GaAs technology with a dual-loop negative feedback topology, the LNA from J. Xu, *et al.* [112] has achieved a simulated *NF* of 0.5 dB across 0.6 – 1.6 GHz frequency range. This LNA employed an off-chip inductor at the input, and therefore a low noise figure is to be expected. Furthermore, the chip area of the LNA is assumed to be large due to the off-chip inductor in the design. The power dissipated for this LNA is 1000 mW, which is 10 times the power dissipated in our circuits.

In their paper, L. Belostotski and J. W. Haslett [113] report a sub 0.2 dB *NF* using 90 nm CMOS technology. The *NF* was simulated across a frequency range of 0.8-1.4 GHz, and matched to 85 Ω source impedance. The size of this LNA is small due to the smaller CMOS technology used. The advantage of this nanotechnology is its small drain current, which results in low power consumption. The power consumption for this LNA is 43 mW. The noise figure and power consumption of this LNA would however be considerably affected if it were to be interfaced to a standard 50 Ω impdedence system. This design also uses an off chip matching resistor and inductors.

The double stage LNA reported by R. H. Witvers [114] achieved a noise figure of less than 0.4 dB.This low *NF* is produced via two mechanisms:

1) large off-chip inductance [115], and
2) matching to high input impedance of 150 Ω [116, 117].

Additionally, the first stage design utilized 6 gate fingers and the second stage used 4 gate fingers. It is noted that a larger device for the first stage provides an overall benefit to the *NF* as it will have a low noise resistance (R_n). The design utiliesd GaAs technology without defining the gate length, even though an e-beam fabricated 70 nm gate length is implied. The design was stable over the frequency range of interest.

Kruger [118] has demonstrated excellent *NF* using commercial GaAs. The measured *NF* was reported to be 0.36 dB across the frequency range of 0.9-1.8 GHz. This LNA used a multipath technique as discussed in [104]. The LNA is matched to a 50 Ω input and output impedance. The design was unconditionally stable, had considerably high gain (27 dB), and dissipated only 100 mW. However, the LNA had a considerable size of 46 x 35 mm^2, due to the discrete components used.

In this project, InP technology with 1 μm gate length was used to design the MMIC LNA. The LNA was fabricated using conventional optical lithography at the University of Manchester. The measured NF of < 1.5 dB is larger than that simulated, largely due to the effect of leakage in the pHEMT [102], mismatches due to the lumped passive elements and CPW transmission lines used in the circuits [108]. This low cost, optically processed LNA provides a high gain of 36 dB with a

low power dissipation of 125 mW, when compared to the majority of LNAs which use off-chip matching components. The chip area for this LNA is 1.6 x 2.5 mm^2.

Table 7-1 Table comparing the in-house fabricated LNA with the LNA obtained by other researchers

Reference	[112]	[113]	[114]	[118]	This work
Year	2005	2007	2010	2012	2012
Bandwidth (GHz)	0.6-1.6	0.8-1.4	0.6-1.8	0.9-1.8	0.4-1.4
Technology	GaAs 0.2 µm	CMOS 90 nm	GaAs	GaAs Commercial	InP 1 µm
Noise Figure (dB) (*Sim/Meas*)	0.5 *Sim*	[3] < 0.2 *Sim*	[4] < 0.4 *Meas*	0.36 *Meas*	*<1.5 Meas*
Gain (dB)	21	17	22	27	36
Power Consumption (mW)	1000	43	Not Available	100	125
Stability	[1]Stable	Not specified	[1] Stable	Unconditionally stable	Unconditionally stable
Impedance (Ω)	50	[3] 85	[4] 150	50	50
LNA Size (mm)	[2]Off-chip inductor	[3]1.1 x 0.75	[2] Off-chip inductor	46 x 35	1.6 x 2.5

1 Authors does not mention the stability condition, either unconditionally stable or conditionally stable.

2 The LNA size is expected to be large due to the off-chip component.

3 Simulated at 85 Ω input impedance. Used off-chip resistor and inductors.

4 Measured 150 Ω input impedance.

7.5 SUMMARY

In this chapter, three MMIC LNAs designs were presented. The active device used in these designs had a 4 x 200 µm gate width and 1 µm gate length. A common source configuration with a high value of gate resistance was used for the LNA designs.

The simulated data shows an excellent agreement with the measured data for all parameters except the noise figure over the required frequency range of 0.4 to 1.4 GHz. The discrepancies between the measured and modelled *NF* was discussed. The calculation of the passives' Q factor has shown that a low Q factor value has caused

this mismatch. The requirement to improve the Q factor values are addressed at the end of the discussion. Overall, the excellent match of measured and modelled data for the wide frequency band verified the models used in the designs.

A gain of 36 dB was achieved from the double stage design and this met the design specification. The power dissipation for all LNAs is considered small for a 1 µm gate length process. The highest power, consumed by the double stage design without an inductor, was only 132 mW. Unconditional stability was one of the design goals for these LNAs. The LNAs demonstrated unconditional stability, with the stability factor, K above one (1) to over 10 GHz.

The results achieved from these measurements have enhanced the confidence in the techniques used to design the MMIC differential LNA described in the next chapter.

CHAPTER 8

MMIC LNA: DIFFERENTIAL TO SINGLE ENDED LNA

8.1 INTRODUCTION

This chapter extends the contributions of previous work discussed in Chapter 7. The differential input to single-ended output LNA is of interest since some elements of the Square Kilometre Array (SKA) project utilise differential output antennas. A differential input amplifier is therefore chosen, and will be interfaced with a differential output receiving antenna. A differential LNA with single-ended output is also preferable for adaptation of the circuit to the subsequent stages in the analogue chain.

The SKA is a future radio telescope that will have one square kilometre of effective collecting area and operates up to a frequency of 1.4 GHz. A low noise figure and power dissipation for the ~10^7 receivers [119] are therefore essential elements for the underlying feasibility of the SKA. This chapter discusses a series of double stage differential LNA designs that can be integrated into the SKA or other wireless communication applications. All designs are optimised for the frequency range of 0.4 to 1.4 GHz

The design of a double stage differential to single-ended MMIC low noise amplifiers (LNA) is presented in this chapter. This LNA is based on novel high breakdown InGaAs/InAlAs/InP pHEMTs that have been developed and fabricated at the University of Manchester, as discussed in Chapter 5. The fabricated devices employ various gate widths (from 100 to 1200 μm), with the gate length optimised at 1 μm for both RF and noise performance. The source-gate and gate-drain separation are both 2 μm. The effects of device scaling are also discussed in Chapter 5, and the advantages of using different device sizes are also discussed in this chapter.

8.2 DIFFERENTIAL AMPLIFIER TOPOLOGY

Two basic configurations of differential amplifier designs were used throughout this project [105]. Figure 8-1 shows the differential input (V_{G1} and V_{G2}) and differential output (O_{ut1} and O_{ut2}) arrangements, while Figure 8-2 shows a differential input (V_{G1} and V_{G2}) and single-ended output (O_{ut}) topology. The operation of these circuits was based on the ability to fabricate matched components on the same chip i.e. T_1 equal to T_2 and T_3 equal to T_4, and both load resistors, R_L fabricated with equal values.

Since all circuits in this project contain not only differential elements, but also a matching network, further design explanations are necessary and are described in the next sub-sections.

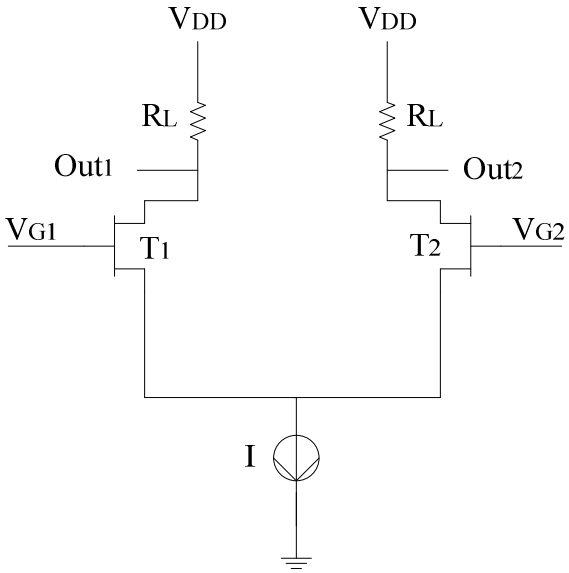


Figure 8-1 Schematic diagram of differential input and differential output topology.

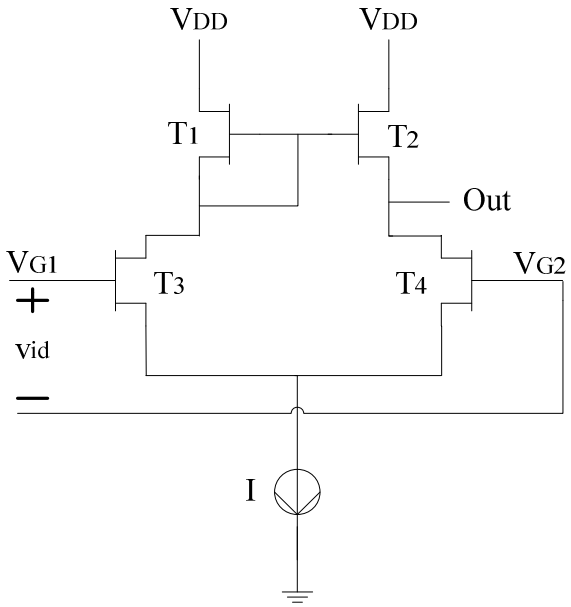


Figure 8-2 Schematic diagram of differential input and single output topology.

8.3 DIFFERENTIAL AMPLIFIER DESIGN

In this section, four different configurations of differential input to single-ended output LNA are designed to meet these specifications:

1) Low noise figure over the frequency range of 0.4 – 1.4 GHz
2) Input and output reflection coefficient less than -8 dB
3) Flat and moderate gain ~25 dB
4) Low power dissipation
5) Unconditionally stable

In all differential amplifier designs, the LNA circuit takes the double stage configurations. To make the explanations simpler, these abbreviations are used throughout this chapter:

1) **DISO** = Differential Input Single Output
2) **SISO** = Single Input Single Output

The designs are detailed in the following section.

8.3.1 Input Stage: DISO and Output Stage: SISO Resistive Biasing (Design 1)

Figure 8-3 shows the schematic of a two stage differential to single-ended MMIC LNA using resistive biasing technique. The first stage is a DISO topology, while the second stage is a SISO design. Input and output impedance was designed to be 50 Ω, and the power supply 3 V.

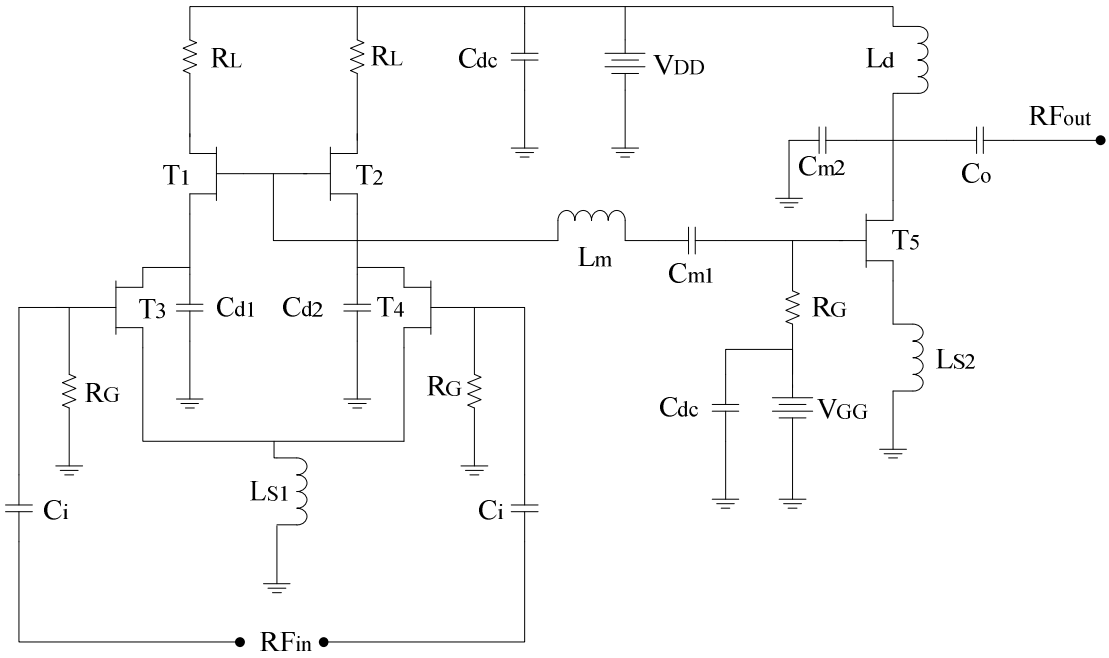


Figure 8-3 Schematic diagram of differential to single-ended MMIC LNA: Input Stage: DISO and Output Stage: SISO Resistive Biasing.

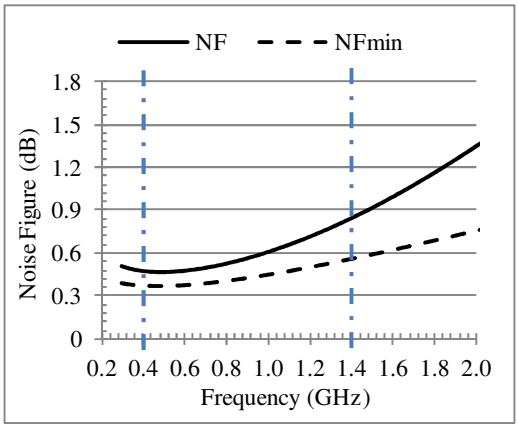
According to Friss [55] (low noise amplifier concepts in multistage designs), the first stage must be optimised for noise performance, and subsequent stages for gain boosting. Therefore, in this design the differential stage is optimised for noise, while the second stage is used to improve the gain.

The differential stage utilises transistors T_1 to T_4, and the output stage uses only transistor T_5. Transistors T_1 and T_2 are active loads, with a width of 2 x 50 µm to minimise the first stage noise (a small transistor has a low minimum noise figure, NF_{min}). Transistors T_3 and T_4 have a large gate width of 4 x 200 µm and are used as the main RF input. These large transistors are biased for low noise at 1 V V_{DS} and 10% I_{dss} as explained previously in Chapter 5. The large transistors can also provide

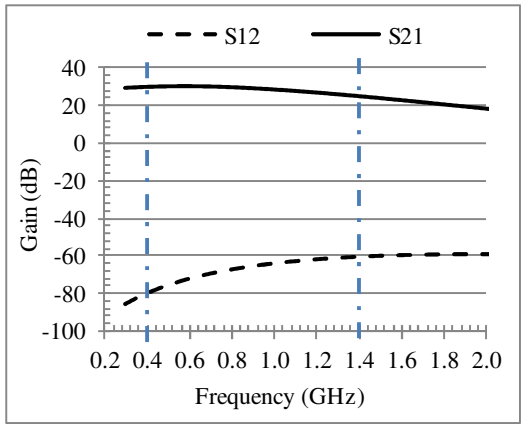
lower noise resistance, R_n and hence improved input matching can be achieved in the LNA design. The second stage was designed to improve the overall gain of the LNA, utilising the 4 x 200 µm T_5 transistor as a large gate width transistor has a large g_m and hence high gain.

Transistors T_3 and T_4 were biased for optimum noise performance i.e. 10% I_{dss} (~20 mA), V_{DS} around 0.5 to 1.5 V and V_{GS} = -0.7 V. The constant-current source was used to drain approximately 40 mA of current under saturation conditions i.e. 20 mA for each leg of the differential pair. From simulation, the actual biasing for T_3 and T4 are 10% I_{dss} = 19.5 mA, V_{DS} = 1.04 V and V_{GS} = -0.7 V. These are the correct biasing conditions for the transistors to operate as intended. The biasing for transistors T_1 and T_2 is not of primary concern since these transistors act as active loads.

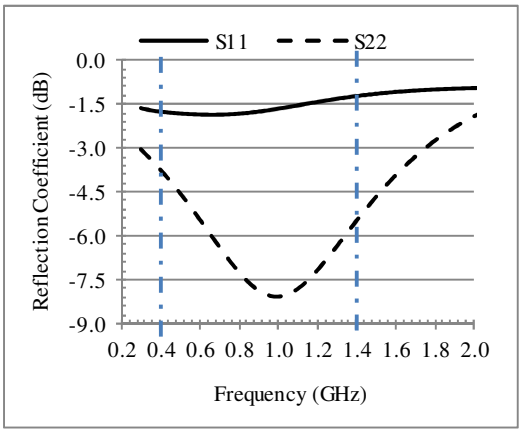
The power handling was also an important design issue. Therefore, the second stage (output) transistor T_5 was biased so that it could improve the gain, yet minimise the power consumption. As explained in Chapter 5, for higher gain, the transistor must be biased at higher drain current, I_{DS}. However, a higher I_{DS} would automatically result in a higher power dissipation. Since the gain of the first stage gain was adequately high (around 11 to 15 dB), only a marginal increase in gain would be required to ensure that the design meets the project specifications as described in section 8.3. Therefore, it was decided to bias transistor T_5 so that it minimises power dissipation, and yet provides the necessary gain. As a result, transistor T_5 is biased at V_{GS} = -0.74 V, I_{DS} = 20 mA and V_{DS} = 2 V. These bias conditions are in the efficiency region (referring to section 4.2). The power consumption for this design was 180 mW which was almost half of the power consumption reported by S. Arshad*, et al* [120]. S-parameters for the design are illustrated in Figure 8-4**.**



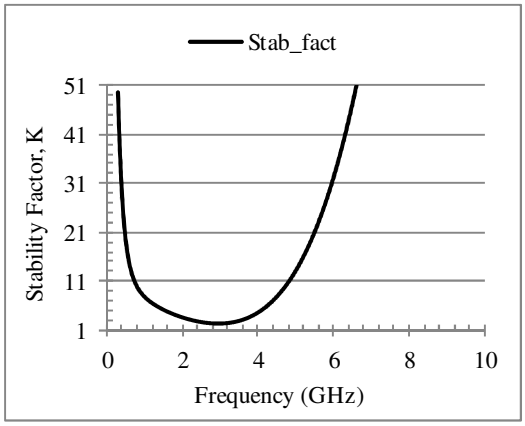
(a) Graph of minimum noise figure, *NFmin* and noise figure, *NF* against frequency



(b) Graph of forward (S21) and reverse (S12) gain against frequency



(c) Graph of input (S11) and output (S22) reflection coefficient



(d) Graph of Rollet stability factor, K

Figure 8-4 Graphs of simulated S-parameters for differential to single-ended MMIC LNA: Input Stage: DISO and Output Stage: SISO Resistive Biasing.

The design was unconditionally stable up to a frequency of over 10 GHz. The noise figure, *NF* was also less than 0.83 dB, with a gain of approximately 25 dB over the frequency range of 0.4 to 1.4 GHz. The design also provided a good output reflection coefficient (S22). As expected, the input reflection coefficient (S11) was severely compromised at -1.3 dB due to the high gain and low noise design. The next design in section 8.3.2 is presented to address this issue of compromised S11.

8.3.2 Input Stage: DISO and Output Stage: SISO Resistive Biasing (Improve S11) (Design 2)

In this design, all biasing conditions, bias networks and matching are similar to the LNA design in section 8.3.1 , allowing direct comparison of each S11 figure. The only differences are the small inductances added to the source tail of transistors T_3 and T_4 as depicted in Figure 8-5. The inductances are used to improve the S11 [121]. Figure 8-6 shows the S-parameters for the design.

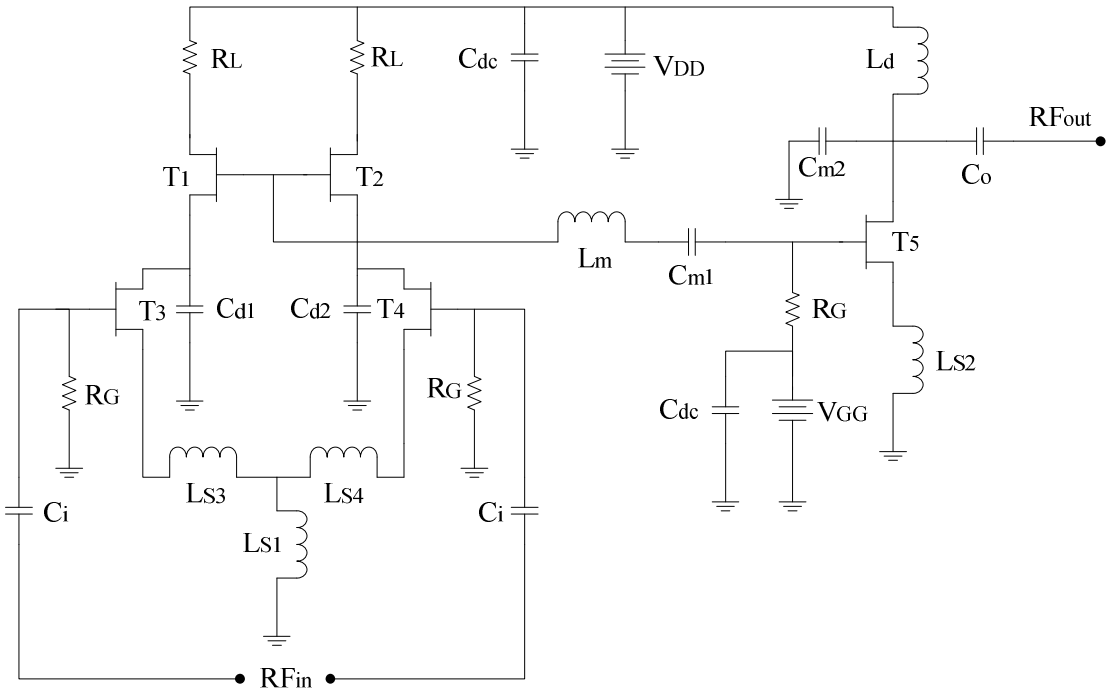
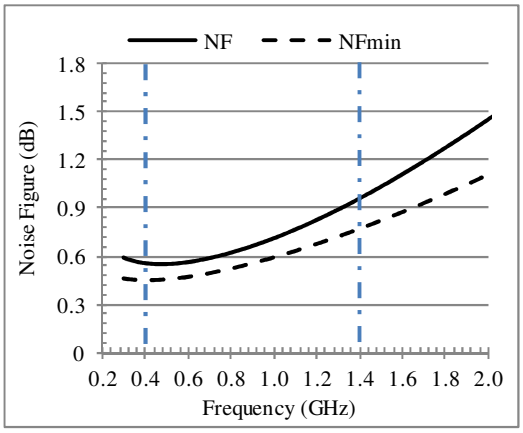
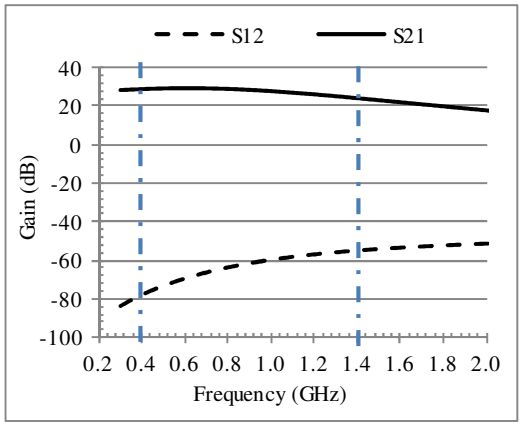


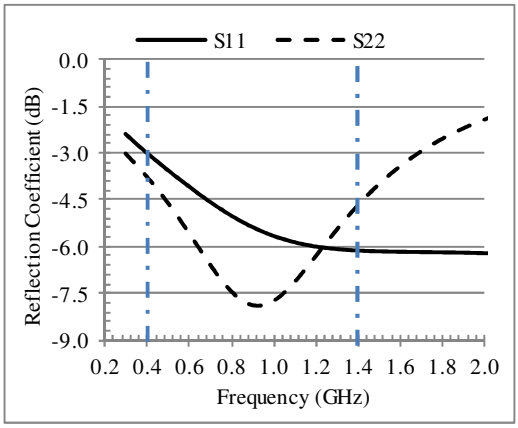
Figure 8-5 Schematic diagram of differential to single-ended MMIC LNA: Input Stage: DISO and Output Stage: SISO Resistive Biasing (Improve S11)



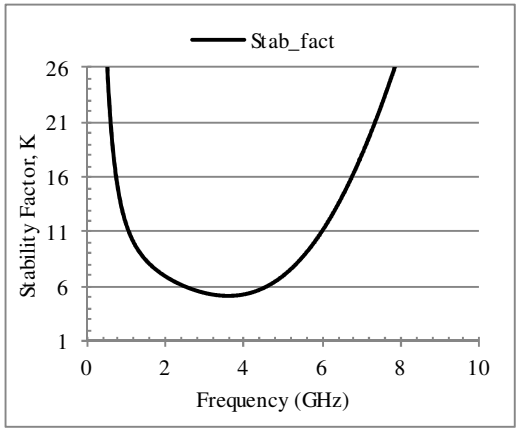
(a) Graph of minimum noise figure, *NFmin* and noise figure, *NF* against frequency



(b) Graph of forward (S21) and reverse (S12) gain against frequency



(c) Graph of input (S11) and output (S22) reflection coefficient



(d) Graph of Rollet stability factor, K

Figure 8-6 Graphs of simulated S-parameters for differential to single-ended MMIC LNA: Input Stage: DISO and Output Stage: SISO Resistive Biasing (Improve S11).

As depicted in Figure 8-6, even though S11 was improved, the *NF* was also increased. The extra inductance added to the source input path of the LNA impacted on gain, *NF*, stability and S11. Improving the S11 still further will further degrade gain and *NF*, yet it will increase the stability. In this design the S11 is -3 to -6.2 dB at 0.4 – 1.4 GHz, while the *NF* increased to 0.95 dB and the gain is maintained at around 24 dB over the frequency band. The power consumption was still 180 mW.

8.3.3 Input Stage: DIDO and Output Stage: DISO (3 V Supply) (Design 3)

In this third MMIC LNA design, the first stage was fully differential (DIDO) and the second stage was differential to single-ended (DISO), as shown in Figure 8-7 (a) and Figure 8-7 (b) respectively. Transistors T1 and T2 (4 x 200 µm pHEMT) were used as the differential RF input. As previously explained, these transistors must be biased at their optimum noise performance since they are located in the first stage. Therefore, these transistors need to be biased at 10% I_{dss} (20 mA), V_{DS} around 0.5 to 1.5 V and V_{GS} = -0.7 V. From simulation, the actual biasing for T_1 and T_2 are 10% I_{dss} = 20.5 mA, V_{DS} around 0.5 V and V_{GS} = -0.66 V, which are the correct biases for minimum noise. A 16 Ω resistor is used as the current source to drain, with approximately 40 mA of current. Therefore, each leg of the differential pair shares half of the current flowing through the resistor.

The differential to single-ended stage utilises transistors T_3 to T_6. Transistor T_3 and T_4 act as active loads, with a transistor size of 2 x 50 µm. Larger gate width devices (4 x 200 µm) are used for transistors T_5 and T_6. As previously stated, a large transistor size will provide lower noise resistance, R_n, yielding improved input matching for the LNA design. It is challenging to control the bias conditions for the second stage, since the sensitivity of the output voltage from the differential stage depends on the gate arm from both transistors, T_5 and T_6. However, simulations showed that the biasing conditions for both T_5 and T_6 were still optimised for noise performance, and validate the design. The simulated bias condition for these transistors is I_{DS} = 16 mA, V_{DS} = 0.86 V and V_{GS} = -0.7 V.

The supply voltage for first stage was 2 V, while that of the second stage was 3 V. Since the supply voltage for this design is not the same, a voltage divider technique was used. With this technique, only one DC voltage would be required for the supply. This would reduce complexity during measurement. However, this method would increase the power dissipation from the design, due to the presence of the resistors in voltage divider circuit. The power consumption for this design is 825 mW. Thus, the next design is proposed to improve the high-power dissipation (section 8.3.4).

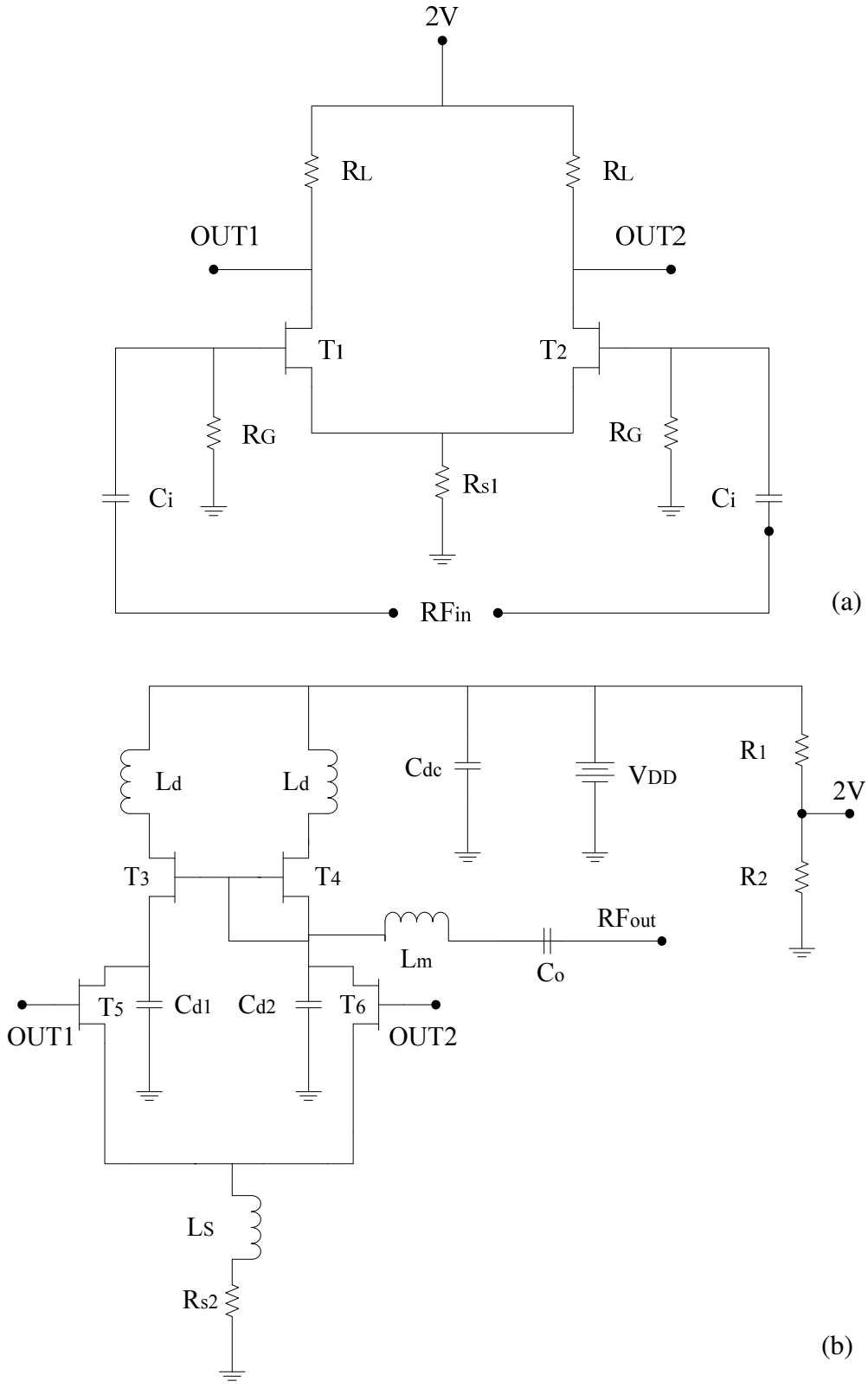
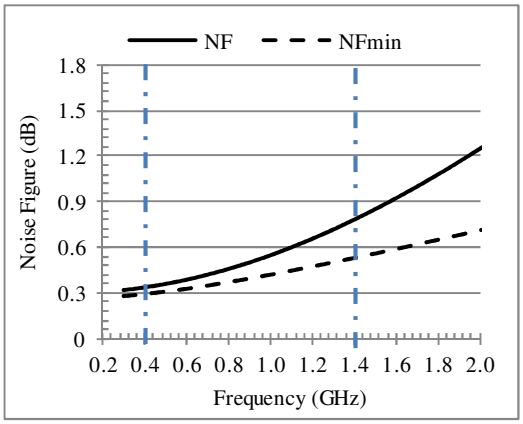
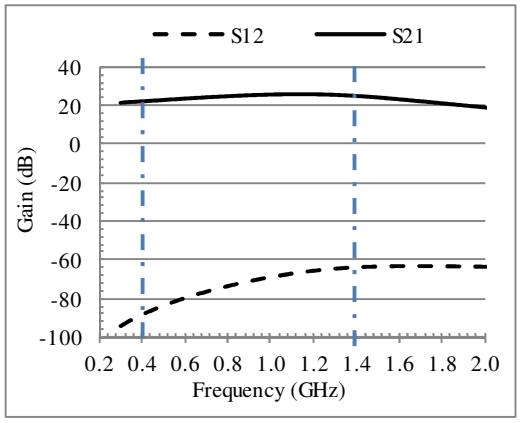


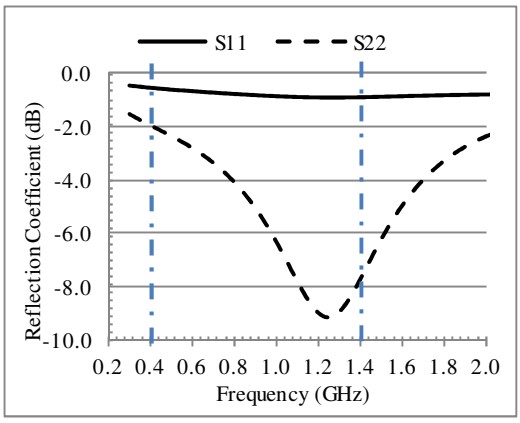
Figure 8-7 Schematic diagram of differential to single-ended MMIC LNA: (a) Input Stage: DIDO and (b) Output Stage: DISO (3 V Supply).



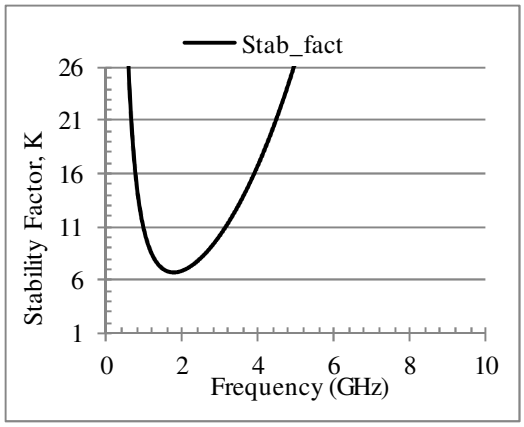
(a) Graph of minimum noise figure, *NFmin* and noise figure, *NF* against frequency



(b) Graph of forward (S21) and reverse (S12) gain against frequency



(c) Graph of input (S11) and output (S22) reflection coefficient



(d) Graph of Rollet stability factor, K

Figure 8-8 Graphs of simulated S-parameters for differential to single-ended MMIC LNA: Input Stage: DIDO and Output Stage: DISO (3 V Supply).

Figure 8-8 showed the S-parameters for the LNA design. The design was unconditionally stable. The *NF* was less than 0.78 dB from 0.4 to 1.4 GHz and the gain (S21) was around 22.0 to 24.7 dB for the same frequency band. The design yielded a poor S11 of between -0.5 dB to -0.9 dB over the frequency band of interest. As discussed in section 8.3.2 , this S11 can be improved by placing a small inductance at the source tail of the input transistors.

8.3.4 Input Stage: DIDO (2 V Supply) and Output Stage: DISO (3 V Supply) (Design 4)

In this section, the MMIC LNA design was similar to section 8.3.3 . There were only two differences in this design. Firstly, there was no voltage divider circuit, and, secondly, small values of series inductance were placed at both source tails in the first stage to improve the input return loss (S11). This design was performed with the assumption that there was no issue in supplying different values of voltage to each stage. In other words, there would be two separate power supplies, i.e. 2 V and 3 V, which must be connected directly to the first stage and second stage respectively. Power dissipation for this design is only 176 mW, compared to previous design which was 825 mW. Therefore, an estimated 79% power saving can be obtained using this technique.

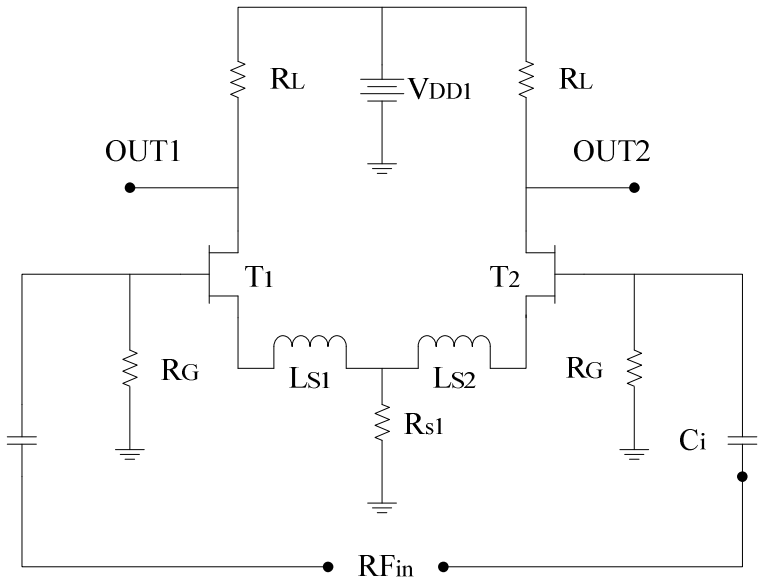


Figure 8-9 Differential to single-ended MMIC LNA: Input stage: DIDO (2 V Supply)

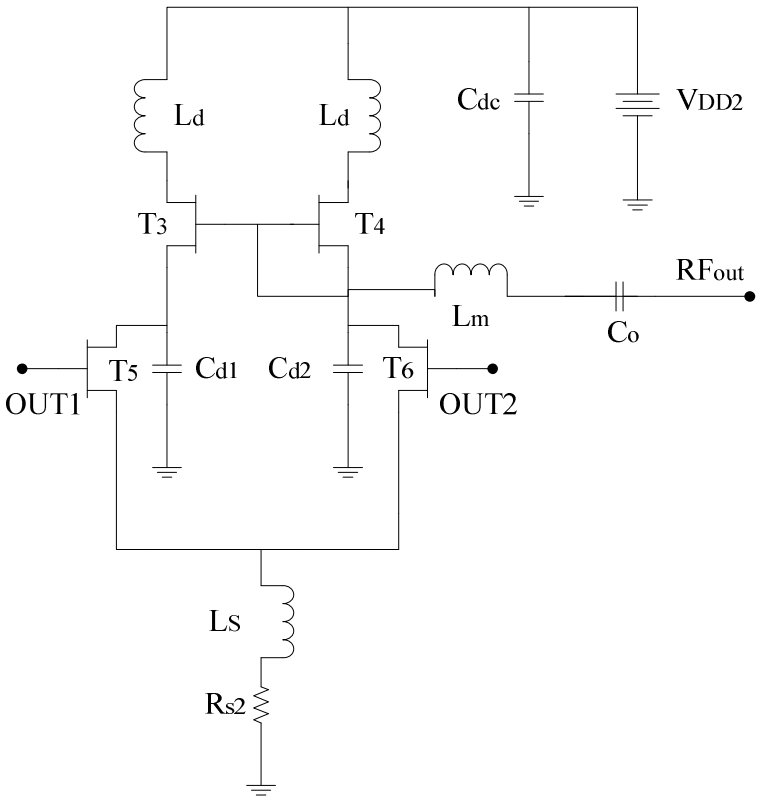
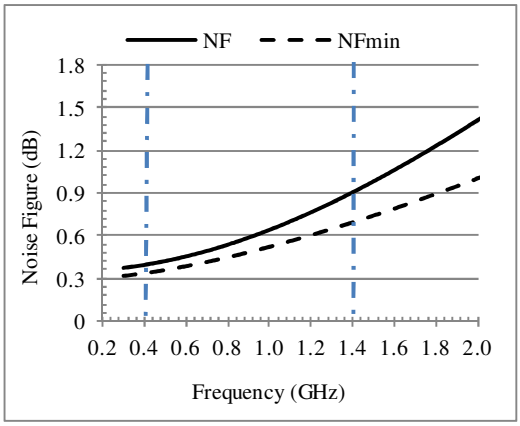
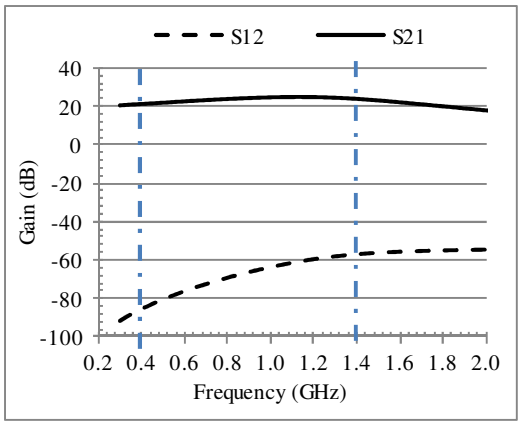


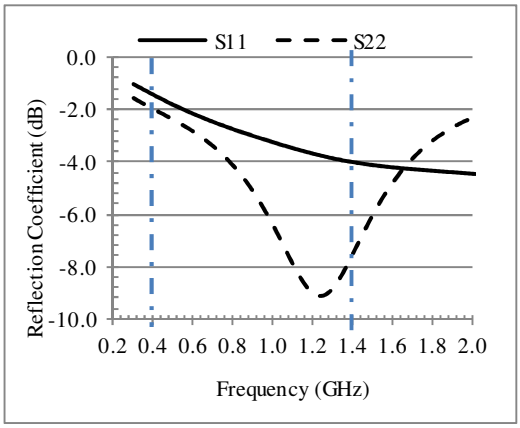
Figure 8-10 Differential to single-ended MMIC LNA: Output stage (3 V Supply)



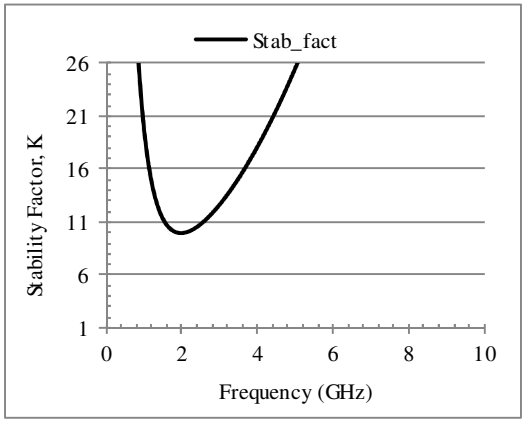
(a) Graph of minimum noise figure, *NFmin* and noise figure, *NF* against frequency



(b) Graph of forward (S21) and reverse (S12) gain against frequency



(c) Graph of input (S11) and output (S22) reflection coefficient



(d) Graph of Rollet stability factor, K

Figure 8-11 Graphs of simulated S-parameters for differential to single-ended MMIC LNA: Input Stage: DIDO (2 V Supply) and Output Stage: DISO (3 V Supply).

The S-parameters for the design are illustrated in Figure 8-11. This design improved S11 in comparison to design 3, with an S11 of -1.4 to -4.0 dB over the frequency range of 0.4 to 1.4 GHz. However, as expected, the *NF* was slightly increased. This MMIC LNA design showed a *NF* of 0.39 to 0.90 dB over the frequency band of interest. The gain on the other hand is comparable with Design 3 in section 8.3.3 .

8.3.5 Design Summary

This report presented four designs of double stage differential to single-ended MMIC LNA for the SKA radio telescope, using in-house InP-based pHEMTs. All design characteristics have been successfully investigated and explained and are unconditionally stable up to 10 GHz. Table 8-1 summarises the designs S-parameters and power dissipation for comparison.

Table 8-1 Table of comparison of gain (S21), noise figure (NF), input reflection coefficient (S11) and power dissipation (P_{diss}) for differential to single-ended MMIC LNA designs

Design	S21 (dB)		NF (dB)		S11 (dB)		P_{diss} (mW)
	0.4 GHz	1.4 GHz	0.4 GHz	1.4 GHz	0.4 GHz	1.4 GHz	
1	30.0	25.1	0.47	0.83	-1.8	-1.3	180
2	29.0	24.3	0.55	0.95	-3.0	-6.2	180
3	22.0	24.7	0.34	0.78	-0.5	-0.9	825
4	20.0	23.5	0.39	0.90	-1.4	-4.0	176

Comparing Design 1 (in section 8.3.1) and Design 2 (in section and 8.3.2), the *NF* in Design 1 is better. However, the S11 for Design 2 is improved. The power dissipation for these two designs is the same, and both designs showed excellent gain flatness.

Design 3 (in section 8.3.3) is not suitable for fabrication since the power dissipation is approximately three times the design specification.

The design with the lowest power dissipation is presented in Design 4 (in section 8.3.4). This design also provided a lower *NF* at the lowest frequency (400 MHz). However, the *NF* was marginally increased (~0.07 dB) at a higher frequency of 1.4 GHz when compared to Design 1. The S11 figure, on the other hand, is an improvement over Design 1. Forward gain (S21) for this design met the specifications target (~25 dB), while the S21 for Design 1 is moderately high (~28 dB).

8.4 COMPARISON WITH OTHER DIFFERENTIAL LNAS

Table 8-2 summarises the available differential LNAs designed for the same frequency range.

Fully differential LNAs presented in [115] and [122] were designed using CMOS technology. However, the LNA designed by Sobhy*, et al.* [122] showed advantages

over the LNA designed by Wang, *et al.* [115]. The excellent performance achieved in [122] was due to the small gate size utilised in the design. However, power consumption reported for both LNAs was measured for the core LNA, rather than the complete circuit. To the author's knowledge, a noise figure of < 2.4 dB is the lowest noise figure that has been reported to date for a fully differential LNA design using nanometer scale CMOS technology.

The differential input to single-ended ouput MMIC LNA designed in this project was an improvement on the design presented by S. Arshad, *et al* [120] in term of power dissipation. The power dissipation for the LNA proposed in this project was reduced by 50%, when compared to the original power consumption reported in [120]. A *NF* of < 0.9 dB was achieved over the frequency range of 0.3-1.4 GHz. This design contains six transistors, and therefore, the gain was moderate (21 dB) to minimise the effect of oscillations. The differential LNA designs proposed in this work is based on InP technology with 1 µm gate length.

Table 8-2 Table comparing the in-house fabricated differential to single-ended LNA with the differential LNA obtained by other researcher

Reference	**[120]**	**[115]**	**[122]**	**This work**
Year	2009	2010	2011	2012
Bandwidth (GHz)	0.3-1.0	0.2-3.8	0.1-1.77	0.3-1.4
Technology	[1]InP 1 µm	[2]CMOS 0.13 µm	[2]CMOS 90 nm	[1]InP 1 µm
Noise Figure (dB) (*Sim./Meas.*)	< 0.6 *Sim.*	< 3.4 *Meas.*	< 2.4 *Meas.*	<0.9 *Sim.*
Gain (dB)	30	13	23	21
Power (mW)	300	[3] 5.8	[3] 2.8	176
Stability	Unconditionally stable	Unconditionally stable	Unconditionally stable	Unconditionally stable
Impedance (Ω)	50	50	50	50

1 Differential input to single-ended output

2 Fully differential

3 Power consumption for core LNA

8.5 CONCLUSION

In conclusion, this chapter discussed four different approaches to designing differential LNAs using InP based pHEMTs in a Double Stage Differential to Single-ended MMIC. Design 1 in section 8.3.4 and Design 4 in section 8.3.1 have shown very low noise characteristics, with low power dissipation, compatible with the stringent requirements of the SKA. Designs using larger transistors in the first stage showed an improvement in noise figure and gain flatness, with unconditional stability over 10 GHz. The power consumption for both designs was low, at ~180 mW.

CHAPTER 9

CONCLUSION AND FUTURE WORK

9.1 THESIS SUMMARY AND CONCLUSIONS

The main goal of this research was to design and test a low noise amplifier (LNA) for the SKA radio telescope system operating over a frequency range of 0.4-1.4 GHz.

The InGaAs/InAlAs/InP pHEMT based on 1 μm gate length technology was chosen for use in this research due to its superior physical properties, resulting in an increased f_T and transconductance (g_m), which are fundamental parameters for low noise characteristics.

The first step towards LNA design involved precise device and passive component modelling. Therefore, empirical device models were developed to accurately predict the behaviour of both active and passive devices over a wide range of frequency under low noise condition. The precision of these models was ensured by validating them with the DC and RF results of respective devices, and further strengthened through the incorporation of the LNA S-parameters measurements into the simulation.

The LNAs designed in this study had three significant common characteristics: Firstly, the active device was biased at low drain currents where the noise contribution is minimised, hence the device could provide not only low noise, but also low power consumption. A low power LNA design is a crucial requirement for the SKA. Secondly, the input network of the LNA was designed for optimum source impedance matching to minimise the input reflection coefficient. Thirdly, the output network of the LNA was designed to provide a minimal output reflection coefficient and therefore produce a flatter gain profile.

The single stage LNA presented in Chapter 7 achieved a number of the design targets required for the SKA. These included high stability and a low noise figure (<1.5 dB) over the frequency range, but failed to produce the specified gain (30 dB). The low gain was resolved via the incorporation of a second stage, without compromising other factors. Alternative designs were also studied (with and without inductors) in an attempt to observe the effect of the inductors on the circuit noise performance and S-parameter values. The design without inductors can be seen to marginally improve the input reflection coefficient and stability performance, but did not dramatically improve the noise performance of the circuit. However, designs without inductors have the advantage of simpler circuit fabrication.

The noise performances were comparable for both double stage designs. The measured noise figure was unfortunately 50% higher at the lower frequency end when compared to the simulated data. This result is expected to be due to the poor Q factor of the integrated inductors and capacitors, hence the passive models and designs require further investigation. However, there are other critical parameters than just a tight specification of passive elements, which must be considered when overall noise measurement is carried out. One of the examples is imperfect system source match, results from the interaction of noise source with the input match of the LNA. This imperfect match of the noise source will cause the noise figure of the noise receiver and LNA to change versus frequency. Other parameters that also importance is mismatch errors due to the imperfect calibration of the noise source or the noise source cascaded with adapters, cables, switches, or probes.

Differential input to single ended output LNA configurations were also proposed in Chapter 8, which will be fabricated in the near future. In comparison to the circuits presented in chapter 7, the noise figure of the differential LNA showed a dramatic improvement. Assuming that the noise figure for these circuits was also 30% - 50% higher after fabrication, the lowest noise figure would therefore be 0.52 dB (300 MHz) and 1 dB (1.4 GHz), which demonstrates the promise of this technology and its competiveness for low power applications. All LNAs in this project are unconditionally stable over 10 GHz.

This thesis has contributed to the feasibility of the MMIC LNA designs for use in the SKA front end requirement, and also for various other commercial applications such as mobile phones and satellite navigation systems.

9.2 SUGGESTIONS FOR FURTHER WORK

The work presented in this thesis offers opportunities for further study in several areas. Shown below are some suggestions of research directions that need to be pursued to make such a system feasible:

1) The most important extension from this work is the preparation of the layout for the MMIC differential LNA designs, followed by development of the fabrication process. Since the differential LNA has a differential input and single output, conceptual understanding of three port networks is essential for the necessary LNA characterisation techniques. The measurements are based on the 3 x 3 matrix of a three-port network.

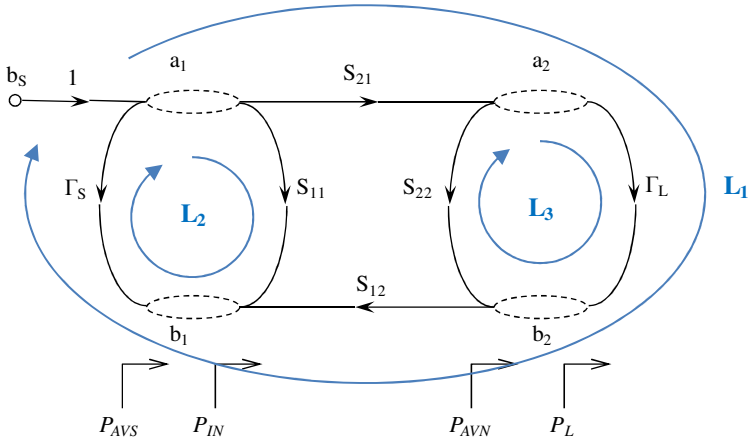
2) Physical modelling of the device to provide improved insight into the device physics and how to further improve the epitaxial structure, especially with respect to noise. This can be done using a physical simulator such as the SILVACO software.

3) Physically integrating the LNA with the SKA antenna prototype to measure the exact noise added to the LNA as well as to compute the transmission losses of the system. To eliminate the transmission losses (or any loss) that may occur before the LNA, the active part of the antenna must be connected directly to the input path of the LNA so that the antenna forms the input network. However, the viability of this system is beyond the scope of this study and therefore, requires further investigation.

4) Investigate the loss in noise performance at low frequencies. The passives' Q factor should be improved by better device design and modelling. This may require further optimisation of the fabrication techniques.

5) Further investigation of the submicron LNA circuit design using I-line optical lithography and 1 μm gate reflow technique. As highlighted in Chapter 5, the submicron devices have higher f_T and consequently lower noise figures. This submicron fabrication process maintains the low-cost requirements of the application, since e-beam technology or expensive phase-shifting masks are eliminated.

APPENDIX A: DERIVATION OF VOLTAGE GAIN FOR TWO PORT NETWORK



From the equation (3.8), the voltage gain $A_v = \frac{V_{OUT}}{V_{IN}} = \frac{a_2+b_2}{a_1+b_1}$

where a_1 = The incident wave at port 1 ,

a_2 = The incident wave at port 2,

b_1 = The reflected wave at port 1, and

b_2 = The reflected wave at port 2

Using Manson's Rule [50, 123], a_1, a_2, b_1 and b_2 can be derived as:

$$P_1\left[1-\sum L(1)^{(1)}+\sum L(2)^{(1)}-\ ...\right]+P_2\left[1-\sum L(1)^{(2)}+\ ...\right] \quad \text{Equation A - 1}$$

Where P_1 and P_2 are the first and second forward paths connecting to the incident/reflected wave. The terms:

$\sum L(1)^{(1)}$, is the sum of all first order loops that do not touch the first path between the variables.

$\sum L(2)^{(1)}$, is the sum of all second order loops that do not touch that path, and so on down the line.

$\sum L(1)^{(2)}$, is the sum of all first order loops that do not touch the second path.

Applying this rule, hence:

$$a_1 = P_1(1 - L_3) = 1(1 - S_{22}\Gamma_L)$$ Equation A - 2

$$b_1 = P_1(1 - L_3) + P_2 \ = S_{11}(1 - S_{22}\Gamma_L) + S_{21}\Gamma_L S_{12}$$ Equation A - 3

$$a_2 = P_1(1 - L_2) = S_{21}(1 - S_{11}\Gamma_S)$$ Equation A - 4

$$b_2 = P_1\,(1 - L_2) = S_{21}\,\Gamma_L\,(1 - S_{11}\Gamma_S)$$ Equation A - 5

where L_1, L_2 and L_3 are the available loops in the two-port network, whereas Γ_L and Γ_S is the load and the source impedance respectively.

By inserting these values to the equation (3.8), therefore the final derivation of voltage gain is as written in equation (3.9):

$$A_V = \frac{S_{21}(1 + \Gamma_L)}{(1 - S_{22}\Gamma_L) + S_{11}(1 - S_{22}\Gamma_L) + S_{21}\Gamma_L S_{12}}$$ Equation A - 6

APPENDIX B: TRANSFORMATION OF Z TO Y MATRIX

For two-port network, the impedance matrix (Z matrix) can be transformed to the admittance matrix (Y matrix) using the following equations and vice versa:

$$Z = \begin{bmatrix} \frac{Y_{22}}{\Delta Y} & \frac{-Y_{12}}{\Delta Y} \\ \frac{-Y_{21}}{\Delta Y} & \frac{Y_{11}}{\Delta Y} \end{bmatrix} \quad \text{Equation B - 1}$$

Where $$\Delta Y = Y_{11}Y_{22} - Y_{12}Y_{21} \quad \text{Equation B - 2}$$

And

$$Y = \begin{bmatrix} \frac{Z_{22}}{\Delta Z} & \frac{-Z_{12}}{\Delta Z} \\ \frac{-Z_{21}}{\Delta Z} & \frac{Z_{11}}{\Delta Z} \end{bmatrix} \quad \text{Equation B - 3}$$

Where $$\Delta Z = Z_{11}Z_{22} - Z_{12}Z_{21} \quad \text{Equation B - 4}$$

APPENDIX C: FABRICATION STEPS

In this project, a series of InP-based transistors are fabricated on the epilayers using a conventional optical lithography process. These transistors were used in the LNA designs described in Chapter 7 and Chapter 8. Below are brief explanations of the fabrication steps for a four gate finger device:

STEP 1: Definition of MESA

The fabrication process starts with etching the unnecessary active region using a non-selective wet chemical etchant. Here, the desired structure will take the shape of a MESA, with a gradual slope edge profile, which is beneficial for good metal coverage for the subsequent Ohmic and gate layer steps. The resulting MESA structure and the corresponding mask are illustrated in Figure C - 1(a).

STEP 2: Formation of Ohmic Contact

The next step is the formation of Ohmic contacts for current conduction between the Source and Drain terminals as shown in Figure C - 1(b). The metal is allowed to diffuse into the semiconductor to form a low resistance path to the 2DEG layer. Note that there is a hanging middle source terminal that will need metal interconnection in the later fabrication process.

STEP 3: Formation of Gate Terminal

After Ohmics, the fabrication process continues with the formation of the gate terminal. Here, two important steps are involved: gate recess and gate metal deposition. The gate recess is a process where the top cap layer is etched, exposing the Schottky barrier layer onto which a gate metal will be evaporated. This process is shown in Figure C - 1(c).

STEP 4: Formation of Probing Pads

The two gate figure device fabrication process ends with the formation of bond pad contacts. These metal pads will allow accurate microwave probing during on-wafer RF measurements (Figure C - 1(d)). For more than two gate finger devices, additional dielectric bridge and metal bridge formations are needed for the device to operate correctly. The bridge will connect the isolated source terminals, which will complete their ground termination.

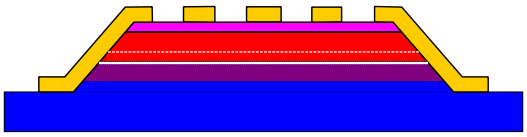
Step 5: Formation of Dielectric Support

As been noted in the fabrication steps (Step 2), the middle source terminal needs to be connected to the other source terminals for a common ground. Since the source interconnection will be formed by a metal bridge layer between the side terminals, with the middle terminal crossing over the gate fingers, a dielectric layer will be needed to passivate the gate metal, to prevent it from being short circuited by the metal bridge. Here, SF11 is used as the dielectric passivation layer, as well as bridge support for the metal interconnection. The formation of the dielectric bridge support is shown in Figure C - 1(e)

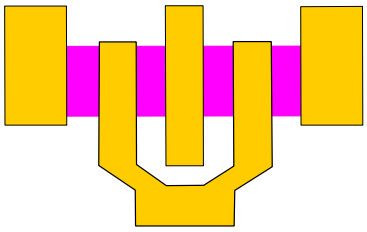
The fabrication process ends with the thermal evaporation of Ti/Au of 50/400 nm thickness as the sources' metal interconnection, as shown in Figure C - 1(f). The metal layer is made smaller than the dielectric support, to prevent the metal from short circuiting. Finally, the device may also be passivated by a nitride or thick resist for environmental shielding

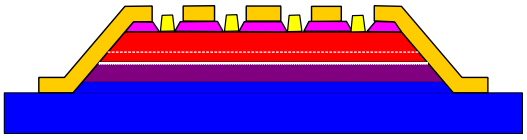
A graphical representation of these fabrication steps is depicted in Figure C - 1.

(a)

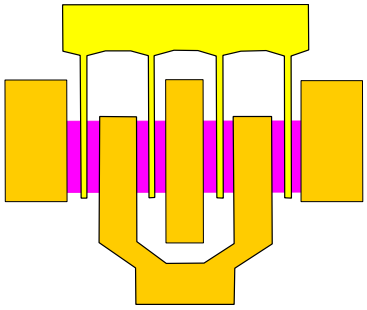


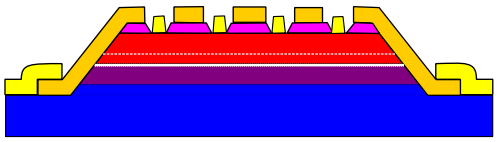
(b)



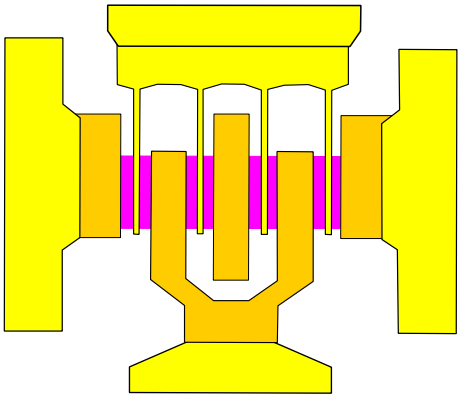


(c)





(d)



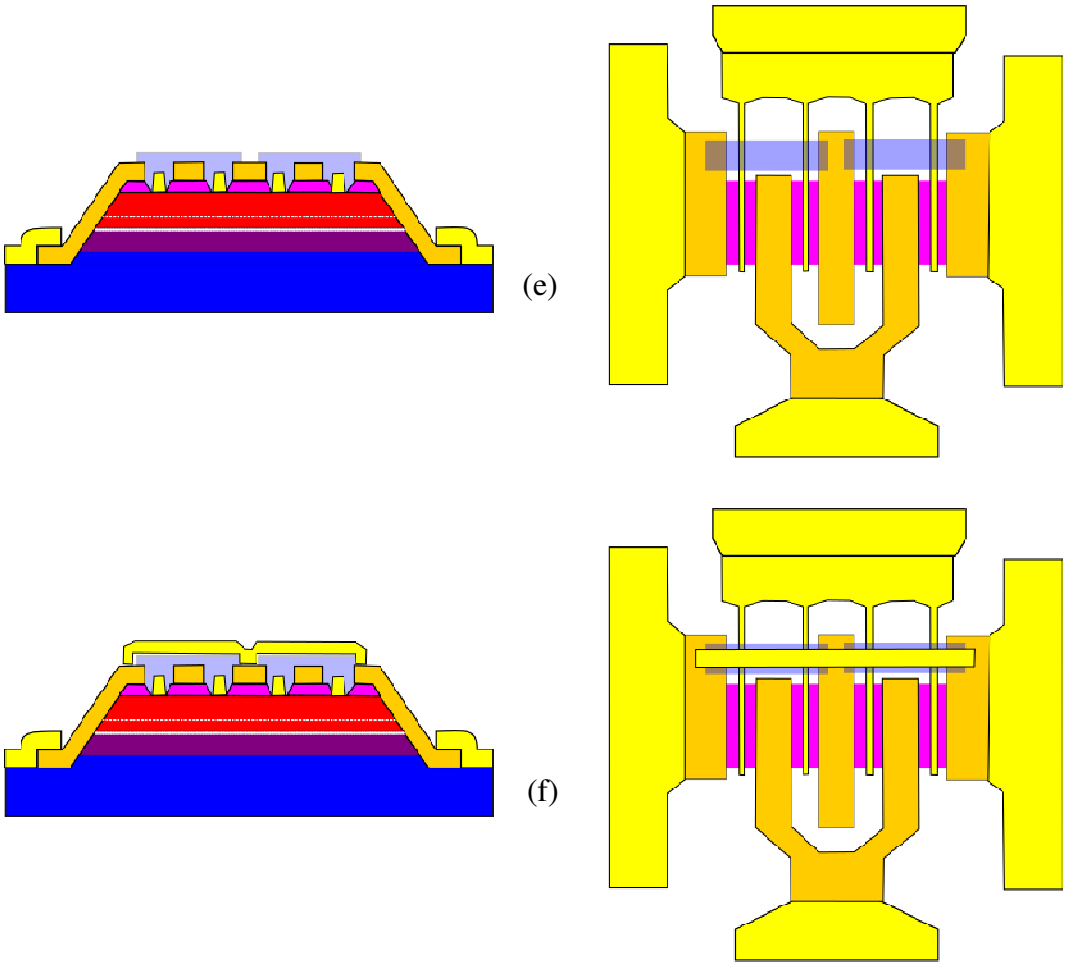


Figure C - 1 Graphical representation of fabrication steps for conventional pHEMT device showing the cross-sectional view on the left and the corresponding mask on the right. The steps are (a) Formation of MESA, (b) Source-Drain Ohmic, (c) Gate and (d) Probing pads (e) Dielectric bridge support and (f) Formation of metal bridge. On top is the conventional pHEMT epilayer.

APPENDIX D: LNA FABRICATION STEPS

The mask layouts presented in this work were prepared using ADS. This section briefly discusses the steps involved in the preparation of the CPW MMIC layouts for the fabrication of the in-house InP-based LNA. Figure D - 1 to Figure D - 3 illustrates the ten process steps of mask layout for SSLNA, DSLNA (with inductor) and DSLNA (without inductor) respectively.

The fabrication starts with the formation of MESA (Mask 1- MESA) for the active area definition. Then, a 50/400 nm layer of Ti/Au is thermally evaporated, and the resist opening filled at the Ohmic location (Mask 2- Ohmic) followed by a lift-off process. Next, the gate fingers are defined (Mask 3- Gate) by lithography, and gate recessing takes place, before the 50/400 nm of Ti/Au metallisation is thermally evaporated and lifted-off. After that, the first metal interconnection, as well as the bottom plate for the capacitors and inductors, are thermally evaporated and lifted-off forming a 50/400 nm thickness of Ti/Au (Mask 4 – Metal 1). Subsequently, 90 nm of Si3N4 is deposited under a low temperature plasma deposition process, and a nitride opening takes place at the designated contact area using CF4 and O2 plasma etches (Mask 5 – Nitride etch). Afterwards, a thin NiCr film is sputtered (Mask 6 – NiCr) before the thermal deposition and lift-off of the second metal interconnection (Mask 7 – Metal 2). Metal 2 also incorporates a top metal plate for capacitors and metal structures for spiral inductors. Consequently, a dielectric bridge made from SF11 (Mask 8 – dielectric bridge) is formed where 50/400 nm of Ti/Au metal bridge (Mask 9 –Metal bridge) is located. The fabrication is completed application of the hardened resist passivation layer for proper environmental shielding of the MMIC circuits (Mask 10 – passivation).

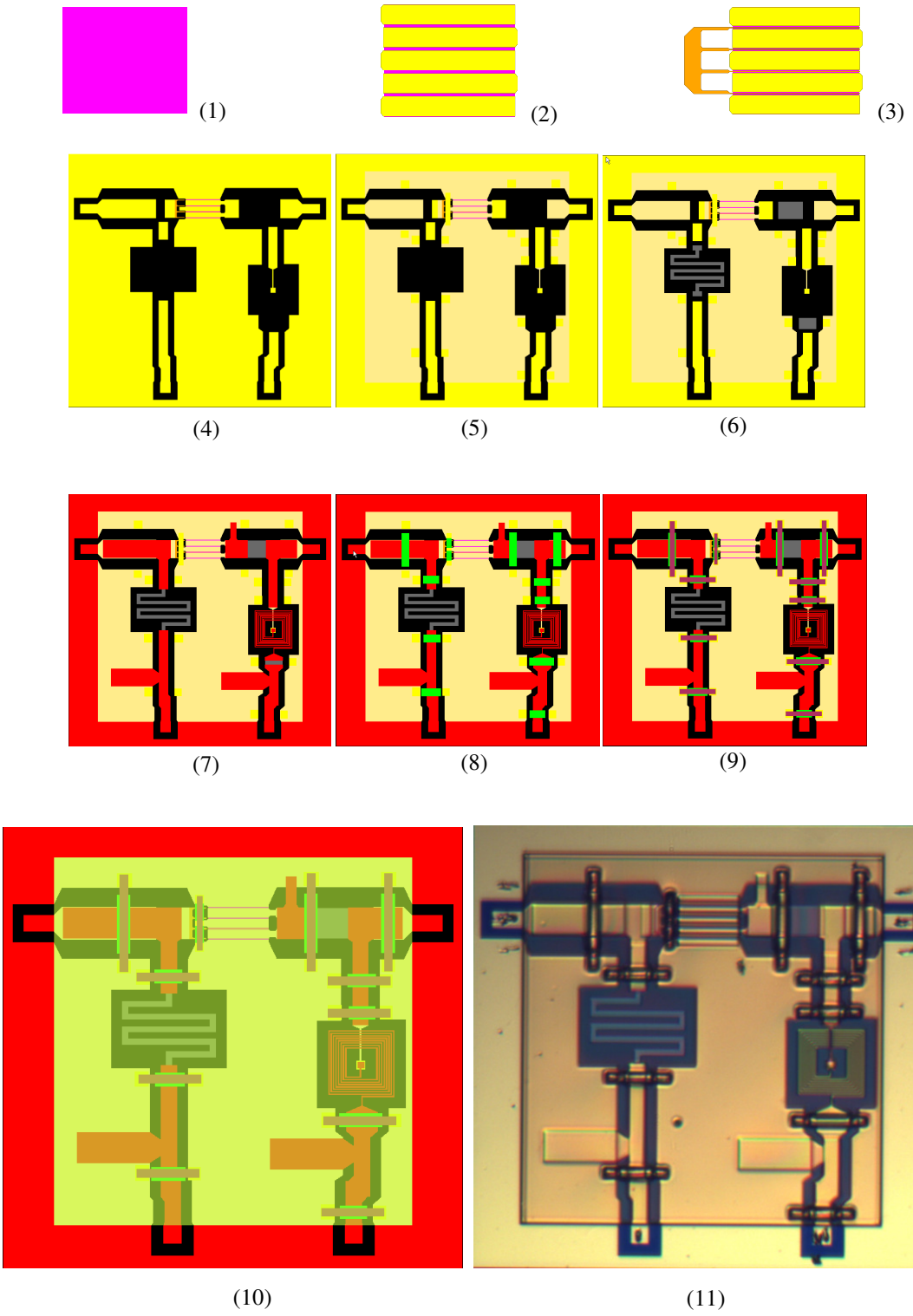


Figure D - 1 Mask layout for SSLNA: (1) MESA, (2) Ohmic, (3) Gate, (4) Metal 1, (5) $S_{13}N_4$ Deposition and etch, (6) NiCr, (7) Metal 2, (8) dielectric Bridge, (9) Metal Bridge, (10) Passivation and (11) Fabricated MMIC SSLNA

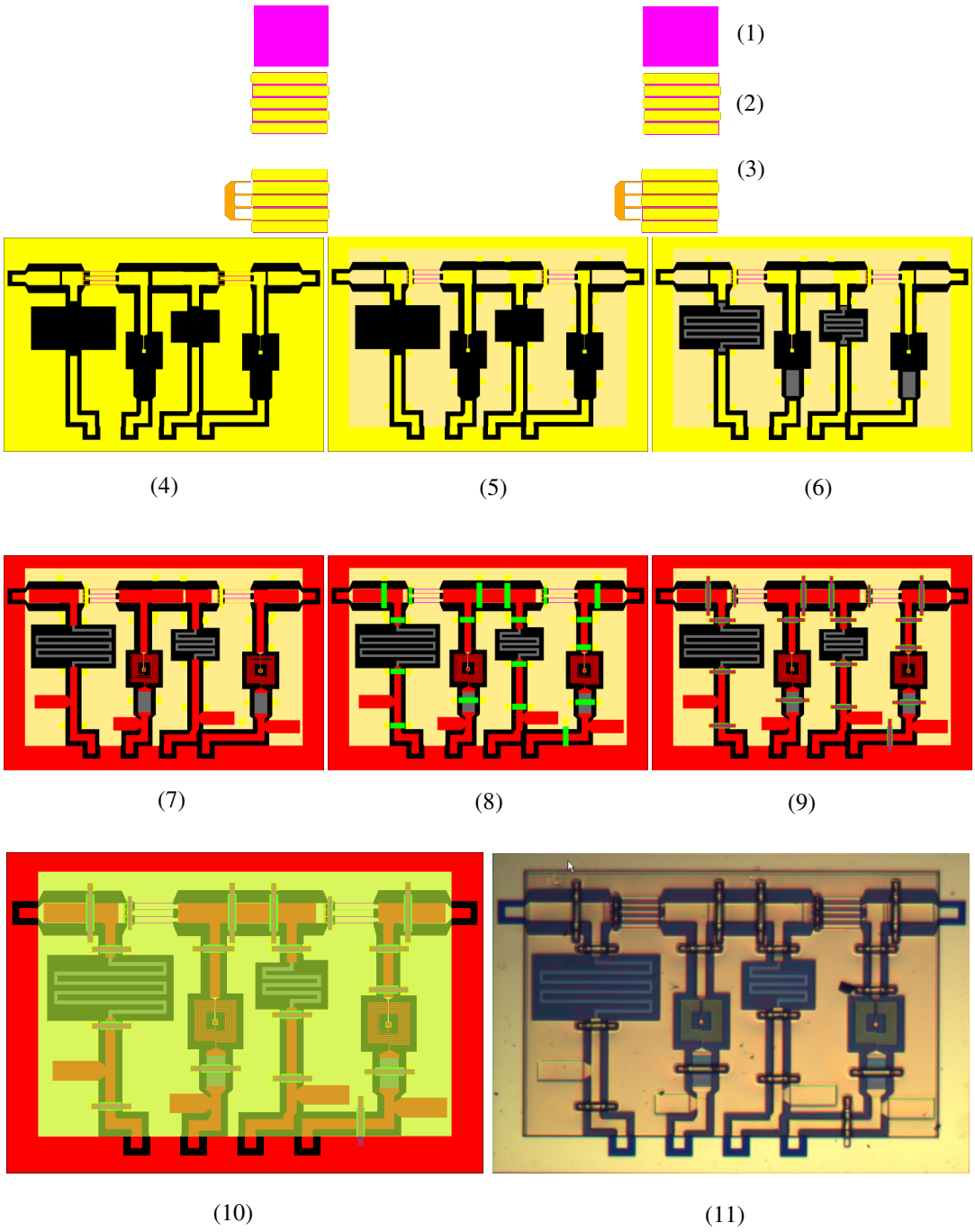


Figure D - 2 Mask layout for HG-DSLNA (1) MESA, (2) Ohmic, (3) Gate, (4) Metal 1, (5) Si_3N_4 Deposition and etch, (6) NiCr, (7) Metal 2, (8) Dielectric Bridge, (9) Metal Bridge, (10) Passivation, and (11) Fabricated MMIC DSLNA (with inductor)

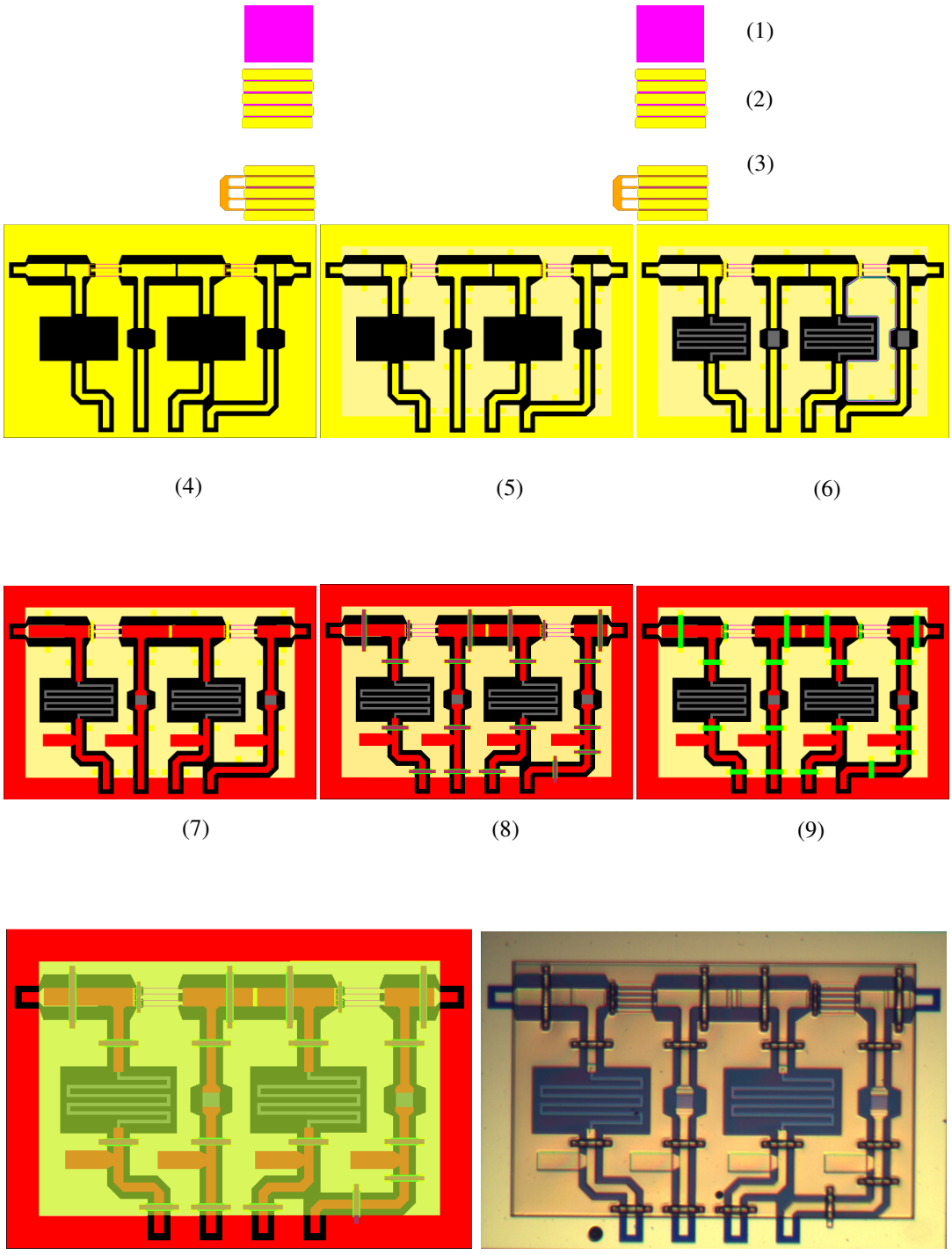


Figure D - 3 Mask layout for MG-DSLNA (1) MESA, (2) Ohmic, (3) Gate, (4) Metal 1, (5) Si_3N_4 Deposition and etch, (6) NiCr, (7) Metal 2, (8) Dielectric Bridge, (9) Metal Bridge, (10) Passivation, and (11) Fabricated MMIC DSLNA (without inductor)

REFERENCES

[1] *ASKAP Science Update: CSIRO Astronomy and Space Science*. Available: http://www.atnf.csiro.au/projects/mira/ASKAP_Science_Update_4.pdf

[2] M. White, *Galileo Galilei: Inventor, Astronomer and Rebel*: Blackbirch Press, 1999.

[3] D. Berlinski, *Newton's Gift: How Sir Isaac Newton Unlocked the System of the World*, Reprint ed.: Free Press, March 2002.

[4] G. Reber, "Cosmic Static," *Astrophysical Journal,* vol. 91, pp. 621-624, 1940.

[5] *SKA brochure: The Internatinal Radio Telescope for the 21st Century*. Available: http://www.jodrellbank.manchester.ac.uk/research/ska//brochure/SKABrochure.pdf

[6] A. Materka and T. Kacprzak, "Computer Calculation of Large-Signal GaAs FET Amplifier Characteristics," *Microwave Theory and Techniques, IEEE Transactions on,* vol. 33, pp. 129-135, 1985.

[7] A. P. Lobano, "The SKA and “High-Resolution” Science," *Instrumentation and Methods for Astrophysics (astro-ph.IM): Cornell University,* p. 9, 1 July 2011.

[8] A. Faulkner*, et al.* (March 2010, *Aperture Arrays for the SKA: the SKADS White Paper* Available: http://www.skads-eu.org/PDF/SKADS_White_Paper_100318_dist.pdf

[9] Y. H. Chang and J. J. Chang, "Analysis of an EEHEMT Model for InP pHEMTs," in *Electron Devices and Solid-State Circuits, 2007. EDSSC 2007. IEEE Conference on*, 2007, pp. 237-240.

[10] H. A. Haus and R. B. Adler, "Optimum Noise Performance of Linear Amplifiers," *Proceedings of the Institute of Radio Engineers,* vol. 46, pp. 1517-1533, 1958.

[11] S. Bhaumik and D. George, "Review of Square Kilometre Array LNATechnologies and Topologies," in *Wide Field Science and Technology for the SKA: SKADS Conference 2009*, Chˆateau de Limelette, Belgium, Nov 2009.

[12] L. Belostotski*, et al.*, "Wide-band CMOS low noise amplifier for applications in radio astronomy," in *Circuits and Systems, 2006. ISCAS 2006. Proceedings. 2006 IEEE International Symposium on*, 2006, p. 4

[13] L. Aluigi*, et al.*, "Design of a Ka-Band LNA for SoC space-based millimeter-wave radiometers," in *Microwave Workshop Series on Millimeter Wave*

Integration Technologies (IMWS), 2011 IEEE MTT-S International, 2011, pp. 156-159.

[14] Y. Wang*, et al.*, "A Broadband Low Noise Amplifer Design," presented at the Electromagnetics Research Symposium, 2008.

[15] W. Shockley, "Circuit Element Utilizing Semiconductive Material," U. S. Patent 2569347, 1951.

[16] R. A. Khabibullin*, et al.*, "The built-in electric field in P-HEMT heterostructures with near-surface quantum wells AlxGa1-xAs/InyGa1-yAs/GaAs," in *Iv Nanotechnology International Forum*. vol. 345, ed, 2012.

[17] Y. Jin*, et al.*, "Semiconductor Heterostructure and Transistor of HEMT Type, in particular for low-frequency low-noise cyrogenic applications," France Patent, April 2012.

[18] A. Y. Cho, "Morphology of Epitaxial Growth of GaAs by a Molecular Beam Method: The Observation of Surface Structures," *Journal of Applied Physics,* vol. 41, pp. 2780-2786, 1970.

[19] J. C. Bean, "Materials and Technologies," in *High-Speed Semiconductor Devices*, ed New York John Wiley & Sons, 1990.

[20] L. Vegard., "Die Konstitution der Mischkristalle und die Raumfüllung der Atome," *Zeitschrift für Physik,* vol. Vol 5, pp. 17-26, 1921.

[21] L. De Caro*, et al.*, "Validity of Vegard's rule for the lattice parameter and the stiffness elastic constant ratios of the AlGaAs ternary compound," *Solid State Communications,* vol. 108, pp. 599-603, 1998// 1998.

[22] J. C. Mikkelsen, Jr. and J. B. Boyce, "Atomic-scale structure of random solid solutions: extended X-ray-absorption fine-structure study of Ga/sub 1-x/In/sub x/As," *Physical Review Letters,* vol. 49, pp. 1412-15, 1982/11/08 1982.

[23] G. Bauer and F. Schäffler, "Self-assembled Si and SiGe nanostructures: New growth concepts and structural analysis," *physica status solidi (a),* vol. 203, pp. 3496-3505, 2006.

[24] T. F. Kuech*, et al.*, "Defect reduction in large lattice mismatch epitaxial growth through block copolymer full wafer patterning," in *Indium Phosphide & Related Materials, 2009. IPRM '09. IEEE International Conference on*, 2009, pp. 63-64.

[25] J. W. Matthews and A. E. Blakeslee, "Defects in epitaxial multilayers: I. Misfit dislocations," *Journal of Crystal Growth,* vol. 27, pp. 118-125, 1974.

[26] J. W. Matthews and A. E. Blakeslee, "Defects in epitaxial multilayers: II. Dislocation pile-ups, threading dislocations, slip lines and cracks," *Journal of Crystal Growth,* vol. 29, pp. 273-280, 1975.

[27] J. W. Matthews and A. E. Blakeslee, "Defects in epitaxial multilayers: III. Preparation of almost perfect multilayers," *Journal of Crystal Growth,* vol. 32, pp. 265-273, 1976.

[28] C. S. Whelan*, et al.*, "Metamorphic transistor technology for RF applications," *Microwave Journal, Euro-Global Edition,* vol. 44, pp. 110-20, 2001/04/ 2001.

[29] S. M. Sze, : John Wiley and Sons, "Semiconductor Devices: Physics and Technology. 2nd ed.," 2002.

[30] R. L. Anderson, "Experiments on Ge-GaAs Heterojunctions," *Solid-State Electronics,* vol. 5, 1962.

[31] S. M. Sze, "Metal-Semictonductor Contacts," in *Physics of Semiconductor Devices*, 2nd ed: A Wiley-Interscience Publication, 1981, pp. 245-311.

[32] M. S. Tyagi, "Schottky Barrier Diode," in *Introduciton to Semiconductor Materials and Devices*, ed: John Wiley and Sons, 1991, pp. 270-288.

[33] J. d. F. Sexton, "Fabrication and Characterisation of High-Speed Indium Phosphide-Based Heterojunction Bipolar Transistors," Doctor of Philosophy, Faculty of Engineering and Physical Sciences, The University of Manchester, Manchester, 2005.

[34] D. K. Schroder, "Metal-Semiconductor Contacts," in *Semiconductor Material and Device Charaterization*, ed: John Wiley & Sons, Inc, 1998, pp. 134-138.

[35] E. F. Schubert*, et al.*, "The delta-doped field-effect transistor (delta-FET)," *Electron Devices, IEEE Transactions on,* vol. 33, pp. 625-632, 1986.

[36] R. Dingle*, et al.*, "Electron mobilities in modulation-doped semiconductor heterojunction superlattices," *Applied Physics Letters,* vol. 33, pp. 665-667, 1978.

[37] J. R. Arthur and J. J. Lepore, "GaAs,GaP nad $GaAs_xP_{1-x}$ Epitaxial Films Grown by Molecular Beam Deposition," *Journal of Vacuum Science & Technology,* vol. 6, p. 545, 1969.

[38] T. Mimura*, et al.*, "A New Field-Effect Transistor with Selectively Doped GaAs-n-$Al_xGa_{1-x}As$ Heterojunctions," *Japanese Journal of Applied Physics,* vol. 19, pp. L225-L227, 1980.

[39] L. Esaki and R. Tsu, "Superlattice and Negative Differential Conductivity in Semiconductors," *IBM Journal of Research and Development,* vol. 14, pp. 61-65, 1970.

[40] R. Dingle*, et al.*, "High mobility multilayered heterojunction devices employing modulated doping," U. S. Patent 4163237, 1978.

[41] H. Morkoc, "Current transport in modulation doped (Al,Ga)As/GaAs heterostructures: Applications to high speed FET's," *Electron Device Letters, IEEE,* vol. 2, pp. 260-262, 1981.

[42] T. E. Zipperian and T. J. Drummond, "Strained-quantum-well, modulation-doped, field-effect transistor," *Electronics Letters,* vol. 21, pp. 823-824, 1985.

[43] J. J. Rosenberg*, et al.*, "An InGaAs/GaAs pseudomorphic single quantum well HEMT," *Electron Device Letters, IEEE,* vol. 6, pp. 491-493, 1985.

[44] A. Ketterson*, et al.*, "High transconductance InGaAs/AlGaAs pseudomorphic modulation-doped field-effect transistors," *Electron Device Letters, IEEE,* vol. 6, pp. 628-630, 1985.

[45] N. Moll*, et al.*, "Pulse-doped AlGaAs/InGaAs pseudomorphic MODFETs," *Electron Devices, IEEE Transactions on,* vol. 35, pp. 879-886, 1988.

[46] U. K. Mishra*, et al.*, "DC and RF performance of 0.1 mu m gate length $Al_{0.48}In_{0.52}As$-$Ga_{0.38}In_{0.62}As$ pseudomorphic HEMTs," *Electron Devices Meeting,* vol. 180, 1988.

[47] M. Aust*, et al.*, "A family of InGaAs/AlGaAs V-band monolithic HEMT LNAs," in *Gallium Arsenide Integrated Circuit (GaAs IC) Symposium, 1989. Technical Digest 1989., 11th Annual*, 1989, pp. 95-98.

[48] M. C. Foisy*, et al.*, "The role of inefficient charge modulations in limiting the current-gain cutoff frequency of the MODFET," *Electron Devices, IEEE Transactions on,* vol. 35, pp. 871-878, 1988.

[49] G. Gonzalez, *Microwave Transistor Amplifiers: Analysis and Design*, Second ed.: Prentice Hall, Inc, 1984.

[50] S. J. Mason, "Feedback Theory-Further Properties of Signal Flow Graphs," *Proceedings of the IRE,* vol. 44, pp. 920-926, 1956.

[51] A. Vanderziel, "GATE NOISE IN FIELD EFFECT TRANSISTORS AT MODERATELY HIGH FREQUENCIES," *Proceedings of the IEEE,* vol. 51, p. 461, 1963.

[52] J. Engberg, "Noise parameters of embedded noisy two-port networks," *Microwaves, Antennas and Propagation, IEE Proceedings H,* vol. 132, pp. 17-22, 1985.

[53] B. Pellegrini, "Semiconductor noise," *Physical review. B, Condensed matter,* vol. 38, pp. 8269-8278, 1988.

[54] C. Chih-Hung*, et al.*, "Novel Noise Parameter Determination for On-Wafer Microwave Noise Measurements," *Instrumentation and Measurement, IEEE Transactions on,* vol. 57, pp. 2462-2471, 2008.

[55] H. T. Friis, "Noise Figure of Radio Receivers," in *Proceedings of the IRE*, 1944, pp. 419-422.

[56] J. M. Rollett, "STABILITY AND POWER-GAIN INVARIANTS OF LINEAR TWOPORTS," *Ire Transactions on Circuit Theory,* vol. CT 9, pp. 29-&, 1962 1962.

[57] R. Ludwig and G. Bogdanov, *RF Circuit Design*, Second ed.: Pearson Prentice Hall, 2009.

[58] I. D. Robertson, *RFIC and MMIC design and technology*: The Institution of Electrical Engineers, 2001.

[59] S. Arshad, "Low Power Wideband InP Based Low Noise Amplifiers for the Square Kilometre Array Radio Telescope " Doctor of Philosophy, Faculty of Engineering and Physical Sciences, University of Manchester, Manchester, 2009.

[60] S. Arshad, "Low Power Wideband InP based Low Noise Amplifier for The Square Kilometre Array Radio Telescope," Doctor of Philosophy, Faculty of Engineering and Physical Sciences, University of Manchester, Manchester, 2009.

[61] Rutherford Aris, *Mathematical Modelling Techniques*. New York: Dover, 1978 (1994).

[62] W. R. Curtice, "A MESFET Model for Use in the Design of GaAs Integrated Circuits," *Microwave Theory and Techniques, IEEE Transactions on,* vol. 28, pp. 448-456, 1980.

[63] E. Arnold*, et al.*, "Direct extraction of GaAs MESFET intrinsic element and parasitic inductance values," in *Microwave Symposium Digest, 1990., IEEE MTT-S International*, 1990, pp. 359-362 vol.1.

[64] G. Dambrine*, et al.*, "A new method for determining the FET small-signal equivalent circuit," *Microwave Theory and Techniques, IEEE Transactions on,* vol. 36, pp. 1151-1159, 1988.

[65] M. Y. Jeon and Y. H. Jeong, "An approach to extract extrinsic parameters of HEMTs," *IEICE Transactions on Electronics,* vol. E83-C, pp. 1930-1935, 2000.

[66] K. Shirakawa, "Approach to determining an equivalent circuit for HEMT's," *IEEE Transactions on Microwave Theory and Techniques,* vol. 43, pp. 499-503, 1995.

[67] A. Caddemi*, et al.*, "Microwave characterization and modeling of packaged HEMTs by a direct extraction procedure down to 30 K," *Instrumentation and Measurement, IEEE Transactions on,* vol. 55, pp. 465-470, 2006.

[68] L. Fujiang and G. Kompa, "FET model parameter extraction based on optimization with multiplane data-fitting and bidirectional search-a new

concept," *Microwave Theory and Techniques, IEEE Transactions on,* vol. 42, pp. 1114-1121, 1994.

[69] S. Yanagawa, "Analytical method for determining equivalent circuit parameters of GaAs FET's," *IEEE Transactions on Microwave Theory and Techniques,* vol. 44, pp. 1637-1641, 1996.

[70] L. Sanga and J. E. Schutt-Aineb, "An improved Nonlinear Current Model for GaN HEMT High Power Amplifier with Large Gate Periphery," *Electromagnetic Waves and Applications,* vol. 26, pp. 284-293, 2012.

[71] I. Angelov*, et al.*, "A new empirical nonlinear model for HEMT and MESFET devices," *Microwave Theory and Techniques, IEEE Transactions on,* vol. 40, pp. 2258-2266, 1992.

[72] A. J. McCamant*, et al.*, "An improved GaAs MESFET model for SPICE," *Microwave Theory and Techniques, IEEE Transactions on,* vol. 38, pp. 822-824, 1990.

[73] H. Statz*, et al.*, "GaAs FET device and circuit simulation in SPICE," *Electron Devices, IEEE Transactions on,* vol. 34, pp. 160-169, 1987.

[74] I. O. Robertson, "CAD techniques for MMICs," in *MMIC's (Monolithic Microwave Integrated Circuits), IEE Colloquium on (Digest No.1995/221)*, 1995, pp. 3/1-3/8.

[75] A. EESof, "Nonlinear Device Models," vol. 2, ed. Palo Alto, CA 94304 USA: Agilent Technologies, 2006.

[76] J. B. Johnson, "Thermal agitation of electricity in conductors," *Physical Review,* vol. 32, pp. 97-109, 1928.

[77] H. Nyquist, "Thermal agitation of electric charge in conductors," *Physical Review,* vol. 32, pp. 110-113, 1928.

[78] A. Sobih, "MMIC Broadband Low Noise Amplifiers for the Square Kilometre Array Radio Telescope," Faculty of Engineering and Physical Sciences, The University of Manchester, Manchester, 2007.

[79] L. Forbes, "1/f Noise of GaAs resistors on semi-insulating substrates," *IEEE transactions on electron devices,* vol. 43, pp. 622-627, 1996.

[80] V. Mitin*, et al.*, *Noise and Fluctuations Control in Electronic Devices*: American Scientific Publishers 2002.

[81] A. B. Pashkovskii and A. S. Tager, "Diffusion noise in field:effect transistors with a submicron gate," *Radiophysics and Quantum Electronics,* vol. 30, pp. 853-860, 1987.

[82] R. L. Ross*, et al.*, *Pseudomorphic HEMT Technology and Applications*. Netherlands: Kluwer Academic Publishers, 1996.

[83] H. Fukui, "Optimal Noise-Figure of Microwave GaAs-MESFETs," *IEEE transactions on electron devices,* vol. 26, pp. 1032-1037, 1979.

[84] H. Fukui, "Design of MIcrowave GAAs-MESFETs for broad-band Low-Noise Amplifiers," *IEEE Transactions on Microwave Theory and Techniques,* vol. 27, pp. 643-650, 1979.

[85] A. Cappy, "Noise Modelling and Measurement Techniques," *IEEE Transactions on Microwave Theory and Techniques,* vol. 36, pp. 1-10, 1988.

[86] M. Pospieszalski, "Modeling of noise parameters of MESFET's and MODFET's and their frequency and temperature dependence," *IEEE Transactions on Microwave Theory and Techniques,* vol. 37, pp. 1340-1350, 1989.

[87] L. Kang-Sung, *et al.*, "35-nm Zigzag T-Gate $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As$ Metamorphic GaAs HEMTs With an Ultrahigh f_{max} of 520 GHz," *Electron Device Letters, IEEE,* vol. 28, pp. 672-675, 2007.

[88] K. M. Indlekofer and J. Malindretos, "WinGreen MX: User's Guide, Version 2," 2002.

[89] (1997, *Industry News : An IC characterisation and analysis program update*. Available:http://www.microwavejournal.com/articles/2105-an-ic-characterization-and-analysis-program-update

[90] "IC-CAP High-Frequency Model Tutorials," *IC-CAP Release 5.0,* vol. 2, June 1997.

[91] C. A. Liechti, "Microwave Field-Effect Transistors--1976," *Microwave Theory and Techniques, IEEE Transactions on,* vol. 24, pp. 279-300, 1976.

[92] G. Gonzalez, *Microwave Transistor Amplifier: Analysis and Design*. New Jersey: Prentice-Hall, 1984.

[93] S. Marsh, *Practical MMIC Design*: Artech House Publishers, 2006.

[94] I. D. Robertson and S. Lucyszyn, *RFIC and MMIC design and technology*: The Institution of Electrical Engineer, London, United Kingdom, 2001.

[95] Hong Shen, *et al.*, "Fabrication and Characterisation of Thin Film Resistors for GaAs-based Power Amplifiers " *International Conference on Compound Semiconductor Mfg,* 2003.

[96] R. Sharma, "RF parameter extraction of MMIC nichrome resistors," *Microwave and optical technology letters,* vol. 39, pp. 409-412, 2003.

[97] A. Meilberg, "An evaluation of three simple scalable AIM capacitor models," *IEEE Transactions on Microwave Theory and Techniques,* vol. 54, pp. 169-172, 2006.

[98] L. Wang, "MIM capacitor simple scalable model determination for MMIC application on gaas," *Electromagnetic waves,* vol. 66, pp. 173-178, 2006.

[99] S. S. Mohan, "Simple accurate expressions for planar spiral inductances," *IEEE journal of solid-state circuits,* vol. 34, pp. 1419-1420, 1999.

[100] "SKA brochure: The Internatinal Radio Telescope for the 21st Century," March 2011.

[101] A. Bouloukou*, et al.*, "Novel High Breakdown InGaAs/InAlAs pHEMTs for radio astronomy application," in *Proceedings of the 4th ESA Workshop on Milimeter Wave Technology and Applications (7th MINT Milimeter-wave International Symposium)*, Finland, 2006, pp. 221-226.

[102] F. Danneville*, et al.*, "Influence of the gate leakage current on the noise performance of MESFETs and MODFETs," *Solid-state electronics,* vol. 38, pp. 1081-1087, 1995.

[103] I. J. Bahl, *Fundamentals of RF and Microwave Transistor Amplifiers* New Jersey: John Wiley & Sons, Inc, 2009.

[104] P. P. Krüger, "A feasibility study of broadband low-noise amplifiers with multiple amplification paths for radio astronomy," Doctor of Philosophy in Physics, North-West University, Africa, 2010.

[105] A. S. Sedra and K. C. Smith, *Microelectronic Circuits*, Fourth Edition ed.: Oxford University Press, 1998.

[106] R. L. Wallace. *Common Gate Amplifiers*. Available: http://people.seas.-harvard.edu/jones/es154/lectures/lecture_6/pdfs/lecture23.pdf

[107] "Advanced Design System (ADS)," Agilent Technologies, Palo Alto, USA 2008.

[108] R. Simons, *Coplanar Waveguide Circuits, Components, and Systems*: Wiley, 2011.

[109] *Coplanar Waveguide Calculator*. Available: http://www.microwaves101-.com/encyclopedia/calcpw.cfm

[110] A. Tessmann*, et al.*, "High-gain cascode MMICs in coplanar technology at W-band frequencies," *Microwave and Guided Wave Letters, IEEE,* vol. 8, pp. 430-431, 1998.

[111] M. Danesh*, et al.*, "A Q-factor enhancement technique for MMIC inductors," in *Radio Frequency Integrated Circuits (RFIC) Symposium, 1998 IEEE*, 1998, pp. 217-220.

[112] J. Xu*, et al.*, "GaAs 0.5 dB NF dual-loop negative-feedback broadband low-noise amplifier IC," *Electronics Letters,* vol. 41, pp. 780-782, 2005.

[113] L. Belostotski and J. W. Haslett, "Sub-0.2 dB noise figure wideband room-temperature CMOS LNA with non-50 Omega signal-source impedance," *IEEE journal of solid-state circuits,* vol. 42, pp. 2492-2502, Nov 2007.

[114] R. H. Witvers*, et al.*, "Sub 0.15dB noise figure room temperature GaAs LNA for next generation radio telescope," in *Microwave Conference (EuMC), 2010 European*, 2010, pp. 1078-1081.

[115] H. Wang*, et al.*, "A Wideband Inductorless LNA With Local Feedback and Noise Cancelling for Low-Power Low-Voltage Applications," *Ieee Transactions on Circuits and Systems I-Regular Papers,* vol. 57, pp. 1993-2005, Aug 2010.

[116] F. A. Levinzon, "Ultra-low-noise high-input impedance amplifier for low-frequency measurement applications," *Ieee Transactions on Circuits and Systems I-Regular Papers,* vol. 55, pp. 1815-1822, Aug 2008.

[117] Y. M. Chi*, et al.*, "Ultra-High Input Impedance, Low Noise Integrated Amplifier for Noncontact Biopotential Sensing," *Emerging and Selected Topics in Circuits and Systems, IEEE Journal on,* vol. 1, pp. 526-535, 2011.

[118] P. P. Kruger, "Cheap 0.36 dB NF broadband multipath LNA," *Electronics Letters,* vol. 48, pp. 315-316, Mar 2012.

[119] www.skatelescop.org.

[120] S. Arshad*, et al.*, "Sub-0.6 dB NF Low Power Differential to Single-Ended MMIC LNA Designs for the SKA using InGaAs/InAlAs/InP pHEMTs," in *Wide Field Astronomy & Technology for the Square Kilometre Array*, Limelette, Belgium, 4-6 November 2009, p. 295.

[121] T. Baker, "Successful LNA design involves performance trade-offs," ed. Freescale Semiconductor, Inc. Tempe, November 2006.

[122] E. A. Sobhy*, et al.*, "A 2.8-mW Sub-2-dB Noise-Figure Inductorless Wideband CMOS LNA Employing Multiple Feedback," *IEEE Transactions on Microwave Theory and Techniques,* vol. 59, pp. 3154-3161, Dec 2011.

[123] *Agilent AN 154 S-Parameter Design Application Note*. Available: http://care.iitd.ac.in/People/Faculty/bspanwar/crl721/S-Parameter%20Design_Agilent%20AN%20154.pdf