# LOW NOISE AMPLIFIERS USING HIGHLY STRAINED InGaAs/InAlAs/InP pHEMT FOR IMPLEMENTATION IN THE SQUARE KILOMETRE ARRAY (SKA)

A thesis submitted to The University of Manchester for the degree of

**Doctor of Philosophy**

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# TABLE OF CONTENTS

# LIST OF TABLES

# LIST OF FIGURES AND ILLUSTRATIONS

# LIST OF ABBREVIATIONS

| | |
|---|---|
| **2-DEG** | 2-Dimensional Electron Gas |
| **ADS** | Advanced Design System |
| **AlGaAs** | Aluminium Galium Arsenide |
| **CMOS** | Complementary Metal Oxide Semiconductor |
| **CPW** | Coplanar Wave Guide |
| **CS** | Common-Source |
| **DI water** | De-ionised water |
| **DSLNA** | Double Stage Low Noise Amplifier |
| **DUT** | Device Under Test |
| **e-beam** | Electron beam |
| **EDA** | Electronic Design Automation |
| **FET** | Field Effect Transistor |
| **FP** | Field plate |
| **Ga** | Galium |
| **GaAs** | Galium Arsenide |
| **Ge** | Germanium |
| **HEMT** | High Electron Mobility Transistor |

| | |
|---|---|
| **HG-DSLNA** | High Gain Double Stage Single-ended LNA |
| **IC** | Integrated Circuit |
| **IC-CAP** | Integrated Circuit Characterisation and Analysis Program |
| **InAlAs** | Indium Aluminium Arsenide |
| **InGaAs** | Indium Galium Arsenide |
| **InP** | Indium Phosphide |
| **IPA** | Isopropanol |
| **LNA** | Low Noise Amplifier |
| **ISS** | Impedance Standard Substrate |
| **M&N** | Microelectronic & Nanostructures |
| **MBE** | Molecular Beam Epitaxy |
| **MESFET** | Metal Semiconductor Field Effect Transistor |
| **MG-DSLNA** | Moderate Gain Double Stage Single-ended LNA |
| **MIC** | Microwave Integrated Circuit |
| **MIM** | Metal-insulator-metal |
| **MMIC** | Monolithic Microwave Integrated Circuit |
| **MOCVD** | Metalorganic Chemical Vapour Deposition |
| **MOSFET** | Metal-Oxide-Semiconductor Field Effect Transistor |
| ***NF*** | Noise Figure |

| | |
|---|---|
| $NF_{min}$ | Minimum Noise Figure |
| **NiCr** | Nickel Chromium or Nichrome |
| **nMOS** | n-type channel MOS |
| **PA** | Power Amplifier |
| **PCM** | Process Control Module |
| **pHEMT** | pseudomorphic High Electron Mobility Transistor |
| **PMGI** | Polymethylglutarimide |
| **QW** | Quantum Well |
| **RA** | Radio Astronomy |
| **RF** | Radio Frequency |
| **RT** | Room Temperature |
| **S-parameter** | Scattering parameter |
| **SA** | Succinic Acid |
| **S-G-D** | Source-Gate-Drain |
| **Si** | Silicon |
| **SiGe** | Silicon Germanium |
| **SKA** | Square Kilometre Array |
| **SNR** | Signal to Noise Ratio |
| **SOLT** | Short-Open-Load-Thru |

| | |
|---|---|
| **SSLNA** | Single Stage Single-ended LNA |
| **TCR** | Temperature Coefficient Resistance |
| **TE** | Thermionic Emission |
| **TFE** | Thermionic Field Emission |
| **TLM** | Transfer Length Method |
| **UoM** | University of Manchester |
| **UV** | Ultraviolet |
| **VLA** | Very Large Array |
| **VNA** | Vector Network Analyser |

# ABSTRACT

The University of Manchester
Candidate : Muammar Mohamad Isa
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Title : Low Noise Amplifiers using highly strained InGaAs/InAlAs/InP pHEMT for implementation in the Square Kilometre Array (SKA)
Date : 17th October 2012

The Square Kilometre Array (SKA) is a multibillion and a multinational science project to build the world's largest and most sensitive radio telescope. For a very large field of view, the combined collecting area would be one square kilometre (or 1, 000, 000 square metre) and spread over more than 3,000 km wide which will require a massive count of antennas (thousands). Each of the antennas contains hundreds of low noise amplifier (LNA) circuits. The antenna arrays are divided into low, medium and high operational frequencies and located at different positions to boost up the telescope's scanning sensitivity.

The objective of this work was to develop and fabricate fully on-chip LNA circuits to meet the stringent requirements for the mid-frequency array from 0.4 GHz to 1.4 GHz of the SKA radio astronomy telescope using Monolithic Microwave Integrated Circuit technology (MMIC). Due to the number of LNA reaching figures of millions, the fabricated circuits were designed with the consideration for low cost fabrication and high reliability in the receiver chain. Therefore, a relaxed optical lithography with $L_g$ = 1 µm was adopted for a high yield fabrication process.

Towards the fulfilment of the device's low noise characteristics, a large number of device designs, fabrication and characterisation of InGaAs/InAlAs/InP pHEMTs were undertaken. These include optimisations at each critical fabrication steps. The device's high breakdown and very low gate leakage characteristics were further improved by a combination of judicious epitaxial growth and manipulation of materials' energy gaps. An attempt to increase the device breakdown voltage was also employed by incorporating Field Plate structure at the gate terminal. This yielded the devices with improvements in the breakdown voltage up to 15 V and very low gate leakage of 1 µA/mm, in addition to high transconductance ($g_m$) characteristic. Fully integrated double stage LNA had measured *NF* varying from 1.2 dB to 1.6 dB from 0.4 GHz to 1.4 GHz, compared with a slightly lower *NF* obtained from simulation (0.8 dB to 1.1 dB) across the same frequency band.

These are amongst the attractive device properties for the implementation of a fully on-chip MMIC LNA circuits demonstrated in this work. The lower circuit's low noise characteristic has been demonstrated using large gate width geometry pHEMTs, where the system's noise resistance ($R_n$) has successfully reduced to a few ohms. The work reported here should facilitate the successful implementation of rugged low noise amplifiers as required by SKA receivers.

## DECLARATION

No portion of the work referred to in the thesis has been submitted in support of an application for another degree or qualification of this or any other university or other institute of learning**.**

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# DEDICATION

*To my caring parents.....*

*To my loving wife.....*

*To my lovely children.....*

# PUBLICATIONS

1. **M. Mohamad Isa** , Y. Lai , D. Saguatti , M. Missous "*Improvement of breakdown voltage in InGaAs/InAlAs/InP pHEMT using band gap engineering and field modulating plate structure*" in UK Semiconductor 2012 Conference, The University of Sheffield, 4-5 July 2012

2. F. Packeer, **M. Mohamad Isa** and M. Missous *"Fabrication and Characterization of Tensile In0.3Al0.7As Barrier and Compressive In0.7Ga0.3As Channel pHEMTs Having Extremely Low Gate Leakage for Low Noise Applications"* in UK Semiconductor 2012 Conference, The University of Sheffield, 4-5 July 2012

3. W M Jubadi, **M. Mohamad Isa** and M. Missous, *" An accurate 2D Physical Model for highly strained InAlAs/InGaAs pHEMTs"* in UK Semiconductor 2012 Conference, The University of Sheffield, 4-5 July 2012

4. N. Ahmad, **M. Mohamad Isa** and M. Missous, "*Modelling, Design and Testing of Novel InGaAs-InAlAs Low Noise Amplifier for Radio Astronomy Applications*" in UK Semiconductor 2012 Conference, The University of Sheffield, 4-5 July 2012

5. **M. Mohamad Isa**, M. Missous and J. Sexton**,** "*A Large Band gap, High breakdown In0.3Al0.7As-In0.7Ga0.3As pHEMT for low power mobile communications system*", Postgraduate Poster Conference and Industrial Advisory Group Meeting, The University of Manchester, 30 Nov 2011.

6. N. Ahmad, **M.Mohamad Isa** and M. Missous "*Modelling and Design of MMIC Low Noise Amplifier using an in-house InP-based Process*", Postgraduate Poster Conference and Industrial Advisory Group Meeting, The University of Manchester, 30 Nov 2011

7. **M. Mohamad Isa**, M. Missous, Y. Lai, J. Sexton, and S. Boulay, "*Fabrication of Low Noise InAlAs-InGaAs pHEMT for SKA application (300MHz to 2GHz)*", in UK Semiconductor 2011 Conference, The University of Sheffield, 6-7 July 2011.

8. Y. Lai, **M. Mohamad Isa** and M. Missous, "*Pulsed DC characterisation of high breakdown, low leakage InAlAs/InGaAs/InP pHEMTs*" in UK Semiconductor 2011 Conference, The University of Sheffield, 6-7 July 2011.

9. **M. Mohamad Isa**, N. Ahmad, M. Missous, Y. Lai, J. Sexton, and S. Boulay**,** "*Fabrication of Low Noise InAlAs-InGaAs pHEMT for SKA application (300MHz to 2GHz)*", in IMiEJS 2011 Conference, Athlone Institute of Technology (AIT), Ireland, 9-11 June 2011.

10. Saguatti, D., Chini, A., Verzellesi, G., **Isa, M. M**., Ian, K. W., and Missous, M. , "*Improvement of Breakdown and DC-to-Pulse Dispersion Properties in Field-Plated InGaAs-InAlAs pHEMTs*" , International Conference on Indium Phosphide & Related Materials (IPRM), 22 – 26 May, 2011 Berlin, Germany, pp. 84-86.

11. **M. Mohamad Isa,** D. Saguatti, G. Verzellesi, A. Chini, K.W. Ian, M. Missous, "*Fabrication of novel high frequency and high breakdown InAlAs-InGaAs pHEMTs*," in 8th International Conference on Advanced Semiconductor Devices & Microsystems (ASDAM), 2010, 25 – 27 Oct. 2010, pp. 41-44.

12. **M. Mohamad Isa,** D. Saguatti, G. Verzellesi, A. Chini, K.W. Ian, M. Missous, *"Novel high frequency and high breakdown InAlAs-InGaAs pHEMTs for low noise and high power applications*", in UK Semiconductor 2010 Conference, The University of Sheffield, 7-8 July 2010.

13. D. Saguatti, **M. Mohamad Isa,** K. W. Ian, and M. Missous, . " *InAlAs-InGaAs pHEMT TCAD Simulation and Optimization"*, in UK Semiconductor 2010 Conference, The University of Sheffield, 7-8 July 2010.

14. Saguatti, D., Chini, A., Verzellesi, G., **Isa, M. M**., Ian, K. W., and Missous, M., "*TCAD optimization of field-plated InAlAs-InGaAs HEMTs*", International Conference on Indium Phosphide & Related Materials (IPRM), 31 May – 4 June 2010. Takamatsu Symbol Tower, Kagawa, Japan, pp. 1-3.

# CHAPTER 1

# INTRODUCTION

## 1.1 OVERVIEW OF THE SKA

Over the last few decades, the desire to learn more about our solar system, and more fundamentally, how the universe began, led to the launch of large astronomy projects and deep space probes. Although these missions have yielded important scientific discoveries and improved our understanding of the cosmos, they have not explored the most fundamental questions about the universe. These include: understanding dark energy, general relativity in extreme conditions, and how the universe was shaped into its current form; from immediately after the big bang to the present day.

The rapid advancement in technology has provided the means for space exploration equipment to deliver more meaningful data about the cosmos than ever before, of which the Square Kilometre Array (SKA) is one example. The project is destined to be a multibillion dollar, multinational science project, for establishing the world's largest and most sensitive radio telescope [1]. Work has already started in the science, engineering and associated industries to drive the development of technology in antennas, signal transport, signal processing, software and computing.

Central to the concept of the SKA is a deep understanding of the sensitivity of a radio telescope. The sensitivity (S) of a telescope is dependent on its effective collecting area ($A_{eff}$) and the receiver equivalent system temperature ($T_{sys}$) [2]:

$$S = \frac{A_{eff}}{T_{sys}} \qquad \text{Equation 1-1}$$

From Equation 1-1, the sensitivity of a Radio Telescope system is directly proportional to the system's effective collecting area. The equation also shows that the sensitivity can be improved if the system is operated at low temperature.

Since the radio signals originating from cosmic sources are very faint in nature, astronomers require a highly sensitive and physically large telescope in order for the very small signals to be detected. However, building such a large telescope receiver is impractical. The most practical way to increase the sensitivity is by arranging a number of smaller-sized receivers in an array, which synthesises a larger telescope receiver.

The shift from a single dish to arrays of receiver dishes began in 1980 with the implementation of the Very Large Array (VLA) radio astronomy telescope. The VLA system consists of 27 independent antennas with each dish having a diameter of 25 metres. The antennas are arrayed along the three arms of a Y-shape, with each arm measuring 21 km in length [3].

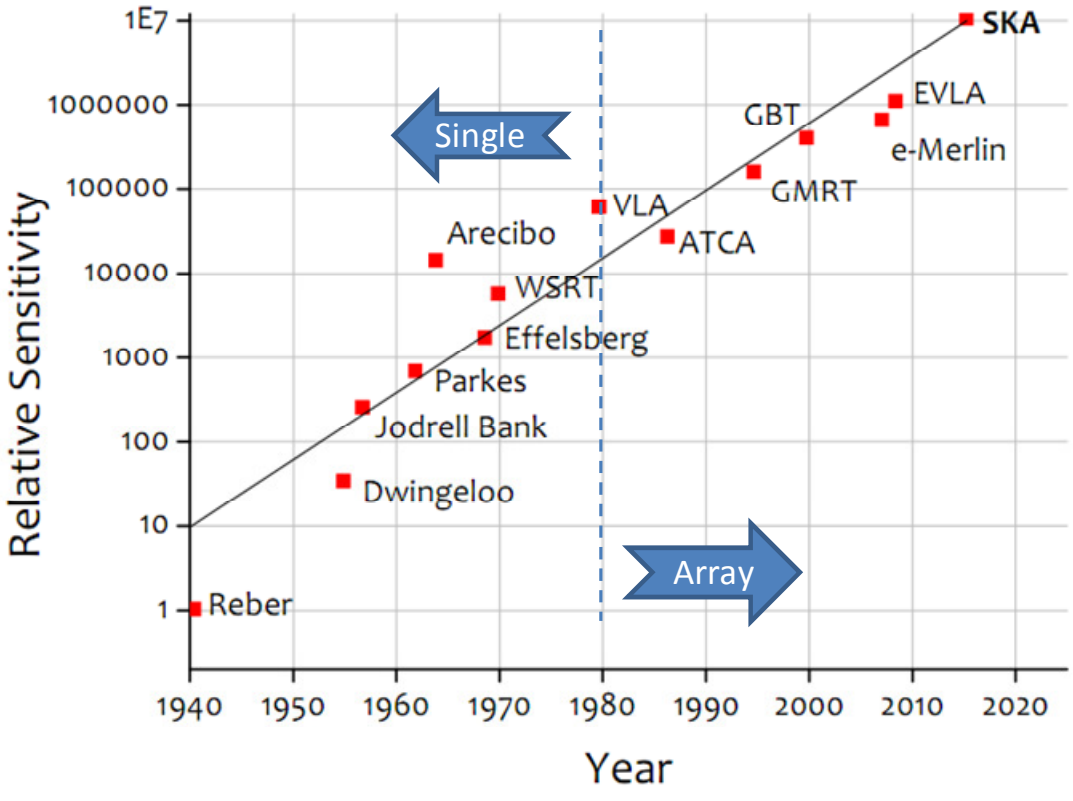



Figure 1-1 Sensitivity of the SKA with world leading telescopes [4]

Over the years, more radio telescopes were built using the similar concept of arrays of receivers with a larger collection area for greater sensitivity. Figure 1-1 illustrates various types of radio telescope and the transition from a single large parabolic dish to an array of smaller dishes. The projection ends with the SKA, which is expected to have a relative sensitivity one hundred times better than the best of the existing radio interferometers today.

Another alternative to increase the system sensitivity is by lowering the system noise temperature (refer Equation 1-1). It is anticipated that the SKA will have a lower noise temperature by cryogenically cooled the receiver modules [5], where the individual sensitivity of each receiver subsystem associated with few thousands Low Noise Amplifiers (LNAs) can be maximised. When the LNAs are cryogenically cooled, the circuit low noise characteristics can be improved to a greater extend and consequently increasing the system sensitivity.

Since large numbers of LNAs are needed (several thousands), considering the cost and complexity of the cryogenic cooled system (which is another extension of greater challenge), the Room Temperature (RT) application is then considered. Therefore, the focus of this SKA project, for the reason mentioned above, is assessed with respect to its RT application [6].

## 1.2 THE CONCEPT OF THE SKA

At present, the complete bandwidth of the SKA ranges from 70 MHz to 10 GHz [7]. To achieve such a wide bandwidth, a massive collecting area that still maintains a high signal to noise ratio (SNR) is achieved by arrays of antennas. These antennas will be arranged in a spiral shape and are distributed in three regions with a diameter extending to 3000 km [8, 9], as shown in Figure 1-2.

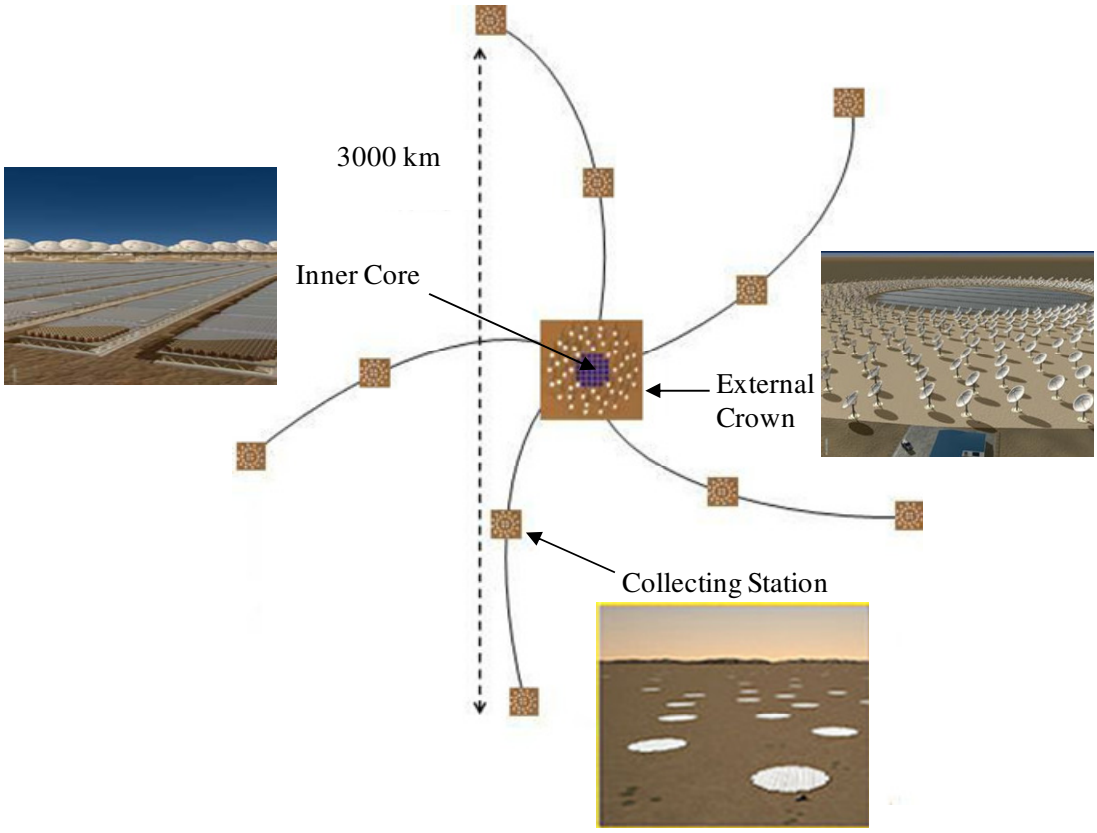



Figure 1-2 An illustration of antenna dislocation [8]

The spiral core will be formed by two topologies of antennas that become half of the collecting area. The core will be smaller in diameter and will contain a dense of aperture arrays for low frequency radio-signals, and will be surrounded by parabolic dishes, which are used for high frequency radio-signals. Even though the resolution will be sacrificed when the aperture arrays are close to each other, this arrangement will capture characteristic information, such as object brightness and temperature. The planar arrays are fixed but they can be steered electronically, whereas the parabolic dishes can be moved mechanically to cover the entire horizon.

Along the spiral arms, several stations are located extending out to 150 km. Each station will contain hundreds of dense aperture arrays for medium frequency radio signals.

The outer region of the SKA will cover a large area between 180 km to 3000 km. This region will include five spiral arms along with aperture arrays that are

combined into stations. There will be an increase in separation of the stations in the outer region of the spiral arms

As briefly described in the above, the SKA will use three different types of antenna across the frequency bandwidth - high frequency dishes for 1.2 to 10 GHz, mid frequency aperture array from 0.4 to 1.4 GHz, and low frequency aperture array from 70 to 450 MHz [10]. Figure 1-3 illustrates the separation and the key observations for each frequency region.

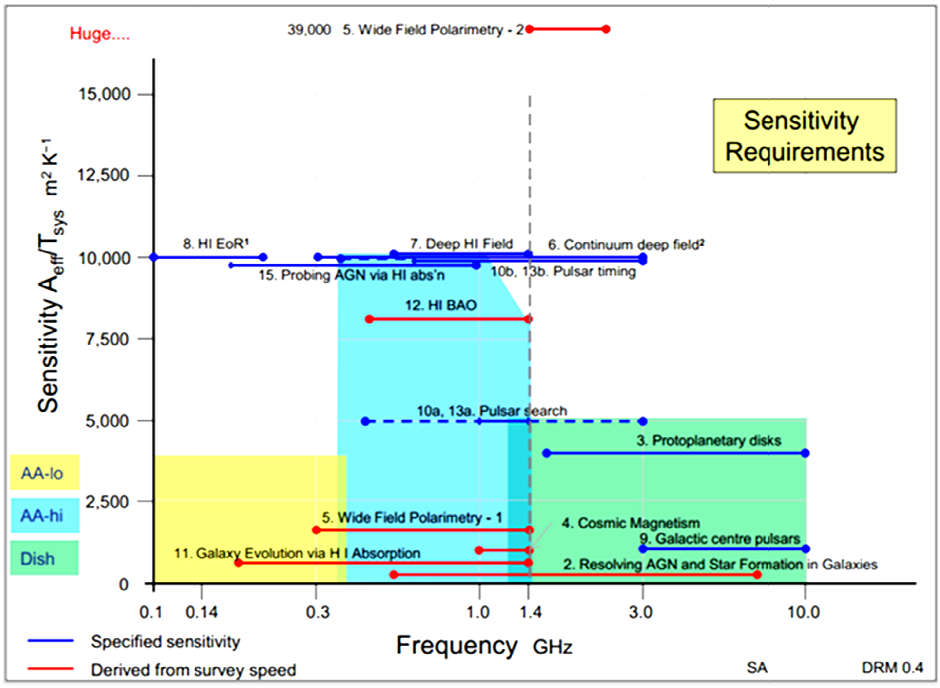



Figure 1-3 The Sensitivity of the SKA Radio Telescope (AA = Aperture array) [10]

The stringent requirement of the SKA for a wide field of view and large collecting area demands a high linearity, low power dissipation, and low-noise phased-array receiving block. In order to amplify the weak signals received by the antenna, a low noise amplifier (LNA) is placed at each receiver end and transfers the signal to the remaining receiving circuits to fulfil the SKA requirements. The large number of receivers adds a significant cost consideration to the design of the unit element to keep the budget under control.

Moreover, cooling of the receiver modules in order to improve their noise temperature has not been fully explored, as the running costs of cooling such a massive collector array would most likely make the cryogenic methods an

economically unfeasible option. For this reason the technology being developed for the SKA is being assessed in respect of its room temperature operating properties [11].

Therefore, in this project, the aim is to develop the front-end system using a novel InP-based pseudomorphic High Electron Mobility Transistor (pHEMT) technology for the design and fabrication of LNAs, optimised in the band 0.4 – 1.4 GHz in meeting the mid frequency performance requirements of the SKA in terms of performance, cost and power budget.

## 1.3 OBJECTIVES

The key objective of this work focuses on the development of Indium Galium Arsenide/Indium Aluminium Arsenide/Indium Phosphide (InGaAs/InAlAs/InP) devices for low noise applications at radio frequencies. The adaptation of band-gap engineering in conjunction with low cost I-line optical photolithography is the prime focus in achieving low noise devices. This is an alternative to highly scaled and sophisticated technologies such as nano-scaled Complementary Metal Oxide Semiconductor (CMOS), which involves more complicated steps and not cost effective with respect to this application. In terms of manufacturability, the requirements for the optical lithography method adopted in this work are less stringent (in terms of feature sizes and mask costs) than deep Ultraviolet (UV) lithography, especially those used in Si technology. Several types of LNA circuits, which employed this technology will be presented here as proof of the suitability of the technology and also to provide a starting point for future applications in microwave communication systems. The LNA design specifications are detailed in the following section.

### 1.3.1 LNA Specifications

All the work presented in this thesis converged into one purpose, which is to obtain a very low Noise Figure (*NF*) amplifiers operating at Room Temperature (RT) using the 1 μm highly strained channel based on InGaAs/InAlAs/InP pHEMT technology

developed at the University of Manchester (UoM). The large gate peripheries are advantageous from the perspective of manufacturing cost and throughput where expensive electron-beam (e-beam) lithography can certainly be avoided.

The LNAs in this project are determined to operate in the mid frequency range (0.4 GHz to 1.4 GHz) of the SKA. The same frequency band has also found its application in medium frequency commercial applications such as Global Positioning System (GPS) and mobile communication.

The paramount importance in terms of specification in the design is the *NF*. The *NF* of the project is set to be less than 1 dB over the chosen frequency bandwidth. However, in the final SKA specification, the *NF* is further tightened to a lower value of 0.5 dB. The lower *NF* is highly desirable for the system as a whole, where low *NF* will only need smaller and consequently cost effective collection area.

The amplifiers must also be unconditionally stable over the entire operational bandwidth. Given that the oscillation is knowingly common in high gain circuit [12], the gain of the circuit is determined to be in modest value of about 25 dB to 35 dB.

Furthermore, the amplifier is configured to consume power of less than 150 mW. The commonly used load impedance of 50 Ω is dedicated for the circuit to facilitate the interfacing with the measurement tools and integration with other components in the system.

## 1.4 THESIS OUTLINE

**Chapter 2** begins with an elaborative study of semiconductor materials suitable for high frequency operation, leading to in-depth discussions concerning appropriate devices for the advanced materials discussed. The discussion continues with an extensive study of the physics and operation of the devices. At the end of the chapter, some important physical parameter extraction methods are highlighted, as these methods are used throughout this work.

**Chapter 3** discusses the performed optimisation steps of the in-house pHEMT's fabrication steps. The task begins with the development of an optimal gate recess

recipe using highly selective succinic acid etchant for highly uniform Schottky contacts. The results from this study are then used for the design of the gate-to-channel isolation technique to minimise the gate leakage current of the device. In addition, a thermal stability study is performed to investigate the reliability of the device during high temperature processing.

**Chapter 4** presents the fabrication and characterisation of a novel low-leakage high-breakdown InGaAs/InAlAs/InP pHEMT, which is targeted for implementation in the LNA design as described in **Chapter 6**. To complete the discussion, comprehensive comparisons are made with other published device data prepared for the same purpose.

**Chapter 5** highlights the adaptation of a field plate structure to improve the device breakdown voltage, which is beneficial for low noise high power applications. For comparison, the DC and RF characteristics of the device are evaluated with respect to the conventional narrow band gap channel InGaAs/InAlAs/InP device.

**Chapter 6** provides the full description of the fabrication process of three LNA circuits utilising the low noise device detailed in **Chapter 4**. At the beginning of the chapter, the fabrication and characterisation of passive devices are described, including out of target passives which caused a mismatch in the circuit's noise performance.

**Chapter 7** summarises the work discussed in this project, stressing the potential from the project and the consequent suitability of the developed devices and LNA circuits to meet the requirements of the SKA. Finally, some additional work is suggested for further improvement and extension from the findings in this thesis.

# CHAPTER 2

# LITERATURE REVIEW

## 2.1 INTRODUCTION

Lower cost and higher levels of integration have undoubtedly allowed Silicon (Si) technologies to become the workhorse of semiconductor material in the digital Integrated Circuit (IC) prime markets in the electronic age. This unrivalled status is mostly due to its superior chemical and electrical characteristics. However, due to Si low intrinsic mobility, other materials are more suitable for future high-speed and low-power applications at high frequencies. For example, III-V materials are having significantly higher intrinsic mobility and can substitute Si as a promising solution for high speed applications. III-V materials can also be designed into suitable device structures by means of adapting similar processing techniques used in Si technology such as lithography and etching [13]. In this regard, III-Vs are considered far more practical than other non-Si materials for future high-speed applications. Indeed, both Galium Arsenide (GaAs) and Indium Galium Arsenide (InGaAs) materials are possible future candidates in the post sub-22 nm node CMOS [14].

This chapter will highlight the properties and operational principles of suitable devices for high speed, low noise applications, derived from III-V materials. Several important parameter extraction methods are also included at the end of the chapter.

## 2.2 HIGH FREQUENCY MATERIALS

III-V compounds have a number of desirable material characteristics which make them superior to Si in high-frequency applications. The primary characteristic is high carrier electron mobility. This contributes to making the materials very responsive to rapid changes in applied electric fields. Furthermore, since the mobility of electrons far exceeds that of the holes, electrons are invariably used in high frequency devices.

Another useful property of III-V compounds is the higher band gap energy compared to Si, allowing the synthesis of insulating and semi-insulating materials that are essential in high frequency circuits. The rich variety of available materials also allow for lower band gap materials with superior transport characteristics and very high mobilities.

However, for a low band gap material, there are a large number of carriers that have sufficient thermal energy to overcome the metal-semiconductor junction barrier, resulting in higher leakage devices when compared with Si. On the other hand, the band gap should not exceed to a greater extent as it may require high thermal energy to turn ON the device. Nevertheless, a suitable combination of small and large band gap materials can be chosen so that the leakage or the required thermal energy does not become a concern.

Figure 2-1 shows the low field electron mobility versus energy band gap for common semiconductors. The semiconductors consist of elemental (Ge and Si) and compound semiconductors (binary compounds such as II-VI and III-V group elements). In the diagram, most of the direct and low band gap materials are located in the first quadrant and have electron mobility higher than that of Si. However, as mentioned above, they are not always the favourable candidates due to their lower energy gap as they lead to leakier device characteristics. The materials in the third quadrant have a higher energy gap than that of Si, but are not good candidates for active channels, since the electron mobility is so much lower than in Si. This characteristic leaves two materials in the second quadrant, where the electron mobility and band gap energy are higher than those of Si. The two compound semiconductors are the GaAs and InP. Both are binary alloys formed from group III and group V element semiconductors. The characteristics of Si, GaAs and InP are shown in Table 2-1. Included in the table are the electrical properties of the high mobility InP-based ternary compound, $In_{0.53}Ga_{0.47}As$, the importance of which will be detailed later.

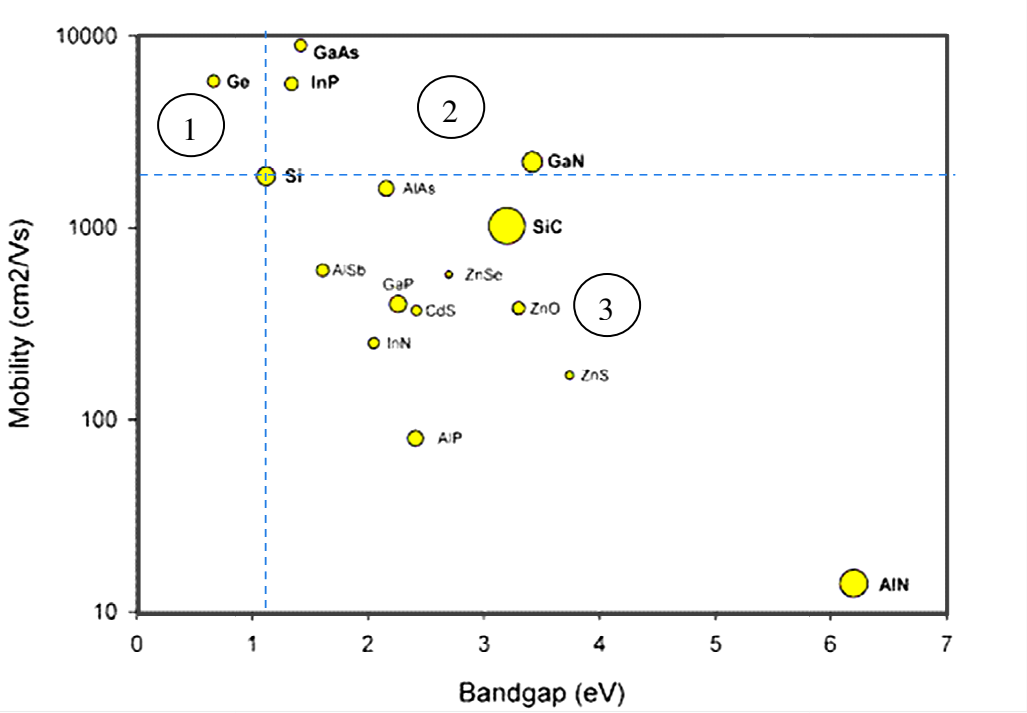



Figure 2-1 Electron mobility at low field strength versus band gap energy for various semiconductor materials. The line represents electron mobility and energy band gap levels higher than Si. The second quadrant materials are the most suitable compound semiconductors for high frequency applications, to replace Si in bulk material (except GaN because $E_g$ is high) [15].

By referring to Table 2-1, the energy band gaps for GaAs and InP (1.42 eV and 1.35 eV respectively) are higher than that of Si. Even though this value is higher than Si, it is still sufficiently small when compared to other semiconductor materials; therefore, electrons are easily excited into the conduction band for effective device conduction. Referring to carrier mobility, InP has an electron mobility three times higher than that of Si, whereas GaAs has a mobility that is almost six times higher than Si. There are many advantages associated with this high carrier mobility. For instance, when considering low noise applications in higher mobility materials, the random noise events resulting from carrier collisions within the lattice are less significant relative to the drift current produced by the carriers [16].

Table 2-1 Comparisons between Si and high frequency materials [17-20].

| Characteristics | Si | GaAs | InP | $In_{0.53}Ga_{0.47}As$ |
|---|---|---|---|---|
| **Lattice Constant (Å)** | 5.431 | 5.653 | 5.869 | 5.869 |
| **Band gap (eV)** | 1.12 | 1.42 | 1.35 | 0.71 |
| **Electron Saturation velocity ($10^7$ cm/s)** | 1.0 | 1.0 | 1.3 | 0.7 |
| **Electron mobility at 300 K ($cm^2$/V.s)** | 1,500 | 8,500 | 4,500 | 12,000 |
| **Hole mobility at 300 K ($cm^2$/V.s)** | 400 | 400 | 150 | 300 |
| **Critical breakdown field (MV/cm)** | 0.3 | 0.4 | 0.5 | 0.2 |
| **Relative dielectric constant** | 11.8 | 12.8 | 12.5 | 13.8 |

However, compared to GaAs and InP, an even higher electron mobility can be achieved from $In_{0.53}Ga_{0.47}As$ which is lattice matched to InP. Even though the energy gap is less than Si, the high carriers' thermal excitation from valance band to conduction band is compensated by this superior electron mobility property. Through the advancement in epitaxial growth, this material (or other materials lattice matched to InP) can be grown on top of an InP substrate, therefore this compound is sometimes called InP-based material. Further discussion of this material is shown in subsequent sections.

Above all, when compared to the Si-based devices, these materials are determined to have more current gain, mainly due to their high electron mobility; if the same input voltage is applied, higher output current can flow from these materials and consequently higher gain can be achieved.

Furthermore, the high electron mobility property implies that the carriers can navigate through the device geometry in a very short transit time, thereby promoting

its high frequency application. A high carrier velocity will allow the device to be responsive to high frequency excitation. A comparison of carrier drift velocity versus applied electric field between Si, GaAs, InP and $In_{0.53}Ga_{0.47}As$ is shown in Figure 2-2. In low field-strength operation, Si is shown to have the lowest drift velocity whereas $In_{0.53}Ga_{0.47}As$ is illustrated to have the highest. However, at high field operation, the carrier velocity for GaAs, InP and $In_{0.53}Ga_{0.47}As$ drop to values that are comparable to the Si saturation velocity. The saturation velocities of undoped materials are also shown in Table 2-1.

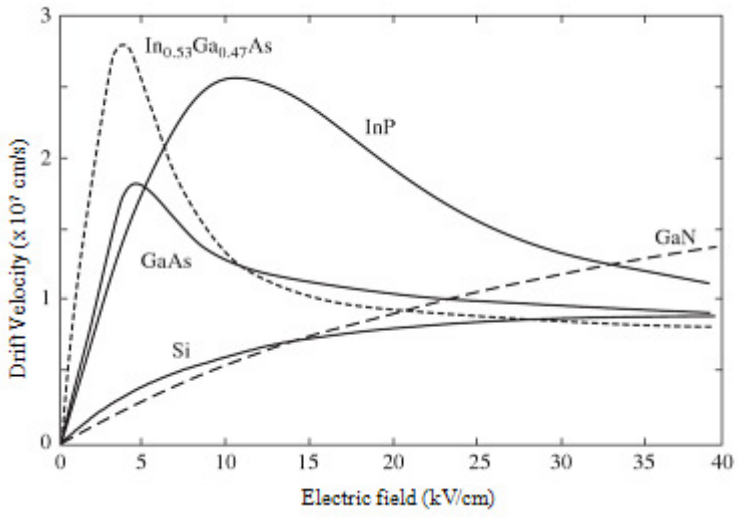



Figure 2-2 Electron drift velocity of common semiconductor materials at low field operation [20]

This phenomenon occurs because in GaAs, InP and $In_{0.53}Ga_{0.47}As$ materials, there exist more than one local minima in the energy band gap. Most of the time (at low electric field-strengths), the electron will occupy the first local minima; at that point the electrons have a low effective mass and therefore high mobility. However, when the applied electric field is increased to about 3.2 kV/cm, the electron will have sufficient energy to occupy the second minima. At the second minima, the electrons will have higher effective mass and will have lost their high mobility property. As the electric field is increased further, more electrons will occupy this low mobility region and their velocity will continue to decrease until a point where all the electrons completely occupy the second local minima. At this point, the drift velocity will level off as shown in Figure 2-2.

Notwithstanding the above advantages, both materials do have drawbacks. In general, Si is a more cost effective material in fabrication processes, is a more mature technology and has better device characterisation and understanding. In production lines, the yield in Si processing has been increased repeatedly, along with improvements in material reliability. It should be noted that Si, with its inherent advantage of exceptional native oxide ($SiO_2$), makes the devices significantly more stable.

At present, Silicon-Germanium (SiGe) heterostructures with Si are a topic of significant research interest in order to cater the low carrier mobility, which closely related to the Si properties. The emerging new material has offered the possibility to extend the reach of Si technology into areas of high mobility - high speed applications which were dominated by the III–V devices. This technology has offered many advantages associated with heterostructures, in addition to largely compatible with standard Si IC processing techniques [21].

For the III-V material type, comparing between GaAs and InP-based compounds such as InGaAs and InAlAs, the advantages of InGaAs-InAlAs over GaAs are less perceptible due to issues such as non-optimum material characteristics, buffer layer and substrate quality problems. There are also additional technical issues related to the low energy gap of the InGaAs channel and low barrier height of InAlAs Schottky gates. Consequently, more electrons are thermally excited over the rather low Schottky barrier and this leads to an increase in gate leakage current [16].

## 2.3 LATTICE MATCHED AND PSEUDOMORPHIC MATERIALS

Over the years, much work has been carried out and a number of material systems have been extensively studied as alternatives to bulk GaAs. One important discovery concerns the manipulation of energy bands by band gap engineering. Here, the idea of combining multiple unequal energy gaps is often advantageous to the electrical properties used in many solid-state device applications. It is realised by growing layers of similar crystalline structure on top of each other by means of Molecular Beam Epitaxy (MBE) or Metalorganic Chemical Vapour Deposition (MOCVD). The interface that occurs between them is called a heterojunction. Multiple

heterojunctions combined in one structure are called heterostructures. This has lead to the emergence of a new class of high-speed devices, that a high quality junction between semiconductors of different band gaps can be formed.

At this point, the quality of the semiconductor depends on the materials' lattice constant ($a_0$). The lattice constant is defined as the distance between the unit-cell of the periodic crystal. A lattice matched structure is formed when two different materials with nearly the same lattice properties are grown on top of each other. Therefore, the quality of the resulting structure greatly depends on the quality of the matching between the two lattice constants [16].

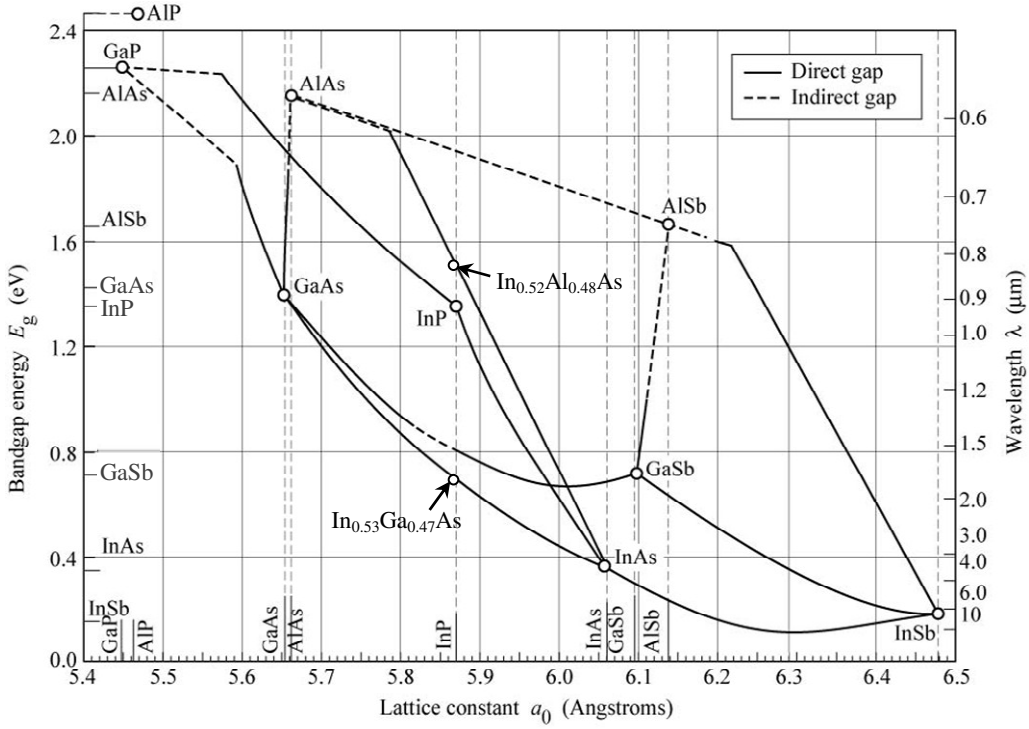



Figure 2-3 Minimum energy band gap versus lattice constant for various semiconductor materials. Shown in the graph is the ternary compound lattice matched to InP substrate [22]

Figure 2-3 shows the energy band gap ($E_g$) versus lattice constant for various semiconductor materials that are of interest to the work presented here. Illustrated in the figure are the ternary compound semiconductor materials that are lattice matched to GaAs and InP substrates. For example, $Al_xGa_{(1-x)}As$ is lattice match with GaAs irrespective of the specific mole fractions, whereas $In_xGa_{(1-x)}As$ and $In_xAl_{(1-x)}As$ are

lattice matched with InP only at a single fixed mole fraction (x ~0.52). An approximation of the ternary's lattice constant and energy band gap can be calculated using Vegard's Law [23, 24], where *x* is the mole fraction and *AZ* and *BZ* are the binary compound lattice constant and band gap values.

$$a_{alloy}=xAZ+(1-x)BZ \qquad \text{Equation 2-1}$$

The lattice constant and band-gap energy for GaAs and InP-based materials are tabulated in Table 2-2 [17, 25]. One can identify immediately the various energy gaps between those materials. Clearly, few pairs of semiconductors have a near-equal lattice constant.

Table 2-2 Lattice constant and band gap of common III-V binary and ternary compound semiconductors at 300 K [17, 25]

| **Alloy** | **Lattice constant, $a_0$ (Å)** | **Band gap, $E_g$ (eV)** |
|---|---|---|
| GaAs | 5.653 | 1.42 |
| AlAs | 5.660 | 2.16 |
| InAs | 6.058 | 0.37 |
| InP | 5.869 | 1.35 |
| $In_{0.53}Ga_{0.47}As$ | 5.869 | 0.76 |
| $In_{0.52}Al_{0.48}As$ | 5.869 | 1.48 |

For nearly equal lattice constant materials, the atoms at the hetero-interface have to slightly adjust their positions in order for them to conserve the geometry of the lattice. The adjustments of the atomic position will result in a small strain at the interface. The strain ($\varepsilon$) at the semiconductor interface is defined in Equation 2-2. Here, $a_L$ is the lattice constant for the overlay semiconductor and $a_S$ is the lattice constant of the baseline semiconductor.

$$\varepsilon = {(a_L - a_S)}/{a_S} \qquad \text{Equation 2-2}$$

However, when lattice matching is not adequate, this strain exceeds a certain critical value and therefore, the crystal lattice cannot hold the excessive force. This will then result in crystal dislocations. The crystal imperfections will propagate through many crystalline layers producing crystal dislocations in the lattice. These defects will invariably trap carriers, which will limit their mobility. They can also become recombination centres, which shorten the carriers' lifetimes. The overall effects result in very poor device properties.

Nevertheless, high quality crystal growth from two mismatched lattices can still be achieved with careful processing through advancements in crystal growth technologies such as MBE and MOCVD [26-28]. The strain can be tolerated by growing thin mismatched epitaxial layers on top of each other. However, as the strain energy increases with the thickness of the strained layer, the overlay layer must be grown below a critical thickness before dislocations can occur [29, 30]. This critical thickness ($h_c$) is defined as:

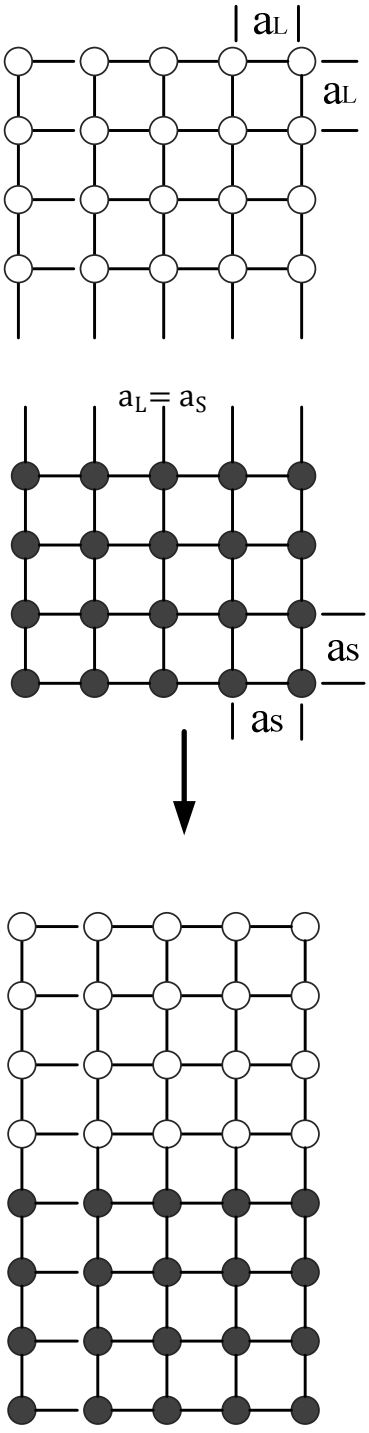
$$h_c = \frac{a_s}{2\varepsilon} \qquad \text{Equation 2-3}$$

To compensate for this difference, the resultant layer will be under strain. This new layer is known as 'pseudomorphic' since it is physically modified from the original crystal structure and consequently its physical properties are changed. This is beneficial in the manipulation of the semiconductors' mole fraction for combining either wider or narrower semiconductor materials. The significance of these material mixes will become clearer shortly.

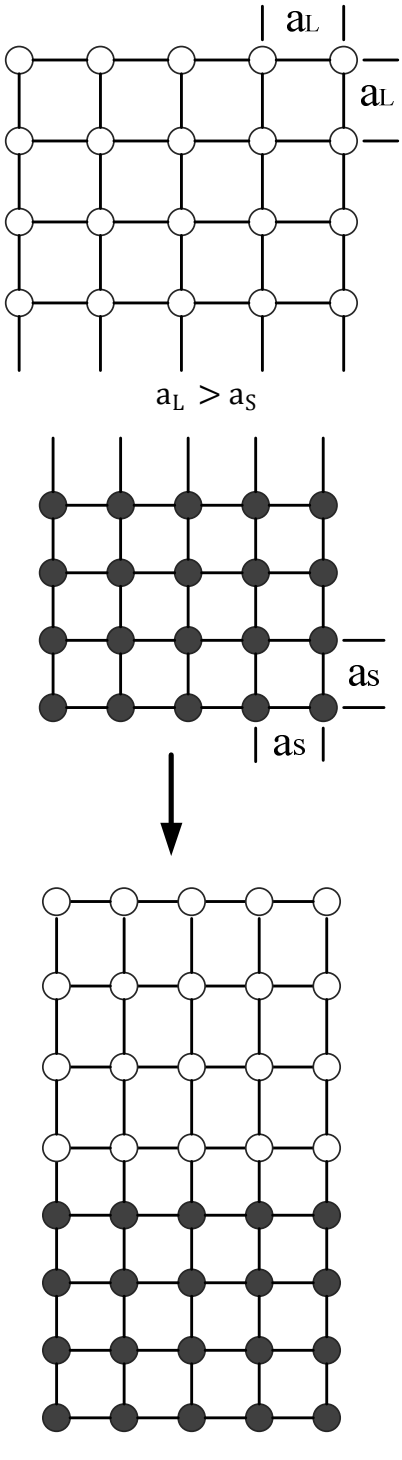
Figure 2-4 shows the crystal formation as above. In figure (a), $a_L$ is lattice matched with $a_S$, and hence the over-layer and base material atoms at the crystal interface are not required to adjust their positions relative to each other.

Figures (b) and (c) show the pseudomorphic crystal structure under compressive and tensile strains respectively. When $a_L$ is larger than $a_S$, the resultant relaxed material is under compressive strain whereas the atoms are under tensile strain when $a_L$ is smaller than $a_S$. Above the critical thickness, the excessive strain energy is released

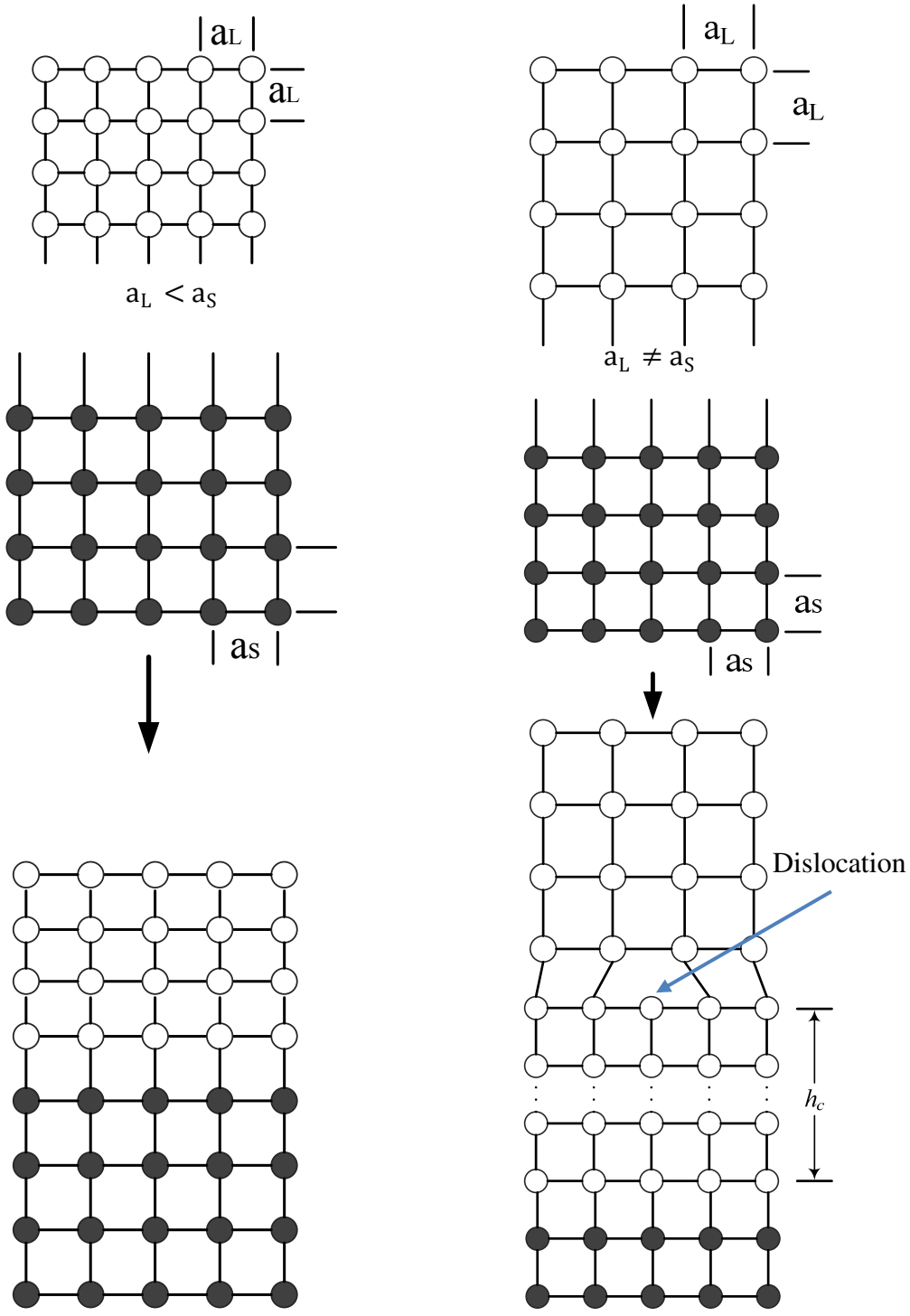
by the formation of dislocations where some of the bonds are missing or extra bonds appear. The resulting crystal defects are shown in figure (d).




(a) Lattice match




(b) Compressive Strain




(c) Tensile Strain

(d) Imperfection - dislocation

Figure 2-4 Conceptual formation of lattice match (a), pseudomorphic compressive strain (b), pseudomorphic tensile strain (c) and lattice mismatched with defects (d)

## 2.4 HIGH SPEED DEVICES

In previous sections, semiconductor materials suitable for high frequency applications have been identified, and the focus has primarily been on GaAs and InGaAs-InAlAs compounds from which high-speed devices have been realised. This section summarises the historical trend in high-speed devices beginning with a brief introduction of the device structure and high-speed limitations of the Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET). Next, the Metal Semiconductor Field Effect Transistor (MESFET), which over the years has been refined, resulting in devices that are more outstanding. Finally, the ultimate device in high frequency device applications, the High Electron Mobility Transistor (HEMT) is described.

In most semiconductor materials, the hole mobility is relatively poor when compared to that of the electron. For this reason, most high-speed devices use electrons as the charge carriers. Thus, the use of n-type channel in MOS (nMOS), and an electron-rich channel in MESFET and HEMT device architectures are required. These are the three terminal device that uses the induced electric field from a gate voltage to control the shape and consequently the conductivity in the channel. All of these devices are referred to Field Effect Transistors (FETs).

### 2.4.1 N-type Metal Oxide Semiconductor Field Effect Transistor (nMOS)

In an nMOS device (see Figure 2-5), the gate terminal is biased to a positive potential with respect to the p-type substrate. The positive charges at the gate terminal will repel the majority holes, and create a depletion region near the gate oxide surface. At the same time, some minority electrons are also attracted to the surface, but at low gate potentials, the accumulation of the electrons is not sufficient to cause current conduction.

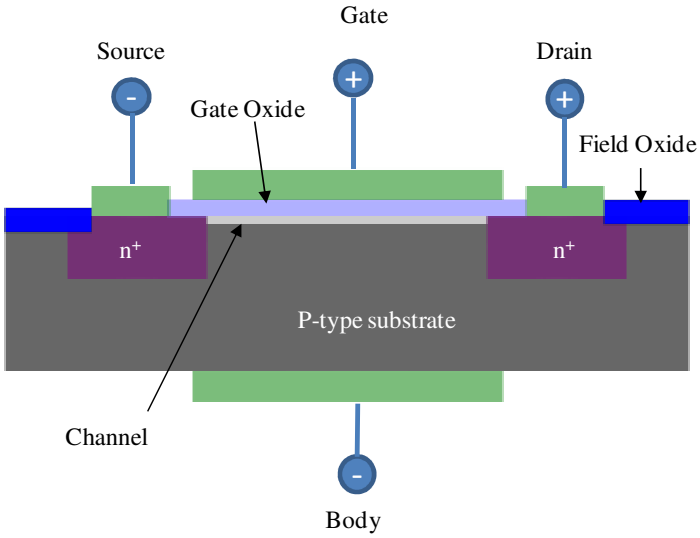



Figure 2-5 nMOS structure

As the gate voltage is increased, a dense inversion layer of electrons is formed under the oxide surface. When the gate potential reaches a threshold voltage ($V_{th}$), an inversion layer of electron-rich conduction channel will be formed and allow current conduction between the source and drain terminals of the MOSFET.

However, the low carrier mobility in Si inherently limits the device application in ultra high frequency operation. For this reason, and for micron-sized devices, the cut-off frequency of these devices is only in the order of 1 to 3 GHz [31]. Deeply scaled MOS devices (gate length of 35 nm or less) reach cut-off frequencies of ~200 to 300 GHz. That is the reason why the micron scale Si MOSFET is widely used in lower frequency electronic circuits.

Alternatively, high-speed material based MOSFET devices employing materials such as GaAs would be a very attractive solution. Unfortunately, these devices have proven so far to be very leaky and complex to design due to the lack of a high quality native oxide. Nevertheless, the use of $Ga_2O_3$ as the gate dielectric material has been reported as a promising high frequency enabler [32]. Therefore, circuit designers are investigating different types of stable materials and devices to suit their high-speed applications.

### 2.4.2 Metal Semiconductor Field Effect Transistor (MESFET)

In general, the device structure of the MESFET is similar to that of a Si based MOSFET. Rather than using an oxide layer as in a MOSFET, the gate metal in a MESFET gate lies directly on top of the semiconductor material (see Figure 2-6). Due to this configuration, an undesirable non-zero gate current might flow at the metal-semiconductor junction, which can be a restriction in the biasing of the device in certain applications.

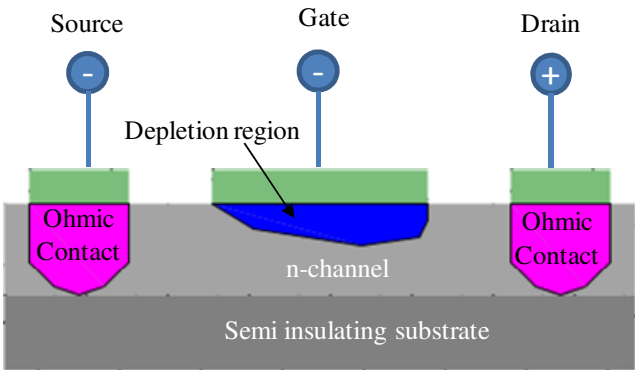



Figure 2-6 MESFET structure

For this reason, the MESFET's gate terminal is normally operated in reverse bias, where the $I_{GS}$ is limited to very small values. Here, the gate current is controlled by the Schottky contact that formed at the metal-semiconductor junction. Consequently, a depletion region or space charge region is formed beneath the gate terminal. The depletion region will constrict the current flow in the channel, which is already formed by the drain-source voltage. As the depletion region continues to grow through the application of an increasing negative gate voltage, the constricted channel will cause a decrease in drain-source current flow. As a result, the drain to source current in the channel is modulated by the applied voltage to the gate.

Compared to the MOSFET, the MESFET is a bulk type device where a high-speed material like GaAs is used as the substrate. As we shall see in the next section, this simple FET structure with a doped channel can be improved by the use of a heterostructure device structure with an undoped high mobility channel.

### 2.4.3 High Electron Mobility Transistor (HEMT)

Compared to the MESFET structure, there are two major advantages to the HEMT, which make the device superior in high-mobility, high-frequency applications. The foremost improvement is carrier confinement through the influence of the hetero-junction quantum well (QW) potential at the un-doped narrow-band gap material to form a high carrier mobility region termed 2-Dimensional Electron Gas (2-DEG) [33, 34].

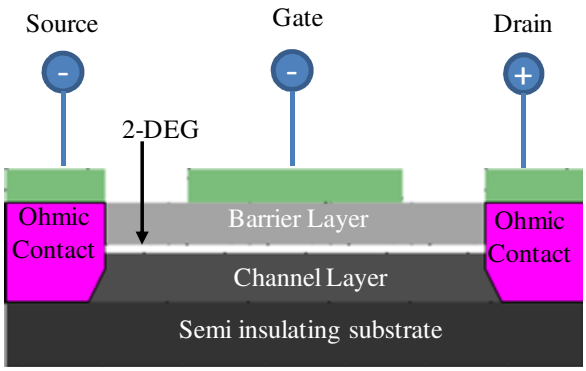



Figure 2-7 HEMT structure

The second improvement is that the carriers are physically separated from the dopant atoms at distances where the Columbic interaction between electron and donor due to the ionised impurities becomes extremely small. This is realised by using modulation doping or delta doping (δ-doping) in the Schottky barrier layer at several depths, separated by an undoped spacer layer between the doping layer and the channel.

Therefore, un-distracted electrons can move freely, thanks to a much reduced number of scattering events with the dopant atoms. Due to this effect, the device's noise performance can be improved because the undesired scattering event of the carriers can be significantly reduced. The occurrence of random and unpredictable scattering events is the cause of noise [16].

In terms of the current control mechanism, the HEMT devices share the same device operational principles with the MESFET. The only difference to other devices is the very close proximity of the gate to the 2-DEG channel. Figure 2-8 summarises the high-speed performance of different devices.

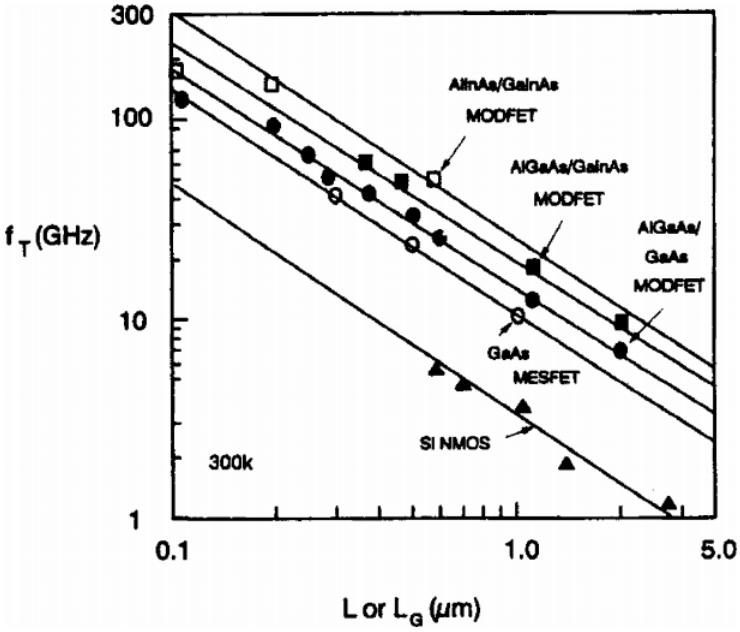



Figure 2-8 Comparison of $f_T$ versus gate length ($L_G$) of several III-V MESFET and MODFET devices with Si nMOS devices [35]

Improvements in advanced carrier transport properties and reductions in gate leakage have resulted in the pseudomorphic HEMT (pHEMT). These devices are very similar to regular HEMTs, except that the channels are made from pseudomorphic materials [36]. Advances in crystal growth and band-gap engineering have allowed these improved properties to be fully realised, and a new variant of this device will be the main discussion in this thesis.

## 2.5 LOW NOISE DEVICE

In designing a high frequency circuit with low noise characteristics, the pHEMT is known to be the most suitable choice. In FETs the noise is mainly generated from the variation of the carrier speed in the device's channel. The random motion of carriers produces variation in current, resulting in noise [37].

By reducing the source and drain resistances ($R_S$ and $R_D$) together with increasing the current gain cutoff frequency ($f_T$), the desired low noise performance ($F_{min}$) can be obtained (Equation 2-4). Maximum transconductance ($g_m$) and minimum gate capacitance ($C_{GS}$) can be achieved by improving the device's design. Proper biasing is the other design necessity to achieve low noise performance (Equation 2-5) [37].

$$F_{min} = 1 + K_f \frac{f}{f_T} \sqrt{g_m (R_S + R_G)} \qquad \text{Equation 2-4}$$

$K_f$ is Fukui's noise figure coefficient.

$$f_T = \frac{g_m}{2\pi (C_{GS} + C_{GD})} \qquad \text{Equation 2-5}$$

Generally, the minimum noise ($NF_{min}$ = 10 log $F_{min}$ in dB) is obtained under low operating source-drain current conditions ($I_{DS}$ ~ $I_{dss}$/10), where $I_{dss}$ is the source-drain current at zero bias. For low noise applications however, there are major differences between the bias range of MESFET and HEMT devices. For a HEMT, $NF_{min}$ can be achieved in a wider $I_{DS}$ range compared to a MESFET. This preferable because larger bias margins can be used in designing Low Noise Amplifier circuits. However, biasing for maximum gain and biasing for low $NF_{min}$ does not always coincide, therefore there is a trade-off between gain and noise. Nevertheless, in the HEMT this effect is significantly reduced due to the wider range of $NF_{min}$ biasing. High gain devices also require epitaxial design with a buffer layer below the channel in order to minimise the carrier injection and reduce the output conductance.

When compared to GaAs, InP-based HEMTs offer the promise of improved low noise operation. The noise performance over frequency of various devices is shown in Figure 2-9. It can be observed that the lattice matched or pseudomorphic InP-based HEMTs operate up to millimetre-wave frequencies where a Noise Figure (*NF*) of 1.2 dB has been demonstrated at 94 GHz [37].

In summary, InP based pHEMTs are the best devices developed so far for high-frequency low noise applications. However, when compared to the leading GaAs technology, InP materials are more expensive, more brittle and the available wafers are smaller in diameter. Nevertheless, the potential future applications, especially in

ultra high speed wireless and satellite communication still makes this a viable material for the future.

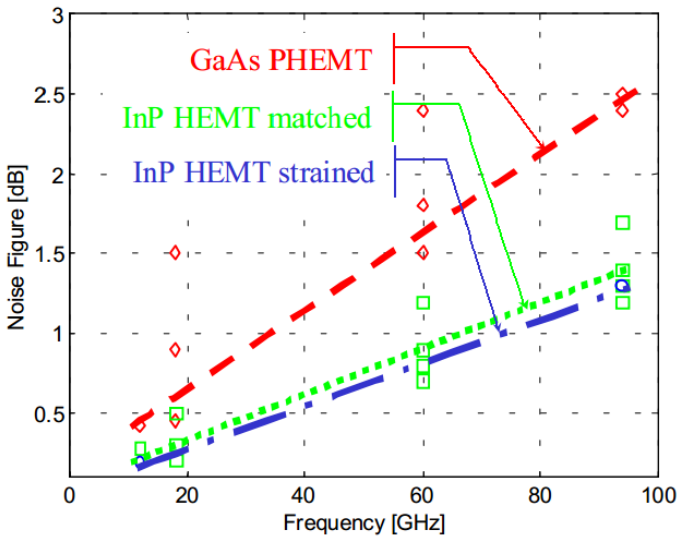



Figure 2-9 Summary of noise performance for GaAs- and InP-based HEMTs as a function of operating frequency [37]

## 2.6 EPITAXIAL STRUCTURES AND ENERGY BAND DIAGRAM OF THE pHEMT

As briefly explained in the previous section, in high frequency applications it is essential for the carrier to move freely without significant collisions with the lattice and impurities in the channel. The device high frequency performance is therefore closely dependent on the carrier velocity (which is the electron carrier velocity for n-type devices). The electron drift velocity ($v_n$) is given by:

$$v_n = -\mu_n \epsilon \qquad \text{Equation 2-6}$$

Where $\mu_n$ is the electron mobility, $\epsilon$ is the electric field and the minus sign denotes that the electrons drift in the opposite direction to $\epsilon$. The mobility $\mu_n$, is proportional to the electron mean free time, $\tau_c$ where:

$$\mu_n = \frac{q\tau_c}{m_n} \qquad \text{Equation 2-7}$$

$m_n$ is the electron effective mass and $\tau_c$ is the average time between collisions. Since the electrons move randomly and collide with lattice atoms, impurity atoms and other scattering centres, Equation 2-6 and Equation 2-7 show that the drift velocity will be high if the electron collision with impurities is minimised.

In Equation 2-8, the probability of collisions taking place in unit time $\frac{1}{\tau_c}$ is equal to the sum of probabilities of scattering due to the lattice ($\frac{1}{\tau_{c,lattice}}$) and scattering due to impurities ($\frac{1}{\tau_{c,impurity}}$).

$$\frac{1}{\tau_c} = \frac{1}{\tau_{c,lattice}} + \frac{1}{\tau_{c,impurity}} \qquad \text{Equation 2-8}$$

As shown in Figure 2-2, InP-based materials have superior properties in terms of carrier drift, and the scattering events in pHEMT devices are the lowest among FET devices. Therefore, this chapter will only focus on InP-based pHEMT characteristics.

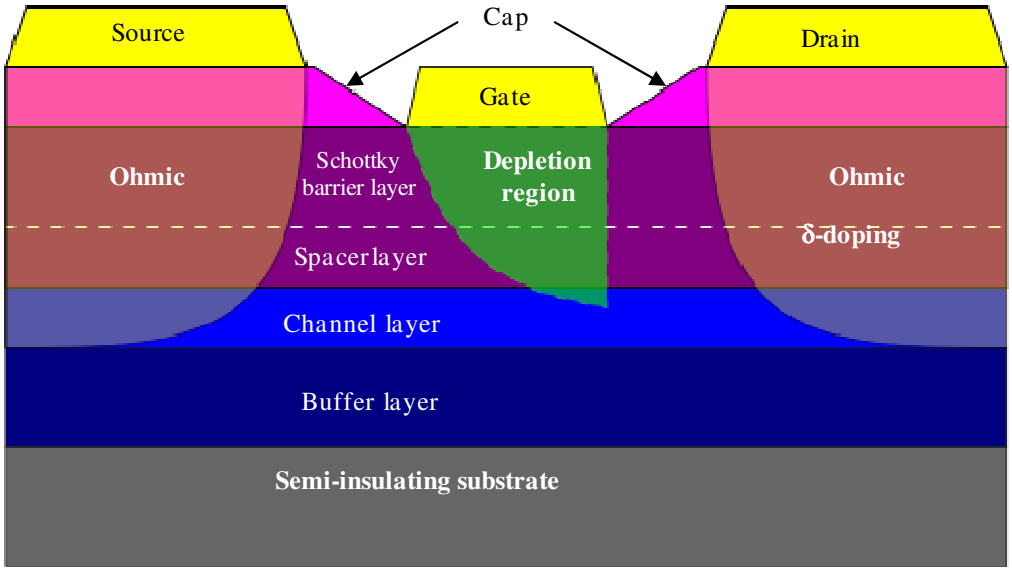



Figure 2-10 Epitaxial structure for InP-based pHEMT

Figure 2-10 illustrates a typical epitaxial structure of an InP-based pHEMT. From this illustration, several key parameters can be highlighted, such as the metal-semiconductor contact type and the formation of the 2-DEG.

### 2.6.1 Metal-Semiconductor Contact

In pHEMT devices there are two types of metal-semiconductor contact that control the current conduction and current modulation mechanism in the channel. The Ohmic contact plays an important role in lossless current conduction between the Source-Drain terminals, whilst the Schottky contact modulates the current flow between these terminals.

An Ohmic contact should have negligible contact resistance and allow current to flow in accordance with linear I-V characteristics. This kind of contact does not control the current flow but provides a low electrical resistance path to the outside world. This means that such contacts can pass current with minimal current loss relative to the voltage drop across the device.

In semiconductor processing, there are two ways in achieving a good Ohmic contact: either by high semiconductor doping layer or through a low Schottky barrier height at metal-semiconductor junction.

At any metal-semiconductor contact, there always exists a Schottky barrier [38]. The carriers must overcome this barrier in order to travel between the metal and semiconductor sides. When the semiconductor is heavily doped ($N_D \geq 10^{19}$ cm$^{-3}$), the depletion width and consequently the barrier width near the metal-semiconductor contact will be reduced. As the depletion width becomes sufficiently narrow, electrons can overcome this barrier and tunnel through it via the mechanism of Thermionic Field Emission (TFE) [39].

Alternatively, the barrier height is reduced by means of a low energy gap material at the semiconductor side. Here, the electrons have energies larger than the potential barrier and Thermionic Emission (TE) takes place by electrons moving over the barrier [35].

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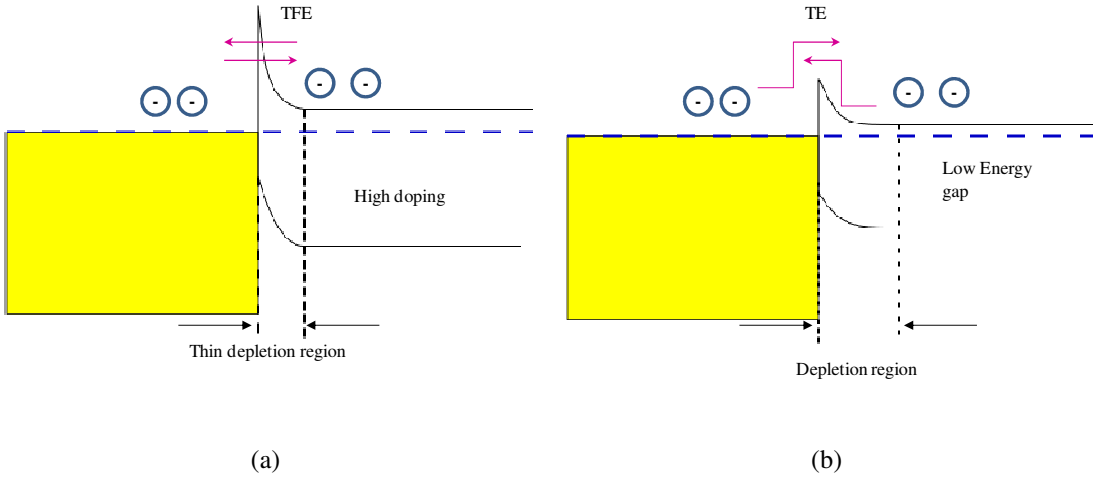



Figure 2-11 Current conduction at Ohmic contact (a) via TFE in highly doped semiconductor and (b) via TE at low Schottky barrier interface [35]

In practice, Ohmic contacts can be divided into non-alloyed and alloyed Ohmic contact schemes. A non-alloyed Ohmic contact is formed by depositing a metal onto a highly doped semiconductor cap layer in the pHEMT device. As shown in Figure 2-11 (a), the thickness of the depletion region is reduced, allowing the carrier to easily tunnel through the barrier. It provides several advantages including faster processing and less damage to the device during the heat treatment steps.

In the case of alloyed contacts, metals containing dopants (e.g. AuGe) are deposited onto the cap layer and subject further for heat treatment process. During the heat treatment process, the dopants diffuse into the semiconductor, forming a heavily doped region under the metal. Carrier tunnelling will then occur with a reduced depletion width under the contact.

A Schottky contact is a rectifying contact, which has a non-linear current characteristic at applied forward and reverse voltages. Typically, it is used for the gate metal contact in the pHEMT device. A Schottky contact is formed when a metal is brought in contact with a lightly doped semiconductor. Figure 2-12 illustrates the formation of a Schottky contact when a metal and a semiconductor with n-type doping come into contact [40].

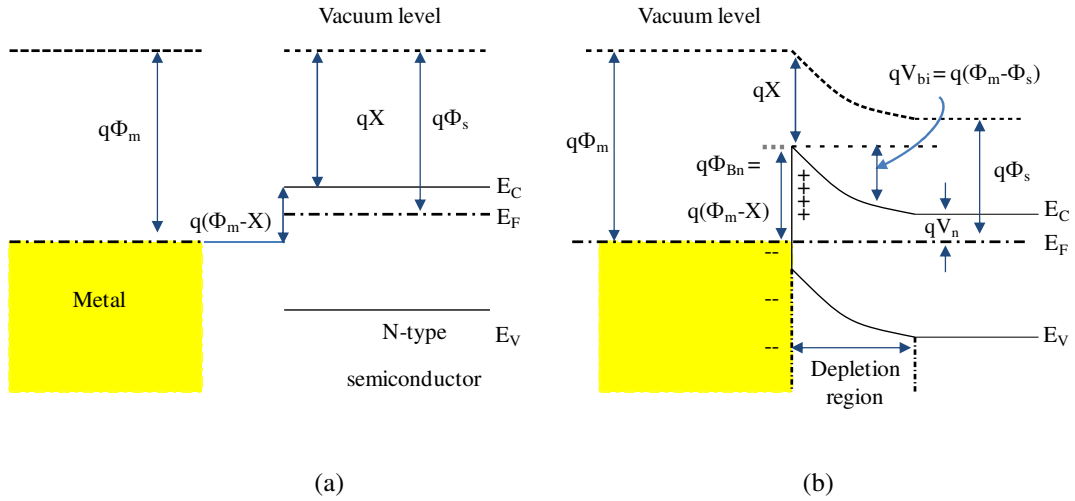



Figure 2-12 Formation of Schottky contact before (a) and after contact (b) [40]

In Figure 2-12(a), $\Phi_m$ and $\Phi_S$ are the work functions of the metal and semiconductor respectively, X is the semiconductor electron affinity and $q\Phi_n$ (n denotes n-type doping) is the difference between the conduction band and Fermi level on the semiconductor side, and $E_C$, $E_F$ and $E_V$ are the Conduction band, Fermi and Valence band energy levels, respectively [38].

When the metal and semiconductor are brought into contact, the Fermi level of the semiconductor will align itself to the metal and thermal equilibrium is established. This will result in the flow of electrons from the semiconductor to metal conduction band, leaving positively charged ionised donors in the triangular-shaped region. Consequently, band bending will occur as depicted in Figure 2-12. This triangular-shaped region is called a depletion region.

The existence of a dipole layer of charges at the contact interface will establish an electric field from the semiconductor to the metal. Schottky barrier ($q\Phi_{Bn}$), is therefore built at the metal to semiconductor junction. The Schottky barrier will prevent further movement of electrons from metal to semiconductor. The potential barrier is given by:

$$q\Phi_{Bn} = q\Phi_m - qX \qquad \text{Equation 2-9}$$

Conversely, electrons travelling from semiconductor to metal will have to overcome a build-in potential ($qV_{Bi}$) seen from the semiconductor side. This is given as a difference between metal and semiconductor work functions as shown in Equation 2-10, or can be rewritten as a function of potential barriers as shown in Equation 2-11.

$$qV_{Bi} = q\Phi_m - q\Phi_S \quad \text{Equation 2-10}$$

$$qV_{Bi} = q\Phi_{Bn} - qV_n \quad \text{Equation 2-11}$$

The magnitude of $V_{Bi}$ is proportional to the amount of current, which can flow through the metal to semiconductor contact while the magnitude of $\Phi_{Bn}$ is related to the amount of current flow in the reverse direction.

$V_{Bi}$ is greatly dependent on the difference between $\Phi_m$ and $\Phi_S$. This is the fundamental difference between Ohmic and Schottky contacts as shown in Figure 2-12, where when $\Phi_m > \Phi_S$, the contact becomes a Schottky contact and vice versa.

### 2.6.2 Band Discontinuities

Figure 2-13 shows a typical band diagram of a heterojunction. In this figure, energy band discontinuities occur when two semiconductor materials with different energy gaps are brought together at thermal equilibrium [41, 42]. Figure 2-13 (b) illustrates the resulting adjustments of the energy band diagrams when a high band gap material is in contact with a low band gap material.

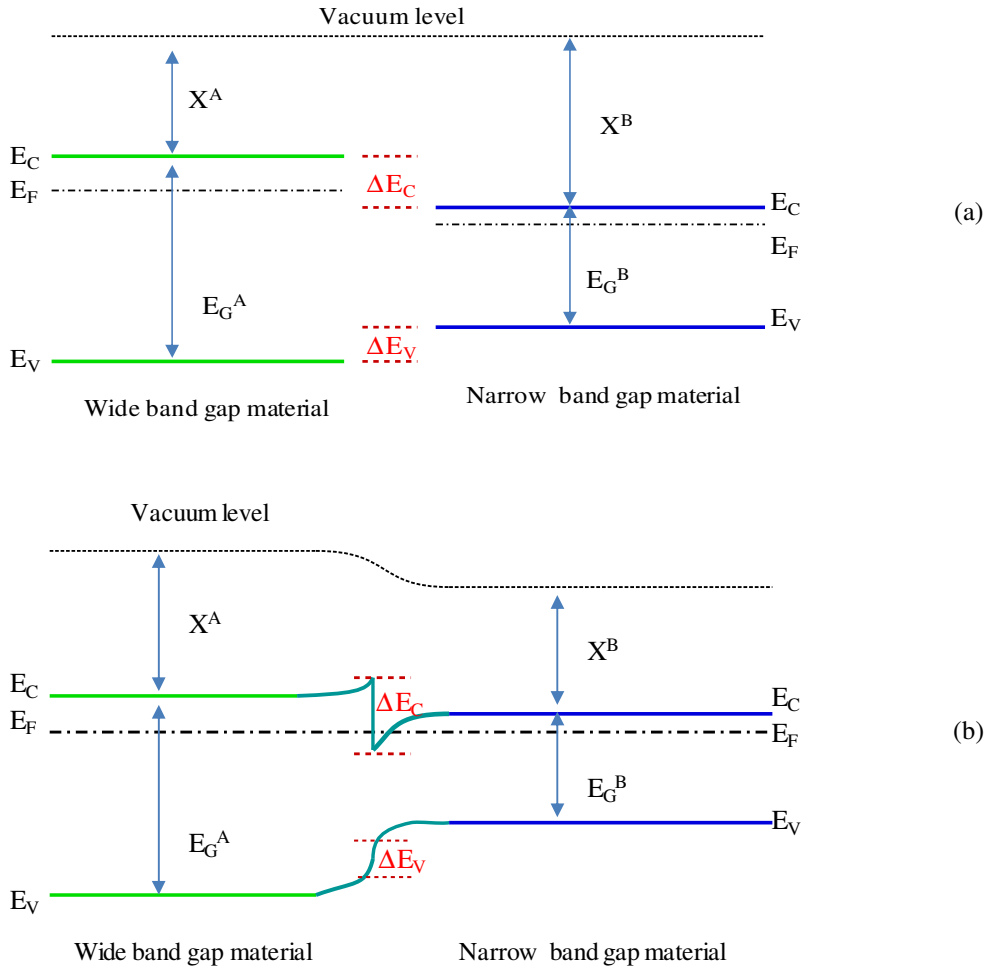



Figure 2-13 Energy band diagrams of wide and narrow band gap materials; (a) before and (b) after contact [43]

In the diagram, $E_C$, $E_F$ and $E_V$ are the conduction band, Fermi and valence band energy levels for material A (high band gap) and B (low band gap) respectively, $X^A$ and $X^B$ are the electron affinity from the bottom of the conduction band to the vacuum level, $E_G^A$ and $E_G^B$ are the energy band gap for material A and B respectively, and $\Delta E_C$ and $\Delta E_V$ are the band discontinuity in the conduction band and valence band respectively.

When thermal equilibrium is established between the two semiconductors, energy band discontinuities are created on both the conduction and valence bands due to the difference in their energy band gap $\Delta E_G$. The degree of the discontinuities is given by Equation 2-12 and Equation 2-13 respectively.

$$\Delta E_G = E_G^A - E_G^B \quad \text{Equation 2-12}$$

$$\Delta E_G = \Delta E_C + \Delta E_V \quad \text{Equation 2-13}$$

To some extent, $\Delta E_G$ can be engineered to achieve numerous amounts of junction discontinuities. A larger $\Delta E_C$ will lead to better carrier confinement and therefore a higher carrier concentration at the 2-DEG interface. The InAlAs/InGaAs/InP material system has many significant advantages over the AlGaAs/GaAs and even pseudomorphic AlGaAs/InGaAs/GaAs material systems. The $\Delta E_C$ between $In_{0.52}Al_{0.48}As$ and $In_{0.53}Ga_{0.47}As$ layer in lattice matched InAlAs/InGaAs/InP material system is greater than 0.50 eV. This is higher than the $\Delta E_C$ between $Al_{0.2}Ga_{0.8}As$ and $In_{0.15}Ga_{0.85}As$ layer in the pseudomorphic $Al_{0.2}Ga_{0.8}As/In_{0.15}Ga_{0.85}As/GaAs$ material system where its value is only 0.30 eV, and even lower for $Al_{0.30}Ga_{0.70}As$ and GaAs material system where the $\Delta E_C$ is only 0.24 eV [16]. This property therefore makes $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As/InP$ an extremely attractive and suitable candidate for high-speed devices where greater flexibility over carrier control at the junction.

### 2.6.3 Quantum Well and 2-DEG

Figure 2-14 illustrates an example of the conduction band diagram of a simple AlGaAs/GaAs heterojunction epitaxial structure.

In Figure 2-14, AlGaAs is the wide band-gap material grown on top of a lower band-gap GaAs layer. A triangular quantum well (QW) is formed due to the differences in energy gaps between them. The free electrons are introduced by doping the wide band-gap AlGaAs supply layer. In this case, the electrons flow from the wide band-gap supply layer into the narrow gap channel, thereby resulting in the accumulation of electrons in the potential well created at the heterojunction.

As shown in the same figure, the energy level of donors in the supply layer is higher than the Fermi energy level ($E_F$) which means that electrons are free to move into the QW. In addition, the lowest quantised energy level ($E_0$) is lower than $E_F$ and electrons will be trapped inside the QW.

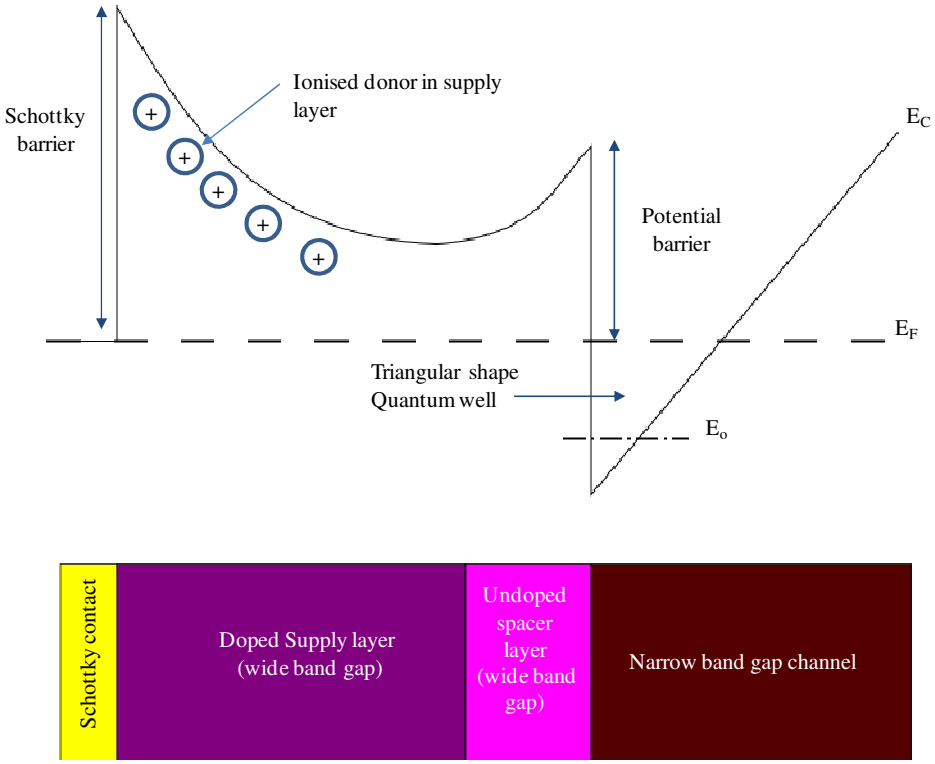



Figure 2-14 Formation of Quantum Well at in AlGaAs/GaAs hetero-junction

Furthermore, the resultant band structure only allows the electrons to move freely in the plane parallel to the un-doped junction, and the absence of ionised donors from the supply layer will greatly increase the carrier mobility in this region.

### 2.6.4 δ-doped versus Bulk Doped Layers

The doped layers used in the previous section are the bulk-doped type, where the impurities are incorporated all the way through the whole of the supply layer. An alternative and improved type of doping, known as δ-doping, has replaced traditional bulk-doping [44] method.

The δ-doping method is also referred to planar, pulse, atomic layer, or spike doping. It consists of a high doping semiconductor ($N_D$ > 5 x $10^{12}$ $cm^{-2}$) layer on a single-atomic plane. Figure 2-15 depicts the energy band diagrams and quantum wells between δ-doped and bulk-doped structures.

By referring to δ-doped energy band diagram in Figure 2-15, $E_1^{\delta}$ is the quantised energy in the δ-doped region, whereas $E_1$ is the quantised energy in the quantum well. When $E_1^{\delta}$ is below the $E_F$, a parallel conductive channel is formed in the supply layer. If it is not fully depleted by the built-in and the applied voltages, this parallel channel will become an undesired portion of the 2-DEG. Similarly, in bulk-doped structure, the parallel conduction will occur if the conduction band minimum in supply layer is lower than $E_F$.

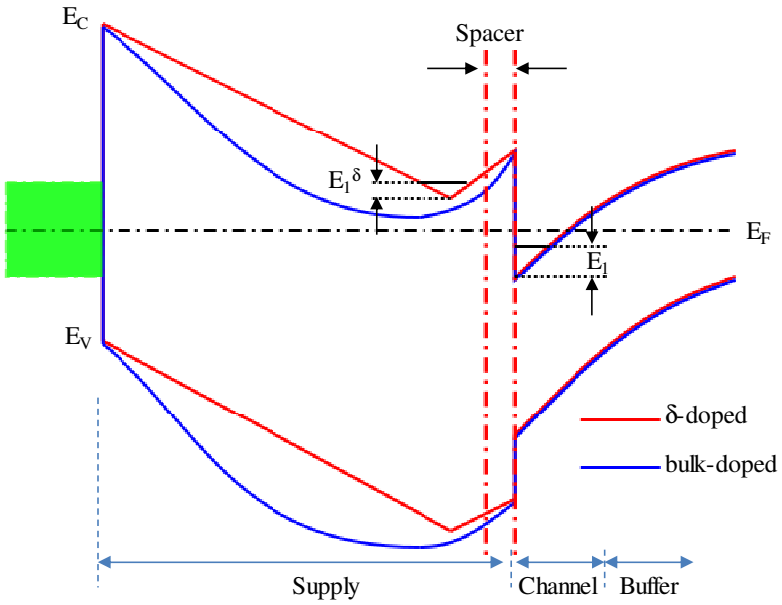



Figure 2-15 Band diagram and quantised carriers between δ-doped and bulk-doped heterostructures resulting similar 2-DEG carrier densities [44]

Figure 2-15 also shows band bending for both δ-doped and bulk-doped structures that resulting in similar carrier concentration in the channel. As compared to δ-doped structure, the same carrier concentration in the channel is achieved at higher doping concentration in bulk-doping structure. In other words, as compared to bulk-doping levels, the δ-doping technique could provide similar 2-DEG carrier densities, despite the use of less dopants. This will cause the conduction band minima to increase in δ-doled layer and eventually avoiding the unwanted parallel conduction.

The high carrier concentration in the δ-doped epilayer can be seen as the carriers are able to climb the slope easily on the thin spacer, as the result of the absence of the

potential drop in the depletion layer, which exists in bulk doping. The electron in a δ-doped layer can also now tunnel through the thin spacer layer and get trapped in the potential well, which results in higher carrier concentration in the QW. All these benefits make the δ-doped structure as the key design in HEMT-based devices.

## 2.7 PRINCIPLE OF OPERATION

In describing the device operation, two important terms, the pinch-off voltage ($V_p$) and the threshold voltage ($V_{th}$), need to be explained.

The pinch-off voltage is the gate voltage that is required to fully deplete the bulk doped supply layer of thickness $d_1$ and is expressed as in Equation 2-14 [41].

$$V_{p,bulk} = \frac{qN_D {d_1}^2}{2\varepsilon_0\varepsilon_s} \qquad \text{Equation 2-14}$$

Where q is the electron charge, $N_D$ is the donor concentration and $\varepsilon_0\varepsilon_s$ is the relative permittivity of supply layer.

Similarly, $V_{p,\delta}$ is the voltage for which all the electrons in the δ-doped layer are transferred to the quantum well:

$$V_{p,\delta} = \frac{qn_\delta d^*}{2\varepsilon_0\varepsilon_s} \qquad \text{Equation 2-15}$$

Here, where $n_\delta$ is the 2 dimensional δ-layer doping concentration and $d^*$ is the distance from the gate metal to the δ-doped layer.

The threshold voltage ($V_{th}$) is the gate voltage where current conduction between source and drain is just starting in the channel. In other words, this is the point that determines the device's ON/OFF behaviour:

$$V_{th} = \Phi_{Bn} - \frac{\Delta E_C}{q} - V_P \qquad \text{Equation 2-16}$$

From Equation 2-16, $V_{th}$ can be adjusted by using different values of $V_P$ and $\Phi_{Bn}$, where $\Delta E_C$ is usually fixed for a given set of semiconductors. For a depletion mode (normally "ON") device where the channel already exists at $V_G$ = 0 V, $V_{th}$ will be negative. In the case of an enhancement mode (normally "OFF") device, $V_{th}$ is normally positive

When the gate voltage is higher than $V_{th}$, the sheet carrier density ($n_s$) in 2-DEG is determined as Equation 2-17 [41]:

$$n_s(x) = \frac{C_i[V_{GS} - V_{th} - V_{DS}(x)]}{q} \qquad \text{Equation 2-17}$$

Where $x$ is an arbitrary point along the channel and $V_{DS}(x)$ is the applied drain-source voltage along the channel. Here, at source (side $x$ = 0) $V_{DS}(x)$ is equal to 0 V and when $x = L_g$, $V_{DS}(x)$ is equal to applied voltage at drain side. Meanwhile, $V_{GS}$ is the applied gate-source voltage and $C_i$ is the gate channel capacitance and is given by Equation 2-18:

$$C_i = \frac{\varepsilon_0 \varepsilon_s}{d_1 + d_2 + d_3} \qquad \text{Equation 2-18}$$

Here, $d1$, $d_2$ and $d_3$ are the channel, supply layer and spacer thicknesses respectively.

Therefore the induced drain-source current $I_{DS}$ for a pHEMT transistor with a gate length $L_G$ and gate width $W$ is given by Equation 2-19.

$$I_{DS} = \frac{W}{L_G}\mu_n C_i \left[(V_{GS} - V_{th})V_{DS} - \frac{{V_{DS}}^2}{2}\right] \qquad \text{Equation 2-19}$$

Where $\mu_n$ is the 2-DEG carrier mobility.

At small $V_{DS}$ where $V_{DS} << (V_G\text{-}V_{TH})$, the second part in the bracket ( $\frac{{V_{DS}}^2}{2}$) can be ignored and Equation 2-19 can be simplified to:

$$I_{DS} = \frac{W}{L_G}\mu_n C_i (V_{GS} - V_{th})V_{DS} \qquad \text{Equation 2-20}$$

Equation 2-20 shows that $I_{DS}$ is linear with $V_{DS}$ and therefore this region is called the linear region.

The corresponding channel resistance in the linear region ($R_{linear}$) is given as below:

$$R_{linear} = \frac{L_g}{W\mu_n C_i} * \frac{1}{V_{GS} - V_{th}} = \frac{\Delta V_{DS}}{\Delta I_{DS}} \quad \text{Equation 2-21}$$

As $V_{DS}$ increases further, the depletion region will be asymmetrical and larger at the drain side compared to the source, due to the high reverse bias at the gate-drain terminal. At the point where $V_{DS} = V_{GS} - V_{th}$ , the saturated drain-source voltage ($V_{DS\_\ sat}$) is reached, and so the electric field at the drain side will increase rapidly and start to deplete the channel (pinch-off point).

Starting from this point, an increase in $V_{DS}$ will only lead to a small increase in $I_{DS}$, and the carrier velocity is saturated ($v_{sat}$). This region is called the saturation region where $I_{DS}$ is now changed to [35]:

$$I_{DS} = \frac{W}{L_G}\mu_n C_i (V_{GS} - V_{th})^2 \quad \text{Equation 2-22}$$

Figure 2-16 shows the typical I-V characteristics of a HEMT device.

The transconductance $g_m$, is defined as the change in drain-source current $I_{DS}$, with a change in gate-source voltage $V_{GS}$, for a fixed drain-source voltage $V_{DS}$. For high $g_m$, a small change in $V_{GS}$ results a large change in $I_{DS}$.

$$g_m = \left.\frac{\partial I_{DS}}{\partial V_{GS}}\right|_{V_{DS}=\text{constant}} \quad \text{Equation 2-23}$$

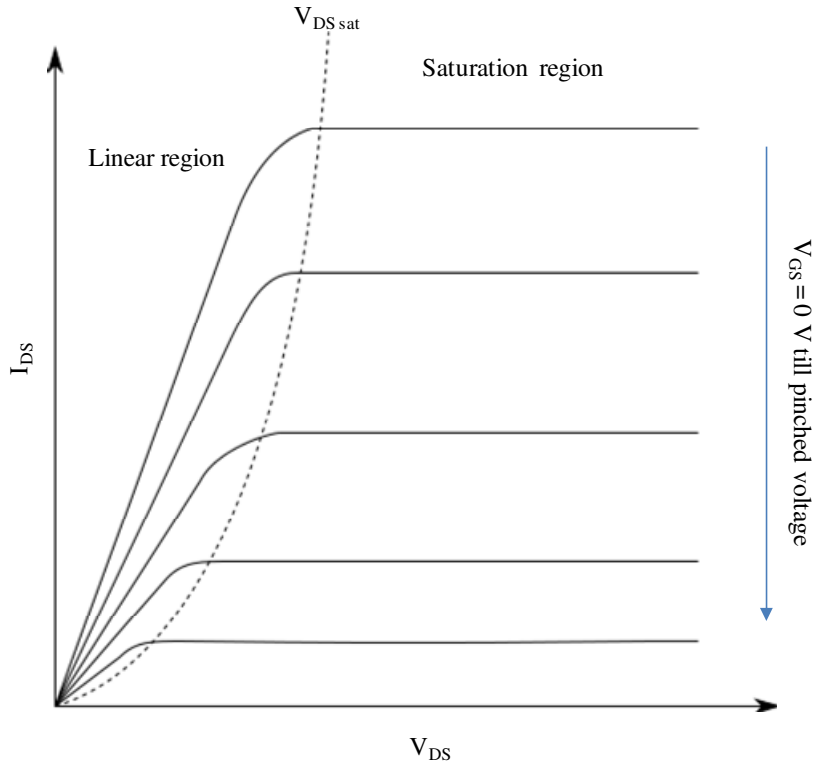



Figure 2-16 Typical HEMT I-V Characteristic

Consequently, $g_m$ in the linear and saturation regions, derived from Equation 2-20 and Equation 2-22 respectively is given below:

$$g_{m\ ,linear} = \frac{W\mu_n C_i V_{DS}}{L_G} \qquad \text{Equation 2-24}$$

$$g_{m,\ saturation} = \frac{W\mu_n C_i (V_{GS} - V_{th})}{L_G} \qquad \text{Equation 2-25}$$

An important parameter in high frequency applications is the cut off frequency or unity current gain frequency $f_T$. It is defined as the frequency at which the device current gain is equal to 1. Referring to the small signal equivalent circuit, one can derive the expression for current gain as shown in Equation 2-26.

$$\left|\frac{i_{out}}{i_{in}}\right| = \left|\frac{g_m}{j\omega(C_{gd} + C_{gs})}\right| = 1$$

Thus, $$\frac{g_m}{\omega(C_{GD} + C_{\mathrm{GS}})} = 1 \qquad \text{where } \omega = 2\pi f_T$$

Therefore, $$f_T = \frac{g_m}{2\pi(C_{GD} + C_{\mathrm{GS}})}$$ Equation 2-26

$C_{GD}$ and $C_{\mathrm{GS}}$ are the gate-drain and gate-source capacitances respectively.

$f_T$ can also be viewed as the transit time ($\tau_C$) for an electron to cross the channel under the gate ($L_G$):

$$\tau_c = \frac{1}{2\pi f_T}$$

Thus, $$f_T = \frac{1}{2\pi\tau_c}$$

But, $$v_{sat} = \frac{L_G}{\tau_c}$$

And hence $$f_T = \frac{v_{sat}}{2\pi L_G}$$ Equation 2-27

Therefore, to improve $f_T$, one should consider a semiconductor with high $g_m$, low parasitic capacitance, high $v_{sat}$ and of course shorter $L_G$.

Another figure of merit is the maximum oscillation frequency, $f_{max}$. It is also known as the frequency where power gain is equal to "1" (or 0 dB). It is the maximum frequency before the device becomes unstable and prone to oscillation [35]:

$$f_{max} = \frac{f_T}{2\sqrt{\frac{R_G + R_{ch} + R_S}{R_{DS}} + 2f_T R_G C_{GD}}}$$ Equation 2-28

This relationship shows that the parasitic resistances ($R_G$, $R_{ch}$, $R_{DS}$ and $R_s$) together with the gate-drain capacitance ($C_{GD}$) strongly affect the value of $f_{max}$.

## 2.8 DEVICE CHARACTERISATION

Throughout the research activities, all devices were characterised by their DC and small signal RF measurements.

### 2.8.1 DC Characteristics

In our facility, the DC characteristic measurement set-up consists of a probe station and a HP4142 Semiconductor Parameter Analyser, which is connected to the workstation and controlled by the Agilent's Integrated Circuit Characterisation and Analysis Program (IC-CAP) software. In this work, the current-voltage measurement is employed for the measurement and analysis of Ohmic contact, Schottky diode characteristic, device's leakage current and the device's I-V output characteristics.

### 2.8.2 RF Characteristics

In this study, the small signal RF measurement set-up composed of a probe station fitted with two Ground-Signal-Ground RF probes, HP8510C Vector Network Analyser (VNA) and a HP4142 Semiconductor Parameter Analyser. Again, the communication among these equipments is controlled by IC-CAP software.

The small-signal characterisation of an active device is carried out by measuring the small-signal Scattering-parameters (S-parameters) measured at their input and output terminals of a two-ports network. The S-parameters are widely used for the characterisation of transistors at microwave frequencies because S-parameters can easily be determined from the measured ratios of the incident and reflected power waves using the network analyser. The measurement of these coefficients only requires termination of the Device Under Test (DUT) with the characteristic impedance of the measurement system, which is equal to 50 Ω.

In order to perform accurate RF characterisation of on-wafer devices, the Impedance Standard Substrate (ISS) provided by Cascade Microtech is used for calibration. This is to remove the effect of connecting cables, define the measurement reference plane to the probe tips and remove measurement errors from, for instance, coupling

between the ports. The Short-Open-Load-Thru (SOLT) calibration technique was used in this work by running the Cascade Microtech WinCal calibration software. Then the error terms were calculated and saved in the network analyser.

Then, the small signal characteristics can be obtained by measuring the device at any given bias point and under small-signal conditions (input power of -20dBm). Here, the magnitude and phase of the S-parameters of a transistor are measured as a function of frequency from 40 MHz to 40 GHz.

## 2.9 PARAMETER EXTRACTION

Throughout the fabrication process, several device characteristics were extracted at various processing steps stages to determine the quality of the device.

### 2.9.1 Transfer Length Method

The Transfer Length Method (TLM) was developed independently by Berger [45], Murrman and Widmann [46]. They have developed a test structure that solved the problem of measurement to determine the specific contact resistance ($R_C$). The resistance between two TLM pads separated by distance d is shown in Figure 2-17.

From the figure, the total resistance, $R_T$ between the two contacts is:

$$R_T = 2R_a + R_b \qquad \text{Equation 2-29}$$

Where $R_a$ is the resistance below the contact and $R_b$ is the resistance in the semiconductor between the contacts. Also shown in the figure are the effective contact length ($L_T$) and the contact width ($W$). In general, the relationships between resistivity ($R$) length ($L$), width ($W$), and thickness ($t$) are as follows:

$$R = \rho \frac{L}{A} = \rho \frac{L}{W * t} = \frac{\rho}{t} * \frac{L}{W} = R_s \frac{L}{W} \qquad \text{Equation 2-30}$$

Where $\rho$ is the material resistivity (in Ω.m) and $R_s$ is the sheet resistance (in Ω/ ).

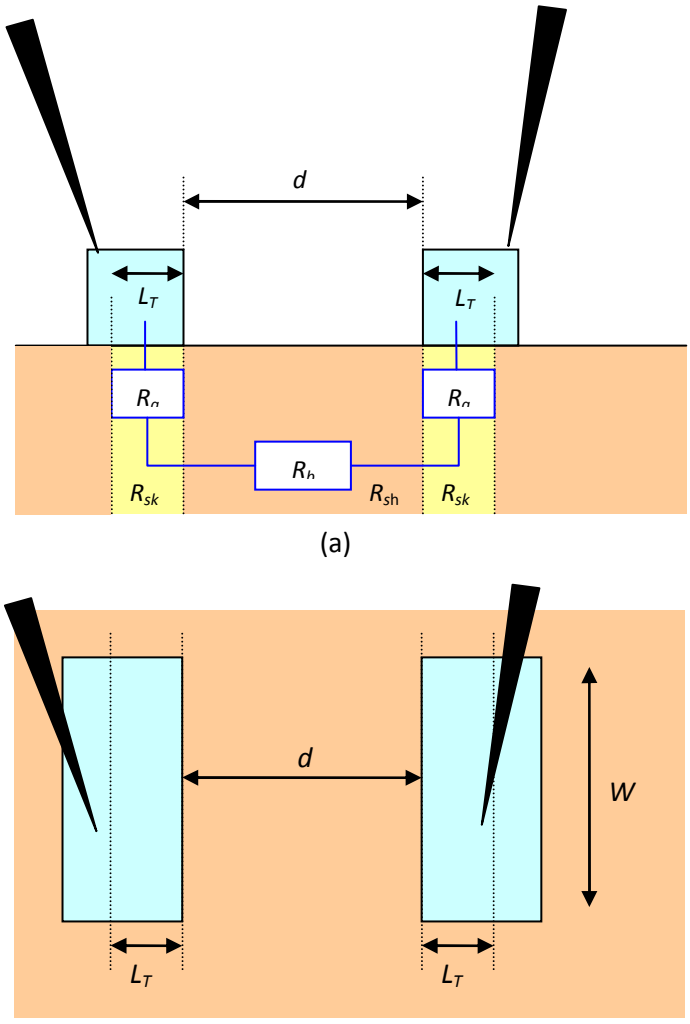



Figure 2-17 Theory behind TLM structures; (a) side view, and (b) top view

At a metal-semiconductor contact, there are two types of sheet resistances; $R_{sk}$ is the sheet resistance below the metallisation structure and $R_{sh}$, the sheet resistance in between the metallisation scheme. Both are in Ω/ . Thus, $R_a$ and $R_b$ can be expressed as $R_{sk}$, $R_{sh}$, $W$ and $d$ as:

$$R_T = 2R_a + R_b = 2R_{sk}\frac{L_T}{W} + R_{sh}\frac{d}{W} \qquad \text{Equation 2-31}$$

Where

$$R_a = R_{sk}\frac{L_T}{W} \qquad \text{Equation 2-32}$$

And

$$R_b = R_{sh}\frac{d}{W} \quad \text{Equation 2-33}$$

Conveniently, $R_T$ can be expressed in term of $R_C$, where for simplicity $R_{sh} \approx R_{sk}$

$$R_T = 2R_C + R_{sh}\frac{d}{W} \quad \text{Equation 2-34}$$

Where

$$R_C = R_{sk}\frac{L_T}{W} \quad \text{Equation 2-35}$$

Here, $R_C$ is measured in Ω.

The resistance between metal-semiconductor contact can be determined using four-point probe method. However, the probe and metal-semiconductor contact will introduce another type of resistances as illustrated in Figure 2-18. In Figure 2-18, $R_p$ is the probe resistance, $R_{CP}$ is the contact resistance between probe and metal, $R_C$ is the contact resistance between metal and semiconductor and $R_{sh}$ is the semiconductor sheet resistance.

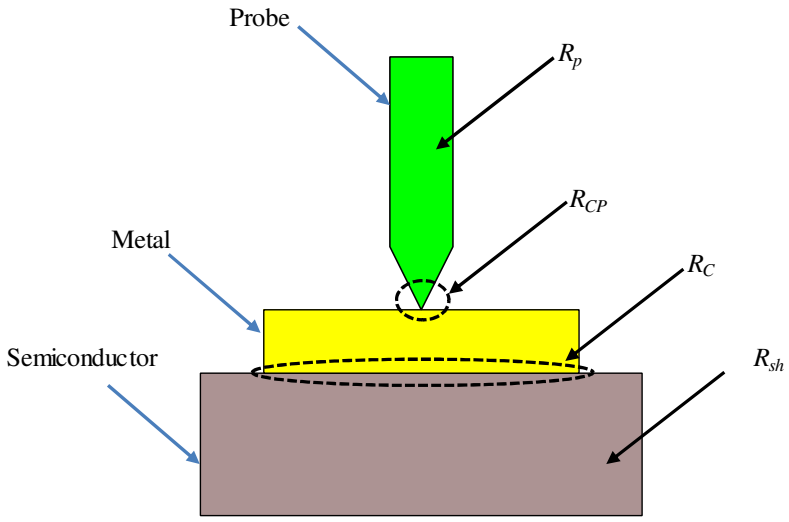



Figure 2-18 Resistances in a metal-semiconductor contact connected with a probe. Black arrows show the resistances and blue arrows are showing the different type of materials.

Figure 2-19 shows the probe arrangement to measure the resistances between two TLM pads.

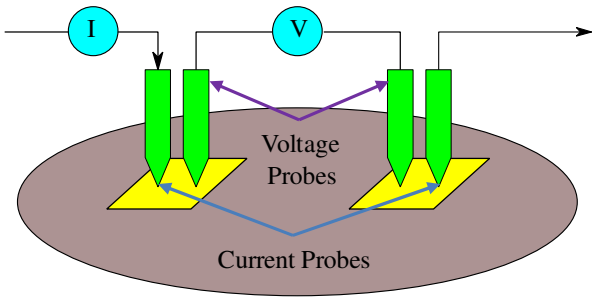



Figure 2-19 Arrangement of probes in a four-point system between two TLM pads.

Since the resistance of the voltmeter is very large (ideally infinity), the small $R_p$ and $R_{CP}$ can be neglected, thus we can accurately determine $R_C$ and $R_{sh}$ from this method. This is the main advantage of using the four-point method where the parasitic resistance introduced by the probes (also the resistances due wire connection to the probe) can be eliminated.

Thus, Equation 2-9 to Equation 2-35 can be simplified to:

$$R_T = 2R_C + R_{sh}\frac{L_i}{W} = {}^{V}/_{I} \qquad \text{Equation 2-36}$$

From Equation 2-36, the value of $R_C$ and $R_{sh}$ can be extracted from the linear plot of total resistance ($R_T$) versus several numbers of TLM pad separation ($L_i$).

A graphical representation of four probing points for TLM measurements are shown in Figure 2-20. As shown in the diagram, $L_i$ is the spacing between adjacent TLM pads, where the spacing is from 5 µm to 45 µm, with increasing in 5 µm steps. A constant DC current of 1 mA is supplied by the current probes between the very top and very bottom pads. The voltage probes are moved between the two adjacent pads spacing ($L_i$) and its potential are then being recorded (in mV). The total resistance ($R_T$) is simply calculated by the dividing the voltage ($V$) by the current ($I$) , as shown in Equation 2-36.

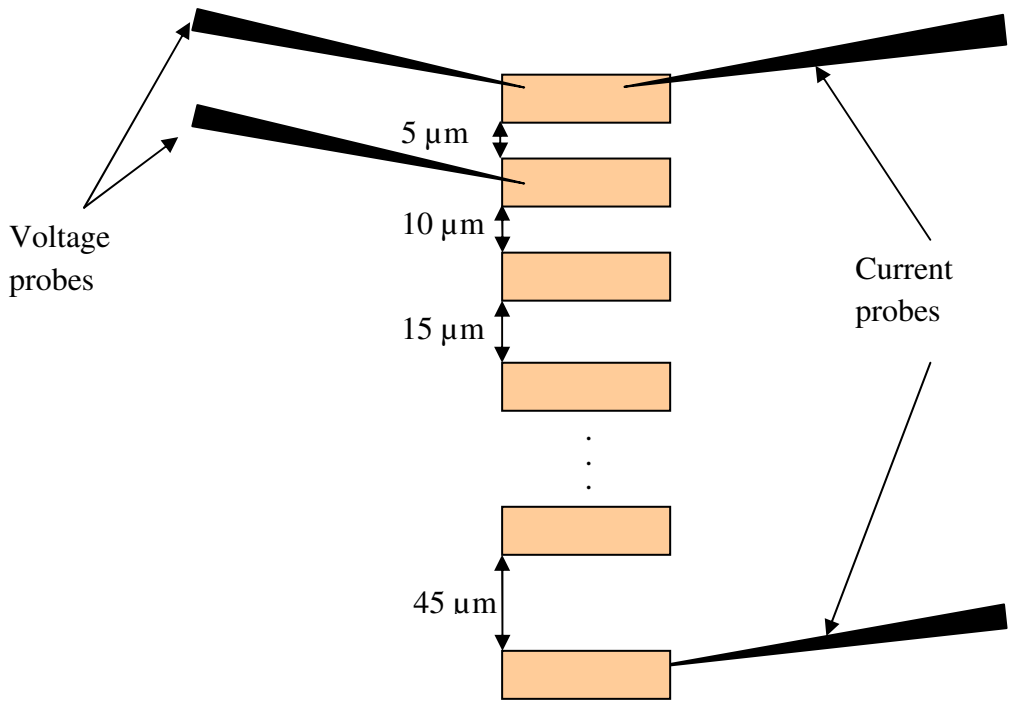



Figure 2-20 Probing techniques in TLM measurement

An illustration of these parameter extractions is shown in Figure 2-21. It is shown that $R_{sh}$ can be extracted from the slope and the $R_C$ can be obtained from the crossing at the y-axis.

From Figure 2-21, for TLM pads with 100 µm width, the extracted data for $R_{sh}$ and $R_C$ is 239 Ω/ and 0.155 Ω.mm respectively.

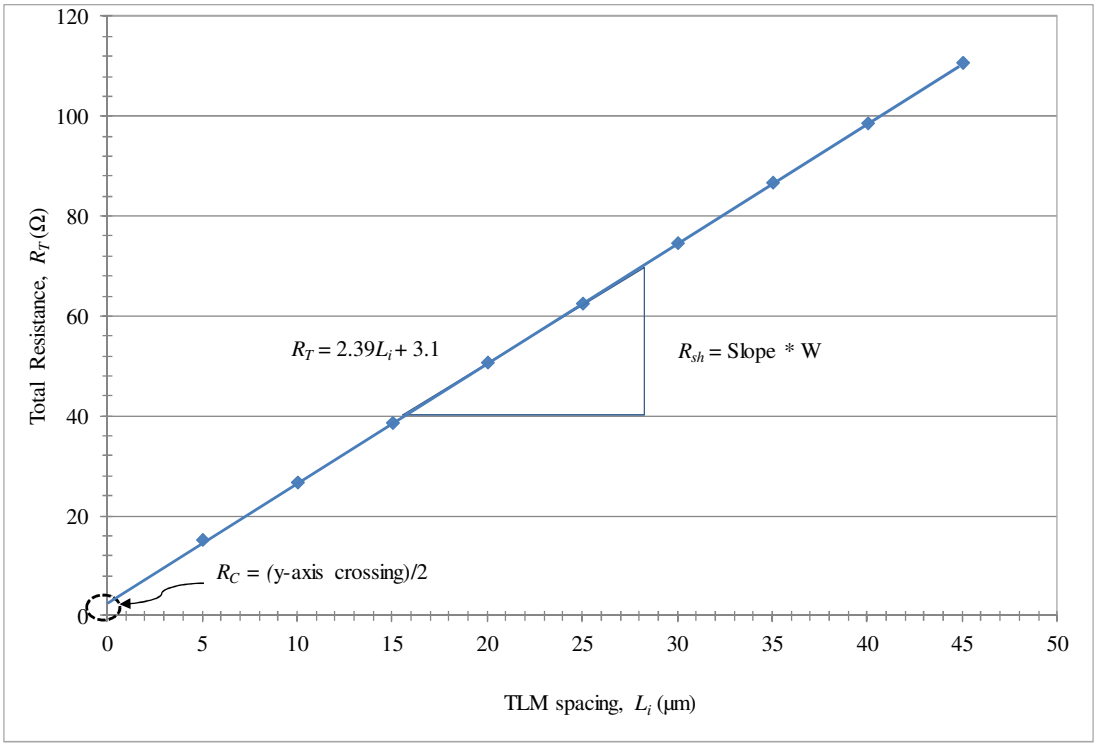



Figure 2-21 An illustration of the determination of $R_C$ and $R_{sh}$ from TLM measurement

### 2.9.2 Ideality Factor and Schottky Barrier Height

After gate recessing and gate metal thermal evaporation, it is essential to check the quality of the gate contact before proceeding to the next fabrication stages. In pHEMT processing, this is the most critical stage, where failure to comply results in device failure.

A comprehensive test at this stage is the determination of ideality factor ($n$), Schottky barrier height ($\Phi_{Bn}$), and series resistance ($r_s$) from the thermionic emission current equation of a forward biased Schottky gate terminal.

Figure 2-22 illustrates the Schottky contact under forward bias. As discussed before, the external bias will reduce the barrier height as seen by electrons from the semiconductor, while maintaining the metal-semiconductor barrier height. As a result, more electrons will have energy to overcome this barrier. At this point, current conduction is dominated by the flow of electrons from the semiconductor to the metal side by the mechanism of thermionic emission.

Conversely, when a reverse gate voltage is applied, an increasing barrier height is seen by the electrons from the semiconductor side, restricting their movement to the metal side. The metal-semiconductor barrier height remains the same. Therefore, in reverse bias, the reverse current is dominated by electron flow from the metal to the semiconductor side.

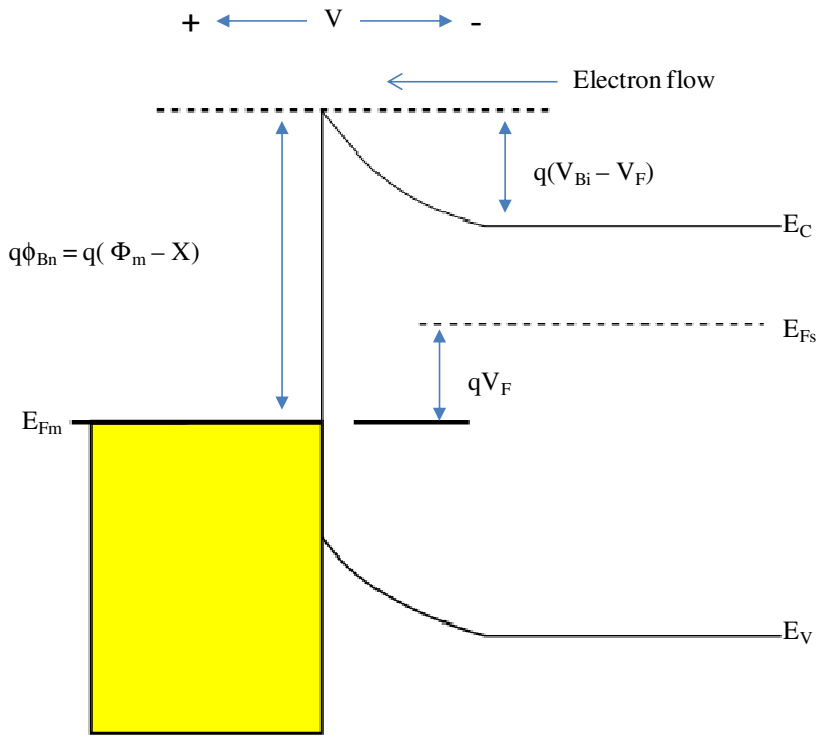



Figure 2-22 An illustration of a Schottky contact band diagram under forward bias.

The thermionic current-voltage relationship of a Schottky barrier diode with area A at an applied voltage V is given by Equation 2-37 to Equation 2-39

In the equations, $I_S$ is the saturation current, A* is the Richardson constant, k is Boltzman constant and T is the temperature in K. Figure 2-23 (a) shows an illustration of Schottky current-voltage characteristic under forward bias.

$$I = A\,A^{*}T^{2}\,e^{\frac{-q\Phi_{Bn}}{kT}}\left(e^{\frac{qV}{nkT}} - 1\right) \qquad \text{Equation 2-37}$$

Substituting

$$I_S = A\,A^{*}T^{2}\,e^{\frac{-q\Phi_{Bn}}{kT}} \qquad \text{Equation 2-38}$$

Thus,

$$I = I_S( e^{\frac{qV}{nkT}} - 1) \quad \text{Equation 2-39}$$

In Figure 2-23, when V > 3 kT/q, the semi log plot of current is linear over the applied voltage. In the linear region, the Schottky current can be simplified to:

$$I = I_S( e^{\frac{qV}{nkT}} ) \quad \text{Equation 2-40}$$

$$slope = \frac{\Delta ln\, I}{\Delta V} = \frac{q}{nkT} \quad \text{Equation 2-41}$$

Thus

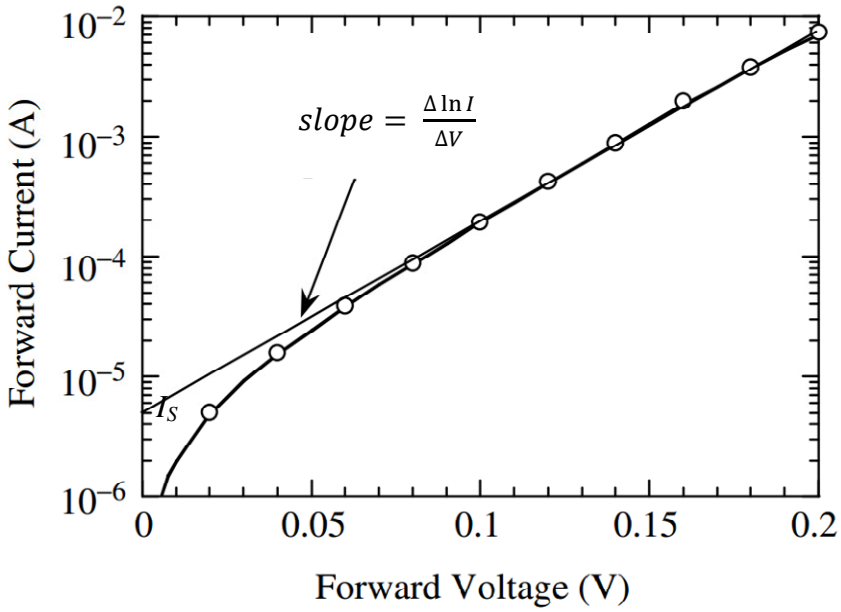
$$n = \frac{\Delta V}{\Delta ln\, I} * \frac{q}{kT} = \frac{q}{kT} * \frac{1}{slope} \quad \text{Equation 2-42}$$

In the same figure, the fitted linear current-voltage relationship based on Equation 2-40 is also illustrated. The value of $I_S$ is obtained by the crossing of the y-axis. Therefore, from Equation 2-38, the barrier height can be calculated as:

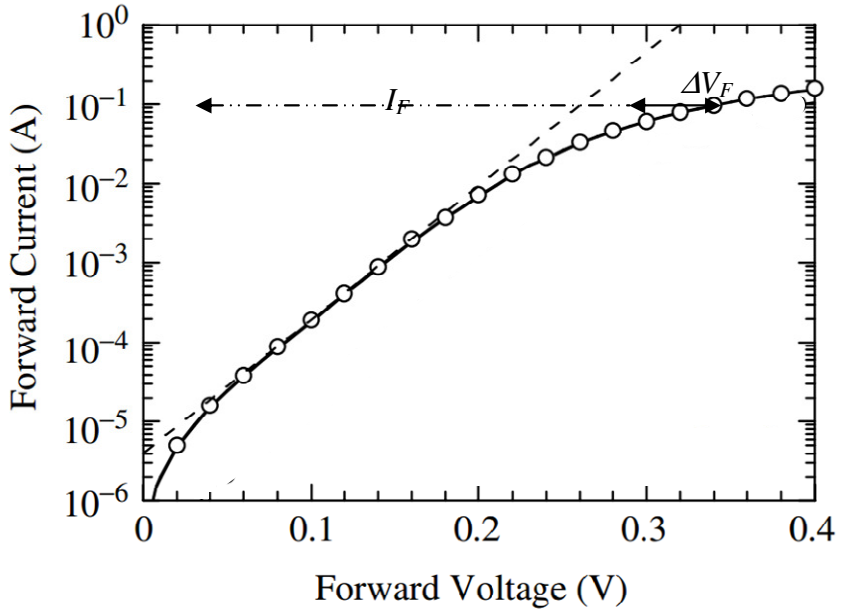
$$\Phi_{Bn} = \frac{kT}{q} \ln\left(\frac{AA^*T}{I_S}\right) \quad \text{Equation 2-43}$$

Figure 2-23 (b) shows the current-voltage relationship at higher applied voltage. At high values of input voltage *V*, the forward current tends to saturate due to the effect of series resistance, $r_s$. If the voltage difference between the fitted straight line and the measured I-V curve is denoted as $\Delta V_F$, at current $I_F$, the series resistance, $r_s$ is simply calculated from:

$$r_s = \frac{\Delta V_F}{I_F} \quad \text{Equation 2-44}$$




(a)




(b)

Figure 2-23 Parameter extraction for (a) ideality factor ($n$) and barrier height ($\Phi_{Bn}$) and (b) series resistance ($r_s$) from Schottky forward current characteristic [47]

# CHAPTER 3

# OPTIMISATION OF InGaAs/InAlAs/InP FABRICATION PROCESS

## 3.1 OPTIMISATION ON GATE RECESS

As described previously, devices under study in this project are depletion-mode type where devices are normally ON when $V_{GS}$= 0 V. The gate recess process plays a vital role in determining the quality of Schottky contact and consequently the device's DC performance. Earlier experiments have shown that the gate recess structure (depth and width) has massive influence on the device's electrical performance such as threshold voltage ($V_{th}$), pinch voltage ($V_p$) and drain-source current ($I_{DS}$)[48]. Due to the importance of the gate recess process, this chapter will begin with the optimisation of gate recess steps, followed by temperature control during the fabrication steps.

### 3.1.1 High Selectivity Wet Etchants

In the pHEMT fabrication process, gate recess is the step where the InGaAs cap layer is removed to expose the underlying InAlAs layer, allowing the formation of Schottky gate structure. As a result, this process will determine the depth and distance between the gate electrode and the centre of the channel layer, which is closely related to $V_{th}$ of the device. A reproducible and controllable gate recess process will not only improve the uniformity of Gate's voltage current modulation, but also plays a very important role in getting better processing yields.

Therefore, the chosen etches should be able to completely etch away the Cap layer and also be able to stop when reaching the underlying Schottky layer. The commonly used Adipic Acid etchant has both process repeatability and reliability problems even though the fabricated working devices have shown remarkable DC and Radio Frequency (RF) performance [49].

For these reasons, it was decided to use a high selectivity etchant, Succinic Acid (SA). Succinic Acid is a more favourable solution due to its high selectivity and smoother etched surface that can be obtained after the etching process [50]. Usually, Succinic Acid is mixed with ammonia ($NH_4OH$) and hydrogen peroxide ($H_2O_2$). Normally two types of chemical reaction take place in this etching mixture. First, the semiconductor surface is oxidised, then this oxidised layer is removed in the second phase of the reaction. Succinic Acid has previously been shown to have a high selectivity to etch away lattice matched InGaAs and InAlAs. The selectivity to etch both materials was shown to be 1000 times and 500 times over AlAs [51, 52]. In the present device processing, a moderate etch rate in the InGaAs layer is chosen so that the etching solution is not very reactive, which can result in detrimental effect to the Schottky under layer. In parallel to this, the etch rate for InAlAs is set to be very slow, so that the Schottky layer etching is not a strong function of time and process variations.

Previously, Fourre et. al. [53] have found that the best Succinic Acid composition selectivity to lattice match InGaAs/InAlAs layers is 70 with 15:2 SA:$H_2O_2$ composition. Their etchant solution is prepared by the dilution of 200 g of crystal acid and Hydrogen Peroxide in one litre of deionised water. Ammonium hydroxide ($NH_4OH$) is then added to the solution to complete the dilutions of acid granulates and regulate the pH of the solution to 5.

Similar experiments were carried out at the start of this project. The initial etch rate of lattice matched InGaAs and InAlAs epitaxial layer was tested by using bulk semiconductor samples. The samples for InGaAs and InAlAs epitaxial layer are VMBE #1593 and VMBE #1594 respectively. The epitaxial structures for both samples were grown using Molecular Beam Epitaxy and schematic profiles of both epitaxial layers are shown in Figure 3-1. As depicted in Figure 3-1 (b), the bulk InAlAs layer is protected by 50 Å of InGaAs layer to prevent the oxidation of the Aluminium compound.

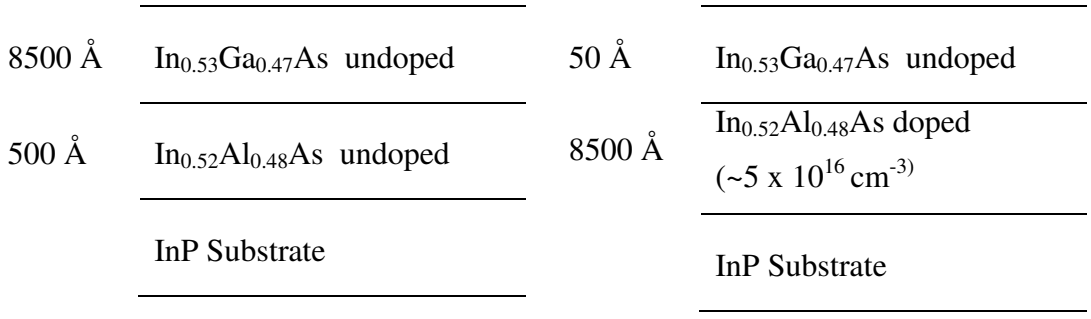



Figure 3-1 Samples' epitaxial layer used in the experiment (a) Bulk lattice match InGaAs VMBE #1593 and (b) Bulk lattice match InAlAs VMBE #1594 (thickness are not to scale)

The samples were prepared by first cleaning them separately in an ultrasonic bath for 5 minutes sequentially with Trichloroethylene, Acetone and Isopropanol (IPA). An additional step on bulk InAlAs was used, where the cap layer was initially removed by a non-selective orthophosporic etch solution ($H_3P0_4$:$H_20_2$:$H_2O$) with 3:1:50 composition for one minute. The etch rate of the orthophosporic composition is ~100 nm/min. All etching processes were performed with agitation and they were rinsed in deionised water for another one minute for proper cleaning. All experiments were done at room temperature (~ 300 K) allowing the chemical compound to be used instantaneously.

The resist used in preparing the structure is AZ® nLOF™ 2070. MESA layer was used as the mask for test structures where the dimensions are larger than 100 µm. The first experiment was aimed at testing the effect of peroxide ($H_2O_2$) composition on the semiconductor etch rate. Since $H_2O_2$ is an oxidising agent, there is a direct relationship with the oxidation rate of the surface layer. The solutions were prepared by the addition of 10 g of succinic acid granulates with 50 ml of deionised water. The acid was then diluted with $NH_4OH$ to pH 6, the same pH value previously used for Adipic Acid etchant [54]. Here, a number of solutions were prepared since each etchant was completed by the addition of varying $H_2O_2$ compositions.

The test structures were patterned by using AZ® nLOF™ 2070 photoresist and MIF 326 developer. At this stage, the etching time was made constant for 5 minutes for InGaAs samples. Since the etch rate of InAlAs is lower than 10 Å/min [53], the

samples were left for 5 hours in the acid solution. The resist layer was then stripped-off and the depth of etching was measured using a Taylor Hobson's Talystep profiler. The resolution of the profiler is 2 nm [55]. The etch rate is calculated by the averaging etch depth over etching time in each of the solutions.

In this chapter, the measurements were taken from five different numbers of trances of 200 μm size each at random locations on the samples. Then, the average values were calculated from these measured data. The resulted etch rate for both InGaAs and InAlAs samples are illustrated in Figure 3-2.

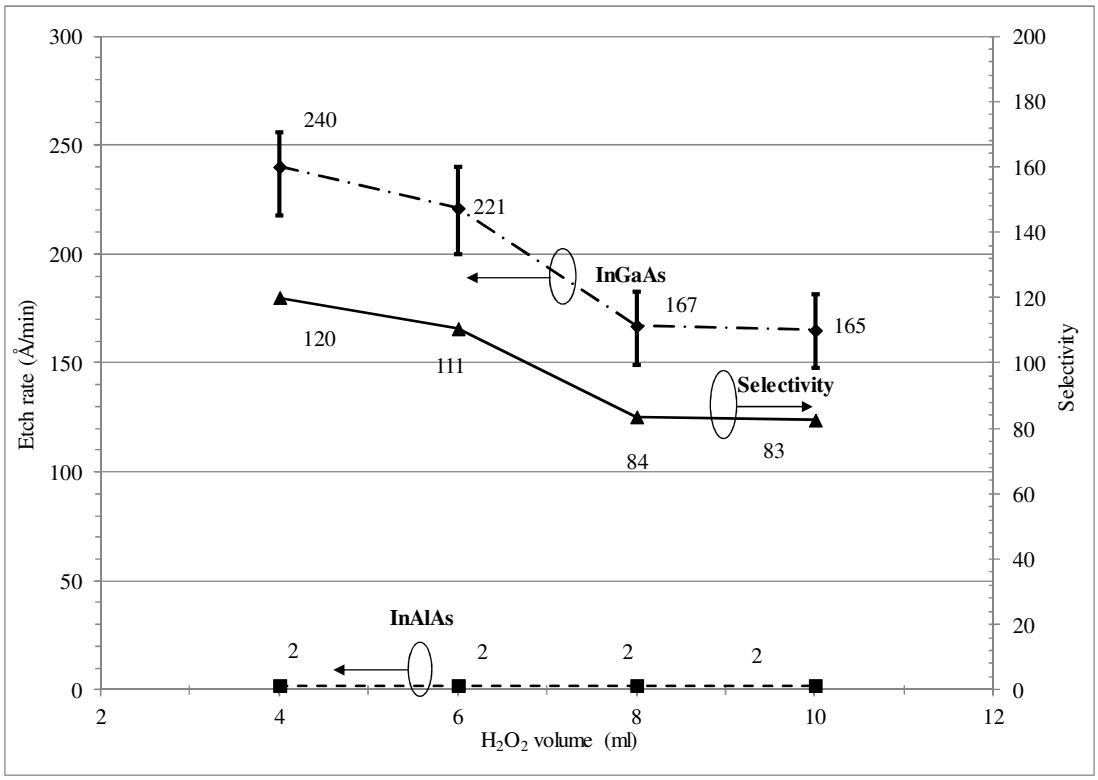



Figure 3-2 Etch rate of lattice matched InGaAs and InAlAs (dashed lines) and selectivity (continuous line) in different $H_2O_2$ composition. (DI volume = 50 ml and pH = 6)

From the above figure (Figure 3-2), a decrease in the etch rate of InGaAs as the $H_2O_2$ volume increases can be observed. The decreasing trend is in agreement with Fourre et al studies. The decreasing etching rate means that the rate of surface oxidation increases as the peroxide volume increases. Thicker oxide layer can hardly be removed from the second chemical reaction, which is represented by a shallower

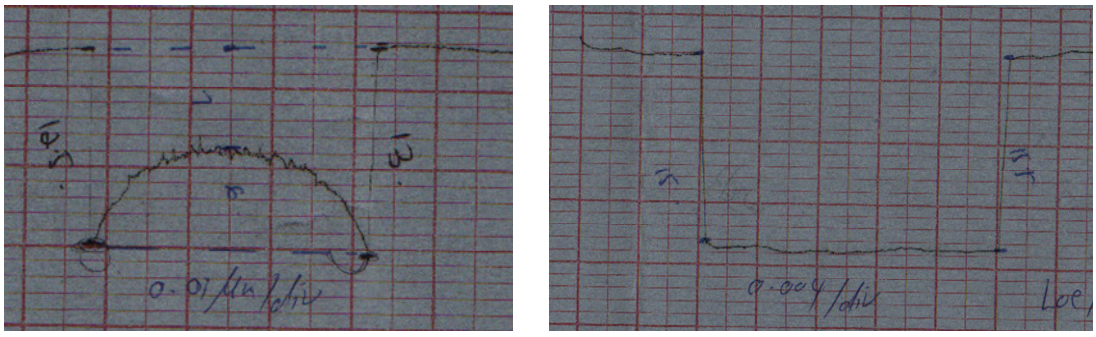
etch depth. Another turning point can be observed at $H_2O_2$ volume between 6.0 ml to 8.0 ml, where the etch rate fall by 50 Å/min, higher than when the $H_2O_2$ volume is < 6.0 ml and > 8.0 ml. When the $H_2O_2$ volume is < 6.0 ml and > 8.0 ml, the InGaAs etch rate is not a strong function of $H_2O_2$ composition.

The etch rate for InAlAs is constant at ~ 2 Å/min. This confirms the purpose of the Aluminium element in a ternary compound as the chemical etch stop layer. From this relationship, the selectivity of etchant can be calculated as in Equation 3-1 . The selectivity shows a declining trend, and is proportional to the InGaAs etching rate.

$$Selectivity = \frac{InGaAs\ etch\ rate\ (\text{Å}/min)}{InAlAs\ etch\ rate\ (\text{Å}/min)} \qquad \text{Equation 3-1}$$

Shown in the same Figure 3-2 is the min-max etches rate error bar with respect to the average value. The error bar in this measurement is about 10 %, which corresponds to deviation of only 20 Å/min between the min-max data from the average values. Since the etch rate of InAlAs is very small, no visible error bar can be seen in this measurement.

During the step profiling measurement, an important observation has been made (as shown in Figure 3-3), particularly on the InGaAs layer. As can be observed in the InGaAs etch profile, there is a “hump” in the middle of the trench caused by the uncompleted etching reaction. This structure will be called “Dome Effect” hereafter. On the other side, InAlAs shows clean and flat trenches etched profile.



(a) (b)

Figure 3-3 Etch profile by Talystep Step Profiler (a) InGaAs sample showing 0.01 µm/div and (b) InAlAs sample showing 0.004 µm/div

To examine the Dome Effect in the InGaAs layer, the percentage of dome height to etch depth is calculated. The graphical representation for the calculated percentage is shown in Figure 3-4 and the calculation formula for Dome Effect is shown in Equation 3-2. The persistence of doming effect can be viewed as the etchants etch away the crystalline materials at different rates depending upon which crystal face is exposed.

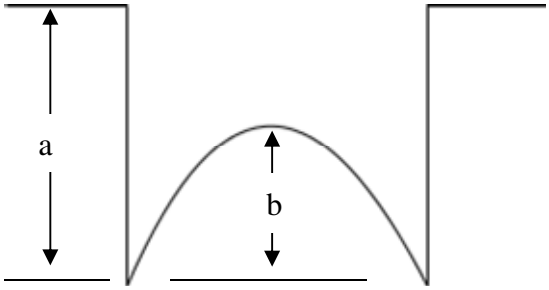



Figure 3-4 Calculation for percentage of dome profile

$$Percentage\ of\ Dome\ Effect = \frac{Dome\ height, b\ (\mathring{A})}{Etch\ depth, a\ (\mathring{A})} \qquad \text{Equation 3-2}$$

From the formula above, the foreseen percentage can be viewed as meaning the higher percentage, the higher the dome height relative to etch depth and thus the more prominent it is in the etching profile.

Figure 3-5 demonstrates the doming effect in InGaAs layers for different $H_2O_2$ composition. It can be seen that the dome height is around 40% to 50% over $H_2O_2$ composition after five minutes etch time. Even though the percentage is stable, it raises a serious processing issue, as it will seriously damage the Schottky contact. Thus, experiments were carried out later not only to decide the best etchant composition, but also to address the elimination of "hump" structure in the InGaAs layers.

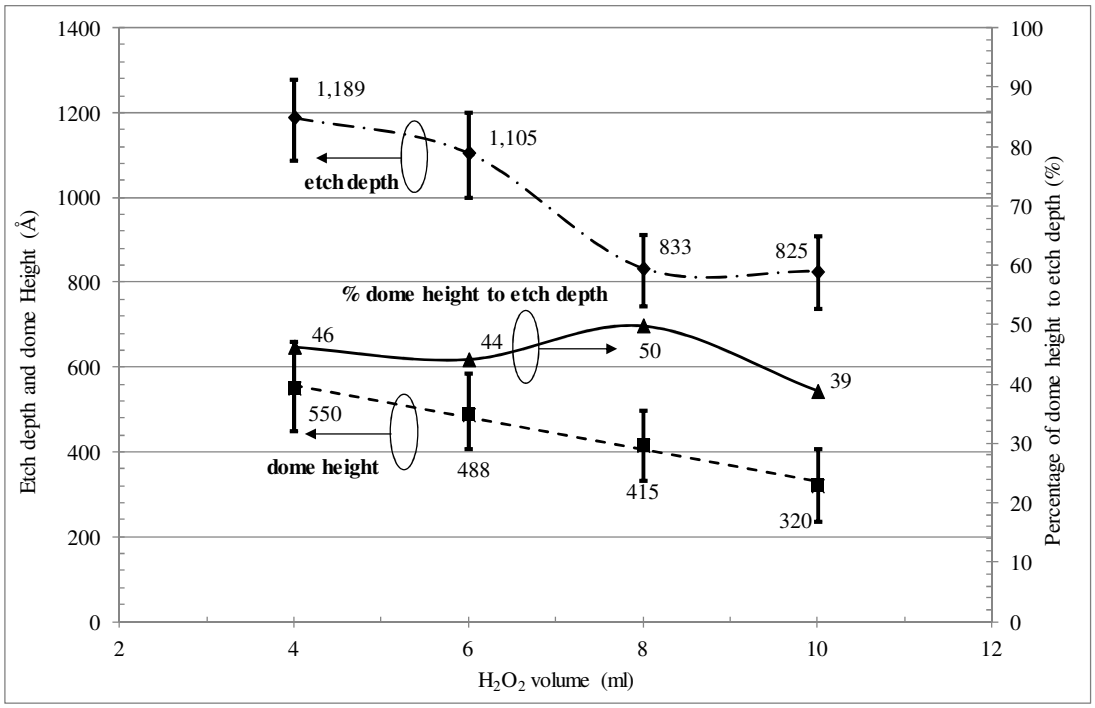



Figure 3-5 Etching profile (dashed lines) and percentage of Dome Effect (solid line) of lattice matched InGaAs (DI volume = 50 ml , pH = 6.0 and etch time = 5 minutes)

The error bar in the measurement of etch depth was also plotted in the same Figure 3-5. For InGaAs etch depth, the error bar is as low as 10 %, which is equivalent to a variation of about ±100 Å from the average value. The variations in dome height are also showing the same value of ±100 Å. Here, all data were measured at the same precision scaling, thus the error in measurement is consistent.

### 3.1.2 Effect of pH Values

Broekaert and Fonstad [52] had investigated the effect of pH value on etch rate of both InGaAs and InAlAs layers. They found that the etch rate of InGaAs peaks at pH 5.0, while the low etch rate for InAlAs is observed at pH 5.0 to pH 7.0. Thus, their experimental data show a high selectivity region at pH from 5.0 to 5.5.

A second set of experiments was prepared to investigate the effect of varying pH values on the selectivity and dome height. By keeping the other compositions at a constant value, the pH value of the prepared solution varied from 5.0 to 6.5. From previous observations, the Succinic acid can be easily and completely dissolved

when the pH value is higher than 5.0, thus this value was set as a starting point. A maximum pH value of 6 is chosen to preserve the solution's acidic characteristic. As the selectivity and Dome Effect did not vary largely with the $H_2O_2$ volume, 8 ml in $H_2O_2$ volume was used for this study. The etching time is 5 minutes and 5 hours for InGaAs and InAlAs, respectively.

The selectivity of solutions and Doming Effect for the second experiment is shown in Figure 3-6 and Figure 3-7 respectively. As shown in Figure 3-6, the InGaAs etch rate decays exponentially while still preserving a low InAlAs etch rate along the pH variations. Thus, the plotted results show that a decrease in the selectivity as the pH value increases. This graph also shows that the pH values do have a strong relationship with the InAlAs etch rate.

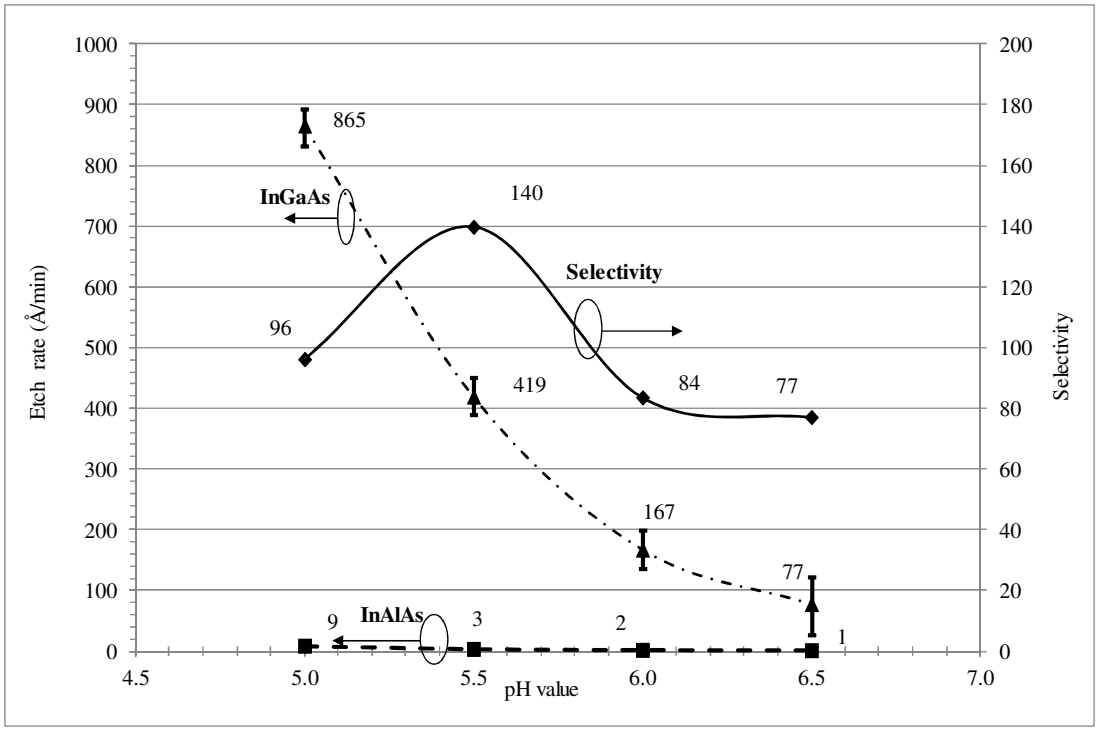



Figure 3-6 Etch rate (dashed lines) and selectivity (solid line) for lattice match InGaAs and InAlAs at different pH values (DI volume = 50 ml and $H_2O_2$ volume = 8.0 ml)

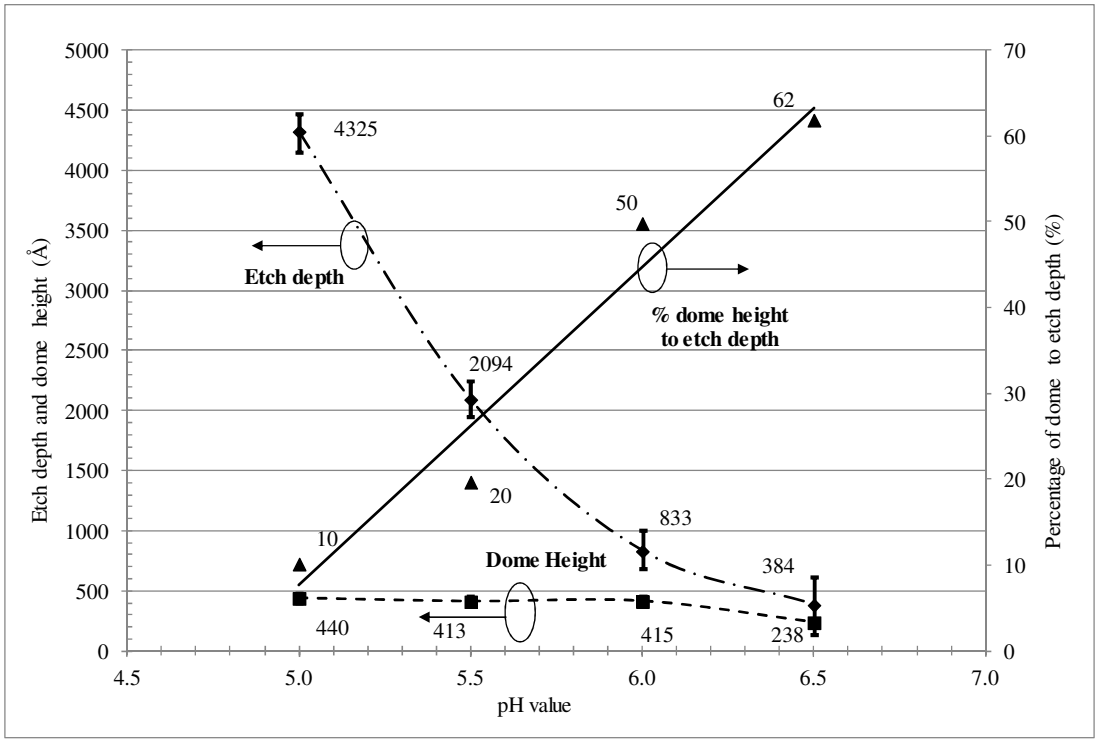



Figure 3-7 Etch profiles (dashed lines) and Doming Effect (solid line) in InGaAs at different pH values (DI volume = 50 ml and $H_2O_2$ volume = 8.0 ml and etch time = 5 minutes)

By referring to Figure 3-7, there is almost a linear transition of Dome Effect percentage across the pH value. This indicates that the doming effect is more pronounced at high pH values. Since the InAlAs layer will act as an etch stop layer, one possible solution for having a clean Schottky gate opening is by etching the surface for longer times in order to eliminate the InGaAs residues. There are little residues at low pH, which can be chosen for a preferable starting point. However, this might initiate another problem of over etching the InAlAs layer, which might damage the Schottky contact.

Thus, other sets of experiments were carried out to investigate the effect of high InGaAs etch rate on InAlAs layer by diluting the solution.

From Figure 3-7, one can observed a large transition in measured data of InGaAs etch depth curve between the lower pH and higher pH values. The large change in measurement will need the experimenter to change the precision scaling, from a lower scaling at low pH value to high precision scaling at high pH value. At large scale, the small variation in etch depth will be invisible thus giving lower percentage

in measurement error. On the other hand, at higher pH, the etch depth was reduced which means higher precision scaling is needed for the measurement. As oppose to large scaling measurement, the small variations in the measurement can easily be seen, in which will increase the measurement error as depicted in Figure 3-7. In this measurement, the error is about 20 % at low pH and increased to more than 60% at higher pH value. The same reason was observed to explain measurement error in Figure 3-6.

With the explanation above, beyond this point, the error bar will be hidden from the presented data due to similar trend, as being presented here.

### 3.1.3 Effect of Buffer Solution

Mouton et al [56] have found that dilution of etching solution can help slow down the etching rate. Their results show that the etch rate drop exponentially as the $H_20$ volume is increased.

Therefore, another set of experiments was conducted to investigate the significance of buffering to both selectivity and Doming Effect. From the previous experiments, low pH was preferred for high selectivity and low dome height percentage. However, in this experiment a pH value of 6.0 is chosen as it is in the middle of the selectivity (89) and dome height (50%) regions (Figure 3-6). Since a high etch selectivity needs to be maintained, $H_2O_2$ volume of 5.0 ml is chosen. The etching time is kept at 5 minutes for InGaAs and 5 hours for InAlAs. This time, the deionised (DI) water was chosen with volumes varying from 50 ml to 200 ml.

The findings from the third study are presented in Figure 3-8 and Figure 3-9. From the plotted data, the falling trends of InGaAs etch rate can be observed, while InAlAs etch rate remains constant at 2 Å/min, which is consistent with previous experiments. A noticeable trend in selectivity is also recorded at low and high buffer solutions. However, the selectivity is high across the buffering, in the order of 140 for 50 ml and 100 ml of $H_20$. A significant drop in selectivity at high buffering is also observed at 150 ml and 200 ml of $H_2O$ volumes, where the selectivity drops to 35 and 29 respectively. Thus, for high selectivity, a volume of 50 - 100 ml of DI water is preferred.

By referring to doming effect plot in Figure 3-9, unexpected but important results were observed. The doming effect is more than 60% on higher water buffering, as compared to 38% at low water buffering. Thus, this reconfirmed that high water buffering is not practical.

The results of studies on chemical composition are summarised in Figure 3-10. The doming effect, which was initially observed in the first experiment, become more prominent at high pH and gets worse at a higher water dilution.

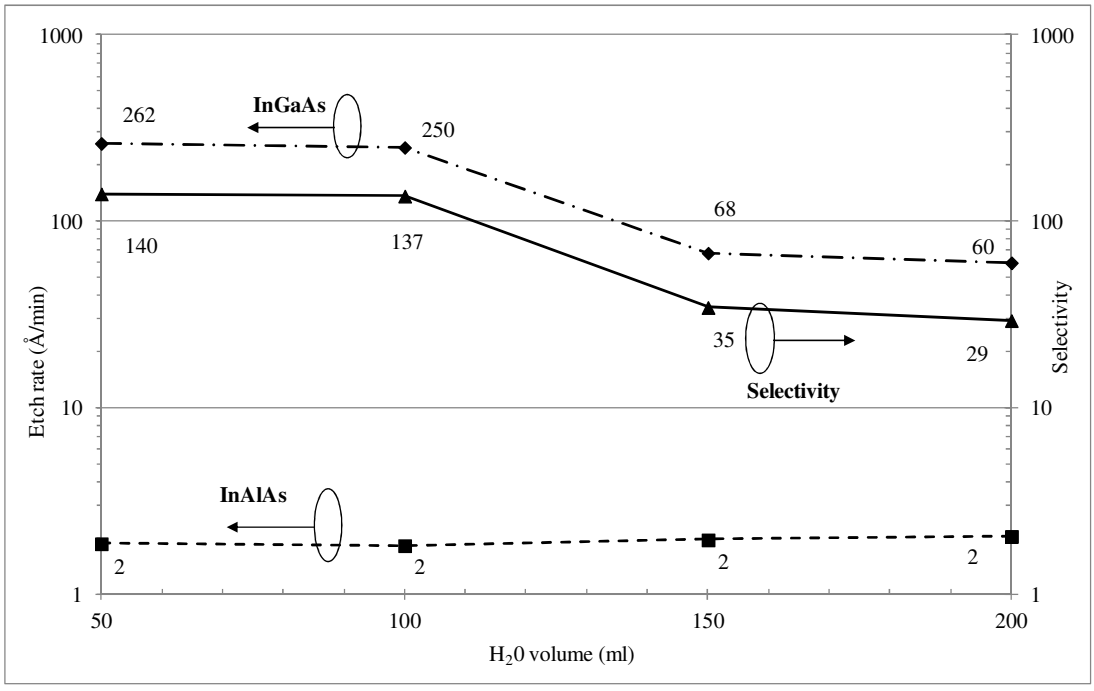



Figure 3-8 Etch rate (dashed lines) and selectivity (solid line) at different DI water volume (pH=6 and $H_2O_2$ volume = 5.0 ml)

From Figure 3-10, it can be concluded that to have a low percentage of Doming Effect, a solution with low pH value, low $H_2O_2$ composition and low DI water must be chosen while maintaining a high InGaAs-InAlAs etching selectivity. Failing to etch the InGaAs cap layer residue is a major cause for the failure in the Schottky contact behaviour. Instead of acting as a Schottky barrier, the InGaAs residue will behave increasingly more like an Ohmic contact after heat treatment and thus deteriorate the device performances. The final chemical composition is summarised in Table 3-1. As mentioned before, these are the most appropriate compositions for

high selectivity and low Dome Effect percentage. As listed in the table, we used 5 ml of $H_2O_2$ for high InGaAs etch rate and high InGaAs-InAlAs selectivity. Additionally, a pH of 5.5 is chosen in order to have a low InAlAs etch rate and low Dome Effect percentage. Finally, low $H_2O$ is chosen for high selectivity in addition to low Doming Effect percentage.

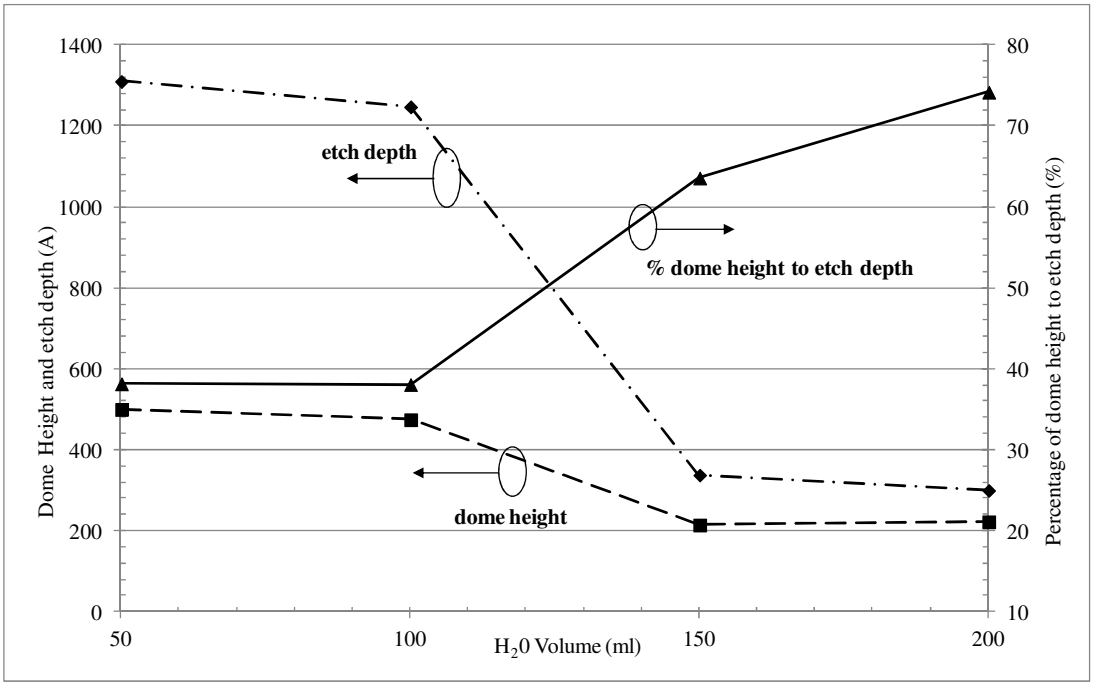



Figure 3-9 Etch profile (dashed lines) and Dome Effect (solid line) at different deionised water volume (pH=6, $H_2O_2$ volume = 5.0 ml and etch time = 5 minutes)

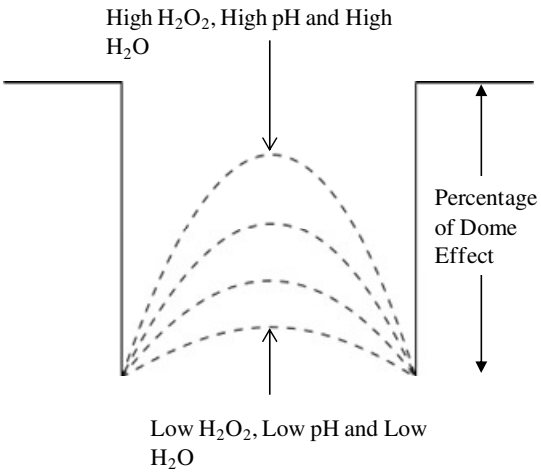



Figure 3-10 Summary from chemical composition studies

Table 3-1 Final succinic acid compositions

| Parameter | Composition/value |
|---|---|
| Succinic acid granulates | 10 g |
| $H_2O_2$ | 5 ml |
| pH | 5.5 |
| $H_2O$ | 50 ml |

### 3.1.4 Etching Time

As pointed out in the previous section, one possible solution to eliminate the Doming Effect is by etching the InGaAs layer for longer times. The findings in section 3.1.3 also show that the Deionised DI water composition does not only reduce the etching rate of InGaAs layer, but more importantly also maintains the etching rate of InAlAs layer. The InAlAs etch rate is approximately 3.5 Å/min (refer to Figure 3-6) at pH 5.5. Capturing these advantages, the optimisation of process steps particularly the etch time is presented in this section.

Since the etch rate of InAlAs is almost negligible, the study was continued only for InGaAs epitaxial layers. By using the same VMBE #1594 samples and etchant composition listed in Table 3-1, a variety of etching times of 0.5 minutes, 1.0 minutes, 1.5 minutes, 2.0 minutes, 3.0 minutes, and 4.0 minutes were used. The results from this experiment are shown in Figure 3-11.

Due to Talystep limitation, for the etching time of 0.5 minute and lower, no measured data were recorded. Thus, the data shown at 0.5 minute in the figure is an approximation. Even though in this experiment, less $H_2O_2$ volume is used, the etch rate at 4.0 minutes shows good agreement with the previous sets of experiments. Previously, the etch rate at the same pH of 8.0 ml of $H_2O_2$ is 419 Å/min (refer Figure 3-6).

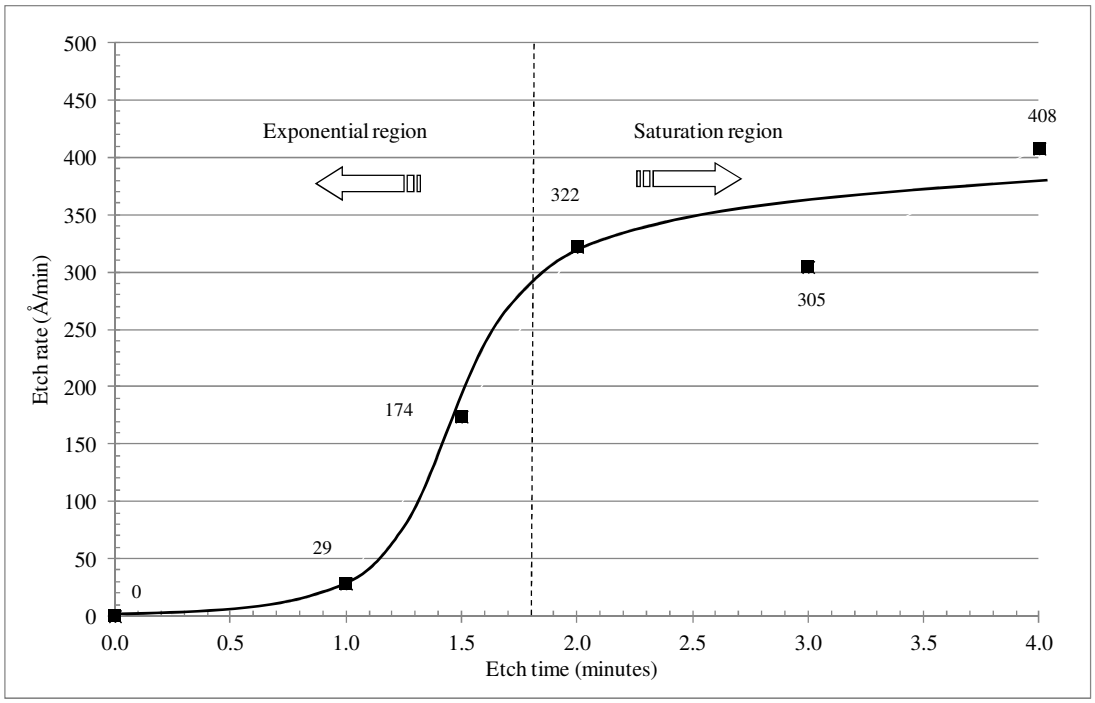



Figure 3-11 Lattice matched InGaAs etch rate at a different etch time
($H_20_2$ = 5.0 ml, pH =5.5 and $H_20$ = 50 ml)

The above figure also illustrates that the etch rate is not a linear relationship with etch time. The distribution of measured data can be described in two regions as shown in Figure 3-11. For a low etching time (less than 2.0 minutes) the etch rate gradually increased from 0 Å/min to about 300 Å/min. This time can be viewed as the time taken for the etchant to break the oxide layer produced from the first chemical reaction before the second chemical reaction can take place. For a longer etch time (greater than 2.0 minutes), the etch rate begins to saturate. Here, the oxide layer is completely etched which makes it possible and easier for the second chemical reaction to take place with the underlying semiconductor surface. As a result, the etch depth is constant over time. This constant etch rate is approximately 360 Å/min

Figure 3-12 illustrates the doming effect at InGaAs samples over different etch times. The 0.5-minute data was left out of the figure due to the tool's limitation. Moreover, even at 1.0 minute the recorded value might be underestimated due to the

same reason. The approximation of real value is shown in the figure as a dotted green line. These data are also consistent with the previous studies.

As depicted in the plot, the etch depth and dome height varies almost linearly over etching time. This reconfirms that the final composition was likely to have a constant etch rate at longer etch times. The figure also indicates that the dome height varies linearly, but at lower rate over etching time. The dome height growth rate is approximately 100 Å/min. In any case the Doming Effect is reduced at a longer etch time and saturates at about 25 %. The results suggest that for better selectivity and smaller Dome Effect, a longer etch time should be selected.

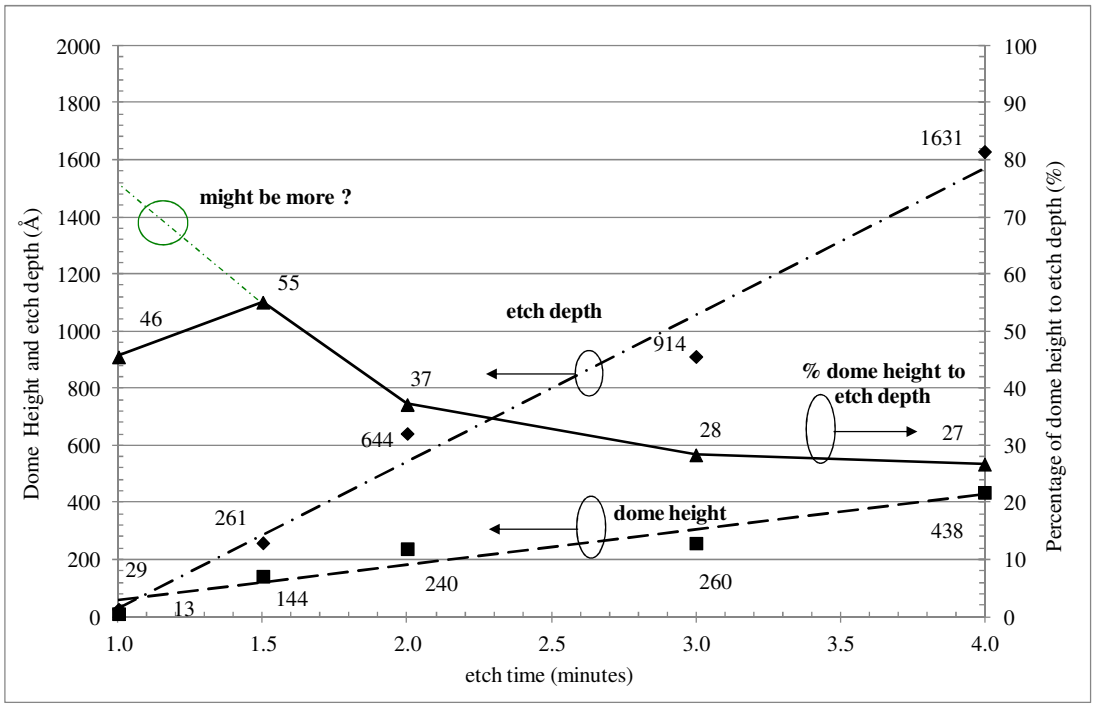



Figure 3-12 Doming effect at different etch time
($H_20_2$ = 5.0 ml, pH =5.5 and $H_20$ = 50 ml)

### 3.1.5 Etching in the Actual pHEMT Epitaxial Layer

The results in section 3.1.4 were not the final conclusion because the samples used were all in bulk lattice matched InGaAs. There was no InAlAs layer that served as a

etch stop layer. Therefore, another experiment was conducted using a sample with an InAlAs etch stop layer. The experiment starts with an epitaxial layer with a 200 Å InGaAs cap layer, and an Aluminium rich InAlAs Schottky layer as the etch stop layer below the InGaAs layer. The thick Cap layer can be advantageous during the Talystep measurement. The epitaxial layer structure is shown in Figure 3-13 and the sample is labelled as XMBE #170. The experiment was carried out at different etch times varying from 1.0 minute to 3.0 minutes with steps of 0.5 minutes. Here, large test structure dimensions were still used. The results are shown in Figure 3-14.

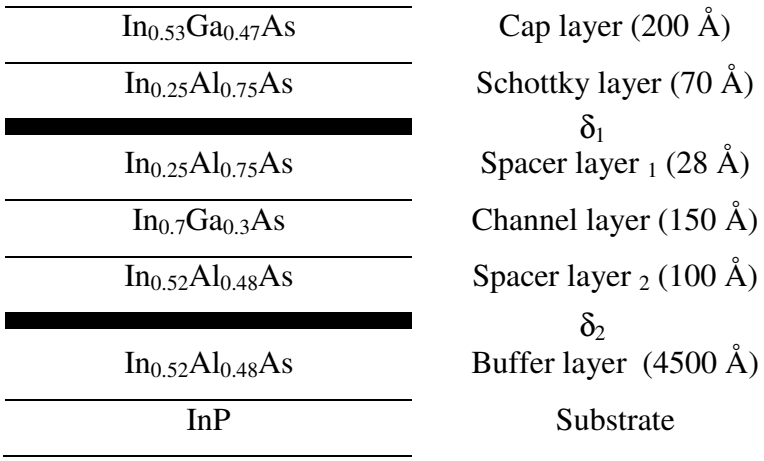



Figure 3-13 Epitaxial layer for XMBE #170 (thickness not to scale)

As shown in Figure 3-14, the dome effect is successfully reduced to 10 % at a higher etches time (longer than 2 minutes). The measured residue on the trenches might be the remaining InGaAs cap or InAlAs layer itself since the final dome height thickness at 2 minutes and longer are about 20 Å with etch depth more than 200 Å. As has been stated before, this might degrade the Schottky behaviour especially for the devices with thin Schottky layers.

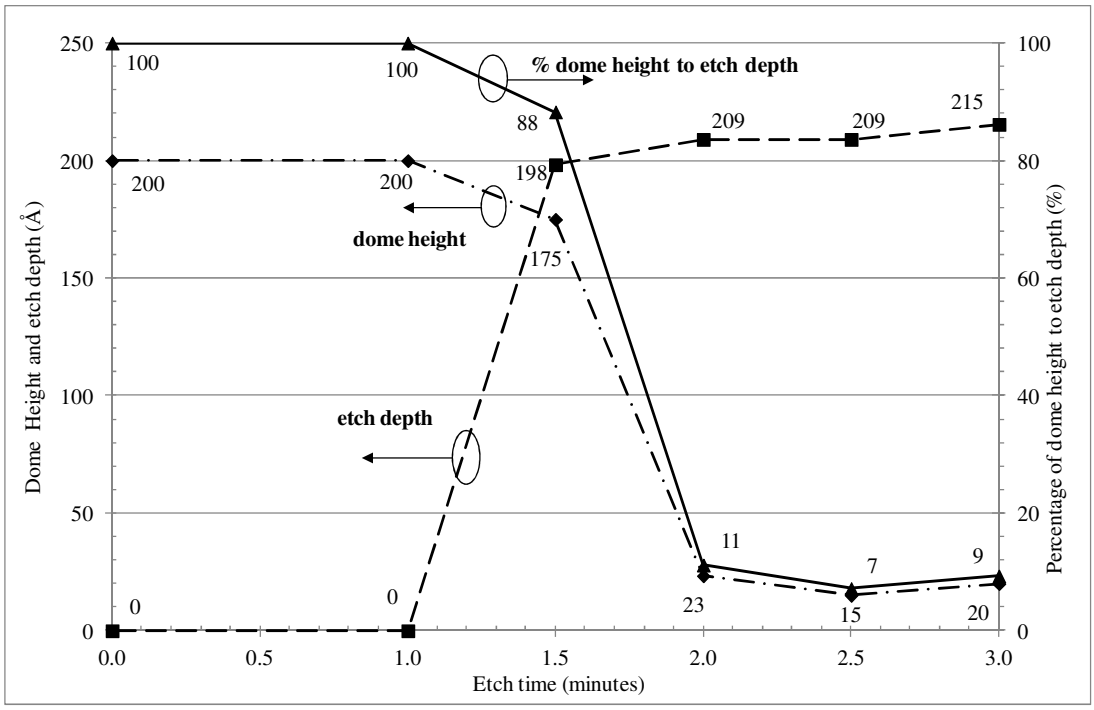



Figure 3-14 Doming effects at XMBE#170 samples

All information gathered from the chemical composition and processing steps studies were used for improvement of 1 µm gate length pHEMT devices. For smaller dimension devices, the doming effect will be more prominent as compared to large trenches dimension in all experiments performed previously.

The 1 µm Schottky contact quality had not been investigated using this newly mixed chemical compound yet. Therefore, this section will conclude with a comparison of the 1 µm length Schottky contact etched by the new etchant with that of the previous gate recess etchant (Adipic Acid). The epitaxial layer used in this experiment (XMBE #129) is shown in Figure 3-15 .

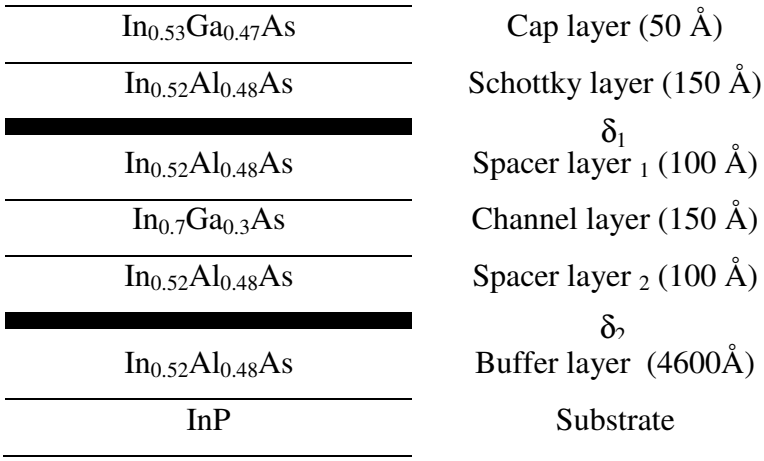



Figure 3-15 Epitaxial layers for XMBE #129 (thickness not to scale)

Figure 3-16 depicts the reverse and forward current for 2-1-2 µm Source-Gate-Drain spacing, 800 µm width Schottky diode, to indicate the improvement of the contact by using the Succinic etchant solution. The Adipic solution was prepared by adding 10g Adipic Acid granulates in 50 ml DI water followed by addition of $NH_4OH$ to adjust pH to 6. The Adipic etch time was set to be 4 minutes. As shown in the figure, the Schottky gate leakage can be improved by nearly 10 times better, just by changing the etchant solution from Adipic Acid to the optimised Succinic Acid solution. No significant change is observed to the surface contact ideality factor ($\eta$) and the metal–semiconductor barrier height ($\phi_B$). The ideality factor and barrier height are maintained at 1.7 and 0.7 eV respectively in both cases.

As shown in Figure 3-16, Schottky gate leakage for devices using Succinic etchant is showing lower gate leakage current than Adipic etchant. For Adipic solution, there were no comprehensive studies about the etching profile or the formation of Dome Effect as presented here, in this work. It seemed that the resulted gate opening from the etching of Adipic Acid solution might not be completed. Thus, there is a high probability that gate trenches have a high percentage of dome height. Since the Cap layer is made from narrow band gap material ($In_{0.53}Ga_{0.47}As$), unfinished gate etching will cause this metal-semiconductor contact to act as an Ohmic, where the carriers from metal side can easily overcome the metal-semiconductor barrier height, which resulting in higher gate leakage current.

Other than that, the improvement on the Schottky leakage can be viewed as evidence of the increase in the gate's off-state breakdown voltage ($V_{off}$). By assuming that both etchants will create the same narrow gate recess trenches, this improvement can be explained by a decrease of surface traps, which reflect the quality of the gate recess surface. The surface traps originate from structural defects during the etching reaction which will capture electrons from the gate when the device is ON, and thus create a negatively charge density on the surface [57]. A clean gate contact surface means reduced surface trap between the metal-semiconductor interfaces, which reduces the peak vertical electric field at the gate. Therefore, the reduced electric field allows higher gate voltage to be applied before the junction breaks down.

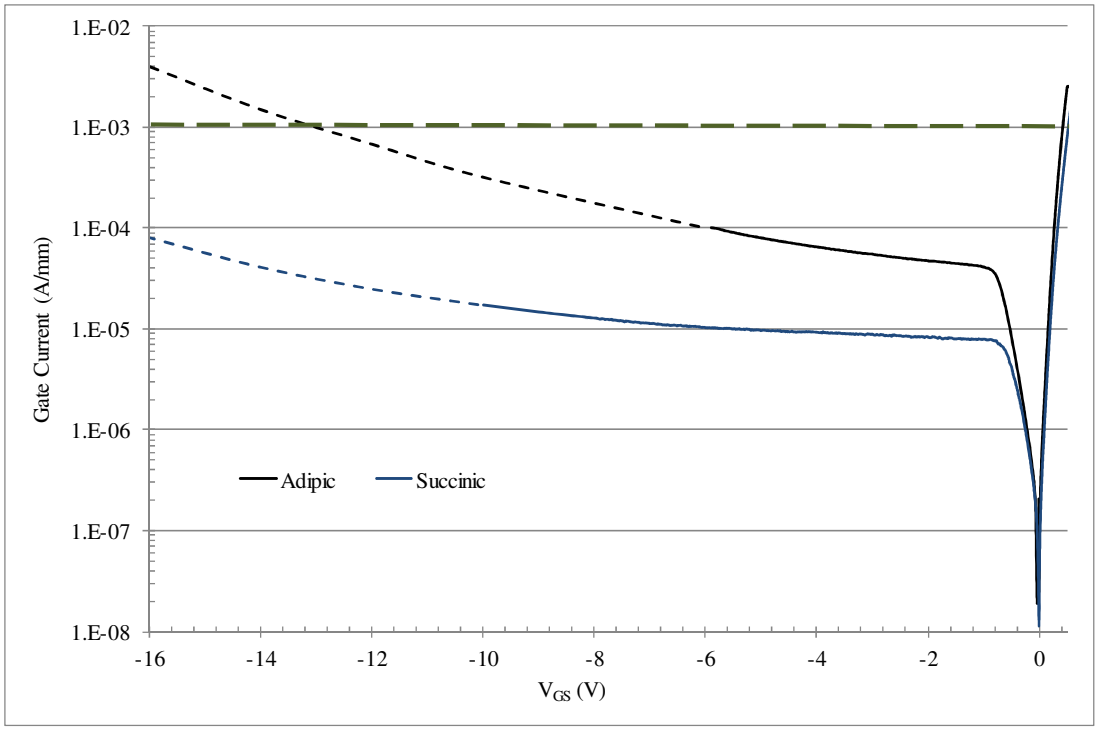



Figure 3-16 Schottky gate current for XMBE #129 showing Adipic (black line) and Succinic (blue line) as the gate recess etchant. The dotted black and blue lines represent the extrapolation of Adipic and Succinic Acid, respectively.

Illustrated in Figure 3-16, the reverse Schottky gate current were measured up to -6V and -10 V for sample etched with Adipic Acid and Succinic Acid, respectively.

Beyond these measurement points, the data were extrapolated to gate voltage of -16 V. By defining the reverse breakdown voltage as the reverse voltage where the reverse gate current is equal to 1 mA/mm, both samples were showing high reverse breakdown voltages. The reverse breakdown voltage for sample etched by Adipic Acid was showing high breakdown voltage of approximately - 13 V, whereas more than - 16 V is demonstrated for Succinic Acid sample.

Similar to other diode characteristics, when higher reverse gate voltage is applied beyond this point, the Schottky diode will be driven into an avalanche breakdown region where the carrier multiplication will occur and there will be an abrupt transition to an excessive amount current flow, in which the Schottky contact will be permanently damaged.

## 3.2 THERMAL STABILITY

In the previous section, the gate recess etching using Succinic has been demonstrated to improve the Schottky contact quality and considerably lower the gate leakage by a factor of ten. However, as depicted in Figure 3-16, the curve bending at higher $V_{GS}$ indicate that the gate still suffers higher leakage, which reduces the gate stability at high $V_{GS}$ values. Therefore, it is essential that the Schottky gate contact is both mechanically and thermally stable, so that the metal gates can survive during high-temperature process and during harsh device operation.

For these reasons, another set of samples was prepared. This time, several sizes of 2-1-2 µm Source-Gate-Drain spacing 1 µm Schottky gate length were patterned on XMBE #178 samples. The epitaxial layer for the samples is shown in Figure 3-17. As illustrated in the figure, the fabricated devices have 50 Å InGaAs cap layer, and a wide band gap $In_{0.25}Al_{0.75}As$ material as the Schottky barrier layer so that thermal stability studies on the Schottky Diode were performed from the advantage of a higher barrier height. As an extension to the previous experiments, three sets of gate recess etching time were also tested in this experiment, namely 3, 4 and 5 minutes. All samples were prepared using the succinic acid composition listed in Table 3-1. All etching processes were done using agitation during the etching period.

A 50 nm of Ti and 400 nm of Au (hereafter denoted as 50/400nm of Ti/Au) metal evaporation took place after the samples were etched. After liftoff, the sintering studies and device's Schottky diode measurements were carried out to examine the gate thermal stability together with the quality of the each gate recess step. For comparison purposes, four sets of different temperature parameters were used in this test: Presintering (25 °C), 200 °C, 250 °C, and 300 °C were used. Each sample was sintered on a hot plate set to the desired temperature for 5 minutes. The Schottky diode measurements were performed using Agilent's B1500 Semiconductor Device Analyser.

| | |
|---|---|
| $In_{0.53}Ga_{0.47}As$ | Cap layer (50 Å) |
| $In_{0.25}Al_{0.75}As$ | Schottky layer (300 Å) |
| δ | |
| $In_{0.25}Al_{0.75}As$ | Spacer layer $_1$ (100 Å) |
| $In_{0.7}Ga_{0.3}As$ | Channel layer (150 Å) |
| $In_{0.52}Al_{0.48}As$ | Buffer layer (4500 Å) |
| InP | Substrate |

Figure 3-17 Epitaxial layer for XMBE #178 (thickness not to scale)

Figure 3-18 shows the gate I-V characteristic for 50 µm total gate width at different sintering temperature after 3 minutes of gate etching time. In this section and hereafter, at least four devices from random locations were measured. The results shown in the figure are only the characteristics for the best device as they were all uniform within variation of 10%.

The almost flat reverse current indicates the advantage of the used high band gap material as the Supply layer. The forward current for Room Temperature (Pre-sintering) and all other sintering temperature peaks at 100 mA/mm at the forward voltage of 1 V. When reverse biased, the graph clearly shows interesting diode characteristics. For pre-sintering and low temperature (200 ° C), the leakage current at a reverse voltage -8 V is about -20 µA/mm whereas at 250 ºC the leakage increases almost doubles to -130 µA/mm and becomes worst at 300 ºC where the

leakage is -1500 µA/mm. Even though heat does not change the forward current, too much it clearly damages the Schottky as seen by the much larger leakage current at 250 ºC and 300 ºC.

Previously the presence of Aluminium oxide layer between the gate metal and InAlAs interface has been reported [58]. Because aluminium will react instantaneously with oxygen to form oxides, this process becomes more prevalent at higher composition of Al atoms in the InAlAs layer and will accelerate at high curing temperatures. This result in an unavoidable oxide layer, which will pull down the barrier heights causing the large leakage, is observed.

In this experiment, the barrier height was deduced to be 0.7 eV after 200 ºC sintering temperature and reduced to 0.6 eV and 0.5 eV at sintering temperatures of 250 ºC and 300 ºC, respectively.

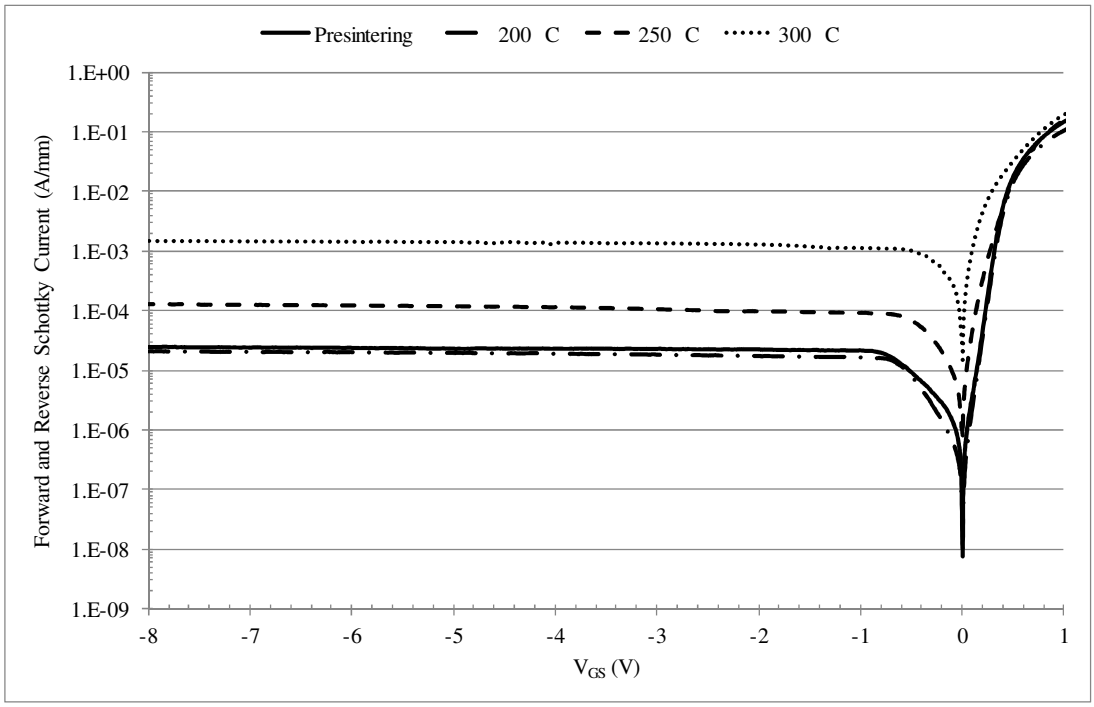



Figure 3-18 1 x 50 µm gate width sintering studies for 3 minutes succinic etch time

Similar trends were observed for both the 4 minutes and 5 minutes gate recess etching times. The peak forward gate current is consistent at 100 mA/mm for all etching times. The Schottky leakage was increased from 10 µA/mm before sintering to 30 – 60 µA/mm after sintering at temperatures of 200 ºC and 250 ºC. At 300 ºC, the leakage was considerably higher than 100 µA/mm for both etching times. The Schottky diode data for both the 4 and 5 minutes etching times are illustrated in Figure 3-19 and Figure 3-20 respectively.

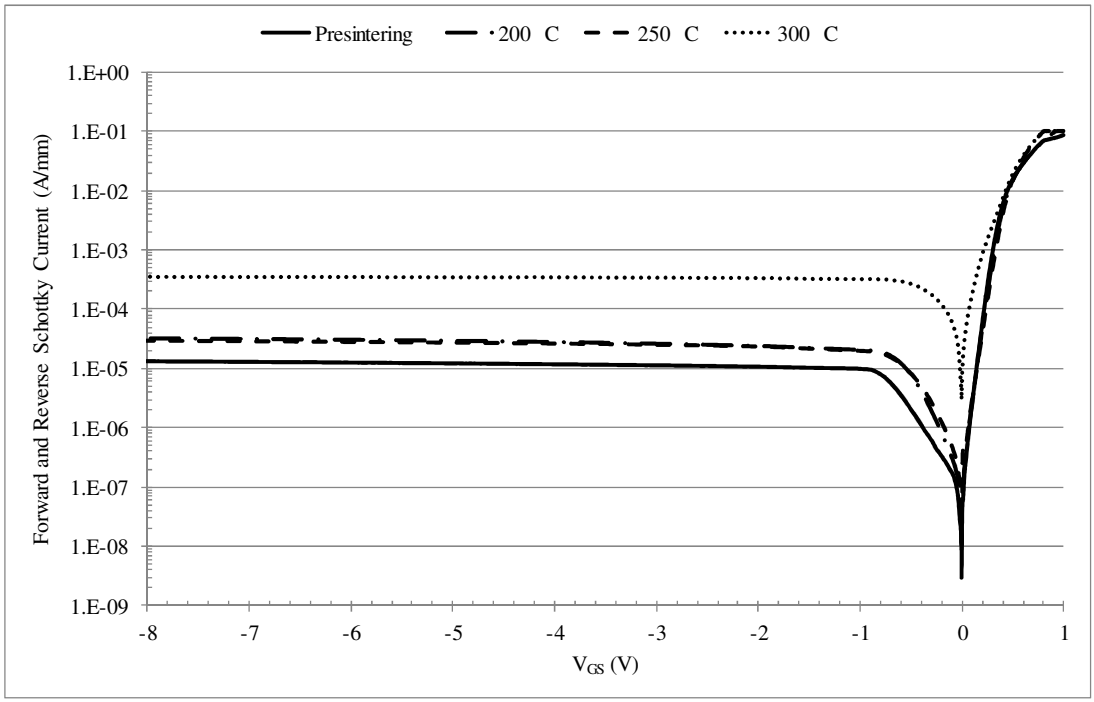



Figure 3-19 1 x 50 µm gate width sintering studies for 4 minutes succinic etch time

From the measured data, it is clear that a low sintering temperature is preferred for better Schottky and lower leakage current. At sintering temperatures lower than 250 ºC, small leakage current (less than 100 µA/mm) can be achieved in this epitaxial structure. For sintering temperature of 300 ºC and for all gate recess etching times, the leakage gets smaller as the etching time was increased. This shows that longer etching time will produce a more stable Schottky contact with lower Schottky gate leakage. It can be concluded from the results of the 400 µm devices that 5 minutes

gate recess etching and 200 ºC sintering temperature can produce a thermally stable Schottky contact.

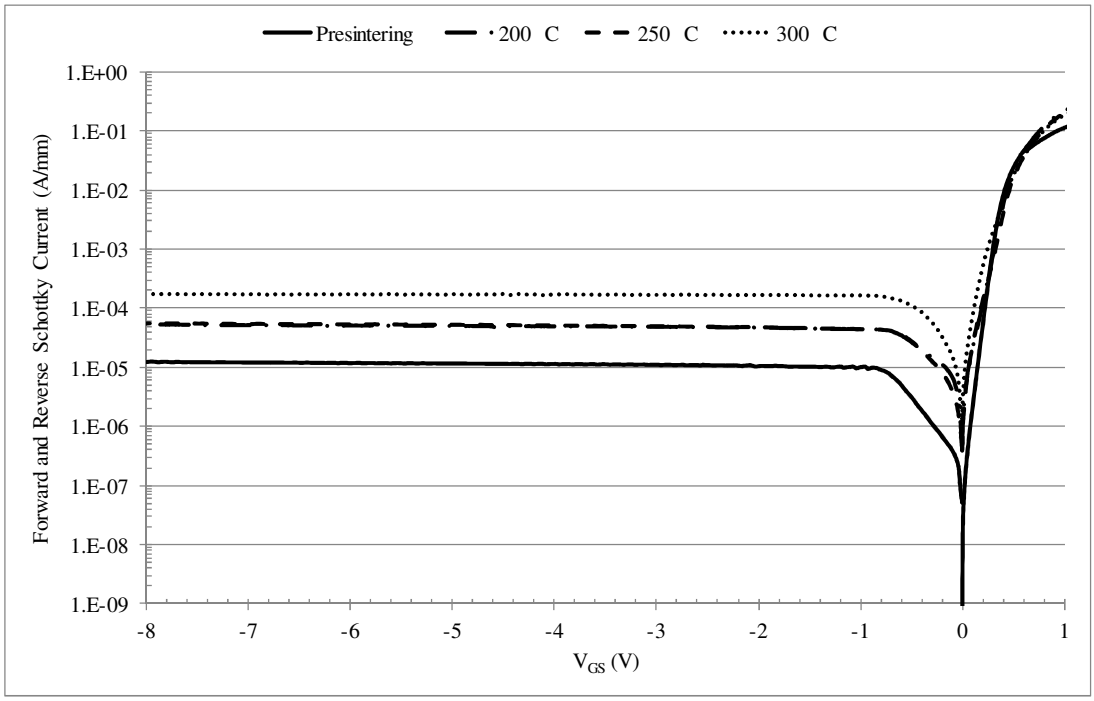



Figure 3-20 1 x 400 µm gate width sintering studies for 5 minutes succinic etch

## 3.3 SIDE WALL SPACER

In the pHEMT device process developed on The University of Manchester, the devices were isolated using a MESA isolation technique. Here, the pyramid like MESA structure was realised by non-selective wet etchant $H_3PO_4$ (3:1:50 chemical composition of $H_3PO_4$:$H_2O_2$:$H_2O$). This structure however, will expose and short-circuited the narrow band gap InGaAs channel to the Schottky gate metal after gate metal evaporation and lift off. The gate metal running up the MESA side is depicted in Figure 3-21. The gate metal in contact with the InGaAs channel will form a complete sidewall-gate leakage path from gate to channel [59].

Although the metal-channel contact area is very small several orders smaller than the gate area, the low Schottky barrier height of metals with narrow band gap

InGaAs channel potentially results in a notable leakage whose path runs from the gate to the channel. The sidewall leakage current has been known to be the main reason of excessive gate leakage current and severely degrades the gate breakdown voltage. Both effects are not desirable in low noise and power device applications. In addition, sidewall leakages were found to worsen with higher doping, increased channel thickness, and increased x ($x > 0.53$) in $In_xGa_{1-x}As$ channel [59-61].

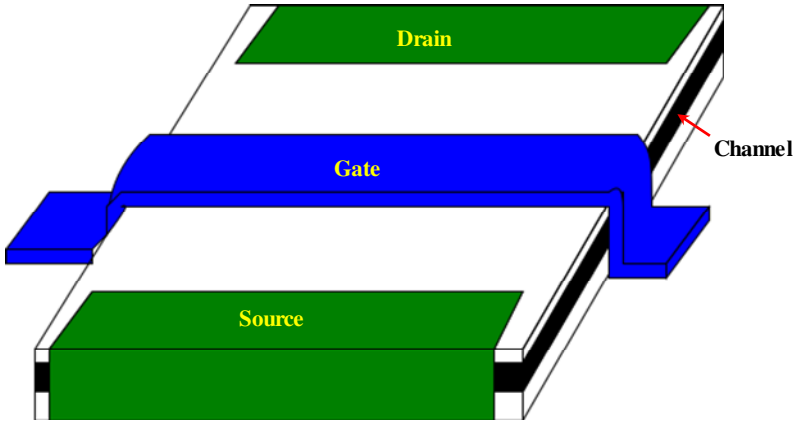



Figure 3-21 Graphical representation of MESA side wall. The Schottky gate running up the MESA will in contact with barrow band gap channel layer which complete the sidewall leakage path [60]

Bahl et al has proposed and demonstrated a new and simple one step technique, which is self-aligned to the MESA and requires no additional masks. The technique is not gate-length dependent, and works for MESAs in all crystallographic directions on the (100) surface [60].

Bahl et al had selectively recessed the exposed InGaAs channel using Succinic Acid:Hydrogen Peroxide solution without removing the MESA mask after orthophosporic etch. As a result, the high selectivity of the InGaAs channel etchant formed a cavity which the flowing gate metallization did not enter the cavity and remained isolated from the channel layer. The sidewall structure with the channel cavity is illustrated in Figure 3-22.

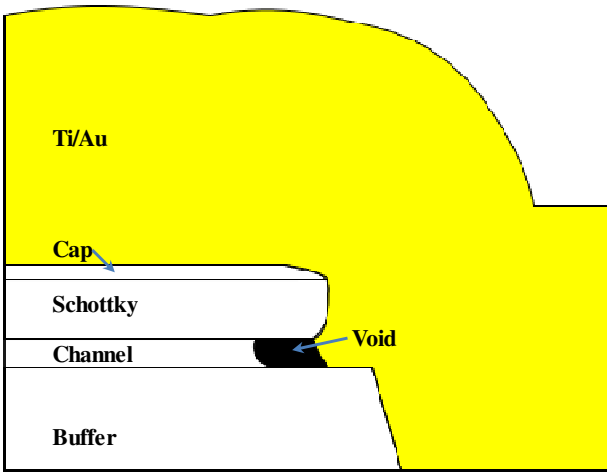



Figure 3-22 Side wall etch showing the channel cavity isolate the gate from InGaAs channel [60]

The same technique was used in the next experiment in our study. The same succinic acid composition as listed in Table 3-1 was used in this experiment. The aim of this experiment was to find out a suitable sidewall etching time to produce the lowest possible gate leakage current as well as a thermally stable gate.

The sample for this study was prepared using the XMBE #129 epitaxial layer. The structure of this layer has already been presented in the previous section. The sample was cleaned and the MESA pattern was transferred using conventional contact photolithography processes. After hard baking the resist mask, the MESA structure was etched down to the buffer layer using the orthophosporic acid solution, for about 150 nm etch depth. Using the same MESA mask, the sample was etched for different etching times of 5 and 10 minutes. To complete the comparisons, the Schottky diode measurements were also taken with no sidewall etching.

As a continuation to previous sintering study, the same sintering temperatures were used here as well. Since 200 °C was found to be the optimal sintering temperature, only this curing temperature is presented here. The sintering time was set to be 5 minutes. A higher sintering temperature or longer sintering time has proven to cause higher leakage, and will not be shown in this section. For comparison purpose, the data before heat treatment for all side wall etching cases were also measured.

Figure 3-23 shows the Schottky diode characteristic before heat treatment for 1 µm x 50 µm gate device. From the forward bias characteristics, the ideality factor (η) and

barrier high ($\phi_B$) for all devices were comparable. For the reverse biased characteristic, all devices had almost flat reverse currents, where the gate leakages are well below 100 µA/mm until -8 V reverse voltage.

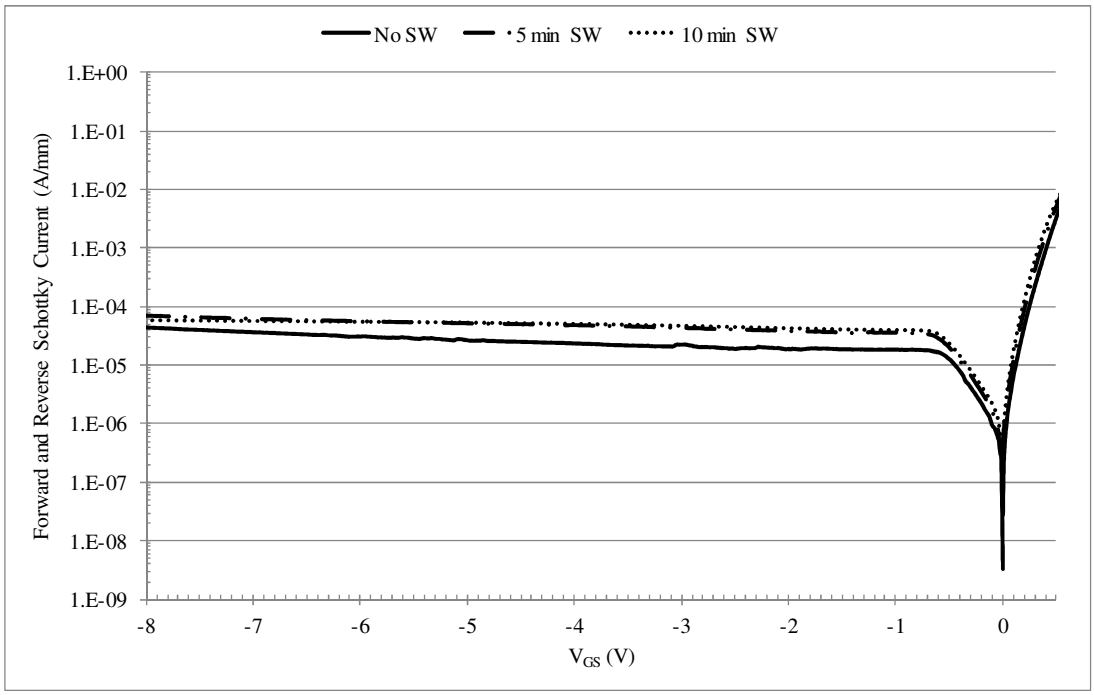



Figure 3-23 Schottky diode characteristic for 1 x 50 µm gate for all sidewall etch condition before heat treatment

By inspecting the leakage current right after gate evaporation and lift-off of 50/100 nm Ti/Au gate metallisation, the leakage of the device without sidewall etching is considerably lower than the leakage of the other two samples with 5 and 10 minutes side wall etching. The gate leakage at $V_{GS}$ = -8 V are 48 µA/mm for no sidewall etching, 57 µA/mm for 5 minutes sidewall etching and 56 µA/mm corresponding for 10 minutes sidewall etching. However, a curing temperature is always performed during the process flow to improve the adhesion between metal and semiconductor.

Figure 3-24 and Figure 3-25 show the diode characteristics of the devices for all etching time after sintering at 200 °C and 250 °C for 5 minutes. At 200 °C, the gate leakage for the device with no sidewall etching was consistent with that of the device before sintering. The gate leakage without sidewall is ~ 50 µA/mm. However, the gate leakage of the device with 5 minutes and 10 minutes sidewall etching show considerable improvement with the leakage reduced to 15 µA/mm, five times lower

than before sintering. The forward currents are comparable with those of the devices without sintering, demonstrating a negligible change in $\eta$ and $\phi_B$.

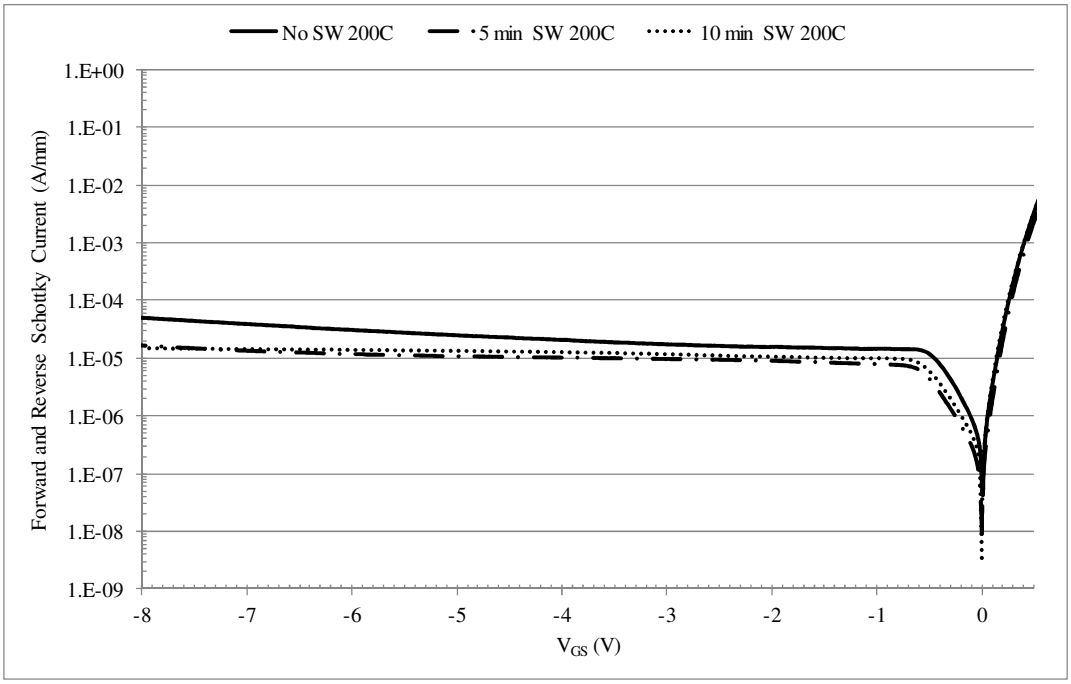



Figure 3-24 Schottky diode characteristic for 1 x 50 µm gate for all side wall etch condition at sintering temperature 200 °C for 5 minutes

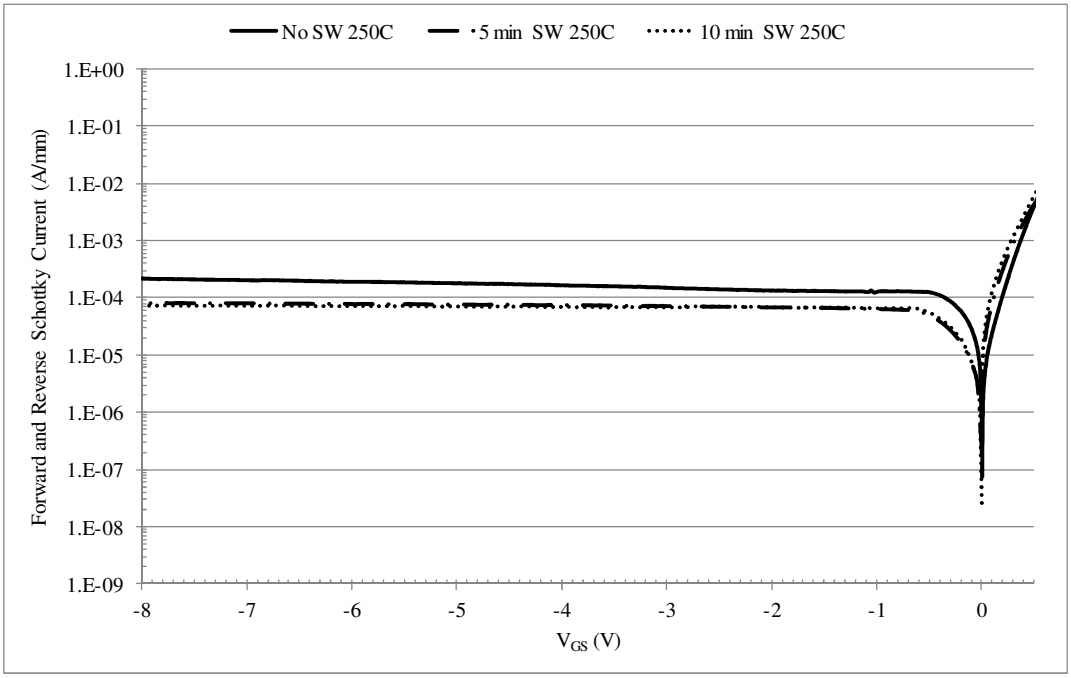



Figure 3-25 Schottky diode characteristic for 1 x 50 µm gate for all side wall etch condition at sintering temperature 250 °C for 5 minutes

However, a decreasing trend can be observed for a sintering temperature of 250 °C. The 5 and 10 minutes sidewall etching have a considerably higher gate leakage current, almost ten times higher. The diodes with no sidewall etching exhibited the worst leakage of 215 µA/mm at $V_{GS}$ = -8 V. For $V_{GS} \geq 0$ V, a less steep slope and higher saturation current ($I_S$) can be observed in the forward bias region implying a falling in ideality factor and $\phi_B$.

The sidewall etching and sintering data for the wider gate devices (1 x 400 µm) also showed similar trends: the Schottky leakage was lower for devices sintered at 200 °C, and higher for devices sintered at higher temperatures. The devices with 5 and 10 minutes sidewall etching also showed lower leakage and better thermal stability as compared to the devices with no sidewall etching.

From this work, two important findings can be observed:

a. The Schottky diodes are thermally stable at low sintering temperatures (T < 200 °C).
b. At sintering temperature 200 °C the sidewall etching reduces the gate leakage by almost 5 times compared with the gate leakage of the devices with no sidewall etching

Since the off-state Schottky gate leakage of the devices with the 5 and 10 minutes sidewall etching does not show significant changes in gate leakage current, a 10 minutes etching time was chosen for all subsequent processing for better sample uniformity. Similarly, and in agreement with previous experiments, excessive thermal energy can damage the metal-semiconductor junction, and therefore should be avoided. A sintering temperature of 200 °C is found to be optimum.

## 3.4 CONCLUSIONS

The effect of succinic acid mixtures and the etching profile of both InGaAs and InAlAs material have been studied in details. The experiments have shown that the doming effect during gate recess can be successfully controlled by etching the InGaAs material for longer times while reducing the over etching of InAlAs by

choosing a slower etching rate. The optimum chemical compositions are shown in Table 3-1, and the optimum gate recess time is 5 minutes. Thermal stability studies were conducted on 1 μm gate length devices, in which it has been found that high processing temperatures are not favoured and can deteriorate the Schottky barriers. The adoption of a sidewall etching technique, which isolates the metal gate and the channel, can significantly reduce the gate leakage during the sintering process. The optimal thermal budget in all the thermal stability studies was found to be 200 °C, with a sidewall etching time of 10 minutes.

The optimised chemical composition and thermal budget were applied in the fabrication of novel low noise and high breakdown pHEMTs for future high power and low noise applications as described in the next chapters.

# CHAPTER 4

# FABRICATION OF NOVEL LOW NOISE - HIGH BREAKDOWN InGaAs/InAlAs/InP pHEMT FOR SKA APPLICATIONS

## 4.1 INTRODUCTION

At present, InP based device technology represents the fastest semiconductor technology. Particularly in low noise applications, the High Electron Mobility Transistor (HEMT) together with advances in Monolithic Microwave Integrated Circuit (MMIC)technology, is driving future high volume, low cost, high performance millimetre-wave applications with high prospects [62]. Cut-off frequencies ($f_T$) in the THz range have been demonstrated with InP-based HEMT devices [63-65]. The unique and inherent properties of the carriers in a 2-DEG provide the device with high electron mobility and high sheet carrier density, making it the best device selection for many optoelectronic, magnetic and electronic applications. Among its applications, wireless and optical communications, passive imaging, and galactic scanning for next generation Square Kilometres Arrays are just a few.

Previously, a novel high-breakdown pHEMT was developed and fabricated on the University of Manchester to suit LNA designs for SKA receivers [54, 66]. In this work, the original epitaxial layer was further improved by precision control of band gap engineering, which resulted in better DC, RF, and noise performance of the pHEMT device. These improvements will be discussed in details in this chapter.

## 4.2 EPITAXIAL LAYER GROWTH

Here, two types of epilayer were studied (the high breakdown baseline XMBE #109 and enhanced low leakage-high breakdown VMBE #2100). Both epitaxial structures under study were grown using an in-house solid-source MBE on multiple wafers

RIBER V100H and V90H systems. The epilayer with prefix VMBE indicates growth in the V90H system, whilst prefix XMBE means the growth was done in the V100H system.

The epilayer profiles for both wafers are depicted in Figure 4-1. Both epilayers are based on InGaAs/InAlAs/InP structures. In general, from bottom to top, the epitaxial structures consist of an iron doped (semi insulating) InP substrate, an InAlAs buffer layer, a strained InGaAs channel, a Si doped modulation layer (δ-doped) in between the InAlAs spacer and Schottky barrier, and finally an undoped InGaAs cap at the top. Comparing the two epilayers, the thickness of each layer is approximately the same. However, the Schottky and spacer layers are made from different materials. For the baseline epilayer, a latticed matched $In_{0.52}Al_{0.48}As$ was grown while for the enhanced epilayer, a highly strained (tensile) epilayer was used. The advantage by using the strained Schottky layer is to both increase the band gap and raise the Schottky barrier height, which reduces the gate leakage tremendously as will be shown later.

| **Epilayer structure** | **XMBE #109 (Material-thickness)** | | **VMBE #2100 (Material-thickness)** | |
|---|---|---|---|---|
| Cap layer | $In_{0.53}Ga_{0.47}As$ | - 50 Å | $In_{0.53}Ga_{0.47}As$ | - 50 Å |
| Schottky layer | $In_{0.52}Al_{0.48}As$ | - 300 Å | $In_{0.30}Al_{0.70}As$ | - 300 Å |
| δ | | | | |
| Spacer layer | $In_{0.52}Al_{0.48}As$ | - 100 Å | $In_{0.30}Al_{0.70}As$ | - 100 Å |
| Channel layer | $In_{0.70}Ga_{0.30}As$ | - 140 Å | $In_{0.70}Ga_{0.30}As$ | - 160 Å |
| Buffer layer | $In_{0.52}Al_{0.48}As$ | - 4500 Å | $In_{0.52}Al_{0.48}As$ | - 4500 Å |
| Substrate | InP Fe doped | | InP Fe doped | |

Figure 4-1 Epitaxial layers for baseline epilayer(XMBE #109) and enhanced epilayer (VMBE #2100)

The carrier mobility and sheet carrier concentration in 2-DEG for both samples are prepared by Hall Effect measurement, and listed in Table 4-1. Hall Effect measurement is a valuable tool for semiconductor materials characterisation. The importance of Hall effect come after the necessity to determine accurately the

semiconductor material sheet resistance ($R_{sh}$), carrier density ($n_H$) and carrier mobility ($\mu_H$). This characterisation technique becomes an essential in the semiconductor industry and research laboratories because of relatively simple method, low cost, and fast turnaround time.

The detailed information about the steps involved in Hall effect measurement is already reported by Bouluku [67]. In general, Hall Effect can be observed when a small transverse voltage (Hall voltage) appeared across a current-carrying thin metal strip in an applied magnetic field (principle of Lorentz force). All samples are prepared using the Van der Pauw four contact method at room temperature (300 K) and low temperature (77 K) using a current of 1 mA with and without the influence of magnetic field of 0.088 T. The extraction of Hall mobility and the carrier sheet density are done automatically using software developed by our group. For all the samples reported in this thesis, the Hall effect measurement and data preparation fall under the responsibility of the Material Growth Team which their functions will be briefly described in the next section.

As in Table 4-1, the carrier mobilities ($\mu_H$) in both channels are approximately the same since similar material is used in both structures. However, the sheet carrier concentration ($n_H$) in the enhanced epilayer is almost 1.5 times higher than the baseline epilayer.

Table 4-1 Hall Measurement data at Room Temperature (300 K) and 77 K

| **Hall Data** | **XMBE #109** | **VMBE #2100** |
|---|---|---|
| Sheet Carrier Concentration ($n_H$) at 300 K / 77 K (x $10^{12}$ $cm^{-2}$) | 1.74 / 2.06 | 2.50 / 2.60 |
| Hall Mobility ($\mu_H$) at 300 K / 77 K ($cm^2$/V.s) | 12,850 / 48,800 | 12,982 / 46,390 |

Simulated energy band diagrams and carrier densities in the channel using the WinGreen simulator [68] are shown in Figure 4-2. WinGreen simulator is based on real-time Green's functions [69] which provides a quantum mechanical approach in

laterally extended layered heterostructures. In WinGreen, the Coulombic interaction between charged particles is calculated via Hartree self consistent single-particle potential [70], by employing the Poisson's equation [71] and the charge density from the Green's functions. This tight binding approach provides an accurate model of the heterointerfaces.

The band diagrams were simulated at Room Temperature and zero biasing. As can be seen in the figure, given that the 2-DEG and buffer layers for both structures are made from the similar epitaxial material of approximately the same thickness, their simulated band diagrams are matched to each other. However, a large Schottky barrier is seen for VMBE #2100 between the Schottky interface and gate metal, which restrains electrons from crossing the junction (especially by thermionic emission), and therefore devices made from this epilayer exhibit lower junction leakage. VMBE #2100 shows higher carrier concentration in the 2-DEG due to the larger band discontinuity resulting in a larger amount of trapped carriers from the modulation doped layer falling into the much deeper quantum well than XMBE #109. More advantages of this epilayer structure will be discussed further in the DC characteristic section.

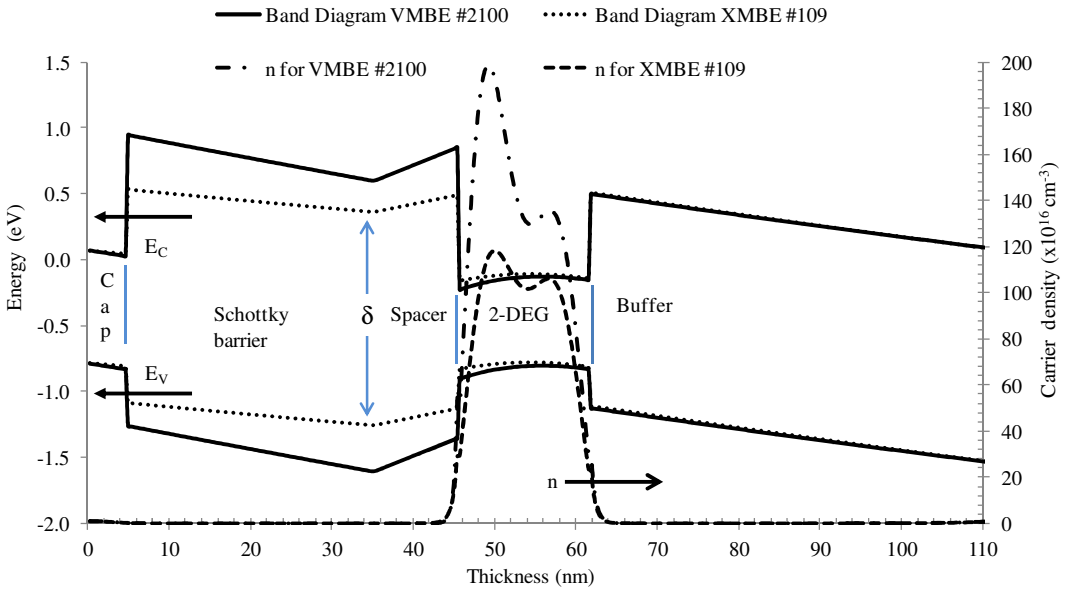



Figure 4-2 Simulated energy band diagrams and carrier density in channel for both epilayers. The energy band and carrier density are made overlapped to each other for comparison purpose.

## 4.3 FABRICATION PROCESS

Figure 4-3 shows the complete LNA workflow in Microelectronic and Nanostructures (M&N) Group at the UoM. The tasks in the workflow are dedicated to three sub-groups, namely Material Growth Team, Fabrication Team and Modelling Team.

The task begins with the various material growth using MBE by the Material Growth Team. The complete epitaxial layers will undergo several material characterisation such as C-V and Hall effect measurements before it is handed to the Fabrication Team for the next task of device fabrication..

The main content of this thesis is for the reporting of the tasks completed by the Fabrication Team. The work begins with device fabrication and the completed devices are characterised using DC and RF measurements. The measured data are then used by the Modelling Team for their linear and nonlinear device modelling. Next, the modelled devices will be used in the circuit design and the Modelling Team will come out with the circuit layout for each of their designs. The Fabrication team will rearrange the circuit layout, adding alignment marks and Process Control Monitoring (PCM) structures in the final mask layout.

The workflow continues with the fabrication of the circuits using the generated mask, and at the end of the workflow, the complete circuits are characterised and measured. Most of the circuit characterisation tasks are done in UoM, and some of them are being outsourced to Spain due to limitations in our equipments.

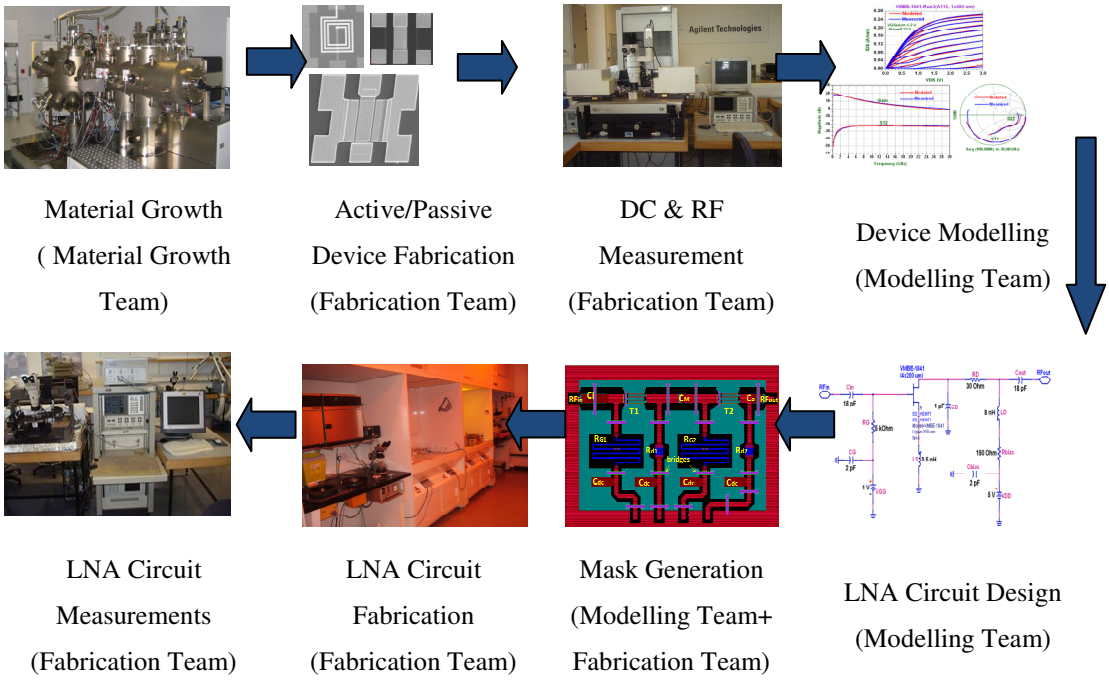



Figure 4-3 The complete workflow process at the UoM. Shown in the brackets are the sub-group that are responsible for the task.

In this chapter, the devices were prepared until device fabrication and characterisation steps. An all-optical lithography process was used to fabricate the devices by following the pHEMT's fabrication steps developed at the UoM. The fabrication steps are illustrated in Figure 4-4. Together with the optimised gate recess process, the newly developed epitaxial layer shows a better DC and RF performances than the previously fabricated baseline transistors as shall be seen later.

The process started with sample cleaning using Trichloroethylene, Acetone, and IPA from organic and inorganic substances or other types of particles when transporting the samples from the wafer growth area to the fabrication laboratory. The devices' active area was then defined by MESA isolation technique using a non-selective wet etch of orthophosporic solution ($H_3PO_4$:$H_2O_2$:$H_2O$) of 3:1:50 composition. A vertical depth of 160 nm was etched away into the buffer layer. With the same photoresist mask, the sidewall etching was performed using high selectivity succinic etching to isolate the gate from the channel in later fabrication steps.

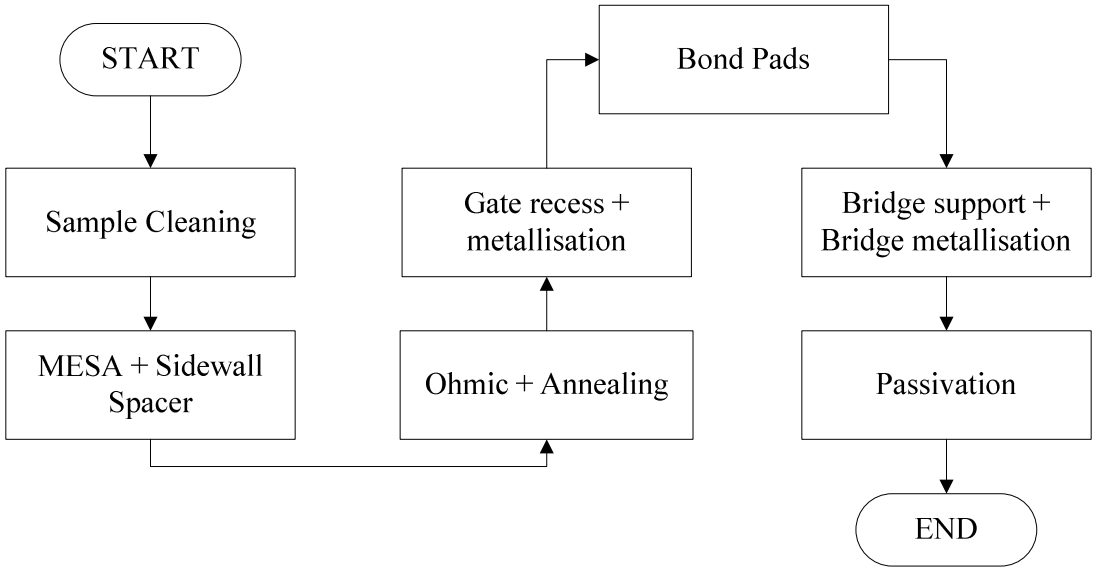



Figure 4-4 Conventional pHEMT process flow developed at UoM

Then the source and drain Ohmic contacts were formed by thermal evaporation and lift-off of AuGe/Au. The Ohmic contact to the 2-DEG was then improved by means of heat treatment. The gate recess process was subsequently performed using the optimised succinic acid composition as described in Chapter 3. Here, AZnLOF 2070 is used as the gate-level photoresist opening which also acts as an etching mask. The gate recess process will remove the 50 Å InGaAs cap layer and shape the 1 µm footprint for the planar gate . The planar gate was deposited by thermal evaporation and lift-off of 50/400 nm thickness of Ti/Au metallisation scheme.

The same metallisation scheme was used for the probing pads, facilitating on-wafer DC and RF measurements. Next, a SF11 bridge support was fabricated to act as source level bridging for the multi-finger devices. SF11 is a type of resist that is based on Polymethylglutarimide (PMGI) polymer. SF11 has the property of high thermal stability and is therefore compatible with our LNA processing. In addition to that, SF11 has superior adhesion to GaAs, InP and many other III-V materials and is virtually insoluble in typical photoresist solvents which determined its suitability in our processing steps [72, 73]. In our process, SF11 with 1 µm thickness is used as a support for the metal bridging.

The fabrication was completed with active area's passivation for proper RF shielding. The details of each fabrication steps are listed in Appendix A. A picture of

a complete four gate fingers with 200 µm width (4 x 200 µm) transistor is shown in Figure 4-5.

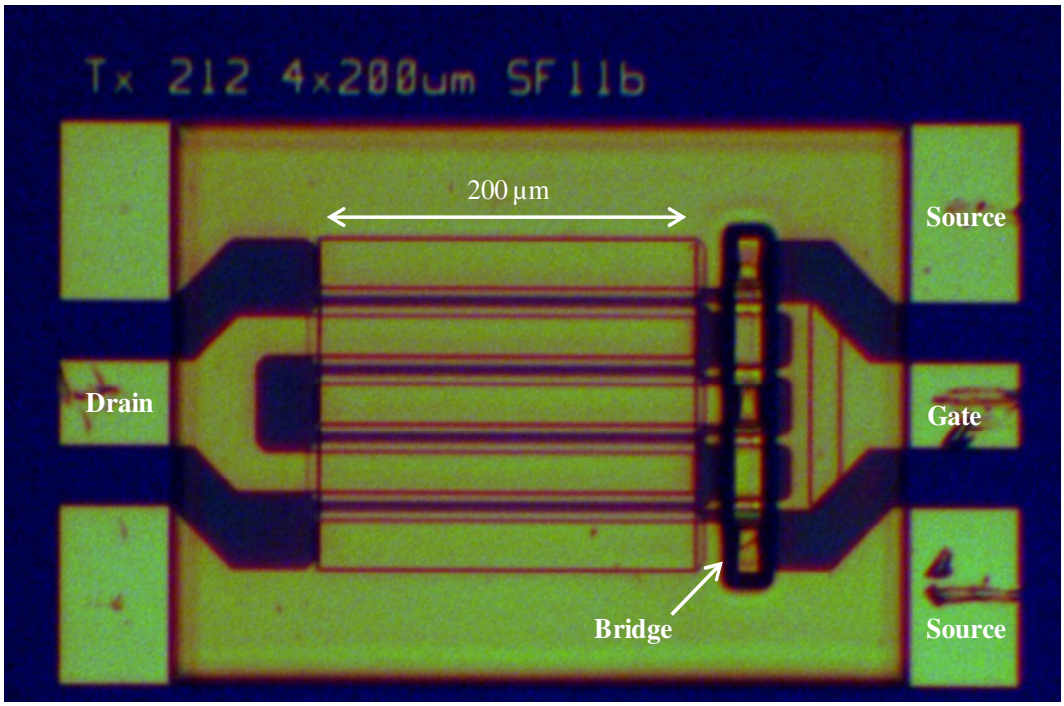



Figure 4-5 An illustration of a complete bridged 4 x 200 µm device (1 µm gate length)

## 4.4 DC CHARACTERISTICS

The devices under investigation are fabricated using 1 µm gate technology developed by UoM and have 2-1-2 µm source-drain separation. At the Ohmic step, the contact resistance values extracted from Transfer Length Method (TLM) measurements using four-point probe system are listed in Table 4-2. The tabulated TLM data were the average values from five TLM ladders located at different locations on the sample.

As oppose to XMBE #109, the Ohmic contacts for the enhanced epilayer XMBE #2100 are evaporated with thinner metal with thickness of 50 nm of AuGe and 100 nm of Au (hereafter will be notated as 50/100 nm of AuGe/Au), whereas the Ohmic thickness for XMBE #109 is 50/400 nm of AuGe/Au. To a first degree, this is for cost effective measure where the thickness of Au is reduced by 75%. The only perceived observation for the thin metallisation scheme is that more heat is needed to

allow the metal diffusion to reach 2-DEG layer. Thus, the sample is heated for another 90 s in 290 °C and $N_2$ ambient after the first sintering for 90 s at 280 °C. The sintering time and temperature for XMBE #109 was only for 90 s and 280 °C. By comparing the contact resistance values, the thin metallisation scheme has demonstrated low and comparable $R_C$ with that of the thick metallisation scheme while saving over 75% of the Au metal.

Table 4-2 Sheet resistances ($R_{sh}$) and Contact residences ($R_C$) of each sample from TLM

| **Sample ID** | **AuGe/Au Metallisation Scheme (nm)** | **Contact resistance, $R_C$ (Ω.mm)** | **Sheet resistance, $R_{sh}$ (Ω/ ) Hall/TLM** |
|---|---|---|---|
| XMBE #109 | 50/400 | 0.18 | 280/238 |
| VMBE #2100 | 50/100 | 0.16 | 193/172 |

From this point on, all presented DC data were measured using an HP4142 parameter analyser. In this chapter, four devices were measured. The results are taken from the best device, while the rest fell within variation of 10% throughout the sample.

The extrapolation for determining $V_{th}$ point is illustrated in Figure 4-6, from which a $V_{th}$ of -1.28 V for XMBE #109 and -1.18 V for VMBE #2100 are extracted. Since the gate to channel distance for both samples are the same (300 Å), the small shift in $V_{th}$ can be explained by the different Schottky barrier height values. However, this small 6% difference is within the processing error margin and the variation can be neglected.

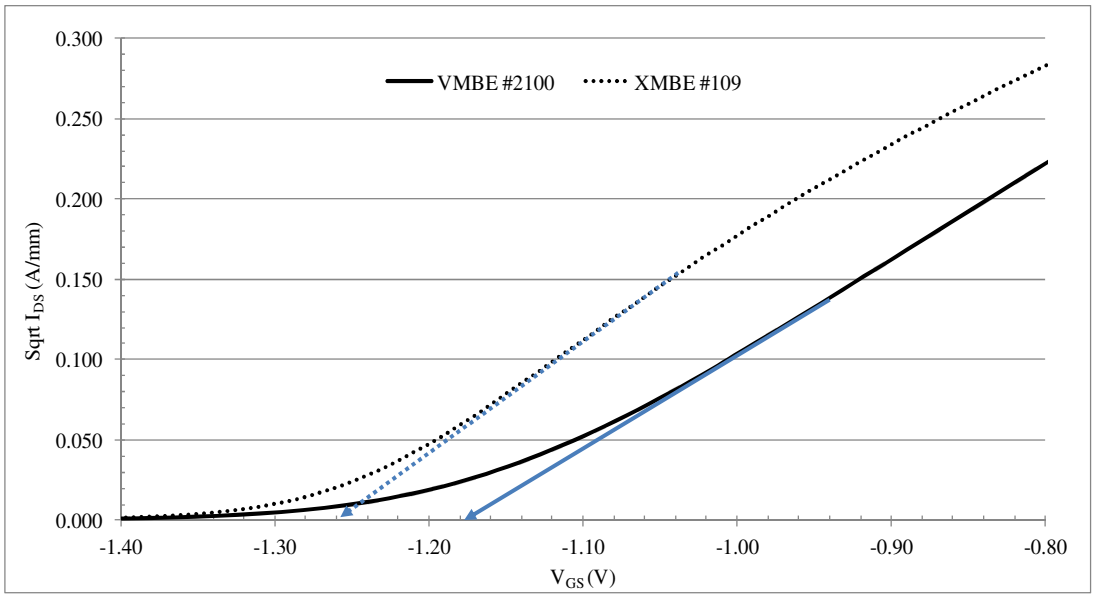



Figure 4-6 Determination of $V_{th}$ . XMBE #109 = -1.26 V and VMBE #2100 = -1.18 V

The Schottky characteristics for both epilayers are shown in Figure 4-7. In general, the reverse Schottky gate leakage for both epilayers increases as the reverse gate voltage ($V_{GS}$) is increased. The advantage of the larger barrier height can already been seen here where the reverse bias gate leakage for VMBE #2100 exhibits lower reverse current than XMBE #109. For larger Schottky barrier height epitaxial layer (VMBE #2100), only small amount of carriers are having energy larger than the barrier height at metal-semiconductor contact, which shown by the lower gate leakage current.

In order to avoid the risk of burning the devices, the Schottky measurement were stopped at - 10 V and - 6 V for VMBE #2100 and XMBE #109, respectively. However, the off-state breakdown voltage using the same channel material had been shown to be over -14 V in [49], which is much higher than the usual values of - 4 V or less for conventional lattice matched InGaAs-InAlAs pHEMT, also demonstrated in the same publication.

Nevertheless, the extrapolated data beyond the measured values has resulted in excellent high breakdown voltages of over -12.4 V in both type of epitaxial layers. Here, the breakdown voltage is defined as the voltage where the reverse gate current value is equal to 1 mA/mm.

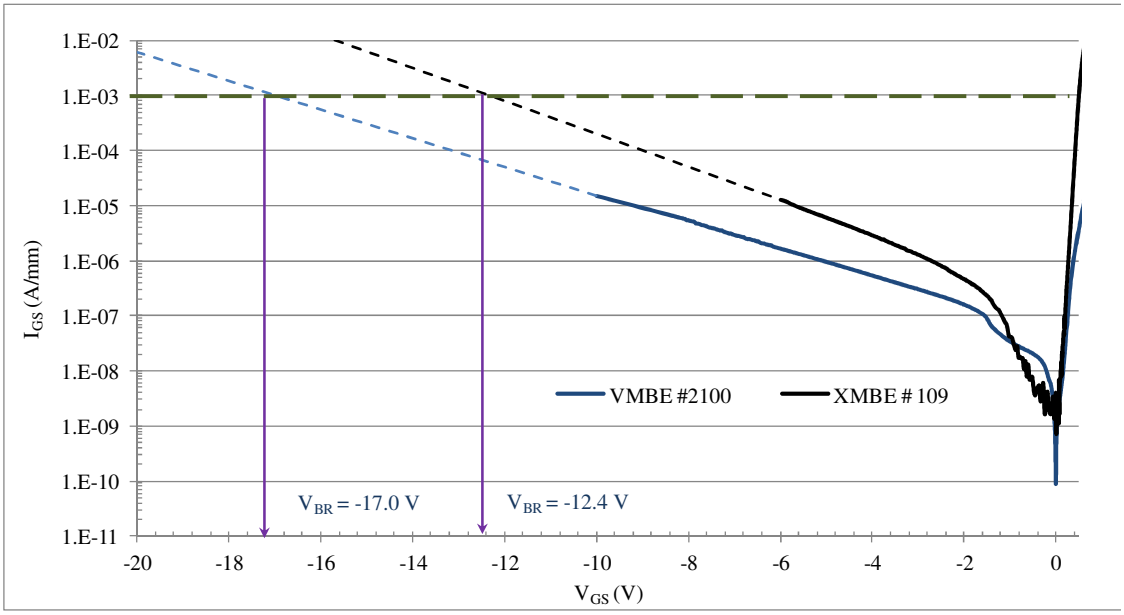



Figure 4-7 Schottky gate leakage for XMBE #109 (black line) and VMBE #2100 (blue line). The dotted black and blue lines are the extrapolation for XMBE #109 and VMBE #2100, respectively.. Shown in the same figure, the 1 mA/mm breakdown line (dotted green line)

From the forward bias curves, the ideality factor ($\eta$) and barrier height ($\phi_B$) can be extracted. The XMBE #109 devices have a $\eta$ of 1.28 and $\phi_B$ of 0.61 eV. Similarly, the extracted values for VMBE #2100 are a $\eta$ of 1.67 and $\phi_B$ of 1.00 eV. The much higher $\phi_B$ value is as expected from the high band gap of $In_{0.3}Al_{0.7}As$ (~2 eV) compared with that of lattice matched $In_{0.52}Al_{0.48}As$ (~1.45 eV) as already observed in the band diagram simulations shown in Figure 4-2.

Figure 4-8 illustrates the bell shape on-state leakage at different $V_{DS}$ biasing for both epitaxial layers. Here, $V_{DS}$ is varied from 1 to 2 V, with 0.25 V steps. Below $V_{th}$ values, the devices are off and the leakage is mostly due to electron tunnelling through the Schottky barrier. The lower leakage observed for VMBE #2100 is due to the much higher barrier seen by the carriers at the Schottky interface. As shown in the inset of Figure 4-8 , at low $V_{DS}$ ($V_{DS}$ = 1 V), the leakage for VMBE #2100 at $V_{GS}$ = -2.5 V is more than seven times lower than that of VMBE #109, exhibiting a large reduction from -2.3 µA/mm to -0.3 µA/mm for XMBE #109 and VMBE #2100 respectively.

Nevertheless, when the $V_{DS}$ biasing is increased beyond 1 V, impact ionisation starts to occur in the highly strained channel. However, below the $V_{th}$ value, the device is off, and no impact ionisation occurs in the channel. Starting with $V_{GS}$ approximately equal to the $V_{th}$ value, the device begins to turn on and impact ionisation starts in in the channel. The electrons injected into the channel by tunnelling are swept by the high electric field between the gate and drain terminals where the impact ionisation occurs. The impact ionisation produces electron-hole pairs, and the holes created in this process will be swept towards the most negatively biased terminal (the gate). As a result, there will be an increased in the gate current ($I_{GS}$) as observed in Figure 4-8 [74].

The remaining hump characteristic (peak and decline) of the reverse gate current due to generation of holes depends on the biasing of the gate terminal. When the $V_{GS}$ biasing is approaching 0 V, the carrier concentration is high, but the lower electric field reduces the impact ionization.

By referring to Figure 4-8, the newly improved epilayer however, still maintains a much lower overall on-state leakage than a typical 0.15 µm x 40 µm gate InP-based HEMT as reported in [74]. The lower gate leakage properties enable the fabrication of large geometry devices for low noise applications, where it is almost impossible to achieve with leakier devices.

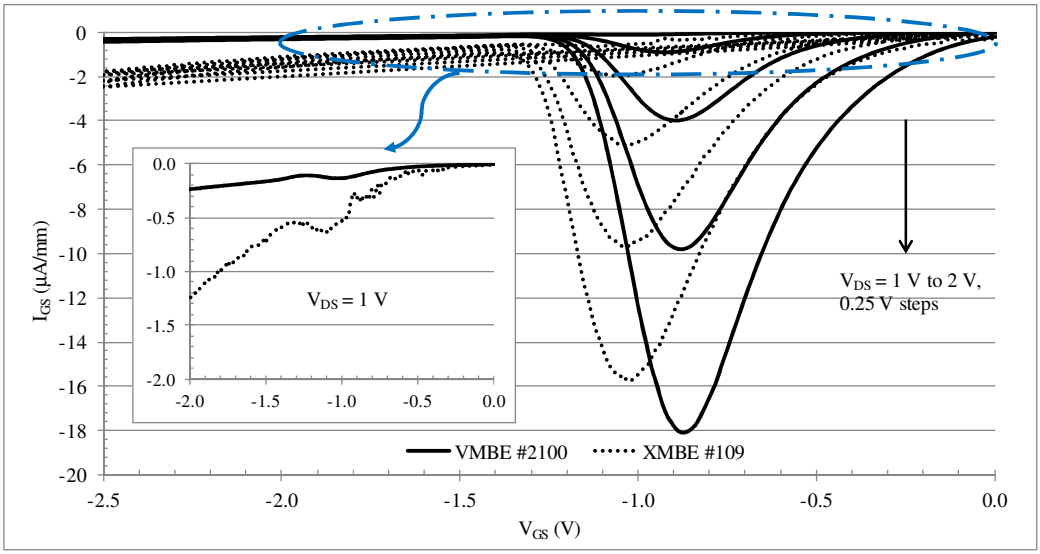
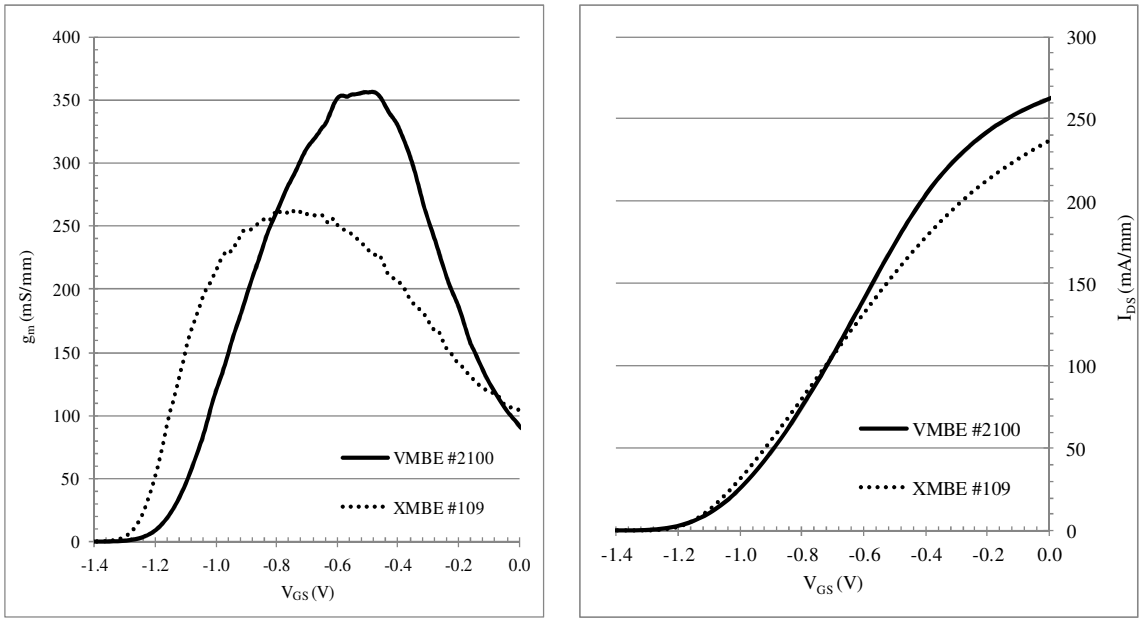



Figure 4-8 Bell shape curve for both epitaxial structures at $V_{DS}$ = 1 to 2 V, steps 0.25 V. Inset, on-state leakage at $V_{DS}$ = 1 V

The on-state leakage at $V_{DS}$= 1 V is shown as an inset in Figure 4.7. Unlike XMBE #109, only a very small leakage due impact ionisation is observed in VMBE #2100. The maximum leakage due impact ionisation for VMBE #2100 is -0.14 µA/mm at $V_{GS}$ ~ -1.0 V, which is almost five times lower than that of XMBE #109 where the maximum leakage is -0.64 µA/mm at the same $V_{GS}$ value. Thus, this biasing point will be used in the LNA designs described in Chapter 6.

The transconductance ($g_m$) curves and the corresponding $I_{DS}$ vs. $V_{GS}$ curve at $V_{DS}$ = 1 V for both epilayer are depicted in Figure 4-9. As can be seen in the figure, the slope of the $I_{DS}$-$V_{GS}$ for VMBE #2100 is much steeper than that of XMBE #109, corresponding to rapid change of current over voltage change. The equivalent peak $g_m$ ($g_{m\_max}$) for VMBE #2100 is 355 mS/mm when $V_{GS}$ = -0.50 V whereas the maximum $g_m$ is 262 mS/mm when $V_{GS}$ = 0.76 V for XMBE #109.




(a) (b)

Figure 4-9 Transconductance (a) and corresponding $I_{DS}$ curve (b) at $V_{DS}$ = 1 V.

As initially indicated in Figure 4-9, the output current density for VMBE #2100 is higher than that of XMBE #109. The complete output current densities at various $V_{GS}$ bias points are shown in Figure 4-10, which indicates higher output current can

be obtained from VMBE #2100 epitaxial layer. As depicted in the energy band diagram (Figure 4-2), it is advantageous to have a large carrier density in the channel where more electrons can contribute to current conduction, and thus increase the $I_{DS}$ output current.

The maximum output current at $V_{GS}$ = 0 V ($I_{dss}$) of 344 mA/mm is observed for VMBE #2100, which is a 30% improvement over that of the $I_{dss}$ of 266 mA/mm for XMBE #109. However, the pinch-off points for both epilayers are almost the same since both samples have almost the same $V_{th}$.

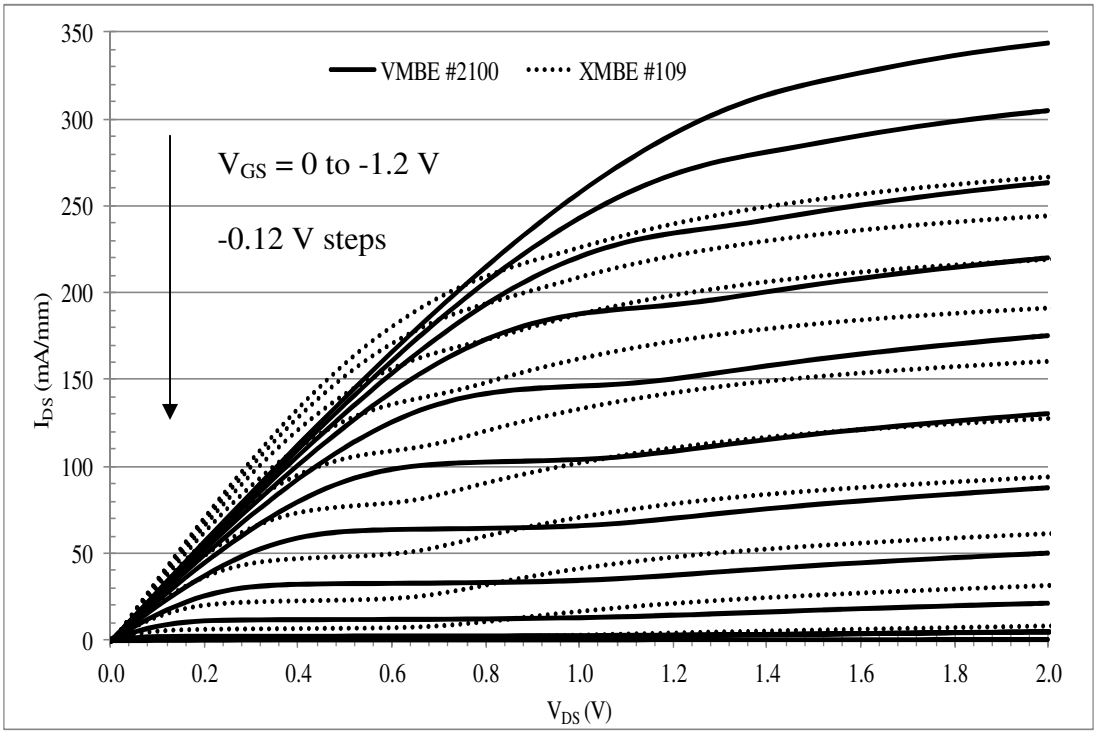



Figure 4-10 I-V outputs characteristic for both samples. Both devices were biased at $V_{GS}$ from 0 V to – 1.2 V with step size of -0.12 V (label the curves, which one is 0V and which one is -1.2V)

Note also that the kink effect is much more reduced in VMBE #2100 because of the larger band gap and increased conduction band discontinuity.

## 4.5 RF CHARACTERISTICS

To complete the device characterisation, RF measurements were also performed on the devices. Here, the microwave performances were analysed using an Anritsu Vector Network Analyser (VNA), which takes a small signal S-parameters analysis from 40 MHz to 40 GHz. The measurement results are illustrated in Figure 4-11. By extracting the value of the Unity Current Gain (h21) crossing at 0 dB line, a cutoff frequency ($f_T$) of ~ 25 GHz was obtained for both the devices. The maximum oscillation frequencies ($f_{max}$) for all devices are between 30 to 40 GHz depending on the devices' total gate width size (with larger gate width devices having smaller $f_{max}$ as would be expected because of the increased parasitic in the large area devices). The RF biasing for the devices are listed in Table 4-3 .

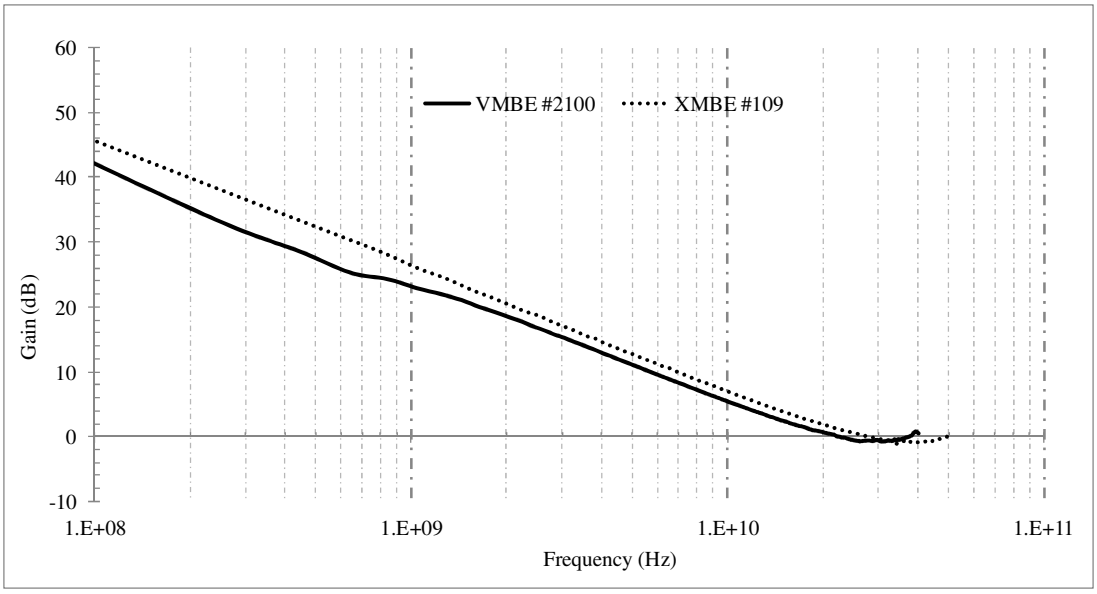



Figure 4-11 Unity current gain (h21) at $V_{DS}$ = 1 V

Table 4-3 Microwave biasing for XMBE #109 and VMBE # 2100

| RF biasing | XMBE #109 | VMBE # 2100 |
|---|---|---|
| VDS (V) | 1.00 | 1.00 |
| VGS (V) | -0.84 | -0.85 |
| IDS (V) | 14.03 | 36.18 |

## 4.6 NOISE CHARACTERISTICS

The Noise Figure (*NF*) is a number used to measure the level of noise generated from an active device when RF signal is applied. A large value of *NF* means that the original signal is badly distorted to the extent that the original signal may not be recoverable. Normally, the *NF* is measured as a function of source impedance presented to the device.

Ideally, the standard source impedance of a matched RF circuit is 50 Ω where the device is at or near its minimum possible *NF* value. However, due to impedance mismatch, the minimum *NF* point will shift to some other impedance point. The value of the minimum possible *NF* at this impedance point is called the minimum noise figure ($NF_{min}$), and the real and imaginary impedance points are called the complex optimum reflection coefficient ($\Gamma_{opt}$) [75].

The relationship between *NF* at any impedance and other noise parameters on a two-port network is expressed by Equation 4-1 [76, 77].

$$NF = NF_{min} + \frac{4R_n}{Z_o} * \frac{\left|\Gamma_S - \Gamma_{opt}\right|^2}{\left|1 + \Gamma_{opt}\right|^2 * (1 - |\Gamma_S|^2)} \qquad \text{Equation 4-1}$$

Where the four noise parameters are:-

$\Gamma_S$ = complex source reflection coefficient,

$\Gamma_{opt}$ = complex optimum reflection coefficient,

$NF_{min}$ = minimum noise figures when $\Gamma_S = \Gamma_{opt}$ in dB,

$R_n$ = the noise resistance,

$Z_o$ = the system impedance (50 Ω).

From the equation, $R_n$ plays a noticeably important role in determining the *NF* of the device. The second term will never be zero in practice as $\Gamma_S \neq \Gamma_{opt}$, and the mismatch between *NF* and $NF_{min}$ can be reduced if $R_n$ is reduced , which means that *NF* does not change much as the impedance moves away from $\Gamma_{opt}$. By using large gate dimensions however, the value of $R_n$ can be reduced [78]. From the device modelling of a 4 x 200 µm gate periphery using an equivalent circuit presented in [79], the $R_n$

is 5 Ω for XMBE #109 and 2 Ω for VMBE #2100. With the superior DC, RF, and noise performances of VMBE #2100, devices with gate geometry of 4 x 200 μm are currently being used in the design and fabrication of broadband Monolithic Microwave Integrated Circuits (MMICs) low-noise amplifier. The results will be discussed in details in Chapter 6.

## 4.7 CONCLUSIONS

In this chapter, an enhancement epitaxial layer based on InGaAs/InAlAs material systems have been successfully fabricated and characterised. Through careful layer growth and band gap engineering, improvements in DC, RF, and noise performances have been observed in this newly improved high breakdown epitaxy system as compared with the previously fabricated epitaxial layer structures. The extremely low leakage and low noise characteristics have enabled them to be implemented as the active device in Low Noise Amplifiers circuit design. A large decrease of noise resistance as a result of the larger transconductance of the large peripheral devices, facilitates them in the implementation of high speed circuit including broadband low-frequency systems, and makes them promising candidates for post Si CMOS era for highly scaled devices.

# CHAPTER 5

# FABRICATION OF IMPROVED DOUBLE δ-DOPED InGaAs/InAlAs pHEMTs FOR POWER APPLICATION USING FIELD PLATE TECHNOLOGY

## 5.1 INTRODUCTION

Amongst all III-V compound semiconductors, the InGaAs-InAlAs materials system has optimum band structure and transport properties making it the material of choice in many optoelectronics, magnetic and electronic applications. Indeed, THz range cut off frequencies have already been reported [63], and this system is road mapped in the sub-22 nm electronics. The InGaAs-InAlAs pseudomorphic High Electron Mobility Transistor (pHEMT) devices have also carved an important role in low noise applications using the advantages listed above.

However, the conventional low-noise InP pHEMTs currently used in both low-noise amplifier (LNA) and power amplifier (PA) designs suffer from inherently low gate breakdown voltages ($V_{BR}$) almost regardless of gate length [80]. The typical InP pHEMT's $V_{BR}$ is ~6 V or lower, which compromises and complicates LNA designs for rugged, room-temperature radio astronomy (RA) applications.

The poor $V_{BR}$ has generally been attributed to the carriers (electrons) that enter the low band gap channel by thermionic field emission from the gate terminal and preserve their energy by impact ionisation [81]. Therefore, if both mechanisms are reduced, the devices will have the advantage of high $V_{BR}$. One way to minimise the thermionic field emission is by raising the barrier height of the Schottky contact. Advances in band gap engineering, which allows substitution of wider ternary or quaternary compounds, as the Schottky barrier layer, have successfully reduced the effect of thermionic emission. Indeed, this advanced material engineering is also being used to reduce the impact ionisation by constructing wider band gap materials

in the channel. What is more, the effect of impact ionisation can also be reduced by lowering the peak electric field at the gate metal edge on the drain side of the device.

Attempts at increasing the pinched-off breakdown voltage have been reported over the years, and have been successful in raising the $V_{BR}$ to 10 V, most of these approaches were compromised by a severe drop in the unity current gain cut-off frequency, $f_T$ (and, hence, an increase in noise), and a drop in current-driving capability [82-85]. Furthermore, the low Schottky barrier formed by the common gate metals on InGaAs usually leads to a side-gate-leakage current with a consequent low breakdown voltage [59]. Therefore, it is clear that the problem of the reduced $V_{BR}$ is far from being solved.

The aim of this work is thus to improve the device breakdown voltages, and, at the same time, uphold the excellent DC and RF performances of the devices. To this effect, two different approaches have been applied in this study: (i) an engineered high-breakdown epitaxial layer structure and (ii) a field modulating structure, leading to robust high breakdown devices that could be of interest for high-efficiency millimetre-wave PAs, as well as robust LNAs that can work with minimal protection circuits. By combining these methods, the resulting devices have led to a novel high frequency and high breakdown double delta-doped (δ-doped) InGaAs/InAlAs pHEMTs are reported here.

## 5.2 MATERIAL GROWTH

Two different types of epitaxial layer are grown for this study. The epilayers are :

a. A conventional indium-rich InGaAs channel epilayer, XMBE #171 and
b. An improved double δ-doped epilayer, XMBE #131.

The epitaxial layer profiles of both samples are summarised in Figure 5-1 and Figure 5-2, respectively. From bottom to top, a lattice match InAlAs interfacial layer was grown on top of both InP substrates. For the conventional epitaxial structure, a highly strained $In_{0.7}Ga_{0.3}As$ layer was then grown on top of the buffer layer for the convenience of a deeper quantum well in this narrow band gap channel material. The

carriers are supplied from a δ-doped layer located on top of a 50 Å lattice matched InAlAs spacer layer. Next, the Schottky and Cap layers were made from an undoped lattice matched InAlAs and InGaAs material of 300 Å and 50 Å thicknesses respectively.

A better confinement of carriers in quantum well is attained by means of two δ-doped layer structure. In the improved epitaxial layer, a narrow band gap $In_{0.7}Ga_{0.3}As$ channel is bounded by two δ-doped layers and two 100 Å lattice matched InAlAs spacer layers side-to-side. Its Schottky barrier layer is made from lattice matched InAlAs at half the thickness than the conventional baseline structure (refer to XMBE #109 epitaxial layer profiles). Similar to the conventional structure, the cap is made from a 50 Å lattice matched InGaAs material.

| | |
|---|---|
| $In_{0.53}Ga_{0.47}As$ | Cap layer (50 Å) |
| $In_{0.52}Al_{0.48}As$ | Schottky layer (300 Å) |
| | δ |
| $In_{0.52}Al_{0.48}As$ | Spacer layer (50 Å) |
| $In_{0.7}Ga_{0.3}As$ | Channel layer (140 Å) |
| $In_{0.52}Al_{0.48}As$ | Buffer layer (4500 Å) |
| InP | Substrate |

Figure 5-1 Epitaxial layer of conventional InGaAs/InAlAs pHEMTs epilayer, XMBE #171(thickness not to scale)

| | |
|---|---|
| $In_{0.53}Ga_{0.47}As$ | Cap layer (50 Å) |
| $In_{0.52}Al_{0.48}As$ | Schottky layer (150 Å) |
| | $\delta_2$ |
| $In_{0.52}Al_{0.48}As$ | Spacer layer $_2$ (100 Å) |
| $In_{0.7}Ga_{0.3}As$ | Channel layer (150 Å) |
| $In_{0.52}Al_{0.48}As$ | Spacer layer $_1$ (100 Å) |
| | $\delta_1$ |
| $In_{0.52}Al_{0.48}As$ | Buffer layer (4500 Å) |
| InP | Substrate |

Figure 5-2 Epitaxial layer of improved double δ-doped InGaAs/InAlAs pHEMTs epilayer, XMBE #131 (thickness not to scale)

For comparison purposes, the Hall measurement data for both materials at 300 K (Room Temperature) and 77 K are shown in Table 4-1. The sheet carrier

concentration in 2-DEG for XMBE #171 (conventional pHEMTs epilayer) is higher than XMBE #131 (improved pHEMT epilayer) due to its thinner spacer layer. This is, however, in exchange for lower barrier thickness seen by the carriers in the quantum well, which, ultimately, will increase the gate leakage. The high carrier mobility seen in the XMBE #131 channel is primarily due to the lower electron-donor Columbic interaction from the δ-doped layer due its thicker spacer layer.

Table 5-1 Hall Measurements at Room Temperature (300 K) and 77 K for XMBE #171 and XMBE #131

| **Hall Data** | **XMBE #171** | **XMBE #131** |
|---|---|---|
| Sheet Carrier Concentration ($n_H$) at 300 K / 77 K (x $10^{12}$ $cm^{-2}$) | 3.16 / 3.56 | 2.40 / 2.50 |
| Hall Mobility ($\mu_H$) at 300 K / 77 K ($cm^2$/V.s) | 10,653 / 24,649 | 13,896 / 47,829 |

To complete the comparisons, the advantages of using the improved epitaxial layer can be seen in the band diagram simulation using WinGreen®. The graphical representation of the energy band diagram for both structures are shown in Figure 5-3 and Figure 5-4. It can clearly be seen that the carrier confinement in the quantum well in XMBE #131 is better than in XMBE #171, where the carriers are trapped in the almost square shape quantum well in XMBE #131 as compared to a triangular shape well at XMBE #171.

The barrier heights of XMBE #131 and XMBE #171 are similar, due to the fact that the materials used for both Schottky layers are the same. Despite a higher transconductance ($g_m$), the current drivability of the XMBE #131 device is seen to be lower, as a result of a thinner gate to channel distance.

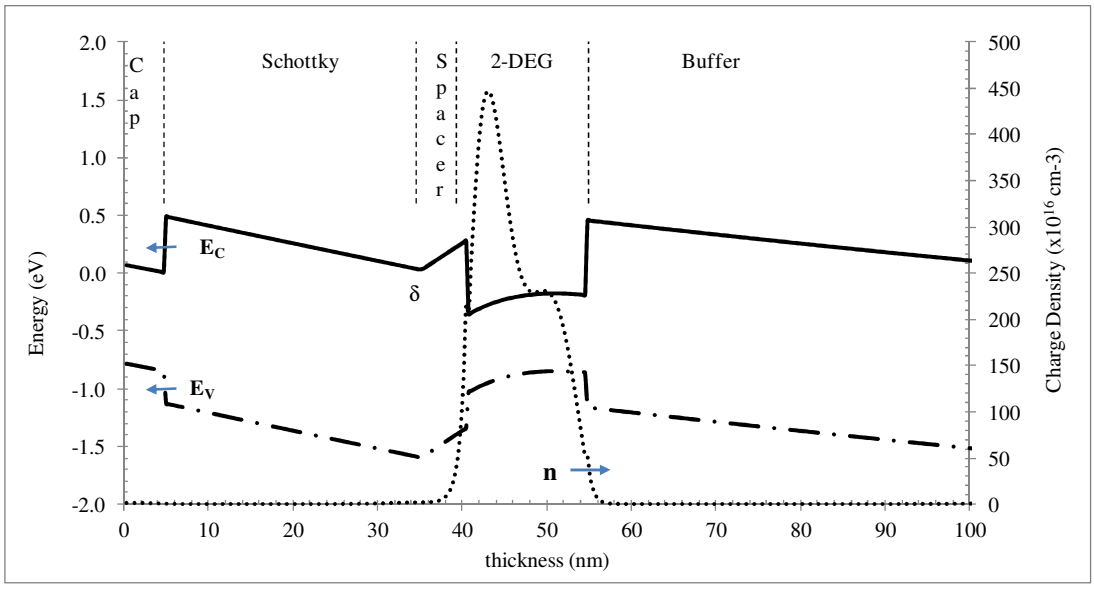



Figure 5-3 Energy band diagram of conventional pHEMTs epilayer, XMBE #171

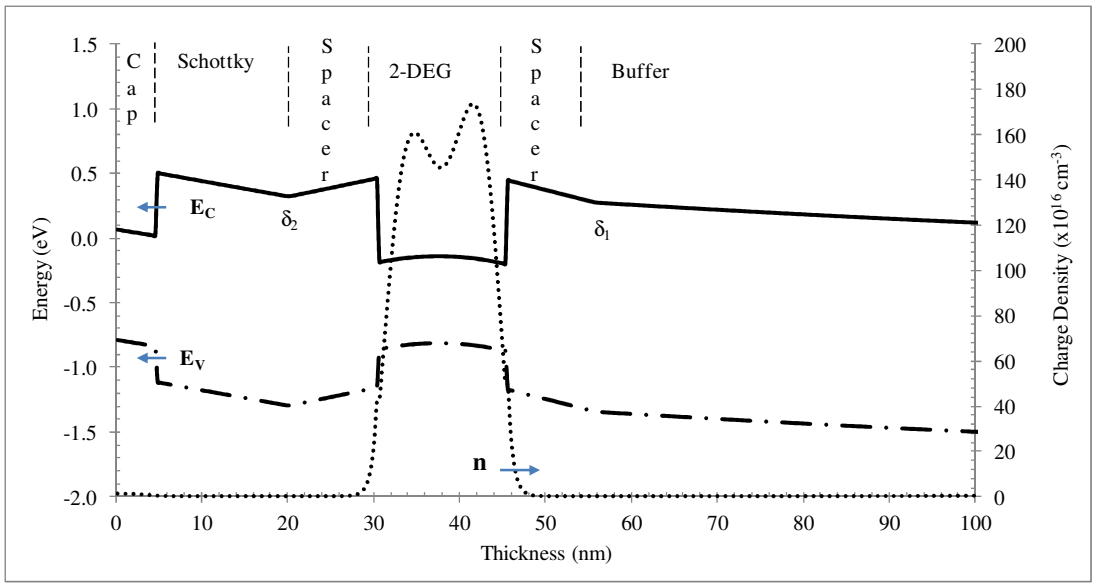



Figure 5-4 Energy band diagram of improved double δ-doped InGaAs/InAlAs pHEMTs epilayer, XMBE #131

## 5.3 DEVICE FABRICATION

Here, all devices were fabricated using the optimised process described in Chapters 3 and 4. The process started with cleaning the sample surface from organic and inorganic substances using Trichloroethylene, Acetone, and IPA. Then the devices'

active or isolation areas are defined by means of a non-selective orthophosporic ($H_3PO_4$:$H_2O_2$:$H_2O$) wet etch to the buffer layer about 160 nm in depth. Then the sidewall of the active layer was etched with succinic acid for better channel to gate isolation for the later gate deposition. The alloyed Ohmic contacts for Source and Drain were then formed by thermal evaporation and lift-off of AuGe/Au. Subsequently, the 1 µm gate footprints were then formed by a highly selective succinic acid etching to remove the 50 Å cap layer. The gate electrodes were then formed by thermal evaporation and lift-off of 50/400 nm Ti/Au metallisation. Later, probing pads were patterned and created via thermal evaporation of 50/400 nm of Ti/Au metallisation scheme. Next, 90 nm of $Si_3N_4$ was deposited using a low temperature process (200°C) in a plasma chamber for thermal feasibility before etching an opening at the end of each terminal for probing and connection for the field plate structures. Finally, field plate extensions ($L_{FP}$) ranging from 0.3 µm to 1.2 µm from gate to drain were formed by thermal evaporation and lift-off of 400 nm Au.

### 5.3.1 Field Plate Design

As briefly explained in the previous section, field plate (FP) structures were the last part of the fabrication process. Note that the FP structures with different gate to drain extension were deposited in separate fabrication steps from the gate electrode after the nitride passivation layer. This has several advantages: (i) ease of fabrication and (ii) $Si_3N_4$ eliminates any surface defects or traps near the gate terminal after the gate recess process. Even though several types of FP structure have been previously proposed [86-88], the chosen design served their purpose of modulating the electric field in-phase with the gate voltage.

In this work, the non-field plate and field plate devices were fabricated on the same epitaxial samples, eliminating sample-to-sample variations in processing. An illustration of the field-plated device showing the field plate extension is shown in Figure 5-5, and the dimensions of the simplified single gate showing field plate extension ($L_{FP}$) and gate length ($L_g$) are shown in Figure 5-6. Note that the field plate and gate electrode are only connected at the gate's pad, whereas along the gate electrode the field palate is isolated by 90 nm thick $Si_3N_4$. Nevertheless, this

structure will increase the gate parasitic capacitances, which will affect the RF performance of the device. Here, the FP was designed to have an extension of 0.3 µm, 0.6 µm, 0.9 µm and 1.2 µm from the gate electrode.

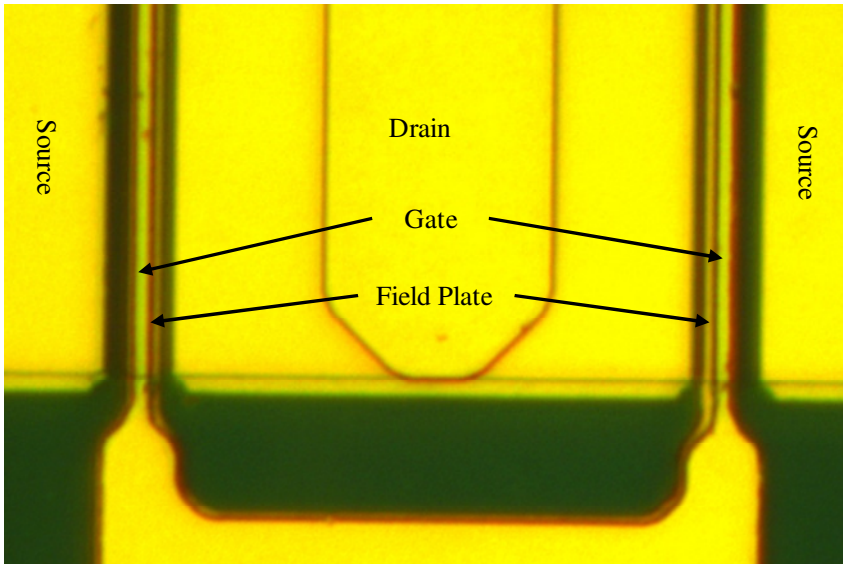



Figure 5-5 Illustration of dual gate terminal and dual Field Plate structure

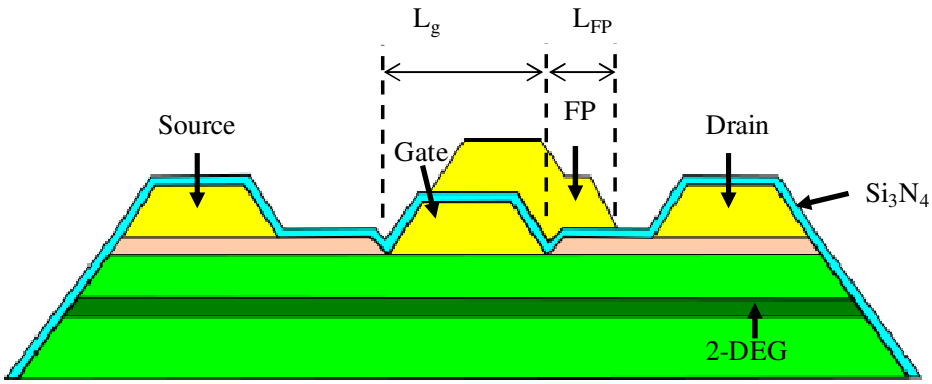



Figure 5-6 Cross section of simplified single gate-FP device

## 5.4 DC AND RF PERFORMANCES

This section will focus on the results from the measurements at each fabrication step of the device. Beginning with the results from the Transfer Length Method (TLM) at

the Ohmic layer, the measurements are then continued with the Schottky and conclude with the DC and RF performances of the devices.

### 5.4.1 Ohmic

All TLM measurements were performed after temperature treatment of the Ohmic metal from thermal evaporation and lift off of AuGe/Au. Here, two types of metallisation scheme were used. For the conventional pHEMTs epilayer, a thick metal was used, 50/400 nm, whereas for the improved double δ-doped, a thin metal was used, 50/100 nm. The heat treatments for both alloys were also different where the thin metal was annealed twice, first at 280 °C for 90 s and second at 290 °C for another 90 s, allowing sufficient metal diffusion to 2-DEG. The thick alloy was only annealed once at 280 °C for 90 s. The resulting average sheet resistance ($R_{sh}$) and contact resistance ($R_c$) from the TLM measurement are tabulated in Table 5-2. For comparison purposes, the $R_{sh}$ from the Hall data are also included. The TLM is made of 50 x 100 µm probing pads, with increasing pad spacing from 5 µm to 45 µm. Both samples show low $R_c$, indicating a good contact to the 2-DEG.

Table 5-2 $R_{sh}$ and $R_c$ from TLM measurement. $R_{sh}$ from Hall measurements are also included

| **Sample ID** | **$R_{sh}$ from Hall data (Ω/ )** | **$R_{sh}$ from TLM (Ω/ )** | **$R_C$ from TLM (Ω.mm)** |
|---|---|---|---|
| XMBE #171 | 186 | 182 | 0.19 |
| XMBE #131 | 187 | 176 | 0.08 |

### 5.4.2 Schottky and DC characteristic

The Schottky and DC measurements were characterised using an HP4142 parameter analyser. Here, two Ground-Signal-Ground (G-S-G) probes were used to measure the device's total width. The effective widths of each device under test are 2 x 100

µm and 2 x 300 µm, respectively. The Source-Gate-Drain (S-G-D) separation for all devices is 2-1-2 µm. For simplicity, only 2 x 100 µm devices are presented with the selection of conventional gate structure (NFP) and field plate with 1.2 µm extensions (FP12). The data presented here were taken from a single device that exhibited the best characteristics, where other device showing uniformity within variation of 10%.

The Schottky gate current is plotted on a semi log scale and presented in Figure 5-7. As expected, the gate leakage from the conventional epilayer is considerably higher, where all devices with and without FP already met the current compliance at as low voltage as $V_{GS}$ = -3 V. The leakage is improved in the double δ-doped epilayer where the leakage for all devices is below 3 mA/mm up to $V_{GS}$ = -8 V. This is shown in Figure 5-8. This much improved characteristic is a result of the better carrier confinement, where most of the electrons are trapped in the wider and nearly square quantum well channel. The calculated ideality factor ($\eta$) for both diodes is 1.5 and 1.7 for XMBE #171 and XMBE #131, respectively. Due to the fact that both epilayers are made from the same lattice match InAlAs material as the Schottky barrier, the barrier height $\phi_B$ for both structures is the same at 0.5 eV.

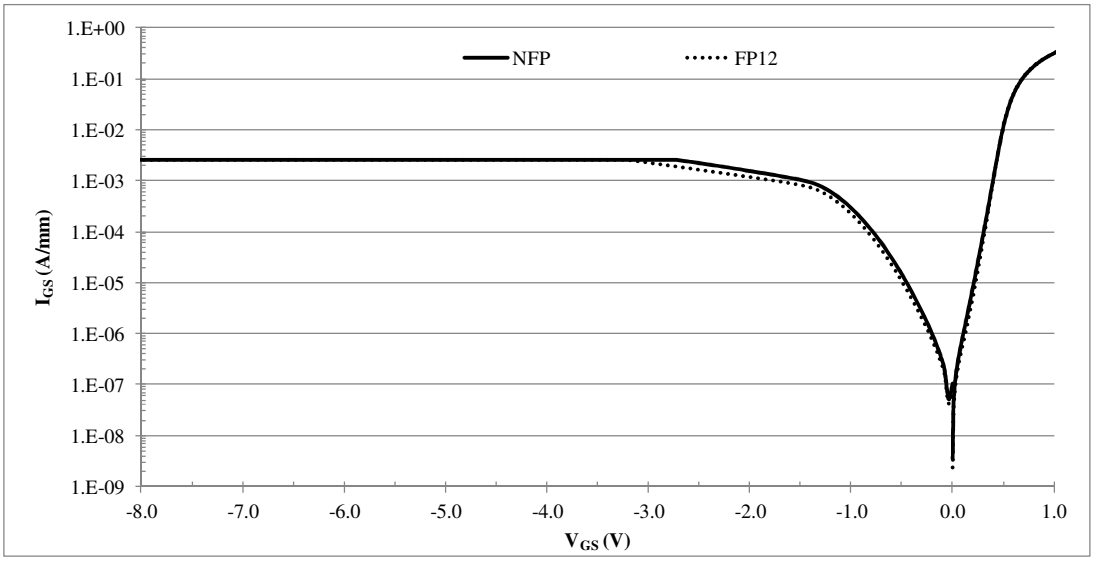



Figure 5-7 Schottky diode measurements for XMBE #171 showing conventional gate (NFP) and FP with 1.2 µm extensions (FP12)

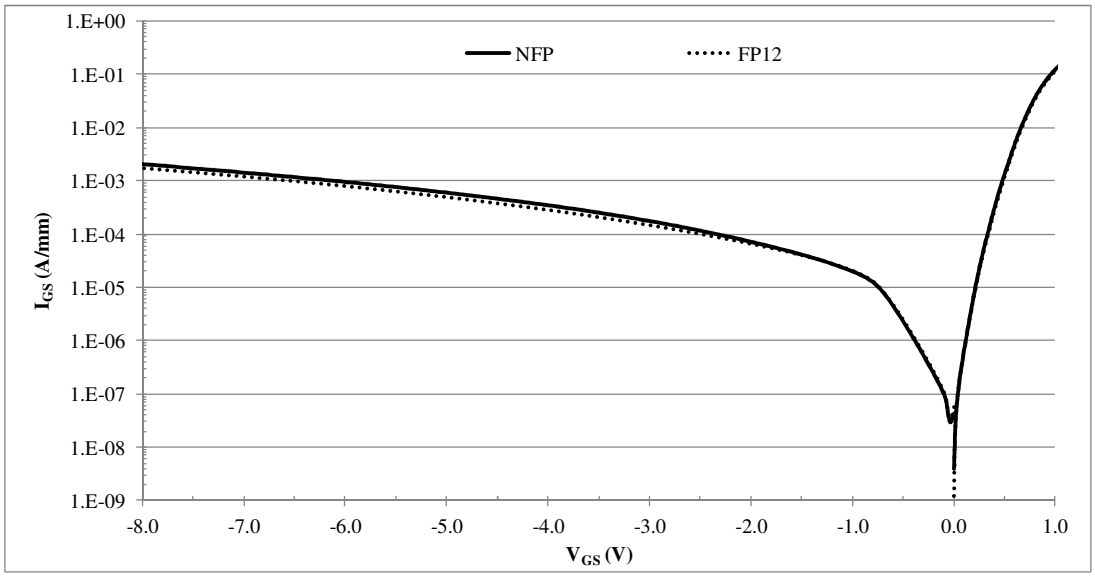



Figure 5-8 Schottky diode measurements for XMBE #131 showing conventional gate (NFP) and FP with 1.2 µm extensions (FP12)

From this point on, the presented data will only show the measurement at $V_{DS}$ = 1 V. In the LNA circuit design especially, most of the time, the $V_{GS}$ biasing is near the impact ionisation region, thus it is essential to choose $V_{DS}$ that gives low gate leakage currents. As compared to other $V_{DS}$ biasing, this is the point where the leakage due to impact ionisation is the least as will be shown in Figure 5-9 and Figure 5-10.

The on-state leakages for both epilayer are demonstrated in Figure 5-9 and Figure 5-10 respectively. Comparing both graphs, the leakages for XMBE #171 are visibly higher than XMBE #131. Particularly, the leakages due to impact ionisation for all XMBE #171 devices are in the range of -1.0 to -1.8 mA/mm, whereas the leakages due to tunnelling already hit -5 mA/mm at $V_{GS}$ between -3.6 V to -4.0 V. The data, however, indicate only a small improvement in the reverse gate leakage when the FP structure is fitted. As for XMBE #131, the gate leakage is lower up to $V_{GS}$ = -6 V, where it is in the range of -1 mA/mm for all devices. The maximum leakage due to impact ionisation is considerably small at -30 µA/mm which is shown in the inset of Figure 5-10. This behaviour is again explained by the better carrier confinement in the 2-DEG by adopting the double δ-doped epilayer structure.

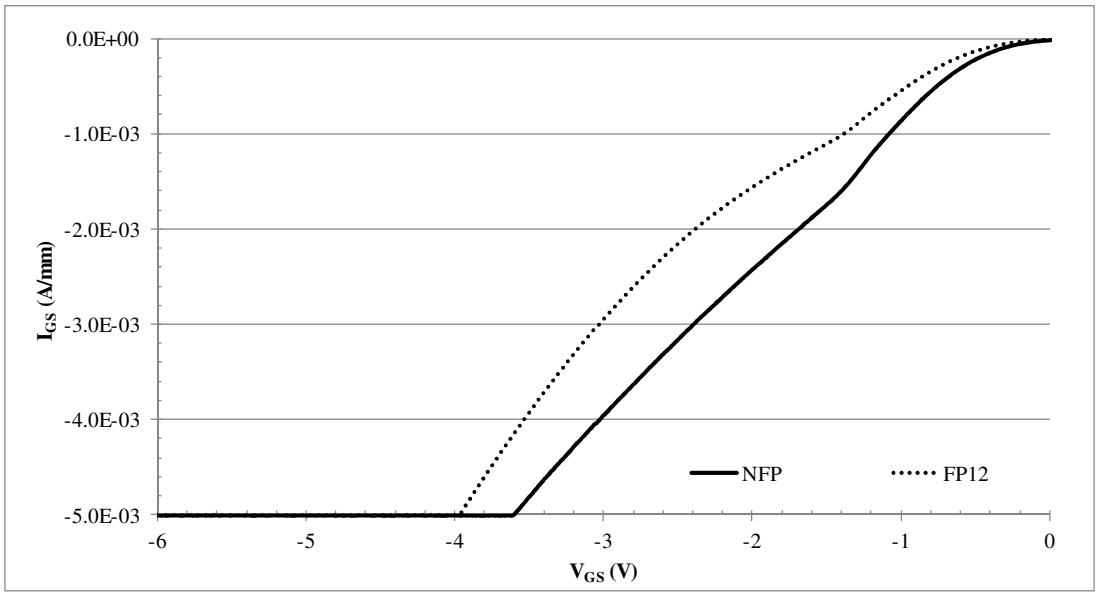



Figure 5-9 On-state leakage measurement for XMBE #171 showing conventional gate (NFP) and FP with 1.2 µm extensions (FP12) at $V_{DS}$ = 1 V

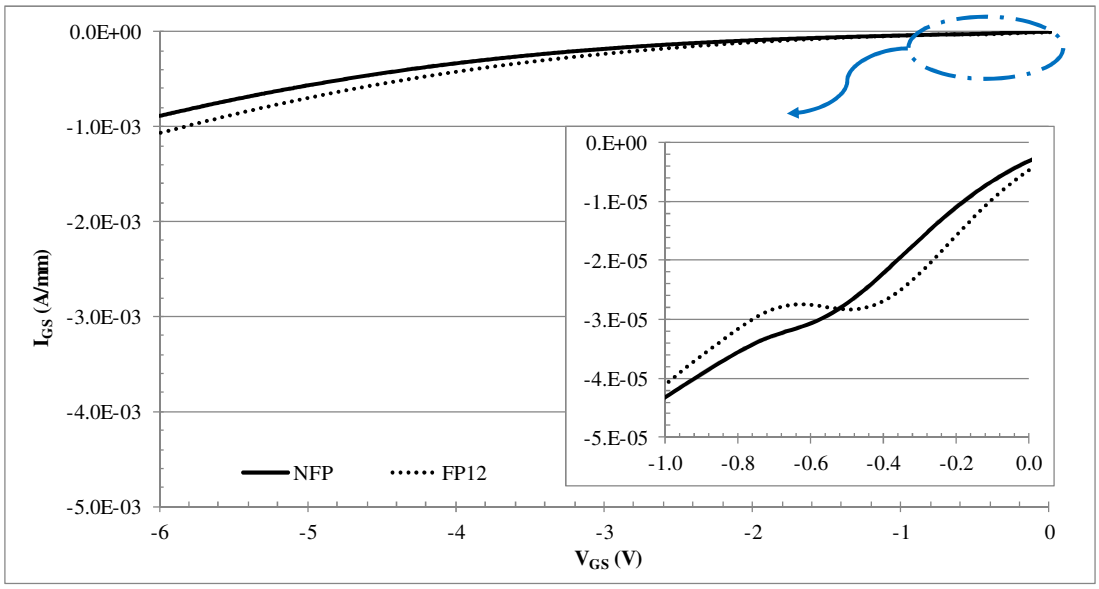



Figure 5-10 On-state leakage measurement for XMBE #131 showing conventional gate (NFP) and FP with 1.2 µm extensions (FP12) at $V_{DS}$ = 1 V. Inset showing the gate leakage due to impact ionisation.

The threshold voltage ($V_{th}$) shift is observed in Figure 5-11 and Figure 5-12. The $V_{th}$ for XMBE #171 is approximately -1.25 V and shifted to a more positive value for XMBE #131 at -0.75 V. The $V_{th}$ shifting is mainly due to the gate to channel distance. By referring back to the epitaxial structures (Figure 5-1 and Figure 5-2), the gate to channel distance for XMBE #171 is 350 Å, whereas for XMBE #131 it is

only 250 Å, 100 Å shorter than the conventional pHEMTs epilayer. The $V_{th}$ difference between FP and non-FP devices for XMBE #171 is about ± 0.1 V, whereas almost non-visible $V_{th}$ variation for the XMBE #131 device is observed.

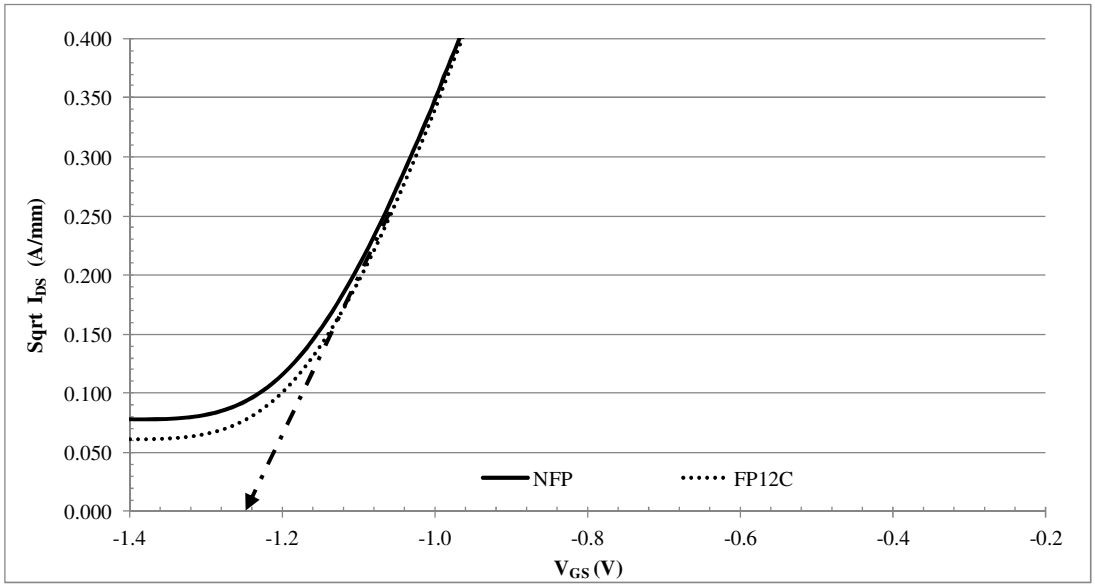



Figure 5-11 Threshold Voltage ($V_{th}$) measurement for XMBE #171 showing conventional gate (NFP) and FP with 1.2 µm extension (FP12) at at $V_{DS}$ = 1 V

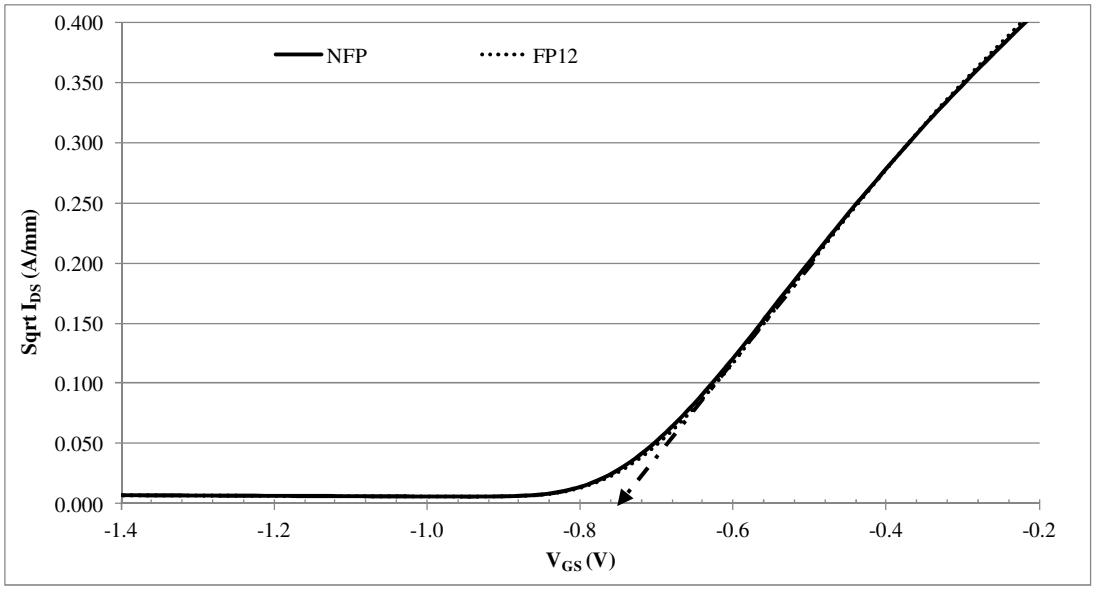



Figure 5-12 Threshold Voltage ($V_{th}$) measurement for XMBE #131 showing conventional gate (NFP) and FP with 1.2 µm extension (FP12) at $V_{DS}$ = 1 V

The transconductance ($g_m$) of HEMT devices is inversely proportional to the gate to channel distance. This is the reason for the higher maximum transconductance

($g_{m\_max}$) for the XMBE #131 device as compared to XMBE #171, as portrayed in Figure 5-13 and Figure 5-14. The $g_{m\_max}$ is 500 mS/mm and 460 mS/mm for XMBE #131 and XMBE #171, respectively. The I-V curves for both epilayers are depicted as Figure 5-15 and Figure 5-16. Since the depletion layer induced by the gate voltage controls the $I_{DS}$, a shorter gate-channel distance (apparently wider depletion layer) will only allow a small amount of carriers to go through the channel. For the thinner gate to channel layer (XMBE #131), the $I_{DS}$ current is thus lower than in XMBE #171 at the same $V_{GS}$ biasing. The maximum $I_{DS}$ at $V_{GS}$ = 0 V ($I_{DSS}$) is approximately 450 mA/mm for XMBE #171 and only 300 mA/mm for XMBE #131. Hence, for a similar reason, XMBE #131 has lower pinch-off voltage ($V_p$) compared to XMBE #171. However, since the reduction of $I_{DS}$ is almost proportional to the shifting to the $V_{th}$, the loss in output current can be corrected by increasing the $V_{GS}$ biasing to a more positive value.

Another essential point observed at this stage is the difference in output current density for the FP and non-FP devices at the same $V_{GS}$ biasing. Illustrated in the same figures, the $I_{DS}$ for non-FP devices are higher than the FP devices. The experimental data for XMBE #171 shows that the $I_{DSS}$ is 474 mA/mm for conventional HEMT, as compared to 453 mA/mm for the FP devices. Similarly, the peak saturation current for XMBE #131 is 326 mA/mm for non FP devices as compared to ~ 300 mA/mm for FP devices. At other $V_{GS}$ biasing, a proportional current reduction is observed in both epilayers. In summary, at least a 4 % and 8 % drop of saturation current can be seen in the XMBE #171 and XMBE #131 epilayers by incorporating FP structures. The FP electrodes together with thin $Si_3N_4$ passivation, yield the larger device's effective gate length, and, consequently, cause a drop in the drain current.

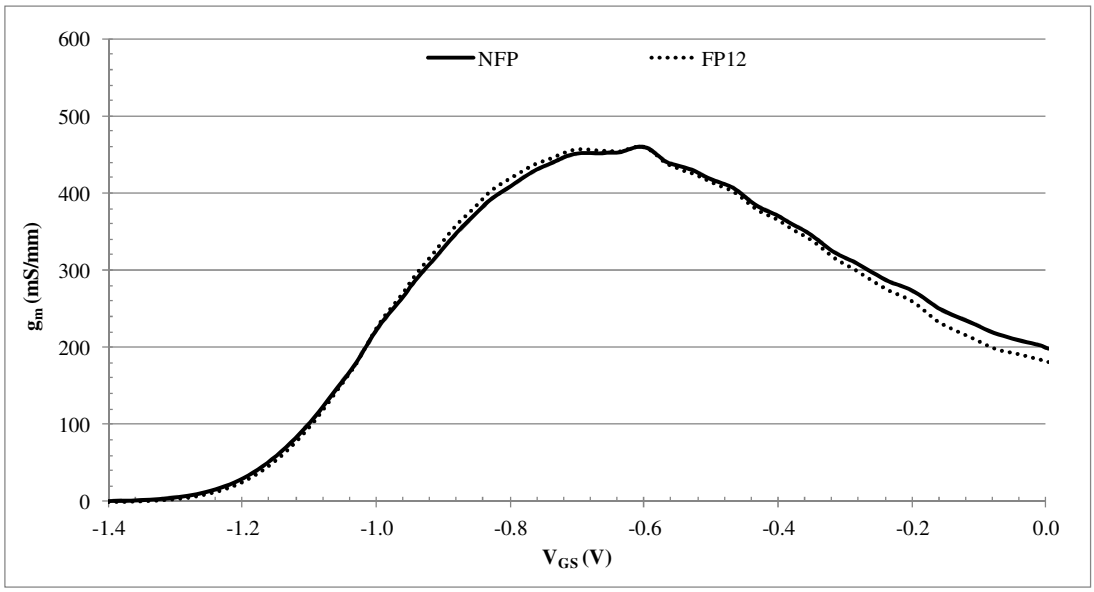



Figure 5-13 Transconductance ($g_m$) measurement for XMBE #171 showing conventional gate (NFP) and FP with 1.2 µm extension (FP12)

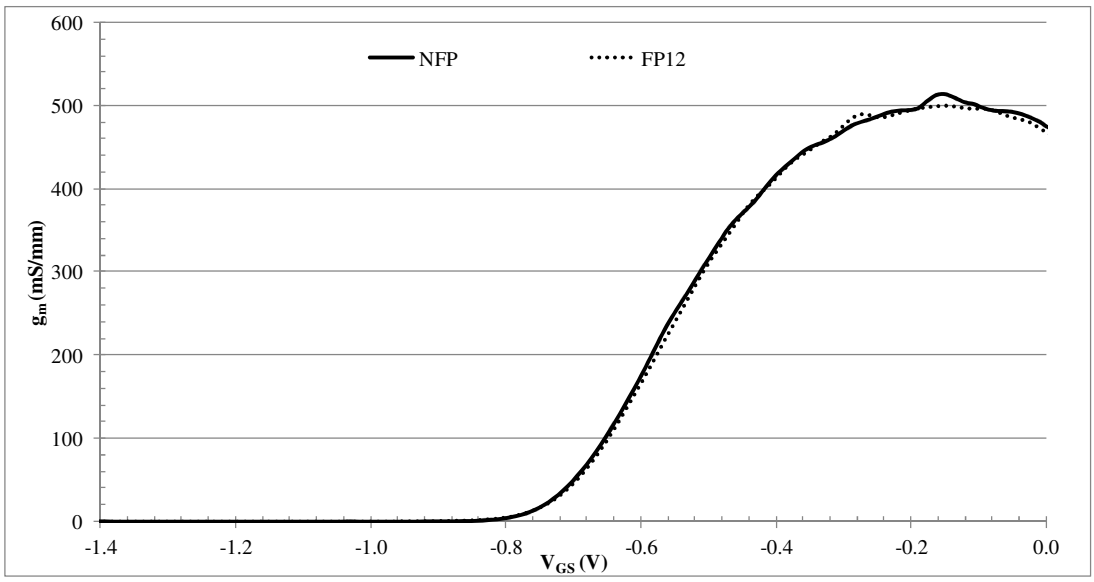



Figure 5-14 Transconductance ($g_m$) measurement for XMBE #131 showing conventional gate (NFP) and FP with 1.2 µm extension (FP12)

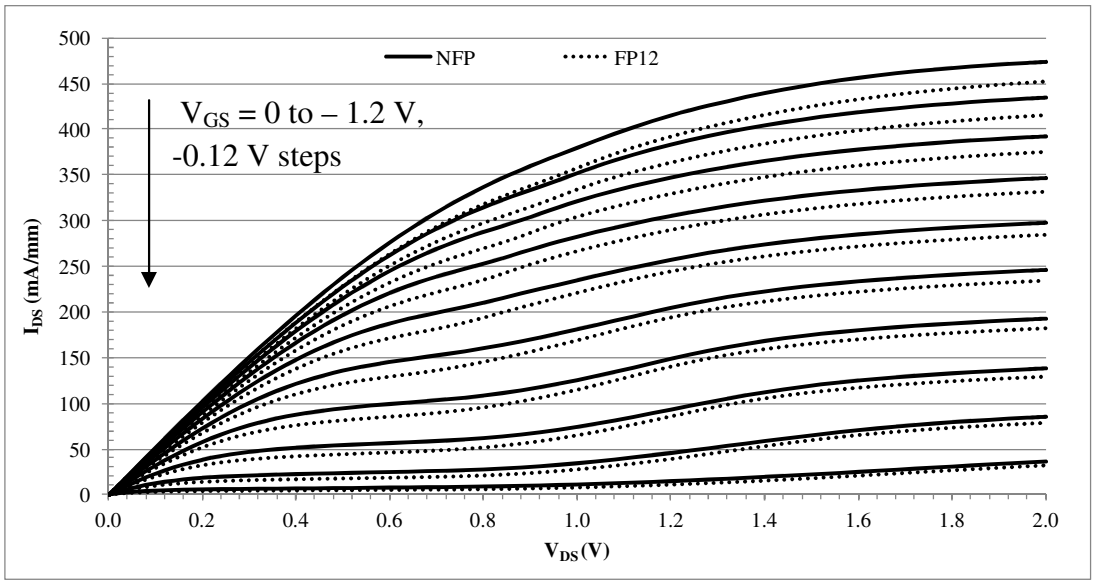



Figure 5-15 Output current density measurement for XMBE #171 showing conventional gate (NFP) and FP with 1.2 µm extension (FP12)

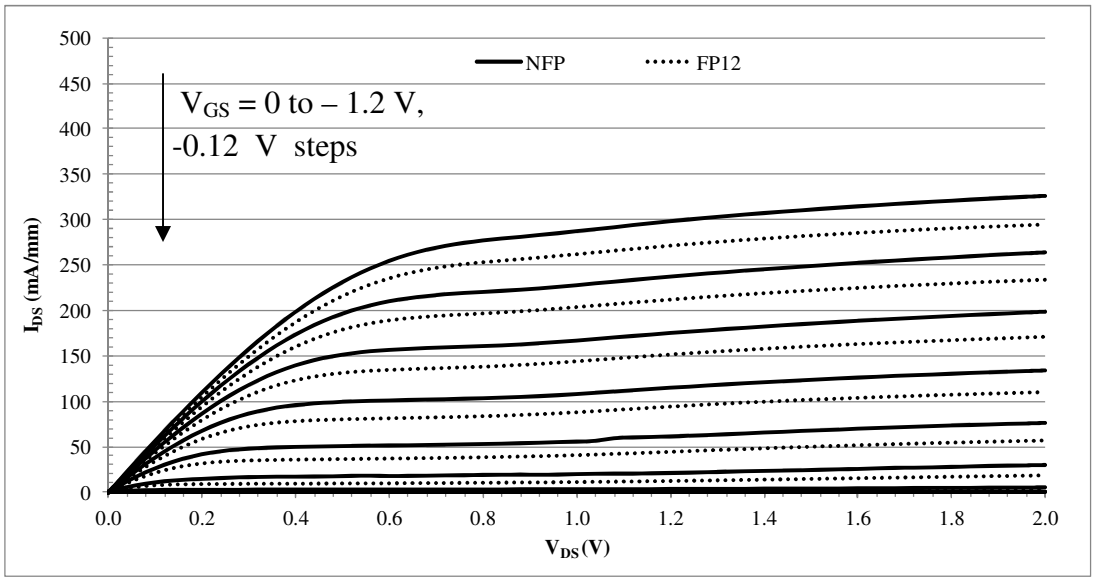



Figure 5-16 Output current density measurement for XMBE #131 showing conventional gate (NFP) and FP with 1.2 µm extension (FP12)

Despite the degradation in $I_{DS}$, the FP devices displayed in Figure 5-17 show a significant improvement in the device's $V_{BR}$. The $V_{BR}$ for the conventional epilayer has been improved by 37 %, from 3.5 V to 4.8 V by the inclusion of FP structures. In the same graph, the field-plate electrode increases the $V_{BR}$ for XMBE #131 from

about 11.5 V to 14.5 V. The results reaffirm the previous finding that the FP structure reduces the peak electric field at the gate end near the drain side and distributes it along the FP structure, which then delays the junction breakdown.

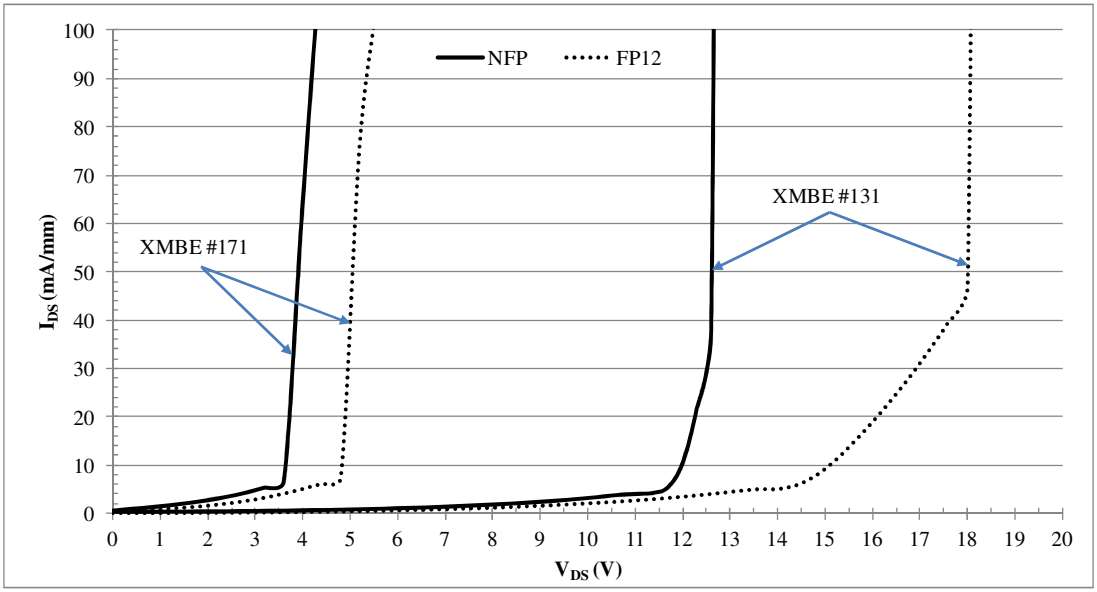



Figure 5-17 Pinched Off breakdown measurement for XMBE #171 and XMBE #131 showing conventional gate (NFP) and FP with 1.2 µm extension (FP12)

### 5.4.3 RF Performances

The RF measurements were performed using an Anritsu Vector Network Analyser (VNA). Based on the DC measurement data, biasing at high $g_m$ (for low noise) was set. The resulting RF measurements are illustrated in Figure 5-18 and Figure 5-19 and the tabulated RF biasing data at 100% $g_{m\_max}$ are summarised in Table 5-3. The results show that the field-plate structures did not have any detrimental effect on the cut-off frequency ($f_T$), but have a visible effect on the device maximum oscillation frequency ($f_{max}$). The resulting $f_T$ for all XMBE #171 devices is ~20 GHz, and ~21 GHz for all XMBE #131 devices.

By incorporating the FP structure, the increase in gate capacitance is inevitable, thus, the $f_{max}$ for field plate extension of 1.2 µm is smaller than the non-FP devices. By

incorporating the field plate structure $f_{max}$ for both epilayers it reduced from 40 GHz to 30 GHz.

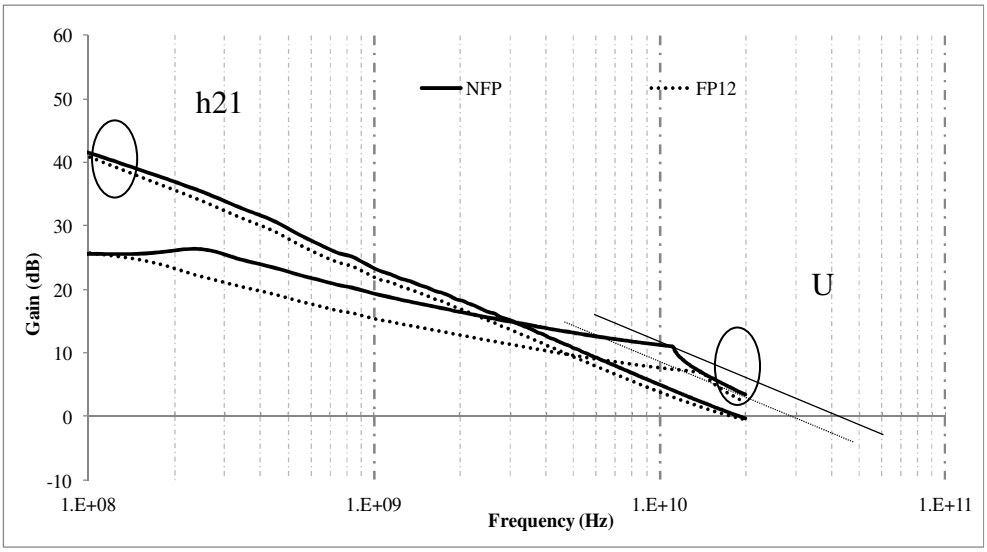



Figure 5-18 Unity Current Gain (h21) and Unilateral Power Gain (U) measurements XMBE #171 showing conventional gate (NFP) and FP with 1.2 µm extension (FP12)

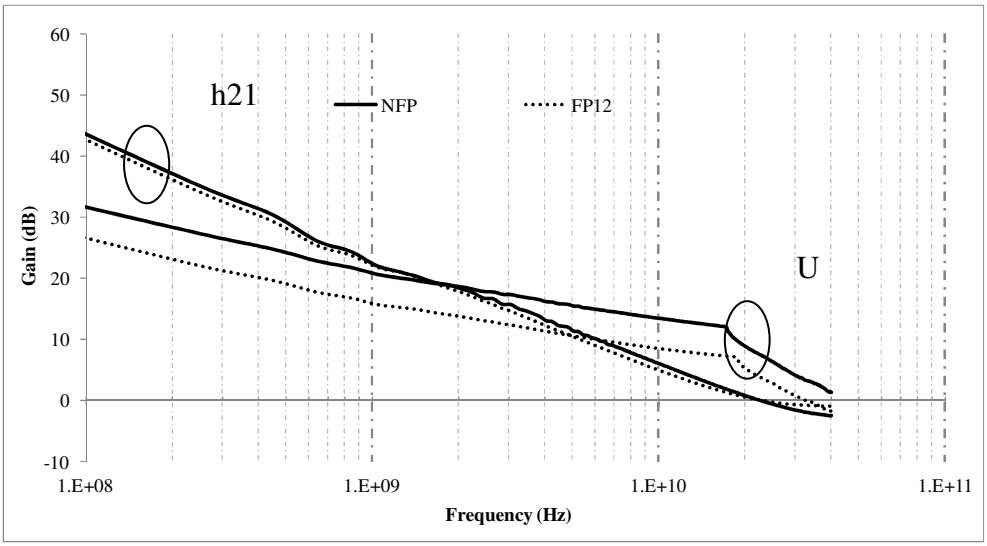



Figure 5-19 Unity Current Gain (h21) and Unilateral Power Gain (U) measurements\

Table 5-3 RF biasing for conventional HEMTs and FP HEMTs

| Parameters | XMBE #171 | XMBE #131 |
|---|---|---|
| $V_{DS}$ (V) | 1.0 | 1.0 |
| $g_{m\_max}$ (mS/mm) | 465 ± 5 | 500 ± 5 |
| $V_{GS}$ (mV) | -675 ± 5 | -125 ± 5 |
| $I_{DS}$ (mA) | 27 ± 1 | 37 ± 2 |
| $f_T$ (GHz) | ~20 (NFP and FP12) | ~20(NFP and FP12) |
| $f_{max}$ (GHz) | 30 (NFP)<br>40 (FP12) | 30 (NFP)<br>40 (FP12) |

## 5.5 SUMMARY

High Breakdown InGaAs-InAlAs pHEMTs incorporating improved epitaxial layer and field plate structures have been successfully fabricated and characterised in this work. The newly optimised epilayer and field plate devices demonstrate more than 3 times improvement in $V_{BR}$, without sacrificing the devices' DC and RF performances. The low noise and high voltage characteristics are encouraging for applications in high voltage, high efficiency Power Amplifiers (PAs) at millimetre-wave band.

# CHAPTER 6

# DEVELOPMENT OF MMIC LNAs FOR SKA RECEIVER (400 MHz TO 1.4 GHz)

## 6.1 INTRODUCTION

For the low frequency spectrum of the SKA, cost-effective Ultra Low-Noise Amplifiers are required at frequencies spanning the range of 300 MHz to 2 GHz. InP-based HEMTs have previously demonstrated superior noise performance at millimetre-wave frequencies using short-gate length and are indeed commonly used in high performance LNAs, albeit at cryogenic temperatures. However, in the low frequency range, matching the LNA for wideband, low noise performance becomes a critical issue, as it requires adding large passives into the design, which can act as sources of added noise if integrated in the LNA. This can be circumvented by using off-chip components but at the expense of both cost and complexity. Thanks to a novel high-breakdown, low-leakage InGaAs/InAlAs pHEMT structures, developed in Manchester, which enable the use of large periphery gate transistors, both low NFmin and low Rn, which are key points for better impedance matching across the ultra-wideband, can be simultaneously obtained. In addition, for low frequency applications, the requirement for extremely high cut-off frequencies is relaxed and larger gate lengths (~1 µm), as opposed to sub-micron, are perfectly adequate in terms of noise performance and stability of the LNA [89].

In this chapter, the development of LNAs using the ultra low leakage and high-breakdown device described in Chapter 5 is addressed. The large periphery devices (4 x 200 µm) based on 1 µm technology developed on UoM, which are used in the design of LNAs, were fabricated based on this newly developed enhanced epitaxial structure, namely VMBE #2100. This chapter will concentrate on the details of the fabrication of the circuit.

## 6.2 MMIC AND COPLANAR WAVEGUIDE (CPW)

A Monolithic Microwave Integrated Circuit (MMIC) is a microwave circuit technology in which the devices operate at microwave frequencies that can range from 300 MHz to 300 GHz. Here, all active and passive components are fabricated on the same substrate. This technology is the successor of the established Microwave Integrated Circuit (MIC) technology where the circuit comprises discrete active devices and passive components integrated onto a common substrate where the interconnection is made by using solder or other conductive epoxy adhesive. Compared to MIC, in MMIC technology, integrated circuit miniaturisation can be achieved, in addition to the exclusion of the extensive use of mechanical design and workshop machining [90].

For such high frequency application, the interconnections are made in such a way that the signal reliability is maintained. Historically, microstrip transmission lines were successfully used in MIC boards where a large number of circuit elements could be made. However, one prominent shortcoming of this type of transmission line is the incorporation of via holes to ground all active devices, which, introduces a significant increase in the parasitic inductance value and results in circuit performance degradation [91].

In MMIC, however, Coplanar Waveguide (CPW) transmission, the suggested substitute for microstrip lines, has attracted most interest owing to its integration capability with electronic devices and fabrication compatibility. These advantages include ease of parallel and series insertion of both active and passive components at high circuit density. What is more, they have better isolation between adjacent lines and lower dispersion characteristics, which are well suited for use with FET, where RF grounding must be close to the device. Here, via holes are not needed and fragile semiconductors need not be made excessively thin [92-94].

The transmission line of a conventional CPW line is illustrated in Figure 6-1, showing the dimensions for calculating the characteristic impedance. The impedance is calculated by the ratio between the conductor width ($w$), slot width ($s$), substrate thickness ($h$) and substrate permittivity ($\varepsilon_o\varepsilon_r$). The details of the calculation formula are explained in [95]. In this work, a characteristic impedance of 50 Ω is used.

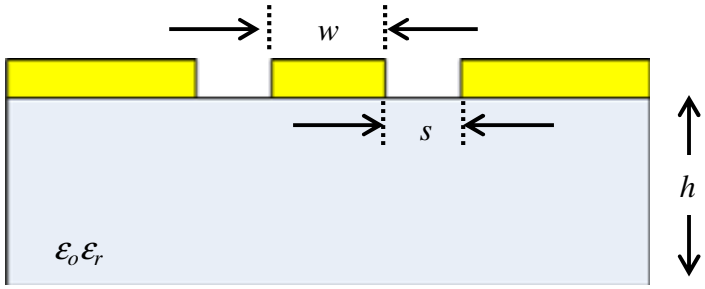



Figure 6-1 CPW transmission lines dimensions for calculation of the characteristic impedance

## 6.3 FABRICATION PROCESS

The full fabrication process was completed entirely using a lithography process in the Microelectronic & Nanostructures (M&N) lab, UoM. The main fabrication process involves photolithography, metal thermal evaporation, nitride deposition and metal sputtering. The fabrication process flow is illustrated in Figure 6-2.

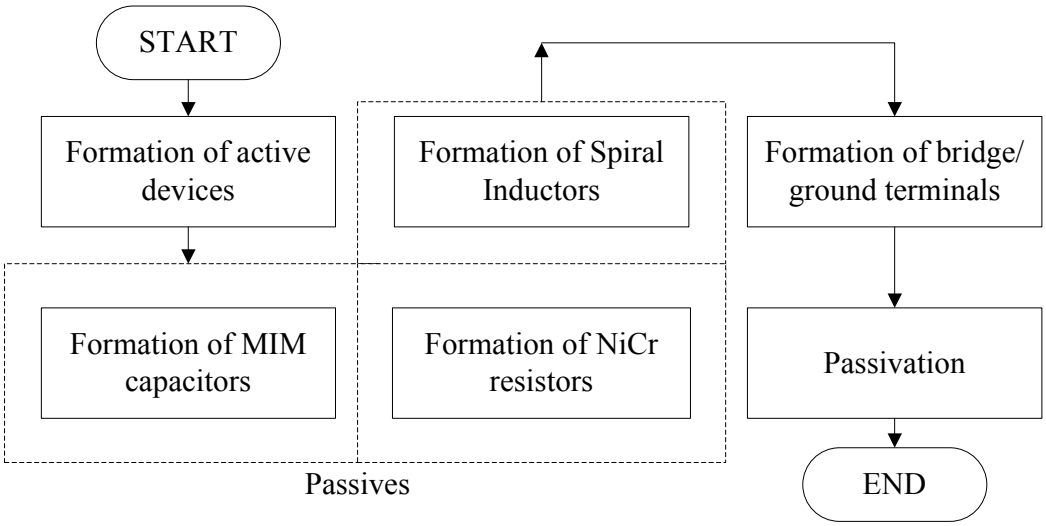



Figure 6-2 LNA's Process Flow at M&N, UoM

In the process flow, the samples were first cleaned to remove organic and inorganic contamination while transporting to the fabrication laboratory by using Trichloroethylene, Acetone, and IPA. After that, the process started with the fabrication of the active device, as described in Chapter 4. Here, only one gate

dimension of 4 x 200 µm with ~1 µm gate length was chosen to drive the LNA circuits. The active device steps were stopped at the probing pads layer (Metal 1) before the passives were fabricated. The Ti/Au probing metal pads (Metal 1) were chosen to be the bottom plate for the integrated metal-insulator-metal (MIM) capacitors and inductor. Metal 1 and Metal 2 are separated by a thin insulator to prevent short circuiting. Here, the insulator was chosen to be $Si_3N_4$ for its thermal stability and combination function as the active device passivation layer, which eliminates the effect of the charge trapping effect. $Si_3N_4$ also acts as the dielectric material for MIM capacitors. After etching the nitride opening at the designated probing interconnection pads, Nickel Chromium (NiCr) thin film resistors were sputtered on top of the nitride before the formation of passive devices was completed by the formation of the second interconnection metal layer (Metal 2) for all capacitors, spiral inductors and top plate capacitors. Next, the SF11 bridge support for the transistor multi-finger source terminal bridging and circuit RF grounding were shaped before the Au metal bridge was deposited on top of the SF11 layer. Finally, the LNA circuit was passivated, where only the probing pads were opened for probing for the next measurements steps.

Here, the particulars of the passive steps are detailed whereas the development of the active devices was described earlier in Chapter 4.

### 6.3.1 MIM Capacitors

In RF circuits, capacitors are usually located at the DC and RF input or output matching circuitry. The DC block capacitor, which is usually located in series with the RF input, will only allow AC signals to pass through to the next stage while blocking any occurring DC function. In contrast, the de-coupling capacitor will work in a way so that only DC components can go through, whilst isolating the AC signal. Normally, the de-coupling capacitor exists in parallel with the DC supply. An illustration of these capacitors and their location is shown in Figure 6-3.

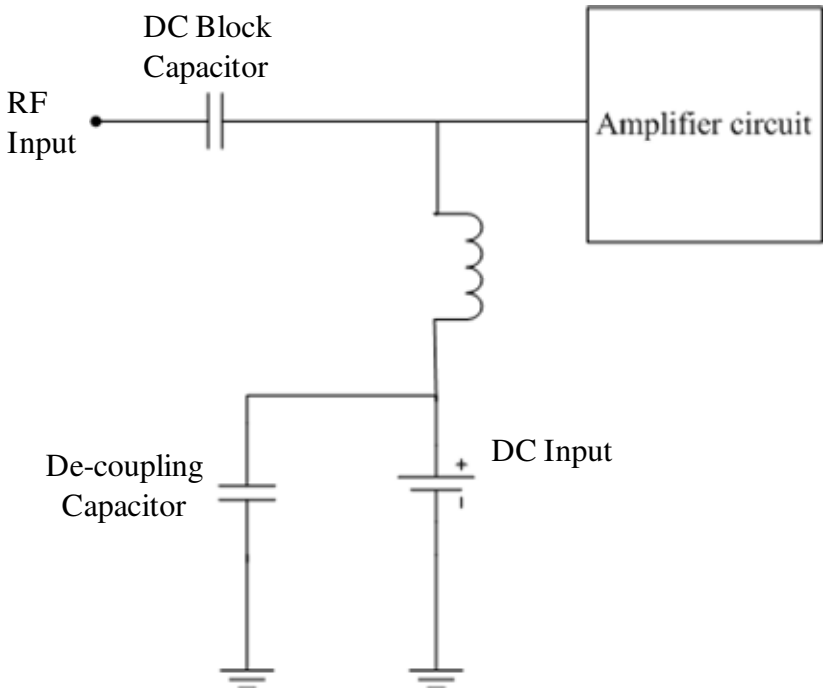



Figure 6-3 Illustration of DC block and de-coupling capacitors in a RF input matching circuitry

In MMIC design, the Metal-Insulator-Metal (MIM) capacitors are created from two parallel conducting plates isolated by a thin insulator layer. As mentioned before, the dielectric layer used in this work is 90 nm $Si_3N_4$ from a low temperature-plasma deposition process. Equation 6-1 shows that the capacitance value ($C$) is determined by the dimensions of the overlapped parallel plates ($W*L$), the permittivity of the dielectric layer ($\varepsilon_o\varepsilon_r$) and dielectric thickness ($t_d$). The CPW MIM capacitor with transmission line of width $w$ and slot width $s$ is depicted in Figure 6-4.

$$C = \varepsilon_o \varepsilon_r \frac{W * L}{t_d} \qquad \text{Equation 6-1}$$

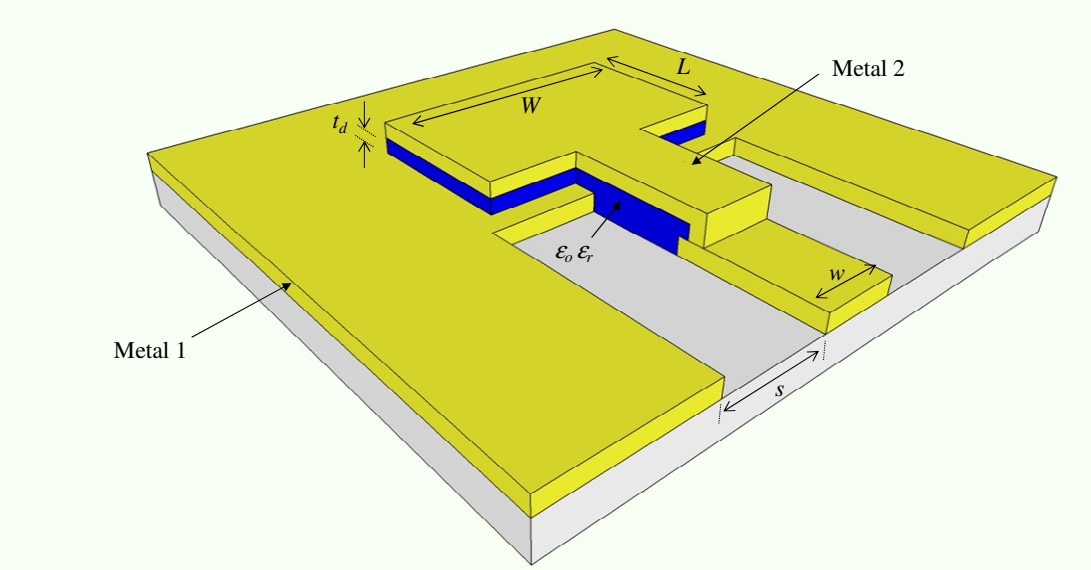



Figure 6-4 Coplanar Wave Guide Metal-Insulator-Metal capacitor

In the fabrication of the device, the bottom plate is the bond pads layer (Metal 1) and the top plate is the second metal layer (Metal 2) from the thermal evaporation and lift-off process. For both metals, Ti/Au of 50/400 nm thickness is chosen for the metallisation scheme. Note that the quality and thickness of the nitride plays an essential role in determining a working capacitor and its value. Thus, in the LNA mask, a number of capacitors ranging from large, medium and small capacitances value were included in the Process Control Module (PCM). The PCM list and their dimensions are tabulated in Table 6-1.

Table 6-1 Capacitor dimensions at PCM structures

| **Capacitor (pF)** | ***L* (µm)** | ***W* (µm)** |
|---|---|---|
| **25.0** | 308.0 | 104.0 |
| **8.0** | 98.0 | 104.0 |
| **2.0** | 29.5 | 104.0 |

These PCM components were tested with a C-V meter fitted in the Agilent's B1500A Semiconductor Device Analyser. The resulting C-V measurement from 1.0 kHz to 1.0 MHz is depicted in Figure 6-5, showing the resulting 24.0 pF, 7.9 pF, and

2.6 pF for nominal 25.0 pF, 8.0 pF and 2.0 pF capacitors, respectively. The data shows a reasonable fit between the measured and designed value with the processing error within 20 %. Note that for the 2 pF capacitor, the percentage of error is higher due to its dimension relative to the small capacitance value.

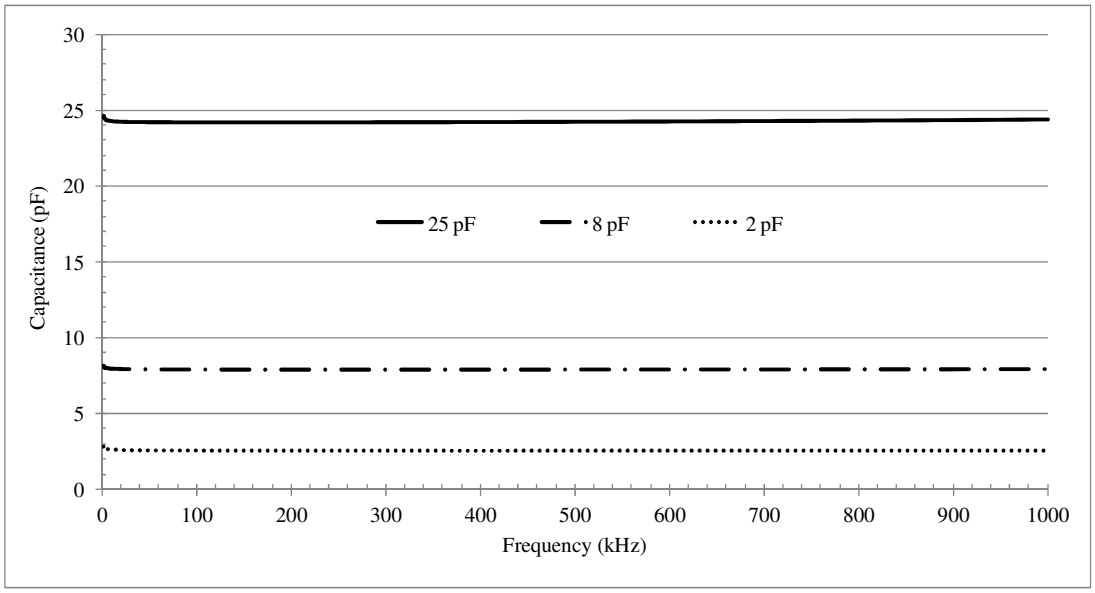



Figure 6-5 PCM's C-V measurement result from 1 kHz to 1 MHz frequency using Agilent's B1500A Semiconductor Device Analyser

The result from the C-V meter indicates that the capacitor already shows a stable response at low frequencies of 1 k Hz to 1 MHz. A digital picture of a fabricated 8 pF MIM capacitor is shown in Figure 6-6.

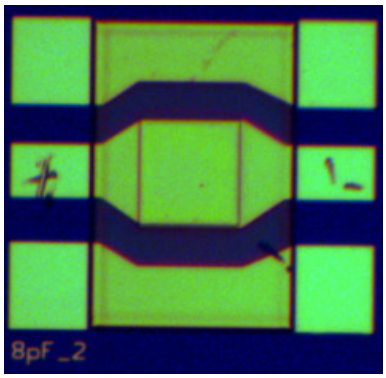



Figure 6-6 A 8 pF MIM capacitor fabricated at UoM

### 6.3.2 NiCr RESISTOR

The resistivity ($R$) of a conductor material having cross-sectional area $A$ and length $l$ is given by Equation 6-2.

$$R = \rho\frac{l}{A} \qquad \text{Equation 6-2}$$

Where $\rho$ is the material resistivity in unit Ω.m. However, for a uniform thickness ($t$) conductor, it is more convenient to express the resistance in terms of two-dimensional entities of length ($l$) with respect to width ($W$). The expression in Equation 6-2 can be rewritten as:

$$R = \rho\frac{l}{W * t} = \frac{\rho}{t} * \frac{l}{W} \qquad \text{Equation 6-3}$$

Which can be simplified to $$R = R_{sh}\frac{l}{W} \qquad \text{Equation 6-4}$$

Where $R_{sh}$ is the material sheet resistance having unit Ω/ , and defined as

$$R_{sh} = \frac{\rho}{t} \qquad \text{Equation 6-5}$$

Now, the conductor resistivity can be calculated by multiplying the material's $R_{sh}$ with the number of squares from the ratio of conductor $l$ with respect to its $W$. For $l$ = 2*$W$, the number of squares in the example is 2. An illustration of these dimensions is shown in Figure 6-7.

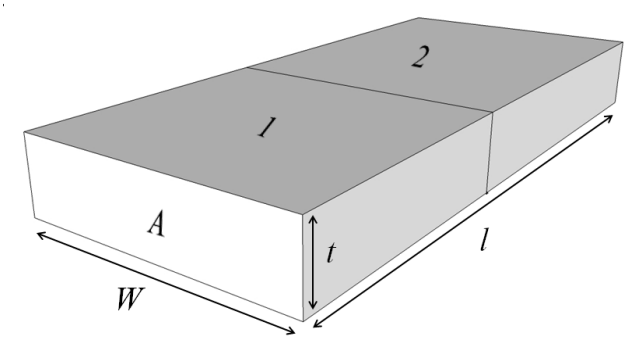



Figure 6-7 An illustration of a conductor having dimensions $W$, $l$ and $t$ for the calculation of its Resistivity ($R$) and the corresponding 2-dimensional number of squares ($l$ = 2*$W$)

In MMIC technology, the resistors must demonstrate a wide range of resistivity by varying the film stoichiometry, low temperature coefficient resistance (TCR), excellent thermal stability, high constancy of electrical properties, and, above all, compatible with the MMIC fabrication process.

To accomplish this, there are two notable ways in resistor formation, namely, semiconductor resistors and thin film metal resistors. In the first method, the resistors are made from the MESA etched structures or by implanting the active layer with impurities, which later act as the resistive medium. The obtainable $R_{sh}$ from this method can be as high as 200 Ω/ or higher in the deeply etched structure. However, referring back to Equation 6-4, a high value of $R_{sh}$ will limit lower values to only a few Ohms and to achieve low value precision resistors becomes particularly difficult. Moreover, the active layer TCP can be as high as 3000 ppm/°C, which gives rise to the non-linear behaviour of resistors at high processing temperatures [96].

For this reason, thin film metal resistors are rapidly replacing semiconductor resistors and are the preferred technique for MMIC application. The deposited low-resistance thin film metal has low $R_{sh}$ in the range of 30 to 50 Ω/ .

Amongst the thin film materials, Nickel Chromium (NiCr) resistors are extensively used as the discrete loads. NiCr fulfils all the properties needed for a good and stable resistor. In addition to excellent wear and corrosion resistance, the required resistivity can be achieved easily by the suitable dimensions and aspect ratio for the thin film [97].

In this work, the NiCr resistors were built on top of the nitride passivation layer and the reactive process took place in a high vacuum DC cathode gas tube where the metal source is loaded with Argon (*Ar*) as the ion bombardment source. The samples were mounted on the carousel anode and rotated by discharge where the product of ion bombardment at the NiCr cathode target sputters in Omni-directional deposition, forming a thin film coating on the surface of the sample [98].

In the LNA circuit, there are a varying number of resistors ranging from the tenth to the kilo-ohm scale. Thus, the resistors in the PCM contain a large value of 8 kΩ and a small value of 40 Ω resistors. These resistors were placed at the four corners near

the alignment marks meant for verifying process uniformity. The NiCr thin film was first patterned by a bi-layer process from LOR3A (undercut layer) and S1828 (imaging resist) before the opening was sputtered to 50 nm thickness. The metallisation of the contacts was made from Ti/Au of 50/400 nm thickness from thermal evaporation and lift-off process using a Metal 2 mask. Here, NiCr with 20 µm width is chosen for our resistor design, thus the resistance value can be achieved by varying the NiCr length. A picture of the fabricated 8 kΩ NiCr resistor with Ti/Au metal contact is depicted in Figure 6-8.

In our process, we chose $R_{sh}$ to be 50 Ω/ . The desired $R_{sh}$ can be achieved by varying the thickness of the sputtered NiCr layer and measuring the $R_{sh}$ by the TLM method. The TLM ladder is the same size and spacing as that of the Ohmic's TLM where contact pads of 100 µm x 50 µm are used for probing to measure the voltage resulting from a 1 mA current supply. The resistance between the two pads is obtained by dividing the resulting voltage over the supply current. The ladders' spacing increases at intervals of 5 µm from 5 µm to 45 µm. The resulting plot of NiCr's $R_{sh}$ versus NiCr thickness is depicted in Figure 6-9. Similar to other TLM data, the tabulated data were from measurement of several TLM ladders, and only the average data are shown. From the plot, the required $R_{sh}$ can be obtained by sputtering ~ 52 nm thick of NiCr thin film metal.

The tabulated $R_{sh}$ and $R_c$ from the sputtered 50 nm NiCr thickness by the TLM method are shown in Table 6-2. The results show that the contact resistance from the NiCr thin film is very low (0.04 Ω.mm) and can be ignored.

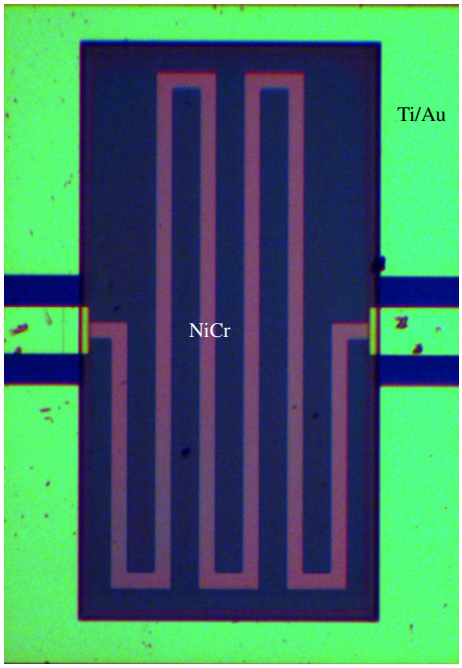



Figure 6-8 8 kΩ NiCr resistor by extending the thin film length ($l$) in meandered track

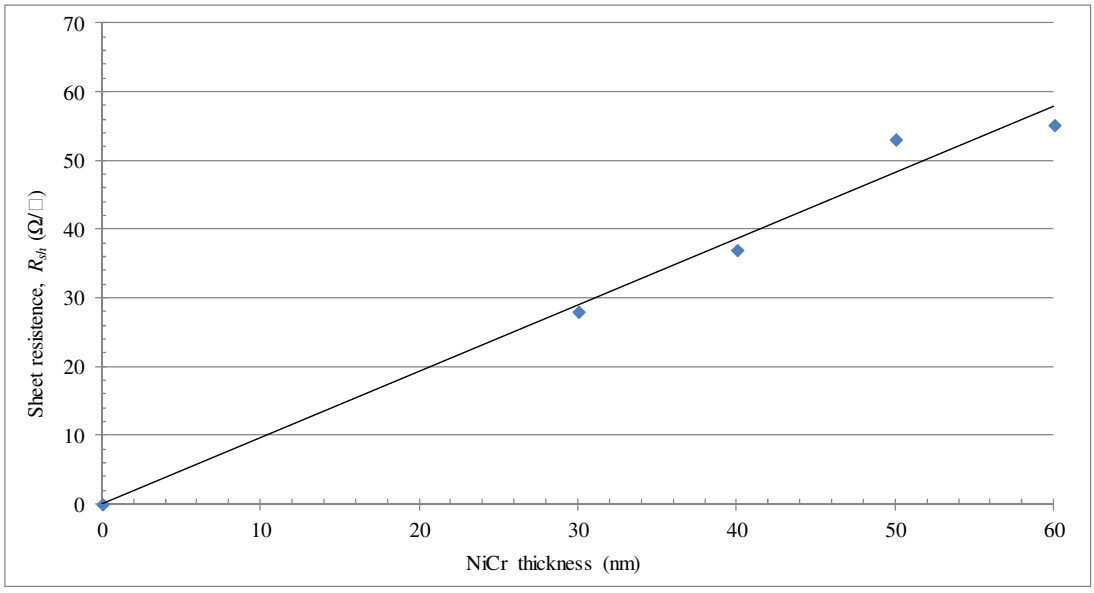



Figure 6-9 Plot of $R_{sh}$ versus thickness for NiCr resistor

Table 6-2 The resulting contact resistance, Rc and Rsh from sputtering 50 nm of NiCr

| Parameters from TLM's extraction | Values |
|---|---|
| Rsh (Ω/ ) | 50.30 |
| Rc(Ω.mm) | 0.04 |

Several PCM devices were also measured at this stage and average values are shown in Table 6-3. As noted in the table, the processing yield is very good with the discrepancy well below 3%.

Table 6-3 The resulting average resistance values for PCM resistors

| PCM's nominal resistor value (Ω) | Measured resistor value (Ω) | Percentage error (%) |
|---|---|---|
| 8,000 | 7, 984 | 0.20 |
| 40 | 41 | 2.75 |

In the LNA design, the resistors are located at the input and output ports of the active device for several reasons. An example of resistor location in a Common-Source (CS) RF amplifier is shown in Figure 6-10.

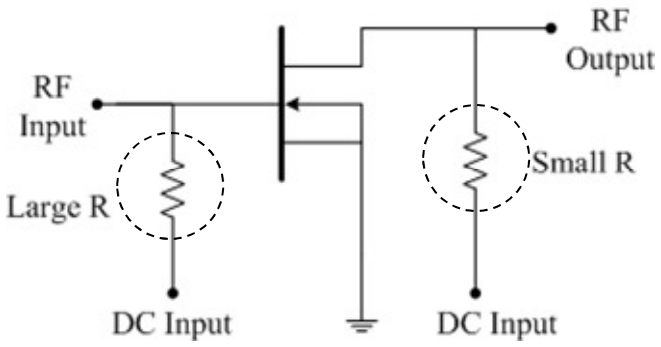



Figure 6-10 An illustration of the resistor location in a common source amplifier

A large resistor is placed at the gate input to bias the active device's input voltage, without initiating any gate leakage current to the transistor. The large resistance will prevent the current flow from the DC supply to the gate input, which, consequently, will bias the gate input voltage to the same potential as the DC input voltage. Another small resistor is located at the output node to improve the RF output stability, prevent oscillation, and used for RF output matching.

### 6.3.3 Spiral Inductor

A basic inductor is made from a wire loop or coil wound around a dielectric or ferromagnetic material. It is a two-terminal passive component that stores energy in the form of a magnetic field. The inductance value is dependent on the radius of the coil, type of material that the coil is wound from and linearly proportional to the number of turns in the coil.

However, in microelectronic circuit design, inductors are created in different ways due to the limitation of the material used and total fabrication area. One of the most widely used on-wafer inductor designs is the spiral inductor, which is made from a transmission line arranged in a spiral shape. Here, the spiral shape can be realised in many different forms, such as rectangular, circular, hexagonal and octagonal [99-101]. In this work, the spiral inductor takes a rectangular shape.

The spiral inductors, however, have to use at least two metal layers to connect the centre turn back to the outside circuit. Thus, this dictates the use of air-bridge crossovers or dielectric space underpass for the metal separation [90]. In our design, we use the second method, because, at the same time, the dielectric is used to form our MIM capacitors and active device passivation.

With reference to Figure 6-11, the top and bottom metal of the MMIC spiral inductor are made from 50/400 nm thick Ti/Au metallisation and are labelled as Metal 2 and Metal 1 layer, respectively. To prevent short-circuiting between these two layers, the top and bottom metal are isolated by 90 nm thick $Si_3N_4$. The connection between the Metal 1 and Metal 2 layers is made through a nitride opening by plasma etching with Halocarbon 14 - Tetrafluoromethane ($CF_4$) and Oxygen ($O_2$) on the metal contact area.

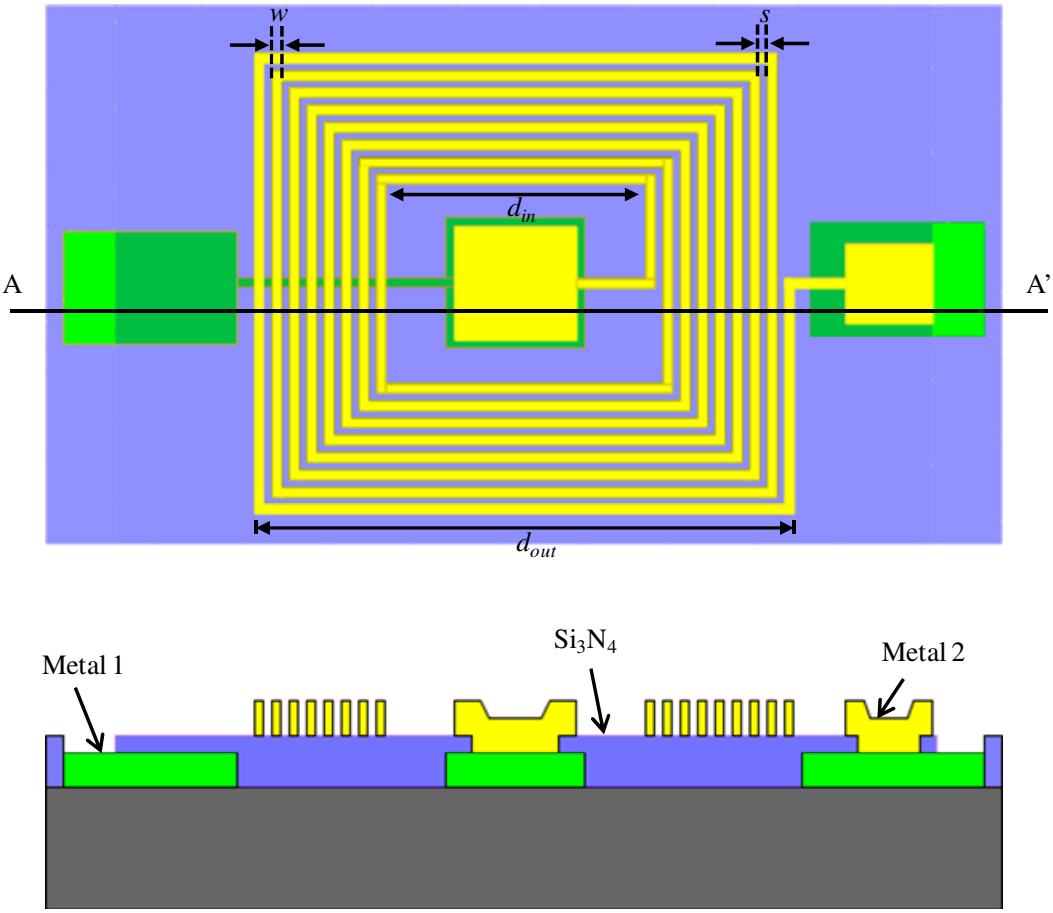



Figure 6-11 Top and cross view along A-A' line for a square shape MMIC spiral inductor

In MMIC design the inductance ($L$) can be calculated by several methods [102, 103]. The simplest expression is given by the Modified Wheeler Formula, as in Equation 6-6 [103]. In the equation, $\mu_0$ is the permeability of free space ($4\pi$ x $10^{-7}$ $Hm^{-1}$), $n_L$ is the number of turns, $d_{avg}$ is the average diameter and $\psi$ is the fill ratio.

$$L = 2.34 * \frac{\mu_0 {n_L}^2 (d_{avg})}{1 + 2.75\psi} \qquad \text{Equation 6-6}$$

$d_{avg}$ is calculated as the average diameter between outer and inner diameter as $d_{avg} = (d_{out}+d_{in})/2$. The fill ratio given by $\psi = (d_{out} - d_{in})/(d_{out} + d_{in})$ represents how hollow the inductor is where a small ratio represents a hollow inductor ($d_{out} \approx d_{in}$) and for a large ratio we have a full inductor ($d_{out} >> d_{in}$). From this expression, a 14 nH square shape spiral inductor can be obtained from $n_L = 8$, $d_{out} = 220$ µm and $d_{in} = 93$ µm.

To verify our fabricated inductors, we have measured the S-parameter characteristics of the component and fitted the measured data with our inductor model using Agilent's Advanced Design System (ADS) software. Our equivalent circuit model is shown in Figure 6-12. Due to the lengthy metal structure used to form the spiral structure, a notable series resistance ($R_S$) is created in series with the inductor ($L$) link. Since two metal layers are used in the formation of the component, two types of capacitor are present in the model. The under plate ($C_p$) capacitors are present at the overlapped metal structures parallel to the component node and the fringing capacitance ($C_F$) due to the arrangement of the metals adjacent to each other.

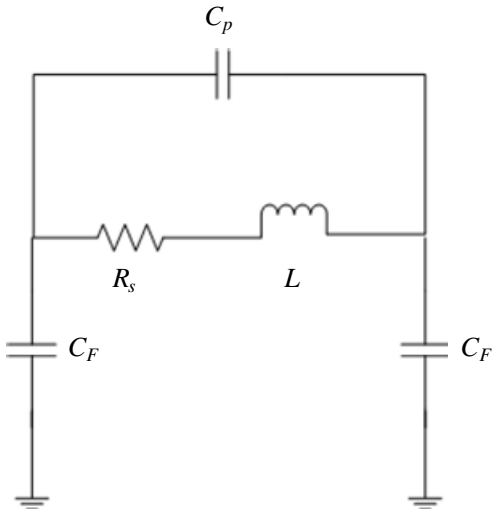



Figure 6-12 Schematic of equivalent circuit model for spiral inductor

Here, the value for inductance is computed using Equation 6-6. The value of $R_S$ is calculated as below:

$$R_S = \rho_m \frac{l_m}{W_m * t_m} \qquad \text{Equation 6-7}$$

Where $\rho_m$ is the metal resistivity ($\rho_m = \rho_{Au} = 2.44 \times 10^{-8}$ Ω.m), $l_m$ physical length of metal, $W_m$ is the width of the square metal and $t_m$ is the metal thickness. The series resistances can be measured by taking the ratio between the inductor voltage and 1 mA current supply.

$C_p$ and $C_F$ can be calculated using the equations as listed below:

$$C_p = n_L \varepsilon_r \varepsilon_o \frac{A_i}{t_d}$$ Equation 6-8

Where $\varepsilon_r \varepsilon_o$ is the permittivity of nitride (7.5 x 8.85 x $10^{-12}$ F/m), $A_i$ the area of metal intersection and $t_d$ is the nitride thickness (90 nm).

$$C_F = n_L W_m{}^2 \frac{2\ \varepsilon_a \varepsilon_o}{s}$$ Equation 6-9

Where $\varepsilon_a \varepsilon_o$ is the permittivity of free air (1 x 8.85 x $10^{-12}$ F/m) and $s$ is the adjacent Metal 2 spacing. An illustration of $C_p$ and $C_F$ is depicted in Figure 6-13.

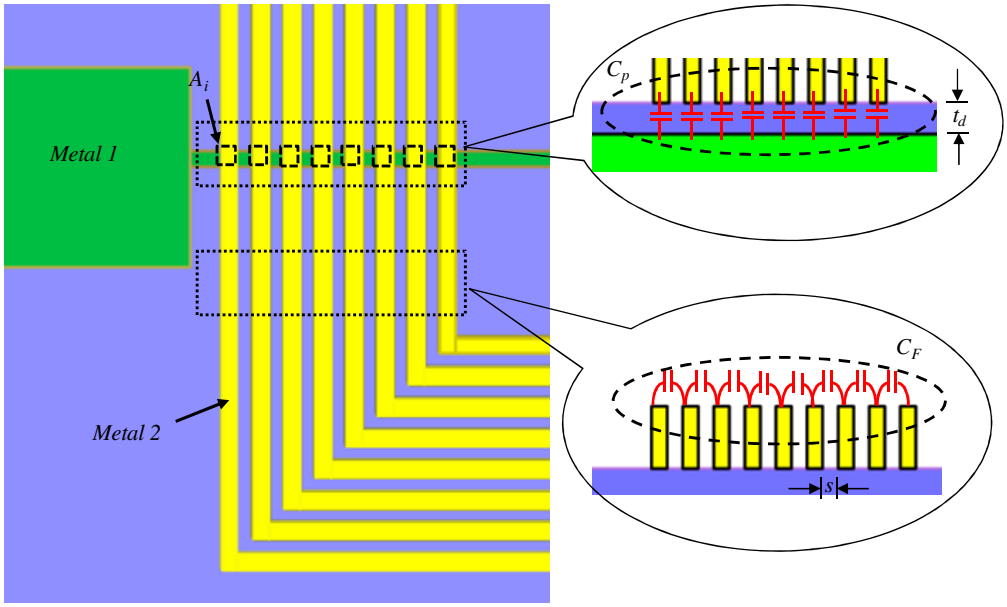



Figure 6-13 Illustration of $C_p$ and $C_F$

The excellent curve fitting between the measured and modelled S-parameters for 14 nH spiral inductor is illustrated in Figure 6-14. A summary of the inductor parasitic elements is tabulated in Table 6-4.

Table 6-4 Summary of parasitic components in the Inductor's model

| Components | Value |
|---|---|
| L (nH) | 13.44 |
| Rs (Ω) | 74.71 |
| CP (pF) | 0.11 |
| CF (pF) | 0.001 |

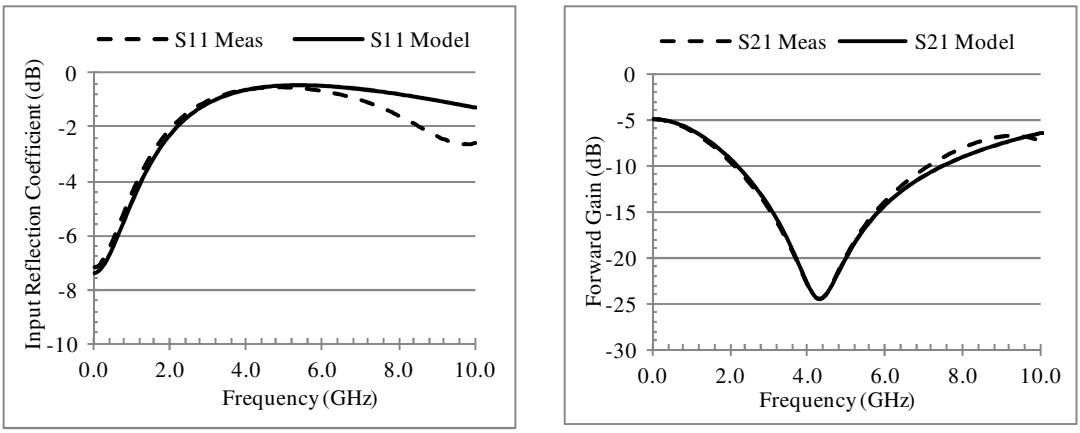



Figure 6-14 Curve fitting between measured and modelled S-parameters for 14 nH spiral inductor

From the summary, the parasitic component due to both capacitances is very small (< 0.2 pF) and can be ignored in the design. However, the Rs value is large and needs to be included in the device's simulation. In LNA design especially, an increase in the resistance value will affect the output RF matching since the inductor is placed at the output port to provide better output match over the wide frequency band, and, hence, ensure the unconditional stability of the LNA.

From this parasitic parameter extraction, the Q factor of the inductor can be calculated from Equation 6-10, which shows that the Q factor at low frequency (< 1

GHz) is less than 1. This indicates that the inductor may lose its efficiency at low frequency due to the heat generated by $R_s$.

$$Q = \frac{2\pi fL}{R_s} = 1\ x\ 10^{-9} * f \qquad \text{Equation 6-10}$$

A photograph of a fabricated 14 nH square shape spiral inductor is depicted in Figure 6-15.

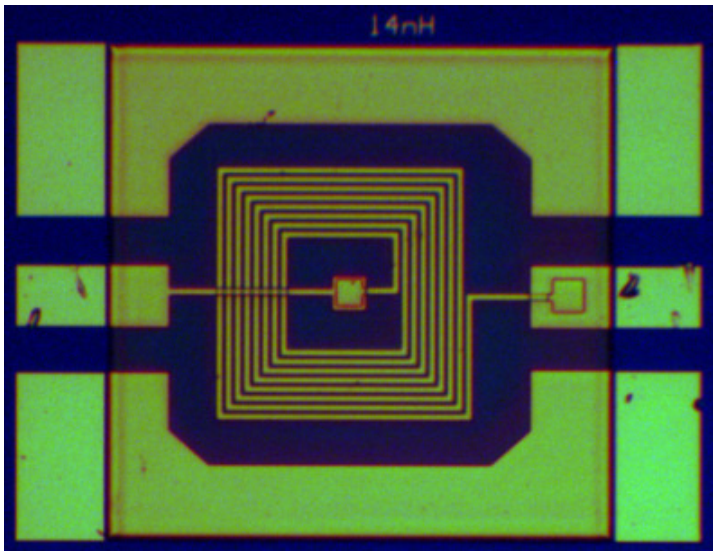



Figure 6-15 Spiral inductor fabricated at the University of Manchester

## 6.4 CIRCUIT DESIGN

In previous sections, the fabrication steps of each active and passive device were clarified together with the characterisation of each device. Before going into details concerning the fabrication, the circuit designs are discussed in brief. In this work, all circuits were designed by Modelling Team as previously described in Section 4.3

Three types of LNA circuit designs, namely, Single Stage Single-ended LNA (SSLNA), High Gain Double Stage Single-ended LNA (HG-DSLNA) and Moderate Gain Double Stage Single-ended LNA (MG-DSLNA) were designed. The circuit design and layout were performed using Agilent's Advanced Design System (ADS)

Electronic Design Automation (EDA) software. The LNA designs were optimised for frequency of operation from 0.4 GHz to 1.4 GHz.

The proposed LNAs are designed to meet the following criteria: low cost, low noise, high gain, unconditionally stable and low power dissipation, as being highlighted in Section 1.3.1.

### 6.4.1 Single Stage Single-ended LNA

The schematic diagram of the Single Stage single-ended MMIC LNA (SSLNA) is shown in Figure 6-16. The LNA is designed to operate at a frequency range of 0.4 GHz to 2 GHz, where, at this frequency, the noise is minimum and the gain is high. As mentioned earlier, the active device used in the design is a 4 x 200 µm depletion mode pHEMT fabricated on a VMBE #2100 epitaxial layer. The active device, labelled as $T_1$, is biased at $V_{DS}$ = 1 V, $V_{GS}$ = -0.92 V and $I_{DS}$ = 22 mA.

The biasing for this LNA employs the common-source technique where the amplifier high gate resistance at the input terminal only allows a very little amount of input current to be injected into the gate terminal. Hence, the optimum gate potential is obtained from the DC input ($V_{GG}$) where VGS ≈ $V_{GG}$ = -0.92 V. In addition, the high gate resistor ($R_G$) also minimises the circuit oscillation at low frequency.

In the circuit, the series input/output capacitor ($C_i$ and $C_O$) will block all DC signals originating from the DC supply voltage ($V_{GG}$ and $V_{DD}$) and prevent the interference of DC with RF signal at the input and output ports. $C_{dc}$ are the input coupling capacitors, which prevent any RF leakage to the DC sources ($V_{DD}$ and $V_{GG}$) by shorting the RF signal to ground.

The drain capacitor ($C_1$) is used to improve the input return loss as well as providing the output matching to the amplifier. The resistor load ($R_1$) is located at the transistor's drain output to prevent the circuit from oscillating. However, this resistor will have no effect on the noise characteristic as it is placed at the output port of the LNA. Nonetheless, it can reduce the amplifier's overall gain, and, therefore, to minimize the gain loss, the value of $R_1$ is kept small. The drain inductor ($L_d$) and

drain resistor ($R_d$) were used to provide good RF output matching over the operating frequency, and, hence, ensure the stability of the LNA.

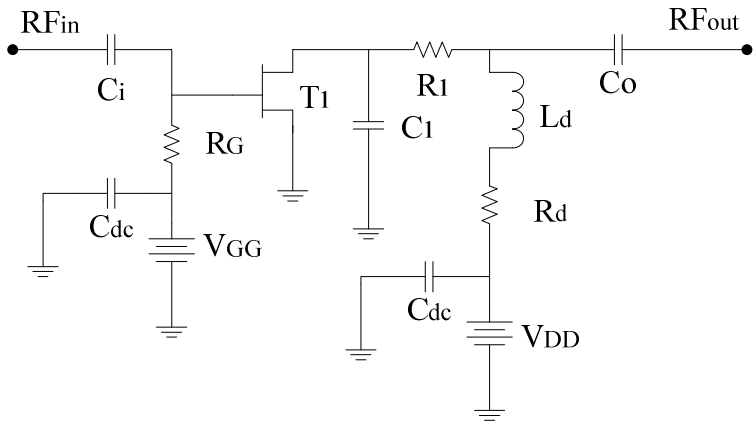



Figure 6-16 Schematic diagram of SSLNA using 4 x 200 µm InP pHEMTs

### 6.4.2 Double Stage Single-ended LNA

In this section, two types of Double Stage Single-ended MMIC LNA (DSLNA) are described, namely, High-gain DSLNA (HG-DSLNA) and Moderate-gain DSLNA (MG- DSLNA). Here, two amplifiers are cascaded together to present low noise as well as higher gains compared to the SSLNA design [104]. In the design, given that the first stage sets the noise performance of the entire circuit, it is designed to have the lowest possible noise figure. The second stage is therefore designed for gain optimisation to the desired value. Thus, in general, the two-stage topology is used to improve the gain as well optimising the noise performance. Similar to the SSLNA, the amplifiers were designed to operate at the same frequency range of 0.4 GHz to 2 GHz.

#### 6.4.2.1 High-gain Double Stages Single-ended MMIC LNA (HG-DSLNA)

An illustration of the HG-DSLNA schematic diagram is depicted in Figure 6-17. As can be seen in the schematic, the two common-source amplifiers are cascaded together by the inter-stage matching capacitor ($C_M$). $C_M$ is also used to isolate the

gate DC supply ($V_{GG}$) of the second stage from the RF output of the first stage. Similar to the SSLNA design, the series input/output capacitor ($C_i$ and $C_O$) still functions as the DC blocking capacitor. $C_{dc}$ still works as the DC coupling capacitor to isolate the RF signal from the DC supplies ($V_{GG}$ and $V_{DD}$).

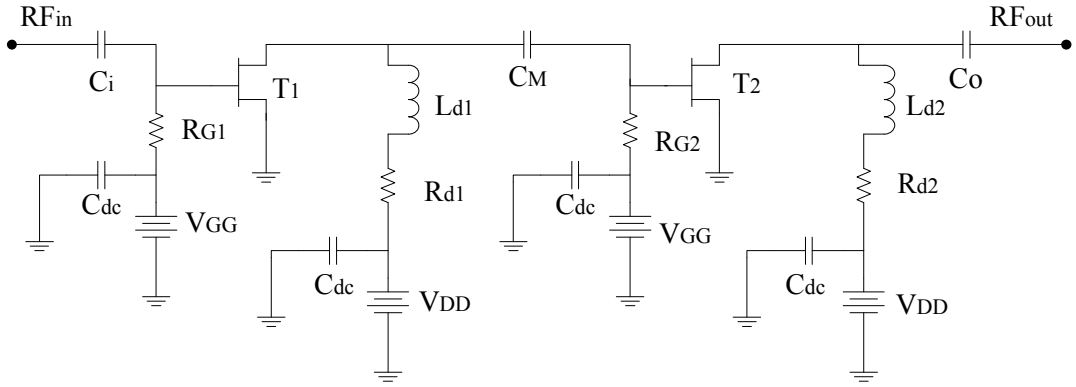



Figure 6-17 Schematic diagram of HG-DSLNA using 4 x 200 µm InP pHEMTs

At the first stage amplifier, again, the high gate resistance ($R_G$) is used at the gate input for low noise biasing. The capacitor $C_M$, inductor $L_{d1}$, and resistor $R_{d1}$ act as the inter-stage matching network of the first stage as well as improve the amplifier stability at higher frequency.

In the second stage, however, due to the inter-stage matching network ($C_M$, $L_{d1}$ and $R_{d1}$) the value for resister $R_{G2}$ is half of $R_{G1}$. $R_{G2}$ is also used to ensure that transistor $T_2$ is at its optimum noise condition biasing. $L_{d2}$ and $R_{d2}$ is the output matching network of the second amplifier for the circuit stability.

Here, the values for passive elements in this LNA circuit have been adjusted as a result of the existence of the inter-stage matching components ($C_M$, $L_{d1}$, and $R_{d1}$) and for the circuit's low noise characteristics. For this reason, although the amplifier in the first stage is an adaptation from the previously designed SSLNA, the passive values for this DSLNA were not the same. Transistors $T_1$ and $T_2$ are biased at $V_{DS}$ = 1 V, $V_{GS}$ = -0.92 V and $I_{DS}$ = 22 mA. This time, the LNA is designed to have a gain of ~ 35 dB.

### 6.4.2.2 Moderate-gain Double Stages Single-ended MMIC LNA (MG-DSLNA)

The schematic diagram for this MG-DSLNA is shown in Figure 6-18. This design is simpler compared to the design in the previous section because no matching inductors were used at the output port of each amplifier. Accordingly, only resistors $R_{d1}$ and $R_{d2}$ were used for the RF matching network. In this design, the transistor gain is set to be of moderate value (~25 dB), even though this topology is capable of achieving as good performance as the high gain LNA.

The other circuit components and their functions on this amplifier are the same as the HG-DSLNA with a small adjustment on each passive value. In this design, the transistors $T_1$ and $T_2$ are biased at $V_{DS}$ = 1 V, $V_{GS}$ = -0.92 V and $I_{DS}$ = 22 mA.

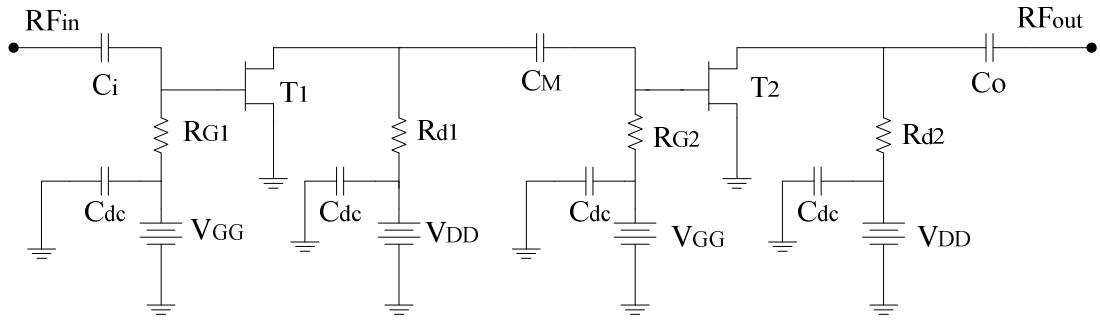



Figure 6-18 Schematic diagram of MG-DSLNA designed using 4 x 200 µm InP pHEMTs

## 6.5 FABRICATION OF LNA

In this section, the fabrication of the passive and active devices discussed earlier is extended to the fabrication of a fully on-chip LNA using MMIC technology. As already mentioned the active device used is the 4 x 200 µm and fabricated on a VMBE #2100 epitaxial layer.

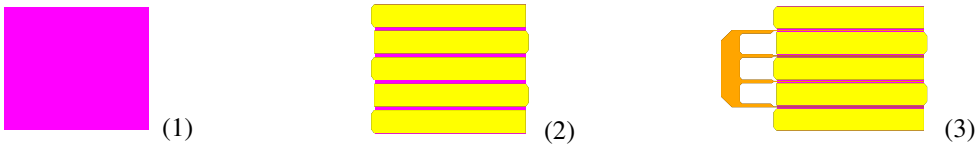
In general, all circuit designs use common source topology where the DC and RF input are connected to the gate and drain terminal. The circuits are biased at low values of $V_{DS}$ and $V_{GS}$ region for very low noise and low power characteristic [90]. All three designed LNAs described previously were fabricated.

### 6.5.1 Mask Design

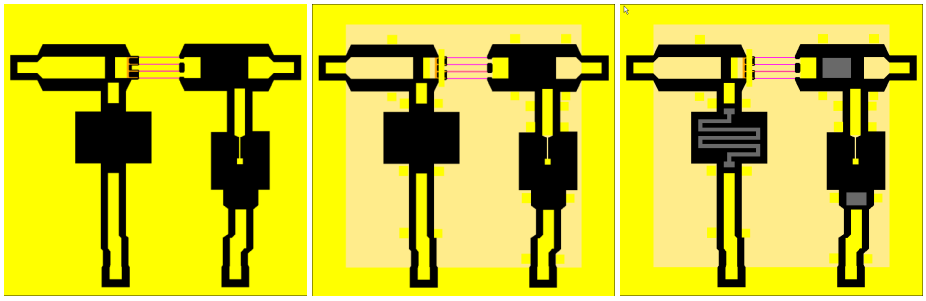
In this work all SSLNA, HG-DSLNA and MG-DSLNA are fabricated on the same sample, which undergoes the same chemical processes at the same time. The graphical representation of each layer mask and the complete fabricated MMIC ICs are shown in Figure 6-19, Figure 6-20 and Figure 6-21 for SSLNA, HG-DSLNA and MG-DSLNA, respectively. The fabrication steps involved for active and passive devices and metal interconnection are listed in Figure 4-3 and Figure 6-2, but will be briefly explained here with the aid of the mask layout.

In the figures, the fabrication started with the formation of MESA (Mask 1- MESA) for the active area definition. Then, the 50/400 nm of Ti/Au was thermally evaporated and the resist opening filled at the Ohmic location (Mask 2- Ohmic) followed by the lift-off process. Next, the gate fingers are defined (Mask 3- Gate) by lithography and the gate recess took place before the 50/400 nm of Ti/Au metallisation scheme was thermally evaporated and lifted-off. After that, the first metal interconnection, as well as the bottom plate for the capacitors and inductors were thermally evaporated and lifted-off forming 50/400 nm thickness of Ti/Au (Mask 4 – Metal 1). Subsequently, 90 nm of $Si_3N_4$ was deposited under a low temperature plasma deposition process, and nitride opening took place at the designated contact area by $CF_4$ and $O_2$ plasma etches (Mask 5 – Nitride etch). Afterwards, a thin NiCr film was sputtered (Mask 6 – NiCr) before the thermal deposition and lift-off of the second metal interconnection (Mask 7 – Metal 2). Metal 2 also incorporated a top metal plate for capacitors and metal structures for spiral inductors. Subsequently, a dielectric bridge made from SF11 (Mask 8 – dielectric bridge) was formed where 50/400 nm of Ti/Au metal bridge (Mask 9 – Metal bridge) is located. The fabrication was completed by the hardened resist passivation layer for proper RF shielding to the MMIC circuits (Mask 10 – passivation).

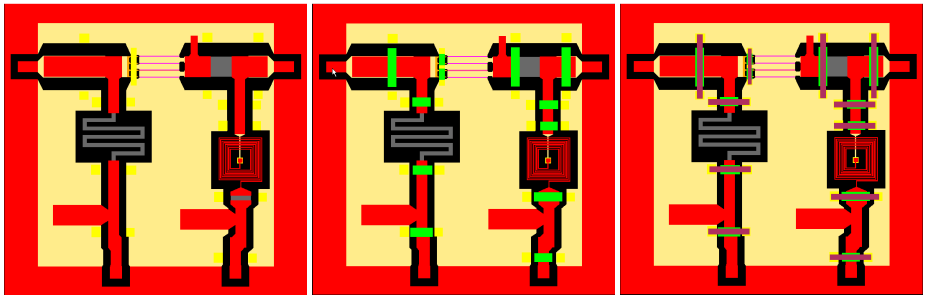
Note that for SSLNA, only one transistor is used to power up the circuit, whereas in DSLNAs the circuits are made of two transistors. The total chip area for the LNAs are 1.5 x 1.5 $mm^2$, 1.6 x 2.5 $mm^2$ and 1.8 x 2.7 $mm^2$ for SSLNA, HG-DSLNA and MG-DSLNA, respectively.



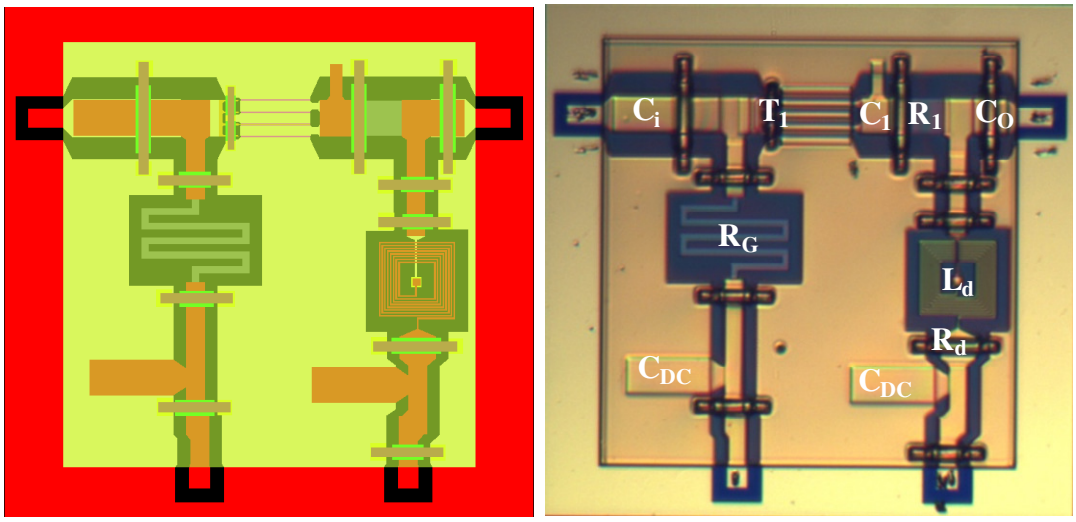
(1) (2) (3)



(4) (5) (6)



(7) (8) (9)




(10) (11)

Figure 6-19 Mask layout for SSLNA (1) MESA, (2) Ohmic, (3) Gate, (4) Metal 1, (5) $Si_3N_4$ Deposition and etch, (6) NiCr, (7) Metal 2, (8) Dielectric Bridge, (9) Metal Bridge, (10) Passivation, and (11) Fabricated MMIC SSLNA

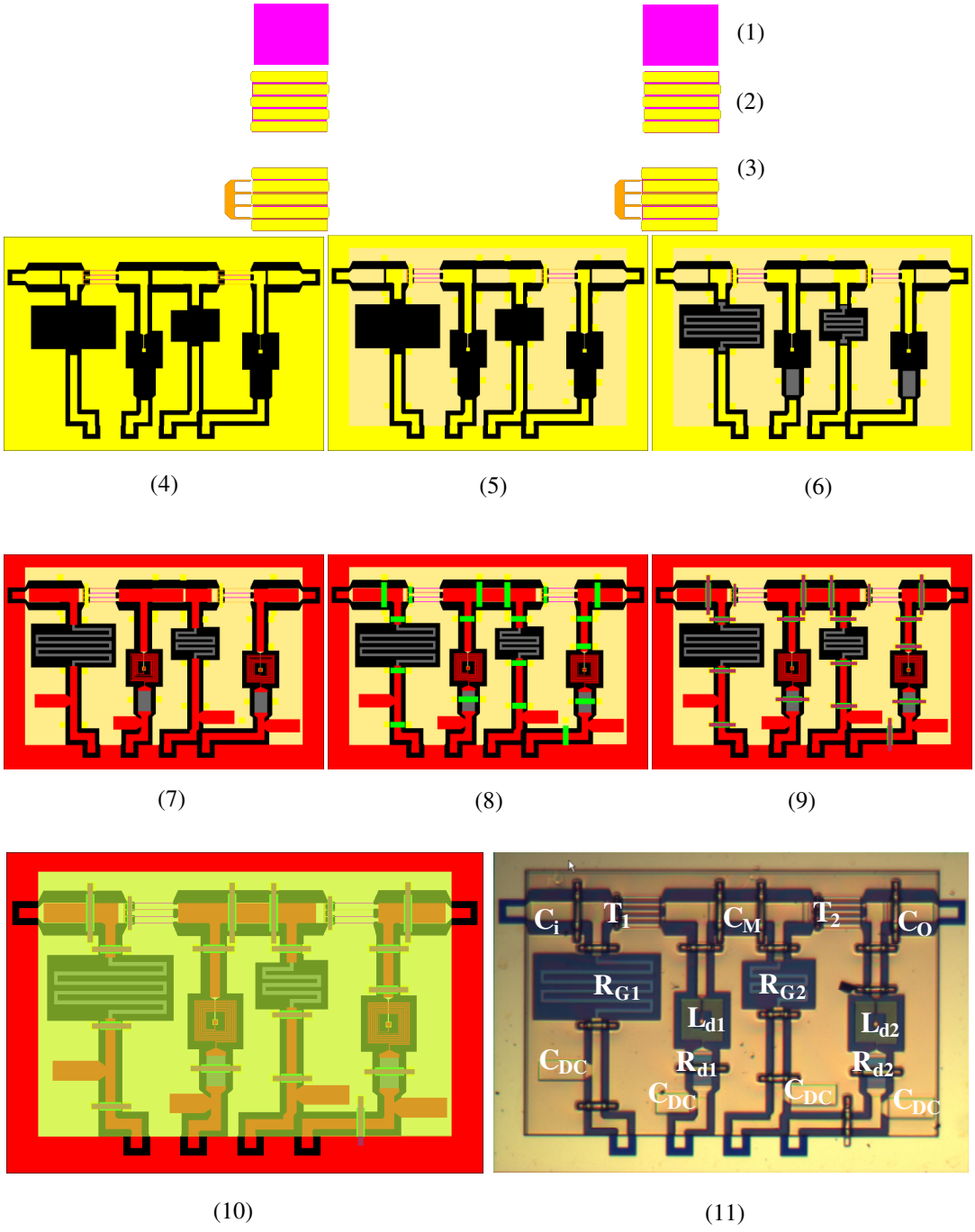



Figure 6-20 Mask layout for HG-DSLNA (1) MESA, (2) Ohmic, (3) Gate, (4) Metal 1, (5) $Si_3N_4$ Deposition and etch, (6) NiCr, (7) Metal 2, (8) Dielectric Bridge, (9) Metal Bridge, (10) Passivation, and (11) Fabricated MMIC HG-DSLNA

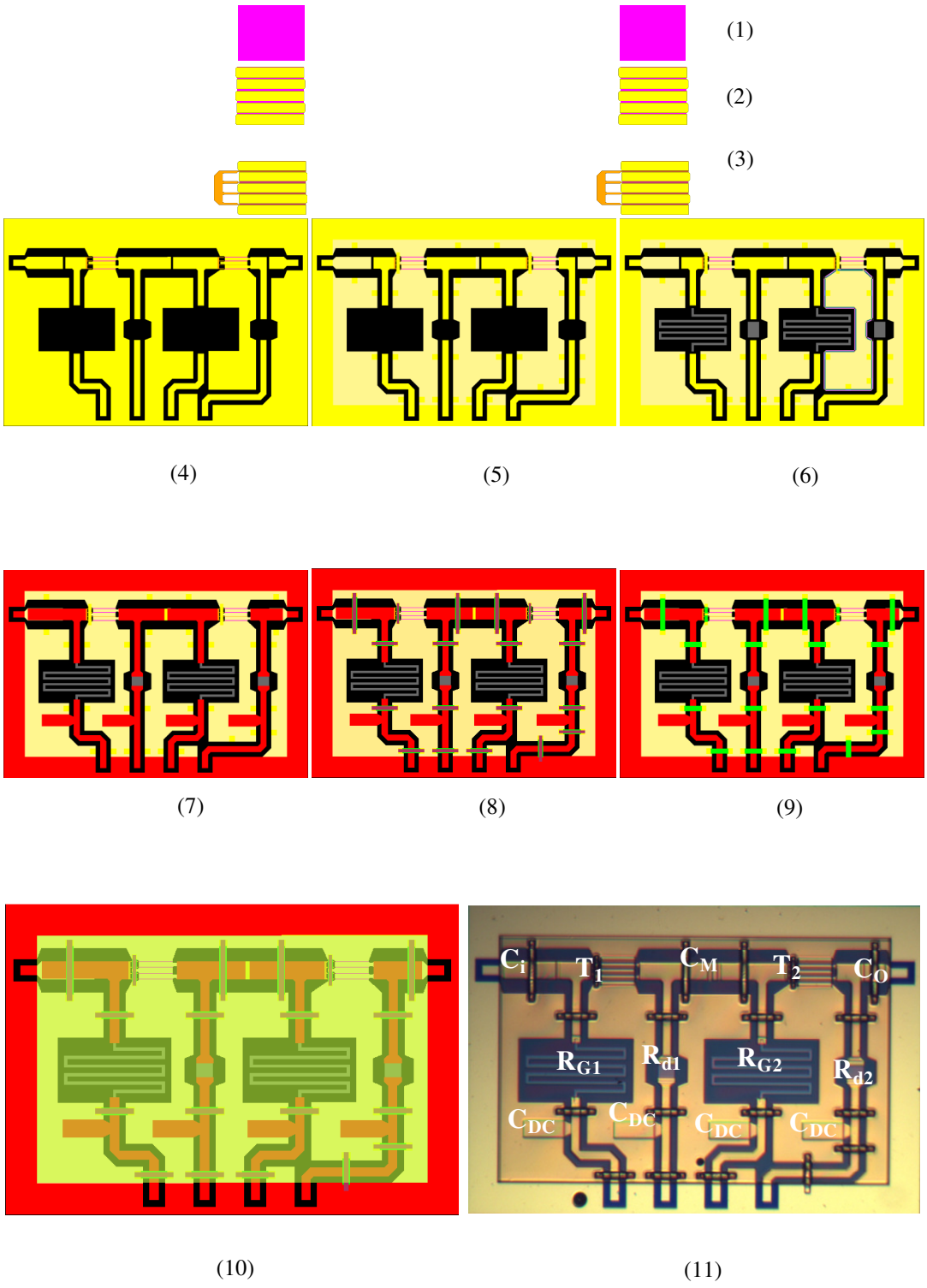
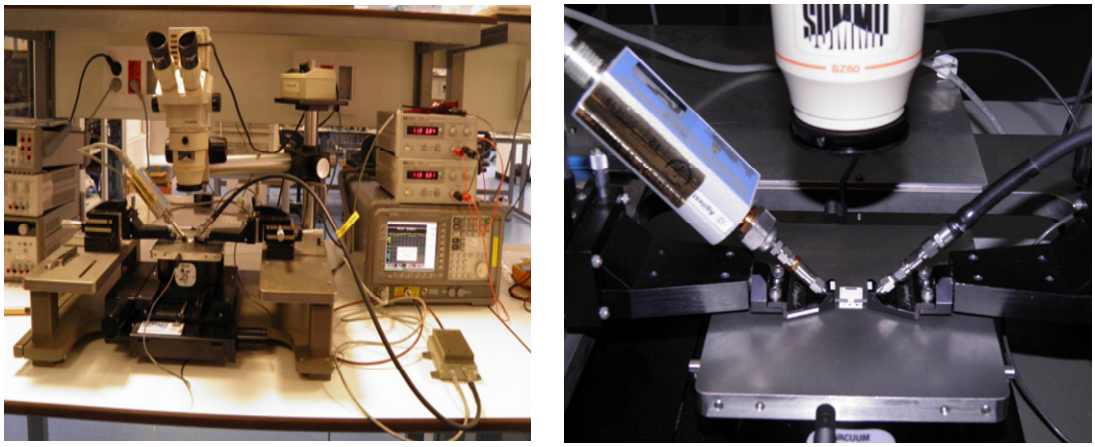



Figure 6-21 Mask layout for MG-DSLNA (1) MESA, (2) Ohmic, (3) Gate, (4) Metal 1, (5) $Si_3N_4$ Deposition and etch, (6) NiCr, (7) Metal 2, (8) Dielectric Bridge, (9) Metal Bridge, (10) Passivation, and (11) Fabricated MMIC MG-DSLNA

## 6.6 S-PARAMETER AND NOISE MEASUREMENT

The S-parameters and noise figure measurements for all LNAs were performed at the University of Cantabria, Spain. The author has no involvement in this S-parameter and noise figure measurements. The measurements were carried out at room temperature on a Cascade Microtech 9000 RF Coplanar Probe Station using 50 Ω input/output impedance systems. The S-parameters and noise figure measurements were analysed using a Vectorial Network Analyzer, PNA E8364A. The circuits are measured at a frequency range of 200 MHz to 4.2 GHz with a step of 10 MHz (401 points). The power of the PNA generator is -20 dBm with an intermediate frequency (IF) bandwidth of 1 kHz. An illustration of the complete setup is shown in Figure 6-22 (a) and a close-up of the Short-Open-Load-Thru (SOLT) CS-5 calibration standard on two ports network is depicted in Figure 6-22 (b).



(a) (b)

Figure 6-22 S-parameter and noise measurement setup (a) A complete setup for noise figure measurement and (b) A close up calibration standard at two port network using CS-5 calibration substrate

In subsequent sections, even though the circuit is optimised for a frequency range of 0.4 GHz to 1.4 GHz, the presented data were shown in a wider frequency range from 0.4 GHz to 2.0 GHz to observe the behaviour of the circuits beyond the bound frequencies. For each type of the LNA, the data shown in all figures in this section are from the best data obtained from measurement of four different circuits. Since each component in the circuit is having their own error (about 10 %) , this time the total error between those circuits has increased to a variation of 20%.

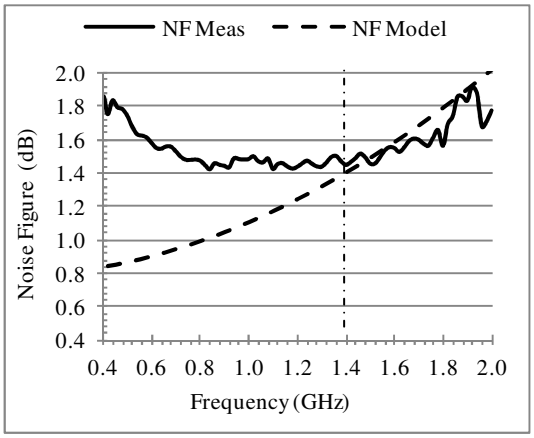
### 6.6.1 NF and S-parameters: SSLNA

Figure 6-23 (a) – (e) show the comparisons between the measured and modelled data for noise figure and S-parameters of the SSLNA design. In general, all the measured and modelled data show excellent agreement with each other.

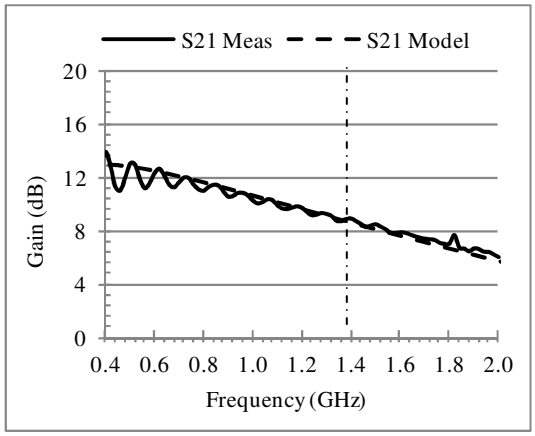
By referring to Figure 6-23 (a), the measured noise figure (*NF)* is reduced from 1.8 dB to 1.5 dB over the frequency range, whereas the simulated data showed an increase in the *NF* from 0.8 dB to 1.4 dB at a frequency of 0.4 GHz and 1.4 GHz, respectively. At a closer look, the *NF* between the measured and simulated data shows a wider gap but starts to converge above a frequency of 1.4 GHz. For example, at a frequency of 0.4 GHz, the difference is ~ 1.0 dB, while it is about 0.2 dB at 1.8 GHz. The reason behind the mismatch at low frequency may arise from the passive mismatch due to the Q factor of the inductor, leakage current that might be present and a non-optimal noise model for the transistor. The mismatch due to the inductor Q factor has been highlighted in section 6.3.3.

The plots between the modelled and measured S-parameters for SSLNA are shown in Figure 6-23. In general, both data show excellent agreement with each other.

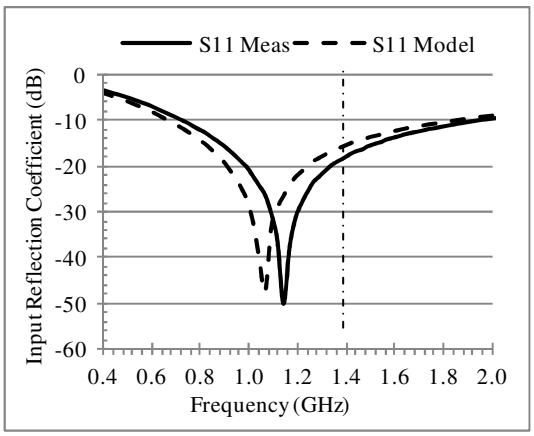
As illustrated in Figure 6-23(b), the simulated gain (S21) is comparable to the measured data over the frequency band. From the plot, both the modelled and measured gain is approximately 13 dB at 0.4 GHz and 9 dB at 1.4 GHz. This gain, however, is considered small for SKA or other wireless applications, and, hence, can be improved by the adaptation of a double stage design. The input and output reflection coefficient (S11 and S22) are well below the 0 dB line for both measured and simulated data, which reflects that the LNA has very good input and output match. However, there was only small difference of ~2 dB between the measured and modelled S11 and S22 at frequencies less than 1.0 GHz. The LNA also showed unconditional stability over 10 GHz. However, for comparison purposes, the data for the Rollet stability factor (K) are shown up to 5 GHz. The stability factor, K is presented in Figure 6-23 (e). The power consumption of this circuit is 66 mW when biased at $V_{DD}$= 3 V supply with $I_{DS}$ = 22 mA.



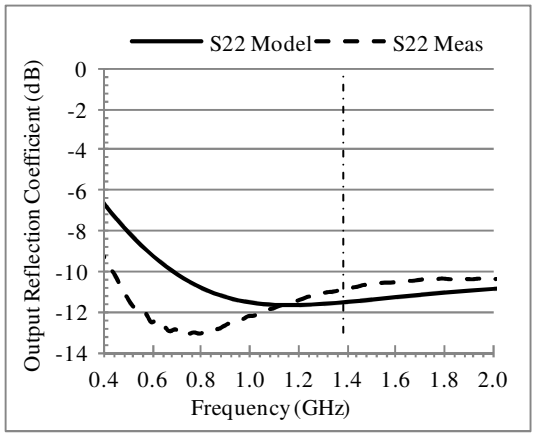

(a)



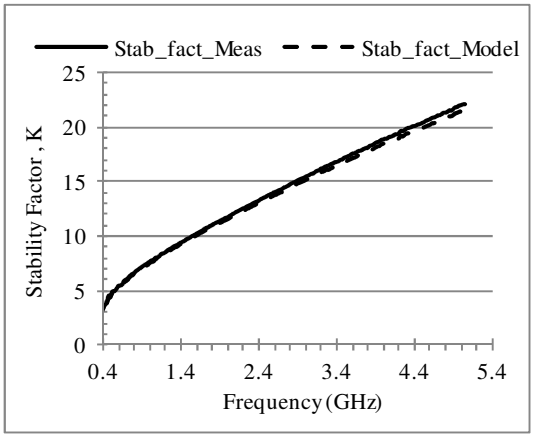

(b)




(c)




(d)




(e)

Figure 6-23 Comparison of measured vs. simulated for SSLNA (a) noise figure (NF) against frequency, (b) gain (S21) against frequency (c) and (d) input/output reflection coefficient (S11, S22) against frequency, and (e) of Rollet stability factor (K) against frequency.

### 6.6.2 NF and S-parameters: HG-DSLNA

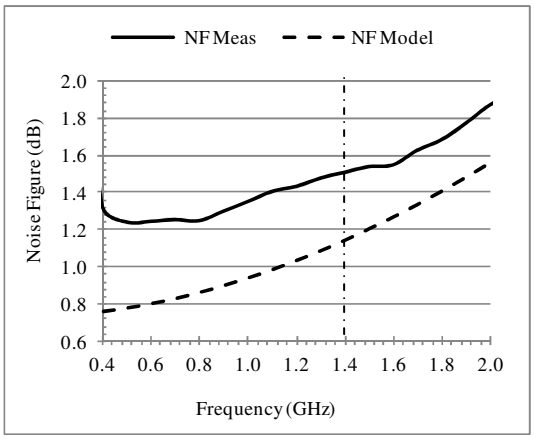
The measured and simulated data for HG-DSLNA are shown in Figure 6-24(a) and Figure 6-24 (b) for noise figure (*NF*) and gain (S21), respectively.

Comparing the measured and modelled *NF* data, there is 0.4 dB difference between the two data sets over the frequency range. The measured *NF* varies from 1.2 dB to 1.5 dB from 0.4 GHz to 1.4 GHz, whereas a lower *NF* is obtained from simulation (0.8 dB to 1.1 dB) across the same frequency. In addition to the mismatch addressed in the SSLNA design, since, in this design, more passive elements are used in the circuit design, more parasitic resistors, inductors and capacitors are introduced, which result in this mismatch.

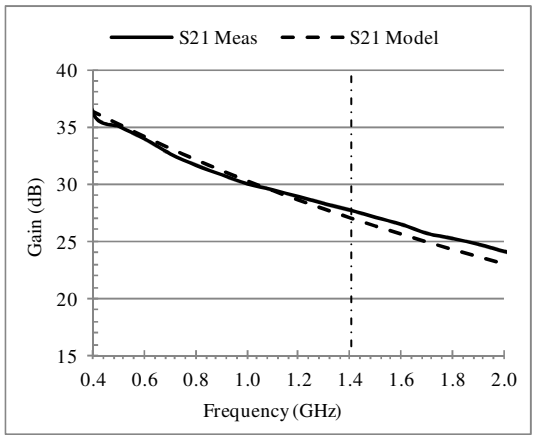
The gain, however, shows excellent agreement between the measured and modelled data. As mentioned in section 6.6.1, the LNAs' gain can be improved by cascading the first stage amplifier with another common-source amplifier at the first stage output port [104]. Now, the gain has increased to 36 dB at 0.4 GHz, which is an increment of 23 dB, compared to the single stage design. At 1.4 GHz, the gain has increased to 28 dB, as compared to 9 dB for SSLNA.

However, the measured input and output reflection coefficients (S11 & S22) and stability factor (K) for this amplifier were not measured at this stage. Nevertheless, the simulated data for both parameters are depicted in Figure 6-24 (a) and Figure 6-24 (b), respectively. The simulated data show that the LNA demonstrated unconditional stability up to the range of interest with good input and output reflection coefficients (S11 and S22). However, the small value of K indicates that the LNA is near the oscillation boundary, and hence there is a possibility of instability.

With a supply voltage $V_{DD} = 3$ V, the total output current for both stages is 41.6 mA, from which the net power consumption for this LNA is 125 mW.

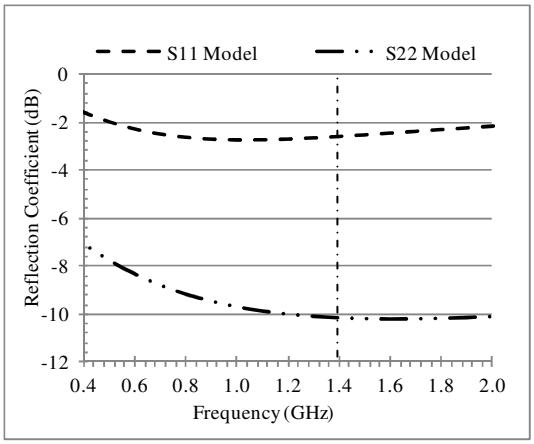



(a)

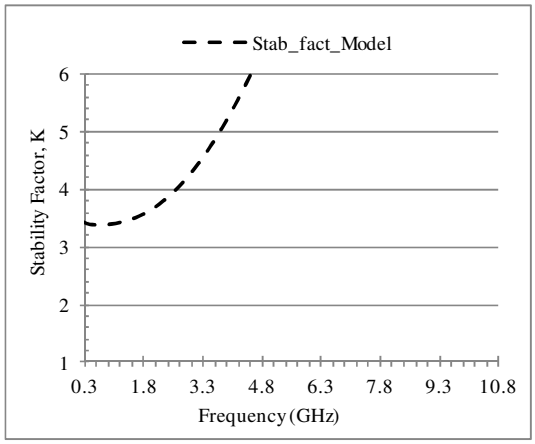



(b)

Figure 6-24 Comparisons of measured and simulated data for HG-SSLNA (a) noise figure (NF) against frequency, (b) gain (S21) against frequency




(a)

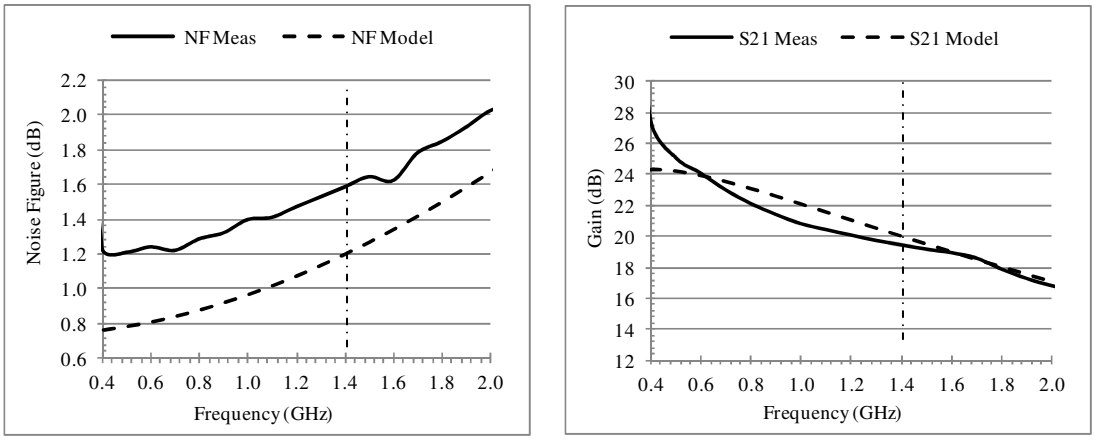



(b)

Figure 6-25 Simulated data for HG-DSLNA (a) Input and output reflection coefficient (S11 & S22) against frequency, (b) Rollet stability factor (K) against frequency

### 6.6.3 NF and S-parameters: MG-DSLNA

The comparisons between measured and simulated data for MG-DSLNA are depicted in Figure 6-26, where subscript (a) shows the *NF* while (b) shows the S21 gain. The difference between measured and modelled in *NF* was expected due to the same reasons given for the first two designs. Note that all LNAs presented in this work were fabricated using the same mask and underwent the same process at the same time, thus, resulting in the same circuit behaviour. Keep in mind that in this circuit design, no inductors were used at the output matching network in contrast to the previous HG-DSLNA design.




(a) (b)

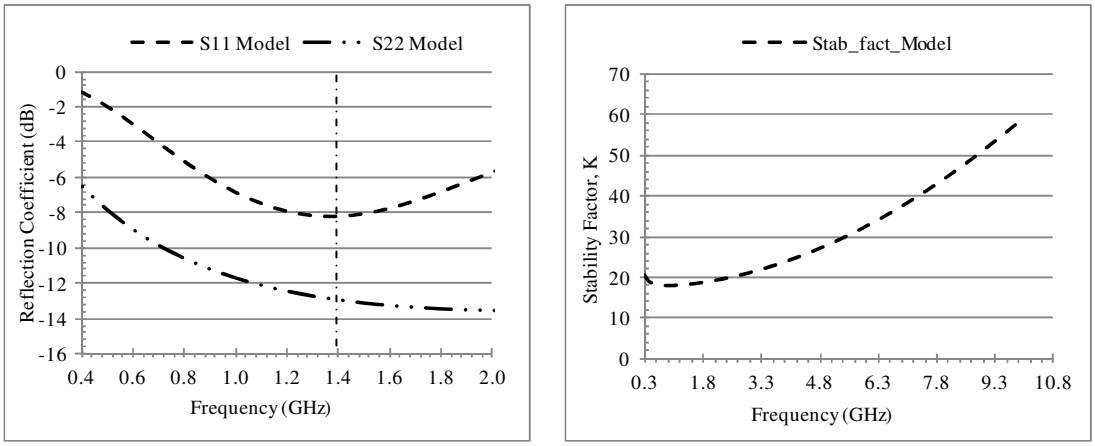
Figure 6-26 Comparisons of simulated and measured data for MG-SSLNA (a) noise figure (NF) against frequency, (b) gain (S21) against frequency

By referring to Figure 6-26 (a), the MG-DSLNA (no inductors) design still offered comparable *NF* performance with the HG-DSLNA (designs with inductors). Across the frequency of interest, the measured *NF* is between 1.2 dB to 1.6 dB and the simulated data showing *NF* between 0.8 dB to 1.2 dB, the small discrepancies of 0.4 dB can be explained by a non-optimum noise model for the transistors used.

As shown in Figure 6-26 (b) across 0.4 GHz to 1.4 GHz, the S21 gain for both measured and simulated data vary from 25 dB to 20 dB. A higher gain was achieved in the previous second stage design where S21 of 36 dB to 28 dB were recorded.

Figure 6-27(a) and Figure 6-27(b) show the simulated input/output reflection coefficient (S11 and S22) and stability factor (K). Compared to the previous design, the S11 and S22 values are more negative, indicating that almost all the microwaves have been passed through the input/output port with less reflection. In addition, this LNA has a Rollet stability factor (K), 20 times better than the previous design.

The power consumption for this design is 138 mW with 23 mA drain current at each stage from a $V_{DD}$ = 3 V supply.




(a) (b)

Figure 6-27 Simulated data for MG-DSLNA (a) Input and output reflection coefficient (S11 & S22) against frequency, (b) of Rollet stability factor (K) against frequency

## 6.7 LNA PERFORMANCES

Researchers around the globe including those from industries have designed sets of diverse amplifiers with very competitive and promising performance. In this section, a short outline of the different LNAs reported in a similar frequency range is provided. As a summary, Table 6-5 shows the comparison between the in-house fabricated HG-DSLNA and the LNAs obtained by other researchers.

Table 6-5 Table comparing the in-house fabricated LNA with the LNA obtained by other researchers

| **Reference** | Xu et al. | Belostotski and Haslett | Bardin and Weinreb | Witvers et al. | Kuger | This work |
|---|---|---|---|---|---|---|
| **Year** | 2005 | 2007 | 2009 | 2010 | 2012 | 2012 |
| **Bandwidth (GHz)** | 0.6 to 1.6 | 0.8 to 1.4 | 0.1 to 5.0 | 0.6 to 1.8 | 0.9 to 1.8 | 0.4 to1.4 |
| **Technology** | GaAs 200 nm | MMIC + off-chip CMOS 90 nm | MMIC + off-chip SiGe HBT 0.12 µm | MMIC + off-chip GaAs 70 nm | MIC GaAs | **MMIC InP 1 µm** |
| **Sim. or Meas. NF (dB)** | 0.5 Sim. | < 0.2 Sim. | 0.9 Meas. | < 0.4 Meas. | 0.36 Meas. | <1.5 Meas. |
| **Gain @ 1.4 GHz (dB)** | 20 | 19 | 28.3 | 18 | 27 | 27 |
| **Power Consumption (mW)** | 1000 | 43 | 76 | Not Available | 100 | 125 |
| **Stability** | Not Specified | Not specified | Not Specified | Not Specified | Unconditionally stable | Unconditionally stable |
| **Impedance** | 50 Ω | Input = 85Ω | 50 Ω | Input = 150 Ω | 50 Ω | 50 Ω |
| **LNA Size ($mm^2$)** | Large (Off-chip) | 1.1 x 0.75 | 0.5 to 0.6 | Large (Off-chip) | 46 x 35 | **1.6 x 2.5** |

In the first comparison, Xu, et al. [105] designed an LNA with a dual-loop negative feedback topology using sub-micron (200 nm) GaAs technology. Note that the output impedance is simulated at 20 Ω. Their simulated design has shown *NF* below 0.5 dB across a frequency range of 0.6 GHz to 1.6 GHz. However, the simulated LNA employed the off-chip matching components of the input and output ports. The discrete components will provide better microwave matching, and, therefore, a low Noise Figure is expected. For this reason, the total chip area of the LNA is expected to be large. Furthermore, the power dissipated for their LNA is ~ 10 times higher than in our design.

Another LNA design using 90 nm CMOS transistors cascaded together was proposed by Belostotski and Haslett [106]. They demonstrated that their LNA showed sub-0.2 dB *NF* at a frequency range of 0.8 GHz to 1.4 GHz. However, the higher source impedance was used in their simulation (85 Ω). In addition, their design still incorporated off-chip components, which help to pull down the *NF* to a lower value. Since nano-devices are used in their design, only 43 mW of power is dissipated from their circuit.

Included in the comparisons is the LNA design proposed by Bardin and Weinreb [107]. Their circuit was fabricated using the 0.12 μm IBM BiCMOS8HP process, where the SiGe Heterojunction Bipolar Transistor (HBT) transistors were used as the active device in their design. However, their amplifier still contain some off-chip components which pulled down the noise to 0.9 dB. This design added another selection of materials that can be used for the low noise applications.

Another cascaded LNA design was reported by Witvers et al. [108]. In their design, they used large off-chip inductance to match the high input impedance (150 Ω) source. Their first stage also incorporates 6 gate finger devices to reduce the low noise resistance, and, consequently, the noise behaviour of the circuit. They used GaAs technology with a gate length of ~ 70 nm using e-beam lithography.

The most recent LNA design using GaAs devices was presented by Kuger [109]. His design had an excellent *NF* of 0.36 dB across the frequency 0.9 GHz to 1.8 GHz. His design used the multipath technique where better matching can be achieved over a

larger frequency band [110] with input/output impedances matched to 50 Ω sources. The design is unconditionally stable, with S21 gains over 27 dB across the frequency and only dissipates 100 mW of power. However, the LNA size is the largest (46 x 35 $mm^2$) due to the fully discrete components that were used. The design is unconditionally stable, considerably high gain (27 dB) and dissipates 100 mW of power.

In this work, InP technology with 1 µm gate length is used to design the fully on-chip MMIC LNA. The LNA was fabricated using conventional I-line optical lithography process at the University of Manchester. The measured *NF* of < 1.6 dB is higher than the simulated value, which largely correlates with the low inductor's Q factor and a non-optimal noise model for the transistor, and to a certain extent the gate length of 1 µm, the largest used in all studies. These low cost optically processed LNA provide a high gain of 27 dB at 1.4 GHz with a considerably low power dissipation of 125 mW. The chip area for this LNA is only 1.6 x 2.5 $mm^2$.

## 6.8 SUMMARY

In this chapter, the passive components were fabricated and characterised. The fabricated capacitor, resistor and inductor were comparable with the designed values. However, additional series resistance and low Q factor from inductor at the output network has affected the microwave matching, especially in the low frequency performance of all LNAs.

In brief, three fully on-chip MMIC designs based on the modelled transistor and lump elements have been presented. A selection of transistor with 4 x 200 µm gate width and 1 µm gate length was used in those designs. A large transistor width was chosen in the design to pull down the noise resistance ($R_n$), and, consequently, the noise characteristics of the LNAs. In this work, a common-source configuration with high value of gate resistance was applied in the designs for better DC biasing at the active device inputs.

\The simulation S-parameter data showed excellent agreement with the measured data in the frequency range of 0.4 GHz to 1.4 GHz. The discrepancies in the noise figure parameter were also discussed in this chapter.

The maximum gain of 25 dB and 36 dB was achieved from both MG-DSLNA and HG-DSLNA design, which met the design specification. The power dissipation for these LNAs was considered small from a 1 μm gate length process. The highest power obtained for these designs was from the MG-DSLNA with only 138 mW. The designed LNAs also demonstrated unconditionally stabile with the stability factor (K) well above one (1) over 10 GHz.

By referring to the design specifications in Section 1.3.1, all these results fulfilled most of the design requirements set at the beginning of the project. However, the highest measured *NF* from the amplifier was about 0.6 dB higher than the targeted value (1 dB). The improvement of the *NF* will be addressed in Chapter 7 for future work and recommendations.

At the end of this chapter, several comparisons were made with other LNAs operated on similar frequency bandwidth. Compared to other designs, our work in this research has the advantages of accomplishing the design specifications by fully on-chip design and low manufacturing cost from 1 μm optical lithography process.

# CHAPTER 7

# CONCLUSIONS AND FUTURE WORK

## 7.1 CONCLUSIONS

The main objective in this work was to develop and fabricate low noise amplifiers (LNAs) dedicated to the mid-frequency range of the SKA radio astronomy telescope operating between 0.4 GHz to 1.4 GHz.

Along the journey leading to the accomplishment of this objective, a great deal of design, fabrication and characterisation of InGaAs/InAlAs pHEMTs suitable for low-frequency applications in the LNA circuit design were undertaken. The 1 μm gate length device has shown its worth in physical properties resulting in lower gate leakage, appropriate cut-off frequency ($f_T$) and high value in its transconductance ($g_m$) by means of careful manipulation of the material's energy band-gaps.

These properties are indispensable for high breakdown and low noise performance for the design of the LNA circuits. The implementation of large geometry pHEMT devices has pulled down the system's noise resistance ($R_n$), simplifying the design of wide band low noise amplifiers as required in the broadband low-frequency SKA receivers.

To this effect a novel high breakdown InGaAs-InAlAs pHEMTs incorporating improved epitaxial layer and field plate structures has been successfully fabricated and characterised in this work. The newly developed field plate devices have demonstrated appreciable improvement in $V_{BR}$ value , with a significant reduction of both off-state (Schottky) and on-state leakage currents while maintaining its excellent Radio Frequency (RF) performance. The low noise and high breakdown voltage properties show promise for applications in high voltage, high efficiency Power Amplifiers (PAs), robust LNAs with streamlined protection circuitry as well as integrated RF transceivers, optimized for low-noise receivers and high-power PA transmitters in the mobile telephone band and up to X-band (10 GHz).

These devices are the culmination of the process optimisation that was conducted earlier. The improvements involved gate recess steps, gate to channel isolation technique and the device's temperature stability.

The MMIC circuits presented in Chapter 6 have achieved a number of design targets that are required for integration into the SKA circuits. The single stage design has shown high stability and low noise measure (<1.8 dB), but does not present sufficiently high gain. However, the low gain is tackled by the second stage design without compromising its high stability and low noise characteristics. Another choice of design without inductors at the input ports was also carried out as an attempt to reduce the noise characteristic and other S-parameters values. Interestingly, this design marginally improved the input reflection coefficient and stability but no noticeable improvement is seen in the circuit's noise performance. The circuit noise levels are comparable with the designs incorporating inductors.

Overall the Noise Figures obtained are larger than the specification required by the SKA (~ 0.5 dB) and therefore the discrepancy between modelled and measured values of 0.2 dB to 1.0 dB over the frequency range of 0.4 GHz to 1.4 GHz need resolving via the use of shorter gate length.

While the SKA remained the primary focus of this effort, the LNAs presented here have high potential in other commercial markets. Opportunities may be identified for the use of these LNAs in various commercial industries, such as mobile phones, satellite receivers, global positioning systems (GPS) and satellite navigation systems.

In conclusion, the MMIC LNA design presented in this work hold promises for use in the SKA front-end requirement provided steps are found to reduce the noise further.

## 7.2 FUTURE WORK

A great deal of work has been done in the area of producing high performance wide-band LNAs suitable for radio-astronomy applications, especially for future telescopes, such as the square kilometre array (SKA) system. As a continuation from

the work conducted in this project, listed below are the three key important areas for future improvement. Some areas are already underway, which include:

a. The variations between the modelled and measured data are mainly caused by the parasitic value from passive components. The effect of the parasitic value can be minimised by substituting the parasitic values in the design while adjusting the circuit's passive value to compensate for the increase in each of the passive values.

b. By referring to the RF biasing point, most of the time the circuit is biased at a location where there is a discrepancy between the modelled and measur$_{ed}$ $I_{DS}$ current due to its kink effect. A better modelling technique, which includes the kink effect, may reduce the inconsistency between the modelled and measured noise characteristics.

c. Notwithstanding the suitability of the 1 µm gate length to deliver the low noise characteristic, further work on highly-scaled pHEMTs should follow as the foremost priority. Rather than expensive, yet low throughput e-beam lithography, a more hassle-free and highly dynamic sub-micron process has been developed and is currently being carried out at Manchester. This process, called "soft reflow" technique, takes advantage of the low temperature reflow process using solvent as the reflow agent, and 0.35 µm gate length synthesised using 1 µm opening with excellent DC and RF characteristics have recently been developed. This technique holds much promise in reducing the noise levels (as a result of the very large increase in $f_T$) to the SKA specifications while preserving the use of low cost I-line lithography.

# APPENDIX A: CONVENTIONAL pHEMT PROCESSING STEPS

| Structure | Step # | Step Name | Chemistry | Equipment | Temp | Time | Comments |
|---|---|---|---|---|---|---|---|
| MESA | 1.1 | Clean | NMP + DI , Acetone (red), IPA (blue) | USP | | 5m each | Finally dry the sample with $N_2$ |
| | 1.2 | Preheat | | Hotplate | 120°C | 1m (HP) + 1m (RT) | * if temp > 120 °C, need to cool down to RT before storing into sample box |
| | 1.3 | Resist Coating | Photoresist : S1805 | | | 30s | Program-4 (Acc=2000, rpm=4000,time=30s) |
| | 1.4 | Prebake | | Hotplate | 115°C | 1m (HP) + 1m (RT) | Expose sample to RT environment for 1m for homogenisation |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | 1.5 | Exposure | | MA4 | | 20s | Intensity=0.9mW/cm$^2$ i-line. Read Mask Aligner document for details. |
| | 1.6 | Develop S1805 | MIF 319 | | | 1m | |
| | 1.7 | Post-bake | | Oven | 120°C | 30m (Ov) + 1m(RT) | to harden the remaining resist before etch |
| | 1.8 | Etch | $H_3PO_4$:$H_2O_2$:$H_2O$ (3:1:50) *$H_2O_2$ High grade | | RT | 1m30s | 15:5:250 ml.<br>Mesa height ~ 150nm. Orthophosphoric<br>etches rate ~100nm/min InGaAs/InAlAs type pHEMT<br>*etches rate ~80nm/min GaAs/InAlAs type pHEMT*<br>It doesn't etch InP<br>etch to buffer layer (150nm = 1m 30s) |
| | 1.9 | Side Wall etch | Succinic acid powder (10g), $H_2O$ (50ml), Ammonia (~10ml to pH of 5.5), $H_2O_2$ (5 ml) | pH meter | RT | 10m | Succinic Etch<br>InGaAs etch rate = 240A/min<br>InAlAs etch rate = 2A/min<br>Etch 50A InGaAs layer<br>InGaAs/InAlAs selectivity 120:1<br>Allow the solution to settle for 5m before etching.<br>Add $H_2O_2$ only after pH of 5.5 is achieved by the intermittent addition of ammonia. |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | 1.10 | Clean | Acetone/IPA | ultrasonic | | 5m + 5m | Dry with $N_2$ |
| **Ohmic** | 2.1 | Clean | Acetone-IPA | USP | | | Finally dry the sample with $N_2$ |
| | 2.2 | Prebake | | Hotplate | 120°C | 1m (HP) + 1m (RT) | To warm up and dry the sample |
| | 2.3 | Resist coating | Photoresist : AZnLOF 2um (AZ neg Lift Off) | Spinner | | 30s | Program-6 (Acc=2000, rpm=3000,time=30s) |
| | 2.4 | Soft-bake | | Hotplate | 110°C | 1m (HP) + 1m (RT) | Expose sample to RT environment for 1m for homogenisation |
| | 2.5 | Exposure | | MA4 | | 5.5s | Intensity I line =0.9mW/cm$^2$. Read Mask Aligner document for details. |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | 2.6 | PEB ( post exposure bake) | | Hotplate | 110°C | 1m (HP) + 1m (RT) | Expose sample to RT environment for 15s for homogenisation |
| | 2.7 | Develop AZnLOF 2070 | MIF 326 | | | 1m | Because of negative resist, exposed region polymerises and unexposed region gets dissolved in the developer. |
| | 2.8 | Load evaporator with crude material | AuGe/Au 70mg/12cm | JNR | | | -Crude AuGe pre-cleaned in Trike/Acetone/Methanol (5m each)and let dry @120C in oven at least 15m<br><br>'-Crude Au pre-cleaned in Trike/Acetone/Methanol (5m each)and etched in concentrated HCL for 2 min and blow dried with N2 |
| | 2.9 | De-scum (Plasma etch) | $O_2$ | Plasma kit | RT | 20s | P:60mTorr, Power= 25W(100 a.u.), $O_2$ flow: 50 sccm |
| | 2.10 | De-oxidise | HCl:$H_2O$ (1:1) | | RT | 30s | |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | 2.11 | Evaporation | AuGe/Au<br>50 nm/ 100 nm | JNR | | | Load ~70mg AuGe and 12cm Au<br>**AuGe will allow Au to diffuse into S/C to make metallisation<br>**thinner Au |
| | 2.12 | Lift-off | NMP (1165) | | 80°C | >30m | Can be left overnight at RT |
| | 2.13 | Clean | Water | | | 3m | Dry with $N_2$ |
| | 2.14 | Anneal | | Furnace | 280°C | 90s | $N_2$ flow: 150 (leave N2 at 30 in Idle), Rc~0.1 ohm/mm |
| | 2.15 | TLM measurement | | ICCAP | | | File: Constant Current (I = 1mA) |
| **Gate** | 3.1 | Clean | Acetone/IPA +<br>Prebake 120°C | USP | | 1m<br>(HP)<br>+<br>1m<br>(RT) | |
| | 3.2 | Resist Coating | Photoreisit :<br>AZnLOF 2070<br>(1µm grade) | Spinner | | 30s | Program-6<br>(Acc=2000, rpm=3000,time=30s) |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | 3.3 | EBR | AzEBR | Only at corners | | 30s | Program-6<br>(Acc=2000, rpm=3000,time=30s) |
| | 3.4 | Soft-bake | | Hotplate | 110°C | 1m<br>(HP)<br>+<br>1m<br>(RT) | Expose sample to RT environment for 1m for homogenisation |
| | 3.5 | Exposure | | MA4 | | 12s | Intensity=0.9mW/cm$^2$ i-line. Set wedge error 1bar!! Read Mask Aligner document for details. |
| | 3.6 | PEB ( post exposure bake) | | Hotplate | 110°C | 1m<br>(HP)<br>+<br>1m<br>(RT) | Expose sample to RT environment for 15s for homogenisation |
| | 3.7 | Develop AZ nLOF 2070 (1µm grade) | MIF 326 | | | 5 m | plus 2 min for each addition of 1s exposure |
| | 3.8 | Load evaporator with crude material | Ti/Au/Au<br>1.5cm/15cm/15cm | EDWINA | | | -Crude Au & Ti pre-cleaned in Trike/Acetone/Methanol (5m each)and etched in concentrated HCL for 2 min and blow dried with N2 |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | 3.9 | De-scum (Plasma etch) | $O_2$ | Plasma kit | RT | 20s | P:60mT, Power= 25W (100 a.u.), $O_2$ flow: 50 sccm |
| | 3.7 | Gate recess | Succinic acid powder (10g), $H_2O$ (50ml), Ammonia (~10ml to pH of 5.5), $H_2O_2$ (5 ml) | pH meter | RT | 5m | Succinic Etch<br>InGaAs etch rate = 240A/min<br>InAlAs etch rate = 2A/min<br>Etch 50A InGaAs layer<br>InGaAs/InAlAs selectivity 120:1<br>Allow the solution to settle for 5m before etching.<br>Add $H_2O_2$ only after pH of 5.5 is achieved by the intermittent addition of ammonia. |
| | 3.8 | Evaporation | Ti/Au 50nm/450nm | EDWINA | | | Load 1.5cm Ti and 15cm of Au in each of the two adjacent boats<br>**Ti have high barrier height, and not allow Au to diffuse |
| | 3.9 | Lift-off | NMP | ultrasonic | 80°C | ~ 30m | Rinse with water |
| | 3.10 | clean | Water | | | 3m | Dry with $N_2$ |
| | 3.11 | Diode Test | | B1500 probe station | | | Before and After Sintering at Round Diode Structure |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Bond pads** | 4.1 | Clean | Acetone/IPA + Prebake 120°C | USP | | 1m (HP) + 1m (RT) | |
| | 4.2 | Resist Coating | Photoresist : AZnLOF 2um (AZ neg Lift Off) | Spinner | | 30s | Program-6 (Acc=2000, rpm=3000,time=30s) |
| | 4.3 | Soft-bake | | Hotplate | 110°C | 1m (HP) + 1m (RT) | Expose sample to RT environment for 15s for homogenisation before prebaking |
| | 4.4 | Exposure | | MA4 | | 5.5s | Intensity I line =0.9mW/cm$^2$. Read Mask Aligner document for details. |
| | 4.5 | PEB ( post exposure bake) | | Hotplate | 110°C | 1m (HP) + 1m (RT) | Expose sample to RT environment for 1m for homogenisation |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | 4.6 | Develop AZ nLOF 2070 | MIF 326 | | | 1m | Because of negative resist, exposed region polymerises and unexposed region gets dissolved in the developer. |
| | 4.7 | Load evaporator with crude material | Ti/Au/Au 1cm/15cm/15cm | EDWINA | | | Crude Ti+Au pre-cleaned in Trike/Acetone/Methanol and let dry @120$^{o}$C in oven at least 15m |
| | 4.8 | De-scum (Plasma etch) | $O_2$ | Plasma kit | RT | 20s | P:60mT, Power= 25W (100 a.u.), $O_2$ flow: 50 sccm |
| | 4.9 | Evaporation | Ti/Au 50nm/450um | EDWINA | | | Load 1.5cm Ti and 15cm of Au in each of the two adjacent boats |
| | 4.10 | Lift-off | NMP | ultrasonic | 80°C | ~ 30m | Rinse with water |
| | 4.11 | Clean | Water | | | 3m | Dry with $N_2$ |
| | 4.12 | Diode Test | | B1500 probe station | | | Before and After Sintering at Gate andSource/Drain |
| **SF11 Bridge support** | 5.1 | Clean | Acetone/IPA + Prebake 120°C | USP | | 1m (HP) + 1m (RT) | |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | 5.2 | Resist Coating | photoresist : SF11 | Spinner | | 45s | Program-13<br>(Acc=10000, rpm=500,time=5s),<br>(Acc=10000, rpm=4000,time=45s),<br>(Acc=10000, rpm=7000,time=5s) |
| | 5.3 | Bake | | Hotplate | 190°C | 5m<br>+<br>1m | Expose sample to RT environment for 15s for homogenisation before prebaking |
| | 5.4 | Resist Coating | Photoresist: S1805 | | | 30s | Program-4<br>(Acc=2000, rpm=4000,time=30s) |
| | 5.5 | Prebake | | Hotplate | 115°C | 1m<br>(HP) | Expose sample to RT environment for 1m for homogenisation |
| | 5.6 | Exposure | | MA4 | | 18s | Intensity=0.9mW/cm$^2$ i-line. Read Mask Aligner document for details. |
| | 5.7 | Develop S1805 | Microdev 1:1 | | | 50s | |
| | 5.8 | DUV(Deep UV) | | UV EPROM eraser | | 15m | Deep Ultraviolet flooding is done to make sure SF11 reacts to XP101A |

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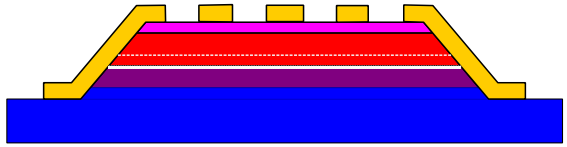
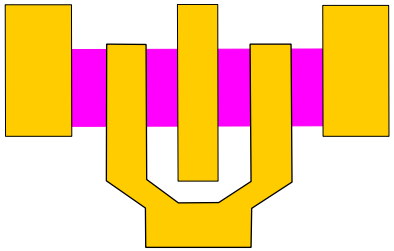
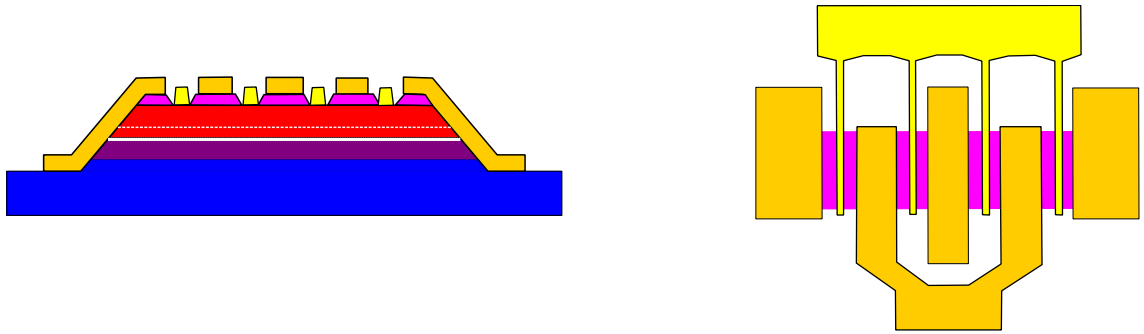
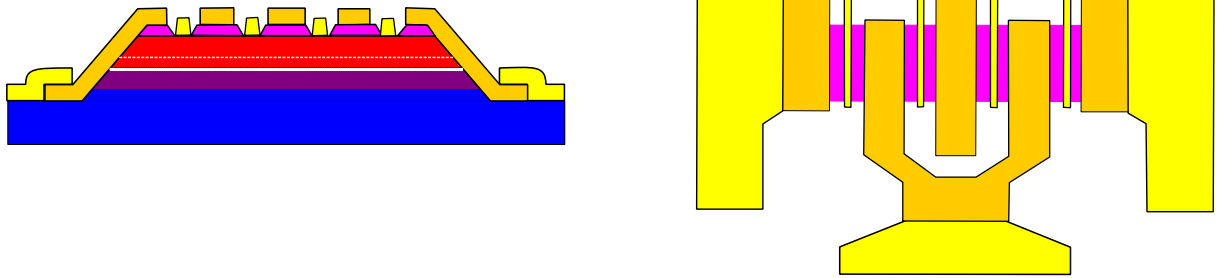
|---|---|---|---|---|---|---|---|
| | 5.9 | Develop SF11 | XP101A | | | 3m | Visually see the colour change to bright grey of the exposed area and rinse the sample with DI water. |
| | 5.10 | Clean | Acetone/IPA | USP | | | |
| | 5.11 | Reflow | | Hot plate | 200°C | 3m | ** heat treatment is done here<br>--> reflow rate = 0.17um/min |
| **Dielectric bridge** | 6.1 | Resist Coating | Photoresist : S1813 | Spinner | | 30s | Program-4<br>(Acc=2000, rpm=4000,time=30s) |
| | 6.2 | Bake | | Hotplate | 115°C | 1m<br>(HP) | Expose sample to RT environment for 1m for homogenisation |
| | 6.3 | Exposure | | MA4 | | 40s | Intensity=0.9mW/cm$^2$ I-line . Dielectric bridge mask. |
| | 6.4 | Develop S1813 | Microdev 1:1 | | | 90s | |
| | 6.5 | Evaporation | Au<br>Target: 500 nm | EDDY JNR | | | Load 15cm Au |
| | 6.6 | Lift-off | ACETONE + IPA | no heat | | ~ 30m | Rinse with water |

# APPENDIX B : FABRICATION STEPS FOR CONVENTIONAL pHEMT DEVICES

| Side view | Top View | Description |
|---|---|---|
|  |  | *MESA + Side wall etch*<br>• Nonselective Orthophosporic etch (3:1:50)<br>• Highly selective succinic acid side wall etch at pH 5.5 |
|  |  | *Ohmic + Annealing*<br>• Thermal deposition of AuGe/Au of 50/100 nm thickness<br>• Annealing at 280 °C for 90 s |

| | |
|---|---|
|  | *Gate recess + deposition*<br>• Gate recess using highly selective succinic etch at pH 5.5<br>• Thermal deposition of Ti/Au of 50/400 nm thickness |
|  | *Probing pads deposition*<br>• Thermal deposition of Ti/Au of 50/400 nm thickness |

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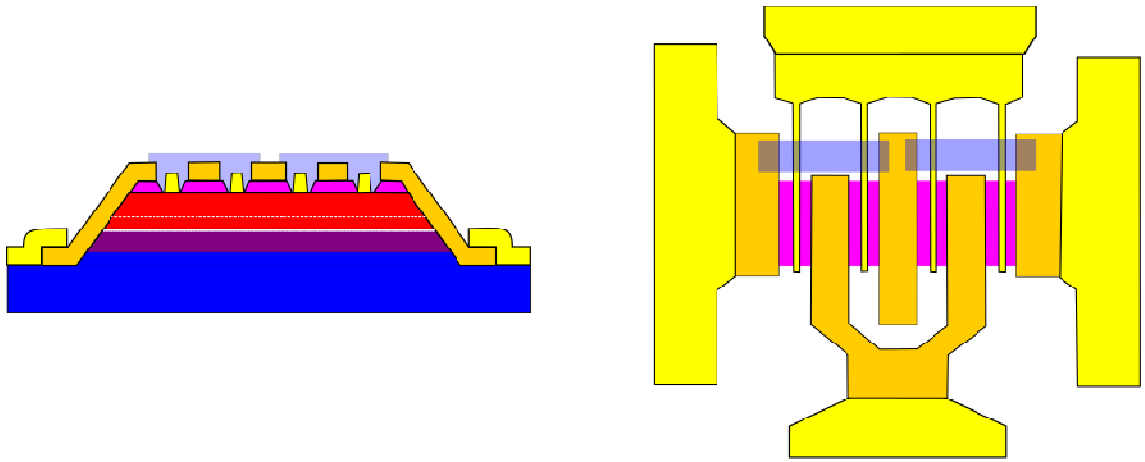
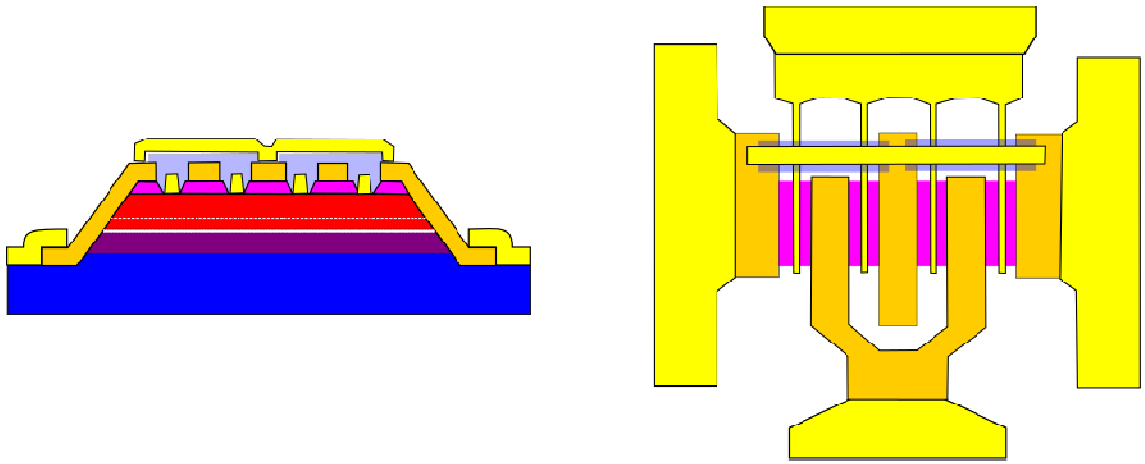
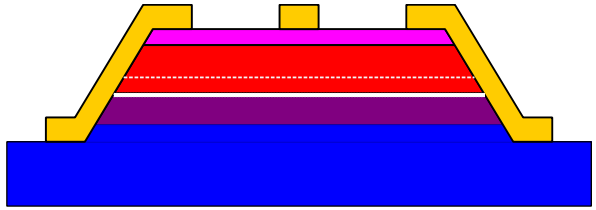
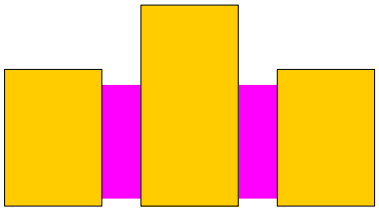
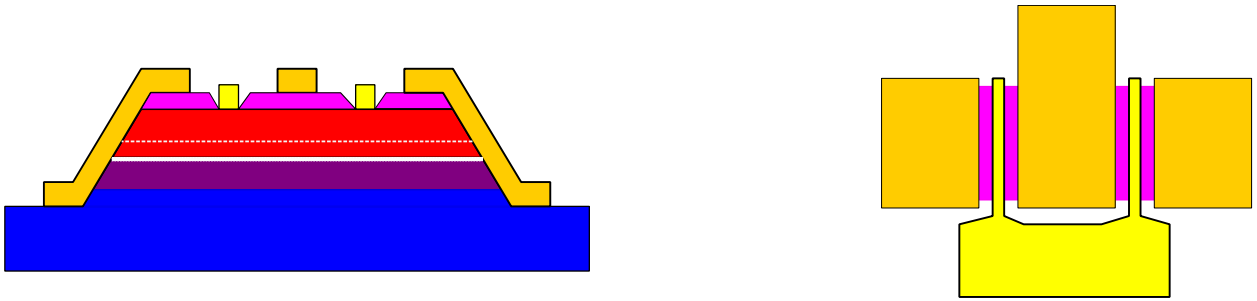
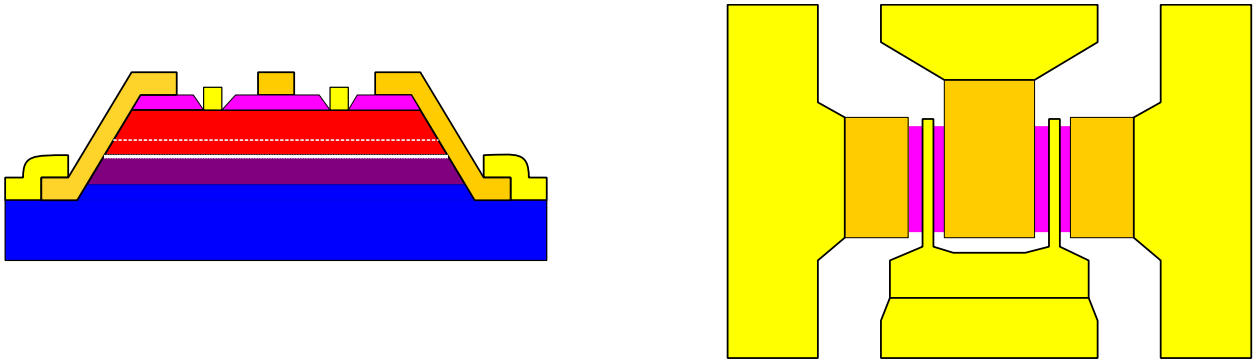
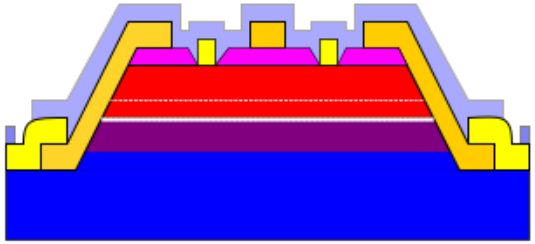
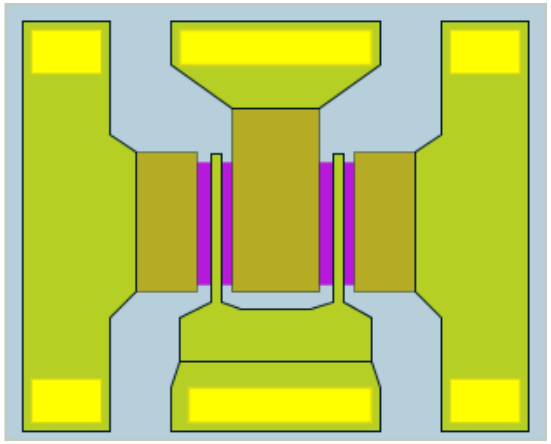
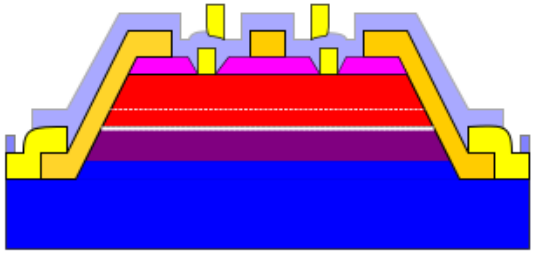
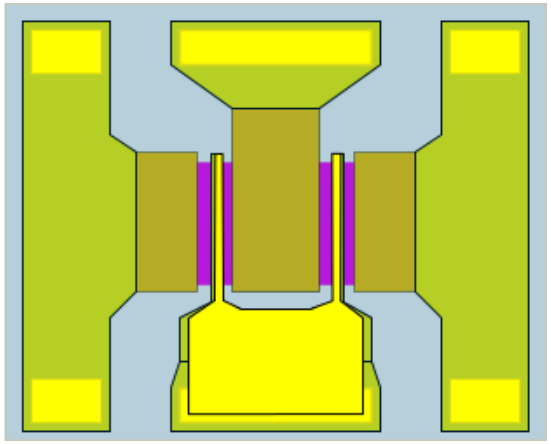
|---|---|
|  | *Dielectric Bridge*<br><br>• SF11 dielectric bridge + reflow |
|  | *Metal interconnection*<br><br>• Thermal deposition of Ti/Au of 50/400 nm on top of SF11 dielectric bridge |

# APPENDIX C : FABRICATION STEPS FOR FIELD PLATE DEVICES

| Side view | Top View | Description |
|---|---|---|
|  |  | *MESA + Side wall etch*<br>• Nonselective Orthophosporic etch (3:1:50)<br>• Highly selective succinic acid side wall etch at pH 5.5 |
|  |  | *Ohmic + Annealing*<br>• Thermal deposition of AuGe/Au of 50/100 nm thickness<br>• Annealing at 280 °C for 90 s |

| | |
|---|---|
|  | *Gate recess + deposition*<br>• Gate recess using highly selective succinic etch at pH 5.5<br>• Thermal deposition of Ti/Au of 50/400 nm thickness |
|  | *Probing pads deposition*<br>• Thermal deposition of Ti/Au of 50/400 nm thickness |

| | | |
|---|---|---|
|  |  | *Nitride deposition and etch*<br>• $Si_3N_4$ deposition at 200 °C<br>• Nitride dry etch using $CF_4 + O_2$ |
|  |  | *Formation of Field Plate terminal*<br>• Thermal deposition of Ti/Au of 50/400 nm thickness |

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