Thermal and Small-Signal Characterisation of AlGaAs/InGaAs pHEMTs in 3D Multilayer CPW MMIC

A thesis submitted to The University of Manchester for the degree of

Doctor of Philosophy

in the Faculty of Engineering and Physical Sciences

2010

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ABSTRACT

Rapid advancement in wireless communications over the years has been the driving force for many novel technologies providing compact and low cost solutions. Recent development of multilayer coplanar waveguide (CPW) MMIC technology promises realization of 3D MMIC in which large area-occupying passive components are translated from horizontal into vertical configuration resulting compact structure. The other main advantages of this technology are elimination of via-holes and wafer-thinning giving alternative performance solution, if not better, from the traditional MMIC. In this thesis, thermal and small-signal characteristics of prefabricated AlGaAs/InGaAs pseudomorphic high electron mobility transistors (pHEMTs) on semi-insulating (S.I.) GaAs substrate incorporated in the 3D MMIC technology have been analysed and modelled for the first time. A comprehensive small-signal parameter extraction procedure has been successfully developed which automatically determines the device small-signal parameters directly from the measured S-parameters.

The developed procedure is unique since it provides a great deal of data on measured devices over a wide bias, temperature and frequency range for future incorporation of different active devices for the 3D MMIC technology and provides a first hand knowledge of how the multilayer structure will affect the performance of pre-fabricated pHEMTs. The extracted small-signal models of both pre- and post- multilayer processed pHEMTs have been compared and validated to the RF S-parameters measurements. The main focus was drawn upon the temperature dependent model parameters and how the underlying physics of the transistors behave in response to the change of temperature. These novel insights are especially valuable for devices designed specifically for high power applications like power amplifiers where tremendous heat could be generated. The data can also be interpreted as a way to optimise the multilayer structure, for example, alternative material with different properties can be implemented. The governing physics affecting device performance are also modelled and discussed empirically in details through extracted device parameters. These investigations would assist in the development of reliable, efficient and low cost production of future compact 3D multilayer CPW MMICs.

DECLARATION

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Acknowledgement

This work is dedicated to my lovely wife

See Yea Huey

List of Publications From This Work

[1] **Jimmy P. H. Tan**, J. Yuan, A. A. Rezazadeh, and Q. Sun, "Temperature Dependent Small-Signal Model Parameters Analysis of AlGaAs/InGaAs pHEMTs in Mulitlayer 3D MMIC Technology," Proceedings of European Microwave Integrated Circuit (EuMIC) Conference, Paris, September 2010, pp. 378-381.

[2] Q. Sun, V. T. Vo, R. A. Davies, A. A. Rezazadeh and **Jimmy P. H. Tan**, "Miniaturized Multilayer CPW pHEMT Amplifiers," Proceedings of European Microwave Integrated Circuit (EuMIC) Conference, Amsterdam, September 2008, pp. 44-47.

[3] **Jimmy P. H. Tan** and Ali A. Rezazadeh, "Small-Signal Characterization of pHEMTs in Multilayer CPW MMIC Technology using IC-CAP," UK Semiconductors 2008, Sheffield, June 2008.

[4] **Jimmy P. H. Tan**, J. Yuan, A. Rezazadeh and Q. Sun, "Thermal Effects on AlGaAs/InGaAs pHEMTs in Multilayer 3D MMIC Technology," to be submitted for journal publication.

Chapter 1   Introduction

1.1 Introduction

In contrast to hybrid microwave integrated circuits (MICs), monolithic microwave integrated circuits (MMICs) technology has the advantages of small size, high reliability, low cost and the capability of large volume production. MMIC is an integrated circuit that incorporates all the circuit components such as resistors, inductors, capacitors, transistors, diodes on a single semiconductor chip [1].

MMIC technology has seen much progress and has been maturing for the past few decades. Recent development of multilayer coplanar waveguide (CPW) MMIC has shown promising features of being capable of eliminating the needs of via-holes and substrate-thinning allowing lower production cost to be achieved [2]. Unlike the microstrip design, in the CPW, the substrate does not need to be thinned down which is the most disadvantage of making the chip fragile [2-4]. In addition, realization of 3D MMIC is possible in the CPW-based MMICs using multilayer technology which consists of thin layer of dielectric and metal conductors. In this way, large area occupying passive components are translated from horizontal to vertical configuration resulting compact designs with reduced cost of manufacturing [5-7].

There have been several reports in the building up of the components library for this multilayer CPW MMIC technology [8-16]. But accurate characterisations of various components are necessary in order to produce a reliable library for future 3D MMIC designs. The research group at Manchester has been successful in demonstrating CPW based 3D MMICs incorporating AlGaAs/InGaAs pseudomorphic high electron mobility transistors (pHEMT), fabricated on thick GaAs substrate, and a multilayer technology consisting of thin polyimide as dielectric layers and Ti/Au as metal layers. Although the initial work has been realised and produced some good results, a great deal of research were required to characterise accurately the pHEMTs used in the multilayer technology. In this work, small-signal characterisation and modelling of pHEMTs in this multilayer CPW MMIC environment have been carried out. Another important issue is that the

thermal charachterisation of pHEMTs used in the multilayer technology needs to be carefully assessed. This is because in the 3D MMICs, thick GaAs substrates (~0.6mm) has been used and since thermal conductivity of GaAs is rather poor (~45W/m°C) as compared to Si (~150W/m°C), transistors can experience a great deal of heat and therefore it is essential to investigate their thermal characterisations.

The multilayer CPW MMIC under investigation has been developed by The Electromagnetics Centre at The University of Manchester with the active devices, AlGaAs/InGaAs pHEMTs, provided by the foundry, Filtronic Compound Semiconductors. A conceptual drawing of this technology can be seen in Figure 1.1. Three metal layers are stacked in between of two dielectric layers, various circuit components are then carefully designed realising 3D MMIC.
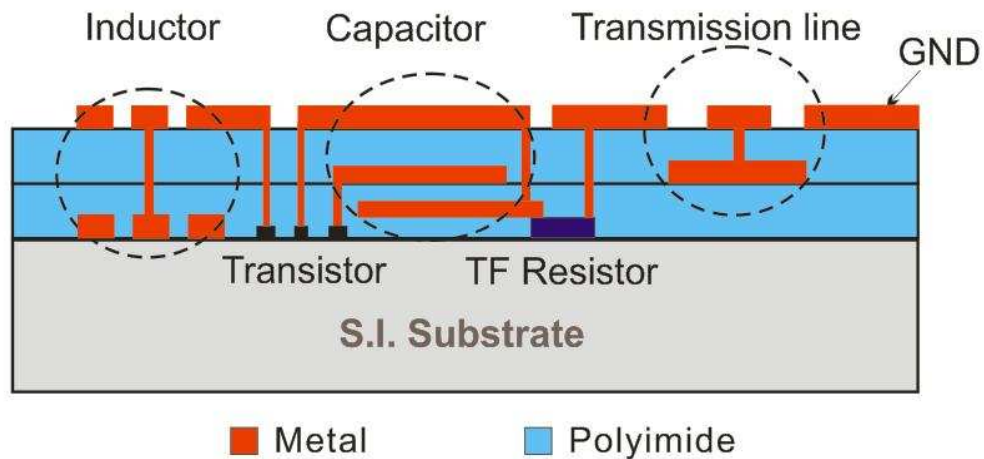
Figure 1.1 Illustration of the multilayer processing [12].

Device modelling work has always been an ongoing project, with many state-of-the-art novel devices being designed every now and then. The establishment of an empirical equivalent circuit model forms an integral part of characterising of a device. It not only provides insights to the underlying physics of the device with the corresponding circuit parameters, but also offers a predictable performance which circuit designers can optimise when incorporating the device in designing amplifiers, switches, oscillators and other useful circuits. Analyses and optimisations such as gain, noise and stability can also be carried out with the aid of a circuit model.

In this work, a small-signal pHEMT model has been developed. Traditionally, small-signal field effect transistor (FET) models and their circuit parameters values were determined by optimization of fit to measured scattering parameters (S-parameters). However, this technique suffers from the disadvantages such as time consuming, less accurate and lack of physical significance. As a solution, direct parameter extraction method, which is fast and accurate, was introduced and is therefore demonstrated in this thesis. The procedure has also been made semi-automated using Agilent's IC-CAP.

Once the equivalent circuit parameters (ECPs) are accounted for, insights of the underlying physics of the device could be achieved by careful analyses. In order to investigate the effect of the multilayer processing, pre- and post-multilayer-processed AlGaAs/InGaAs pHEMTs are compared with their corresponding ECPs.

Thermal effects, being one of the major issues for power-related applications, are one of the key research areas in this work. This is because the AlGaAs/InGaAs pHEMTs that are multilayer-processed in this work are suitable to be designed as power amplifiers. Enormous heat could be generated during the operation and hence to know how the change of temperature would affect the characteristics and performance of the AlGaAs/InGaAs pHEMTs is of the major concern.

1.2 Key Objectives

The main aims of this research work are:

- To carry out a review of published theoretical and experimental reports on device modeling, placing special emphasis on AlGaAs/InGaAs pHEMTs.

- To investigate the uniformity of pre- and post-multilayer-processed AlGaAs/InGaAs pHEMTs in 3D MMIC environment.

- To establish suitable physics based compact expressions for the transport of the electrons in a pHEMT which in turn forms the circuit parameters of a physically intuitive pi-model.

- To develop a small-signal model parameter extraction algorithm. Direct parameter extraction is to be used, where the extraction is made directly from the measured DC and RF data without requirement of iterations or optimisations.

- To extend the small-signal model development to both pre- and post-multilayer-processed AlGaAs/InGaAs pHEMTs and validate the models to the on wafer S-parameters measurements.

- To develop temperature dependent small-signal models for the pre- and post-multilayer-processed AlGaAs/InGaAs pHEMTs.

- To establish linear temperature dependent expressions for each of the equivalent circuit model parameters and observe the temperature coefficients between pre- and post-multilayer-processed AlGaAs/InGaAs pHEMTs.

- To analyse and attain knowledge of the underlying physics governing the electrons transport in various temperature and explore ways of optimising the performance.

1.3 Overview of The Thesis

This thesis is divided into the following chapters:

In Chapter 1, general overview of the research work is presented with introduction of the 3D MMIC technology. Motivation and key objectives are highlighted. An outline of the thesis is also given.

Chapter 2 provides background reviews on the MMIC technology, advantages and disadvantages are discussed. III-V semiconductors are reviewed next, with various designs and technologies presented including applications. Following, principles of pHEMT are reviewed placing emphasis on the development of small-signal model. Lastly, thermal effects are discussed with its implications on the performance explained.

The experimental set-up is presented in Chapter 3. Software tools that are used during the course of this work are introduced. Procedures and how to apply them in order to achieve good results are discussed and explained. On-wafer DC and RF measurements are shown and temperature control set-up is given.

Chapter 4 is the main results chapters providing analyses and discussions of the obtained data.

The device structure is first presented in Section 4.1. The top and cross-sectional views of the AlGaAs/InGaAs pHEMTs provide information of fundamental specifications. Layouts of the pre- and post-multilayer-processed pHEMTs are shown. Incorporations of the AlGaAs/InGaAs pHEMTs to the 3D MMIC are presented showing interconnects realising various circuit components.

Following that, Section 4.2 investigates the uniformity of both the pre- (virgin) and post-multialyer-processed (multilayer) pHEMTs and observations are shown. Section 4.3 of Chapter 4 is about the modelling of pHEMTs. It first shows the DC characteristics of the multilayer AlGaAs/InGaAs pHEMTs. After that, direct on-wafer RF S-parameters measurements are shown. Equivalent circuit model for the pHEMTs is adopted and procedure of the extractions for each of the circuit parameters are presented and carried out. The procedure can be roughly divided into cold and hot bias measurements with careful bias points selected and measured. In the last part of Section 4.3, the developed small-signal models for both the virgin and multilayer AlGaAs/InGaAs pHEMTs are validated and compared to the measurements.

Section 4.4 of Chapter 4 moves on to explore the DC temperature dependent modelling of the pHEMTs, the change of DC characteristics of the pHEMTs to the change of temperature is observed and explained with the thermal effect on the electron transport physics. In Section 4.5, the concept of the development of small-signal model is extended to temperature dependent small-signal model for both virgin and multilayer pHEMTs. Circuit parameters are divided into two categories, extrinsic and intrinsic, and analysed. Each of the circuit parameters is expressed in a linear temperature-dependent equation giving a temperature coefficient. The implications of the temperature

coefficients are discussed and both virgin and multilayer AlGaAs/InGaAs pHEMTs are compared.

And finally, Chapter 5 presents the conclusion and the future works. Key observations and results are highlighted. Potential future works are suggested and discussed.

Chapter 2   Background Review

2.1 MMIC Technology

2.1.1 History of GaAs MMIC Technology

In 1959, first concept of integrated circuit (IC) was brought forward by Kilby of Texas Instruments [17]. Rapid development was started in early 1960s by Moll following several publications on the integrated circuit applications [18-21]. In 1964, first Silicon based monolithic microwave integrated circuit (MMIC) was invented by Ruegg [22]. It was an analogue FET switch as presented in Figure 2.1. However, like all pioneering inventions, it suffered from poor switching speed due to the low mobility of Silicon. MMIC proceeded to further improvement and in 1960s, with maturing development of microstrip lines reported by Wheeler [23-25], two publications were made [26-27] and widely recognised as the first original realisation of Gallium Arsenide (GaAs) based MMIC technology. Figure 2.2 shows the Schottky diode circuit reported in the papers.
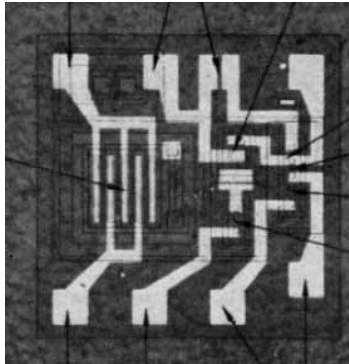
Figure 2.1 Micrograph of the analogue FET switch based on Silicon MMIC technology [22].
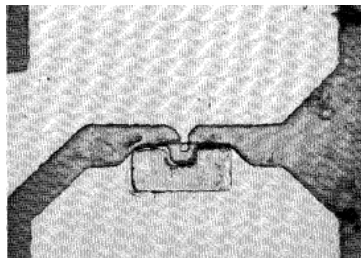
Figure 2.2 Micrograph of the schottky barrier diode for use in 94GHz mixer circuit [27].

In 1976, Pengelly and Turner, who were widely acknowledged as the inventor of MMICs, reported a GaAs FET amplifier [28]. This is thus known as the first practical MMIC. This single-stage amplifier was capable of 5dB gain at X-band with 1μm optically-written gates. Figure 2.3 shows the picture of this amplifier. No DC block was used and the lumped element matching network was designed using computer optimisation. This invention spurred a new interest in MMIC and many great developments and associated technologies were achieved. MMIC with better performance and higher operating frequency is sought after ever since.
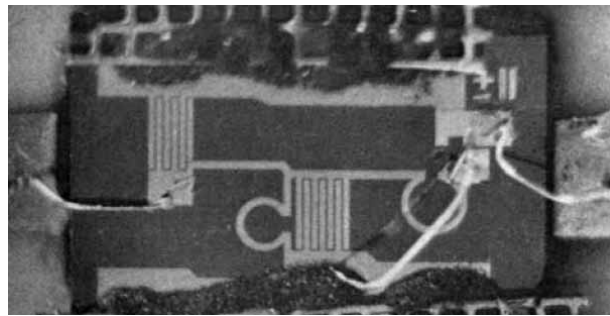
Figure 2.3 Micrograph of the first monolithic amplifier [28].

For realisation of active devices, Silicon is one of the most mature and popular semiconductor materials. It has gone through intensive research for several decades and achieved great maturity in terms of fabrication technology. The main attraction of Silicon as the building block of integrated circuits is its low processing cost. However, limitations of Silicon based active devices started to shown at high operation frequency, especially after X-band. The key issue is to do with the low electron mobility of the material property.

There is where GaAs was first proposed in late 1970s as an alternative material to make up for the tasks for high frequency applications [29]. GaAs was introduced with some superior electronic properties that Silicon is lacking. A comparison of the physical and electronic properties of GaAs and Silicon can be seen in Table 2.1. GaAs has an intrinsic electron mobility of 8500 $cm^2V^{-1}s^{-1}$ at 300K, five time greater than the 1500 of Silicon. On the other hand, the saturation velocity of GaAs is much higher than that of Silicon. The result is that GaAs based circuit can be operated with a lower voltage and perform faster than the Silicon counterpart. Also, it means with the same doping density, GaAs

based devices will have lower resistivity. Low resistivity is especially important for low noise applications as noise is normally created as thermal noise in the channel resistance and the gate, drain and source contact resistance. Therefore, a lower resistivity found in GaAs material compared to Silicon will generate a lower power level of noise. This is also why GaAs is attractive to be designed as low noise amplifier at microwave frequency. Furthermore, as a substrate, as can be seen in the Table 2.1, GaAs exhibits resistivity of 10^9 Ω·cm while Silicon has merely 10^3 Ω·cm. It makes GaAs a much better substrate which introduces lower substrate associated losses [30].

Table 2.1 Electronic and physical properties of GaAs and Silicon [30-32]

Properties	Si	GaAs
Intrinsic Electron Mobility at 300K, $cm^2V^{-1}s^{-1}$	1500	8500
Electron Saturation velocity, cms^{-1}	9×10^6	1.3×10^7
Intrinsic Hole Mobility at 300K, $cm^2V^{-1}s^{-1}$	450	400
Thermal conductivity at 300K, $Wcm^{-1}K^{-1}$	1.5	0.46
Dielectric constant	11.9	12.9
Substrate (intrinsic) resistivity at 300K, Ω·cm	10^3	3.7×10^8
Band gap at 300K, eV	1.12	1.424

Unfortunately, one of the shortcomings of GaAs is that it has a lower thermal conductivity, 0.46 $Wcm^{-1}K^{-1}$, compared to Silicon's 1.5 $Wcm^{-1}K^{-1}$. It means that GaAs has poorer heat handling capability and more susceptible to adverse heat effects [32]. That is why thinning process is introduced for GaAs based devices to reduce the thermal resistance. This thinning process however introduces additional processing cost and time and results in a fragile wafer. In contrast, Silicon, the second most abundant element within the Earth's crust, is a very low cost material. It is therefore, GaAs based active devices are almost always more expensive compared to Silicon.

Hole mobility of GaAs is much lower than its electron mobility, compared to Silicon. In Silicon, the hole and electron mobilities are comparable and that is why complementary metal-oxide-semiconductor (CMOS) is possible. Therefore, there is yet a feasible CMOS equivalent technology in GaAs material due to the fact that p-type GaAs devices will perform much slower than n-type GaAs devices [32].

2.1.2 Advantages and Disadvantages of MMICs

Traditional microwave hybrid integrated circuit (MIC) consists of wire bonding and other surface mounted discrete components. Soldering and conductive epoxy could also be found to bond on-chip and off-chip components on a single substrate. In contrast, monolithic microwave integrated circuit (MMIC) is a microwave circuit where all active and passive components are fabricated together during the process on a single semiconductor substrate [1].

Many unwanted losses could be introduced in MIC, such as the parasitics associated with the wiring and solders. During the assembly, use of various interconnects could result in many undesirable coupling or interference that could seriously affect the target performance of the circuit.

This is where MMIC technology is more superior than hybrid MIC for there is no need for any kind of wire bonding, soldering and gluing. Parasitics are kept at the minimum, unwanted losses would then be minimised. Better performance at high frequency can thus be achieved. A table comparing the advantages and disadvantages of both MMIC and MIC is presented in Table 2.2.

Table 2.2 Advantages and disadvantages of MMIC and hybrid MIC [1].

	MMIC	Hybrid MIC
Cost	Cheap in large quantities Cheap for complicated circuits with large number of components	Cheap for simple circuits and with automated assembly
Choice of components	Limited choice of components	Vast selection of components
Parasitic	Less unwanted parasitic Can be controlled	More unwanted parasitic from bond pads/bond wires Cannot be controlled
Performance	Good broadband performance	Limited bandwidth performance
Frequency of operation	Good performances to well over 100 GHz	Very hard to realise above 30 GHz
Assembly work	Minimal	Can be difficult and time-consuming to assemble
Reproducibility	Very good	Poor
Reliability	Very good	Adequate
Size, weight and layout area	Very small and light in general Must miniaturise area as much as possible to stay commercially competitive	Larger and heavier than MMICs Less pressure to miniaturise layout as substrate is low cost
Turnaround and post-fabrication modifications	Typically 3-6 months Cannot make any changes to the design after fabrication	Typically a few days Possible to tune after fabrication
Investment required	Very expensive to start up	Little investment required to start up

The main attractiveness of MMIC lies in the fact of their excellent reproductivity at large quantity in a relatively cheaper cost. A table showing the approximated chip fabrication cost in 1995 with respect to chip size is shown in Table 2.3. It was a high yield MESFET process using ion implantation. As can be seen in the table, smaller chip size is attractive due to a more compact structure and at the same time lower production cost. An example of a single stage MMIC amplifier is shown in Figure 2.4.

Table 2.3 Effect of chip size on fabrication cost in 1995 [1].

Chip size(mm^2)	Yields (%)	working circuits per 3 inch wafer	Cost of single chip at $4000 per wafer($)
1 X 1	80	3600	1.1
2 X 2	70	800	5
5 X 5	45	80	50
7 X 7	30	25	160
10 X 10	20	9	440
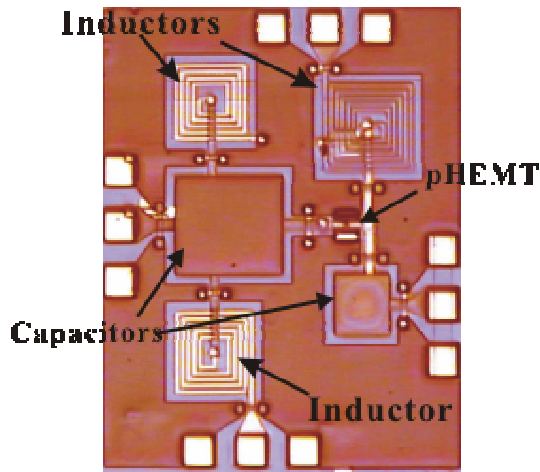
Figure 2.4 Micrograph of a planar CPW amplifier using MMIC technology [16].

2.1.3 Multilayer Technology and Coplanar Waveguide

Microstrip has been the most popular configuration found in MMIC technology for the past few decades. In microstrip technology, a conductive ground plane is needed at the bottom of the substrate. Therefore, vias are needed to be constructed. An illustration of this can be seen in Figure 2.5. As vias can introduce unwanted losses to the circuit, in order to keep these to the minimum, substrate thinning is required. Unfortunately, this would introduce additional cost during the fabrication process. A thinned down wafer also suffers from the fragility and is difficult to handle.
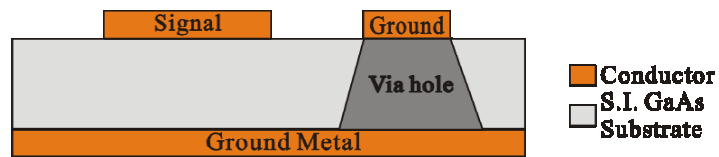
Figure 2.5 Cross-sectional view of a Microstrip type MMIC with via holes.

Therefore, alternative configuration is sought after and coplanar waveguide (CPW) technology has arisen as the possible solution. CPW is first invented by Wen [2]. A cross sectional view of a typical CPW structure is presented in Figure 2.6, where G is the gap width between the signal and ground conductors, W is the signal trace width and T and H are the metal and substrate thickness respectively. No via is needed as can be seen and thus parasitics associated with the vias are eliminated. Production cost can also be driven down as no vias construction and wafer thinning process are required.

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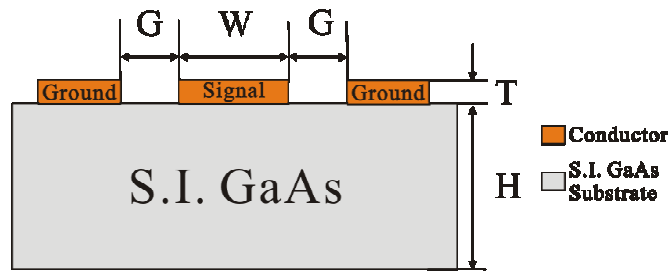
Figure 2.6 Cross-sectional view of a typical CPW MMIC structure.

For a conventional MMIC like the one found in Figure 2.4, the most area-occupying components are the passives. Spiral inductors and capacitors are both huge in size compared to the active devices. As the cost for a given size wafer is more or less fixed, much of the cost will be on the large size passives. A 3D multilayer CPW MMIC technology is thus proposed and developed. In this technology, minimised cost could be achieved as the passives are constructed in layers, translating the planar components into 3D structure. A much more compact size of the wafer could then be obtained. Many miniatured components and circuits have been reported since late 1980s [33-48].

An illustration of the 3D multilayer CPW MMIC is presented in Figure 2.7. As can be observed, the passive components, such as resistors, capacitors and inductors are moved from their conventional planar to vertical plane with respect to the wafer. Layers of dielectrics and metal conductors are fabricated in the multilayer process as well realising required functions. Interconnects are made in the form of via holes.

3D multilayer CPW MMIC has the advantages of compact size, minimised coupling and a great flexibility in layout designs. Compactness is achieved as mentioned before most of the are-occupying components are now translated into vertical direction. Unwanted coupling between nearby components found in conventional CPW MMIC can be made minimum after a much further separations made possible in 3D multilayer CPW MMIC. Also, compared to MMIC in microstrip configuration, CPW MMIC with the ground on the same plane as the signal traces, separating adjacent components, unwanted crosstalks could be minimised.
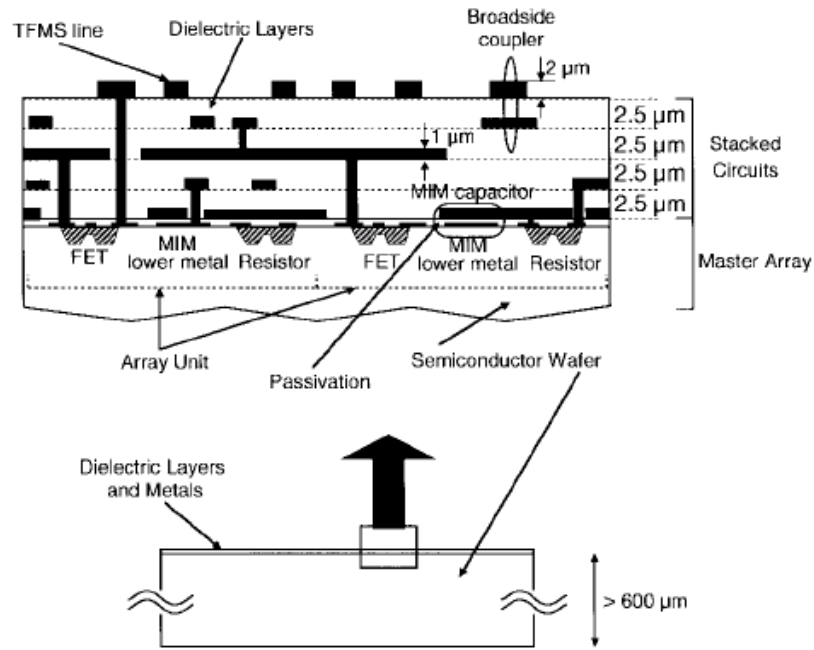
Figure 2.7 Basic structure of a multilayer MMIC [49].

There is however a potential disadvantage of 3D multilayer CPW structure. All this layers stacking could make the generated heat during the operation difficult to be dissipated. The thick substrate would make the problem harder and reduce the heat dissipation efficiency. This is especially noteworthy as GaAs has much worse thermal conductivity compared to Silicon. Hence, a comprehensive thermal characterisation in this technology is required.

2.1.4 Polyimide as Dielectric in Multilayer Structure

Polyimide has been chosen to be used as the dielectric in the multilayer structure. It can serve firstly for the purpose of supporting and insulating layers of conductors in the 3D MMIC designs and also secondly of planarising and passivating the surface of MMICs.

Careful designing process has been carried out investigating the thickness effect of the polyimide in 3D MMIC. It has been built with 2 layers of about 2.5 microns during the fabrication. This thickness was chosen to ensure most of the electric flux would be fallen within the polyimide. With a much lower dielectric constant of about 3.7 in comparison to GaAs of about 12.9, various passive components and transmission lines could be

designed. This is especially the case for lower values of MIM capacitors. Also, in order to design high impedance transmission lines, according to the fundamental definition of characteristic impedance of CPW transmission lines, the ratio of inductance to capacitance has to be kept as high as possible. It is therefore, when a lower dielectric constant polyimide is placed underneath the CPW transmission lines in compared to GaAs substrate, higher impedance could be achieved. Dissipation loss of the transmission lines could also be minimised with a material of lower dielectric constant. The accessibility and controllability of polyimide in the clean room are also the other major considerations in selecting it as the dielectric.

2.1.5 Fabrication Process

3D CPW MMIC fabrication is carried out in the clean room of the School of Electrical and Electronic Engineering, University of Manchester. An illustration of the fabrication process can be seen in Figure 2.8. It could be mainly divided into 7 steps with 3 conductors layers separated and insulated by the 2 dielectric layers, which in this case polyimide is used. Plasma etching technique is used to etch dielectric windows in order to build the interconnects.
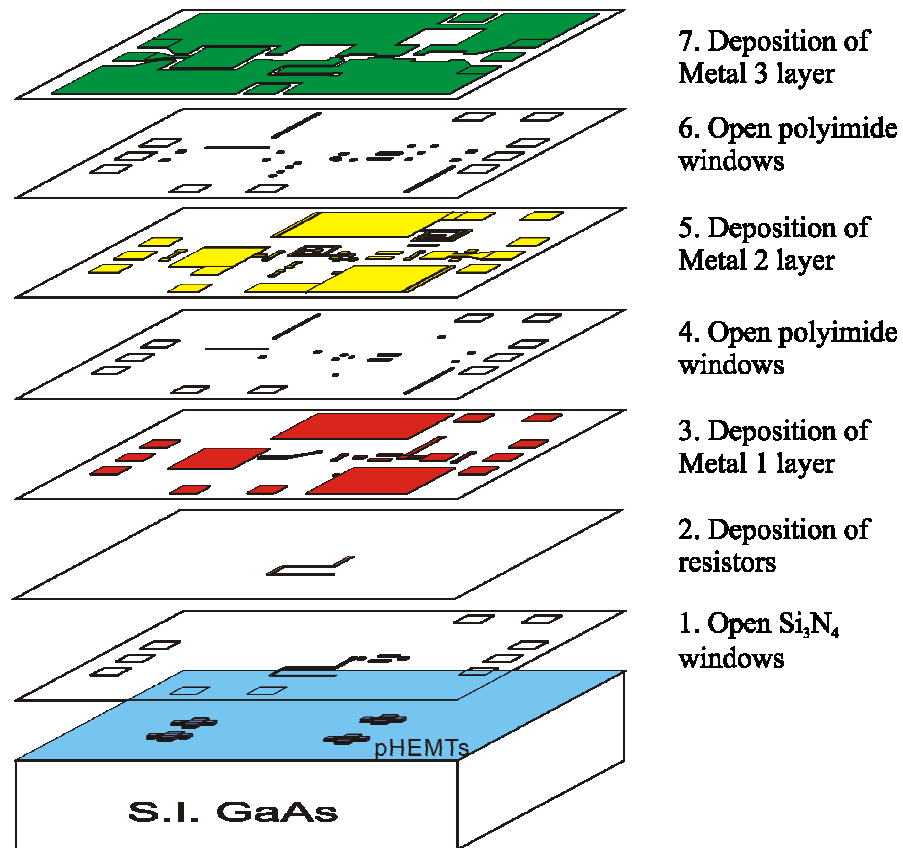
Figure 2.8 Illustration of the 3D CPW MMIC fabrication steps.

One of the very first steps of the fabrication process is to open windows of the Si_3N_4 passivation supplied by the semiconductor foundry. Photoresist were used during the process of lithography. Figure 2.9 shows the step 1 or etching the Si_3N_4, care should be taken as residue of Si_3N_4 results in poor metal contact. First, dehydration bake was done at 110 °C for 10 minutes. Next, photoresist S1813 was spin thin at 5200 rpm for 30 seconds. Softbaking was done at 90 °C for 30 minutes, after that, the back of the sample was checked to make sure there was any residue of photoresist. Exposure was next done for 45 seconds with the mask design. 1 Microdev to 2 D.I. water was mixed to develop photoresist for 50 seconds followed by postbake at 110 °C for 30 minutes. Bufferal HF was used to remove Si_3N_4 for 120 to 140 seconds. No Si_3N_4 was to be found in the holes. Lastly, acetone was used to remove the remaining photoresist and the sample was then rinsed in D.I. water.
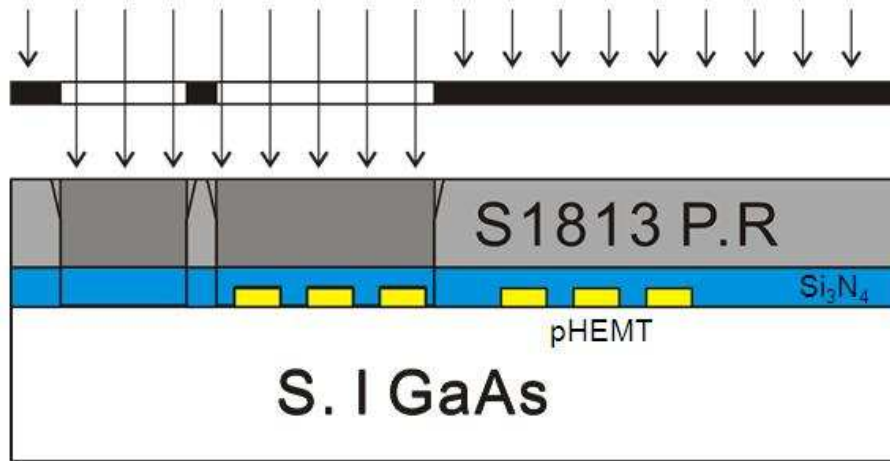
Figure 2.9 Step 1: Opening Si$_3$N$_4$ windows.

The second step is making the thin film resistor, evaporating the NiCr. The sheet resistance of the thin film resistors depends on the ratio of Ni and Cr. First, the sample was dried at 110 °C for 10 minutes. Photoresist was spin into at 5200 rpm for 30 seconds followed by softbaking at 70 °C for 30 minutes. Again, back of the sample needed to be checked to ensure there was no photoresist residue. After that, the sample was under exposure for 45 seconds. The development was done using 1 Microdev to 2 D.I. water for 50 seconds. Next, sample was cleaned using HCL (10%) to remove metal oxide for 15 seconds. Evaporating speed was controlled at 0.1 nm/sec. Lastly, unwanted metal was lifted off by removing photoresist using acetone. The step is presented in Figure 2.10.
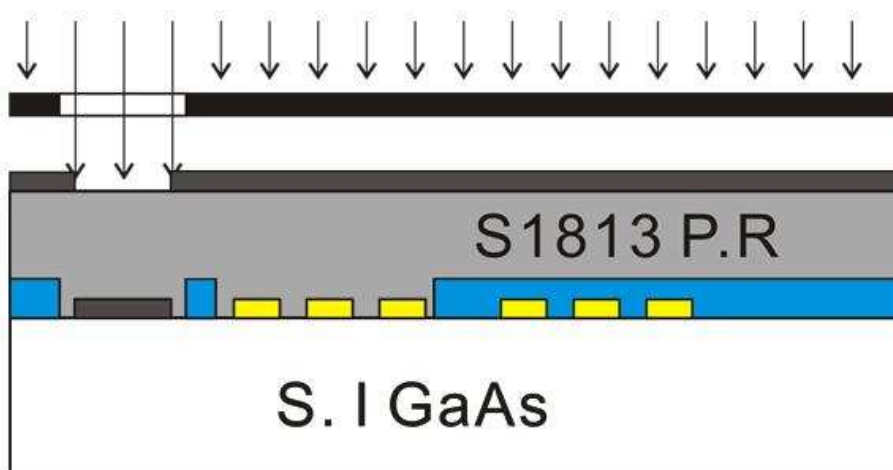
Figure 2.10 Step 2: Making thin film NiCr resistors.

The third step is to do with evaporating the Ti/Au metal layer 1.This step involves developing hardened photoresist by applying chlorobenzene treatment to achieve overhanging profile. Plasma etching was used to remove photoresist residue. During the evaporation of metal, clean Ti was required to obtain good metal adhesion. Like what previously done, the sample was cleaned first and dried at 110 ℃ for 10 minutes. Photoresist was spin at 5200 rpm for 30 seconds and softbaked at 70 ℃ for 30 minutes, residue was to be checked. Exposure was later done for 210 seconds. Chlorobenzene was used to harden the photoresist for 1 minute. Postbaking was followed at 70 ℃ for 10 minutes. 1 Microdev to 2 D.I. water was mixed in for 50 seconds and undercuts was checked using microscope. Redevelopment could be done if required. Next, plasma etching was used to remove photoresist residue for 30 seconds. HCL (10%) was applied to remove metal oxide for 15 seconds. The sample was then rinsed using D.I. water and dried to be ready for the evaporation of metal. Before opening the shutter, Ti was evaporated with dirty and the evaporation was carried out at 0.1 nm/sec to prevent photoresist from overheating. The Au evaporating speed was adjusted to 1 nm/sec and was stopped for 10 minutes for every 150 nm of Au to avoid photoresist overheating. Finally, metal was lifted off using NMP (photoresist stripper 1165). The illustration of the third step is shown in Figure 2.11.
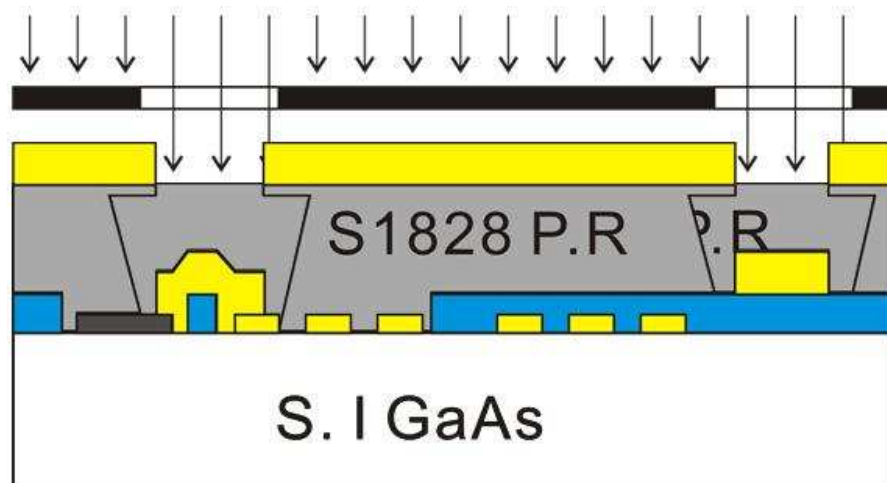
Figure 2.11 Step 3: Evaporating Au/Ti metal layer 1.

The forth step is about applying the polyimide layer 1. After the usual steps of cleaning and drying the sample, polyimide was pre-baked at 110 ℃ for 10 minutes. The

polyimide (PI 6210) was then spin at 2200 rpm for 40 seconds. Next, it was soft cured at 110 °C for 30 minutes in the oven. After curing, residue of polyimide was removed from the backside using microposit developer. The final cure was done at 200 °C for 4 hours in vacuum oven. Following that, photoresist was applied. It was spin at 3000 rpm for 30 seconds, softbaked at 90 °C for 30 minutes. The photoresist residue was checked to avoid poor metal contact. Exposure was then done for 250 seconds. The development process involved using 1 microdev to 2 D.I. water to develop for 50 seconds. The post-baking was then carried out at 110 °C for 30 minutes. The polyimide was then etched using plasma etching technique at 50scm O2, 140W, 100mTorr for 13 to 14 minutes. Residue was checked. Photoresist was then removed in NMP. 1 minute of plasma etching was added at 50W to improve metal adhesion. Finally, it was rinsed in microposit developer to remove residue of polyimide. It was rinsed again lastly in D.I. water. An illustration of this step is shown in Figure 2.12.
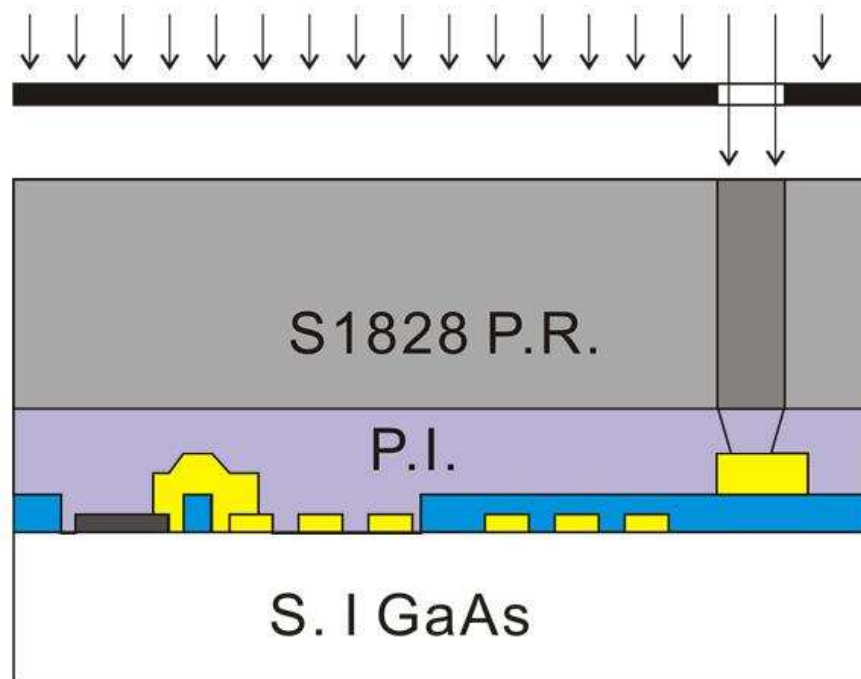
Figure 2.12 Step 4: Applying Polyimide layer 1.

Step 5 is about evaporating metal layer 2. Almost the identical processing steps in Step 3 were carried out again. After that, Step 6 is applying the second layer of polyimide layer (Polyimide layer 2), again, the same steps elaborated in Step 4 were taken. The final step of Step 7 is evaporating the final metal layer 3. Once again, identical steps undertaken in

Step 3 and Step 5 were carried out to apply the conductor layer. Illustrations of the final three steps are presented in Figure 2.13 to 2.15.
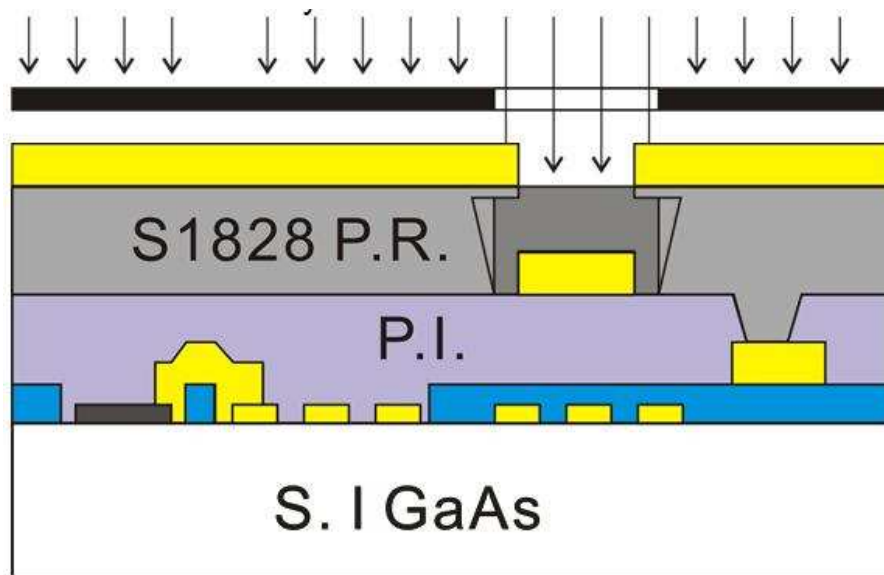
Figure 2.13 Step 5: Evaporating Au/Ti metal layer 2.
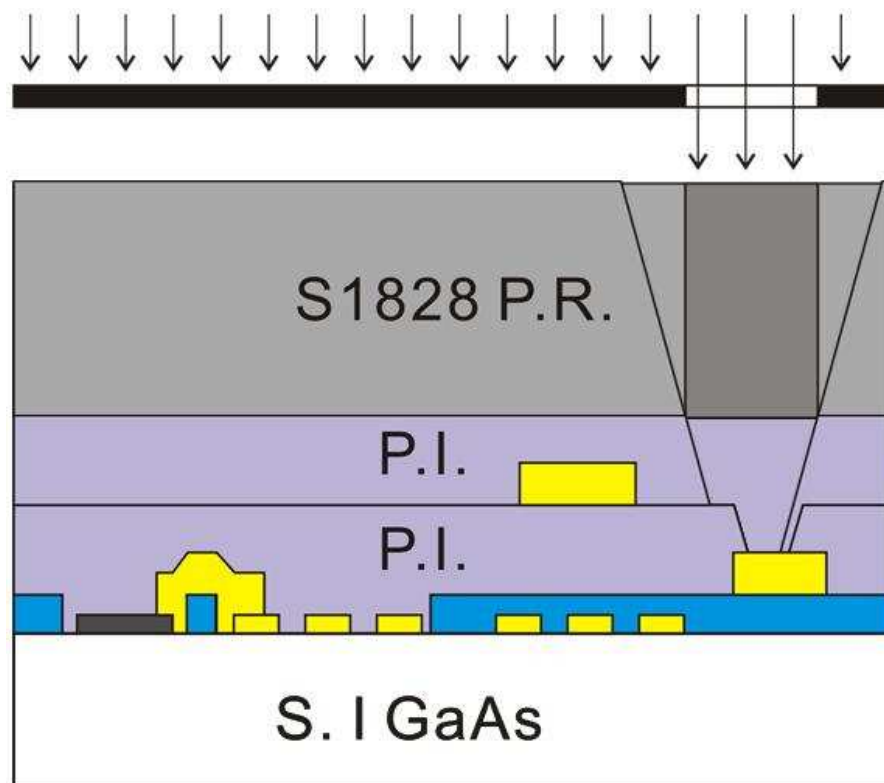
Figure 2.14 Step 6: Applying Polyimide layer 2.
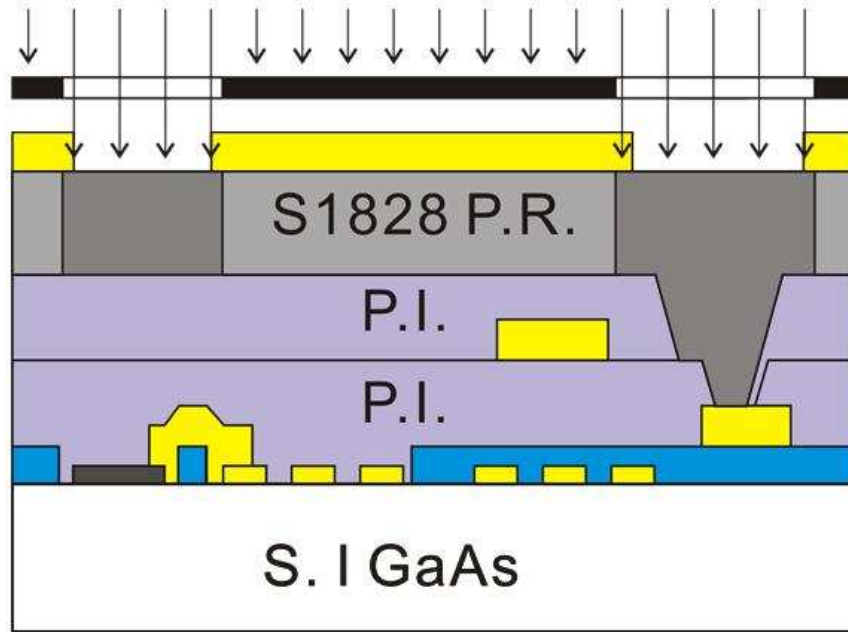
Figure 2.15 Step 7: Evaporating Au/Ti metal layer 3.

Due to the nature of the multilayer MMIC, each conductor and dielectric layers has to be provided with a mask design. Alignment among them was achieved with the help of alignment marks. Due to the nature of the polyimide, it is difficult to deposit gold conductor layers on it. That is why an alloy of Ti/Au was chosen in order to ensure the contact.

Figure 2.16 shows the mask set design of the 3D MMIC under investigation in this work. As can be seen, multilayer transmission lines with different geometries realising various impedances, couplers, inductors and capacitors with different designs and geometries together with demonstrations of integration of the pHEMTs with passive components realising a 2GHz CPW amplifier can all be found in this mask set. There is also a bandpass filter designed using multilayer passive components in this mask set.
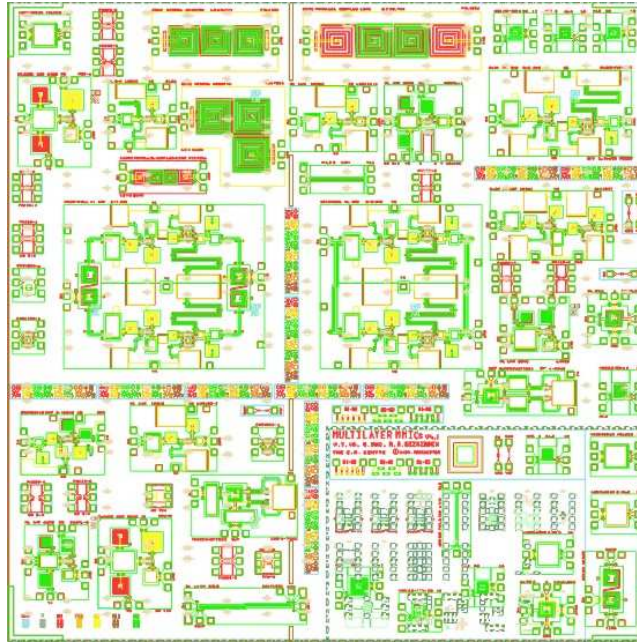
Figure 2.16 Mask set design (a single unit cell).

Although MMIC is a highly repeatable technology for industrial fabrication process, there are some limitations of the facilities available in the clean room of the University of Manchester. That is why uniformity study is vital and needs to be carefully investigated for parameter variations in this work.

2.2 III – V Transistors

2.2.1 Introduction

Driven by the advancement of lithography technology, transistor dimensions have continuously shrunk for the last few decades as predicted by Moore's Law [50]. As the dimension pushes into the sub-micron regime, it becomes more and more challenging to realise CMOS transistors with good and acceptable performance at microwave frequency. Both fundamental physics and practical considerations contribute to the limitation of Silicon technology scaling into sub-micron dimensions. As the gate length goes shorter and shorter coupled with the scaled down oxide, the off-state leakage current becomes a prominent issue. Other than that, as parasitic resistance and capacitance become comparable to the channel resistance and capacitance, a practical

limit as how small the scaling can go has been set. There are also considerations like how small the lithography can go and if single molecular transistor is possible.

In order to overcome the limitations of Silicon material, researchers around the world have been trying to find alternative semiconductor technology, among them compound III-V semiconductors are found. The fundamental physics of them having light effective masses means higher electron mobilities and larger output currents. All these make them attractive candidates for microwave applications.

2.2.2 Unipolar and Bipolar Transistors

Solid-state transistors can be generally categorised into two families, ie. unipolar and bipolar transistors. Unipolar transistors, also called field-effect transistors, deploy only one type of carriers, either electron or hole, to perform the transistor functions. Whereas, bipolar transistors are using both hole and electron carriers to perform the tasks. JFET (Junction Field-Effect Transistor), MOSFET (Metal-Oxide Semiconductor Field-Effect Transistor), MESFET (Metal Semiconductor Field-Effect Transistor), HEMT (High Electron Mobility Transistor) and pHEMT (pseudomorphic High Electron Mobility Transistor) are all unipolar transistors. On the other hand, BJT (Bipolar Junction Transistor) and HBT (Heterojunction Bipolar Transistor) are bipolar transistors. Another main difference between a unipolar and bipolar transistor is that unipolar transistor has higher input impedance than the bipolar counterpart [51].

Both unipolar and bipolar transistors have their own merits in terms of suitability for a specific application. Being unipolar or bipolar is not the sole reason for a particular device to be chosen for a given task. It also involves the semiconductor material used to construct the device. Silicon, Germanium, compound III-V semiconductors (GaAs, InP etc.) have all their special material property to make them especially suited for a certain job.

2.2.3 Microwave Applications

Amplifier and switch are the two major device applications at microwave frequency. High power outputs are the imperative task required for a power amplifier. The best power amplifiers are those who have high voltage, high current density, high power density and low thermal impedance. In order to minimise the losses due to impedance matching, the power amplifier should possess a very high input impedance. Of course, the gain of the device used must be the most important parameter to be judged as the suitability for power amplifier design. On the other hand, low noise and linear amplifiers require the device to be inherently low noise and highly linear.

Switch demands a different requirement from the device. As switching function does not require any gain from the device, gate resistance is not as important. Not only that, instead of matching the gate input impedance to the matching network, the gate of the switch uses the highest impedance to stop the RF energy from leaking to the biasing network. In MMIC technology, the most popular choice of switch is the FET. It is very compatible to and flexible to be integrated to the MMIC. The ON- and OFF-state of the FET switch are achieved by opening or shutting down the conducting channel. The main challenge of FET switch compared to PIN diode switch is that the OFF-state capacitance of FET switch is significantly higher than PIN diode switch, in other words, isolation is relatively poorer [52].

2.3 Principle of pHEMT

2.3.1 Introduction

As discussed above, field effect transistors (FET) can be fabricated using Silicon or Gallium Arsenide (GaAs). GaAs based active devices, due to its material property, can generally perform much faster than Silicon based devices. It is also why they are more suitable to be used for microwave and milimeter wave applications.

The differences between MESFET (Metal Semiconductor Field-Effect Transistor), HEMT (High Electron Mobility Transistor) and pHEMT (pseudomorphic High Electron

Mobility Transistor) are illustrated in Figure 2.17. In the figure, they are all n-type field-effect transistors, and HEMT and pHEMT have heterojunction formed in their structure to improve the performance achieving high electron mobility in the devices.
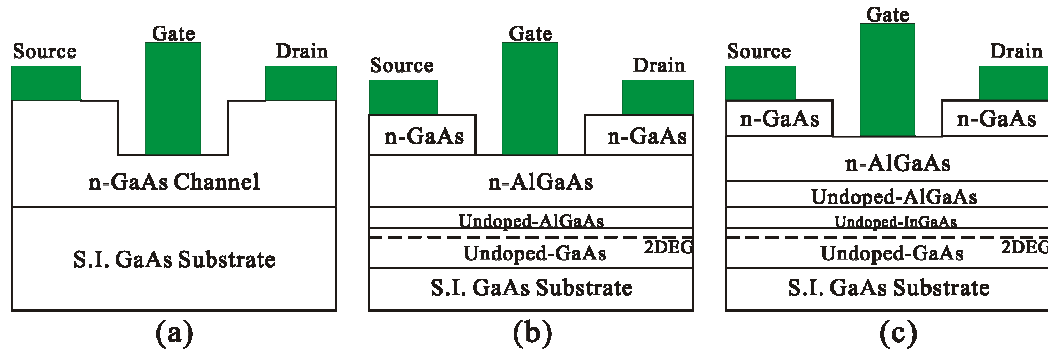
Figure 2.17 Structures of three types of FETs: (a)MESFET, (b)HEMT and (c)pHEMT.

Among them, MESFET has the simplest structure where a homogeneous material is used throughout the structure. For a device to perform good conductivity, high doping of impurities to generate the majority carriers is needed. However, for a structure like MESFET, high doping of the impurities would also introduce unwanted scattering effect hindering the electrons moving path in the channel. In other words, a higher channel resistance is observed [53].

That is why heterojunction is introduced [54-55]. Heterojunction is created when two material having two different energy bandgaps are joint together. Fundamental physics require the Fermi Levels of the two materials to be aligned, with that, at the interface, a quantum well is created with the bands bending in order to be joined together. The existence of the quantum well makes a good confinement for the electrons to travel in a certain path, the channel. The electrons are so well-confined in this path and hence it almost makes the electrons travel in 2 dimensions. Therefore, the electrons in this case are called 2DEG, 2 dimensional electron gas.

As shown in Figure 2.17, in HEMT, a ternary material AlGaAs is added on top of the GaAs. AlGaAs has a wider bandgap than GaAs, a heterojunction is thus formed at the interface of these two materials. AlGaAs can be taken as the supply layer, where high doping is done to generate n-type electron carriers. Before the interface of AlGaAs and GaAs, which is where the 2DEG is located, an undoped AlGaAs region is created. This

is sometimes called a spacer layer. Due to the fact that it is undoped, it creates a barrier for the 2DEG to escape from the quantum well, therefore a better confinement. As the doping is done in the AlGaAs supply layer, there is no need for doping done in the 2DEG GaAs channel layer. In other words, no impurities found in the channel layer which would further improve the mobility [53].

The latest improvement is seen in the pHEMT in Figure 2.17. Not any two materials could be joined and create the heterojunction. A lattice constant matched is a prerequisite for a heterojunction to be formed. However, it was found in 1990s that a lattice constant mismatched pair of materials could still be joined together to form heterojunction [56-58]. The requirement is that there is a limit on the thickness of the top material, it is called the critical thickness. As can be observed in Figure 2.17, a very thin layer of InGaAs is placed on top of the GaAs. InGaAs compared to GaAs can further improve the performance of the transistor because it can be made to have a very narrow bandgap and a much better confinement is made possible due to the bigger bandgap mismatch of AlGaAs and InGaAs.

One of the most important driver for compound semiconductor development is the advancement of growth techniques such as the Metal Organic Chemical Vapour Deposition (MOCVD) and Molecular Beam Epitaxy (MBE). For InGaAs and AlGaAs, the addition of Indium and Aluminium will alter the bandgap of the semiconductor according to (at 300K):

$$Al_{1-x}Ga_{1-x}As : E_g = 1.423 + 1.247x \qquad (2.1)$$
$$In_{1-x}Ga_{1-x}As : E_g = 1.423 - 1.53x \qquad (2.2)$$

Bandgap of the GaAs would increase with addition of Aluminium component but decrease with Indium. Bandgap engineering could thus be achieved and new transistor designs could be created and made possible. Stacking difference layers of material with varying bandgap (discontinuities of valence band and conductor band) could create heterojunctions which in turn would create quantum wells making the 2DEG possible. Not only accumulation of the carriers could be achieved, the heterojunctions could also introduce some migration barriers for the carriers which both would contribute to a high mobility transistor. This bandgap engineering could also be implemented in bipolar

transistors family, where both majority and minority carriers could be accumulated and confined in the respective mismatchs of valence or conduction bands. However, in the case of the unipolar transistors family such as pHEMT, only one type of carrier would be affected.

Figure 2.18 shows how the band diagrams would look like before and after the creation of heterojunction of AlGaAs and GaAs. Fermi level indicates the energy level that the probability of finding an electron is half. The spacing between conduction band and the Fermi level is defined as the relative electron density. As can be seen in Figure 2.18(b), along the conduction band, there is a "quantum well" area (falling below the Fermi level) where accumulation and confinement of electrons could be achieved. The differences in conduction band and valence band are represented by ΔE_C and ΔE_V respectively. Ideally, the difference in conduction band should simply be the difference in the electron affinities, X_1 and X_2 of the two materials:

$$\Delta E_c = X_1 + X_2 \tag{2.3}$$

And

$$E_{g2} = E_{g1} + \Delta E_c + \Delta E_v \tag{2.4}$$

Rearranging (2.4):

$$\Delta E_c + \Delta E_v = E_{g2} - E_{g1} = E_g \tag{2.5}$$

where X_1 = electron affinity in AlGaAs, X_2 = electron affinity in GaAs, Eg_1 = bandgap of AlGaAs ad Eg_2 = bandgap of GaAs.
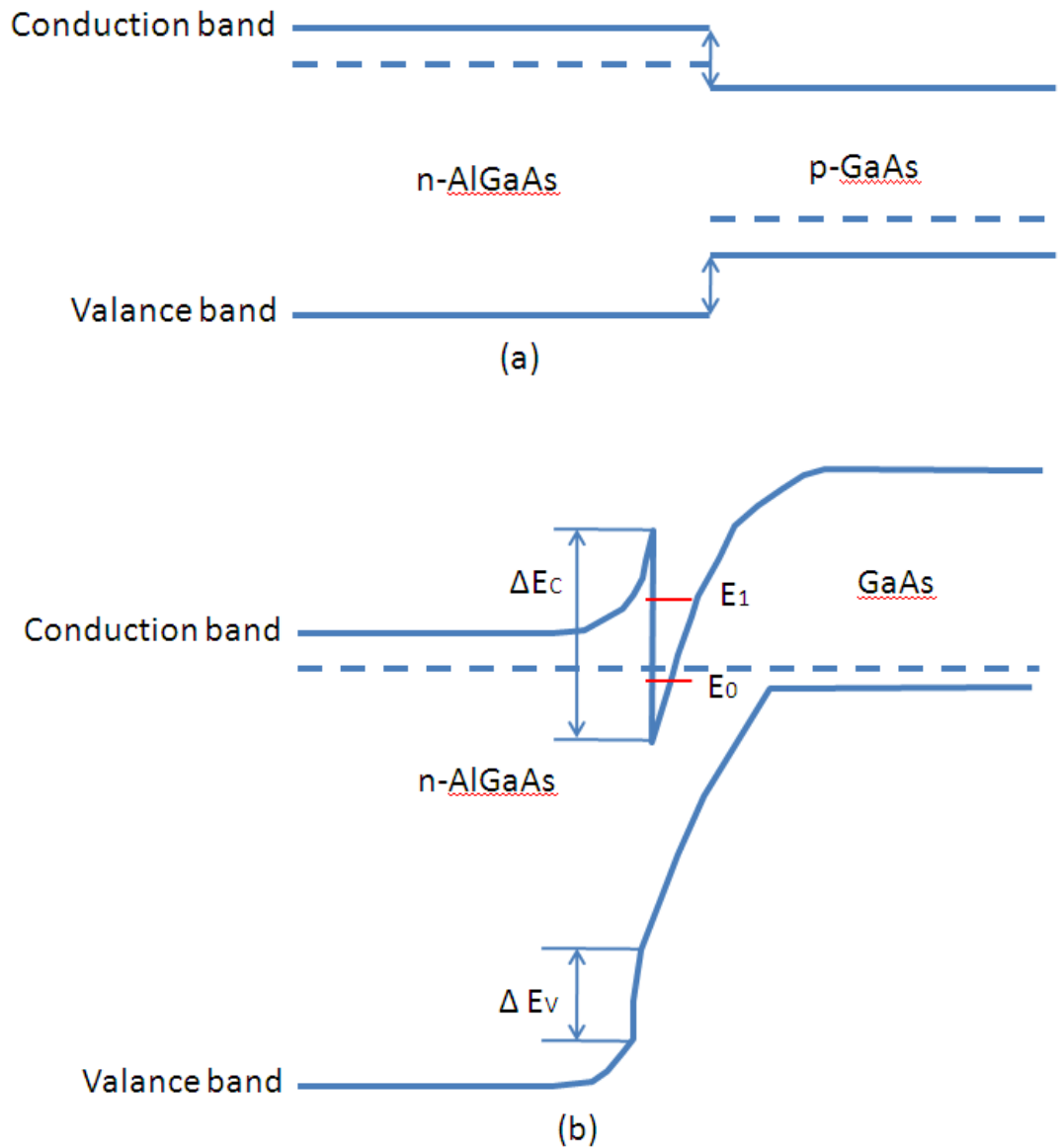
Figure 2.18 Band structure of AlGaAs/GaAs heterojunction: (a)before and (b)after connecting.

The operation of a pHEMT, or HEMT in this manner, is very similar to the operation of a MESFET. Figure 2.19 shows the operation of an n-type depletion-mode MESFET under common source configuration. The gate is used as the input and is reverse bias and the drain is used as the output and forward bias. A depletion region under the gate-semiconductor Schottky barrier is formed, due to reverse bias. This depletion region will have a rectifying effect on the electron transport along the channel which flows from the source to the drain end. It is clear that, if the gate voltage is fixed, as the drain voltage increases, more current will flow through. That is why, initially, for small drain voltage, the MESFET behaves like a resistor. However, as the potential at the drain end is

increased, the depletion width closer to the drain end will become larger, a point will be reached when the channel could accommodate the maximum velocity of the electrons. As this happens, the current starts to saturate.
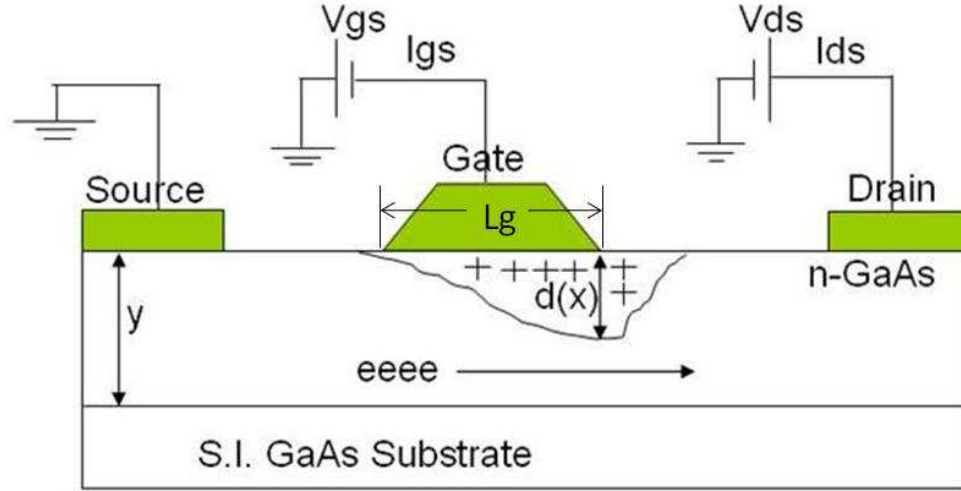
Figure 2.19 Cross-sectional view of a GaAs MESFET under common source configuration

For long channel (gate length $L_g \gg y$), based on constant low field mobility and gradual channel approximation, the current I_{ds} is given as [59]:

$$I_{ds} = Z[Y - d(x)]qN_d\mu \cdot \frac{dV}{dx}$$

(2.6)

where Z is the gate width, Y is the channel depth, d(x) is the depletion width and N_d is the doping concentration.

d(x), the depletion width, is given by [59]:

$$d(x) = \left\{ \frac{2\varepsilon_s[V(x)+V_{bi}-V_{gs}]}{qN_d} \right\}^{1/2}$$

(2.7)

where $\varepsilon_s = \varepsilon_0\varepsilon_r$ is the semiconductor dielectric constant, V_{bi} the built-in potential.

Substituting equation (2.7) into equation (2.6):

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$$I_{ds} = G_0 \left\{ V_{ds} - \frac{2[(V_{ds} + V_{bi} - V_{gs})^{3/2} - (V_{bi} - V_{gs})^{3/2}]}{3V_p^{1/2}} \right\}$$

(2.8)

where G_0, the channel conductance and is given by [59]:

$$G_0 = \frac{q\mu N_d ZY}{L}$$

(2.9)

and V_p, the pinch-off voltage when the depletion width d(x) equals the channel depth Y, is [59]:

$$V_p = \frac{qN_d Y^2}{2\varepsilon_s}$$

(2.10)

On the other hand, for short channel MESFET (small Lg/Y ratio), the $I_{ds(sat)}$ can be approximated as [59]:

$$I_{ds(sat)} = Z[Y - d]qN_d v_{sat}$$

(2.11)

where v_{sat} is the saturation velocity and the intrinsic transconductance, g_m, can be given by [59]:

$$g_m = \frac{\varepsilon_s Z v_{sat}}{d}$$

(2.12)

A typical DC characteristics of a pHEMT can be seen in Figure 2.20 and 2.21.
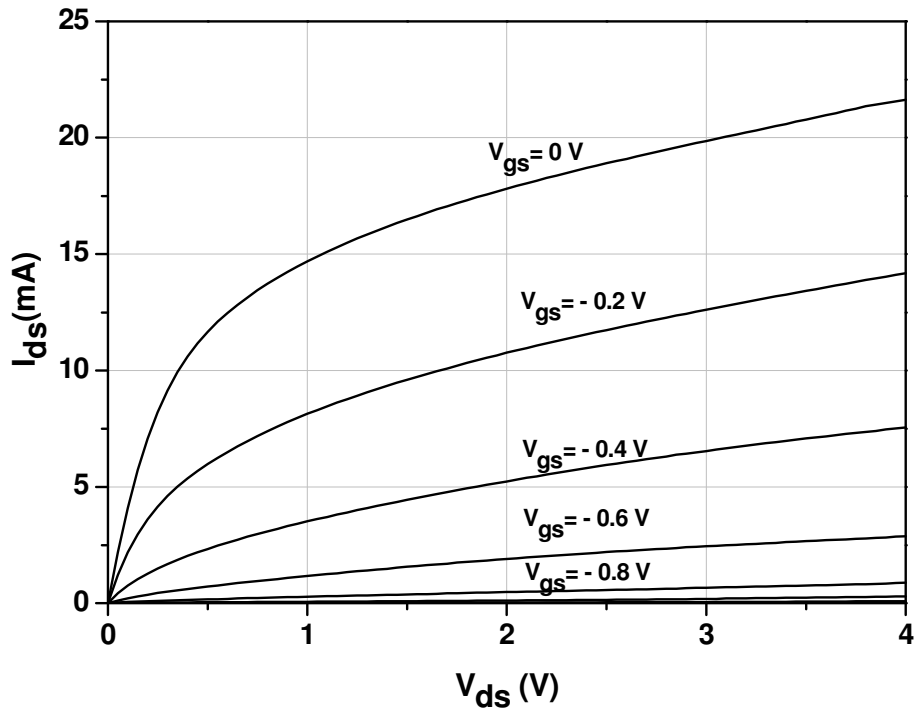
Figure 2.20 The output characteristics of a pHEMT.
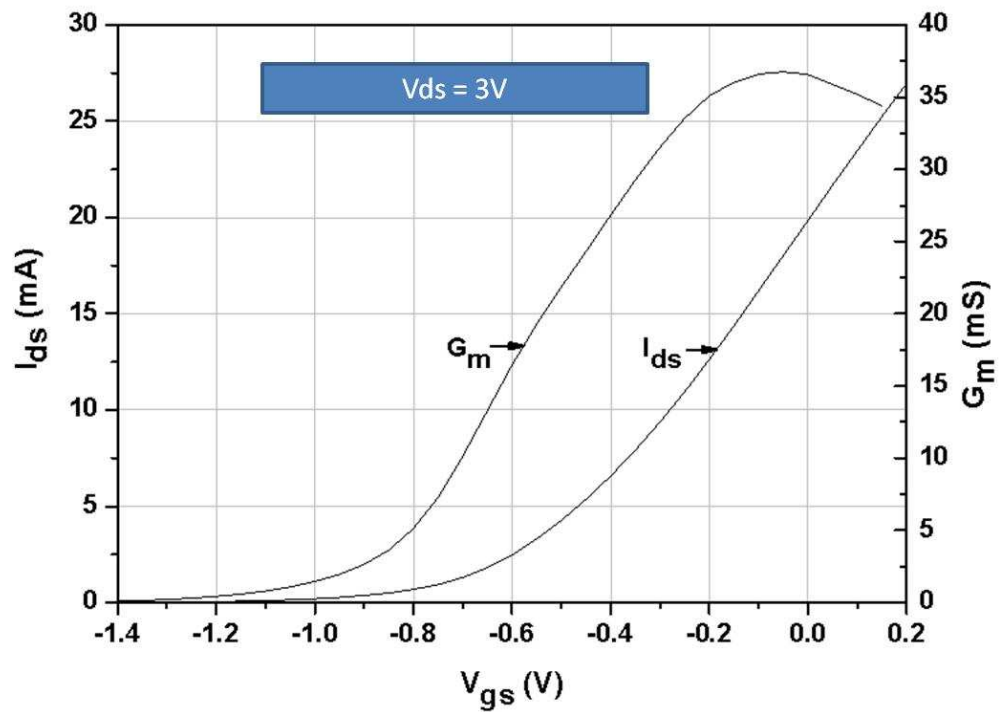
Figure 2.21 The transfer characteristics of a pHEMT.

2.3.2 Small-Signal Analysis

A small-signal model is developed through understanding of the underlying physics of the FET. The equivalent circuit is an abstraction and simplification which provides a representation of the FET that is manageable. Nonetheless, it must represent adequately all the important physical processed which take place in actual devices, including signal delay, charge and energy storage, current modulation and energy loss. Such a model is given in Figure 2.22 [60].
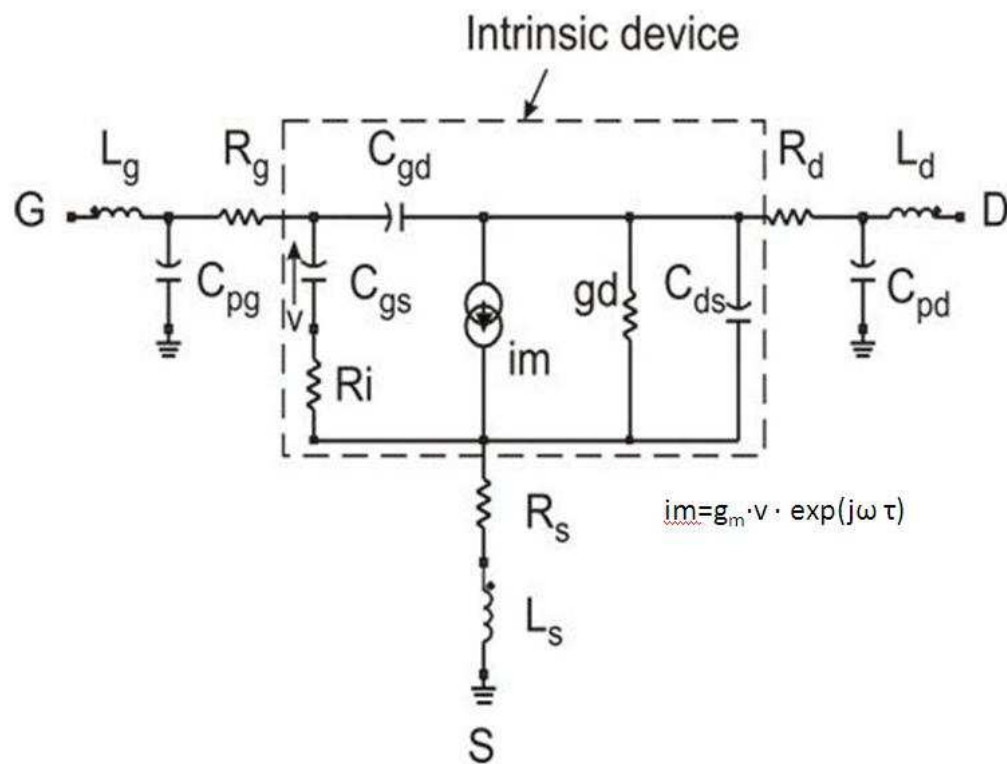
Figure 2.22 Small-Signal equivalent circuit of a FET.

All the parameters are developed both intuitively and empirically to the physics of a FET. C_{pg}, C_{pd}, L_g, L_d, L_s, R_g, R_d and R_s are extrinsic parameters and sometimes called parasitics. They are bias-independent and should remain constant for different biasings. C_{pg} and C_{pd} are the parasitic capacitances that are mainly made up of the sum of capacitances formed between the gate and drain contact pads to the ground. L_g, L_d and L_s are inductances of the three contacts. Dimensions and geometries of the source/drain pads and gate fingers are the most contributing factors to C_{pg}, C_{pd} and L_g, L_d, L_s. R_g, R_d

and R_s are the resistances associated to the three terminals. Note must be taken that not only the metalisation contacts attribute to the resistances, the semiconductor contact resistances and bulk resistances will contribute the overall R_s and R_d.

On the other hand, the intrinsic parameters are C_{gs}, C_{gd}, C_{ds}, R_i, g_d, g_m and τ. C_{gs} and C_{gd} are capacitances associated with the depletion region underneath the gate, as the bias changes the width of the depletion region, C_{gs} and C_{gd} will increase or decrease accordingly. C_{ds} is attributed to the substrate current, the substrate current can be seen as a leakage current from the main channel current and will contribute as a loss. The material used for the substrate will affect the value of the C_{ds}. R_i is the channel resistance, measuring how difficult the electrons flow in the channel and is apparently to do with the bias. g_d also called R_{ds}, is the drain to source conductance/resistance, it is again a parameter related to the substrate current and the material used for the substrate. g_m is the transconductance, indicating how much change in output current from a change of a given input voltage. It is one of the most important parameters which, generally speaking, can represent the gain of the device. Lastly, τ represents the time delay for the output current to be generated with the given input voltage [61-67].

Equations that can be used to calculate or evaluate these parameters values of the equivalent circuit following the technology are tabulated in Table 2.4 [53].

Table 2.4 Relationships of small-signal parameters to the physical properties of FET [53].

Element	Equation	Comment
$R_{contact}$	$\dfrac{1}{Z}\sqrt{\dfrac{\rho_c}{q\mu N_d Y}}$	Contact Resistance
R_{SG}	$\dfrac{L_{SG}}{qN_d\mu YZ}$	Bulk Resistance; $R_g = R_{contact}+R_{SG}$ L_{SG} is the distance between source and gate contact
R_{GD}	$\dfrac{L_{GD}}{qN_d\mu YZ}$	Bulk Resistance; $R_d = R_{contact}+R_{GD}$ L_{GD} is the distance between drain and gate contact
R_g	$\dfrac{\rho Z}{3m^2 hL}$	Gate Series Resistance; M = number of gate strips
C_{gs}	$\dfrac{\varepsilon_s ZL}{d}\left(1+\dfrac{X}{2L}-\dfrac{2d}{L+2X}\right)$	Gate-Source Capacitance
C_{gd}	$\dfrac{2\varepsilon_s Z}{1+2X/L}$	Gate-Drain Capacitance
R_i	$\dfrac{v_{sat}L}{\mu I_{ds}}$	Input Resistance; μ is the low field mobility
g_{m0}	$\dfrac{\varepsilon_s v_{sat}Z}{d}$	Intrinsic Transconductance
τ	$\dfrac{1}{v_{sat}}\left(\dfrac{X}{2}-\dfrac{2d}{1+2X/L}\right)$	Signal Delay
d	$\left[\dfrac{2\varepsilon_s(V_{SG}+V_{bi})}{qN}\right]^{1/2}$	Depletion Width
X	$\left[\dfrac{2\varepsilon_s}{qN_d(V_{SG}+V_{bi})}\right]^{1/2}(V_{DG}+V_{bi})$	Depletion Extension toward the Drain End
I_{ds}	$qN_d v_{sat}(Y-d)Z$	Drain-Source Current

2.4 Temperature Characterisation

High frequency operations often involve circuitry performing at high power level such as wireless communication and advanced radar systems. Gallium Arsenide (GaAs) has been one of the most popular semiconductors used in these applications and compared to Silicon, presents a whole new dimension of challenging thermal issue. It has always typically been assumed that a uniform distribution of heat generation across the surface is found for the case of Silicon. This assumption is not as applicable for GaAs devices [68-69]. The reason is being that the thermal conductivity of GaAs is approximately one-

third of Silicon and it is normally found that the generated heat distribution is localised rather than spread out in a uniform fashion.

There are mainly two important reasons to have a good knowledge of the thermal characteristics of GaAs devices. First is that electrical performance of a GaAs device is a function of temperature. The temperature dependent parameters include gain, efficiency, output power, phase shift and many more. The second reason is to have an accurate prediction of the device reliability.

In fundamental physics level, the most significant temperature dependent properties are bandgap of the material, electron saturation velocity, electron mobility, built-in potential and barrier height of the material, dielectric constants and specific contact resistance. The bandgap energy can be expressed as [70]:

$$E_{gap}(T) = E_{gap}(T_0) + \frac{\alpha T^2}{T + \beta} \qquad (2.13)$$

where α and β are constants. For GaAs, α is $-5.4 \times 10^{-4}/K^2$ and β is 204K. For trinary materials such as AlGaAs, InGaAs, their αs and βs are extrapolated according to the composition of the elements. Even though Equation (2.13) is not exactly linear, but over the temperature range from -25 to 125 °C, the deviation is barely noticeable.

The electron saturation velocity can be expressed as [70]:

$$v_{sat}(T) = v_{sat}(T_0)[1 + B_{vsat}(T - T_0)] \qquad (2.14)$$

where B_{vsat} is between -1 and $-2.5 \times 10^{-3}/°C$.

The change in the Schottky barrier height and surface potential with temperature can be expressed as:

$$V_{bi}(T) = V_{bi}(T_0) + m[E_{gap}(T) - E_{gap}(T_0)] \qquad (2.15)$$

where m is between 0 and 1.

Both dielectric constant ($X = \varepsilon$) and specific contact resistance ($X = \rho_c$) can be expressed as:

$$X(T) = X(T_0)[1 + B_X(T - T_0)] \qquad (2.16)$$

where $B_\varepsilon \sim 10^{-4}/°C$ and $B_{\rho c}$ will be determined by measurements.

Temperature will have different influence on these physical parameters and some will compensate or counter-affect the others. Overall thermal effect would be a resultant one and depends on the dominant parameters.

In this work, one of the objectives is to develop a temperature dependent small-signal model. It is observed that, apart from some extreme heat or cold, for a certain temperature range, for example from -25 to 125 °C, all the equivalent circuit parameters (ECPs), like those fundamental physical parameters mentioned above, will exhibit a linear temperature dependent relationship [70]. They can be expressed as:

$$P(T) = P(T_0)[1 + B(T - T_0)] \qquad (2.17)$$

Where B is the temperature coefficient (TC) in units per degree, T_0 is the reference temperature in $0°C$, and $P(T_0)$ is the value of the parameter at the reference temperature.

Chapter 3   Experimental Details

3.1 CAD Software

3.1.1 Integrated Circuit Characterization and Analysis Program (IC-CAP)

Agilent's IC-CAP is a powerful commercial software specialising in DC and RF semiconductor device modelling. It extracts accurate compact models for various applications, such as high speed/digital, analogue and power RF applications. Device technologies like silicon CMOS, Bipolar, III-V compound gallium arsenide (GaAs), gallium nitride (GaN) and many more in the industry are using IC-CAP to perform the tasks of measurement, simulation, optimisation and statistical analysis. IC-CAP not only provides a very reliable toolkit for the required tasks, it also manages to perform all these on a single platform [71].

There are several industry standard CMOS and FET models built-in available in IC-CAP. The excellent data acquisition and handling capabilities of IC-CAP allows user to perform some huge amount of measurements, extractions and optimisations with ease. The GUI is user-friendly, with flexibility of customising own specific routines. The interactions with other instrumentations, such as DC source, Vector Network Analyser (VNA) and other Time/Frequency domain instruments are done by the GPIB interface. Results obtained from the IC-CAP have also the flexibility of several popular formats that could be easily incorporated in some of the most popular CAD software in the market.

One of the key features of IC-CAP is that there is an inherently built scripting language, Parameter Extraction Language (PEL). With this programmable language, macros which automate huge amount of tasks could be established, minimising the human interference. Fast and accurate results could thus be achieved. In this work, IC-CAP is used to perform DC, RF measurements and model parameter extractions. The procedures or routines of these measurements and extractions are later written in macros and become

automated. A typical view of the IC-CAP working environment can be seen in Figure 3.1.
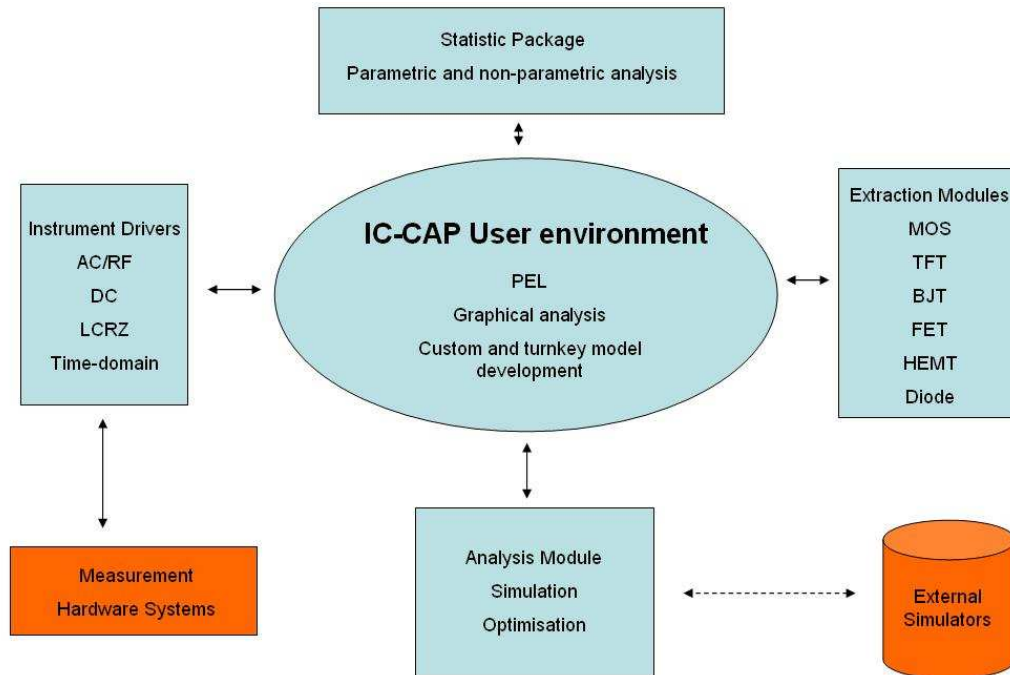
Figure 3.1 A pictorial view of IC-CAP environment [71].

3.1.2 Parameter Extraction in IC-CAP

With appropriate model chosen for the device under investigation, in order to perform parameter extraction in IC-CAP, routine has to be setup and configured. The required bias condition, measurement input parameters are to be configured in such a way that IC-CAP would understand and no errors to be found. So often, multiple measurements are to be taken and the results plotted in typical and representative graphs. Figure 3.2 shows a typical IC-CAP measurement setup. Extraction of parameter can then be achieved by manipulating the data. Usually, a set of expressions for the parameter are derived first from the theorised equivalent model, and judging from the expressions, a certain aspect of the measurement results would need to be taken and rearranged to extract the parameter. A typical procedure implemented in IC-CAP for parameter extraction is shown in Figure 3.3.
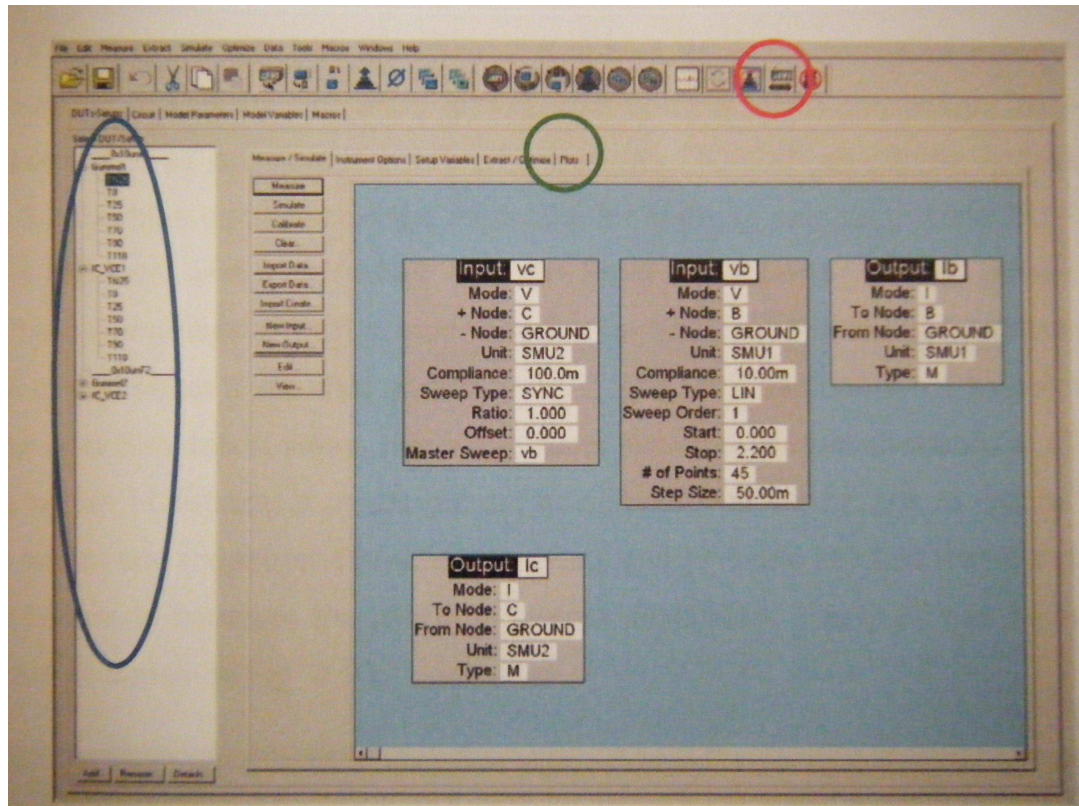
Figure 3.2 Typical IC-CAP window showing the DUT and Setups (Blue Oval) and the instrument server option (Red Oval).
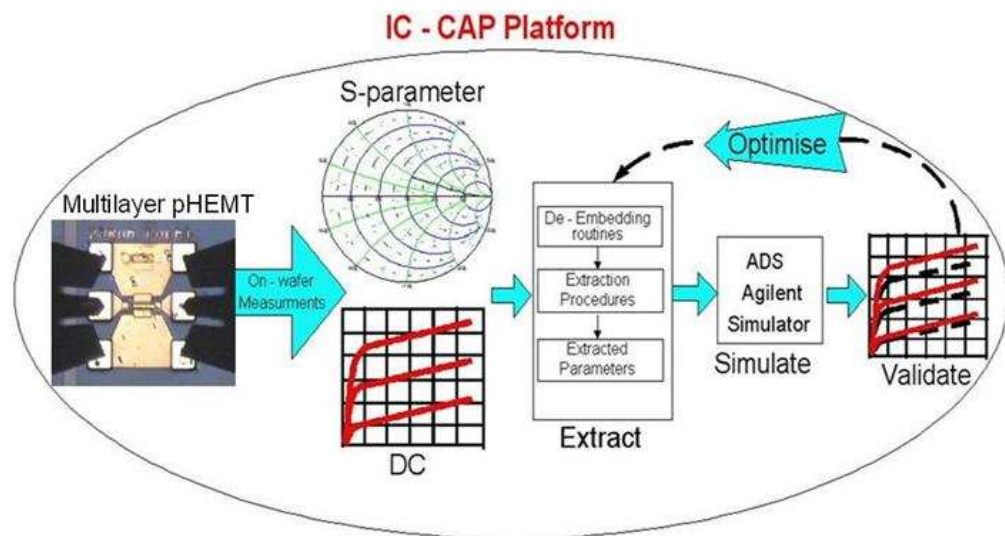
Figure 3.3 A pictorial view of parameter extraction using IC-CAP.

In this work, after the on-wafer direct DC and RF S-parameter measurements are taken, extraction procedure needs to be established. Figure 3.4 shows an example of parameter

extraction using the built-in programmable extraction language (PEL). The extracted parameters are then stored in IC-CAP. After that, these data are transferred to Agilent's Advance Design System (ADS). ADS is a circuit simulator which is totally compatible to the data formats of IC-CAP. Transferring of the data could be achieved via the data/instrument server option in IC-CAP. Simulation of the raw data could also be achieved in ADS. Although there is a built-in simulator in IC-CAP, in this work, simulation work is carried out in ADS. This is because an equivalent circuit model is adopted for the AlGaAs/InGaAs multilayer pHEMTs and ADS is an excellent circuit schematic simulator. It provides the flexibility and ease of reference to test-bench definitions. Comparisons between developed model and raw measurement are done in ADS as well, gaining the advantage of validation on a single platform. A flowchart of how IC-CAP makes decision of parameter extraction is shown in Figure 3.5.
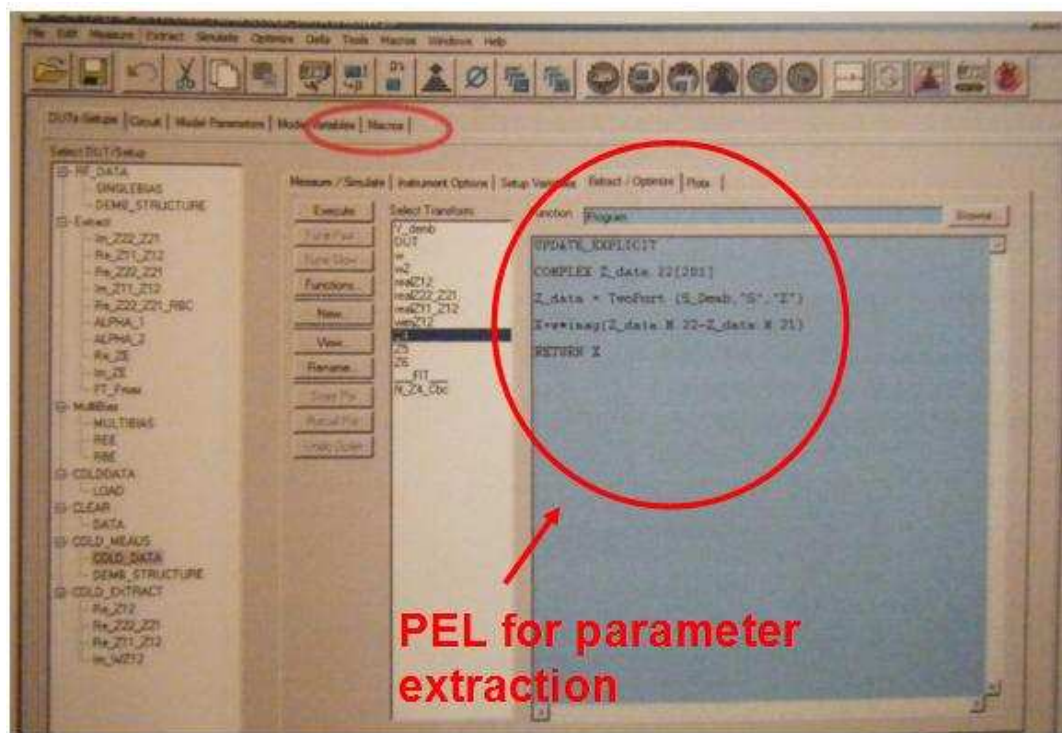
Figure 3.4 Parameter extraction using PEL in IC-CAP.
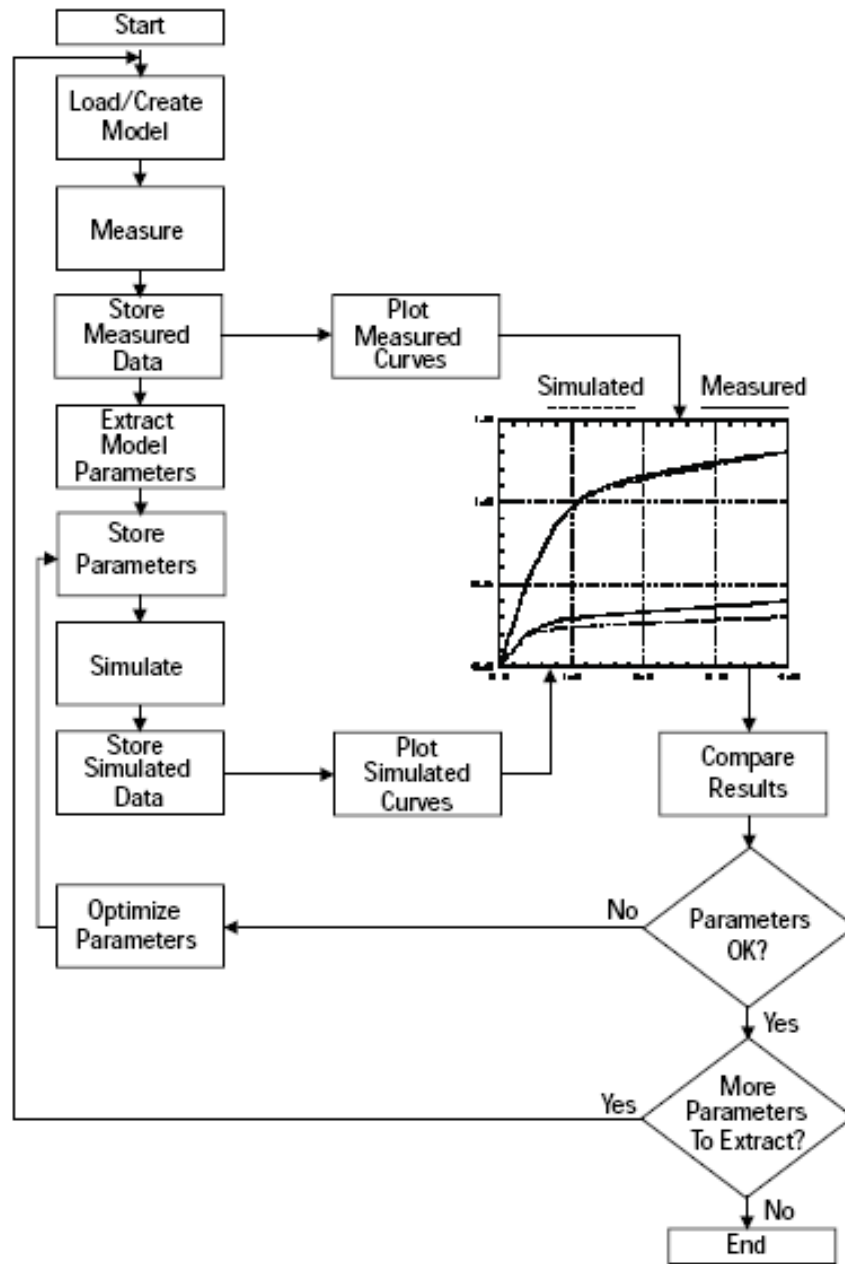
Figure 3.5 Work flowchart of IC-CAP during parameter extraction [71].

3.1.3 Device Modelling Tool

Agilent's Advanced Design System (ADS) is a useful CAD software, particularly suitable for electronic circuit simulation, that allows circuit design engineers to run circuit simulations in many settings, like time or frequency domain. Its comprehensive library of electronic components and the user-friendly environment make it a vital tool

for tasks such as designing, modeling, and optimization of performance for electronic device or circuit [72].

The popularity of ADS lies in the fact that it possesses a large amount of simulation modes and settings for various DC, AC and RF applications and high speed digital circuits. Optimisation and tuning can also be easily achieved with its built-in functions and settings. Specific optimised target and aims can be introduced but singularity must be taken care of by the user. Inherently, it provides several circuit configurations that reduce the complexity. Brief descriptions of the simulation types that used in this work are listed in Table 3.1.

Table 3.1 Descriptions of ADS simulation types [72].

Simulator	Description
DC	Fundamental to all simulations, it performs a topology check and an analysis of the DC operating point of a circuit.
AC	Obtains small-signal transfer parameters, such as voltage gain, current gain, and linear noise voltage and currents. This simulator is useful in designing passive circuits and small-signal active circuits such as low-noise amplifiers (LNAs).
S-parameter	Provides linear S-parameters, linear noise parameters, transimpedance (Z_{ij}), and transadmittance (Y_{ij}), by linearizing the circuit about the DC operating point and performing a linear small-signal analysis that treats the circuit as a multiport. Each port is turned on sequentially. S-parameters can be converted to Y- and Z-parameters.

The DC simulation provides the DC operating characteristics of a circuit design. The simulator calculates the response of a circuit to a particular stimulus by solving it numerically with formulated circuit equation system. Small-signal, linear AC analysis is carried out in AC simulation in ADS and small-signal transfer parameters, such as voltage gain, current gain, transimpedance, transadmittance, and linear noise are computed. Two-port scattering parameters (S-parameters) simulation can also be performed in ADS, where a circuit network under investigation will be simulated and computed with the inherent formulated equations. The result is a set of S-parameters that user can study and possibly optimise. Conversion to other 2-port parameters such as Z, Y, ABCD parameters can also be carried out in ADS.

Basic simulation procedure in ADS goes through the first step of creating the schematic, adding stimulis such as current probes, labelling wires and pins and indentifying the nodes of which to collect the data. Next, a simulation method has to be selected with required parameters specified. After that, a simulation can be carried out. Most of the straight forward simulations could be done in a short time, normally in a few seconds. With the completion of the simulation, acquired results could be viewed as specified. Detailed or brief operating data could be reported as well. As plotting has been the most popular and easiest way to interpret results, a new data display window could be created with results plotted in various meaningful plots such as, logarithm S-parameters (dB/Frequency) or Smith Chart. After everything, the circuit schematic could be retuned and optimised with targets or aims specified. An example of a circuit schematic created in ADS can be seen in Figure 3.6.
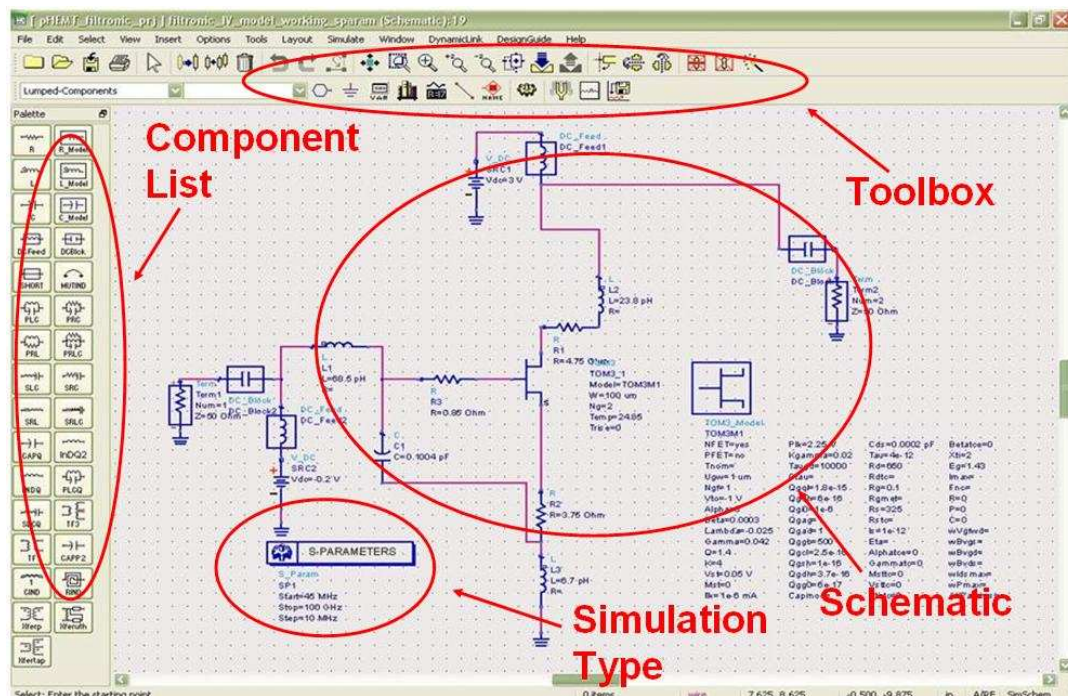
Figure 3.6 ADS Schematic simulator user interface.

3.2 On-Wafer RF and DC Measurements

In this work, on-wafer DC and RF measurements are carried out providing a fast, accurate and repeatable way of charaterising the devices. Agilent's Vector Network

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Analyser (VNA) HP85107A, DC source HP4142B, Cascade Microtech probe stations and Ground-Signal-Ground (GSG) probes are all hooked up together to perform the measurement tasks. The VNA is capable of RF S-parameter measurements up to 110 GHz in frequency domain while the Cascade Microtech probes could be used up to 40GHz. DC control and biasing is provided by the HP4142B DC source. The equipment setup is shown in Figure 3.7.
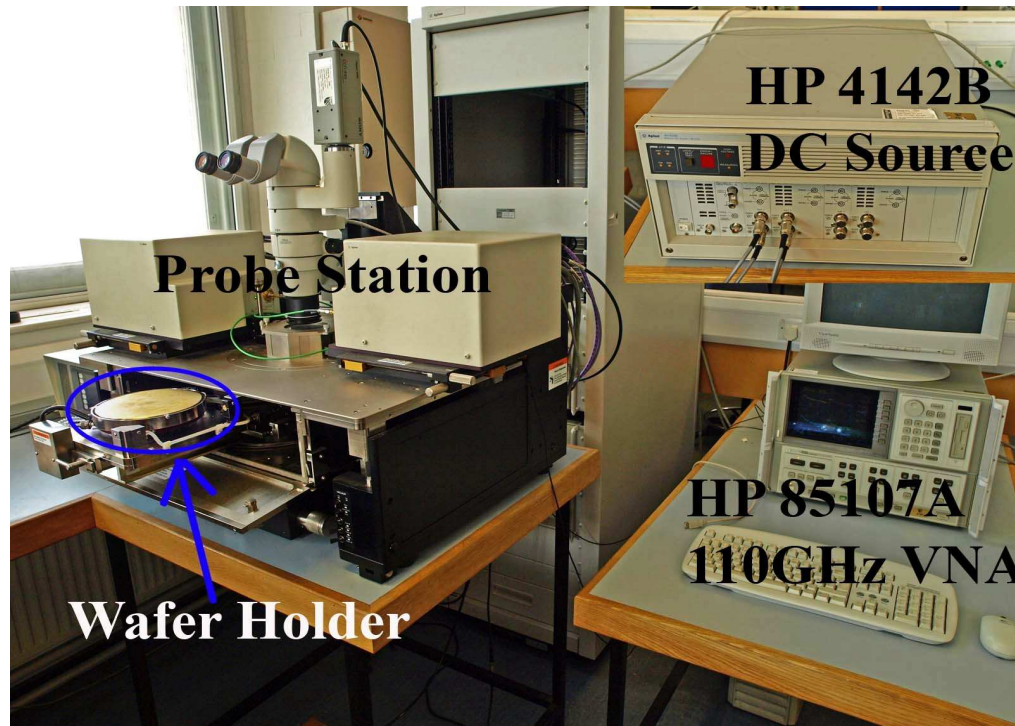
Figure 3.7 On-wafer measurement setup showing the HP 85107A VNA, HP 4142B DC source, probe station and wafer holder.

Figure 3.8 shows the multilayer pHEMT investigated in this work under probes. In addition, a useful technique is adopted in which during the small-signal modelling of pHEMT, empty pads or dummy structure, where only layout design is present, are measured. As a result, parasitic capacitances in the small-signal model can be determined more easily. Empty pads of the multilayer AlGaAs/InGaAs pHEMT can be seen in Figure 3.9.
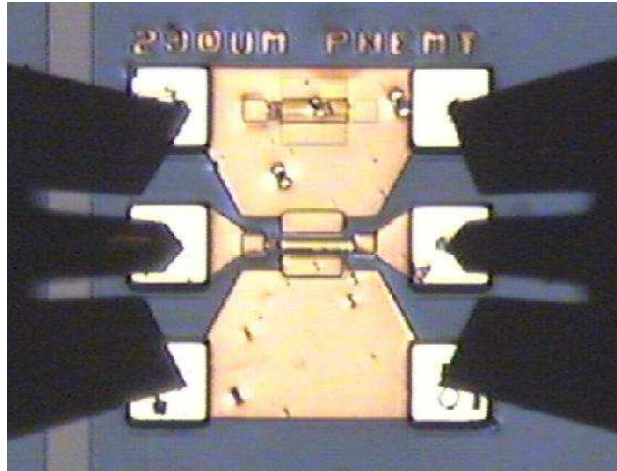
Figure 3.8 Micrograph of a multilayer pHEMT under on-wafer probing.
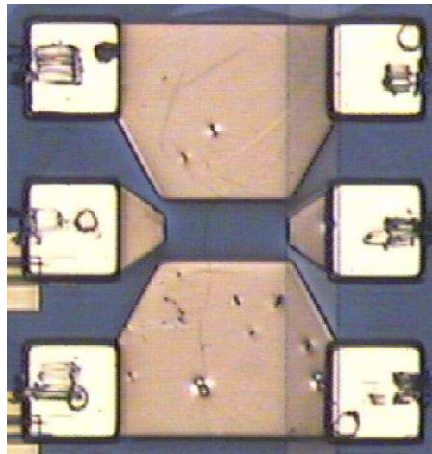
Figure 3.9 Micrograph of an empty pad of the multilayer pHEMT.

3.2.1 Calibration Technique

Parasitics are well known errors associated with RF measurements. It exists in interconnects like cables, wires, probing tips and etc. The parasitic inductances, resistances and capacitances have to be removed in order to have accurate reading of measurement. Moreover, so often, phase reference planes have to be realigned to the edge of the device under test (DUT) instead of the contact points of VNA. It is therefore, a careful calibration has to be carried out to eliminate the unwanted parasitic effects. A Line-Reflect-Reflect-Match (LRRM) advanced calibration method is used in this work and the calibration standard is provided by the probes manufacturer, Cascade Microtech.

The associated calibration software, WinCal, is installed in a PC and can be hence controlled by the user [73].

An illustration of the calibration standard used in the LRRM calibration method is presented in Figure 3.10. As required, open, short, load and thru standards are needed to have proper calibration. The through-line delay and DC resistance of matched load needs to be specified during the calibration process. A successful calibration graph is presented in Figure 3.11. It should be noted that for the following temperature study and measurements, for each measured temperature, calibration is carried out everytime after the temperature stabilising period of half an hour.
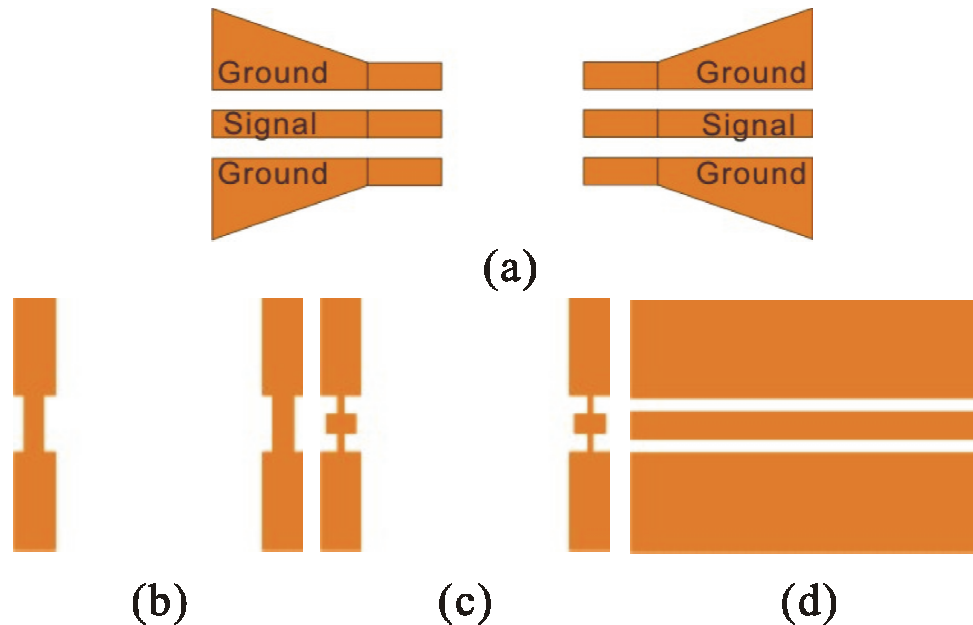
Figure 3.10 GSG probes and calibration standards for LRRM method: (a) GSG probes, (b) short standard, (c) load standard and (d) through standard.
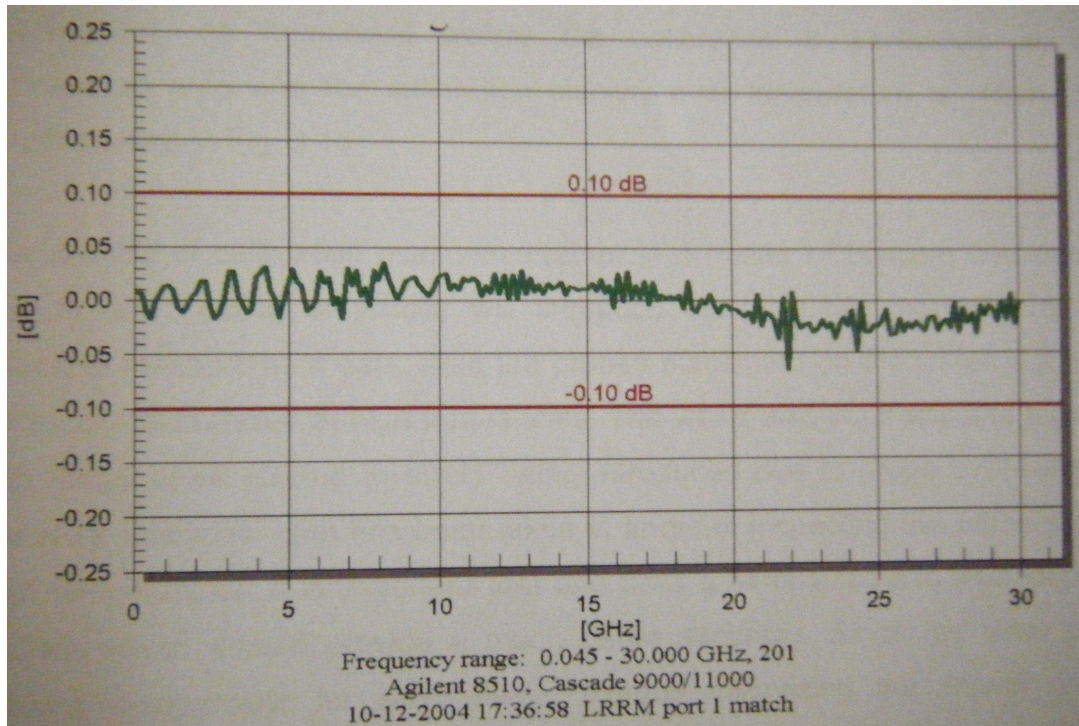
Figure 3.11 Magnitude of S11 versus frequency showing a good calibration of S-parameter measurements (±0.05 dB of error).

3.2.2 Temperature Control Tool

One of the key components of this work is concerned with the temperature study of pHEMTs incorporated into the multilayer technology. Therefore, temperature control equipment is needed to perform measurements covering several temperatures over a broad range. The specific temperature of the device is introduced by means of creating an ambient temperature through the wafer chuck. A temperature stabilising period is required to have accurate measurement. This is normally done by leaving the wafer in the temperature control chamber for more than 30 minutes. A Temptronic TP03200A temperature control unit together with the temperature control wafer chuck are integrated with the VNA in this work. The equipment provides an accuracy of $\pm 2^{\circ}$C. Figure 3.12 shows the pictures of the wafer chuck and the temperature control unit. For each temperature setting, a stabilising period of 30 minutes would be provided.

(a) **(b)**
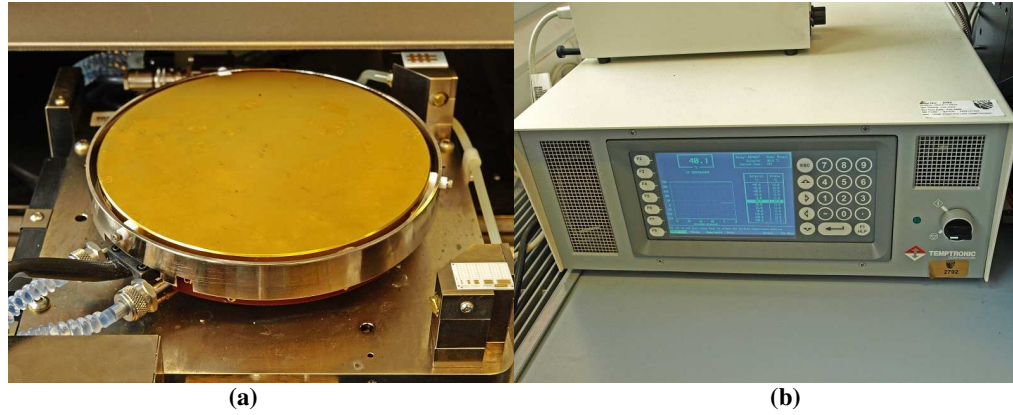
Figure 3.12 The temperature control equipment: (a) temperature controlled wafer chuck and (b) Temptronic TP03200A temperature controller.

3.3 S-Parameters

A popular and useful way of representing the idea of input and output powers for a specific RF/microwave network is using the Scattering parameters, or S-parameters. Transmitted and reflected powers can also be easily interpreted by S-parameters. A N-port network can be described by a matrix of S-parameters, incident travelling waves and reflected ones from the ports are defined and expressed as [74]:

$$
\begin{bmatrix} b_1 \\ b_2 \\ \vdots \\ b_N \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} & \cdots & S_{1N} \\ S_{21} & & & \vdots \\ \vdots & & & \vdots \\ S_{N1} & \cdots & \cdots & S_{NN} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \\ \vdots \\ a_N \end{bmatrix} \tag{3.1}
$$

where [S] is called the scattering matrix, [a] is the incident wave matrix and [b] is the reflected wave matrix. Figure 3.13 shows a sketch of how [a] and [b] can be seen in an N-port network.
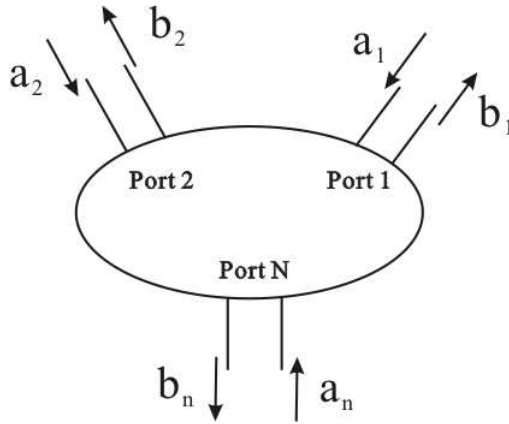
Figure 3.13 An N-port microwave network.

A specific element of scattering matrix, [S] can be expressed as:

$$S_{ij} = \left. \frac{b_i}{a_j} \right|_{a_k = 0 \, for \ \ k \neq j} \tag{3.2}$$

For example, in a 2-port network, the [a] and [b] are related to the S-parameters as:

$$b_1 = S_{11}a_1 + S_{12}a_2 \tag{3.3a}$$

$$b_2 = S_{21}a_1 + S_{22}a_2 \tag{3.3b}$$

This 2-port network could also be extended to multiple-port networks with the incident and reflected waves at each ports defining the characteristics of the corresponding ports. One of the main advantage of describing electrical functions in S-parameters is because of the fact that voltages and currents at high frequency are very hard to be quantified and described correctly.

S-parameters can also be regarded as normalized power for their definition:

$$|S_{11}|^2 \Rightarrow Normalized \ reflected \ power \ of \ port1$$

$$|S_{12}|^2 \Rightarrow Normalized \ transmitted \ power \ from \ port2 \ to \ port1$$

$$|S_{12}|^2 \Rightarrow Normalized \ transmitted \ power \ from \ port1 \ to \ port2$$

$\left| S_{11} \right|^2 \Rightarrow Normalized\ reflected\ power\ of\ port2$

Chapter 4   Results and Discussion

4.1 Device Structure

The pHEMT that is under investigation in this report is an AlGaAs/InGaAs/GaAs pHEMT with gate length, L_g, of 0.5 µm and gate width, W_g, of 100 µm, it has 2 gate fingers making it a 0.5x200 µm^2 pHEMT, its top and cross-sectional view are shown in Figure 4.1 [75]. Probing pads have been fabricated for the purpose of characterising this pre-multilayer-processed (virgin) pHEMT. The layout of the virgin sample is shown in Figure 4.2.

The main study here is to investigate the effects of multilayer processing on the active devices. Therefore, probing pads have also beeen fabricated on both the pre-multilayer-processed (virgin) and post-multilayer-processed (multilayer) pHEMTs as shown in Figure 4.2. The layout designs of the probing pads of virgin and multilayer pHEMTs are different due to some constraints of initial multilayer processing. Nonetheless, only the parasitics of the interconnects are expected to be affected, the active region of the devices are still the same. In this chapter, various comparisons between the virgin pHEMTs and multilayer pHEMTs are made to study the effects of multilayer processing.
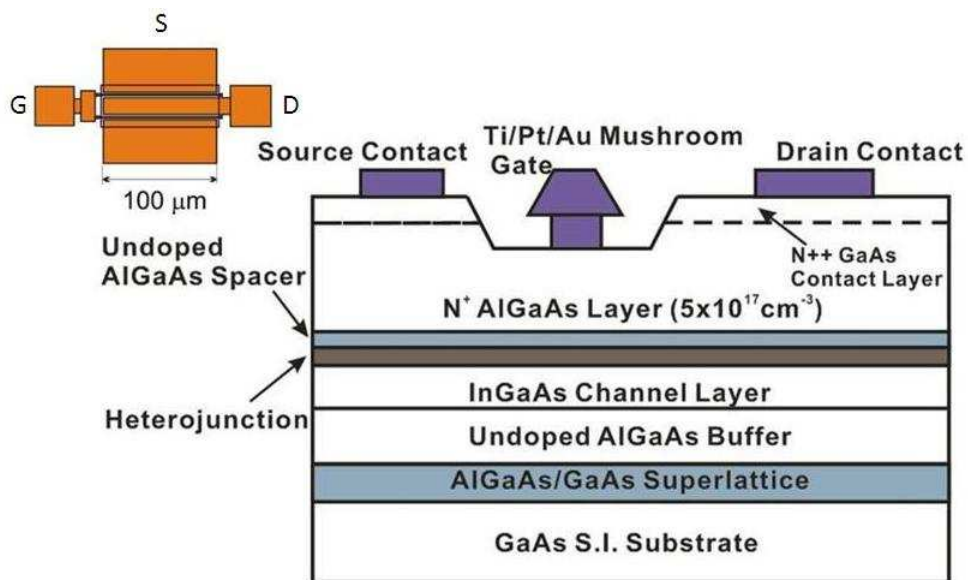
Figure 4.1 Top and cross-sectional view of the AlGaAs/InGaAs pHEMT.
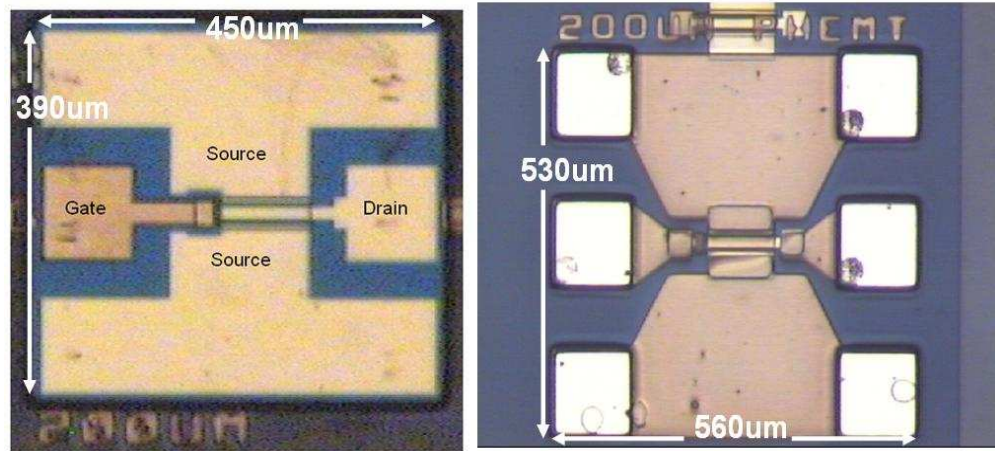
Figure 4.2 Micrographs of the fabricated pre- (virgin) and post-multilayer-processed multilayer pHEMTs.

pHEMTs incorporated in multilayer CPW MMIC technology will have layers of polyimide and metal layers added on top of the pHEMTs. A conceptual drawing of how the pHEMTs are positioned in the multilayer MMIC is depicted in Figure 4.3 [12]. In this figure, it can be seen how the three terminals of the transistor, drain, source and gate are connected to the rest of the circuitry.
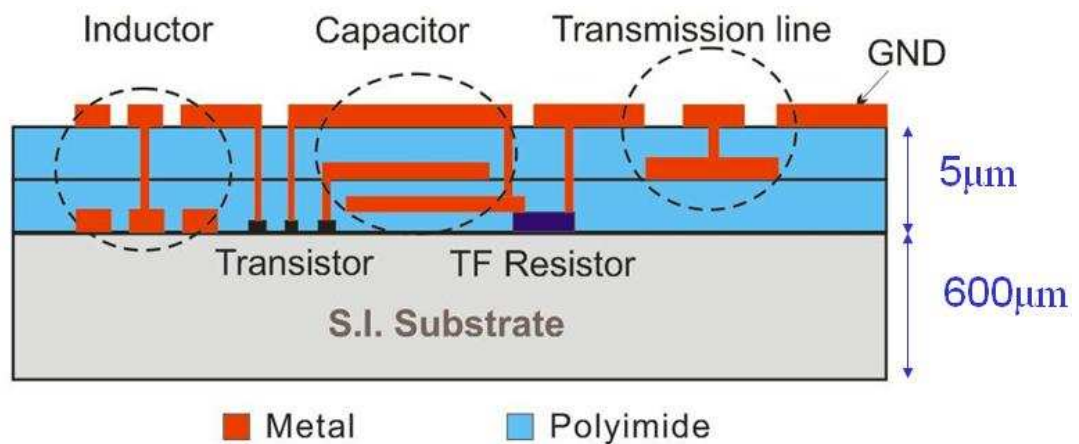
Figure 4.3 Illustration of the multilayer fabrication process technology [12].

4.2 Uniformity of pHEMTs

Uniformity is important to ensure good yields from the device fabrication. Insights can also be gained in terms of the limitation of fabrication technology. When active devices

are incorporated in the multilayer CPW MMIC technology, they are first fabricated on the semiconductor wafer. This has been provided by a semiconductor wafer fabrication foundry, Filtronic Compound Semiconductor. Following this, various passive components such as inductors, capacitors, transmission line etc have been fabricated by the research group at Manchester using the established multilayer processing using polyimide as dielectric and Ti/Au as conductor track.

In this section, the uniformity of the pre-multilayer-processed (virgin) pHEMTs is first investigated followed by investigating the uniformity of the post-multilayer-processed (multilayer) pHEMTs.

4.2.1 Uniformity of the Virgin pHEMTs

In this section, the uniformity of the virgin pHEMTs is investigated first to get an idea of the quality of this parameter on one of the prefabricated multilayer wafers. Five virgin pHEMTs are chosen at different representative locations to reflect the degree of consistency. A simplified sketch to indicate the locations of the chosen five virgin pHEMTs is shown in Figure 4.4. The chosen five are all pHEMT2, the one in the middle, from each cells. The dimension of each cell is 12mm x 12mm.
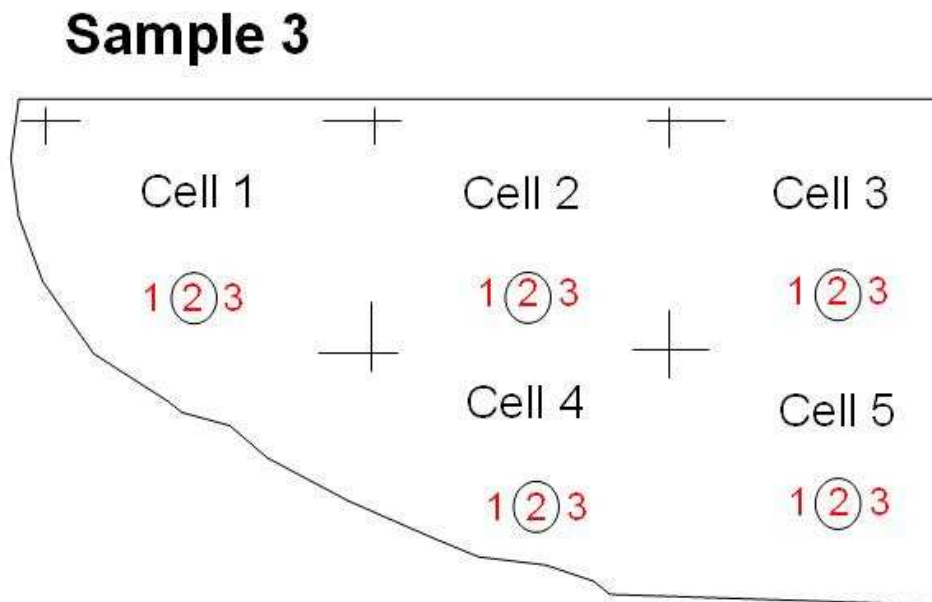
Figure 4.4 Sketch showing the locations of the chosen five (circled) virgin pHEMTs on Sample 3.

Figures 4.5 and 4.6 show the measured DC input characteristics and output characteristics of these five virgin pHEMTs. These data suggest that the uniformity of these devices is generally good within the manufacturing limitations. A closer look at the data of figure 4.5 suggests the pHEMTs in Cells1 and 4 have relatively poorer performances (lower output currents) as compared with the devices located on the other cells. This can be attributed to the fact that the pHEMTs in these two particular celles are located close to the edge of the sample and may have been degraded due to the unavoidable limitations of fabrication.
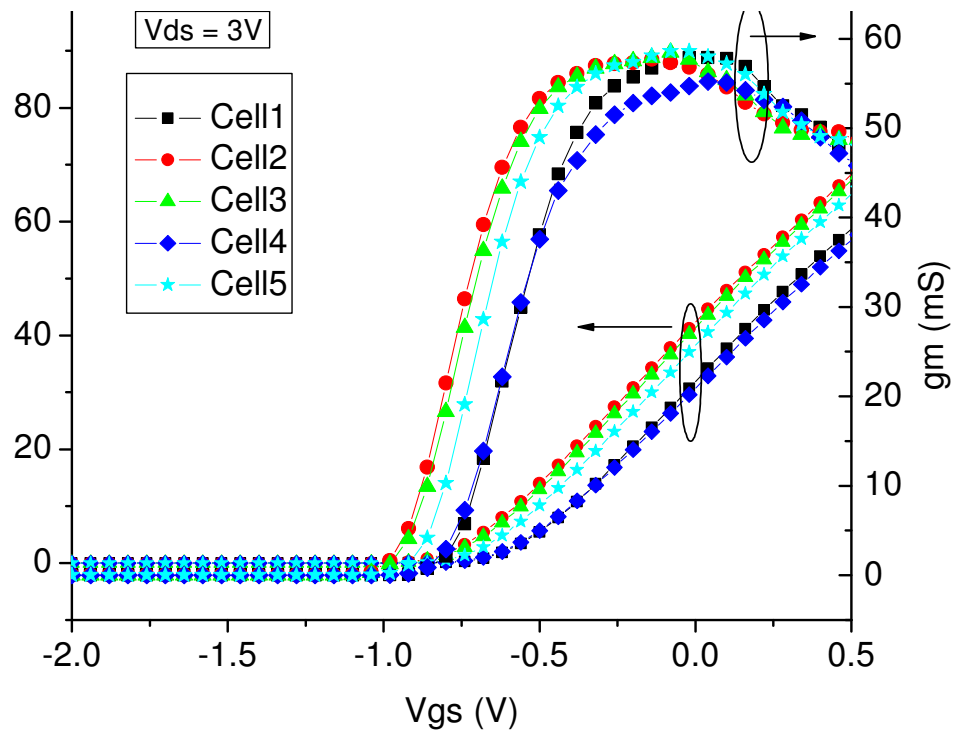
Figure 4.5 Measured transfer characteristics of the five virgin pHEMTs (0.5x200 µm^2) at room temperature.
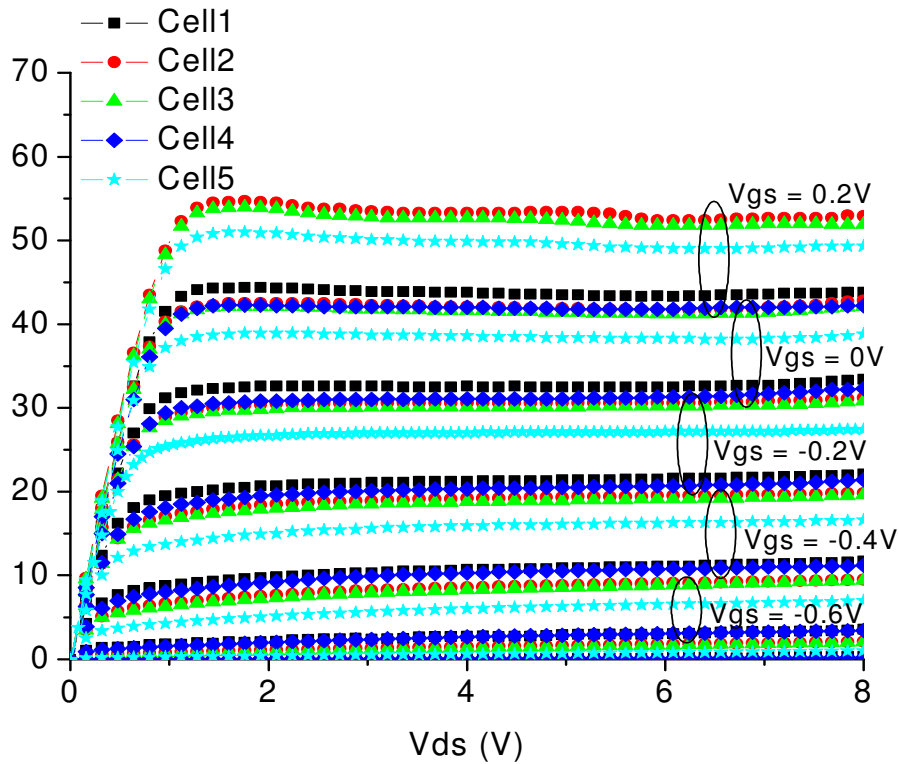
Figure 4.6 Measured output characteristics of the five virgin pHEMTs (0.5x200 μm^2).

Next, in order to look into the uniformity of these five virgin pHEMTs at high frequency operation, on-wafer S-parameters measurements are carried out from 45 MHz to 60 GHz using HP8510C Network Analyzer controlled by IC-CAP at biasing conditions of V_{gs} = -0.2 V and V_{ds} = 3 V. The devices are biased via ground-signal-ground microwave probes using Agilent 4142B Modular DC source/monitor in conjunction with IC-CAP. All the measurement setups are configured on IC-CAP, which administers the instruments connected via a standard GPIB interface. The measured S-parameters of the five virgin pHEMTs version are shown in Figures 4.7 and 4.8, whereas, Figure 4.9 shows the current and power gains respectively in which cut-off frequency and maximum available gain frequencies can be determined.
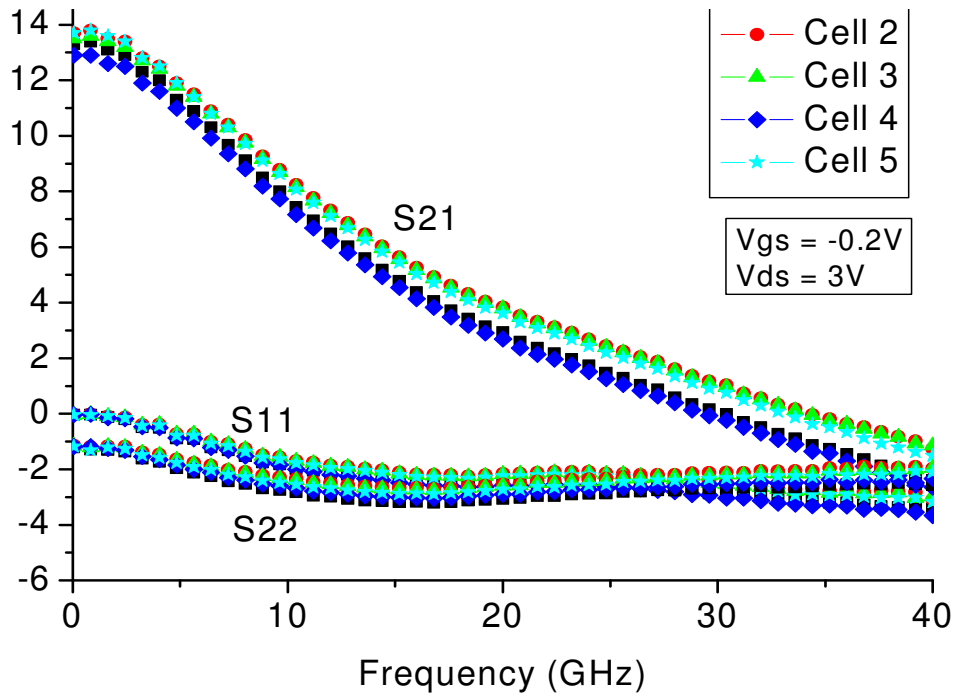
Figure 4.7 S11, S21 and S22 of the five virgin pHEMTs ($0.5 \times 200 \ \mu m^2$).
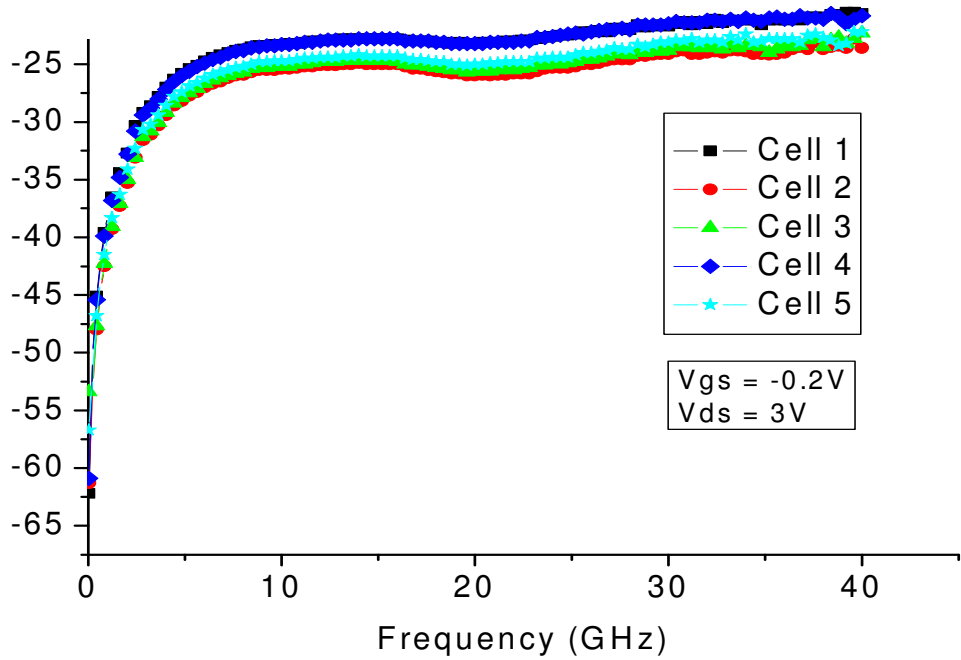
Figure 4.8 S12 of the five virgin pHEMTs ($0.5 \times 200 \ \mu m^2$).
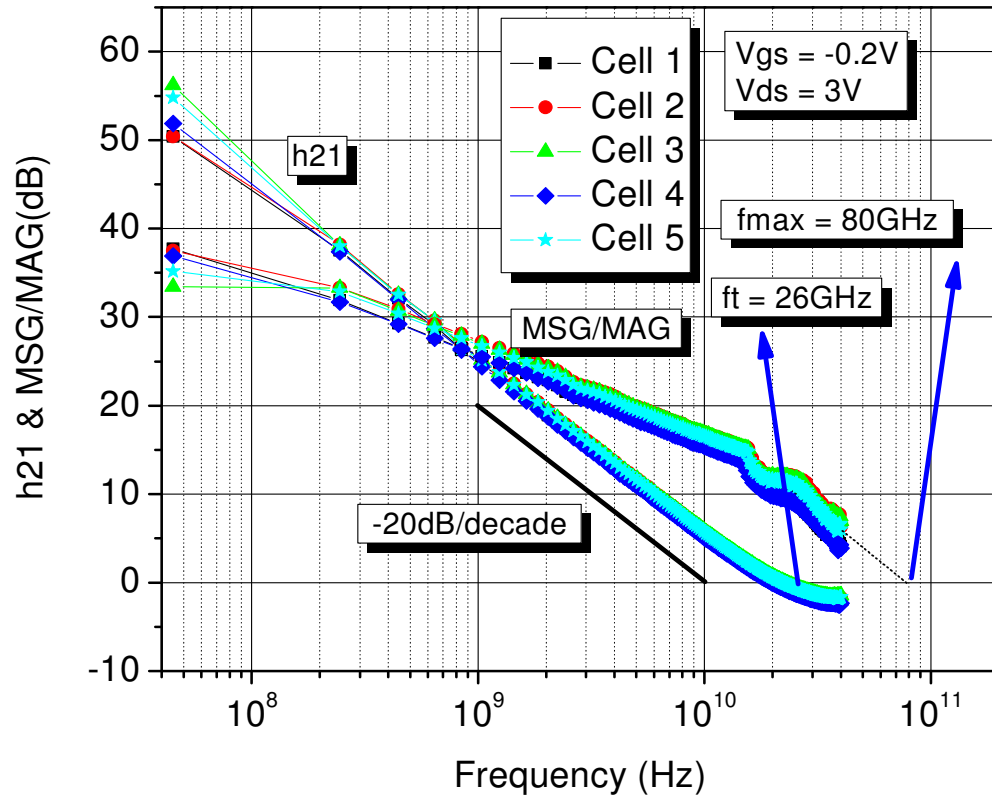
Figure 4.9 Current and power gains of the five virgin pHEMTs (0.5x200 μm².

Again, pHEMTs from Cell1 and Cell4 are noted in Figures 4.7 to 4.8 to have relatively poorer performances at high frequency regime, notably lower gains, poorer isolations and lower cut-off frequencies. Apart from these two devices the uniformity of the virgin pHEMTs is generally good.

4.2.2 Uniformity of the Multilayer pHEMTs

Uniformity of processing is important to ensure fabrication quality is met. In order to investigate the uniformity of the post-processed pHEMTs (ie those devices which have gone through the multilayer process fabrication), DC and S-parameters measurements are performed on five chosen multilayer pHEMTs at different locations on the wafer. These five multilayer pHEMTs are named after the unit cells that they are located, they are Cell1, Cell2, Cell5, Cell6 and Cell8 (these are circled in Figure 4.10).
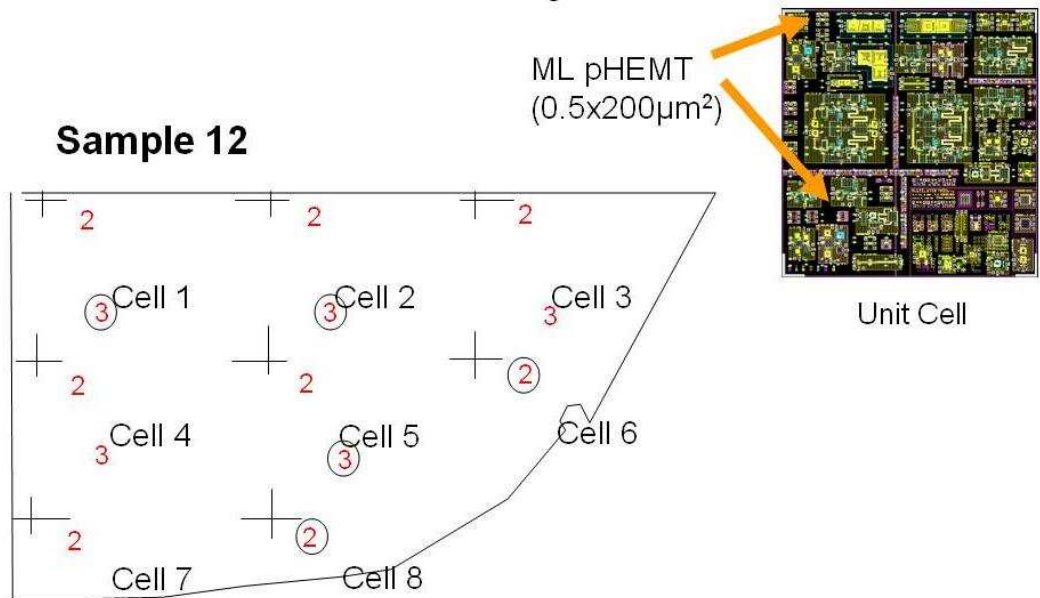
Figure 4.10 Locations of the five (circled) multilayer pHEMTs on sample 12 and the top view of the unit cell.

Figures 4.11 and 4.12 show the DC input and output characteristics of the five mentioned multilayer pHEMTs. It can be seen that, the uniformity of these post-processed pHEMTs are well preserved.
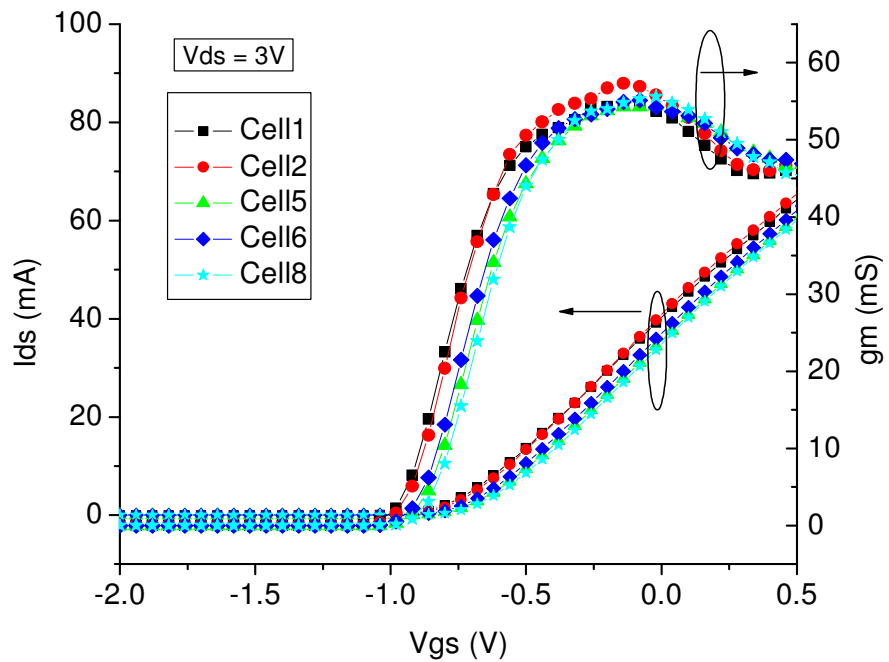
Figure 4.11 Measured transfer characteristics of the five multilayer pHEMTs (0.5x200 μm^2) on Sample 12.
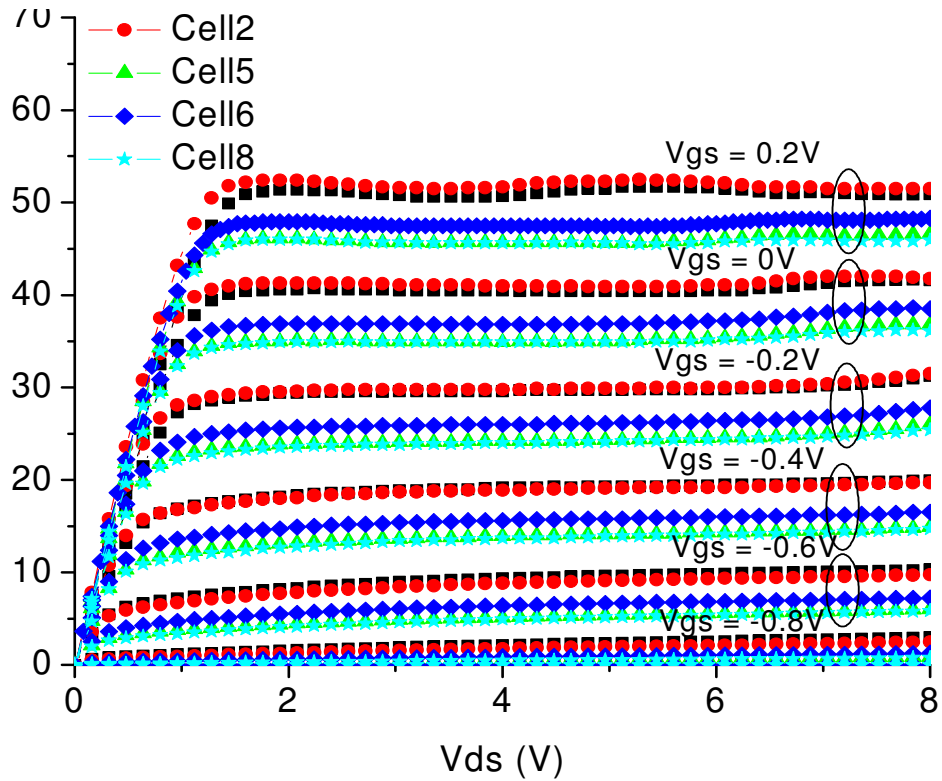
Figure 4.12 Measured output characteristics of the five multilayer pHEMTs (0.5x200 μm^2) on Sample 12.

Next, in order to look into the uniformity of these post-processed pHEMTs operating at high frequency, on-wafer S-parameters measurements are carried out from 45 MHz to 60 GHz using HP8510C Network Analyzer controlled by IC-CAP at biasing conditions of V_{gs} = -0.2 V and V_{ds} = 3 V. It is the same condition as applied for the virgin pHEMTs as shown in Figures 4.7-4.9. The measured S-parameters are shown in Figures 4.13 and 4.14, whereas, Figure 4.15 shows the current and power gains respectively in which cut-off frequency and maximum available gain frequency can be determined.
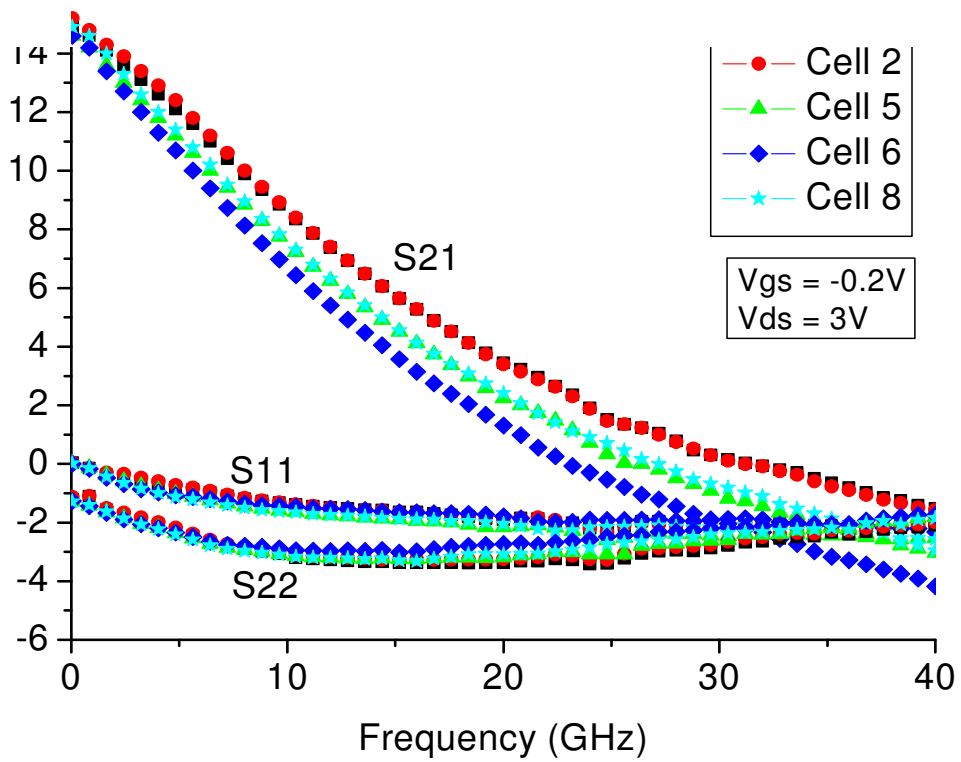
Figure 4.13 S11, S21 and S22 of the five multilayer pHEMTs (0.5x200 μm^2) on Sample 12.
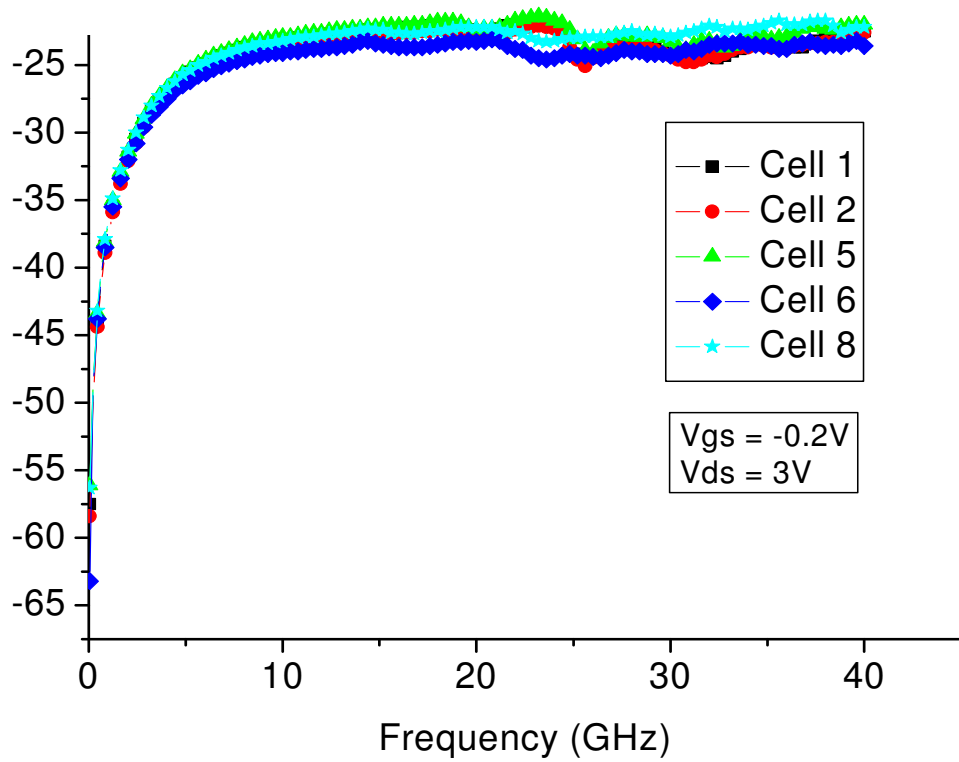
Figure 4.14 S12 of the five multilayer pHEMTs (0.5x200 μm^2) on Sample 12.
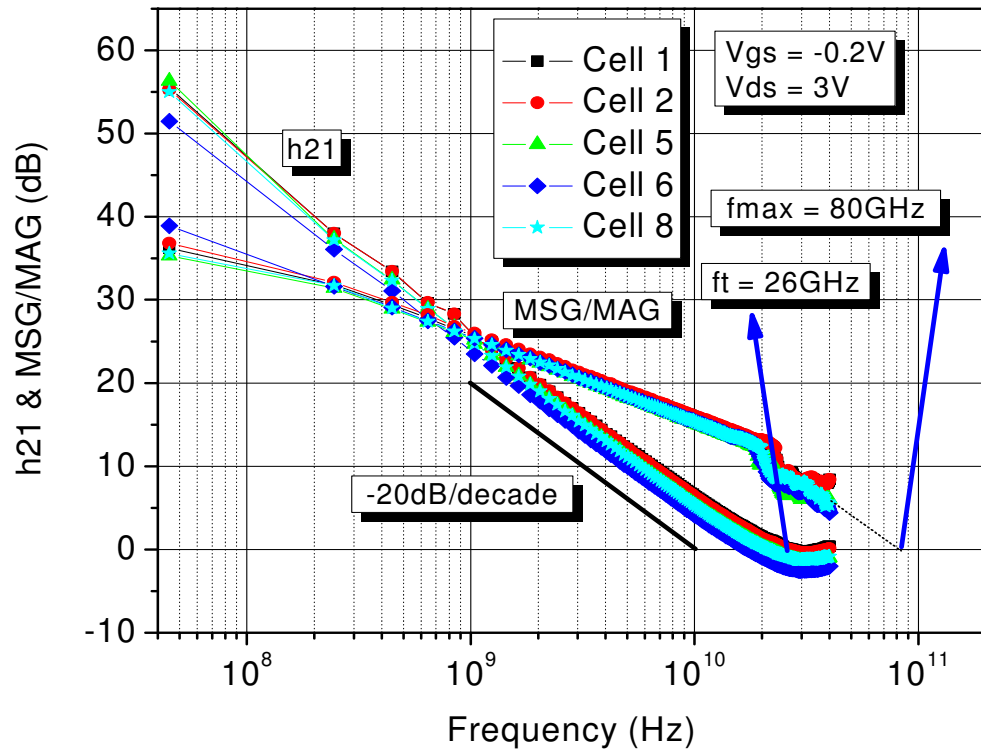
Figure 4.15 Current and power gains of the five multilayer pHEMTs (0.5x200 μm²) on Sample 12.

With these measured data, it can be concluded that, for the multilayer pHEMT, good agreements of the measurements confirm that the uniformity of the post-processed pHEMTs is observed. However, with close observation, it can be seen that Cell1 and Cell2 are having better performance compared to the other 3 multilayer pHEMTs. This could be attributed to the fact that the other 3 multilayer pHEMTs, Cell5, Cell6 and Cell8 are closer to the edge of the wafer, whereas Cell1 and Cell2 are more closer to the center part of the wafer.

4.3 Multilayer pHEMTs Modelling

In this section, multilayer-processed pHEMTs are characterised by first looking at the DC charecteristics. Comparison is made between the virgin and multilayer pHEMTs to study the effects of the multilayer processing. Following this, the small-signal parameters extraction is produced using a direct S-parameter measurement technique. This method has been created as an automated procedure with the aid of Agilent's IC-

CAP. The small-signal models for both virgin and multilayer pHEMTs are validated by comparing to the measurements.

4.3.1 DC Characterisation and Results

In order to investigate the effect of the processing, comparisons of the DC characteristics of the virgin and multilayer pHEMTs are shown in Figures 4.16 and 4.17. It should be noted that these results are taken as the average of the five pHEMTs, either virgin or multilayer, studied in the previous uniformity sections. It can be seen that although there are slight differences between the virgin and multilayer pHEMTs, for example the pinch-off voltage, and the maximum attainable g_m, they are still considered to be very much similar to each other. This is especially true, when the uniformity results shown in the previous section are taken in account. In other words, the disparity is well within the tolerance. More in-depth analysis between them will be made later when in sections dealing with the temperature study of pHEMTs.
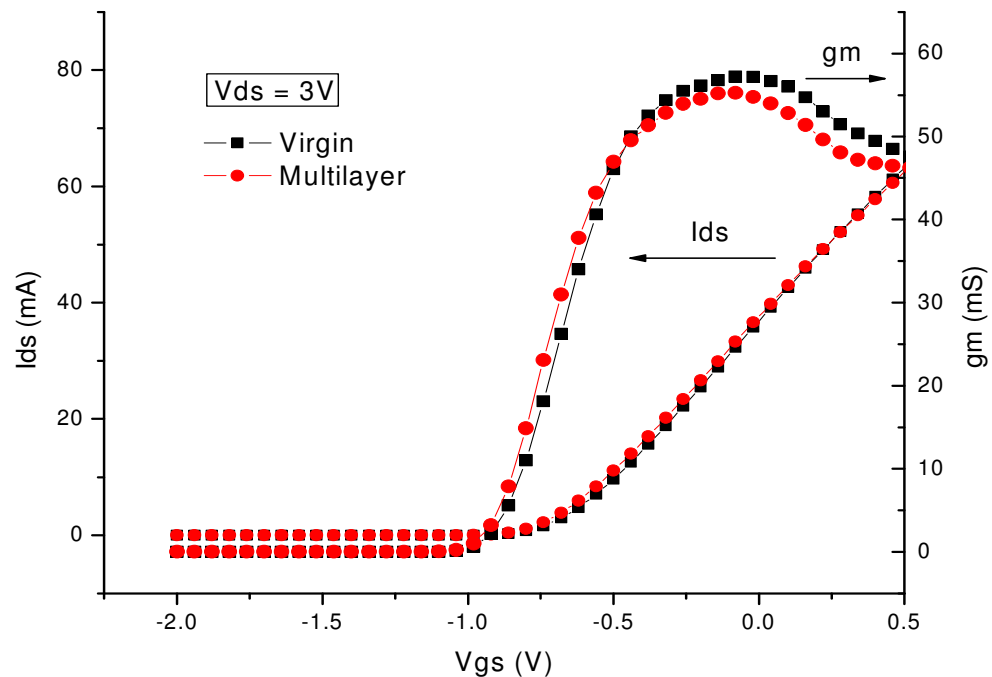
Figure 4.16 Comparison of measured Ids and gm characteristics between virgin and multilayer 0.5x200 μm^2 pHEMTs.
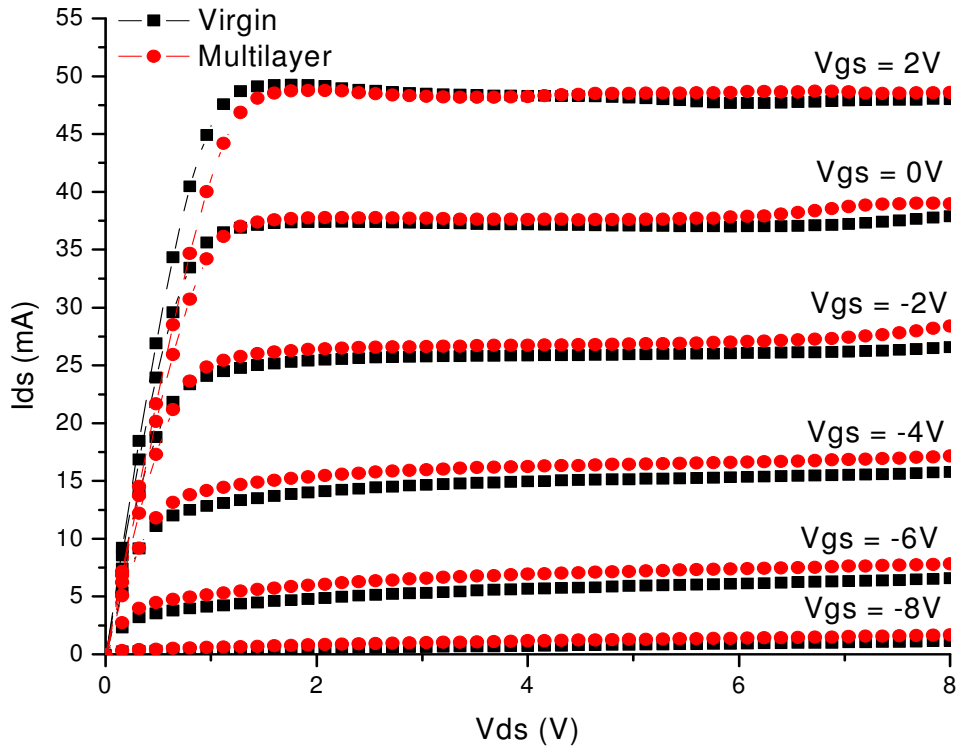
Figure 4.17 Comparison of output characteristics between virgin and multilayer 0.5x200 μm^2 pHEMTs.

From Figures 4.17 and 4.18, it can be observed that there is little difference between the virgin and multilayer pHEMTs. The minor differences noted here are actually smaller than those seen in uniformity sections. In other words, it can be concluded that multilayer processing does not introduce any significant degradation of performance of the pHEMTs.

4.3.2 RF Parameter Extraction

Small-signal equivalent circuit model parameters are vital for the characterizing and analyzing of device performance. It is useful in term of analyzing gain, noise, stability and other figures of merits when designing circuits. It is also part of the procedure of developing a large-signal model.

The development of a small-signal model is normally started off by first making DC and RF S-parameters measurements. The measurements data will then be used in a

procedure called parameter extraction. Various methods of small-signal parameter extraction have been reported and proposed [76]. Among them, direct parameter extraction has been made popular especially with the help of modern CAD simulators [60, 77].

In this section, the procedure of direct small-signal parameter extraction for a pHEMT is presented. DC and RF measurements at a few different biasing conditions are needed for the following presented technique. Cold or pinch-off bias is required in order to determine the extrinsic parameters. Agilent's Integrated Circuit Characterization and Analysis Program (IC-CAP) is then used to perform the extraction in which enable the analysis to be done on a single platform.

An equivalent circuit pi-model, like the one presented in the previous chapter in Figure 2.12, is first adopted as the small-signal model for the pHEMT. It is shown in Figure.4.18. Basically, the equivalent circuit can be seen as two different parts – the intrinsic and the extrinsic parts [60]:

1. The intrinsic elements g_m, g_d (R_{ds}), C_{gs}, C_{gd}, C_{ds}, R_i and τ which are bias dependent elements and hence are required to be extracted at hot biasing condition.

2. The extrinsic elements L_g, R_g, C_{pg}, L_s, R_s, R_d, C_{pd} and L_d which are independent of the biasing condition. These are extracted using off and cold bias conditions.
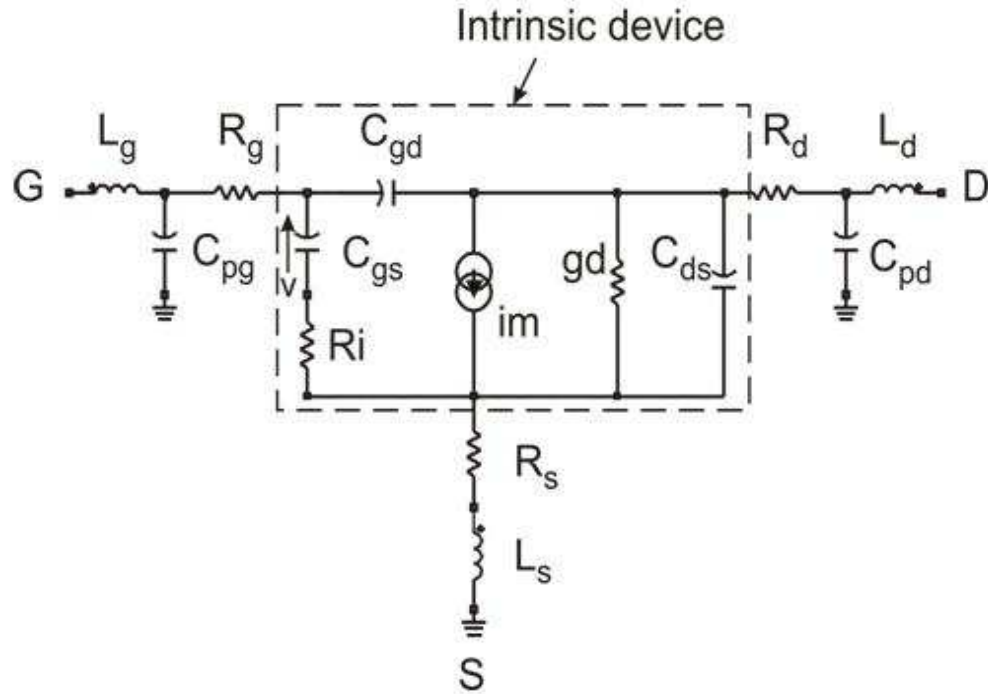
Figure 4.18 Π small-signal equivalent circuit model for pHEMT in common source configuration [60].

4.3.2.1 Cold Bias Extraction

The extraction process can thus be divided into two parts. Extrinsic parameters are determined first. Later, these extrinsic parameters will then be subtracted from the whole device model and, as a result, intrinsic parameters can be determined.

Two different operating conditions are needed to extract the extrinsic parameters:

1. OFF ($V_{DS} = 0$ and $V_{GS} = 0$)

2. STRONG PINCH-OFF ($V_{DS} = 0$ and V_{GS} much lower than pinch off voltage V_{PO}).

The following flow chart in Figure 4.19 shows the steps to be followed to extract the corresponding extrinsic values.
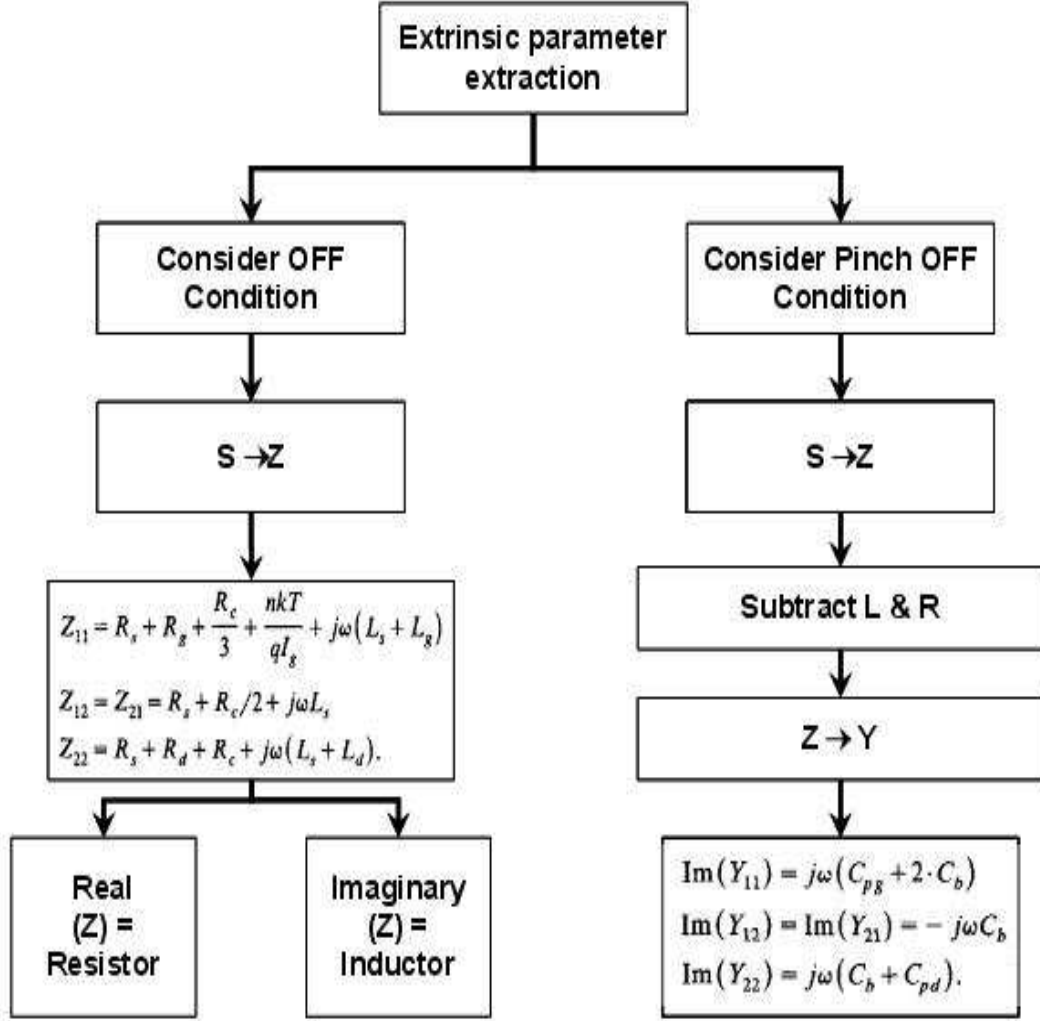
Figure 4.19 Flow chart for determining the extrinsic parameters of FETs[60].

To extract the extrinsic parasitic inductances and resistances in Figure 4.18, OFF state S-parameters measurements ($V_{DS} = 0$ and $V_{GS} = 0$) are taken using IC-CAP. These S-parameters are then converted to Z-parameters. The expressions for the Z-parameters at OFF state are given as [60]:

$$Z_{11} = R_S + R_g + 0.33R_{ch} + j\left[\omega\left(L_S + L_g\right) - \frac{1}{\omega C_g}\right] \tag{4.1}$$

$$Z_{12} = Z_{21} = R_S + 0.5R_{ch} + j\omega L_s \tag{4.2}$$

$$Z_{22} = R_d + R_S + R_{ch} + j\omega\left(L_S + L_d\right) \tag{4.3}$$

As can be seen, the parasitic inductances L_s, L_d and L_g can be computed by using the imaginary parts of the above equations:

From the equations (4.1)-(4.3),

→ **To extract L_s**

$$\text{Im}\,(Z_{12}) = j\omega L_s \tag{4.4}$$

$$L_s = \frac{\text{Im}(Z_{12})}{\omega} \tag{4.5}$$

→ **To extract L_d**

$$\text{Im}(Z_{22}) = j\omega(L_s + L_d) \tag{4.6}$$

$$L_d = \frac{\text{Im}\,(Z_{22})}{\omega} - L_s \tag{4.7}$$

→ **To extract L_g**

$$\text{Im}\,(Z_{11}) = j\omega(L_s + L_g) \tag{4.8}$$

$$L_g = \frac{\text{Im}\,(Z_{11})}{\omega} - L_s \tag{4.9}$$

Similarly, the resistances can be extracted from the real parts of equations (4.1)-(4.3). However, an additional expression is needed as there are four unknowns needing four equations. As a solution, under the heavy pinch-off condition ($V_{DS} = 0$ and V_{GS} much lower than pinch off voltage V_{PO}), the channel is completely off and the real part of Z_{11} is given as [60]:

$$\text{Re}\,[Z_{11(v_{po})}] = R_s + R_g \tag{4.10}$$

As a result, by looking at equations (4.1)-(4.3) and (4.10), the resistances can be extracted as follows:

→ **To extract R_{ch} (only R_{ch} is extracted using both Pinch off and OFF state)**

$$\text{Re}\,[Z_{11\,(V_{PO})}] = R_s + R_g \quad \text{@ pinch off} \tag{4.11}$$

$$\text{Re}\,[Z_{11}] = R_s + R_g + 0.33R_{ch} \quad \text{@ OFF state} \tag{4.12}$$

$$R_{ch} = 3 \times \left\{ \text{Re}\left[Z_{11} \right] - \text{Re}\left[Z_{11(V_{PO})} \right] \right\} \tag{4.13}$$

→ **To extract R_s**

$$\text{Re}\,[Z_{12}] = 0.5\,R_{ch} + R_s \tag{4.14}$$

$$R_s = \text{Re}\,[Z_{12}] - 0.5R_{ch} \tag{4.15}$$

→ **To extract R_g**

$$R_g = \mathrm{Re}\,[Z_{11}] - R_s - 0.5R_{ch} \tag{4.16}$$

→ **To extract R_d**

$$R_d = \mathrm{Re}\left[Z_{22}\right] - R_s - R_{ch} \tag{4.17}$$

From the equivalent circuit model in Figure 4.18, there are two parasitic capacitances that are required to be extracted, C_{pg} and $C_{pd,}$ which are the pad capacitances formed on the gate and drain side respectively. For this extraction again the cold or pinch-off bias condition is used. The S-parameters measured at this condition are converted to the respective Z-parameters and then, according to the topology of the equivalent circuit model, the inductances and the resistances computed in the previous section are subtracted to eliminate their effect:

$$Z_{11} - R_S - R_g - j\omega\left(L_S + L_g\right) \tag{4.18}$$

$$Z_{12} - R_S - j\omega L_s = Z_{21} - R_S - j\omega L_s \tag{4.19}$$

$$Z_{22} - R_d - R_S - j\omega\left(L_S + L_d\right) \tag{4.20}$$

After that, the resultant Z parameters are transformed to the respective Y- parameters. The capacitances can then be extracted and are given as:

$$Y_{11} = j\omega(2C_b + C_{pg}) \tag{4.21}$$

$$Y_{12} = Y_{21} = j\omega C_b \tag{4.22}$$

$$Y_{22} = j\omega(C_b + C_{pd}) \tag{4.23}$$

Where, C_b is the fringing capacitance due to depleted layer extension at each side of the gate/residual capacitance [60].

Using equations (4.21)-(4.23) the pad parasitic capacitances can be extracted as follows:

→ **To extract C_b**

$$C_b = \mathrm{Im}(Y_{12}) \tag{4.24}$$

→ **To extract C_{pg}**

$$\mathrm{Im}(Y_{11}) = jw(2C_b + C_{pg}) \tag{4.25}$$

$$C_{pg} = \frac{\mathrm{Im}(Y_{11})}{\omega} - 2C_b \tag{4.26}$$

→ **To extract C_{pg}**

$$\mathrm{Im}(Y_{22}) = j\omega(C_b + C_{pd}) \tag{4.27}$$

$$C_{pd} = \frac{\text{Im}(Y_{22})}{\omega} - C_b \qquad (4.28)$$

With all the extrinsic parameters extracted, the intrinsic bias dependent parameters can now be extracted and determined.

4.3.2.2 Hot Bias Extraction

The intrinsic elements g_m, g_d, C_{gs}, C_{gd}, C_{ds}, R_i and τ are bias dependent elements and hence required to be extracted at non-zero biasing conditions. The flowchart of the extraction of the intrinsic parameters is presented in Figure 4.20.
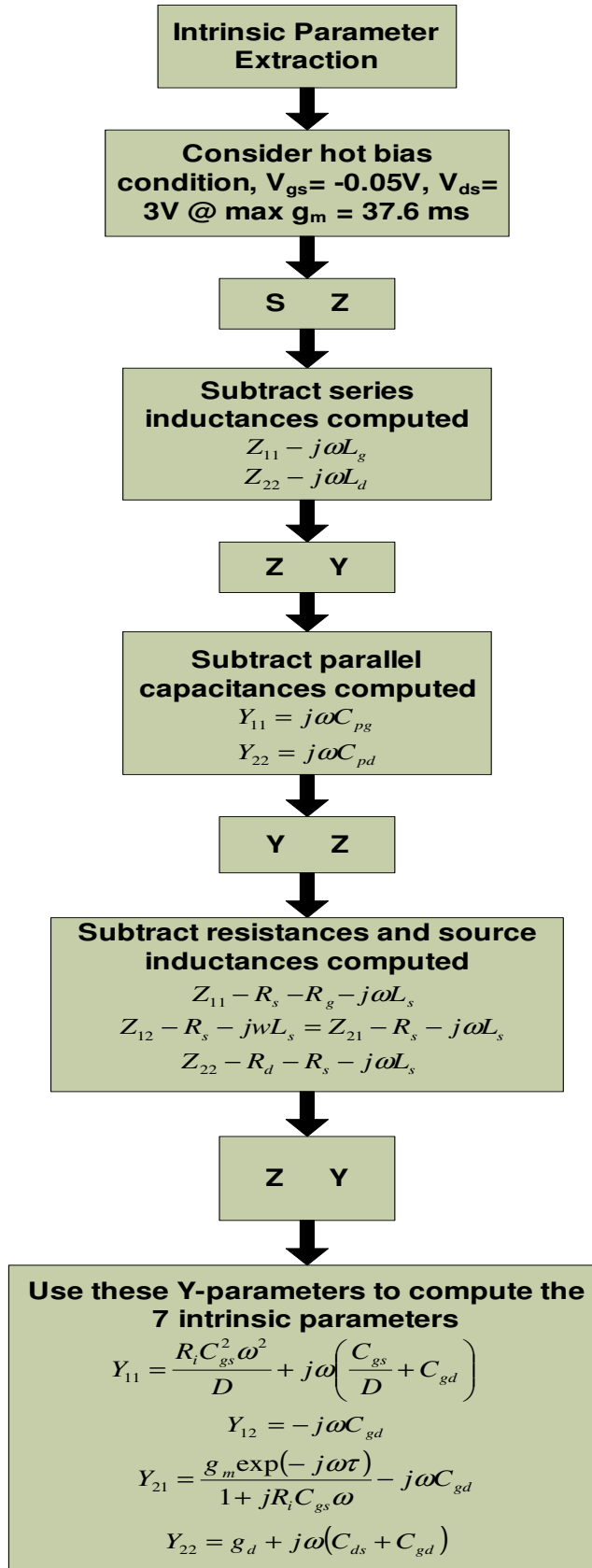
Figure 4.20 Flow chart for determining the intrinsic parameters of FETs [60].

As shown in Figure 4.20, to determine the intrinsic parameters, firstly the computed extrinsic parameters are to be deembedded. This is carried out by using the following procedure:

1. Transform the S-parameters of the chosen bias point into Z-parameters. From the obtained Z-parameters, the gate and the drain parasitic series inductances computed from previous extrinsic extractions are subtracted.

$$Z_{11} - j\omega L_g \qquad\qquad (4.29)$$
$$Z_{22} - j\omega L_d \qquad\qquad (4.30)$$

2. The resulting Z-parameters are then converted to Y parameters and then the effects of the two parasitic capacitances are eliminated.

$$Y_{11} - j\omega C_{pg} \qquad\qquad (4.31)$$
$$Y_{22} - j\omega C_{pd} \qquad\qquad (4.32)$$

3. For the final step of deembedding the extrinsic parameters, the Y-parameters are converted back to Z-parameters and the series resistances and source inductance are subtracted.

$$Z_{11} - R_s - R_g - j\omega L_s \qquad\qquad (4.33)$$
$$Z_{12} - R_s - j\omega L_s = Z_{21} - R_s - j\omega L_s \qquad\qquad (4.34)$$
$$Z_{22} - R_d - R_s - j\omega L_s \qquad\qquad (4.35)$$

4. The Z-parameters obtained are then converted back into Y-parameters which are now ready for the intrinsic parameter extraction. The following equations are used to determine the intrinsic parameters:

$$C_{gd} = -\frac{\mathrm{Im}(Y_{12})}{\omega} \qquad\qquad (4.36)$$

$$C_{gs} = \frac{[\mathrm{Im}(Y_{11}) - \omega C_{gd}]}{\omega}\left[1 + \frac{\mathrm{Re}^2(Y_{11})}{[\mathrm{Im}(Y_{11}) - \omega C_{gd}]^2}\right] \qquad\qquad (4.37)$$

$$g_{ds} = \mathrm{Re}(Y_{22}) \qquad\qquad (4.38)$$

$$C_{ds} = \frac{\text{Im}(Y_{22}) - \omega C_{gd}}{\omega} \qquad (4.39)$$

$$R_i = \frac{\text{Re}(Y_{11})}{\text{Re}^2(Y_{11}) + [\text{Im}(Y_{11}) - \omega C_{gd}]^2} \qquad (4.40)$$

$$\tau = \frac{1}{\omega} arcsin\left[\frac{-\text{Im}(Y_{21}) - \omega C_{gd} - \omega C_{gs} R_i \text{Re}(Y_{21})}{g_m}\right] \qquad (4.41)$$

$$g_m = \left[\left[\text{Im}(Y_{21}) + \omega C_{gd}\right]^2 + \text{Re}^2(Y_{21})\right]^{\frac{1}{2}} \left(1 + \omega^2 R_i^2 C_{gs}^2\right)^{\frac{1}{2}} \qquad (4.42)$$

4.3.3 RF Small-Signal Characterisation

The RF S-parameters measurements results are shown in Figures 4.21 and 4.22. Comparison between the virgin and multilayer pHEMTs can also be seen in these figures. Just like the results seen in section 4.3.1, these results are again the average of the five pHEMTs, either virgin or multilayer, studied in the uniformity section 4.2.
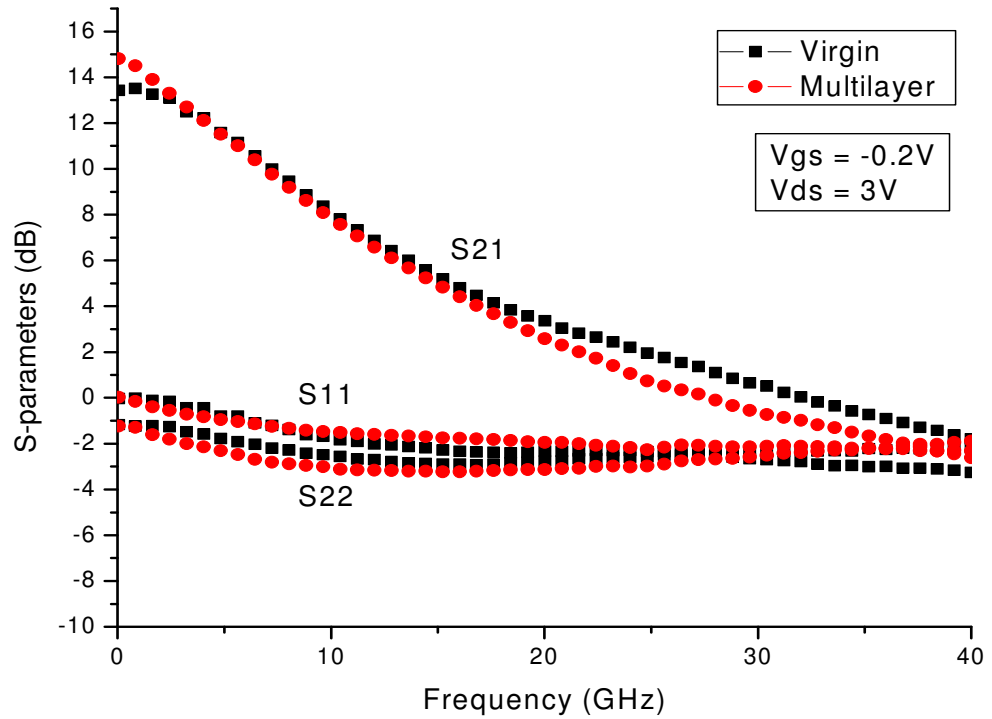
Figure 4.21 Comparison of S11, S21 and S22 between virgin and multilayer 0.5x200 µm² pHEMTs.
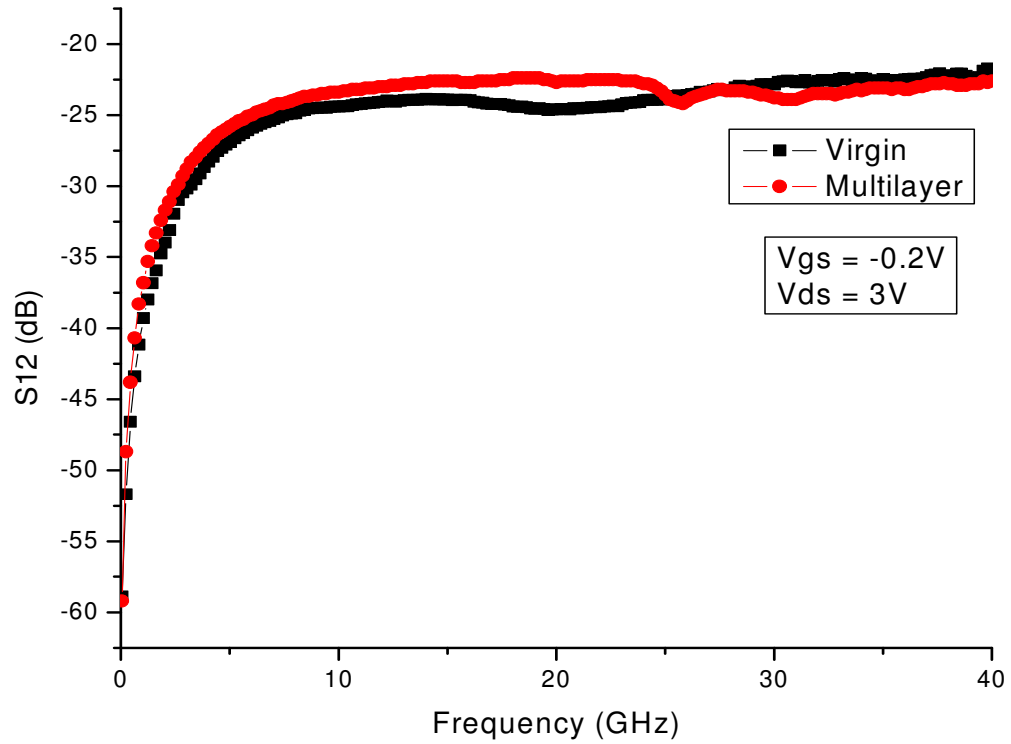
Figure 4.22 Comparison of S12 between virgin and multilayer 0.5x200 µm^2 pHEMTs.
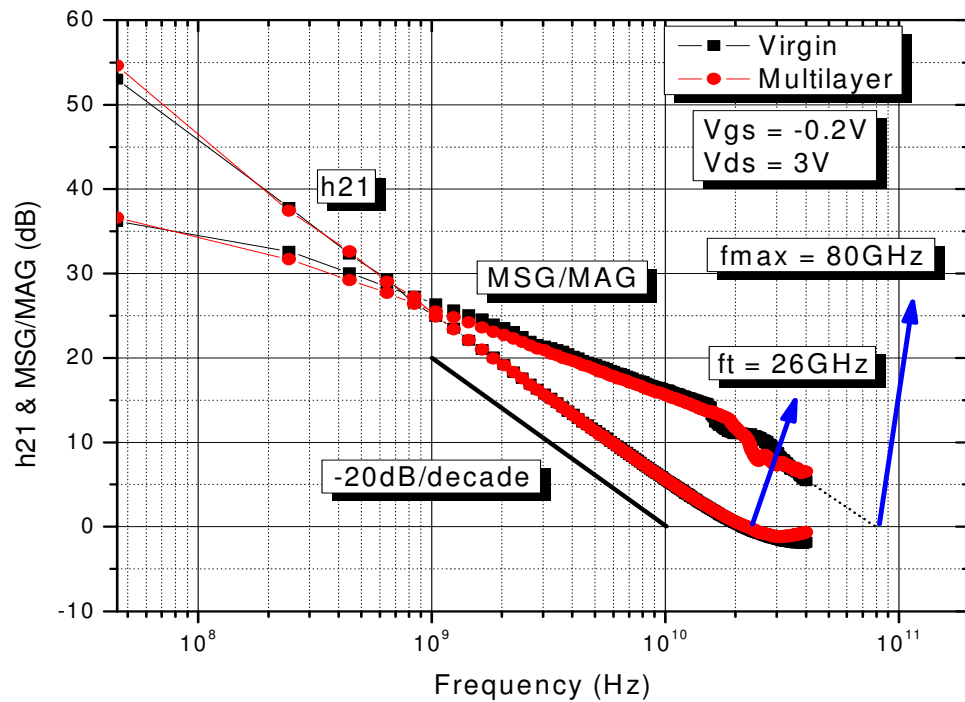
Figure 4.23 Comparison of current and power gains between virgin and multilayer 0.5x200 µm^2 pHEMTs.

Figure 4.23 gives the current gain, h21, and the maximum available gain (MAG) of the virgin and multilayer pHEMTs. From this figure, the cut-off frequency can be found by locating the point at which the 20 dB/decade slope of h21 line intersects the 0 dB (current gain = unity). The f_T is found to be about 26 GHz. On the other hand, the maximum oscillation frequency, f_{max}, can be found at the intersection of the MAG and the 0 dB lines where in Figure 4.23, f_{max} is found, after extrapolation, to be about 80 GHz.

From Figures 4.16, 4.17 and 4.21 to 4.23, it can be seen, that the raw measurements for both DC and RF, that the differences between the virgin and multilayer pHEMT is very small suggesting the multilayer fabrication processing affects little of the pHEMT performance. Intuitively, the processing should only introduce additional parasitic resistances, inductances and capacitances. Even these additional parasitics are kept at minimum as shown in the above-mentioned data.

4.3.3.1 Small-Signal Model of Virgin pHEMTs

Using the methodology of developing a small-signal model of pHEMT presented in previous section, a small-signal model is established for the virgin pHEMT. A bias point of drain voltage V_{ds} = 3 V and gate voltage V_{gs} = -0.2 V have been chosen to achieve the maximum transconductance, g_m, as shown in Figure 4.16. The extracted small-signal parameters values are tabulated in Table 4.1.

Table 4.1 Extracted small-signal parameter for the virgin 0.5x200 μm^2 pHEMT

Parameter @ V_{gs} = -0.2 V & V_{ds} = 3V	Value	Description
C_{pg} (fF)	53	Parasitic gate capacitance
C_{pd} (fF)	35	Parasitic drain capacitance
L_s (pH)	3.8	Source inductance
L_d (pH)	78	Drain inductance
L_g (pH)	151	Gate inductance
R_s (Ω)	3.7	Source resistance
R_d (Ω)	6.7	Drain resistance
R_g (Ω)	1.2	Gate resistance
C_{gd} (fF)	17.3	Gate-drain capacitance
C_{ds} (fF)	67.8	Drain-source capacitance
C_{gs} (fF)	368	Gate-source capacitance
R_{ds} (Ω)	608	Output resistance
R_i (Ω)	1.4	Input resistance
g_m (mS)	64	Intrinsic transconductance
τ (ps)	3.0	Signal delay

In order to investigate the validity of the developed small-signal model for the virgin pHEMT, comparisons between the simulated and measured S-parameters are made as shown in Figures 4.24 and 4.25. Comparisons of current gain, h21, and maximum available gain are also made in Figure 4.26.

Figure 4.24 Comparison of measured and modelled S11, S21 and S22 (virgin 0.5x200 µm² pHEMT).
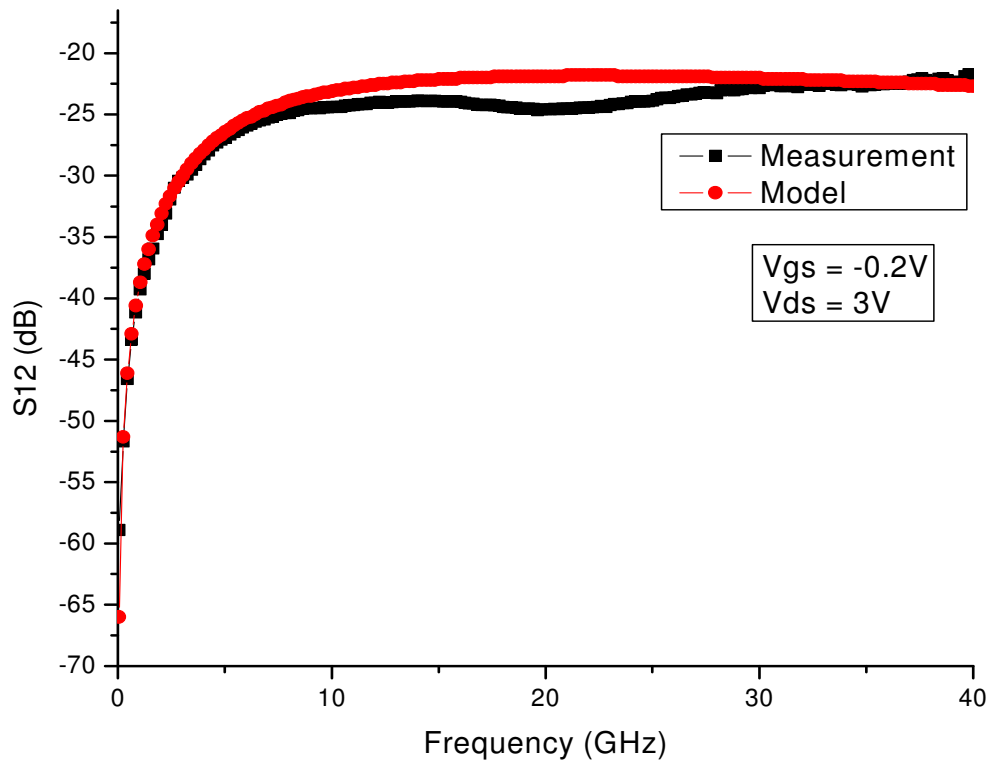
Figure 4.25 Comparison of measured and modelled S12 (virgin 0.5x200 µm² pHEMT).
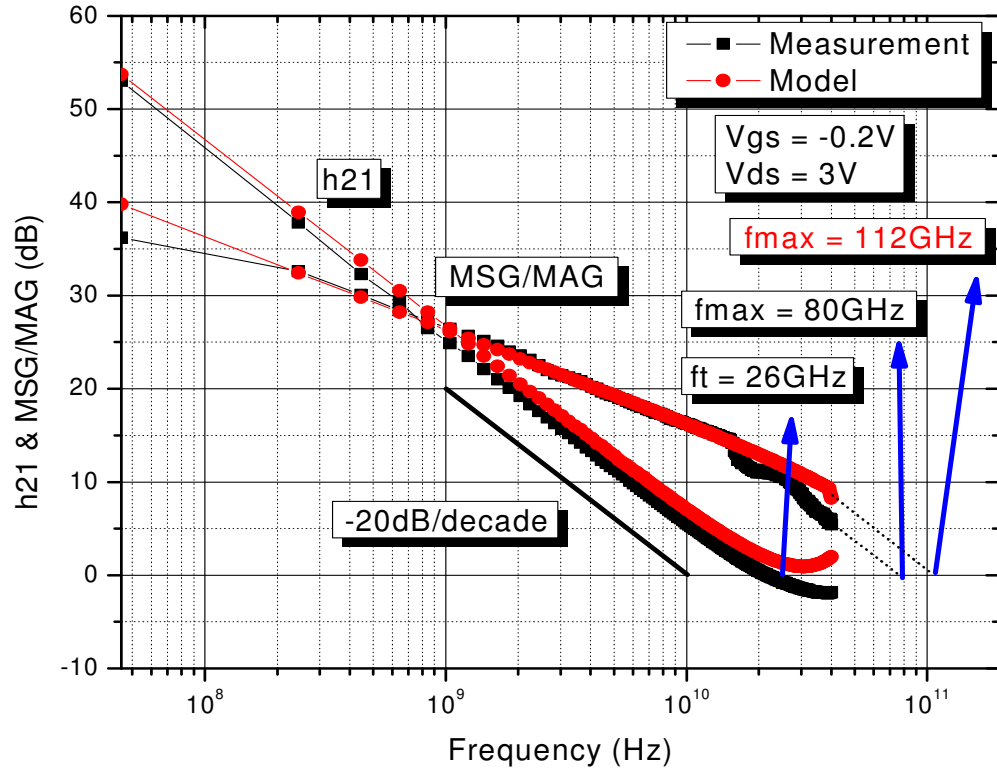
Figure 4.26 Comparisons of measured and modelled current and power gains (virgin 0.5x200 μm^2 pHEMT).

Observation of the previous data and the comparisons suggest that the developed small-signal model of the virgin pHEMT is accurate enough to represent the actual device. The extraction technique is proved to be successful in determining the small-signal parameters values.

For the Figure 4.26, the cut-off frequency, f_T, and the maximum oscillation frequency, f_{max}, can be found by locating the points at which the 20 dB/decade slope of lines intersects the 0 dB. From Figure 4.26, f_T is found to be about 26 GHz where f_{max} is found to be, after extrapolation, about 112 GHz for the model.

These figures of merits can be calculated by given formulas as well. The f_T is given as [1]:

$$f_t = \frac{g_m}{2\pi\left(C_{gs} + C_{gd}\right)} \tag{4.43}$$

From the extracted parameters of the Table 4.1,

g_m = 64 mS

C_{gs} = 368 fF

C_{gd} = 17.3 fF

Substituting this in equation (4.43),

f_T = 26.4 GHz

The MAG is given as [1]:

$$MAG = 10 \times \log \frac{|S_{21}|}{|S_{12}|} + 10 \times \log \left| K \pm \sqrt{K^2 - 1} \right| \qquad (4.44)$$

where

$$K = \frac{1 + |D_s|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{21}||S_{12}|} \qquad (4.45)$$

$$D_s = S_{11}S_{22} - S_{12}S_{21} \qquad (4.46)$$

The analytical formula for f_{max} is given as [1]:

$$f_{max} = \frac{f_t}{2\sqrt{r_1 + f_t \tau}} \qquad (4.47)$$

where

$$r_1 = \frac{R_g + R_i + R_s}{R_{ds}} \qquad (4.48)$$

$$\tau = 2\pi R_g C_{gd} \qquad (4.49)$$

From the extracted parameters in Table 4.1,

$R_g = 3.7\ \Omega$

$R_i = 1.42\ \Omega$

$R_s = 3.8\ \Omega$

$R_{ds} = 740\ \Omega$

$C_{gd} = 20.3\ \text{fF}$

$f_T = 26.4\ \text{GHz}$

And therefore,

$f_{max} = 112.3\ \text{GHz}$

The calculated f_t and f_{max} is almost identical to the modelled ones found from Figure 4.26 (calculated f_t and f_{max}: 26.4 GHz and 112.3 GHz; modelled f_t and f_{max}: 26 GHz and 112 GHz). There is a discrepancy of the f_{max} between modelled and measured results (modelled: 112 GHz; measured: 80 GHz). This can be explained from the same reasoning that the equivalent circuit model adopted is a basic first order model. The compactness of the model is the main attractiveness of the model. The disadvantage as observed is that it is not as effective at modelling higher frequency behaviour. Apart from that, it can be said that the model is a very accurate representation of the actual device upto the f_t of 26 GHz.

4.3.3.2 Small-Signal Model of Multilayer pHEMTs

Using the same technique as in the previous section, a small-signal model for the multilayer pHEMT has also been developed. Again in order to get maximum g_m, bias point of drain voltage $V_{ds} = 3$ V and gate voltage $V_{gs} = -0.2$ V has been chosen. Following that, RF S-parameters measurement is made at this particular bias point. Direct parameter extraction routine, as discussed in previous section, can thus be made

from the measured S-parameters. The extracted small-signal parameters values are presented in Table 4.2.

Table 4.2 Extracted small-signal parameters for the multilayer 0.5x200 μm² pHEMT

Parameter @ V_{gs} = -0.2 V & V_{ds} = 3V	Value	Description
C_{pg} (fF)	56	Parasitic gate capacitance
C_{pd} (fF)	56	Parasitic drain capacitance
L_s (pH)	1.2	Source inductance
L_d (pH)	72	Drain inductance
L_g (pH)	139	Gate inductance
R_s (Ω)	3.3	Source resistance
R_d (Ω)	9.1	Drain resistance
R_g (Ω)	1.0	Gate resistance
C_{gd} (fF)	20.6	Gate-drain capacitance
C_{ds} (fF)	103	Drain-source capacitance
C_{gs} (fF)	381	Gate-source capacitance
R_{ds} (Ω)	476	Output resistance
R_i (Ω)	1.5	Input resistance
g_m (mS)	74	Intrinsic transconductance
τ (ps)	1.0	Signal delay

With these parameters extracted, by putting them in the small-signal circuit model as shown in Figure 4.18 in ADS, simulation is made and then compared to the measurement data. The S-parameters comparisons are presented in Figures 4.27 and 4.28.
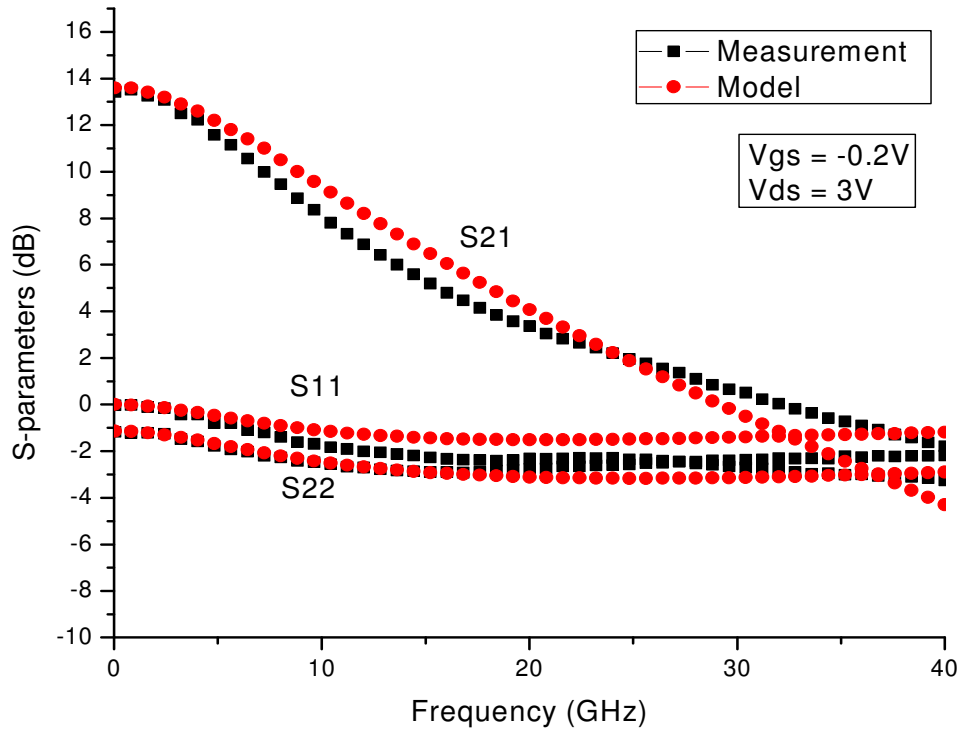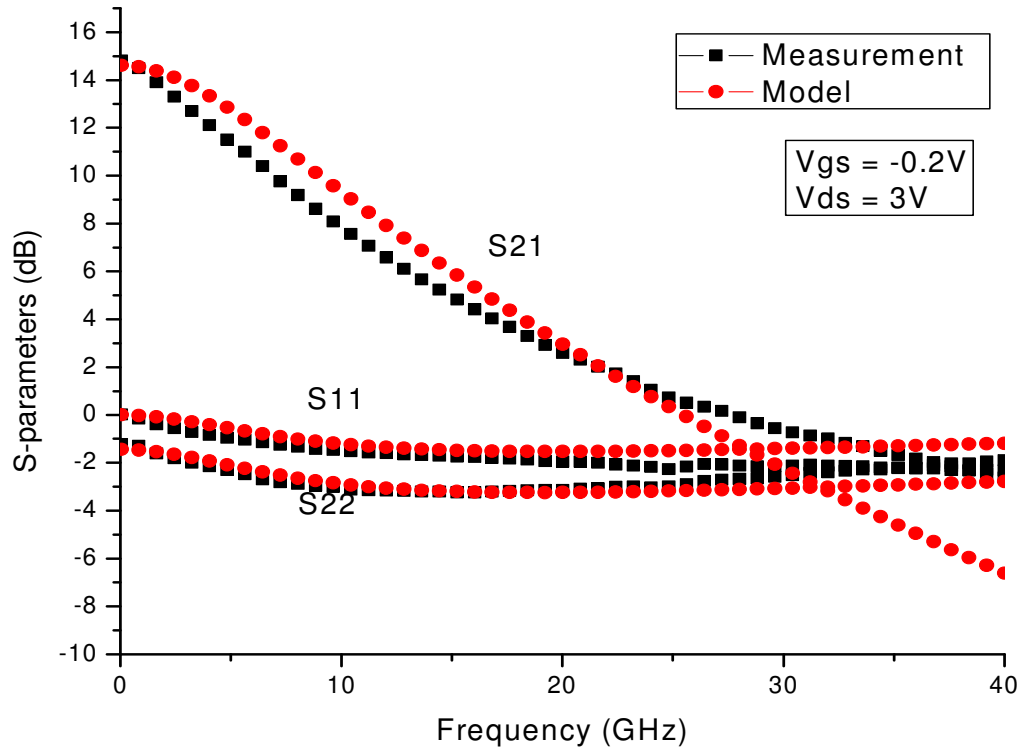
Figure 4.27 Comparison of measured and modelled S11, S21 and S22 (multilayer 0.5x200 μm^2 pHEMT).
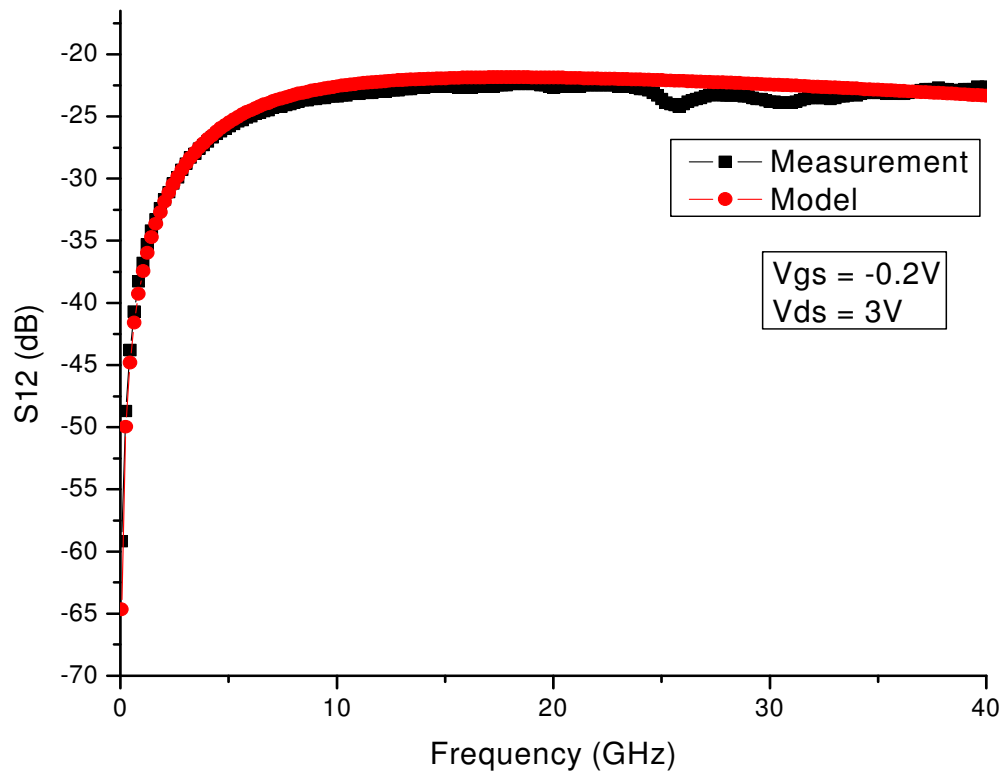
Figure 4.28 Comparison measured and modelled of S12 (multilayer 0.5x200 μm^2 pHEMT).
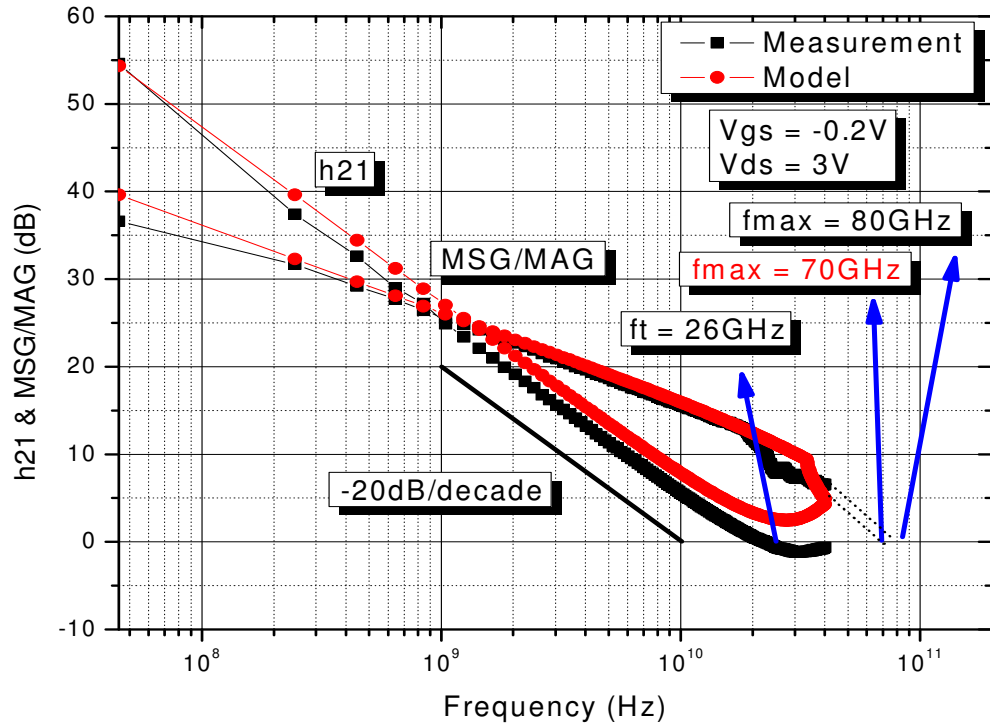
Figure 4.29 Comparisons of measured and modelled current and power gains (multilayer 0.5x200 μm² pHEMT).

As can be seen, from Figures 4.27, 4.28 and 4.29, the simulated results from the small-signal model and the measurements data have very good agreements for the multilayer pHEMTs. Therefore, the presented methodology of finding a small-signal model including the direct parameters extraction technique is well validated. It should be noted that the established methodology can be extended to every operating bias point which will become useful for establishing large-signal model.

In Figure 4.29, the cut-off frequency, f_T, can be found at the point when the current gain, h21, equals to zero. The f_T is found to be close to 26 GHz. This can be verified by using the given analytical formula in equation (4.43).

From the extracted parameters of the Table 4.2,

g_m = 74 mS

C_{gs} = 381 fF

C_{gd} = 20.6 fF

Substituting this in equation (4.43),

f_T = 29.3 GHz

It should be noted that the small-signal model presented here is a first order model, of which the validity cannot be extended throughout the whole frequency range, especially beyond 20 GHz. Alternative higher order model might be needed. However, the model presented here proves to be accurate enough for normal applications and is particularly useful and fast for developing large-signal model.

Similarly, in Figure 4.29, the maximum oscillation frequency, f_{max}, can be found by plotting the maximum available gain, MAG. It can be seen that, the f_{max} can be found at about 70 GHz for the model. Again, analytical formula can also be used to determine the f_{max} using the extracted parameters values. It is given in equations (4.44) to (4.49).

From the extracted parameters in Table 4.2,

R_g = 1.0 Ω

R_i = 1.5 Ω

R_s = 3.3 Ω

R_{ds} = 476 Ω

C_{gd} = 20.6 fF

f_T = 29.3 GHz

And therefore,

f_{max} = 115.9 GHz

Comparing the calculated f_t and f_{max} to the measured ones found from Figure 4.29 (calculated f_t and f_{max}: 29.3 GHz and 115.9 GHz; modelled f_t and f_{max}: 26 GHz and 70 GHz), about 11.3% and 39% of differences of f_t and f_{max} could be found. The f_t is within for most of the applications where tolerance of about 10% could be accepted. On the other hand there is a huge difference between the calculated and modelled f_{max} in Figure 4.29. Also, the actual measured f_{max} is found to be about 80 GHz. All of these discrepancies could be attributed to the fact that the adopted model is a first order crude model which is not as effective as representing high frequency (beyond 20 GHz) behaviour of the transistor. In addition, the measurement equipment was only calibrated and capable of accurate measurements up to 40 GHz, effectiveness of capturing higher frequency behaviours degrade significantly beyond the 40GHz upper limit. However, it should be noted as the f_t is about 26 GHz, the device would almost only be designed below this cut-off frequency, and up to 26 GHz, the above presented small-signal model is still a very good and accurate representation of the actual device.

4.4 DC Temperature Dependent Multilayer pHEMTs Modelling

Temperature dependence study is a vital part of the complete characterization on active devices. It is especially important if the active devices are to be designed for high power applications where enormous heat could be generated during the operatin of the chip. The work here involves studying the temperature dependence of AlGaAs/InGaAs/GaAs pHEMTs in multilayer CPW MMIC. Although previous studies on temperature dependence of AlGaAs/InGaAs/GaAs pHEMTs have been reported [78-81], this is the first time that the AlGaAs/InGaAs/GaAs pHEMTs in multilayer CPW MMIC have been presented since the multilayer technology is a novel configuration and have not been investigated in the past.

4.4.1 Thermal Effects

It is a common practice to study thermal effects of active devices at high temperature involving complicated phenomenon in the intrinsic part of the device, especially under

the gate and drain region. Hot-electrons and impact ionization are two of the most dominant effects which are reported [78-81]. Depending on the bias point and temperature, their effects can be extremely strong or moderate compared to other effects like scattering and mobility reduction. In order to achieve high-frequency applications, increasing short gate length has been designed and this results in electric field soaring to very high values for relatively low drain bias. At the same time, in order to get high output power, the device must be biased at high field region. Therefore, it is very normal for these high field phenomenons affecting the performance of the device. On the other hand, pHEMTs which achieve better performance by having better confinement of carriers in the pseudomorphic channel favours the impact ionization due to the narrow bandgap material used for the channel. Figure 4.30 shows the high field phenomenon in an AlGaAs pHEMT [78].

When impact ionization happens in the channel layer, a lattice atom will give out a pair of electron and hole. The electron could achieve sufficient energy to become a carrier contributing to the overall current. Meanwhile, the hole could overcome the band discontinuity and go into the donor AlGaAs layer. It could be collected by the gate electrode and produce gate current or it could get trapped in one of the interface or surface states causing a degradation in transconductance (g_m), drain current (I_d), and pinch-off voltage (V_p) [81].
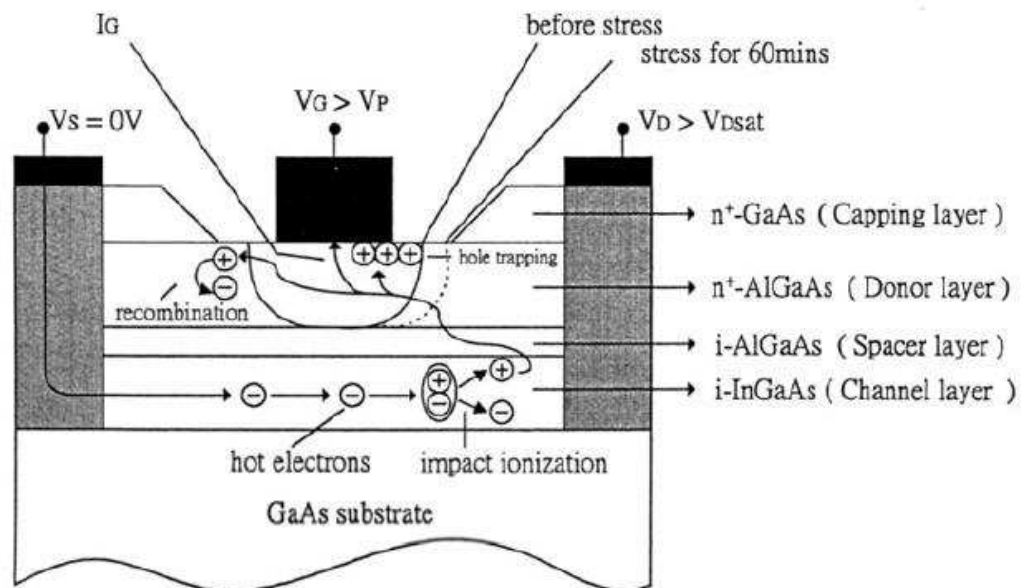
Figure 4.30 Hot electrons and impact ionization effects [78].

4.4.2 Results and Discussion

Before examining the temperature effects on the virgin and multilayer pHEMTs, it is useful to note the comparisons of DC characteristics at room temperature as shown in Figures 4.31 and 4.32. It can be observed that although some differences can be observed, they are mainly confined in the lower V_{gs} region, closer to the pinch-off. At higher biases of V_{gs} and V_{ds}, the differences are rather small. These differences can be attributed to the uniformity of the fabrication, and are considered to be well within the tolerance.
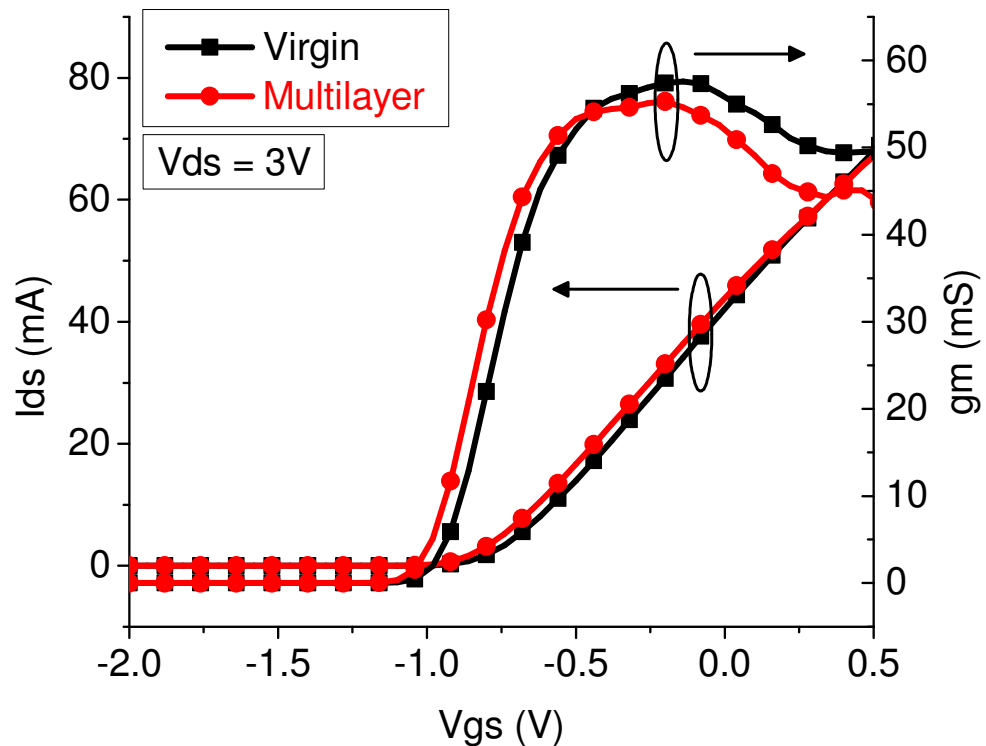
Figure 4.31 Comparisons of measured transfer characteristics and transconductances of virgin and multilayer pHEMTs at room temperature.
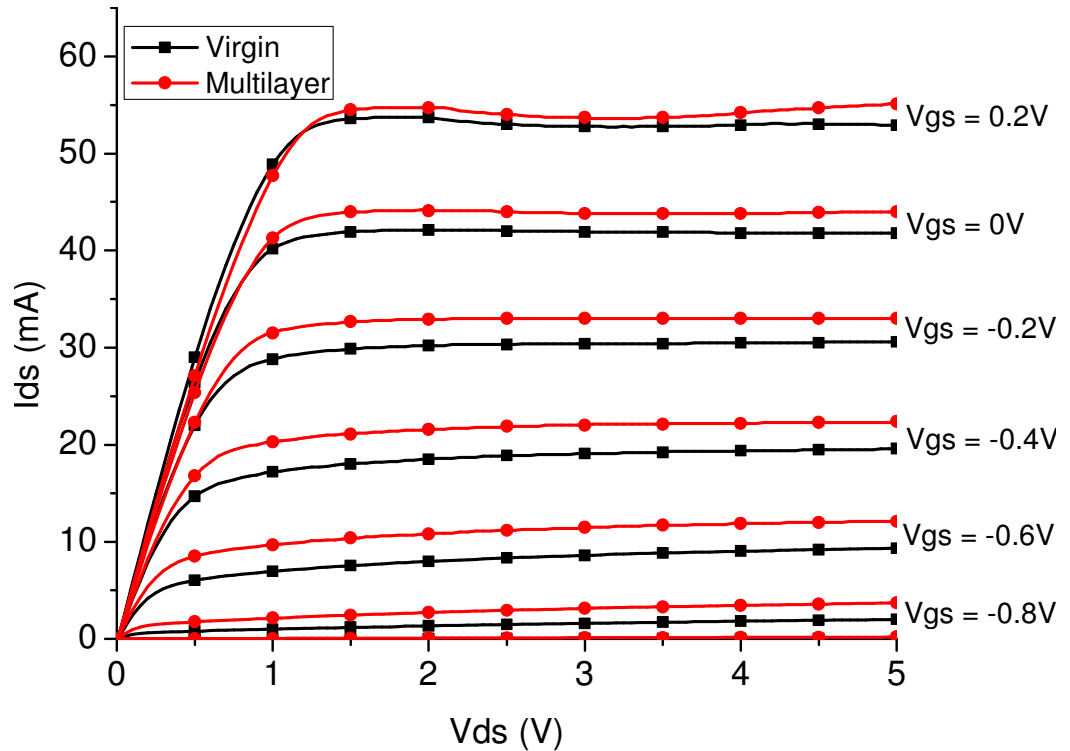
**Figure 4.32 Comparisons of measured output characteristics of virgin and multilayer 0.5x200 μm²
pHEMTs at room temperature.**

In order to study the effects of temperature on the performance of pHETMs, both
pHEMTs (virgin and multilyer) charachterisitcs were measured at 7 different
temperatures, -25, 0, 25, 40, 55, 70 and 125°C. The input characteristic of virgin
pHEMTs is presented in Figure 4.33. Degradation of the output current, I_{ds}, can be
observed as the temperature increases. This is due to the fact that, at high temperature,
carrier mobility is reduced due to increased scattering effect of the carriers. However, on
the other hand, at lower V_{gs}, higher current can be seen at higher temperature, this is due
to the fact that mobility reduction and scattering effect are high field phenomenon,
whereas, at lower field, the pinch-off voltage shift/reduction is more prominent. The
pinch-off voltage shift is due to the higher carrier concentration resulting earlier channel
opening at high temperature. It should be noted that this effect will be offset and
overwhelmed by the reduction of carrier mobility and more scattering effect at higher
V_{gs} (high field region). The same trend is also observed for the multilayer pHEMTs
except that greater variation is seen and will be shown later.
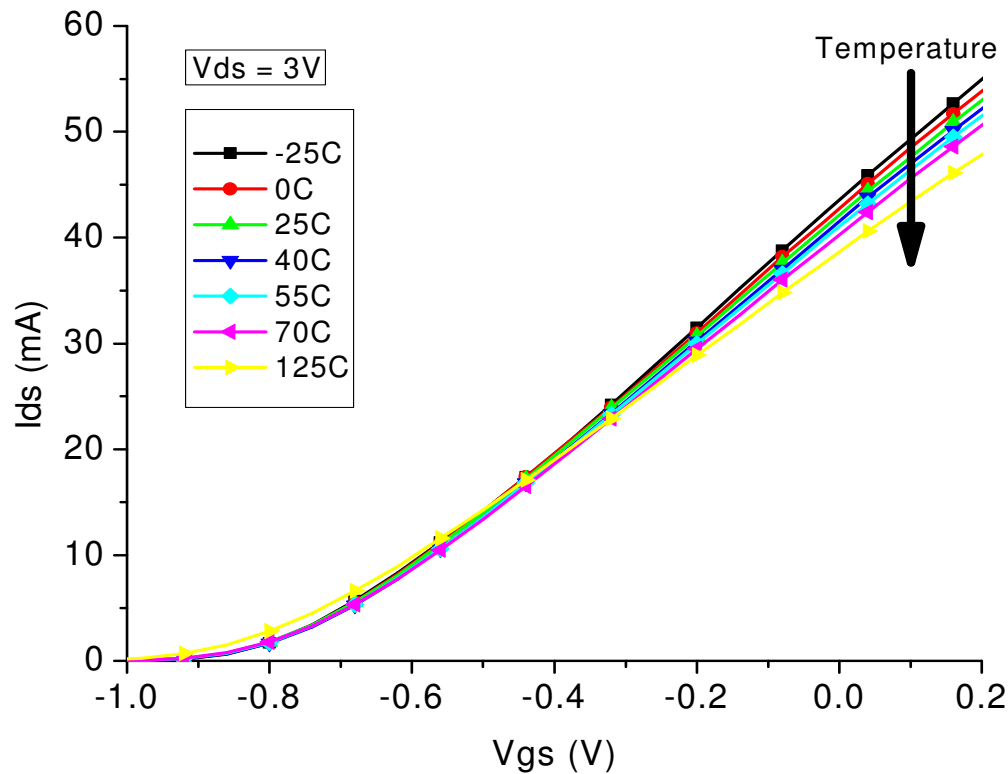
Figure 4.33 Temperature dependent transfer characteristics of the virgin 0.5x200 µm² pHEMTs (V_ds = 3V).

Temperature dependent output characteristics of the virgin pHEMT is presented in Figure 4.34. Degradation of output current can again be seen in this plot at high field, high Vgs, due to greater scattering and lower mobility. Whereas, at low field, low Vgs, pinch-off voltage shift gives higher current at higher temperature.

At Vgs = 0.2 V, a visible kink can be seen at lower temperatures, 0C and -25°C. This is due to trapping/detrapping phenomenon and/or impact ionization at high field [56]. At high field, electrons are more difficult to be trapped since they can escape from the deep level traps and contribute to the overall output current. Impact ionization which happens at high field provides additional holes and electrons [80]. Some of the holes get recombined at the deep level traps and this results in additional channel width and hence the output current increases. These effects are significantly reduced with temperature getting higher introducing scattering and mobility reduction. Again, the same trend is observed in multilayer pHEMTs with greater variation as will be discussed later.
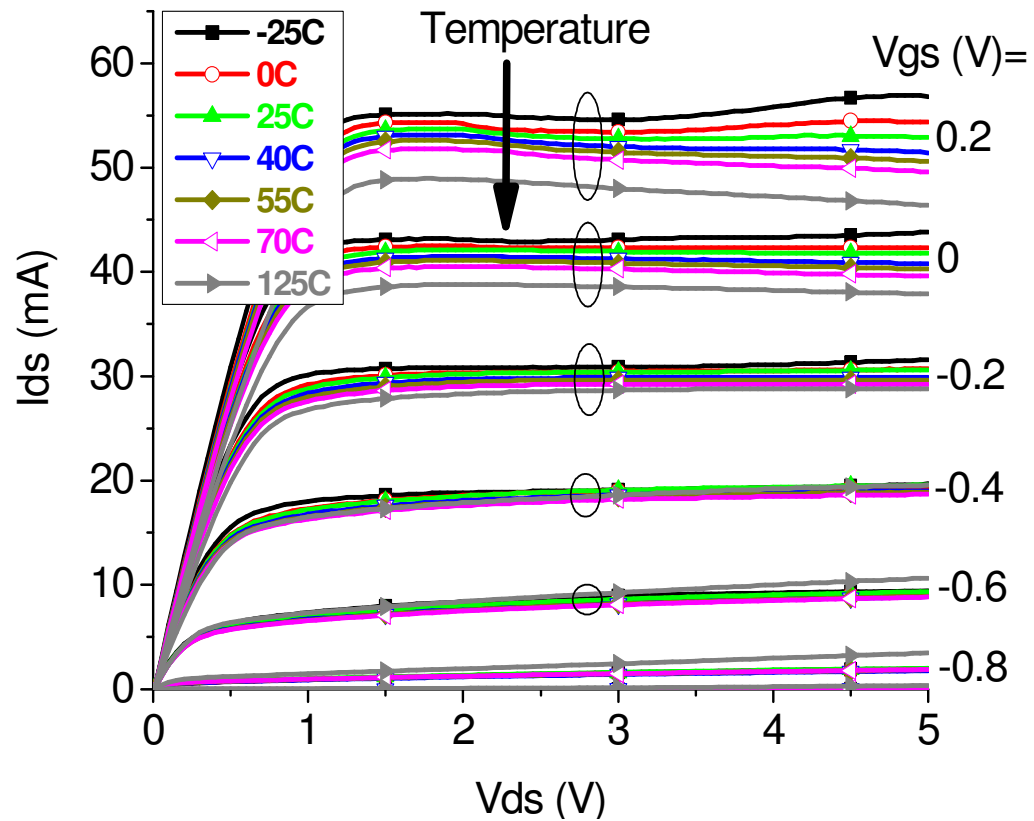
Figure 4.34 Temperature dependent of output characteristics of the virgin 0.5x200 µm² pHEMTs.

As mentioned above, it is observed that the multilayer pHEMT is showing the same trend as the virgin pHEMT except that there is a greater variation of the data as compared with those of virgin results. The greater variation may suggest that the multilayer pHEMTs are more subceptible to the temperature effects than those of virgin devices. In order to investigate the differences in terms of degree of changes due to thermal effects, a few performance parameters need to be studied.

In order to study the effect of temperature on the pinch-off voltage shift, a comparison between the virgin and multilayer pHEMTs is made in Figure 4.35. The plots are both normalised to the data measured at 25°C to eliminate the difference seen in the output currents observed in Figures 4.31 and 4.32. In Figure 4.35, it can be seen that the change in pinch-off voltage is much greater for the multilayer pHEMT. This is especially so at higher temperatures. This can indicate that the multilayer pHEMTs experience greater change in pinch-off voltage with the change of temperature compared to the virgin pHEMTs. It is believed that the thick (~5 µm) polyimide sitting on the top of the multilayer pHEMTs can make the heat dissipation more difficult and this can result in

more heat effect to be seen by the device under test. The multilayer process could also introduce some realignment of surface state for the multilayer pHEMTs. This will also cause a difference in trapping/detrapping phenomenon between the virgin and multilayer pHEMTs which would then result in a difference in the pinch-off voltage shift as device temperature changes. The effects of a lower pinch-off voltage (more negative) would mean an earlier opening of channel allowing electrons to flow through, hence, for the same applied V_{gs}, a lower pinch-off voltage (happening at high temperature) would result in more output current I_{ds}. This is what is observed in Figures 4.33 and 4.34, at low V_{gs} (close to pinch-off).
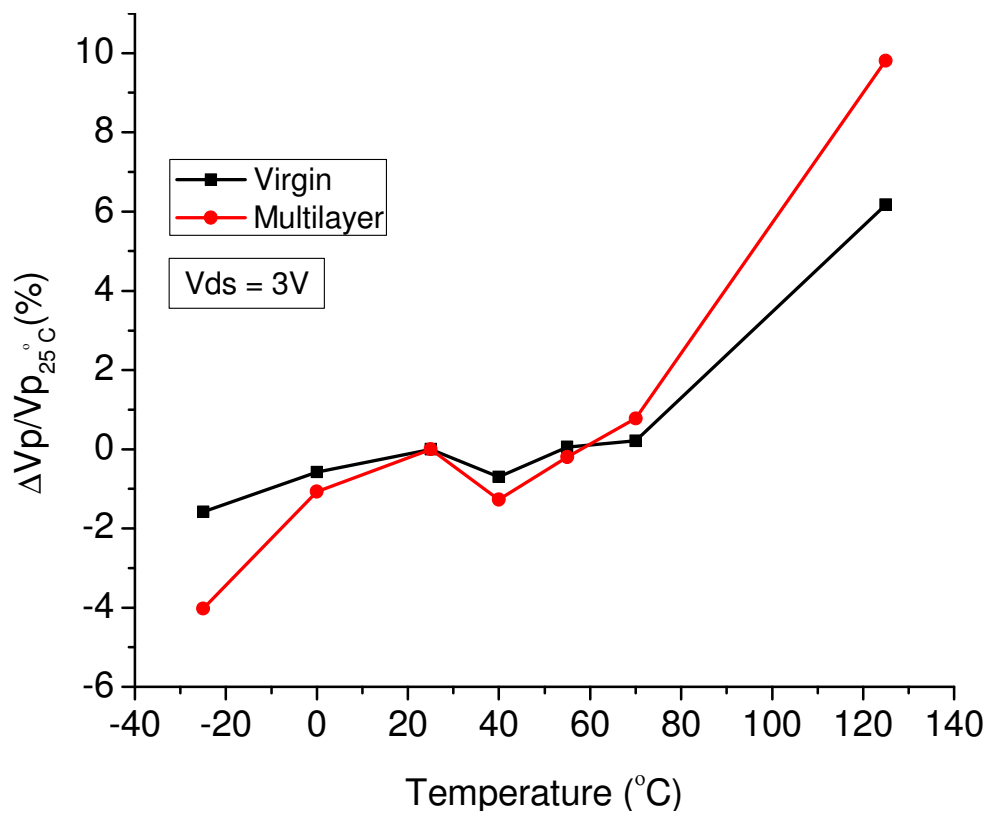
Figure 4.35 Comparison of pinch-off voltage shift with respect to the temperature between virgin and multilayer 0.5x200 μm^2 pHEMTs (V_{ds} = 3V).

Figure 4.36 shows degradation of transconductance, g_m, with temperature. Again, although both virgin and multilayer pHEMTs have the same trend of degradation of transconductance, this variation is greater for the multilayer pHEMTs. The degradation of transconductance is due to the lower output current, Ids, that happens at high temperature and this can imply a slower rate of increase of the output current. The

degradation of g_m is greater in the multilayer pHEMTs because these devices are more sensitive to the change of temperature as compared with the virgin transistors.

As the g_m is directly related to output current I_{ds}, similar kind of comparison of the degradation of the output current Ids is shown in Figure 4.37. A similar trend is seen and multilayer pHEMTs are more susceptible to the heat effect and a bigger drop of output current is found.
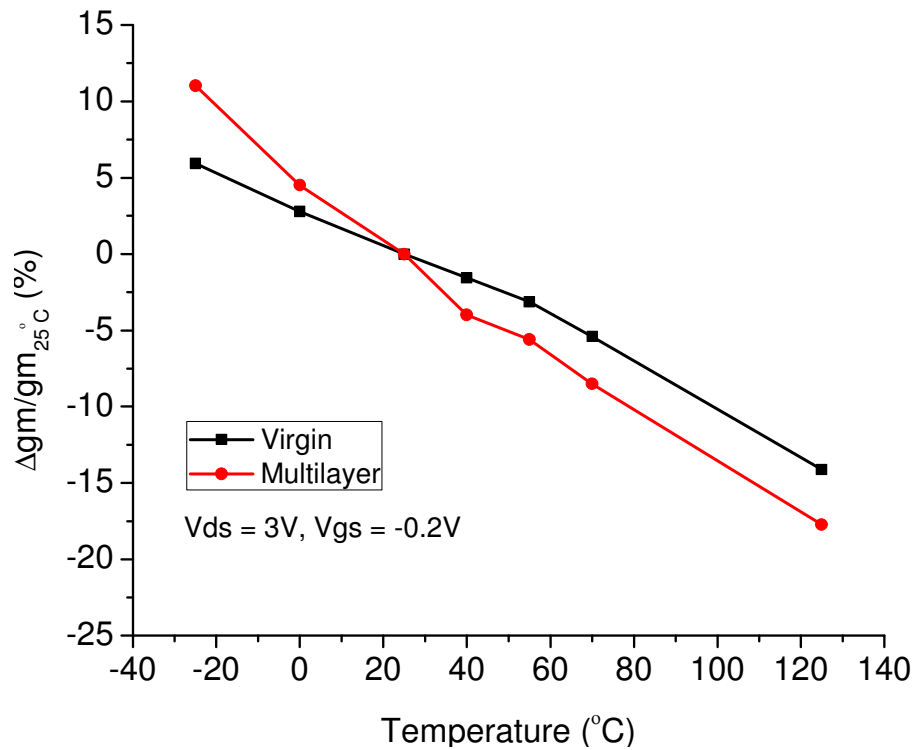
Figure 4.36 Comparison of degradation of transconductance with respect to the temperature between virgin and multilayer 0.5x200 μm^2 pHEMTs (V_{ds} = 3V; V_{gs} = -0.2V).
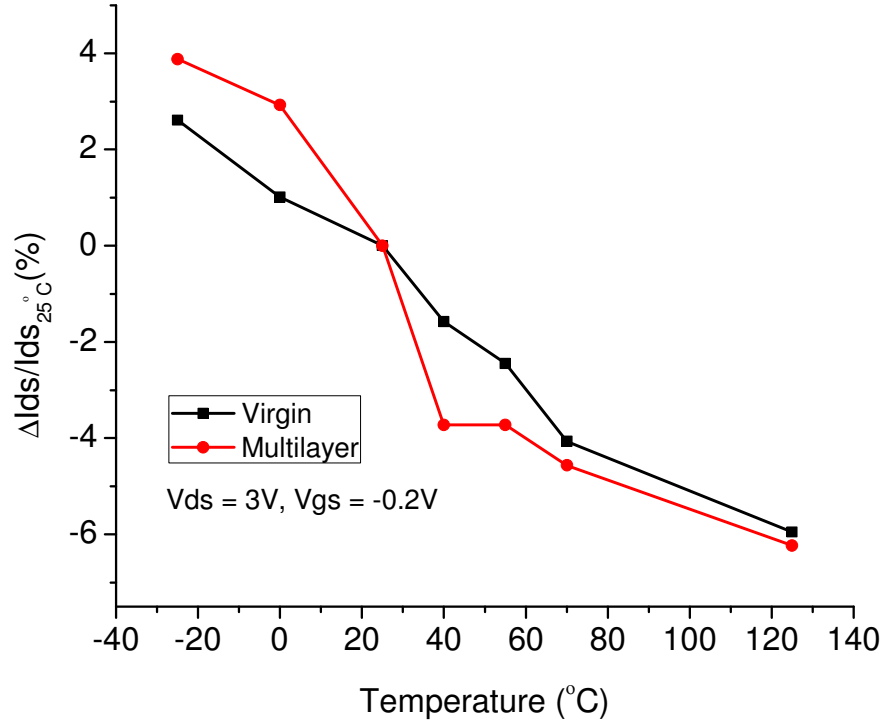
Figure 4.37 Comparison of degradation of output current with respect to the temperature between virgin and multilayer 0.5x200 μm^2 pHEMTs (Vds = 3V; Vgs = -0.2V).

4.5 Small-Signal Temperature Dependent Multilayer pHEMTs Modelling

An important part of the study involves developing linear temperature dependent small-signal models for the pHEMTs. For this study, Dambrine et al.'s [60] equivalent circuit model is adopted. In this work, an automated parameters extractions procedure is developed and written in the Agilent's IC-CAP using the Parameter Extraction Language (PEL). Therefore, direct equivalent circuit parameters (ECPs) extractions can be achieved right after the on-wafer S-parameters measurements. In this work, comparison of both the virgin and multilayer AlGaAs/InGaAs pHEMTs is made in order to investigate the effect of multilayer processing and the sensitivity of both of these devices to thermal effects. Analyses of both sets of the extracted ECPs provide some valuable insights to the governing physics of the transistors which can be helpful for future designs and optimizations of multilayer 3D MMICs.

From the last section, temperature dependent DC characteristics of the multilayer pHEMTs have been discussed. It is found that multilayer pHEMTs, compared to the virgin pHEMTs, are more sensitive to the change of temperature. For that reason, an essential study of the temperature dependent small-signal model for the multilayer pHEMTs is required. The small-signal model is to be utilized as an accurate tool to predict the behaviours of the device at high frequency can be obtained. The adopted model topology has been shown in section 4.3 in Figure 4.18.

On-wafer S-parameters measurements are performed from 45MHz to 40GHz using HP8510C VNA controlled by the IC-CAP. Direct parameters extractions are then performed where it gives maximum transconductance, g_m. Temperature control is provided by Temptronic TP03200A varying from -25 to 125^oC. Within this range of temperature and the bias point, the ECPs are expected to be linearly dependent with the temperature [70] and can be represented as:

$$P(T) = P(T_0)[1 + B(T - T_0)]$$

(4.50)

Where B is the temperature coefficient (TC) in units per degree, T_0 is the reference temperature in 0^oC, and P_0 is the value of the parameter at the reference temperature.

4.5.1 Extrinsic Parameters Analysis

During the development of temperature-dependent small-signal model, extrinsic parameters, namely the device parasitics C_{pg}, C_{pd}, L_s, L_g, L_d, R_s, R_g and R_d, are first extracted followed by the intrinsic parameters. The parasitic capacitances and inductances are found to be unchanged with the temperature. As understood from the relationships between the small-signal parameters and the physical structure of the pHEMTs, C_{pg} and C_{pd} are the parasitic capacitances that are predominantly determined by the probing pads [53]. Hence, as seen from the Figure 4.2, the sizes of the probing pads of the multilayer pHEMTs are bigger than the virgin pHEMTs which result in the greater values of C_{pg} and C_{pd}. Their repective values are shown in Figure 4.38. C_{pg} and C_{pd} as being parasitic capacitances should not vary with temperature according to the definition of capacitance

$$C = \frac{\varepsilon_o \varepsilon_r A}{d}$$

<div align="right">(4.51)</div>

Pads sizes, A, do not change with temperature as well as the distances, d, between them. Temperature coefficient of the dielectric constant of GaAs is about 10^{-4}, therefore the change should be minimal.
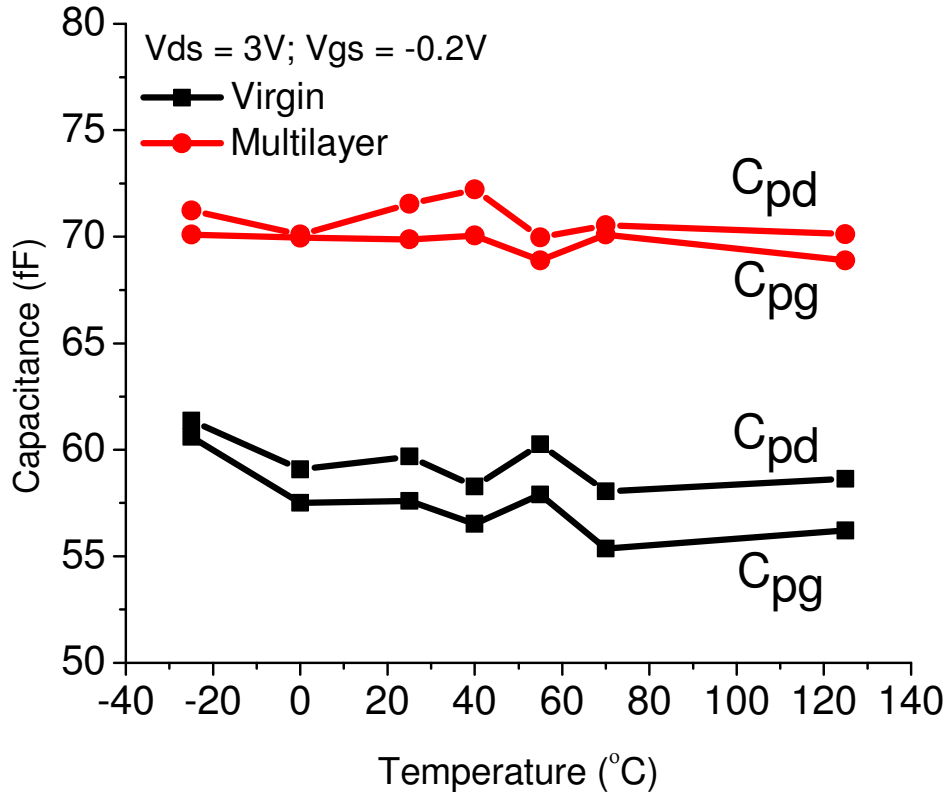
Figure 4.38 Temperature dependent of C_{pg} and C_{pd} for the virgin and multilayer pHEMTs.

The parasitic inductances, L_s, L_d and L_g, again, relate to the physical structure of the pHEMTs. Fundamental definition of inductance suggests that the longer the trace, the greater inductance will be. Compared to the virgin pHEMTs, multilayer pHEMTs have longer interconnects, as can be observed in Figure 4.2, suggesting greater inductances. However, on the other hand, the source pads of the multialyer pHEMTs are very much bigger than the virgin ones. Wider conducting trace indicates lower inductance, therefore, a lower L_s could be expected. Figure 4.39 shows the extracted values of these inductances and verifies the rationales above. In addition, it also shows that L_g has the higest values among the three. This can be explained by the fact that gate fingers are the

narrowest (Figure 4.2) and should thus possess greater inductances. Temperature wise, the parasitic inductances should not vary much with the temperature if one only considers the definition of the inductance. Available closed forms to calculate inductance normally only involve parameters like number of turns, trace widths and lengths, spacing between traces [53]. None of the parameters defining the inductance is sensitive to the change of temperature.
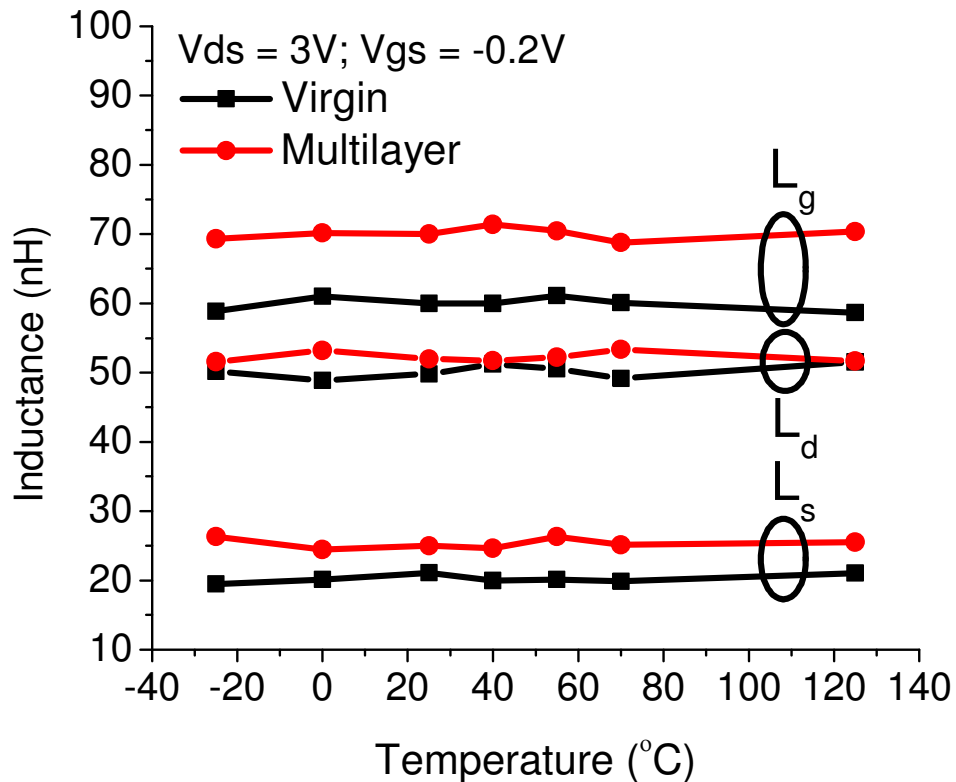
Figure 4.39 Temperature dependent of L_s, L_d and L_g for the virgin and multilayer pHEMTs.

The terminal resistances of the devices, on the other hand, vary linearly with the temperature and they are shown in Figure 4.40, it can be seen that the resistances of the multilayer ones are greater than the virgin pHEMTs. This is because the overall physical dimensions of the interconnects and probing pads of the multilayer pHEMT are longer and bigger than the virgin ones as can be seen in Figure 4.2. The resistance is well understood to change with temperature. It is mainly due to the fact that both the conductivities of the metalization and the semiconductor are affected by the temperature. Among the three, R_g should be the lowest because it only consists of the metalization, whereas R_s and R_d are related to both the metalizations as well as the semiconductor

access resistances. Similar results involving multilayer 3D MMIC technology are also reported in [9].
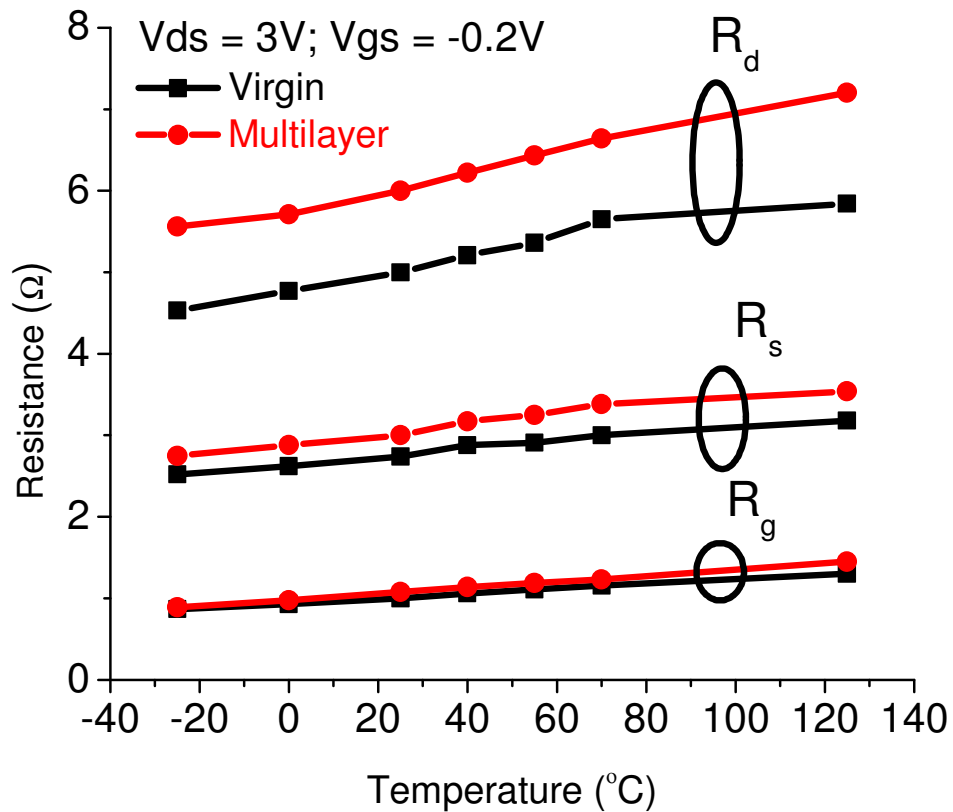
Figure 4.40 Temperature dependent of R$_s$, R$_d$ and R$_g$ for the virgin and multilayer pHEMTs.

4.5.2 Intrinsic Parameters Analysis

In order to investigate the difference in temperature sensitivity between the virgin and multilayer pHEMTs, intrinsic parameters are extracted and normalised to room temperature 25°C. Figures 4.41 and 4.42 show the temperature dependent C$_{gs}$ and g$_m$ respectively. As seen in both figures, multilayer pHEMTs are more sensitive to the change in temperature. This can be attributed to the fact that in the multilayer structure, with layers of polyimides (~5μm) and metals, the generated heat is harder to dissipate as compared to the virgin pHEMTs thus greater thermal effects are experienced in the multilayer devices.
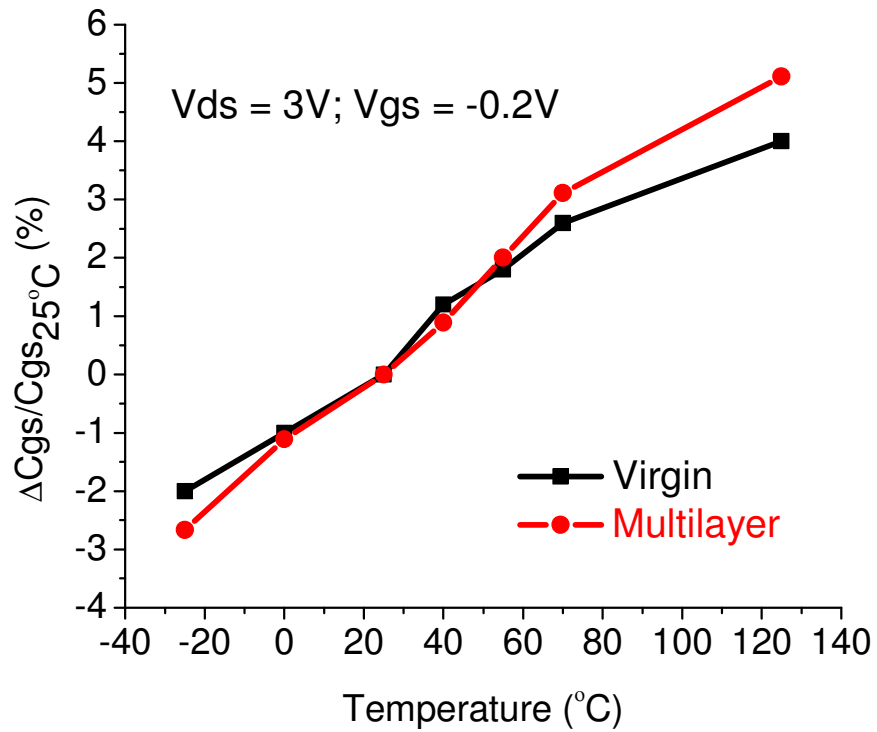
Figure 4.41 Temperature dependent of C$_{gs}$ of the virgin and multilayer pHEMTs (normalised to 25°C).
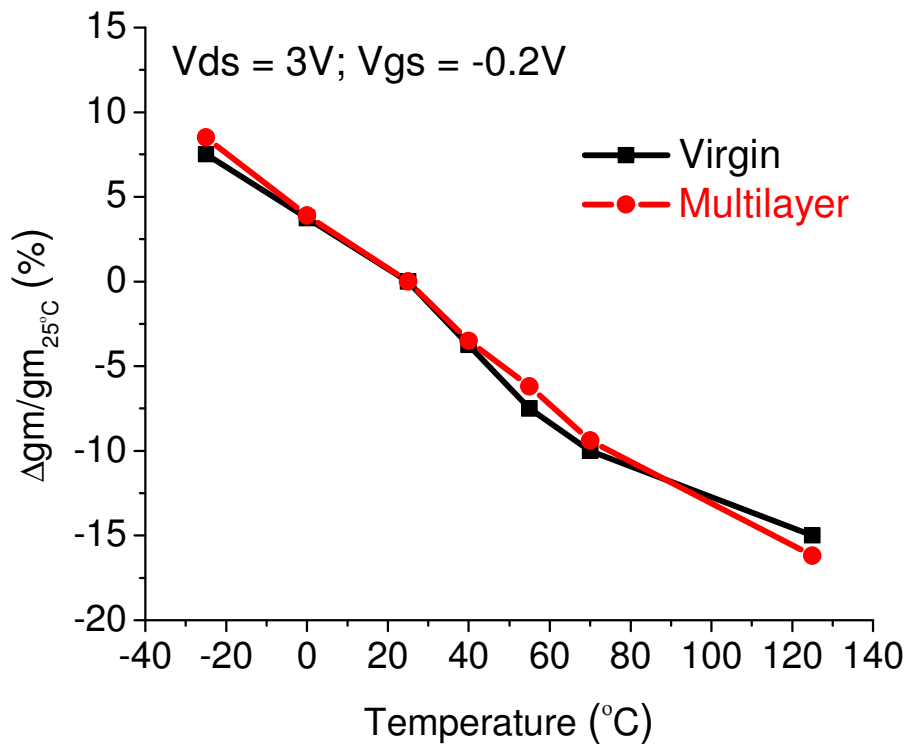
Figure 4.42 Temperature dependent of maximum g$_m$ of the virgin and multilayer pHEMTs (normalised to 25°C).

Comparisons between C_{gd} and C_{ds} can also be observed in Figures 4.43 and 4.44 respectively. C_{gd} represents the miniscule capacitance formed at the edge of the depletion region closer to the drain side. Therefore, this capacitance would change with respect to the change of depletion region. As discussed above, depletion region suffers from thermal effect where induced impact ionisation could significantly change the shape of the depletion width. Due to the fact C_{gd} is a small capacitance, the change in percentage is much greater as seen in Figure 4.43. On the other hand, the change in percentage seen in C_{ds} is smaller. C_{ds} is the only intrinsic capacitance, apart from gm, that is having a negative temperature coefficient which means it decreases as the temperature goes higher. This suggests that a different degradation of the performance of the device as a smaller C_{ds} indicates a greater substrate current component.
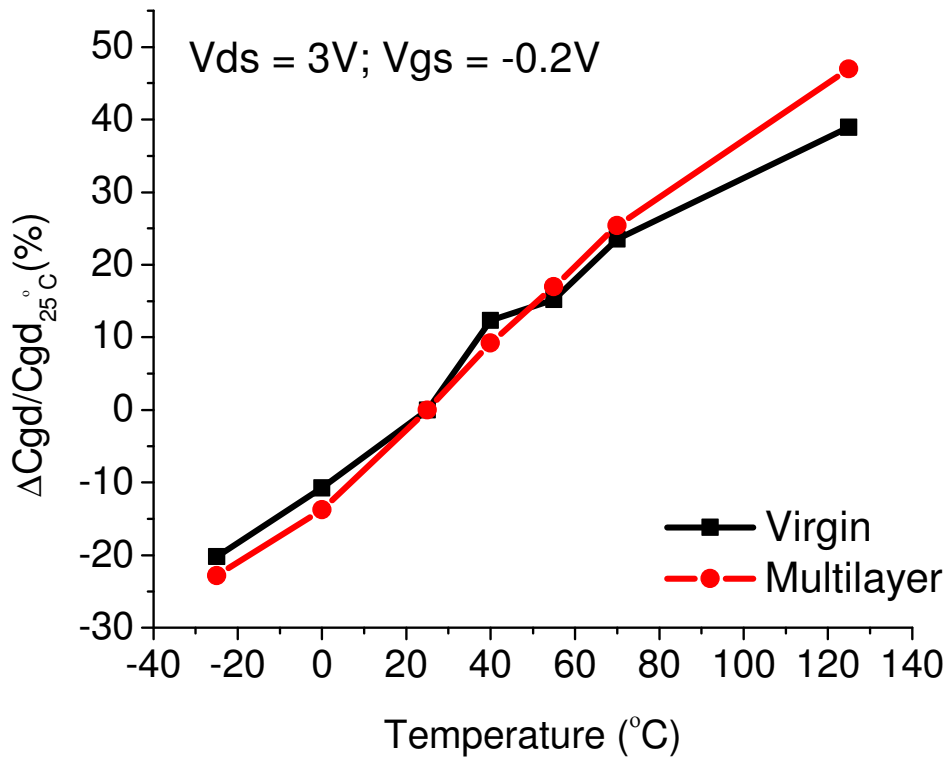
Figure 4.43 Temperature dependent of C_{gd} of the virgin and multilayer pHEMTs (normalised to 25°C).
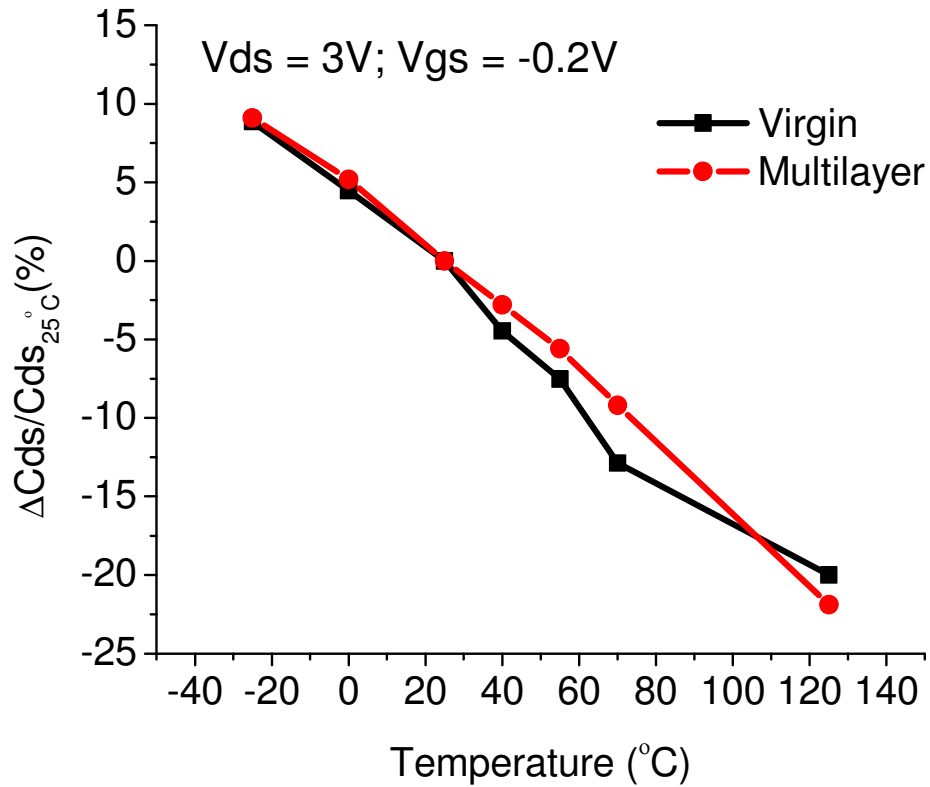
Figure 4.44 Temperature dependent of C_{ds} of the virgin and multilayer pHEMTs (normalised to 25°C).

From Figures 4.45 and 4.46, comparisons of R_{ds} and R_i between virgin and multilayer are presented. As expected from the resistance response to the temperature change, both of R_{ds} and R_i show an increasing trend as the temperature increases. Again, between virgin and multilayer, multilayer pHEMTs show a greater sensitivity to the temperature change. As R_i represents the channel resistance, it indicates yet another degradation of the performance as less current can pass through the channel. The percentage of change in R_i is greater because it is usually a very small resistance.
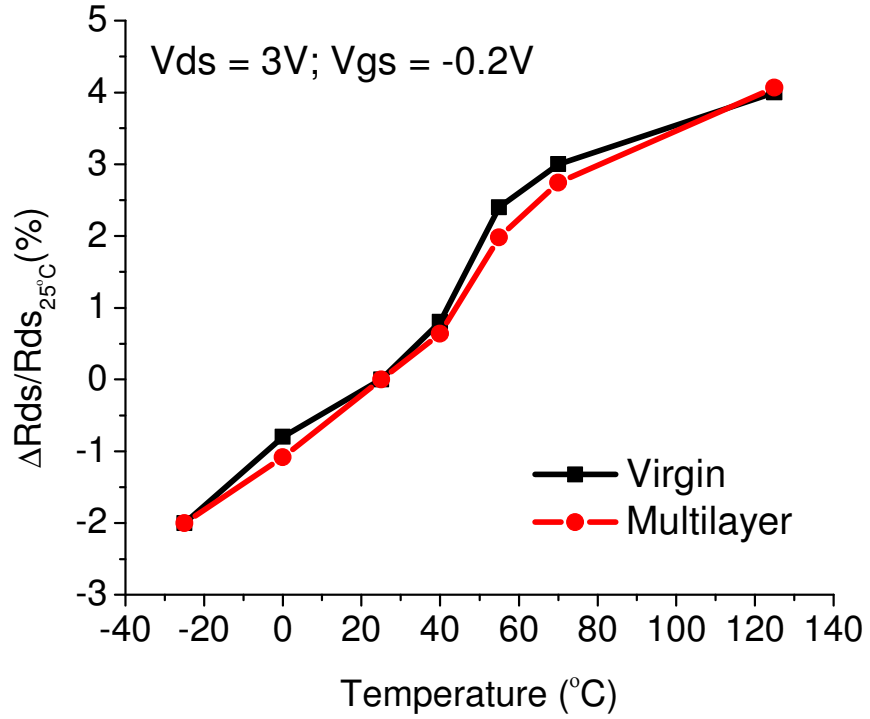
Figure 4.45 Temperature dependent of R$_{ds}$ of the virgin and multilayer pHEMTs (normalised to 25°C).
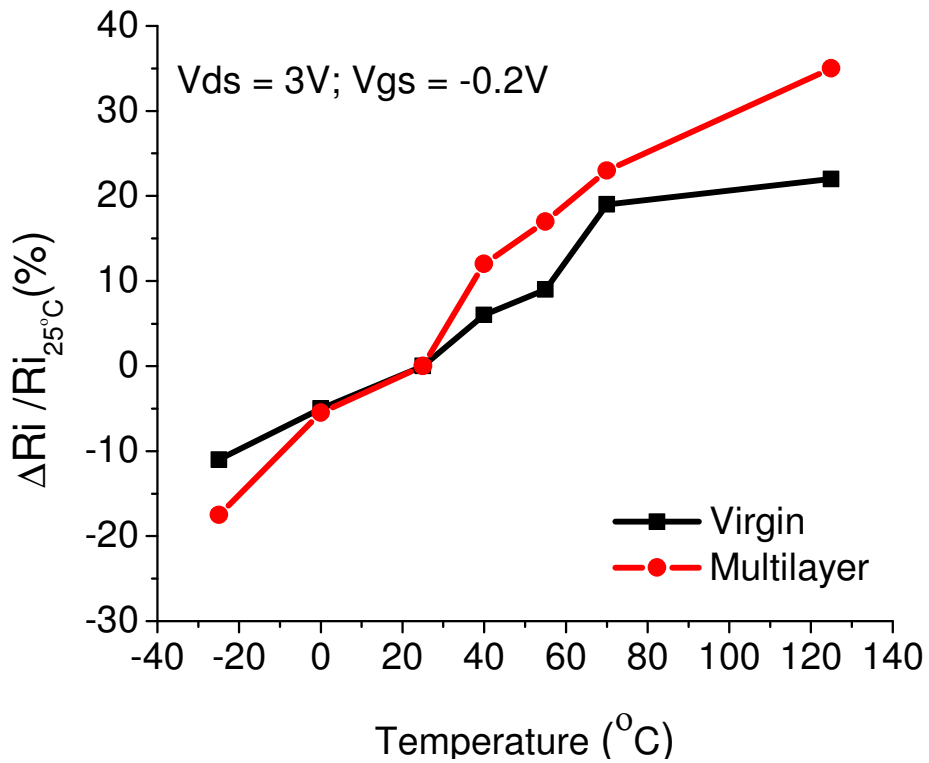
Figure 4.46 Temperature dependent of R$_i$ of the virgin and multilayer pHEMTs (normalised to 25°C).

Figure 4.47 shows comparison of the last intrinsic parameter, the time delay of the transconductance, τ. As can be observed, it degrades higher temperature suggesting a longer time delay. Multilayer pHEMTs, as can be seen, suffer from a higher degree of change of delay compared to the virgin ones.
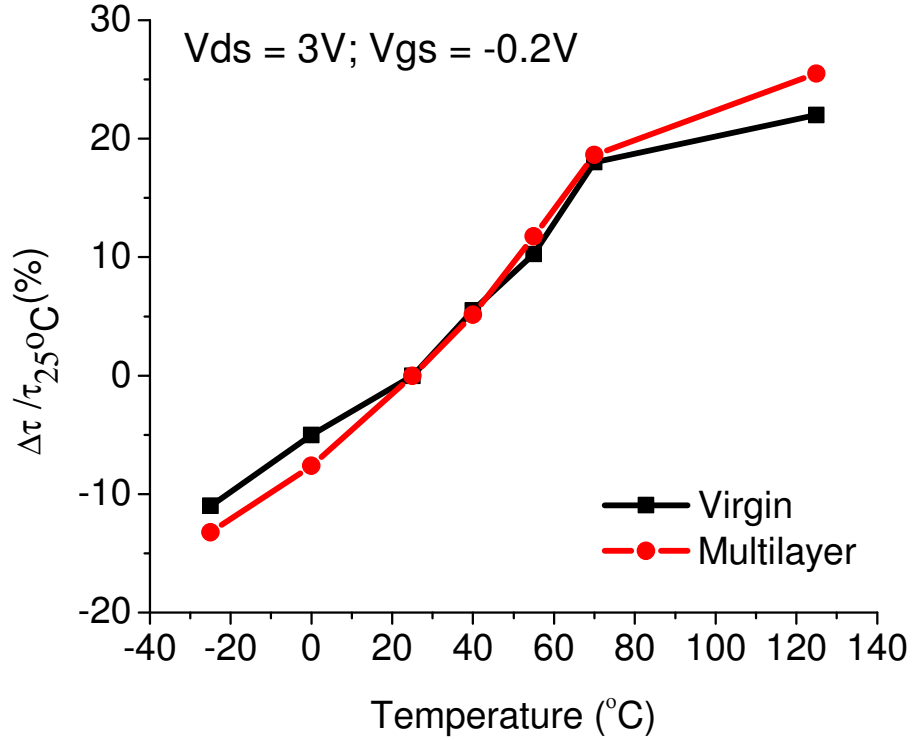
Figure 4.47 Temperature dependent of τ of the virgin and multilayer pHEMTs (normalised to 25°C).

It is also useful to compare frequency characteristic of the devices with increasing of temperature. Figure 4.48 shows temperature dependent f_t and f_{max} of virgin and multilayer pHEMTs. The degradations seen are dominantly caused by the degradation of g_m (Figure 4.42), as seen from the expressions given below [70]:

$$f_t(T) = \frac{g_m(T)}{2\pi\left(C_{gs}(T) + C_{gd}(T)\right)} \qquad (4.52)$$

$$f_{max}(T) = \frac{f_t(T)}{2\sqrt{r_1(T) + \tau(T)f_t(T)}} \qquad (4.53)$$

Where

$$r_1(T) = \frac{R_g(T) + R_i(T) + R_s(T)}{R_{ds}(T)} \qquad (4.54)$$

$$\tau(T) = 2\pi R_g(T) C_{gd}(T) \qquad (4.55)$$
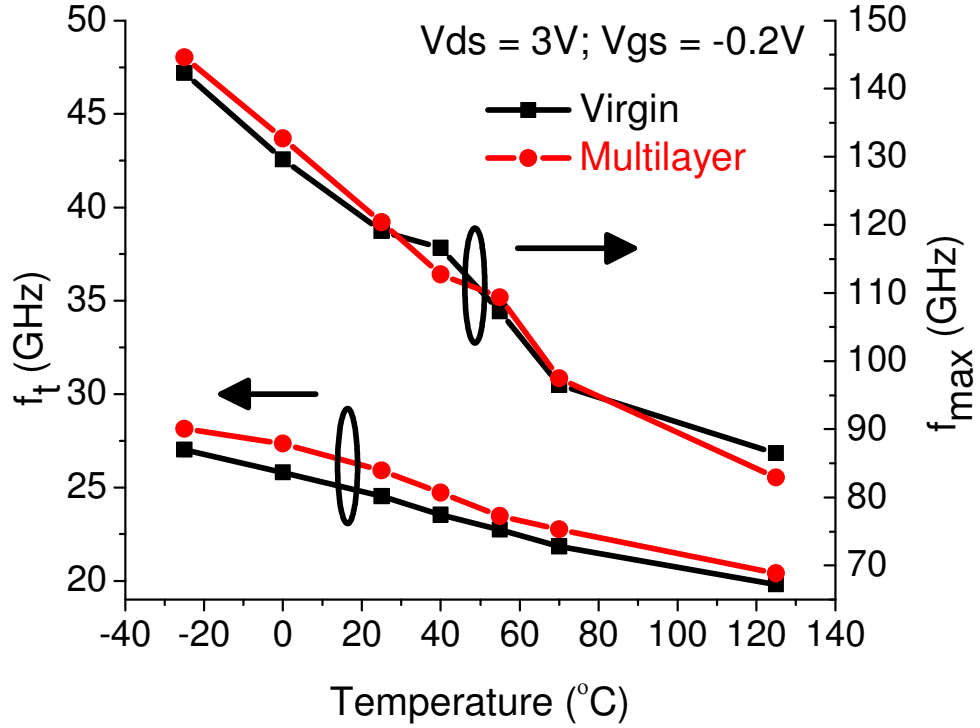
Figure 4.48 Temperature dependent of f_t and f_{max} of the virgin and multilayer pHEMTs.

Table 4.3 presents all the temperature dependent ECPs as well as the f_t and f_{max} with the associated temperature coefficients (TCs) with reference temperature at 0^oC. It can be readily seen that all the ECPs of multilayer pHEMTs are greater than the virgin ones confirming multilayer pHEMTs are more sensitive to the temperature. Applying temperature coefficients given in Table I to Equation (2.12) provides all the essential temperature dependent small-signal parameters. For the virgin pHEMTs:

$$R_s(T) = R_s(T_0)\left[1 + 1.71 \times 10^{-3}(T - T_0)\right] \qquad (4.56)$$

$$R_d(T) = R_d(T_0)\left[1 + 1.79 \times 10^{-3}(T - T_0)\right] \qquad (4.57)$$

$$R_g(T) = R_g(T_0)\left[1 + 3.18 \times 10^{-3}(T - T_0)\right] \qquad (4.58)$$

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$$C_{gd}(T) = C_{gd}(T_0)\left[1 + 4.45 \times 10^{-3}(T - T_0)\right] \tag{4.59}$$

$$C_{ds}(T) = C_{ds}(T_0)\left[1 - 1.87 \times 10^{-3}(T - T_0)\right] \tag{4.60}$$

$$C_{gs}(T) = C_{gs}(T_0)\left[1 + 0.4 \times 10^{-3}(T - T_0)\right] \tag{4.61}$$

$$R_{ds}(T) = R_{ds}(T_0)\left[1 + 0.39 \times 10^{-3}(T - T_0)\right] \tag{4.62}$$

$$R_i(T) = R_i(T_0)\left[1 + 2.27 \times 10^{-3}(T - T_0)\right] \tag{4.63}$$

$$g_m(T) = g_m(T_0)\left[1 - 1.44 \times 10^{-3}(T - T_0)\right] \tag{4.64}$$

$$\tau(T) = \tau(T_0)\left[1 + 2.3 \times 10^{-3}(T - T_0)\right] \tag{4.65}$$

$$f_t(T) = f_t(T_0)\left[1 - 1.86 \times 10^{-3}(T - T_0)\right] \tag{4.66}$$

$$f_{\max}(T) = f_{\max}(T_0)\left[1 - 2.66 \times 10^{-3}(T - T_0)\right] \tag{4.67}$$

For the multilayer pHEMTs:

$$R_s(T) = R_s(T_0)\left[1 + 1.87 \times 10^{-3}(T - T_0)\right] \tag{4.68}$$

$$R_d(T) = R_d(T_0)\left[1 + 2.09 \times 10^{-3}(T - T_0)\right] \tag{4.69}$$

$$R_g(T) = R_g(T_0)\left[1 + 3.83 \times 10^{-3}(T - T_0)\right] \tag{4.70}$$

$$C_{gd}(T) = C_{gd}(T_0)\left[1 + 5.17 \times 10^{-3}(T - T_0)\right] \tag{4.71}$$

$$C_{ds}(T) = C_{ds}(T_0)\left[1 - 1.92 \times 10^{-3}(T - T_0)\right] \tag{4.72}$$

$$C_{gs}(T) = C_{gs}(T_0)\left[1 + 0.5 \times 10^{-3}(T - T_0)\right] \tag{4.73}$$

$$R_{ds}(T) = R_{ds}(T_0)\left[1 + 0.41 \times 10^{-3}(T - T_0)\right] \tag{4.74}$$

$$R_i(T) = R_i(T_0)\left[1 + 3.42 \times 10^{-3}(T - T_0)\right] \tag{4.75}$$

$$g_m(T) = g_m(T_0)\left[1 - 1.5 \times 10^{-3}(T - T_0)\right] \tag{4.76}$$

$$\tau(T) = \tau(T_0)\left[1 + 2.6 \times 10^{-3}(T - T_0)\right] \tag{4.77}$$

$$f_t(T) = f_t(T_0)\left[1 - 2.03 \times 10^{-3}(T - T_0)\right] \tag{4.78}$$

$$f_{max}(T) = f_{max}(T_0)\left[1 - 3 \times 10^{-3}(T - T_0)\right] \tag{4.79}$$

Table 4.3 Temperature coefficients (TCs) for equivalent circuit parameters (ECPs) and f_t and f_{max} with reference temperature at $0\,^{\circ}\text{C}$ ($V_{gs} = -0.2V$; $V_{ds} = 3V$)

Properties	B(10^{-3}/°C)_virgin	B(10^{-3}/°C)_multilayer
R_s (Ω)	1.71	1.87
R_d (Ω)	1.79	2.09
R_g (Ω)	3.18	3.83
C_{gd} (fF)	4.45	5.17
C_{ds} (fF)	-1.87	-1.92
C_{gs} (fF)	0.4	0.5
R_{ds} (Ω)	0.39	0.41
R_i (Ω)	2.27	3.42
g_m (mS)	-1.44	-1.5
τ (ps)	2.3	2.6
F_t (GHz)	-1.86	-2.03
F_{max} (GHz)	-2.66	-3

Thermal effects on semiconductors can be summarised into the following important temperature dependent physical parameters: bandgap of the material, electron saturation velocity, electron mobility, built-in potential and barrier height of the material, dielectric constants and specific contact resistance [10]. The different TCs extracted in Table 4.3 between the virgin and multilayer pHEMTs are due to the change of surface built-in potential and barrier height during the multilayer processing, and also, the change of dielectric constant and specific contact resistance of the multilayer technology. The reason for the different TCs extracted for each ECPs is because all the above mentioned temperature dependent physical parameters will have different degree of influence on the respective ECPs. Comparing to published work in [70], all the extracted TCs are found in similar fashion although different in magnitudes. It should be noted that g_m and C_{ds} were found to be negative too in [70].
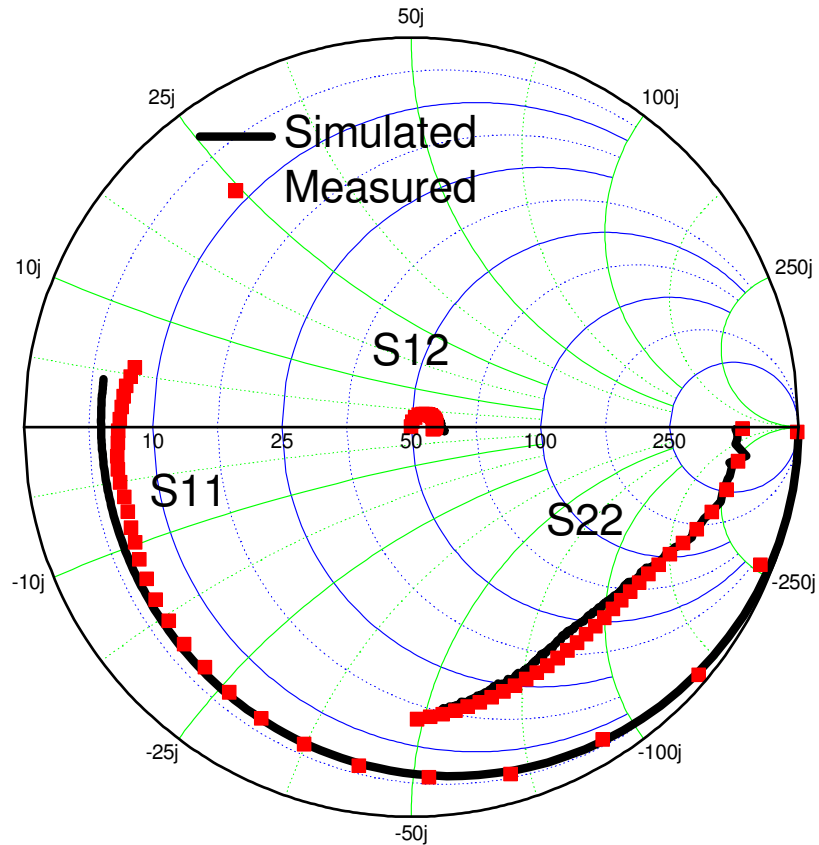
Figure 4.49 Comparisons between measured and simulated S-parameters of the virgin pHEMT at 125 °C (bias: V_{gs}=-0.2V; V_{ds}=3V).

The validation of the temperature dependent small-signal model is shown in Figure 4.49 which indicates comparisons between the model and measurement at 125°C at the chosen bias point. Good agreement can be observed thus verifying the accuracy of the model.

Linear temperature dependent small-signal models for both pre- and post-multilayer-process AlGaAs/InGaAs pHEMTs have been successfully developed using an automated direct equivalent circuit parameters extractions from on-wafer S-parameters measurements. The models provide accurate predictions of the devices performance covering a temperature range from -25 to 125°C. A slight greater impact of thermal effects on multilayer pHEMTs is observed through the overall greater temperature coefficients found in these devices. This is due to the additional layers of polyimides and metals on top of the active region making the heat dissipation inefficient. This information is useful for CAD designers in providing a compact and faster and better

prediction of the behaviours of multilayer CPW MMIC in the future. Optimization of the device design and multilayer technology can also be achieved.

Chapter 5   Conclusions and Future Works

5.1 Conclusions

The multilayer coplanar waveguide (CPW) monolithic microwave integrated circuit (MMIC) technology is a new area of research leading to the development of compact 3D MMICs. This requires in building a library of active and passive circuit components that can be directly integrated in this technology for realisation of various functional circuitries. The characterisation and modeling of AlGaAs/InGaAs pHEMTs under this novel 3D MMIC environment have been successfully carried out in this work for the first time. A fast and accurate semi-automated circuit parameters extraction procedure is developed with the aid of a commercial toolkit. On-wafer S-parameters measurement data is directly fed into the extraction routine and a reliable and compact equivalent circuit model is thus established. This empirical process is extended to multiple bias conditions over a wide range of temperature and up to frequency of 40 GHz for pHEMTs integrated into the 3D multilayer MMICs.

The AlGaAs/InGaAs pHEMTs under investigation in this work have been designed and fabricated on semi-insulating GaAs substrate by Filtronic Compound Semiconductors. Multilayer processing is then applied on the pre-fabricated pHEMT wafers at The Electromagnetics Centre at The University of Manchester. In order to study the uniformity of both the pre- (virgin) and post-multilayer-processed (multilayer) AlGaAs/InGaAs pHEMTs, DC and RF S-parameters measurements were carried out and their DC and RF characteristics were compared. It is found that the pHEMTs fabricated closer to the edge of the wafer have poorer performance than the rest. At the same operating bias point, 10% or greater lower output current, I_{ds}, can be seen in DC. The same degree of poorer performance can be observed in lower cut-off frequencies, f_t, poorer isolations and lower gains. Apart from these exceptions, it is shown that uniformities are observed for both virgin and multilayer pHEMTs. The discrepancies are well within the tolerance and less than 3%. It is also found that, by comparing the DC and RF characteristics of both virgin and multilayer pHEMTs, the multilayer process does not introduce any unwanted effects on the pHEMTs fabricated with the multilayer

technology. The difference between the virgin and the multilayer results is again within the tolerance of the measurement system and is less than 3%.

Several fabricated multilayer MMICs wafers which have some virgin and multilayer pHEMTs have been carefully characterised by on-wafer measurements of DC and S-parameter measurements. Traditional approach involves numerous iterations and optimizations in order to develop an accurate equivalent circuit model. In this work, an automatic data extraction tool has been developed by using Agilent's IC-CAP. By using the built-in Parameter Extraction Language (PEL), macro scripts are written to automate the measurements and extractions procedure. An equivalent circuit model is adopted and it is compact and intuitively built with the underlying physics of FET taken into account. In contrast to conventional methods, the extraction procedure developed in this work, does not involve optimisations and thus offer a fast and accurate way of modelling the device. In order to extract the required equivalent circuit parameters (ECPs), three biasing conditions have been considered in the measured data. They are pinch-off, cold and hot biasing conditions. The hot biasing condition is chosen at the point where V_{gs} = -0.2V and V_{ds} = 3V, this point is selected to obtain the maximum transconductance, g_m, available in the pHEMTs studied. Two small-signal models for each virgin and multilayer pHEMTs have been developed. The validations of the models have been verified by comparing the data with the measured results. It is shown that the simulation results of the generated small-signal models match very well with the measured data, especially from low frequency up to 20GHz. This procedure is attractive not only due to its accuracy but also the considerable shorter time span needed and the compactness of the procedure involved. Circuit designers can easily adopt these models into their designs and optimise the performance of the product accordingly. Models at other biasing conditions have also been established by using the same approach.

The pHEMTs studied in this work have been designed for linear power amplifiers MMICs. Since enormous amount of heat can be generated during the operation of these circuits and the fact that the thermal conductivity of GaAs (~45W/m°C) is only one third of Silicon (~150W/m°C), therefore the GaAs devices performances can be affected by the generated heat. This is specially so when one considers those pHEMTs which are incorporated in the multilayer technology. Therefore an important part of this thesis was concerned with the study of the temperature characterisation of these devices. A

TEMPTRONIC temperature control and a wafer chamber were used to measure the DC and S-parameters behaviours of these devices from -25 to 125 °C. For the DC measurements, at lower V_{gs}, close to pinch-off voltage, V_p, it is found that the I_{ds} magnitude increased at higher temperature as compared to the ambient environment for the same input voltage V_{gs}. This was found to be due to the generation of higher carriers concentrations at higher temperature which resulted in a pinch-off voltage, V_p, shift. In other words, as the channel is now effectively "more doped", the channel opens earlier than previously at lower temperature. In contrast, at higher V_{gs}, scattering phenomenon and reduced carriers mobility at higher temperature are the dominant effects resulting in lower output current, I_{ds}, at the same input voltage, V_{gs}. At higher V_{gs}, with the electric field going stronger, various high field phenomena are also happening such as impact ionisation, trapping and detrapping of electrons. These can produce a kink in the output current of the device. This kink is more evidently seen at low temperature (at -25 °C) as shown in this work.

In comparison, the multilayer pHEMTs have been observed to be more susceptible to the thermal effect than the virgin counterparts. The difference with respect to temperature in the multilayer pHEMTs is more prominent for example, a greater pinch-off voltage, V_p, shift is observed. These results are therefore suggesting that the multilayer pHEMTs are more sensitive to the heat than those of virgin devices. This can be explained by looking at the structural difference between a virgin and a multilayer pHEMT. Multilayer pHEMTs with the extra layers of polyimides (~5μm) and metals on top of the active devices have more difficulty in terms of heat dissipation. A lower capability of heat-handling results in a greater sensitivity to the temperature.

A compact small-signal modelling technique for the pHEMTs has been established and this is extended for the temperature study with the aim of developing a novel temperature-dependent small-signal parameter model. For each device parameter a set of measurements has been taken at several temperatures covering the range from -25 to 125 °C. Within this range of temperature, it was assumed that most of the equivalent circuit parameters (ECPs) can be expressed as linear equations with temperature coefficients (TCs). Extrinsic parameters, C_{pg}, C_{pd}, R_s, R_d, R_g, L_s, L_d and L_g are bias-independent and extracted using the given procedure. The study of these parameters indicated that the parasitic capacitances and inductances are unchanged with respect to the temperature.

On the other hand, the extrinsic resistances were found to be linearly dependent with temperature. This was found to be consistent with the known knowledge that the conductor used in this work (mainly gold layer) is linearly dependent with temperature.

All intrinsic parameters, on the other hand, show a linear dependence with the temperature. The magnitude of most of these parameters increase with the increase of device temperature showing positive temperature coefficients. Drain-Source capacitance, C_{ds}, and transconductance, g_m, are the only two parameters which show negative temperature coefficients. It is also observed that the temperature coefficients for all the parameters are different because the thermal effects will have different degree of influence on the parameters. The degradation of g_m can be explained in the same fashion as the degradation of I_{ds} seen in DC. Lower output current at the same input voltage at higher temperature results in lower transconductance. As the g_m is one of the most important parameters governing the performance of a device, the overall cut-off frequency, f_t, and maximum available gain frequency, f_{max}, are limited by the dominant effect of degradation of g_m and this shows linear reductions with respect to temperature.

Tabulated extracted temperature coefficients for both virgin and multilayer pHEMTs indicate a greater temperature sensitivity for the multilayer pHEMTs. All temperature coefficients for each of the ECPs are greater than the virgin counterparts, most of them show a more than 10% swing. This is again another observation showing that multilayer pHEMTs is more susceptible to the heat effects. In other words, the degradation of performance of multilayer pHEMTs is more prominent due to their poorer heat-handling capability. There are several possibilites for this including a possible change of built-in potential or barrier height during the multilayer processing as the surface states of the device layer could be realigned; another possibility is the change of effective dielectric constant of layers of polyimide and the possibility of change of specific contact resistance of the multilayer pHEMTs.

Furthermore, the developed temperature-dependent small-signal models for both virgin and multilayer pHEMTs are validated to the measured data and show very good agreements with error less than 5%. This procedure shows how these models could be easily incorporated into circuit designs for greater optimisations. The study of this work

can also be extended into exploring alternative materials to be used in the 3D MMIC technology and thus optimising their performances.

5.2 Future Works

As the usefulness of a small-signal model, even a temperature dependent one, is hugely dependent on the specific applications and designs. So often, CAD designers would like a more complex model that could account for a broad range of biases and temperatures. It is imperative to extend the established techniques in this work to large-signal modelling. The knowledge acquired in this work about manoeuvring IC-CAP would be extremely valuable and with the necessary scripts written, an automated procedure could be established and complex and time-consuming steps could be completed in a much shorter time span.

Regarding the multilayer technology, as mentioned, alternative materials could be carefully selected to be used as the dielectric layers to boost the performance. A thorough statistical analysis of the multilayer process could also be established to investigate the normal distribution of changes in terms of performance and the standard deviations. As the device technology under study in this work is based on AlGaAs/InGaAs pHEMT, different semiconductor devices could be incorporated in this multilayer technology again to investigate any possible reliability improvements during multilayer fabrication.

Another area of interest would be to designing amplifiers by taking into account the great information which has been achieved in the multilayer project. For example there are various data in the group that show temperature characterisation of various multilayer passive circuits including: multilayer spiral inductors, multilayer folded capacitors and multilayer transmission lines. It would be interesting to design circuits by integrating the passives and the AlGaAs/InGaAs pHEMTs in this work. This would provide a good way to further investigating the data obtained in the present work and to validate the established temperature-dependent models for both active and passive devices.

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