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Flexible Sigma Delta Time-Interleaved Bandpass Analog-to-Digital Converter

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FLEXIBLE SIGMA DELTA TIME-INTERLEAVED BANDPASS ANALOG-TO-DIGITAL CONVERTER

A thesis submitted in partial fulfillment
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By

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I HEREBY RECOMMEND THAT THE THESIS PREPARED UNDER MY SUPERVISION BY Ryan McGinnis ENTITLED Flexible Sigma Delta Time-Interleaved Bandpass Analog-to-Digital Converter BE ACCEPTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE DEGREE OF Master of Science in Engineering.

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ABSTRACT

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Conversion of analog signals to their digital equivalent earlier in a circuit's topology facilitates faster and more efficient exploitation of the information contained within. Analog-to-digital converters (ADCs) form the link between the analog and digital realms. In high frequency circuits ADCs must often be implemented further downstream after several stages of down-conversion, or through the use of more expensive technologies such as Bi-polar Junction Transistors or Gallium Arsenide. This thesis presents a technique to utilize Complimentary Metal Oxide Semiconductor technology in a parallel time-interleaved architecture. This will reduce circuit complexity and allow the ADC to be placed further upstream reducing the need for large and expensive analog hardware. This thesis utilizes an architecture that allows for higher frequency input signals through the use of down-sampling, parallel processing, and recombination.

This thesis will also present the use of sigma delta based modulation in order to increase the resolution of the digital output signal. Exploitation of oversampling and the resultant noise-shaping characteristics of the sigma delta modulator will enable the user to gain resolution without the increased cost of implementing more expensive ADC architectures such as Flash.

This thesis also presents a flexible converter such that both the center frequency and resolution can be modified by manipulating inputs. Specifically, the input and output filters as well as the sampling frequency can be tuned such that the circuit will operate at a particular center frequency. Also, the circuit will have flexible resolution which can be controlled by the clock input.

Proof of concept is accomplished with a Matlab® simulation followed by schematic implementation in Cadence®. The design is constructed using IBM® 0.13 µm technology with a rail voltage of 1.2 V. Results are evaluated through the calculation of the effective number of bits and the signal to noise ratio. Conclusions and guidance on future research are provided.

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1. INTRODUCTION

Conversion of analog signals to their digital equivalent early in a circuit's architecture increases system flexibility, reduces overall cost, and allows for more efficient exploitation of signals. In this context there is a reduced need for large analog components resulting in a smaller overall size, weight, and dissipated power [6]. This is especially true in Radio Frequency (RF) circuits, where the incoming signal is in the Giga-Hertz (GHz) range.

This research project focuses on developing a flexible sigma delta (ΣΔ) modulator based parallel time-interleaved (PTI) analog-to-digital converter (ADC). This circuit will enable ADC at high speeds while maintaining the ability to change center frequencies and output bit resolution.

Additionally, this project will utilize the unique characteristics of ΣΔ oversampling and noise shaping in order to achieve superior resolution compared to ordinary Nyquist converters [4]. This project will also research a bandpass implementation of the time-interleaving configuration such that the desired output signal can be recovered in multiple frequency ranges [6]. Further, the unique architecture of this project allows the user to input higher frequency signals, perform ADC in lowpass sub-sampled frequency domain with parallel stages, and to recombine the results with the appropriate time delay to reconstruct the digital equivalent higher frequency output signal.

This research project will use IBM® 0.13 µm technology. This technology was chosen due to its small feature size and potential for high performance analog and digital devices.

1.1 PURPOSE

This research project was undertaken to establish proof of concept for a ΣΔ modulator-based PTI ADC as well as to design and analyze the potential performance of this ADC configuration.

1.2 SCOPE

This project will encompass proof of concept simulation and schematic construction of a ΣΔ-based PTI ADC. Particular emphasis will be given to performance as measured by effective number of bits (ENOB) and signal to noise ratio (SNR) at the output.

1.3 PROBLEM

The task is to design a high performance ΣΔ-based ADC that is capable of operating at high frequencies. The design is to provide the user with adjustable center frequencies and variable output resolution. The adjustable center frequencies will be controlled by analog and digital filtering and an adjustable sampling frequency. Variable output resolution will be controlled by adjustable over-sampling.

1.4 METHODOLOGY

This research project was completed in two phases. Phase one focused on proof-of-concept utilizing Matlab®. An ideal system was constructed and tested. This system was evaluated for performance by measuring ENOB and SNR as mentioned previously.

Phase two included the design and testing of the entire circuit utilizing Cadence® design tools. Similar performance metrics were gathered on the schematic implementation and contrasted with the ideal results. IBM® 0.13 µm technology will be utilized in Cadence® for the schematic design.

2 BACKGROUND

Mixed-signal circuits are an essential component in today's world. Efficient exploitation of real-world signals requires that they be converted to digital form. ADCs are the link between the analog and digital domains and can be broken down into two main categories. These categories are comprised of Nyquist rate converters and oversampling converters [1]. Nyquist rate converters rely on the Nyquist principle as shown in Equation 1.

$$fs = 2 f_{MAX}$$

Equation 1 Nyquist Principle [7]

This states that the sampling frequency of the converter, fs, must equal to twice the maximum frequency component of the input signal, f_{MAX}. This ensures that the signal can be uniquely resolved without the effects of aliasing.

Oversampling converters exceed the requirements of the Nyquist principle. This is stated in Equation 2.

$$fs > 2 f_{MAX}$$

Equation 2 Oversampling Criterion [7]

This criterion can reduce the potential for aliasing extraneous signals into the bandwidth of interest [1]. Oversampling converters

are typically characterized by the ratio of the circuit sampling frequency to the Nyquist sampling rate. This is referred to as the Oversampling Ratio (OSR) and is shown in Equation 3.

$$OSR = \frac{f_{\Delta}}{f_{NYQUIST}}$$

Where

f_{Δ} = Sampling frequency of the oversampling circuit

And

$f_{NYQUIST}$ = sampling rate necessary to satisfy the Nyquist principle

Equation 3 Oversampling ratio [1]

Oversampling converters sacrifice computational speed in exchange for higher resolution and reduced quantization error.

2.1 Sigma Delta MODULATOR

The ΣΔ modulator performs ADC while providing noise-shaping functionality that is necessary in order to increase the resolution of the digital signal. The ΣΔ modulator block diagram is shown in Figure 1.

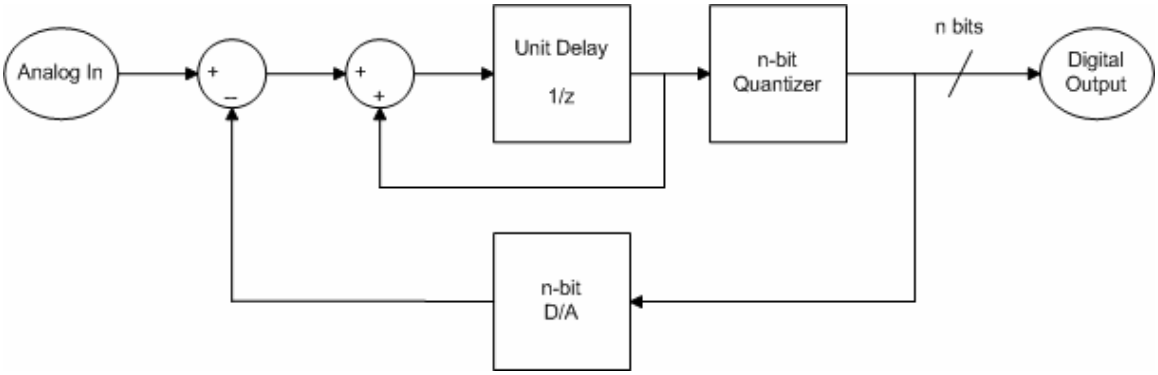

Figure 1 Sigma Delta Modulator Block Diagram

The ΣΔ Modulator consists of a forward and feedback path and components such as an integrator, quantizer, and adder. The forward path consists of the adders, integrator, and quantizer. The integrator tracks the input signal. The quantizer serves to provide the digital output. The feedback path consists of a digital-to-analog converter (DAC). In the case of a single bit modulator, this can be a wire. However, since this project utilizes a ΣΔ modulator which internally has four bits of resolution, the feedback path must utilize a digital to analog converter (DAC). This analog equivalent of the digital output is fed back and subtracted from the input. The adder serves to add the feedback signal, the integrator output, and the input signal. Discrete quantization levels in the quantizer lead to quantization errors.

The method for removing the quantization noise is straightforward. The input signal is converted to its digital equivalent with some quantization error. This signal is converted into an analog equivalent and is fed back to the adder. Also, the integrator signal, which is comprised of the input signal and quantization error, is fed back to the adder. Three signals are present at the adders including the input signal, integrator feedback

composed of the input signal with quantization error, and the analog equivalent of the input signal with quantization error. Effectively the quantization error cancels out because the DAC feedback signal with error is subtracted and the integrator signal with quantization error is added. In this sense, the ΣΔ modulator not only converts analog input signals to digital output signals, but also removes quantization noise in the modulation process. Quantization noise is modeled by inserting an adder directly before the output in the forward path and inserting a noise source $e(n)$. See Figure 2.

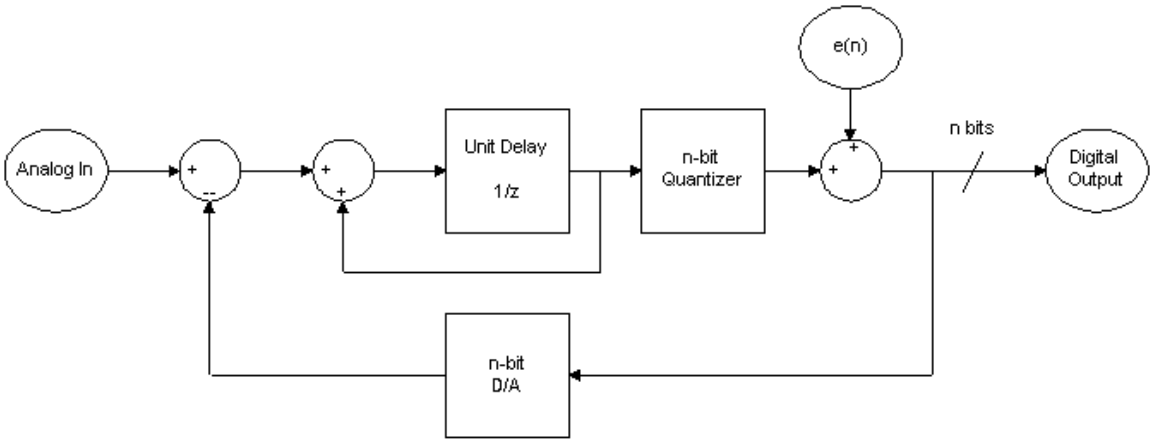

Figure 2 Sigma Delta Modulator Block Diagram with Error Signal

The transfer functions, shown in Equation 4, provide insight into the functionality of the circuit.

$$Y(z) = S_X(z)X(z) + N_E(z)E(z)$$

Where

$Y(z)$ is the transfer function of the ΣΔ modulator

And

$X(z)$ is the input signal

And

$E(z)$ is the quantization noise

And

$$Sx(z) = \frac{H(z)}{1+H(z)}$$

(signal transfer function)

And

$$N_E(z) = \frac{1}{1+H(z)}$$

(noise transfer function)

With

$$H(z) = \frac{z^{-1}}{1-z^{-1}}$$

(ideal integrator)

Yielding

$$Y(z) = z^{-1}X(z) + (1-z^{-1})E(z)$$

Equation 4 Sigma Delta Modulator Transfer Functions [6]

Noise shaping occurs due to the high-pass filter properties of the noise transfer function. This moves a portion of the noise energy beyond the frequencies of interest and thus can be readily filtered after the signal has been processed. This occurs while the input signal is effectively passed through unchanged with a single clock delay. Higher order modulators accentuate the noise shaping property according to Equation 5.

$$NTF(z) = \left(1 - z^{-1}\right)^{K}$$

Where K is the order of the modulator

Equation 5 Higher-Order Sigma Delta Modulator Noise Shaping [13]

Analysis of this equation shows that for higher-order modulators, the noise-shaping increases exponentially, while still passing through the input signal with a single clock delay. A first-order ΣΔ modulator was chosen for this research project due to its stability and to enforce single clock loop delay [13].

Noise shaping in the ΣΔ modulator is also achieved through the use of oversampling. This oversampling causes the quantization noise to be spread over a wider band of frequencies, thus reducing the noise density in the bandwidth of interest [7].

Further motivation for the selection of ΣΔ modulation, is that it has been shown to be robust and able to withstand certain hardware imperfections including quantizer threshold inconsistencies, integrator leakage, and even random noise [14]. The robustness has been attributed to the redundancy built into the ΣΔ modulator [14].

The ΣΔ modulator produces a digital version of the input signal. In the case of this research project, the ΣΔ modulator has four bits of

resolution. This results in sixteen discrete levels that the output can assume. Each bit is a separate output signal assuming binary values either logic "1" or "0". The output from the ΣΔ modulator is then a series of logic "1" or "0" for each bit, which when graphed will appear as a series of pulses. This can be thought of as a coded output signal where each pulse can be decoded to reconstruct the output [14].

2.2 Parallel Time Interleaving

Parallel processing enables processes to run quickly as a problem can be broken down into more manageable tasks. This technique will be utilized in this research project in order to achieve higher resolution and increased frequency range performing ADC using Complimentary Metal Oxide Semiconductor (CMOS) technology. Typically higher frequency ranges have been serviced by other technologies including Bi-Polar Junction Transistors and Gallium Arsenide, which are both costly and inefficient [9]. The trend in receiver technology has been to move the ADC closer to the antenna in order to remove the multiple stages of down-conversion to lower frequencies allowing for the utilization of CMOS technology [6]. It is through the use of CMOS technology that one can achieve low-cost and efficient implementations to higher frequency systems. PTI allows for the signal to be computed in parallel, and then the individual results recombined with appropriate time-shifts, in order to achieve the desired result [6]. The block diagram is shown in Figure 3.

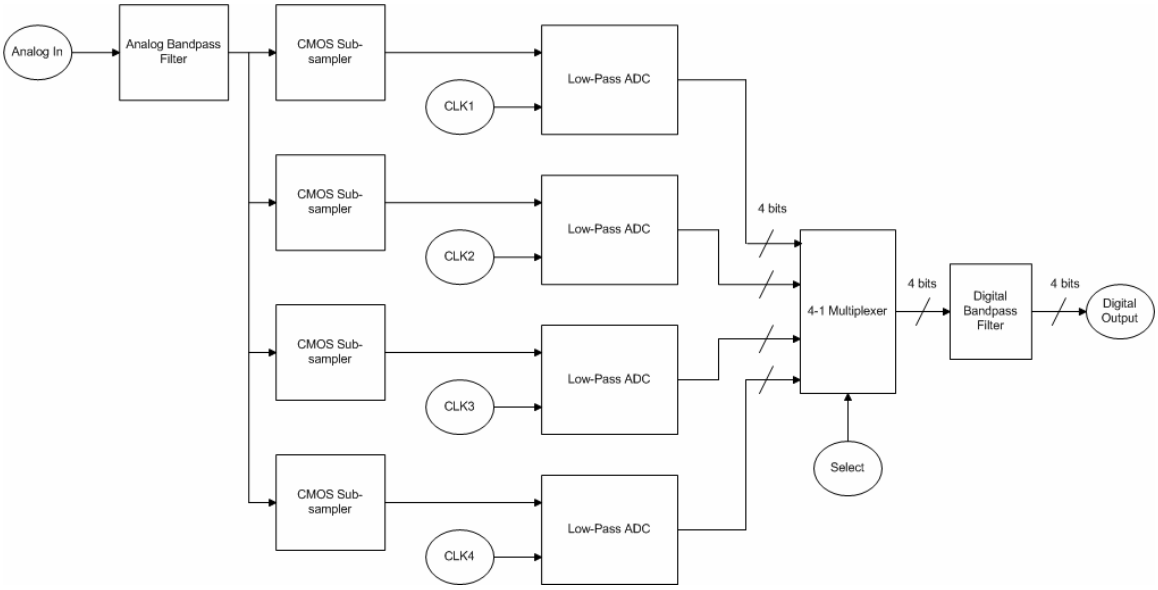

Figure 3 Parallel Time Interleaving Block Diagram

It can be seen in this diagram that four CMOS sub-sampling sample-hold (S/H) circuits and four ΣΔ modulators will be used, each of these pairs operating in parallel. The input signal will be passed to each of the four sub-sampling S/H circuits in order to be down-sampled to a lower frequency range. These circuits will operate at the same frequency as their respective ΣΔ modulator and with the same time delay. Each ΣΔ modulator will be offset by approximately one-fourth of a clock cycle. In this manner, the ΣΔ modulators will provide a digital output with the appropriate time delay. All four digital outputs will be recombined at the four bit four-to-one multiplexer which operates at four times the clock frequency of the individual ΣΔ modulators. This process will recombine the individual outputs of the ΣΔ modulators in the correct order, creating the digital equivalent of the input signal. In the PTI architecture, the input signal can be filtered and the down-sampled so that each ΣΔ modulator will only see the band-limited signal in a frequency range that is easily

accommodated with CMOS technology [6]. This is accomplished by the two blocks in the front end labeled Analog Bandpass Filter and CMOS Sub-sampler. These two blocks acting together serve to provide the four ΣΔ modulators with a band-limited, sub-sampled signal. The bandpass capability of the PTI ADC technique reduces the need for complex and expensive down-conversion hardware [6]. The bandpass capability is derived from band-limiting the input signals and then recombining the outputs from the individual ΣΔ modulators with the appropriate time delays. The user is able to input a signal in the RF range directly to the analog bandpass filter. Through the use of appropriate time delays and recombination in the circuit, the output will reflect the digital output of the input signal. Center frequencies in the RF range are achievable in this architecture without the need for the CMOS sub-circuits to operate in that frequency range. In fact, this process allows for each ΣΔ modulator to operate in a low-pass format. That is, each ΣΔ modulator will only receive the output from the front end band-limited signal that is decimated and will range from DC (0 Hz) to f_{BW}, the bandwidth provided by the front end filter. The front end analog bandpass filter and the sample-hold sub-sampling circuits were not researched in this project. These devices require careful calibration and fast responses as they must operate at high frequencies.

The effective sampling ratio of the PTI is much higher than the individual modulators and as a result can achieve higher center frequencies [7]. This translates to a significant increase in the frequency capability of the circuit while maintaining the noise shaping provided by the ΣΔ modulation [6].

The OSR of the PTI ΣΔ modulator-based circuit is still governed by the individual ΣΔ modulators. The OSR of the circuit is equal to the sampling frequency of the ΣΔ modulator divided by the bandwidth of

the digital bandpass filter. In this project, the OSR will be equal to 10. This is derived from a sampling frequency of 400 MHz and a bandwidth of 20 MHz.

The digital bandpass filter that follows the multiplexer was not researched in this project. This device, in combination with the front-end analog bandpass filter, can be used to select the frequency range from which to receive the input signal. The front-end bandpass filter allows the user to select the maximum frequency that the modulator will receive. Note that the maximum frequency is only relevant outside of the ΣΔ modulator, as the signal has been band-limited and down-sampled so that the ΣΔ modulator can operate in a lower frequency range.

The noise floor will be significantly attenuated in frequency bands at multiples of the modulator sampling frequency, such as fs, $2fs$ $3fs$ and similarly up to the number of stages. This allows the user to choose any of these regions as the operating bandwidth. These regions can be chosen by changing the sampling frequency of each channel of the PTI ADC. The signal can be extracted at any of the regions where significant noise attenuation occurs (except in cases of aliasing as in $2f_s$), so that the functionality of the ΣΔ modulator is maximized. This is illustrated in Figure 4.

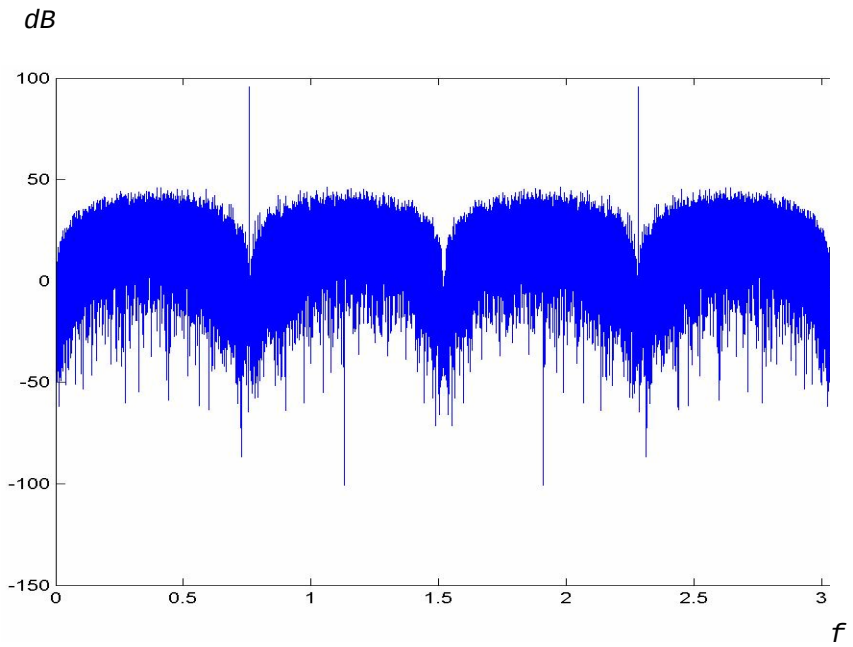

Figure 4 PTI Output Waveform

Attenuation occurs at multiples of the sampling frequency and the signal that is present in these regions. The output signal is filtered so that the quantization noise, which has been moved out of the frequencies near the signal by the noise shaping properties, can then be removed by the digital filter.

3 THEORETICAL SIMULATION RESULTS

Proof of concept was accomplished through the use of Matlab®. The PTI ΣΔ system was modeled in Simulink® and results generated. The system block diagram can be seen in Figure 3.

The circuit was simulated with a 2.28 GHz input signal and a bandwidth of 20 MHz. The clock frequency for each ΣΔ modulator was 760 MHz and the select frequency of the multiplexer was 3.04 GHz. It can be seen from the waveforms in Figure 4 that the circuit shaped the noise. The signal can be seen as a spike within a bandwidth near both one-fourth and three-fourths of the multiplexer select frequency. This corresponds to one-fourth and three-fourths of the effective sampling frequency, Mf_S. Also, one can see that the noise floor decreases in this region, as the ΣΔ modulator provides noise-shaping and pushes the noise out of the desired frequency band.

The results showed a Signal to Noise and Distortion Ratio (SINAD) of 70.61 dB and 11.44 effective bits at the output. These results indicate that the circuit is capable of performing well at higher frequencies.

4 HARDWARE IMPLEMENTATION

With the proof of concept complete, the task of building the bandpass ADC began. All schematic design was completed in Cadence®. First, basic gates were constructed. These gates include NAND, NOR, XOR, and the Inverter. Next, building blocks such as the D-Flip Flop, Sample Hold, Adder, Comparator, and Analog Buffer were constructed. Finally, larger circuits such as the Quantizer, Multiplexer, and Sigma Delta Modulator were constructed.

4.1 BASIC GATES

All basic gates, including AND, NAND, OR, NOR, XOR, and the Inverter were constructed and tested successfully in Cadence®.

4.2 BUILDING BLOCKS

Building on the basic gates, construction now began on the D-Flip Flop, Sample-Hold, Operational Amplifier, Adder, Comparator, and Analog Buffer.

4.2.1 D-Flip Flop

The D-Flip Flop (DFF) was constructed from inverters and pass gates. The circuit consists of a latch stage and a hold stage. The latch circuit consists of two inverters and two pass gates. The input to the DFF enters through a pass gate controlled by the clock (CLK). An input can only enter into the latch stage when the CLK is in the high state (is at logic “1”). After the signal passes through the

first pass gate, it then enters into a loop. The forward path of the loop consists of two inverters that serve to maintain the signal. This occurs when the CLK is in the low state (is at logic "0"). The feedback path on this loop is through a pass gate controlled by the inverse of the CLK signal, CLKB. When the clock goes low the loop is connected, and the signal is maintained by the two inverters and the feedback pass gate for the duration of CLKB. When CLKB is high (is at logic "1") the signal is transmitted through a pass gate that is the link between the latch stage and the hold stage and the signal that is latched by the first stage is passed to the hold stage. The hold stage is constructed identically to the latch stage, with two pass gates and two inverters. A signal that is passed into the hold stage on CLKB will become latched into the feedback path while CLK is high, as CLK is the signal controlling the feedback path pass gate. The feedback path pass gate and the inverters perpetuate the signal that was passed in during CLKB and present it to the output while CLK is high. In this respect, the signal that was latched during the initial CLK being high, is now present during the next CLK event. This fully defines the operation of the DFF [9]. The circuit schematic is shown in Figure 5.

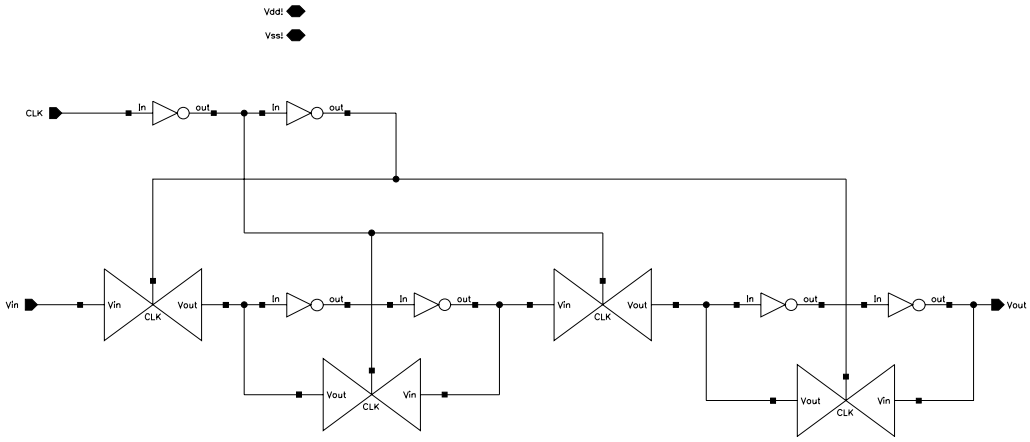

Figure 5 D Flip Flop Circuit Schematic

The performance of the DFF was evaluated with a CLK of 1 GHZ. The waveforms for the CLK, input signal, and output signal can be seen in Figures 6, 7, and 8 respectively.

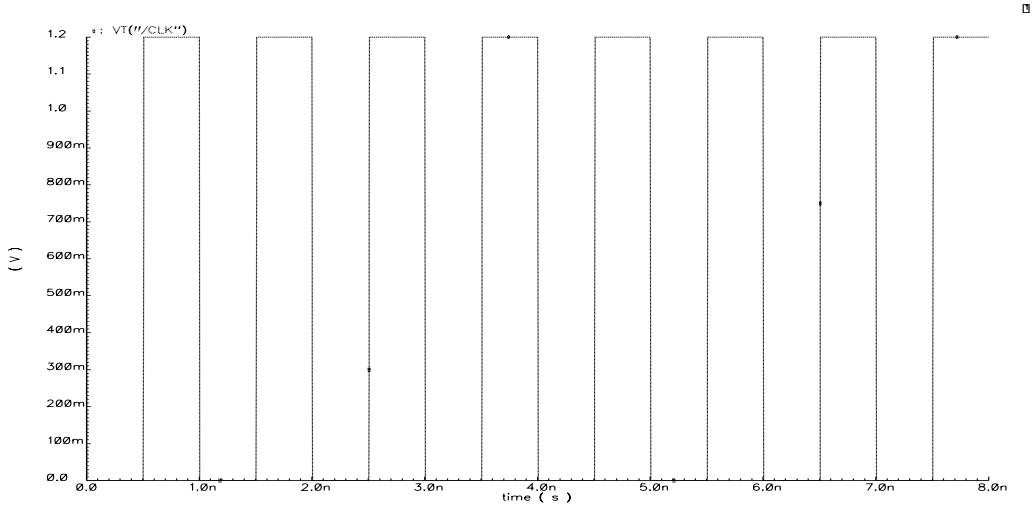

Figure 6 D Flip Flop CLK Waveform

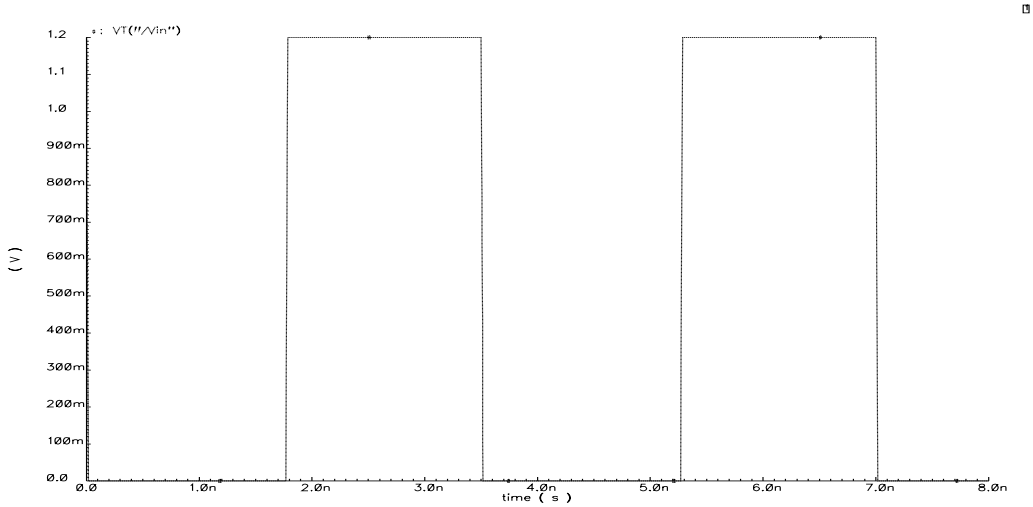

Figure 7 D Flip Flop Input Signal Waveform

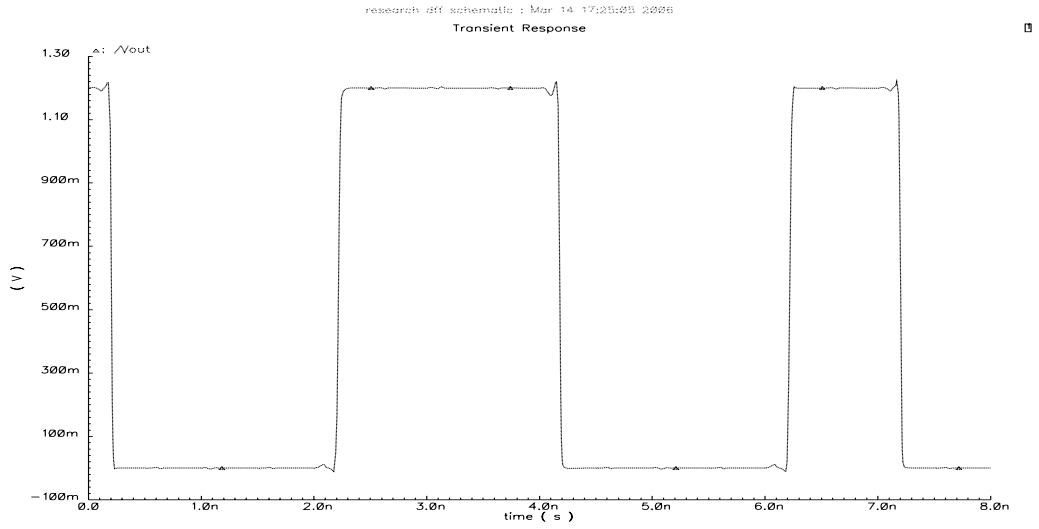

Figure 8 D Flip Flop Output Signal Waveform

4.2.2 Dummy Switch

A dummy switch was used in the S/H circuit. The dummy switch circuit attempts to mitigate the effects of charge injection. This will ultimately reduce the quantization error as less error is introduced in tracking the input voltage. This quantization error is a result of charge injection. Chare injection refers to induced voltage resulting from charge underneath the gates of the transistors leaking out to the circuit. This charge is transferred through the coupling capacitance from the gate to both the source and the drain [4]. This charge induces a voltage on the output of the switch reducing the accuracy of the circuit. In an attempt to reduce this effect, a dummy switch has been implemented. This circuit is comprised of two stages. The first stage consists of a pair of n and p-type transistors. They will work in tandem to pass the input voltage to their output. They are tied together at the source of the n-type and the drain of the p-type. They are also tied together at the drain of the n-type and the source of the p-type. The transistors are controlled by inverse

control signals at their gates so that they will conduct at the same time. Pairing the n and p-type transistors together is one method of reducing the effects of charge injection. This pair of transistors is then connected to another pair of n-type and p-type transistors that are shorted across their drain and source terminals. These two transistors are also controlled by inverse control signals. When transistors are shorted in a switch they are referred to as "dummy", because they simply transmit the input signal through. It is in this manner that they absorb any excess gate charge leaked from the first pair so that the output voltage is not affected. Another method implemented in this project to mitigate the effects of charge injection including using small switches to reduce the overall charge stored underneath each gate [4]. The circuit schematic can be seen in Figure 9.

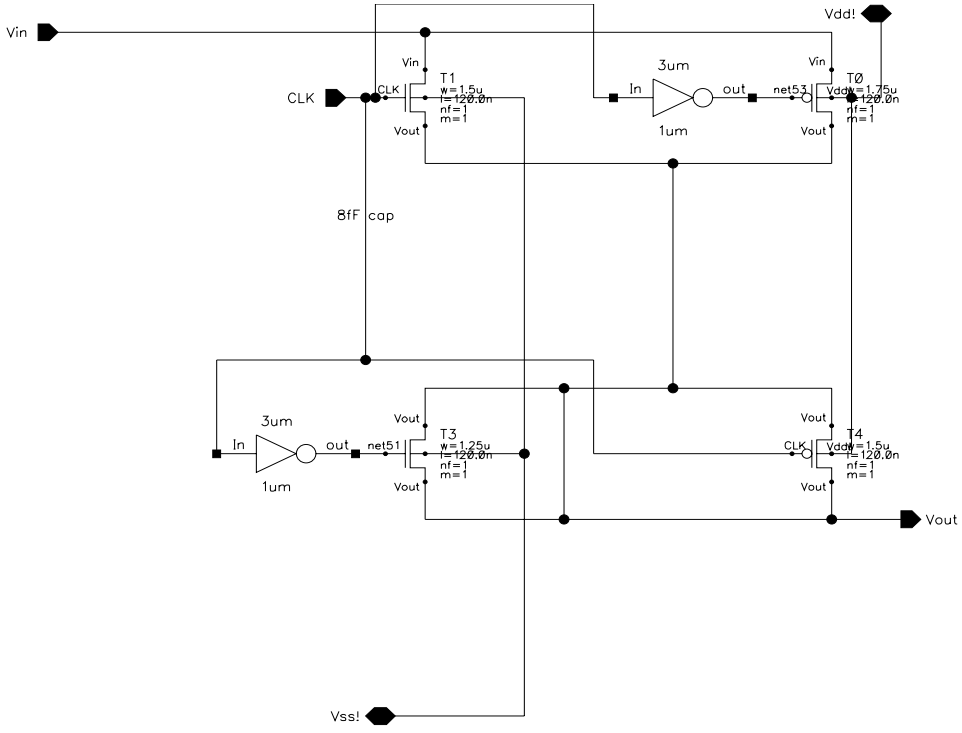

Figure 9 Dummy Switch Circuit Schematic

The performance of the S/H was evaluated with an input of 20 MHZ clocked at 250 MHz. The waveforms for the input and output voltages can be seen in Figure 10.

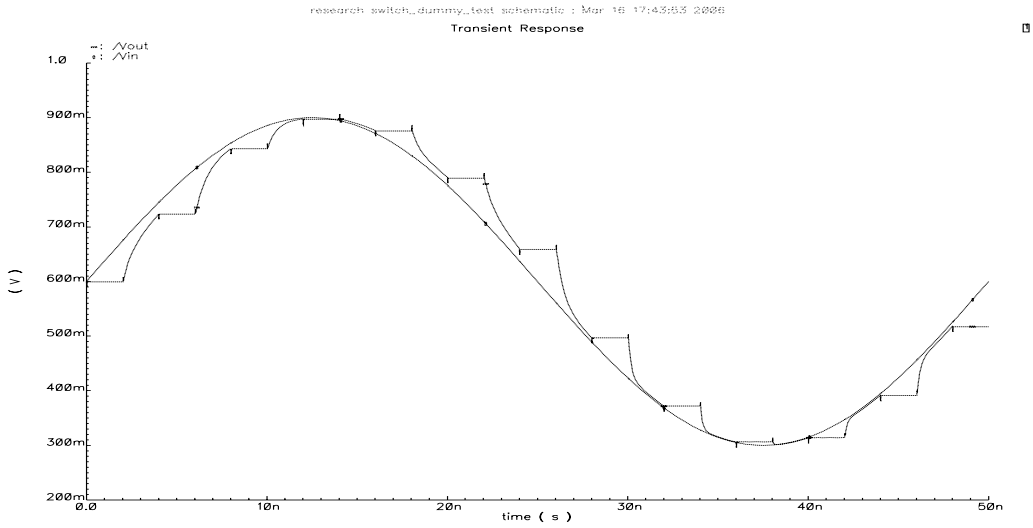

Figure 10 Dummy Switch Input and Output Signal Waveforms

4.2.3 Operational Amplifier

An operational amplifier was designed as several circuits will require its use including the S/H, analog adder, quantizer, and the sigma delta circuit. The operational amplifier consists of a differential pair followed by an output stage that yields higher gain. The sizing of the transistors is essential so that a phase margin greater than 60° is maintained for assurances of stability. A very high slew rate is also needed so that when used as an analog buffer, the operational amplifier will be able to follow the input signal. A high gain is essential when the operational amplifier is used in closed-loop form, as in the analog adder, so that the generalizations assuming the operational amplifier has infinite gain will hold. It

would be very difficult to achieve all of these goals with a single circuit and it was decided that two operational amplifiers would be designed. One would be concerned with analog operation and used in the analog adder, analog buffer, and S/H. The other would be suited for digital operation and would be used in the comparator.

4.2.3.1 Analog Operational Amplifier

Slew rate and open-loop gain are very important characteristics in the design of an analog operational amplifier. The analog operational amplifier must be able to approximate the infinite gain of an ideal operational amplifier so that the analog circuits will perform correctly in closed-loop operation. The circuit schematic for the open-loop analog operational amplifier is shown in Figure 11.

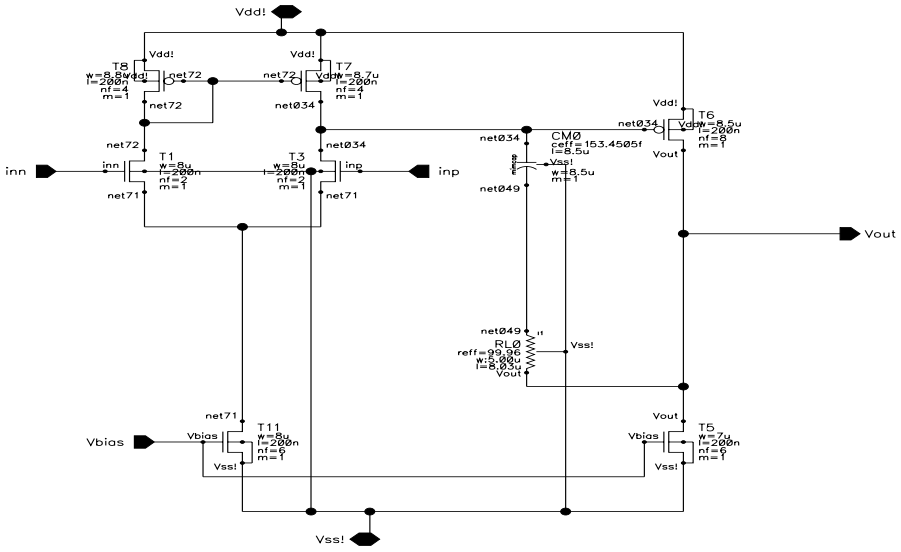

Figure 11 Open-Loop Analog Operational Amplifier Schematic

The first stage consists of a differential pair biased by a current source. Miller compensation is utilized between the first and second stage to increase the bandwidth of the operational amplifier

[3]. The second stage provides current gain that allows for the operational amplifier to drive larger loads. This operational amplifier will be utilized in the analog adder, analog buffer and the S/H circuit. The design of the analog operational amplifier was done using the criteria described in [4].

The performance of the analog operational amplifier was evaluated both in open-loop operation and with an AC sweep. The waveforms for the output voltage for open-loop operation can be seen in Figure 12.

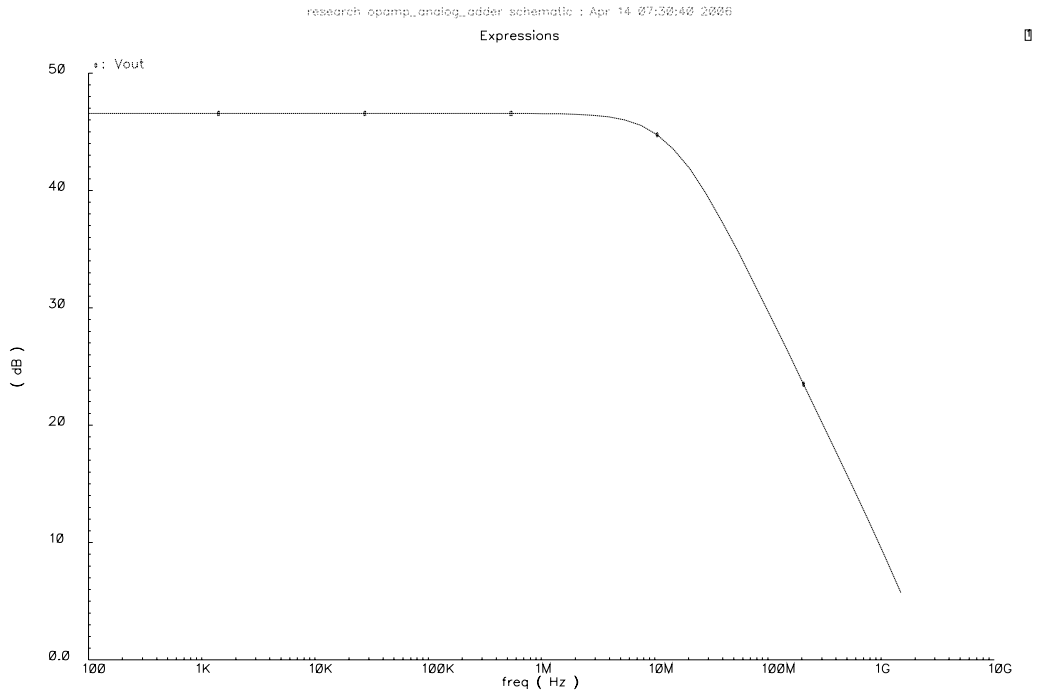

Figure 12 Open-Loop Analog Operational Amplifier Waveform

The open-loop gain was found to be 46.57 dB with a bandwidth of approximately 14.5 MHz. Closed-loop performance will be discussed in Section 4.2.4.

4.2.3.2 Digital Operational Amplifier

Phase margin was of the little concern during the design of the digital operational amplifier. The key component to the digital operational amplifier was slew rate. There is no need for the device to include Miller compensation. The concern with this circuit was the slew rate and the ability to drive a load. The digital operational amplifier must be able to quickly change between logic "1" and "0" when used as a comparator. Also, the load placed on each comparator will be comprised of two XOR gates and the digital operational amplifier will be required to drive those gates at sufficient speed. The schematic for the digital operational amplifier can be seen in Figure 13.

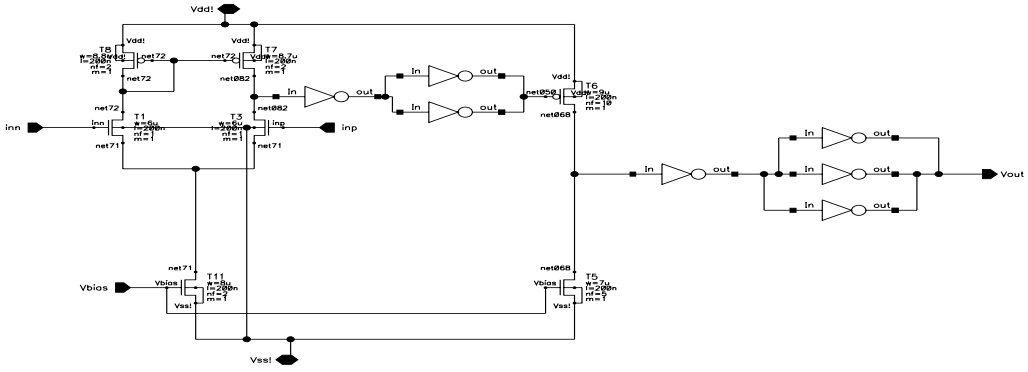

Figure 13 Digital Operational Amplifier Circuit Schematic

The digital operational amplifier consists of two main stages. The first stage is a differential pair. A buffer system resides between the first and second stage. The buffer system consists of three inverters arranged so that the first stage of the operational amplifier only drives a single inverter. The first inverter drives two more inverters that drive the operational amplifier output stage. The

second stage serves as a current source so that larger loads can be driven. The second stage is also buffered due to the demands of the XOR gates in the quantizer. The operational amplifier output stage drives a single inverter that in turn drives three inverters. In this manner, the digital operational amplifier is able to drive larger loads. The digital operational amplifier was designed using the criteria in [4], which ensure proper operation. The only exception is the removal of the Miller compensation, which was deemed unnecessary in digital operation. Correct operation of this circuit will be shown in Section 4.2.7.

4.2.4 Analog Buffer

The analog buffer was formed by operating the analog operational amplifier in unity gain configuration. In this setup, the operational amplifier will have unity gain. The waveform for the analog buffer can be seen in Figure 14.

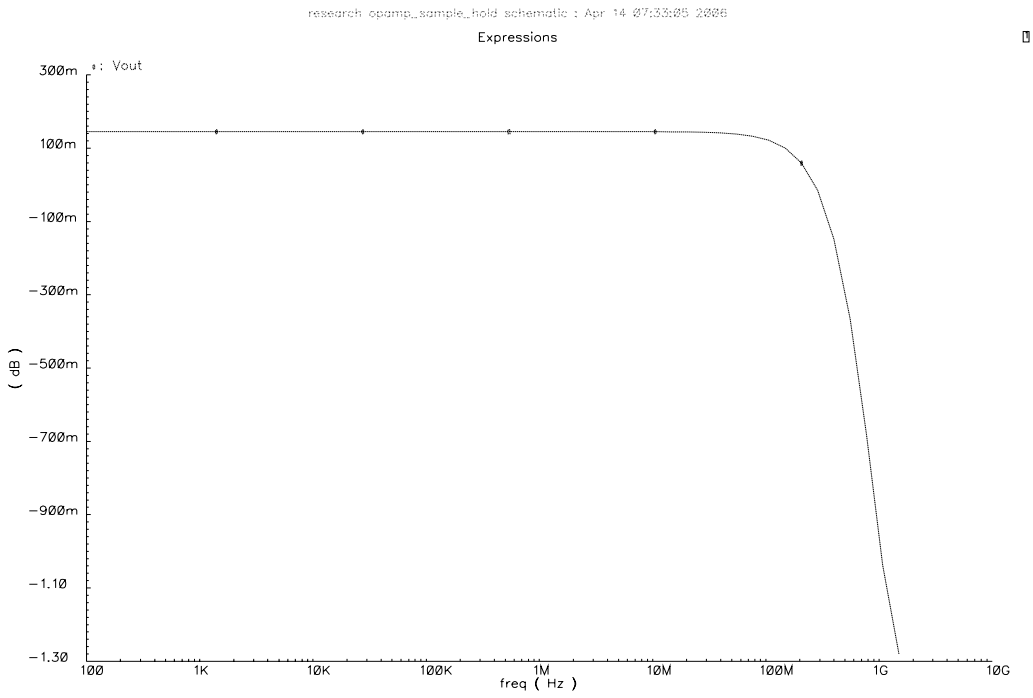

Figure 14 Closed-Loop Analog Operational Amplifier Waveform

The performance of the analog operational amplifier was evaluated in closed-loop operation with an AC sweep. The closed-loop gain was found to be approximately 0 dB with a corner frequency of beyond 1 GHz.

4.2.5 Sample Hold

The S/H is implemented as a two-stage device. The first stage is the dummy switch and the second stage is an analog buffer. The buffer, the analog operational amplifier in unity gain configuration, shields the dummy switch from loading so that the input signal can be followed accurately. The circuit schematic for the S/H circuit can be seen in Figure 15.

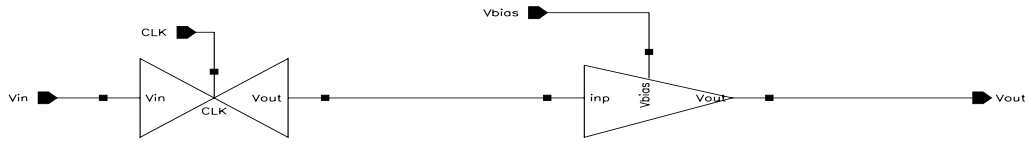

Figure 15 Sample Hold Circuit Schematic

The performance of the S/H was evaluated with an input of 20 MHZ clocked at 250 MHz. The waveforms for the input and output voltages can be seen in Figure 16.

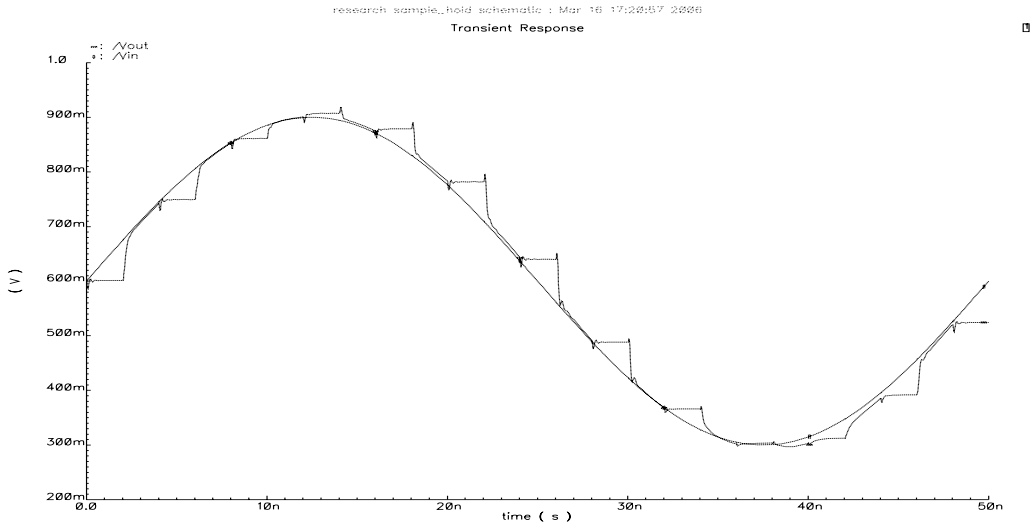

Figure 16 Sample Hold Input and Output Signal Waveforms

4.2.6 Adder

An adder circuit was constructed utilizing the previously mentioned analog operational amplifier circuit as well as resistors.

The analog operational amplifier was utilized in closed-loop form and the output will adhere to Equation 6.

$$V_{OUT} = \left(1 + \frac{R_F}{R_S}\right)\left(\frac{V_A + V_B + ... + V_N}{N}\right)$$

Where

N = number of input sources

Equation 6 Analog Adder Function [3]

The feedback resistor was set to 5.75 kΩ. The source resistance was set to 3.0 kΩ. Each resistor with the voltage sources were set to 3.0 kΩ. The output of the adder was then equal to the sum of the three input voltages.

It was of interest to have an analog adder with a common voltage of 0.6 V. This was achieved by connecting the positive terminal of the analog operational amplifier to 0.6 V through R_S. In this manner, voltages can be added with a common reference. Voltages less than the reference voltage are deemed negative and voltages greater than the reference voltage are deemed positive. The circuit schematic is shown in Figure 17.

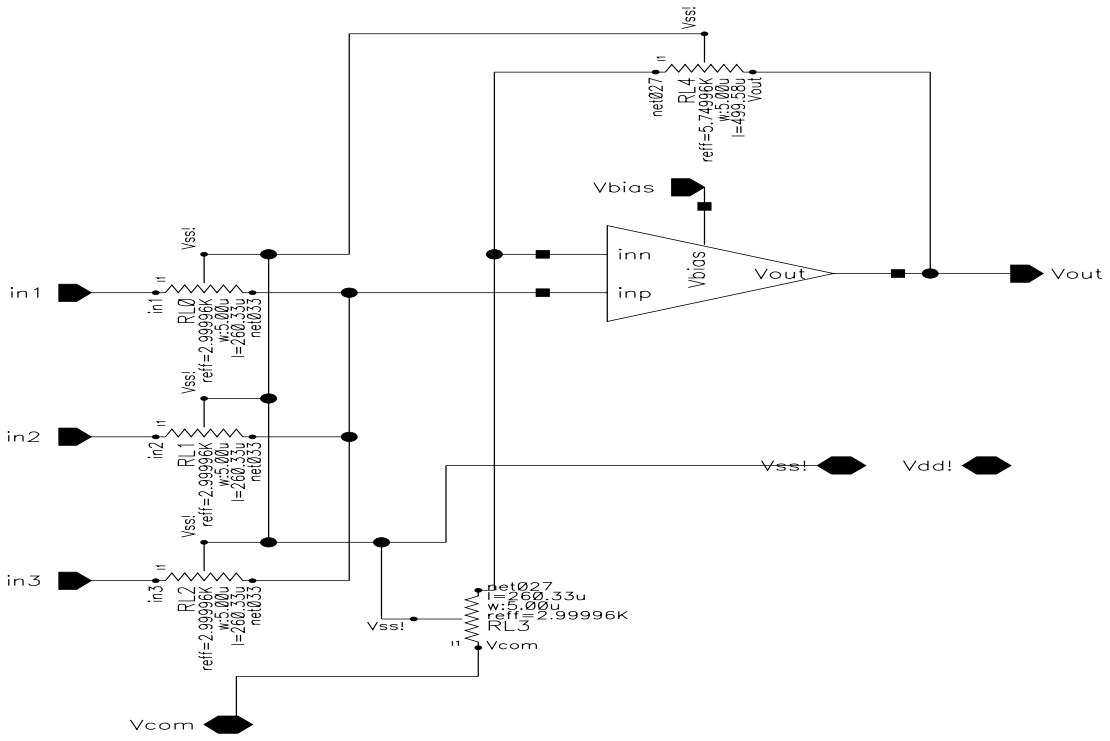

Figure 17 Analog Adder Circuit Schematic

The performance of the analog adder was evaluated with an input of 100 MHZ. The waveforms for the input voltages and output can be seen in Figure 18.

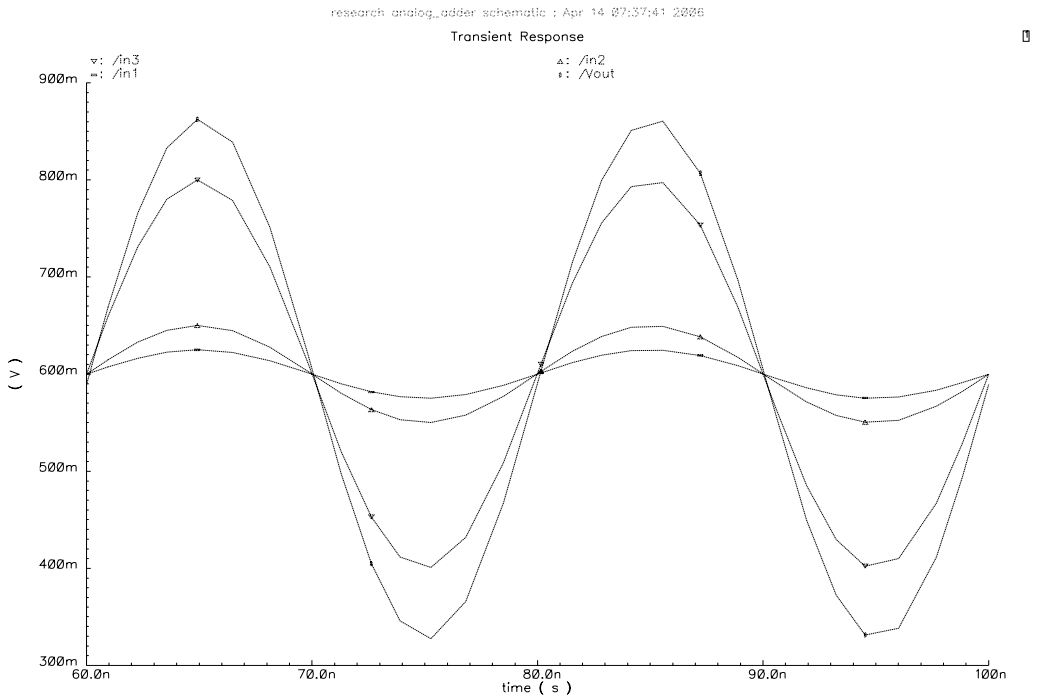

Figure 18 Analog Adder Input and Output Signal Waveforms

One can see that the reference voltage is 0.6 V and the input voltages are added with respect to 0.6 V. This is the proper operation as the assumption is that all inputs to the circuit will be biased at 0.6 V.

4.2.7 Comparator

A comparator was designed for use in the quantizer. A comparator consists of an open-loop operational amplifier and evaluates the voltage levels at the two inputs and selects the output accordingly. A digital "0" is selected as the output of the comparator if the voltage level at the negative input terminal is greater than the voltage level at the positive input terminal. Conversely, a digital "1" is selected as the output of the comparator if the voltage level at the positive terminal is greater than the voltage level at the negative

terminal. This circuit is used internal to the Flash ADC in order to create the digital output and the analog feedback signals.

The performance of the comparator was evaluated with two inputs. One input is a constant DC voltage of 400 mV. This is similar to operation inside the quantizer where the reference voltage is developed by a resistor tree. This input voltage is connected to the negative terminal of the operational amplifier. The other input simulates a varying input voltage and is centered at 300 mV with amplitude of 200 mV and a frequency of 16.67 MHZ. This input is connected to the positive terminal of the operational amplifier. The waveforms for the input voltages and output can be seen in Figure 19.

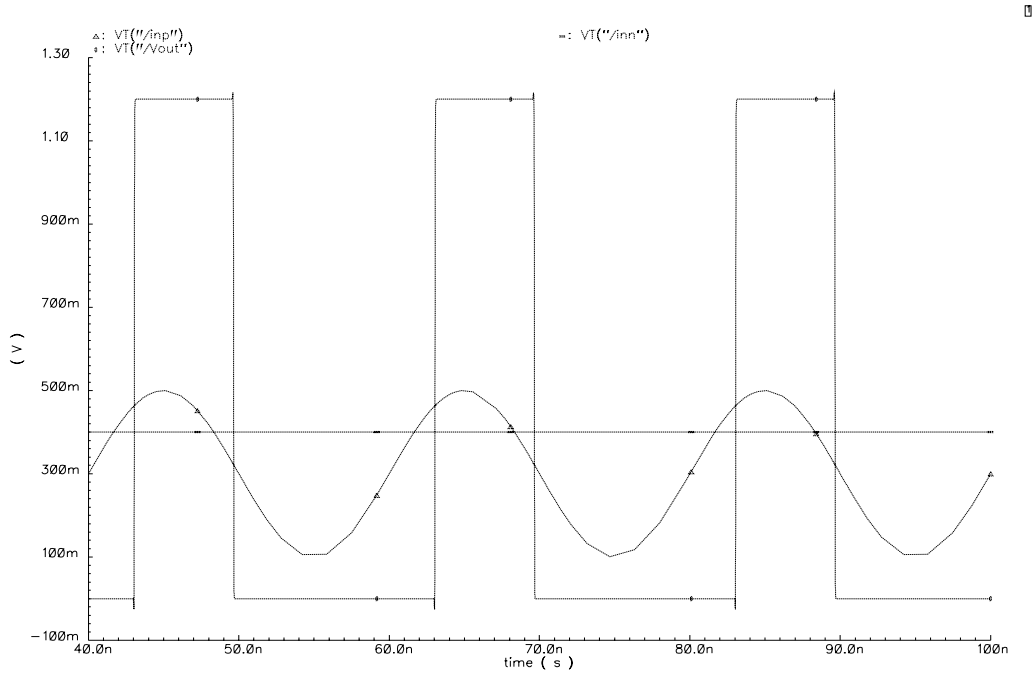

Figure 19 Comparator Input and Output Signal Waveforms

4.2.8 Quantizer

The quantizer is used inside the ΣΔ loop in order to create the digital output as well as the analog feedback signal. A flash ADC was implemented consisting of a resistor tree, comparators, XOR gates, OR gates, transmission gates, and DFFs. A flash ADC is characterized as having a direct conversion in which a comparator is utilized for each discrete level of the digital output [4]. This configuration provides the fastest conversion as the input is directly converted into its digital equivalent instead of through successive approximation. The flash ADC is limited in output resolution due to its relatively large footprint. The large area required for a Flash ADC is due to the number of comparators required as shown in Equation 7.

$$C = 2^n - 1$$

Where

C = number of comparators

And

n = number of output bits

Equation 7 Comparator Requirement [2]

This stage is then followed by combinational logic in order to decode the output of the comparators. While this circuit provides the fastest conversion time, limitations arise in output resolution, space requirements, and circuit complexity [2]. This design was chosen for the internal ADC due to its fast response to input signals and the need for only four bits of resolution. The circuit is also utilized as a DAC by using the encoded input signal. This signal selects the appropriate transmission gate that is tied to a second resistor tree to

provide the correct output voltage. In a ΣΔ modulator, the inverse of the digital output is transmitted back to the input so that this signal is subtracted from the delayed input signal. The quantizer serves as both a DAC for the analog feedback signal as well as an ADC for the digital output signal. The circuit schematic of the quantizer can be seen in Figure 20.

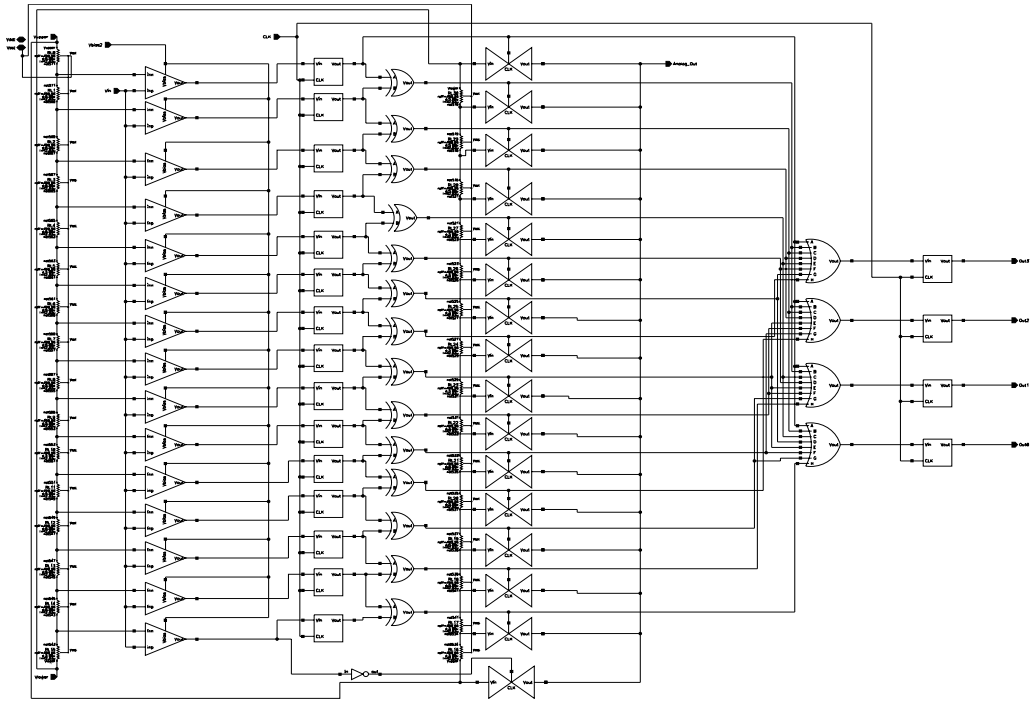

Figure 20 Quantizer Circuit Schematic

The performance of the quantizer was evaluated with an input of 20 MHZ clocked at 250 MHz. The waveforms for the input and output voltages can be seen in Figure 21.

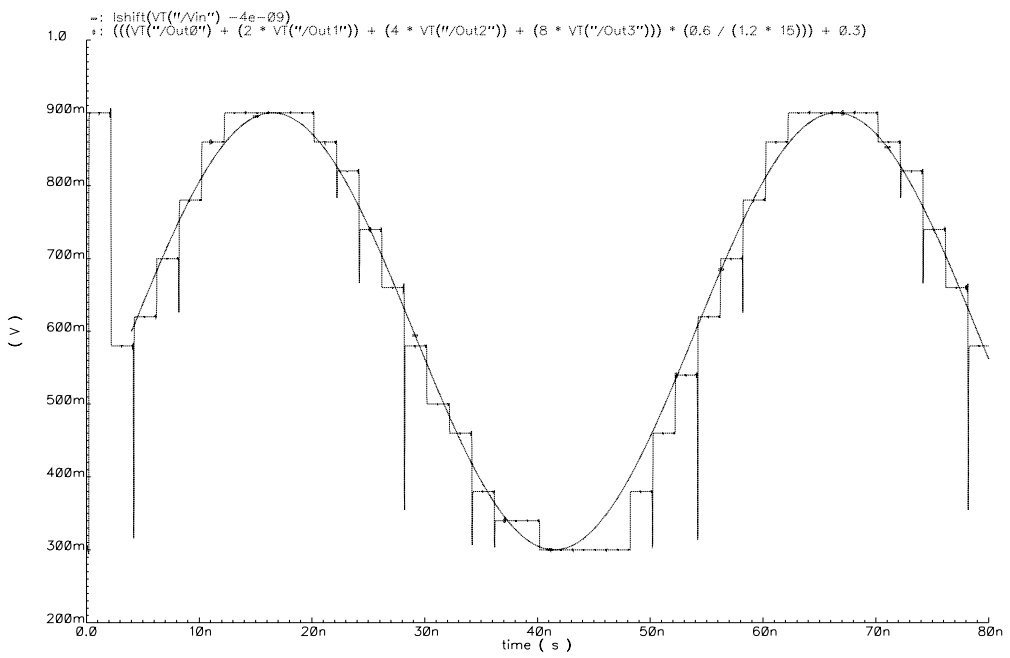

Figure 21 Quantizer Input and Output Signal Waveforms

4.2.9 Sigma Delta Modulator

A ΣΔ modulator serves as the basis of the ADC. Oversampling and noise shaping yield a higher output resolution with less overall hardware compared to other converters including flash-based ADCs. In this project, four ΣΔ modulators will be time interleaved so that the recombination of the individual components will yield the correct results and the individual circuits do not need to operate at the input signal frequency. In this manner, cost savings can be achieved through the use of CMOS technology and less demanding specifications for hardware design [6]. The block diagram of the ΣΔ modulator can be seen in Figure 1. The circuit consists of a forward loop and a feedback loop. The forward loop consists of an analog adder (combining the two individual adders into a single three input adder), an integrator, and a quantizer. The integrator simply follows the input and feeds that signal back to the adder. The quantizer serves two purposes. The quantizer consists of both a DAC and an ADC. The ADC portion of the ΣΔ

modulator is comprised of a Flash ADC which provides the digital output. The quantizer was also designed to provide the analog feedback used in the ΣΔ modulator feedback path. It is necessary to perform the conversion of the feedback signal because in this project each ΣΔ modulator has four bit resolution. If the ΣΔ modulator had single bit resolution then a wire would suffice as the feedback signal, containing the analog equivalent of either a logical "1" or "0". In the case of four bits, one must perform the ADC of the output signal to find the analog equivalent and then feed that back to the input where it is subtracted. The subtraction was realized through inverting the analog feedback signal by reversing the rails on the resistor tree inside the quantizer. This inverted signal can be fed back to the input signal. This feedback signal is delayed by one clock tick due to the delay in combinational logic. This allows for the integrator signal and the feedback signal to arrive at the adder at the same time, effectively cancelling out and leaving the input signal to be tracked by the ΣΔ modulator [4]. The circuit diagram is shown in Figure 22.

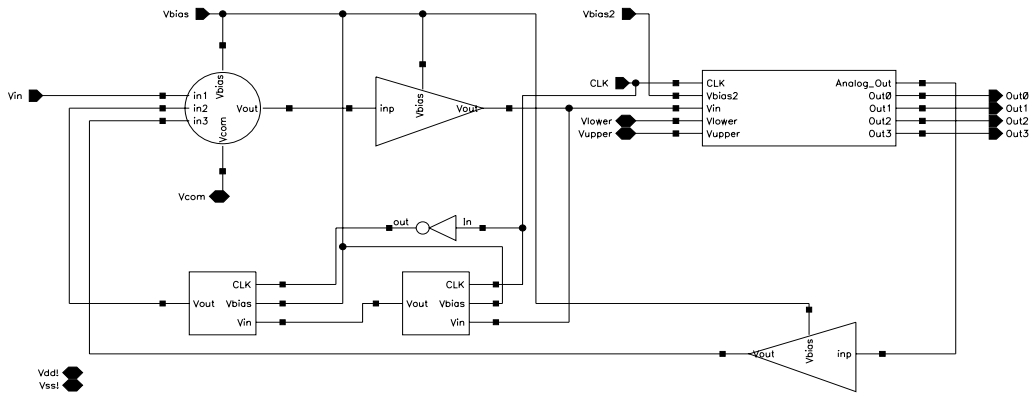

Figure 22 Sigma Delta Modulator Circuit Schematic

In order to isolate the quantizer and adder from large loads, analog buffers were utilized. The integrator loop is formed by two S/H circuits operated by the inverse clock signal so that the input signal is fed back to the input with one clock delay.

The performance of the ΣΔ modulator was evaluated with an input of 1 MHZ clocked at 400 MHz. The waveforms for the input and output voltages for one cycle at 1 MHz can be seen in Figure 23. The four bit digital output of the modulators for one cycle at 1 MHz can be seen in Figure 24. The ΣΔ modulator was also evaluated with an input of 5 MHz clocked at 400 MHz. The waveforms for the input and output voltages for one cycle at 5 MHz can be seen in Figure 25. The four bit digital output of the modulators for one cycle at 5 MHz can be seen in Figure 26.

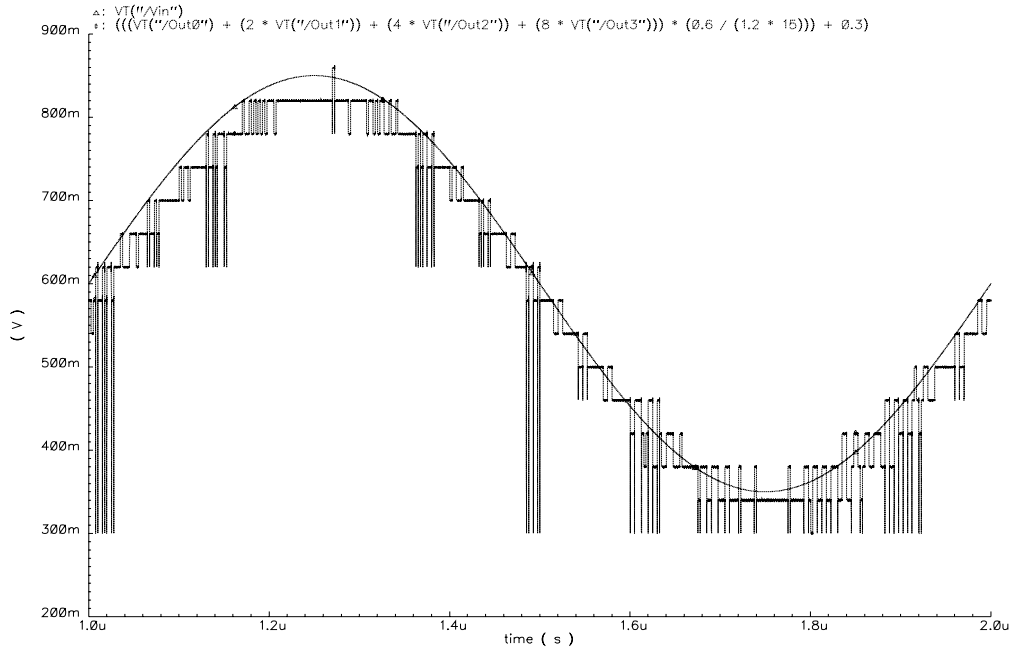

Figure 23 Sigma Delta Modulator 1 MHz Input and Output Signal Waveforms

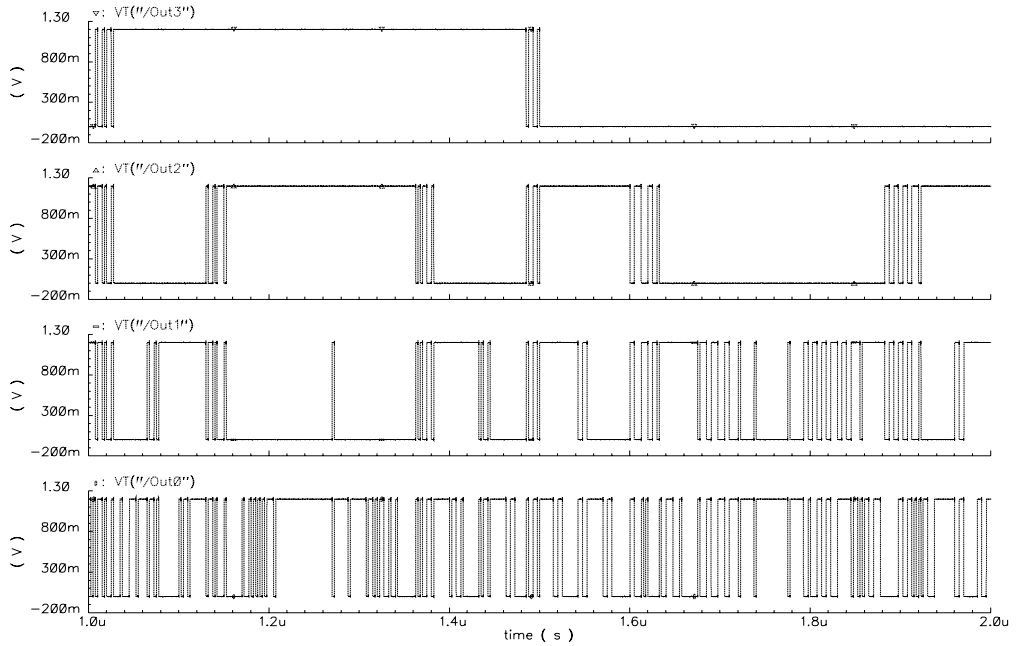

Figure 24 Sigma Delta Modulator 1 MHz Digital Output Signals

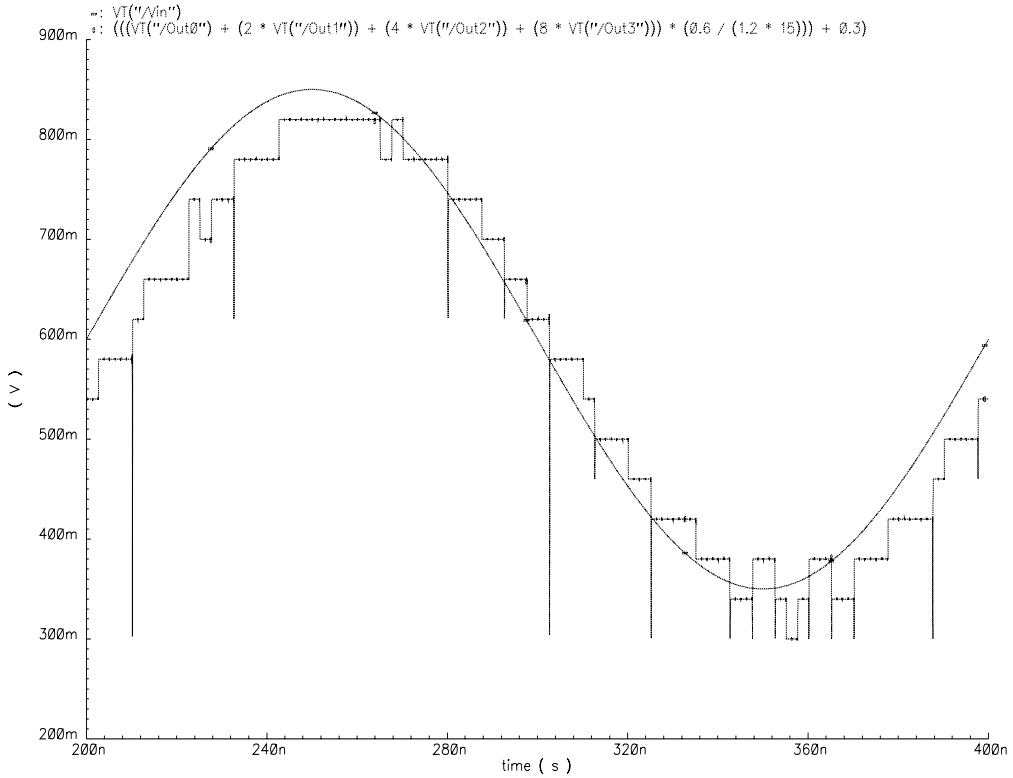

Figure 25 Sigma Delta Modulator 5 MHz Input and Output Signal Waveforms

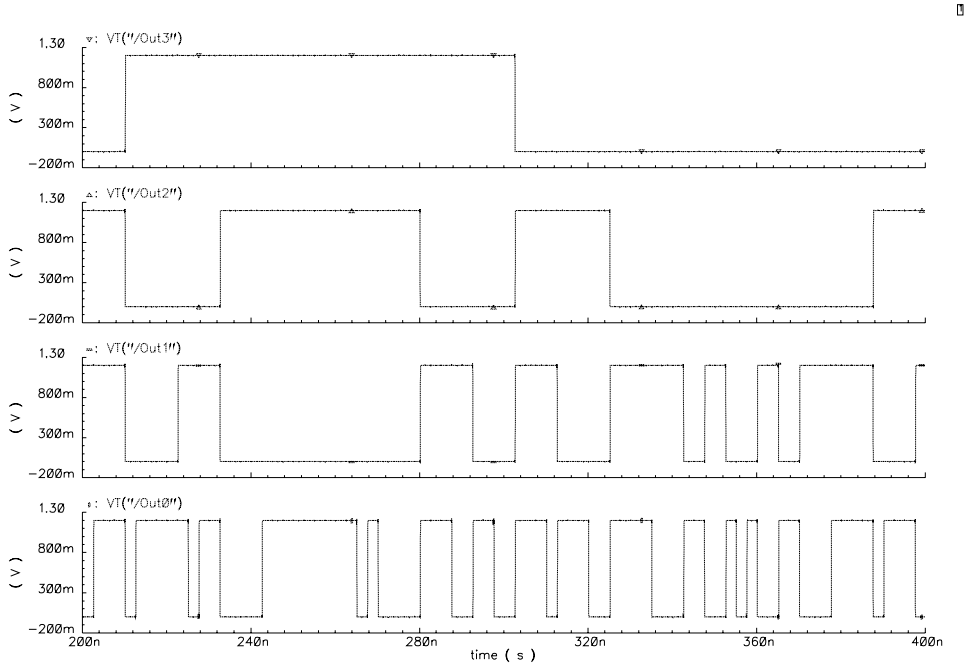

Figure 26 Sigma Delta Modulator 5 MHz Digital Output Signals

This circuit has a slight tendency toward the Vss rail (0 V). This may result from offset error in the integrator, quantizer, or operational amplifier. Further research can be done to optimize these circuit components and eliminate the bias of this circuit. This would result in increased performance and less quantization noise.

4.2.10 Multixplexer

In order to recombine the outputs of each ΣΔ modulator, a multiplexer was designed. This multiplexer has to be n inputs, where n is the number of ΣΔ modulators that are time-interleaved. In this project, n = 4. A simple multiplexer of combinational logic with two select signals was constructed. The truth chart can be seen in Table 1.

Select Signals	Output
S0 = 0, S1 = 0	A
S0 = 1, S1 = 0	B
S0 = 0, S1 = 1	C
S0 = 1, S1 = 1	D

Table 1 Multiplexer Truth Table [10]

From this truth table, the logic function can be evaluated and is shown in Equation 8.

$$F = \overline{S_0}\,\overline{S_1}A \mid S_0\overline{S_1}B \mid \overline{S_0}S_1C \mid S_0S_1D$$

Equation 8 Multiplexer Logic Function

The multiplexer was constructed of AND and OR gates. Each input was ANDed with the correct combination of the select signals and then the outputs of the AND gates were all ORed together in order to realize the circuit [10]. The circuit schematic for the multiplexer can be seen in Figure 27.

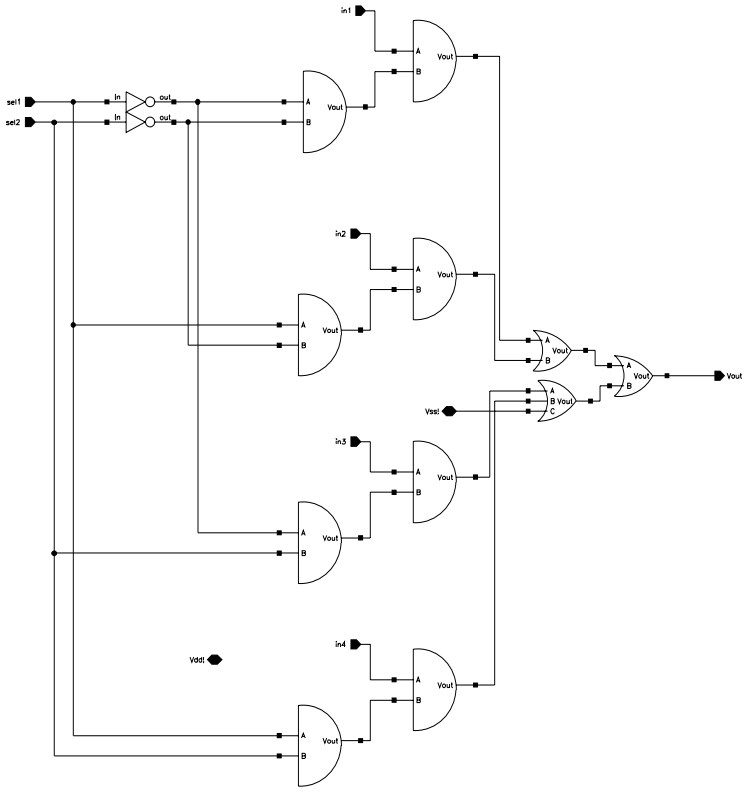

Figure 27 Multiplexer Circuit Schematic

The performance of the Multiplexer was evaluated with two select inputs. One select operates at 1 GHz while the other operates at 2 GHz. The waveforms for the output voltage and select signals can be seen in Figure 28.

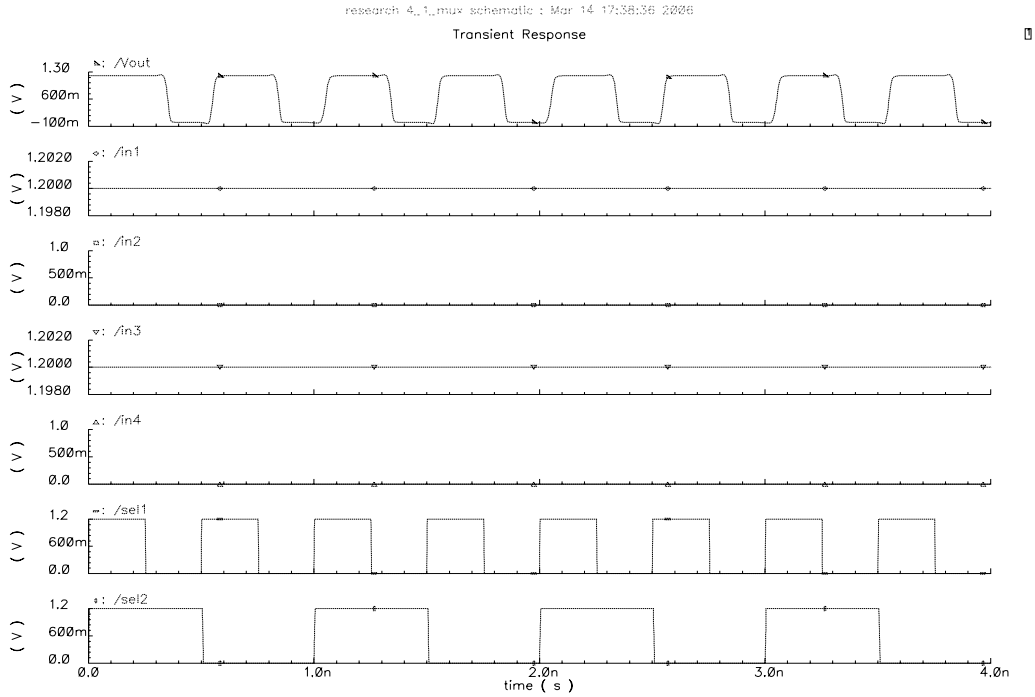

Figure 28 Multiplexer Control and Output Signal Waveforms

4.2.11 Counter

A circuit that was capable of controlling the select signals for the multiplexer was needed. This is due to the requirement that the multiplexer operate at n times the frequency of each individual ΣΔ modulator, where n is the number of ΣΔ modulators being time-interleaved. In this case, the multiplexer was required to operate at four times the ΣΔ modulator clock frequency of 400 MHz, or 1.6 GHz. A two bit counter was implemented that will translate the clock signal into a two bit discrete signal. This two bit signal will control the multiplexer so that each ΣΔ modulator is selected at the appropriate time. The circuit consists of one AND gate, two XOR gates, and two DFFs. Design of this circuit was based on criteria posed in [10]. The analysis of this circuit forces assumes an initial condition for both inputs of being logic "0" with the enable being logic "1". This defines State 0 where Out0 is logic "0" and Out1 is logic "0". If this

is the case, then the first XOR gate will have inputs of logic "0" from the feedback of the output and logic "1" of the enable. This causes a logic "1" to appear at the first output one clock tick later. The second output would have been logic "0", as the AND gate would have passed a logic "0" and the feedback of the assumed second output would have been logic "0". This defines State 1 where Out0 is logic "1" and Out1 is logic "0". At the next clock tick, the inputs to the first XOR gate would be a logic "1" from the enable and a logic "1" from the first output. This causes a logic "0" to be passed to the first output at the next clock tick. The AND gate receives a logic "1" from both the enable and the feedback of the first output. This causes a logic "1" to appear at the second XOR gate from the AND gate as well as a logic "0" from the feedback of the second output. This in turn causes a logic "1" to appear to the second output at the next clock tick. This defines State 2 where Out0 is logic "0" and Out1 is logic "1". At the next clock tick, the inputs to the first XOR gate are a logic "1" from the enable and a logic "0" from the feedback of the first output. This causes a logic "1" to appear at the first output one clock tick later. The inputs to the AND gate are a logic "1" from the enable and a logic "0" from the feedback of the first output. This causes a logic "0" to appear at the input of the second XOR gate as well as a logic "1" appearing the other input of the XOR gate from the feedback of the second input. This causes a logic "1" to appear at the second output one clock tick later. This defines State 3 where Out0 is logic "1" and Out1 is logic "1". Lastly, both outputs will reset back to logic "0" at the next clock tick as all feedback paths are logic "1", causing both XOR gates to pass a logic "0" to both outputs one clock tick later. This returns the circuit to State 0 where both outputs are logic "0". The circuit utilizes CLK signal events to generate a two

bit count pattern. This will be used to control the select signals of the multiplexer so that the multiplexer will operate at four times the frequency of the individual ΣΔ modulators. The circuit schematic for the counter can be seen in Figure 29.

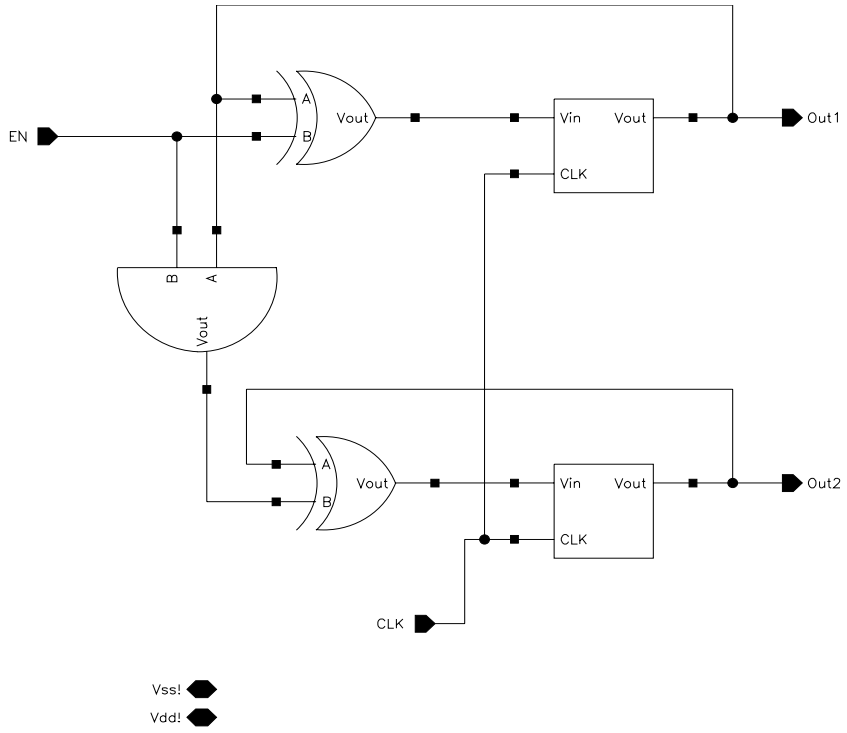

Figure 29 Counter Circuit Schematic

The performance of the Counter was evaluated with an input signal of 1 GHz. The waveforms for the input and output voltages can be seen in Figure 30.

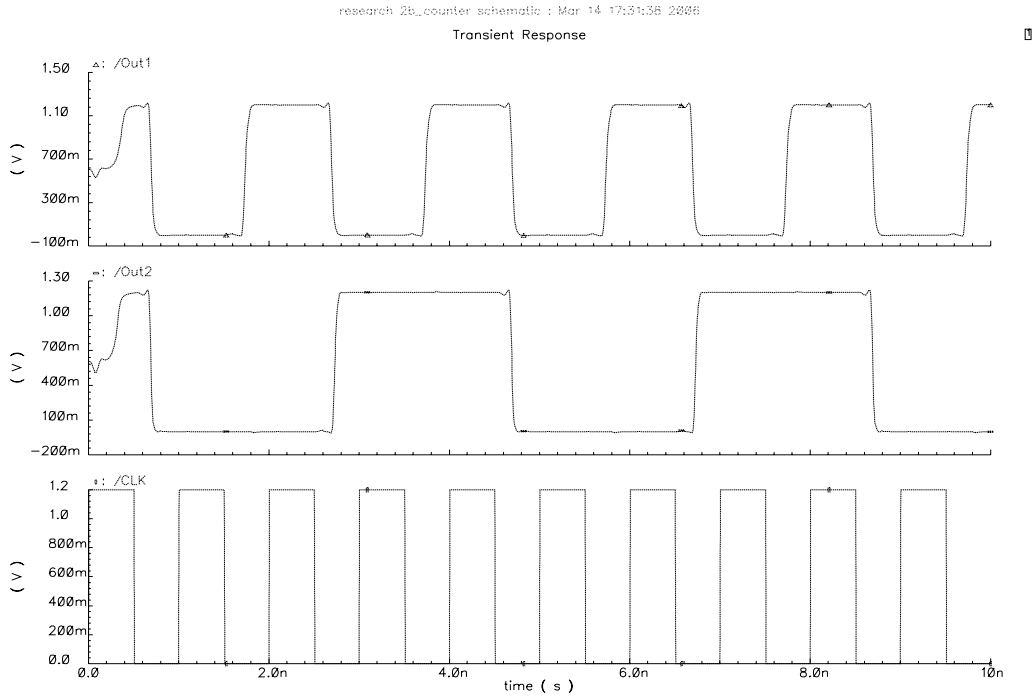

Figure 30 Counter Clock and Output Signal Waveforms

The glitch at the beginning of the circuit is the initialization of the output signals. The circuit changes from "00" to "01" to "10" to "11" and then resets to "00" and begins the count over again. This coincides with the revolving count required of the select signals.

4.3 Parallel Time Interleaved Analog-to-Digital Converter

The PTI ΣΔ modulator-based ADC was constructed. This circuit consists of four ΣΔ modulators linked in parallel. The outputs of each ΣΔ modulator are combined in time delays at the output. The delay for each channel is shown in Equation 9.

$$Delay(n) = \frac{n-1}{m * f_S}$$

Where m = *total number of* ΣΔ modulators

And

n = nth ΣΔ modulator

and

fs = clock frequency of each modulator

Equation 9 Channel Delay [6]

This equation states the delay for the *nth* ΣΔ modulator with respect to m ΣΔ modulators acting in parallel. For this project, the equation reduces to Equation 10.

$$Delay(n) = \frac{n-1}{4 * f_S}$$

Equation 10 Simplified Channel Delay

This shows that for f_S = 400 MHz, the delay of the first, second, third, and fourth ΣΔ modulators is 0.0 ns, 0.625 ns, 1.25 ns, and 1.875 ns respectively. This is the delay that is associated with the clock signal that is sent to each individual ΣΔ modulator. With this in place, each ΣΔ modulator will be sampling the input signal at the correct time-interleaved spacing. The effective sampling frequency and corner frequency are shown in Equation 11. The circuit schematic for the PTI ADC is shown in Figure 31.

$$f_{eff} = Mf_S$$

And

$$f_{NYQ} = Mf_S / 2$$

Where

f_{eff} = effective sampling frequency of the PTI ADC

And

M = total number of modulators being interleaved

And

f_S = sampling frequency of each modulator

Equation 11 Parallel Time Interleaved Effective Sampling Frequency and Corner Frequency [6]

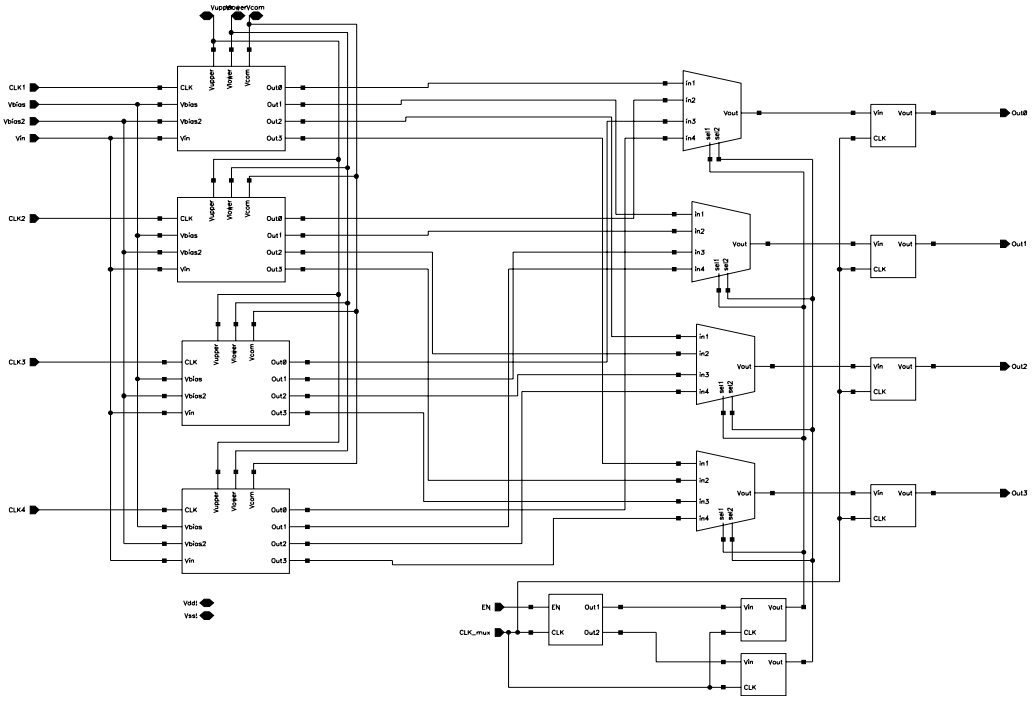

Figure 31 Parallel Time Interleaved Analog-to-Digital Circuit Schematic

The front-end sub-sampling S/H circuits were not researched. The goal of this research project was to show that the circuit was capable of receiving a much higher frequency signal at the front-end, acting on a sub-sampled version of this signal inside each ΣΔ modulator, and recombining the outputs with the correct time interleaving through the multiplexer so that the original signal is correctly reconstructed. In order to accomplish this without the front-end sub-sampling S/H circuit, four individual inputs were constructed such that they resemble an appropriate input. The difficulty is that creating a quantized signal inside Cadence® is non-intuitive. It was decided that four continuous signals with the correct phasing would be used in order to reconstruct this signal. In order to recreate a 399 MHz signal or 1.199 GHz (the two signals appear the same when sampled at 400 MHz), four 1 MHz signals were used as inputs to the system. These signals were assigned an appropriate phase according to Equation 12.

$$\theta_K = -\left(\frac{n}{4}360\right) - \frac{360n}{f_S}$$

Where

θ_K = the phase of the k stage sub-sampling S/H circuit in degrees

And

n = the number of the stage (1,2,3...)

And

f_S = the sampling frequency of the ΣΔ modulators

Equation 12 Input Phase Equation

So the delay of the stages will be -90.9°, -181.8°, and -272.7° respectively. These signals will provide the necessary signals to each stage to simulate a properly calibrate system of sub-sampling S/H circuits so that each ΣΔ modulator will see a 1 MHz signal properly time-interleaved and the output can be recombined to form a 399 MHz (or 1.199 GHz signal). The input signals were generated experimentally and are shown in Figure 32.

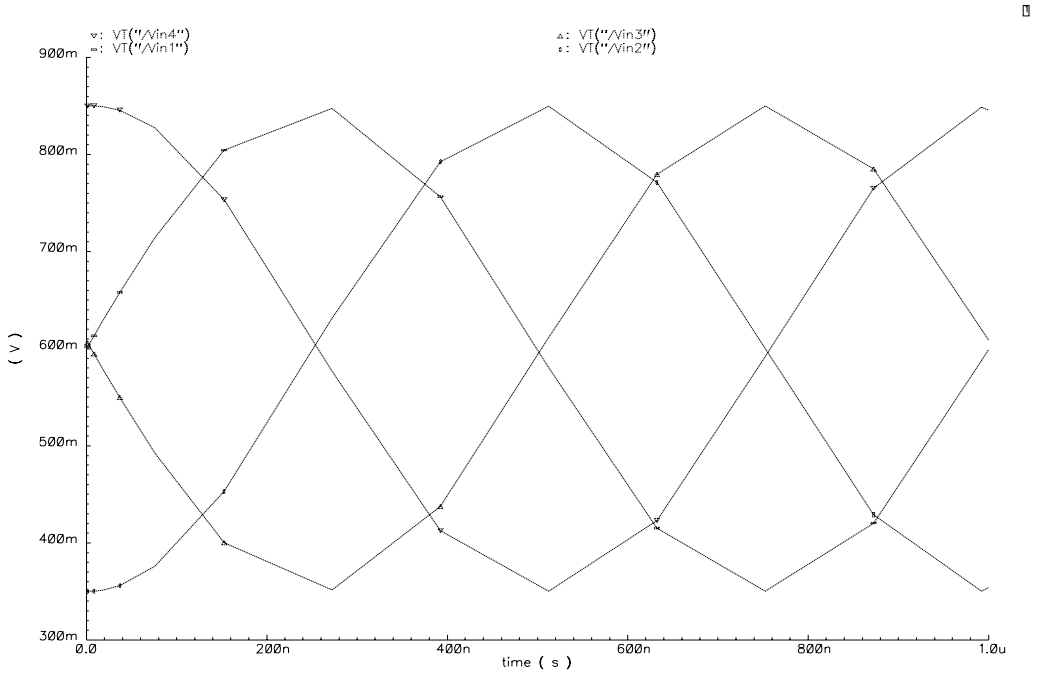

Figure 32 Phase-Delayed Input Signals

The signals are offset from each other by approximately one-fourth of a 1 MHz cycle. The recombination of these signals through the appropriate time delays will yield an output signal with the same frequency as the original input signal before sub-sampling. This recombination occurs by offsetting the clock signals on each ΣΔ modulator and correctly selecting the multiplexer outputs.

The performance of the PTI ADC was evaluated with four 1 MHz inputs appropriately phase-delayed to resemble a 399 MHz (or 1.199 GHz signal). Each ΣΔ modulator is clocked at 400 MHz and the multiplexer is clocked at 1.6 GHz. The waveforms for the input and output voltages can be seen in Figure 33.

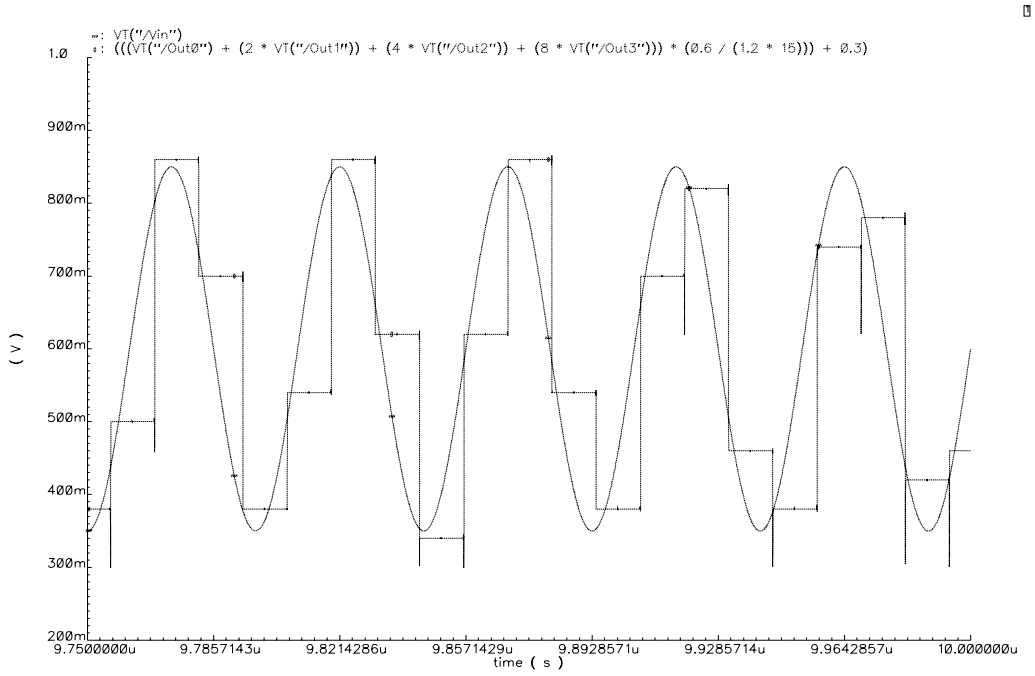

Figure 33 Parallel Time Interleaved Analog-to-Digital Input and Output Signal Waveforms

5 SIMULATION RESULTS

The PTI ΣΔ modulator-based ADC was constructed and evaluated with an input frequency equal to either 399 MHz (or 1.199 GHz). For simplicity, the input signal will be assumed to be 399 MHz. Each ΣΔ modulator is clocked at 400 MHz and the multiplexer is clocked at 1.6 GHz. The resultant OSR for each ΣΔ modulator is 10. This is due to each ΣΔ modulator operating in a bandwidth of 20 MHz with a sampling ratio of 400 MHz. A zoomed-in view of the input and output waveforms are shown in Figure 34.

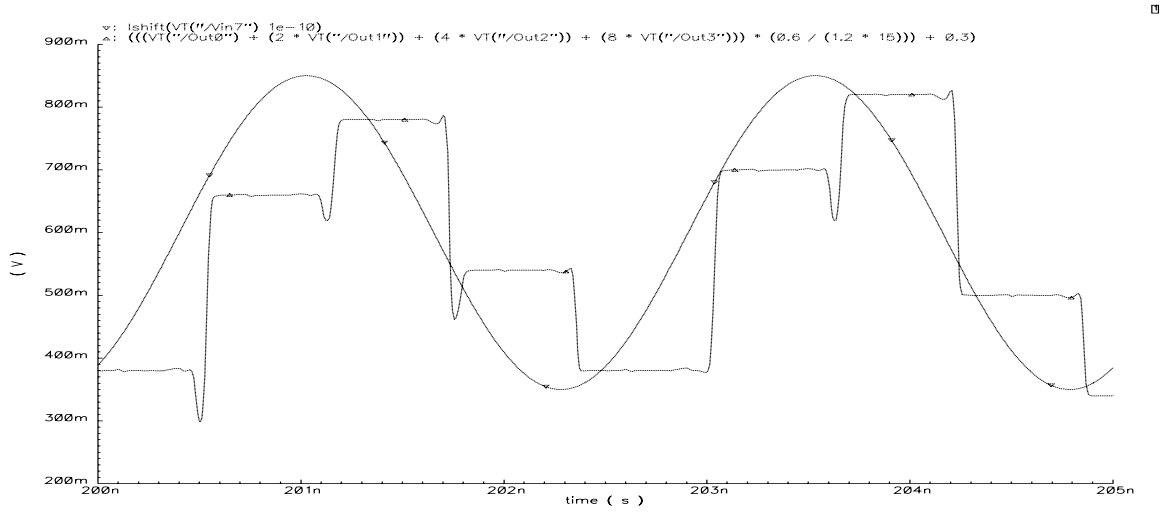

Figure 34 Parallel Time Interleaved Analog-to-Digital Converter Input and Output Signal Waveforms Zoomed-in View

The output of the PTI ΣΔ modulator-based ADC was allowed to run for an extended time (within system limitations of processor and

memory) and a Discrete Fourier Transform (DFT) was performed in order to extract the frequency content of the digitized output signal. This was done in order to evaluate the Signal to Noise and Distortion Ratio (SINAD) show in Equation 13.

$$SINAD = 10\log\left(\frac{S_x^{\,2}}{\sum S_e^{\,2}}\right)$$

Where

S_x = the amplitude of the signal in linear scale

And

S_e = the amplitude of each error signal in linear scale

Equation 13 Signal to Noise and Distortion [5]

Theoretical results in an ideal Matlab® environment indicate results of over 11 effective bits were possible at the output. Results in Cadence® will be unable to match these for multiple reasons. First, Matlab® fails to take into consideration the non-ideal characteristics of each circuit component. Also, Cadence® does not allow for easy DFT computation as frequency bins are correlated with the simulation run time ultimately limiting frequency bin resolution due to run time constraints. The DFT in dB scale of the output signal can be seen in Figure 35.

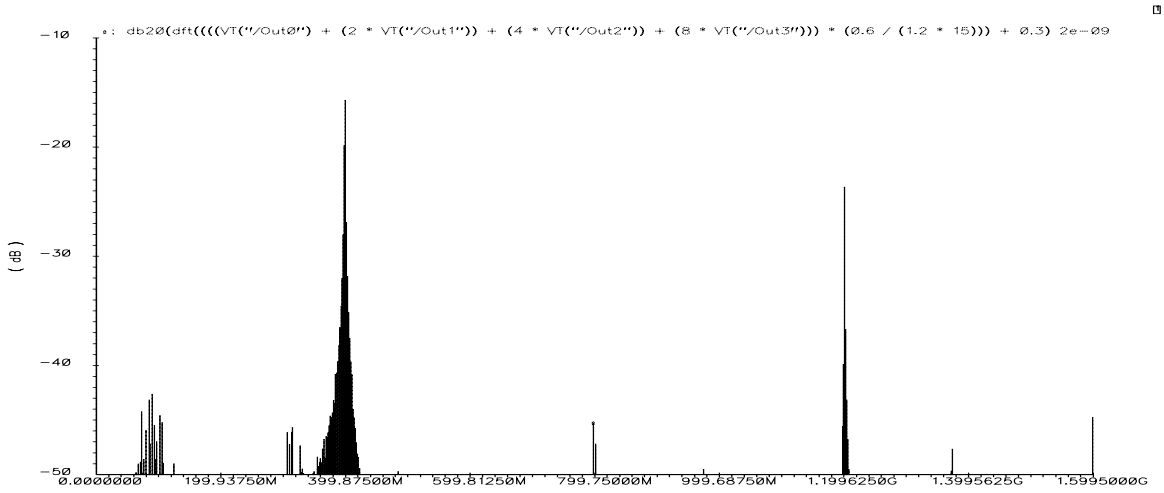

Figure 35 Parallel Time Interleaved Analog-to-Digital Discrete Fourier Transform Decibel Scale

Noise shaping occurs at multiples of the sampling frequency near 400 MHz and 1.2 GHz. There is a significant amount of signal that is spread over the frequency spectrum as the frequency bins in the DFT do not coincide with the format of the output signal. Utilizing Equation 10, the SINAD was estimated to be 36 dB. Assuming 6 dB of SINAD for bit of output resolution, the PTI ΣΔ modulator-based ADC was capable of approximately 6 bits of resolution.

Also note that the center frequency of the circuit is adjustable by combining a sampling frequency paired with the appropriate filtering. For instance, if a center frequency of 1.5 GHz is desired for the second Nyquist region (500 MHz in the first Nyquist region), a sampling frequency of 500 MHz must be utilized with the appropriate filtering. In this manner, the circuit can achieve flexible center frequencies.

6 CONCLUSIONS

The main objective of this project was to ascertain the capabilities of a PTI ΣΔ modulator-based ADC. This was accomplished in two stages. First, the system was modeled in Simulink© with ideal components to establish proof of concept. This experiment yielded promising results, with performance indicated by a SINAD of 70.61 dB and over 11 effective bits of output resolution. Secondly, the system was modeled in Cadence®. All sub-circuits were created using IBM® 0.13 µm technology and a working PTI ΣΔ modulator-based ADC was constructed. This circuit was evaluated for signal integrity at an operating frequency of 399 MHz (or 1.199 GHz) with each individual ΣΔ modulator clocked at 400 MHz and the multiplexer clocked at 1.6 GHz. The bandwidth was set at 20 MHz and was chosen due to its feasibility of implementation. After accounting for simulation limitations, real-world conditions, and DFT difficulties, the results show a SINAD of 36 dB which would yield 6 bits of output. This is in contrast to having only four bits of internal resolution in the Flash ADC. One can conclude that a ΣΔ modulator-based ADC is a feasible solution for achieving high resolution ADC at higher frequencies with reduced hardware and circuit complexity than through traditional conversion techniques such as flash and successive-approximation.

7 RECOMMENDATIONS

Future work should include further optimization of the sub-circuits, particularly the analog operational amplifier. The characteristics of the analog operational amplifier were chosen such that it would perform well in open or closed-loop operation. In order to achieve a wide bandwidth and fast slew-rate, this circuit became both large and power-hungry. It has been shown that non-ideal operational amplifiers can greatly affect the modulation process [14]. This includes not having sufficient gain in the circuit, offset voltage, and non-matching devices. These issues can result in a violation of the virtual ground concept at the terminals of the operational amplifier [11]. This property ultimately degrades the noise-shaping characteristics of the ΣΔ modulator [11].

Another very important characteristic in ΣΔ modulators is loop timing. It is essential that the analog feedback loop and the integrator signals arrive at the adder at precisely the correct timing. Further research into the delay inherent in the analog buffer in both the forward and feedback paths may yield insight into adequate compensation to ensure correct loop timing.

The PTI ΣΔ modulator-based ADC that was constructed assumed the correct operation of two key components. These include a front end S/H and sub-sampling circuit and a decimation filter on the back end. The S/H and sub-sampling circuit would perform the necessary down-conversion for the ΣΔ modulators to operate in a reduced frequency environment that is suitable for CMOS devices. This down-sampling is

essential to realize the cost savings associated with reduced circuit complexity and CMOS implementation. This circuit must be researched and optimized for use at high frequencies.

The decimation filter at the back end of the PTI ΣΔ modulator-based ADC typically occupies most of the die area and consumes the majority of the power [4]. Recent work has been done in this area concerning optimization of the performance, power, and size constraints [15]. This filter attenuates the quantization noise, band-limits the output signal, and suppresses extraneous out-of-band signals [4]. This filtering ultimately allows the circuit to realize the noise-shaping benefits. This is because the noise signal that has been pushed out of the frequencies of interest can now be removed entirely by a suitable high-pass filter. Research can be done in this area to reduce the circuit complexity, reduce the footprint, and increase overall resolution by reducing extraneous noise sources.

Another possible method of implementation for the back-end filter is to implement filters on each individual ΣΔ modulator channel. The output signal for each ΣΔ modulator could be filtered in order to remove all quantization noise prior to recombining the signals together to form the output signal. Research into this area may yield performance improvements, but consideration will have to be given to other noise sources that remain in the circuit including the high frequency switching of the multiplexer. Also, this implementation requires four individual filters which may ultimately occupy a larger area than a single, more robust filter. Research into this may lead to decreased size and/or increased performance.

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