Wright State University

CORE Scholar

Winter 2005

CEG 820-01: Computer Architecture II

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CEG 820 Computer Architecture II

Winter Quarter, 2005

Description : Continuation of CEG720 with more details on multiprocessor systems, parallel processing, and performance analysis.

Prerequisite : CEG720 or an equivalent course.

Instructor : Dr. Soon M. Chung
      schung@cs.wright.edu
      403 Russ Engineering Center, 775-5119

Class : M. W. 4:10-5:25 p.m. at 140 Health Science

Office hour : M. W. 1:30-2:30 p.m. at 403 Russ Center
                or by appointment.
      * use e-mail for short questions.

Text Book : K. Hwang, *Advanced Computer Architecture: Parallelism, Scalability, and Programmability* (McGraw-Hill, 1993), and technical papers.

Topics : Vectorization and vector processing methods
      SIMD processing algorithms
      Multiprocessor architecture and interconnects (Sec 7.1)
      Multicache coherence algorithms (Sec 7.2)
      Message-passing architecture and routing mechanism (Sec 7.3, 7.4)
      Systolic array
      Reconfigurable processor array
      Conditions of parallelism (Sec 2.1)
      Performance metrics (Sec 3.1.3)
      Data flow computers (Sec 9.5)
      Parallel language constructs (Sec 10.2)
      Program partitioning and multiprocessor scheduling (Sec 2.2)

Grading : A:[85,100], B:[75,85), C:[65,75), D:[55,65), F:[0,55)

      Midterm   25% (Feb. 16, Open book, note, and handouts)
      Final   40% (Mar. 14, 5:45-7:45 p.m., Open book, note, and handouts)
      Project 35%
        { originality 10%
         organization of the report 5%
         class presentation 10%
         discussion 10% }