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Drain Current Multiplication In Thin Pillar Vertical MOSFETS Due to Depletion Isolation And Charge Coupling

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Abstract Drain current multiplication in vertical MOSFETs due to body isolation by the drain depletion region and gate-gate charge coupling are investigated at pillar thicknesses in the range 200-10 nm. For pillar thickness > 120 nm depletion isolation does not occur and hence the body contact is found to be completely effective with no multiplication in drain current, whereas for pillar thicknesses < 60 nm depletion isolation occurs for all drain biases and hence the body contact is ineffective. For intermediate pillar thicknesses of 60-120 nm, even though depletion isolation is apparent, the body contact is still effective in improving floating body effects and breakdown. At these intermediate pillar thicknesses, a kink is also observed in the output characteristics due to partial depletion isolation. The charging kink and the breakdown behaviour are characterized as a function of pillar thickness and a transition in the transistor behavior is seen at a pillar thickness of 60 nm. For pillar thickness greater than 60 nm, the voltage at which body charging occurs decreases (and the normalized breakdown current increases) with decreasing pillar thickness, whereas for pillar thickness less than 60 nm, the opposite trend is seen. The relative contributions to the drain current of depletion isolation and the inherent gate-gate charge coupling are quantified. For pillar thickness between 120 and 80 nm, the rise in the drain current is found to be mainly due to depletion isolation., whereas for pillar thicknesses < 60 nm, the increase in the drain current is found to be governed by the inherent gate-gate charge coupling.

Key words Vertical MOSFETs, Partially depleted, Fully depleted, Floating body effects.

1 Introduction

Aggressive scaling of CMOS devices has highlighted the requirement for fully depleted double or surround gate MOSFETS in order to control short channel effects at very short channel lengths [1]. The fully depleted channel region and the double gate reduce the field penetration from drain to source [2-3] and hence give devices with almost ideal subthreshold slopes and excellent short channel behavior. An additional advantage of the increased gate control is that the punch through stopper ($>10^{18}/cm^3$) required for conventional bulk MOSFETs can be avoided and lower channel doping can be used. This eliminates the disadvantages of a high channel doping such as increased leakage current [1], degraded mobility [4], and threshold voltage variations due to random microscopic fluctuations of dopant atoms both in numbers and placement [5]. Therefore, fully depleted double (DG) or surround gate MOSFETs are extremely promising for high density, low voltage, and low power DRAM, SRAM, and conventional CMOS applications. Technologically these fully depleted double or surround gate MOSFETs can be realized using DG SOI [2,3,6-**9**], FinFETs [10-**13**], surround gate structures [**14**] or vertical MOSFETs [15-20].

Though a major advantage of DG SOI and FinFET technologies is the ease of device isolation, in most cases the body is left floating and hence, these devices can suffer from floating body effects whereby weak avalanche in the drain causes hole injection to the body which raises the potential there. The rise in body potential reduces the threshold voltage and also forward biases the source-body junction which can result in parasitic bipolar transistor (PBT) latch-up. Extensive work has been done on floating body effects in both partially depleted (PD) and fully depleted (FD) planar SOI transistors [21-24].

Fig. 1 (a) and (b) show respectively, schematic cross-sectional views of planar partially depleted SOI and depletion isolated vertical MOSFET. The floating body effects (FBE) are somewhat different for these two architectures and a bulk MOSFET. The SOI device usually experiences a steepening of the sub-threshold

slope for low drain voltage, leading to a latch effect due to the PBT, at higher drain voltage. The SOI-PBT gain tends to be emitter efficiency limited and so can be controlled by source engineering [23]. In a body contacted bulk MOSFET, floating body effects arise due to a resistive voltage drop caused by the flow of generated holes to the body contact, although for very short channel devices, a direct PBT action also contributes as generated holes preferentially flow from the body into the source. In the case of the vertical MOSFET with drain at the bottom (Fig. 1(b)) generated holes are separated by the geometry of the architecture. Holes are swept both upwards towards the source, causing the FBE and also downwards where they diffuse to the body contact.

Surround-gate vertical MOSFETs have the advantage that it is easier to make a body contact and hence, the floating body effect should potentially be less severe than in planar SOI MOSFETs. But with the scaling of pillar thickness the floating body effect is also observed in vertical MOSFETs during source on top mode of operation, even if a body contact is provided [25]. This effect has been termed depletion isolation [25] and is caused by the penetration of the depletion region of the bottom drain junction towards the center of the pillar and the eventual isolation of the pillar from the body contact as shown in fig. 1(b). In vertical MOSFETs the floating body effect therefore depends on both pillar thickness and drain bias, and hence is very different from the floating body effect seen in planar SOI transistors. Terauchi et al [25] found depletion isolation in partially depleted vertical MOSFETs and showed how this effect influenced the output and substrate current characteristics. However, no work has been reported on the transition from partially depleted to fully depleted operation in vertical MOSFETs or on the relative contributions of depletion isolation and gate-gate charge coupling to the drain current during this transition.

In this article a comprehensive investigation is undertaken of the transition from partial to fully depleted operation in vertical MOSFETs to better understand the depletion isolation effect. Floating body effects are simulated for different pillar thickness to characterize the impact of the body contact during the transition from partially depleted to fully depleted operation. Subsequently the contributions to drain current of depletion isolation and gate-gate charge coupling are quantified. It is found that the transition from partially depleted to fully depleted operation is different in vertical MOSFETs than in planar MOSFETs because the body contact affects the drain current even after depletion isolation. This result is explained by the strength of the potential barrier formed by the merged drain depletion regions and the ability of holes of the isolated body to surmount the barrier.

2 Modeling Procedure

Analysis of the floating body effect was performed with the aid of numerical simulations using the Silvaco Atlas device simulator [26], implemented on a SUN workstation. A 100 nm channel length vertical ion-implanted double gate nMOSFET as shown in fig. 1(b), was simulated for different pillar thicknesses (T_{Si}). The gate oxide thickness was 2 nm and the gate electrode chosen was a metal with a work function of 4.5 V. The metal gate was chosen for optimal characteristics with no gate depletion problem [27] and low gate resistance. Employing a single metal approach, the gate work function needs to be somewhere near the mid-gap of the gate dielectric, hence making the work function difference ϕ_{ms} equal to zero. The bandgap of the gate dielectric, in this case, silicon dioxide, is about 9eV, which sets the work function of the gate electrode to be 4.5eV. The body doping was $10^{18}/cm^3$ and in source/drain regions a heavily doped region of $1\times10^{20}/cm^3$ was surrounded by a lightly doped region of $1\times10^{19}/cm^3$.

A 2D coupled Poisson's drift-diffusion solver was used to investigate the device operation. It is known that for a pillar thickness, T_{si}> 5 nm, quantum mechanical effects on threshold voltage (V_t) are not significant [28], suggesting that a classical distribution of inversion-layer electrons is still an appropriate approximation. This allowed the use of the 2D coupled Poisson's/drift diffusion solver in the pillar thickness range of 10 nm to 200 nm. To account for the reduced carrier concentration in heavily doped regions, Fermi-Dirac statistics were used to predict the carrier distribution and the effect of bandgap narrowing was also included.

To invoke the dependence of carrier mobility on the parallel and transverse fields in non-planar devices like vertical MOSFETs, the Lombardi CVT model was used [26]. In this model, the dependences of the transverse field, doping and temperature are given by three terms that are combined using Mathiessen's rule. These components are the surface mobility limited by scattering with acoustic phonons (μ_{AC},), the mobility limited by surface roughness (μ_{sr}) and the mobility limited by scattering with optical intervalley phonons (μ_b). The mobility parameters in the simulator were calibrated against a bulk silicon transistor [26]. In particular the mobility degradation due to surface roughness arising from dry etch of vertical pillar was accounted for by adjusting the surface roughness factor in the model.

Impact ionization was modeled by the Selberherr law for the generation rate and the model parameters have already been optimized for submicron bulk silicon transistors [29]. The model for carrier emission and absorption processes proposed by Shockley-Read-Hall (SRH) was used to reflect the recombination phenomenon within the device. The electron and hole lifetimes τ_n and τ_p were modeled as concentration dependent. The simulations were performed at room temperature and the silicon parameter values were taken from [26, 29].

Fig. 2 compares the simulated I_d-V_g characteristics of a 100 nm channel length vertical MOSFET with the experimental characteristics reported in literature [18]. During this calibration we took the substrate-doping concentration to be $10^{18}/cm^3$ and the source/drain doping densities were taken from the SIMS profile of the fabricated device [18], where a heavily doped region of $10^{20}/cm^3$ was surrounded by a lightly doped region of $1\times10^{19}/cm^3$. **As the fabricated device was a polysilicon gate MOSFET [18], we chose polyslicon as gate electrode and polysilicon depletion was taken into account during this calibration.** It can be seen that satisfactory agreement between simulated and experimental characteristics is obtained when the surface roughness factor in the CVT model is reduced from $\delta(elec) = 5.82\times10^{14}$ and $\delta(holes) = 2.0546\times10^{14}$ to $\delta(elec) = 2.91\times10^{13}$ and $\delta(holes) = 1.027\times10^{13}$.

3 Results

Fig. 3 shows the output characteristics of the simulated vertical MOSFETs with and without a body contact, for three different pillar thicknesses and for source on top mode of operation. In the body contacted thick pillar vertical MOSFET (Fig. 3(a)), ideal characteristics are obtained with no evidence of a breakdown kink at high drain voltages. In contrast in the vertical MOSFET without a body contact, a breakdown kink can be seen at a drain voltage of around 4.4V, and the values of drain current are higher (1.73 times at V_d=2V) than equivalent values in the body contacted device at all drain voltages. These results indicate that in the thick pillar device, the pillar does not become isolated by the drain depletion region and the body contact is completely effective in suppressing floating body effects.

For the intermediate pillar thickness in fig. 3(b), the vertical MOSFET without a body contact shows similar characteristics to the equivalent device in fig. 3(a), although the impact ionization effect is sharper and the values of drain current at a given drain voltage are slightly higher. In contrast, the body contacted device is considerably different than the equivalent body contacted device in fig. 3(a). In particular, the device shows an impact ionization effect at a drain bias around 4.4V and higher values of drain current at all drain voltages (1.15 times at V_g=1.5V and V_d=1.5V). When comparing characteristics of the devices with and without a body contact, it can be seen that the body contacted device has lower values of drain current at all drain biases and the breakdown occurs at a slightly higher drain voltage. **This result indicates that the depletion isolation has occurred but the body contact is partially effective at this pillar thickness.**

For the thinnest pillar in fig. 3(c), the characteristics for vertical MOSFETs with and without a body contact are very similar **indicating a completely ineffective body contact at this pillar thickness**. The values of drain current are significantly higher than those for the device in fig. 3(b) (2.38 times at V_g=1.5V and V_d=1.5V), and the avalanche breakdown effect is less severe because of the drain de-biasing effect due to the elevated body potential. This moderate floating body effect in fully depleted MOSFETs is well known [22].

To further investigate the role of impact ionization, fig. 4 compares the output characteristics of the device presented in fig. 3(b) with the output characteristics of the same device with a body contact but without impact ionization. The characteristic for the device without impact ionization represents the situation without any

body charging. The characteristics for body contacted devices with and without impact ionization are similar at low drain biases (≤ 2V for V_g=1 V), clearly indicating that the body is not isolated at these voltages. For drain voltages above 2V, a kink in the output characteristics of the body contacted devices can be clearly seen, indicating body charging by holes from weak avalanche and the presence of depletion isolation at this pillar thickness. The difference in drain current between the devices with and without a body contact for drain biases above 2V indicates that floating body effects are less severe in the body contacted devices even after depletion isolation.

To quantify the drain voltage values for a noticeable change in the drive current characteristics of the body contacted vertical MOSFETs after onset of depletion isolation, fig. 5 shows the simulated values of charge-up drain voltage (V_{db}) as a function of pillar thickness for several values of gate voltage. The charge-up drain voltage (V_{db}) was calculated by comparing the output characteristics of body contacted devices with and without impact ionization, and **identifying the drain voltage at which $(I_{d\ with\ II}-I_{d\ without\ II})/I_{d\ without\ II}\times100$ starts deviating from 5%.** A transition is observed in the dependence of V_{db} at a pillar thickness of 60 nm. For pillar thicknesses ≥ 60 nm, V_{db} reduces with decreasing pillar thickness, whereas for pillar thicknesses < 60 nm, V_{db} increases with decreasing pillar thickness. A similar transition can also be seen in the dependence of V_{db} on gate voltage, V_g. For pillar thicknesses ≥ 60 nm, V_{db} decreases with increasing V_g, whereas for pillar thickness < 60 nm, V_{db} increases with increasing V_g.

To characterize the role of the body contact on the impact ionization effect we have quantified the severity of breakdown at high drain bias (5V) by calculating the normalized breakdown current. This was defined as the difference in drain current of devices with and without impact ionization divided by the drain current without impact ionization, ie, Normalized breakdown current = $(I_{D\ with\ impact\ ionization}-I_{D\ without\ impact\ ionization})/I_{D\ without\ impact\ ionization}$. Fig. 6 shows the normalized breakdown current of vertical MOSFETs with and without a body contact as a function of pillar thickness for various values of gate voltage. Three different regimes of vertical MOSFET operation can be identified. In the thick pillar regime, the pillar is not isolated and hence the simulated drain currents of body contacted devices with and without impact ionization are similar, giving low values of normalized breakdown current. In contrast, the device without a body contact shows floating body effects, giving a high value of normalized breakdown current. For pillar thickness between 120 and 60 nm, the impact ionization effect is observed in both devices with and without a body contact, though the normalized breakdown current is always lower in the device with a body contact. This indicates that even when the pillar is depletion isolated, the body contact still plays an important role in improving the breakdown behavior and in reducing the normalized breakdown current. For pillar thicknesses < 60 nm, the devices are depletion isolated at all drain biases and devices with and without body contact show similar breakdown characteristics and hence similar values of normalized breakdown current. In this regime the body contact is ineffective. A similar transition to that observed in fig. 5 can be seen in the normalized breakdown current of body contacted vertical MOSFETs, at a pillar thickness of 60 nm. For pillar thickness ≥ 60 nm, the normalized breakdown current of body contacted devices increases with decreasing pillar thickness, whereas for pillar thickness < 60 nm the normalized breakdown current decreases with decreasing pillar thickness.

4 Discussion

In this section the role of the body contact after depletion isolation and the origin of the charging kink are physically explained using the depletion isolation phenomenon. Fig. 7 shows the simulated depletion region edges of body contacted vertical MOSFETs at low (0V) and high (5V) drain bias (before and after depletion isolation) for various pillar thicknesses. **The depletion edge is plotted by tracing the line where majority carrier (hole) concentration is reduced by 0.3 times of the body doping concentration.** For a pillar thickness of 200 nm (fig. 7(a)), no depletion isolation occurs within the range of drain biases shown in fig. 3. Therefore, no body charging occurs and the output characteristic of the body contacted vertical MOSFET does not exhibit any breakdown trend or charging kink as seen in fig. 3(a). The difference in current in fig. 3(a) between the vertical MOSFETs with and without a body contact at high drain biases is the well-known impact ionization effect, which has been explained elsewhere in the literature [21-23]. The difference in current found, at low drain bias in the weak impact ionization regime can be mainly attributed to the body potential differences between the vertical MOSFETs with and without body contact. In the body contacted vertical MOSFET potential profile of body is different than that of the vertical MOSFET without body contact due to forced grounding of the body. This difference in current between devices with and without a body contact is also seen in planar devices [24].

For pillar thicknesses of 120 and 80 nm (fig. 7(b) & fig. 7(c)), pillar is not isolated at low drain bias. At high drain bias the depletion region from the bottom drain region gradually isolates the Si pillar from the substrate and divides the body into two distinct regions. In body

contacted vertical MOSFETs region two still remains connected to the body contact at the bottom of the pillar after the depletion isolation, whereas region 1 is isolated. In vertical MOSFETs without a body contact both regions are isolated. The effect of such a separation of regions 1 and 2 on drain current will be discussed later. However, contrary to the thick pillar case, the observed breakdown behaviour in the body contacted vertical MOSFETs of 80 nm pillar thickness (Fig. 3(b)) definitely reflects the existence of depletion isolation as can be seen from the presence of the impact ionization effect in the body contacted device. It is worth noting that the change from total depletion (i.e., insignificant majority carrier concentration) to perfect neutral is not abrupt and the transition between the depleted and neutral region extends over 2-3 Debye lengths on each side of the pillar. For a body doping of $10^{18}/cm^3$ there is a 10-15 nm of transition region for depletion isolation consideration. Therefore, once depletion regions from the two sides of the pillar overlap, the strength of the merged depletion region depends on pillar thickness due to Debye length considerations. Moreover, this also controls the actual PD-FD boundary [30].

For a pillar thickness of 60 nm, fig. 7(c) shows that the pillar is isolated at all drain biases. Therefore, for pillar thickness of 60 nm or less, the output characteristics of devices with and without a body contact are very similar, as can be seen in fig. 3 (c) for a pillar thickness of 10 nm. A moderate breakdown kink is also found at this pillar thickness, which has already been explained by Fossum et al. [22] by classical gate coupling theory [31].

To help explain the different output characteristics in fig. 3(b) for devices with and without a body contact, fig. 8 shows the hole concentration contour plot and **the body potential as a function of relative distance from pillar bottom drain (location A) through the middle of the pillar for pillar thicknesses of 80 and 60 nm at V_g=1 V and V_d=5 V. The difference between the peak potential near the pillar bottom drain (location A) and the middle of the pillar is taken as drain-body potential barrier.** For pillar thickness of 80 nm (fig. 8(a)), it can be seen that even if the pillar is isolated, some holes surmounts the potential barrier of the depletion region merged at the bottom of the pillar. This is possible because the potential barrier is small, with a value of 0.052 V (i. e., 2kT/q). In contrast, for a pillar thickness of 60 nm, fig. 8(b) shows that the potential barrier is much bigger (0.52 V) and hence the hole flow from the pillar to the substrate is almost stopped This indicates that even though the pillar is isolated, the strength of the merged depletion region at the bottom of the pillar controls the hole flow to the body contact, hence the device behaviour. Therefore, even though the body is isolated, the body contact still influences the output characteristic as shown in fig. 3(b) for a 80 nm pillar.

We now discuss the transition in the charge up drain bias (V_{db}) seen in fig. 5 at a pillar thickness of 60 nm. This can be **explained from the relationship between the pillar thickness and depletion isolation at the bottom of the pillar. Reducing the pillar thickness at a fixed gate bias or increasing the gate voltage at a given pillar thickness brings the depletion regions at the bottom of the pillar closer together thereby increasing the strength of the merged depletion region at the bottom of the pillar which eventually controls the hole flow to the body contact. Therefore, as the pillar thickness is reduced from 120 to 60 nm, the charge up drain bias (V_{db}) decreases with decreasing pillar thickness because sufficiently strong depletion isolation that may affect hole flow to the body contact occurs at progressively lower values of drain bias. For the same reason, the increased drain depletion width resulting from an increased gate voltage also causes V_{db} to decrease with increasing gate voltage.** In contrast, for pillar thicknesses < 60 nm, the pillar is fully depleted and scaling of the pillar thickness from 60 nm to 10 nm results in a transition to a more strongly depleted regime of operation. **Strongly depleted operation is known to reduce floating body effects [22, 24, 31] and hence, for pillar thicknesses < 60 nm,** V_{db} increases with decreasing pillar thickness and also increases with increasing gate voltage at a given pillar thickness.

We now explain the impact ionization effect in fig.6. The convergence of the normalized breakdown current for devices with and without a body contact and the peak in the normalized breakdown current of the body contacted device at a pillar thickness of 60 nm can be explained by the same relationship between the pillar thickness and depletion isolation at the bottom of the pillar. Reducing pillar thickness from 120 to 60 nm, results in the strengthening of drain-body potential barrier due to the merged depletion regions. This causes the body contact to become gradually less effective for any fixed bias condition with the scaling of the pillar thickness and results in the convergence of the normalized breakdown current for devices with and without a body contact. In contrast, the reduction in the normalized breakdown current for pillar thickness < 60 nm is due to the fully depleted regime of operation. The behaviour found for pillar thicknesses < 60 nm, corresponds to the film thickness scaling effect seen in planar SOI MOSFETs [24].

To fully explain the output characteristics in fig. 3 and the behaviour in the depletion isolation region in figs 5 and 6, we need to consider the effect of the charge

coupling of the two gates. In thin pillar, depletion isolated vertical MOSFETs we would expect the threshold voltage to decrease due to the coupling of the fields from the two gates. This would reduce the source-body potential barrier (ϕ_{SB}) and cause a rise in drain current with decreasing pillar thickness. At the same time holes generated by impact ionization would forward bias the body and result in a further increase in drain current. To isolate the effects of depletion isolation and gate-gate charge coupling we have simulated devices at various pillar thickness with and without impact ionization. A relative drain current was then calculated by dividing the drain current of the device at a given pillar thickness by the drain current of the 200 nm pillar device with impact ionization deactivated. The drain current at the pillar thickness of 200 nm was chosen because at this pillar thickness there is no coupling of the gates and also there is no depletion isolation. Therefore the curve without impact ionization allows us to see the rise in the drain current due to the gate-gate charge coupling, whereas the curve with impact ionization takes account of both depletion isolation and gate-gate coupling. Fig. 9 shows the relative drain current as a function of pillar thickness for vertical MOSFETs with and without impact ionization and for V_g=2 V and V_d=3.5 V. We see that for pillar thickness ≥ 140 nm, the relative drain currents with and without impact ionization are identical. This indicates that at these pillar thicknesses, the pillar is not isolated and there is no gate-gate charge coupling. The rise in drain current due to gate-gate coupling starts at a pillar thickness of 100 nm, whereas the effect of depletion isolation starts at a pillar thickness of 120 nm. For pillar thicknesses between 120 and 80 nm, we see that the rise in relative drain current is mainly due to depletion isolation, for a pillar thickness 60 nm the two mechanisms contribute similar amounts to the rise in current, and for pillar thicknesses ≤ 40 nm, the rise in current is mainly due to the gate-gate charge coupling. This result indicates that depletion isolation dominates the device behaviour for pillar thicknesses in the range of 120-80 nm. However, for pillar thicknesses ≤ 40 nm the depletion isolation effect is suppressed and the device operates in the fully depleted regime where the behaviour is dominated by the inherent gate-gate charge coupling.

We also investigate the combined effect of depletion isolation and coupling of channels on the source-body potential barrier (ϕ_{SB}). Fig. 10 shows the simulated source body potential barrier (ϕ_{SB}) in vertical MOSFETs with and without a body contact as a function of pillar thickness for various values of gate voltage. ϕ_{SB} were calculated in the middle of the pillar at V_{DS}=5V (heavy impact ionization regime). It is found that for the device without a body contact, ϕ_{SB} decreases slowly with reducing pillar thickness, whereas for the body contacted device a sharp decrease is observed, beginning at a pillar thickness of 120 nm and ending at a pillar thickness of 60 nm. This behaviour is due to depletion isolation raising the potential of the body and thereby decreasing the source/body potential barrier (ϕ_{SB}). The effect of the change in ϕ_{SB} on recombination is exemplified in fig. **10(b).** A drastic increase of the recombination is observed in body contacted devices when the pillar thickness is reduced below 120 nm.

Finally we investigate the effect of body separation by depletion isolation on the drain current. Two types of devices were simulated to study this effect as shown in fig. 11. Fig. 11(a) corresponds to a device with a large body region below the pillar, whereas fig. 11(b) corresponds to a device with a small body region below the pillar. Fig. 12 shows the output characteristics of the two types of device presented in fig. 11. It is found that device 12(a) and 12(b) show identical output characteristics both in body contacted and floating body conditions, indicating that carriers below the pillar has no effect on the drain current.

4 Conclusions

We have investigated depletion isolation and the effect of the body contact in vertical MOSFETs with pillar thicknesses in the range 200-10 nm to study the drain current multiplication in vertical MOSFETs during transition from partial to fully depleted operation. For pillar thicknesses > 120 nm the body contact is completely effective with no multiplication in drain current and the output characteristics do not exhibit any breakdown trend, whereas for pillar thickness < 60 nm the body contact is ineffective. For pillar thickness between 120 and 60 nm depletion isolation gives rise to a charging kink in the output characteristics of body contacted devices due to body charging after depletion isolation. Though depletion isolation occurs in this regime, the body contact is still partially effective after depletion isolation, as can be seen from improved floating body effects and improved breakdown behaviour. In this regime the voltage at which the charging kink occurs and the normalized breakdown current vary with pillar thickness and shows a transition at a pillar thickness of 60 nm. For pillars thicker than 60 nm, the body charging voltage decreases (and the normalized breakdown current increases) with decreasing pillar thickness, while for pillars thinner than 60 nm the opposite trend is seen. For the pillar thicknesses > 60 nm, the trend observed with reducing pillar thickness are explained by the occurrence of depletion isolation at progressively lower drain

voltages and the strengthening of the potential barrier at the drain due to the merged depletion regions. Whereas the trend observed for pillar thickness < 60 nm, are explained by the fully depleted regime of operation. For pillar thickness between 120 and 80 nm, it has been shown that depletion isolation dominates the drain current of body contacted devices, whereas for pillar thicknesses of ≤ 40 nm, the inherent gate-gate charge coupling under the two gates dominates, because the device is operating in the fully depleted regime.

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List of figures

Fig. 1 Schematic cross-sectional view of a) planar SOI and b) vertical MOSFET operated in the depletion isolated mode.

Fig. 2 Comparison of simulated and measured transfer characteristics (I_d vs Vg) of the 100 nm channel length ion-implanted vertical MOSFET reported in [18].

Fig. 3 Simulated output characteristics (I_d vs V_d) of vertical MOSFETs with and without a body contact for pillar thicknesses of a) 200 nm, b) 60 nm and c) 10 nm.

Fig. 4 Simulated output characteristics (I_d vs V_d) of vertical MOSFETs with and without a body contact at a pillar thickness of 80 nm and with impact ionization (II) turned on and off. Dashed lines represent the vertical MOSFET with impact ionization and without a body contact, solid lines represent the body contacted

vertical MOSFET with impact ionization and circles represent the body contacted vertical MOSFET without impact ionization.

Fig. 5 Simulated values of charge-up drain voltage (V_{db}) as a function of pillar thickness and for several values of gate voltage. V_{db} was calculated by comparing the output characteristics of body contacted devices with and without impact ionization and identifying the voltage at which characteristics diverge.

Fig. 6 Simulated normalized breakdown current of vertical MOSFETs with and without a body contact as a function of pillar thickness and for several values of gate voltage. The normalized breakdown current was defined as the difference in drain current of devices with and without impact ionization divided by the drain current without impact ionization.

Fig. 7 Cross-sectional views of body contacted vertical MOSFETs before and after depletion isolation, for pillar thicknesses of a) 200 nm, b) 120 nm c) 80 nm and d) 60 nm.

Fig. 8 Hole concentration contour plot and the body potential as a function of relative distance from pillar bottom drain (location A) through the middle of the pillar for pillar thicknesses of a) 80 nm, and b) 60 nm. The gate voltage was 1V and the drain voltage was 5V.

Fig. 9: The relative drain current of vertical MOSFETs as a function of pillar thickness with and without impact ionization for V_g=2 V and V_d=3.5 V. The relative drain current was calculated by dividing the drain current of the device at various pillar thicknesses by the drain current of the device for a pillar thickness of 200 nm with impact ionization inactivated.

Fig. 10: Source body potential barrier (ϕ_{SB}) and the recombination rate in vertical MOSFETs with and without a body contact as a function of pillar thickness for various values of gate voltage. The drain bias was 5V.

Fig. 11 Schematic cross-sectional views of vertical MOSFETs with large (a) and small (b) body regions below the pillar (region 2).

Fig. 12 Simulated output characteristics (I_d vs V_d) of vertical MOSFETs with large and small body regions below the pillar (fig. 11). Results are shown for devices with and without a body contact.

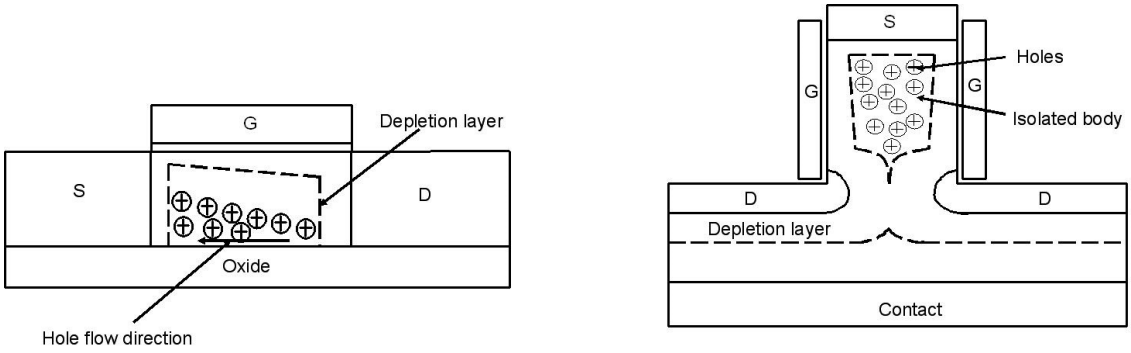

G
Depletion layer
S
D
Oxide
Hole flow direction
(a)
S
Holes
G
G
Isolated body
D
D
Depletion layer
Contact
(b)

Fig. 1

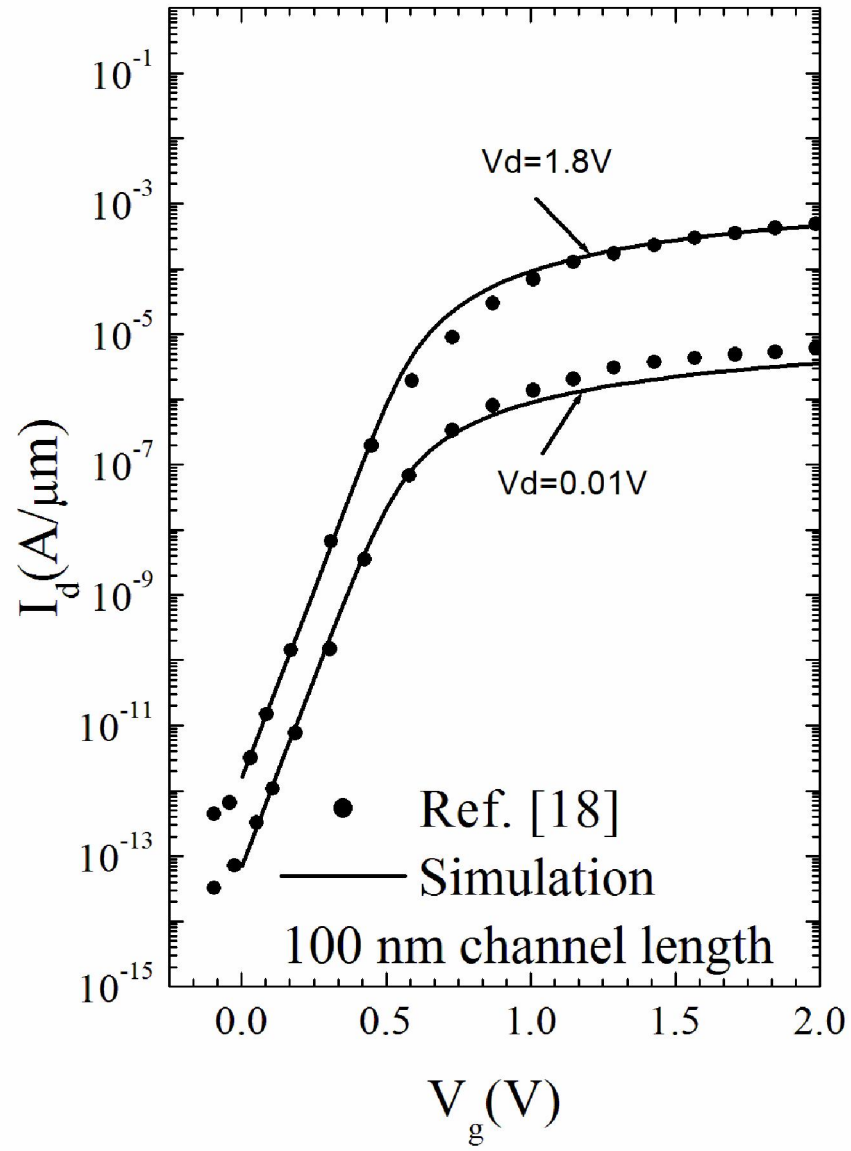

10^{-1}
10^{-3}
10^{-5}
10^{-7}
10^{-9}
10^{-11}
10^{-13}
10^{-15}
I_d(A/μm)
Vd=1.8V
Vd=0.01V
Ref. [18]
Simulation
100 nm channel length
0.0
0.5
1.0
1.5
2.0
V_g(V)

Fig. 2

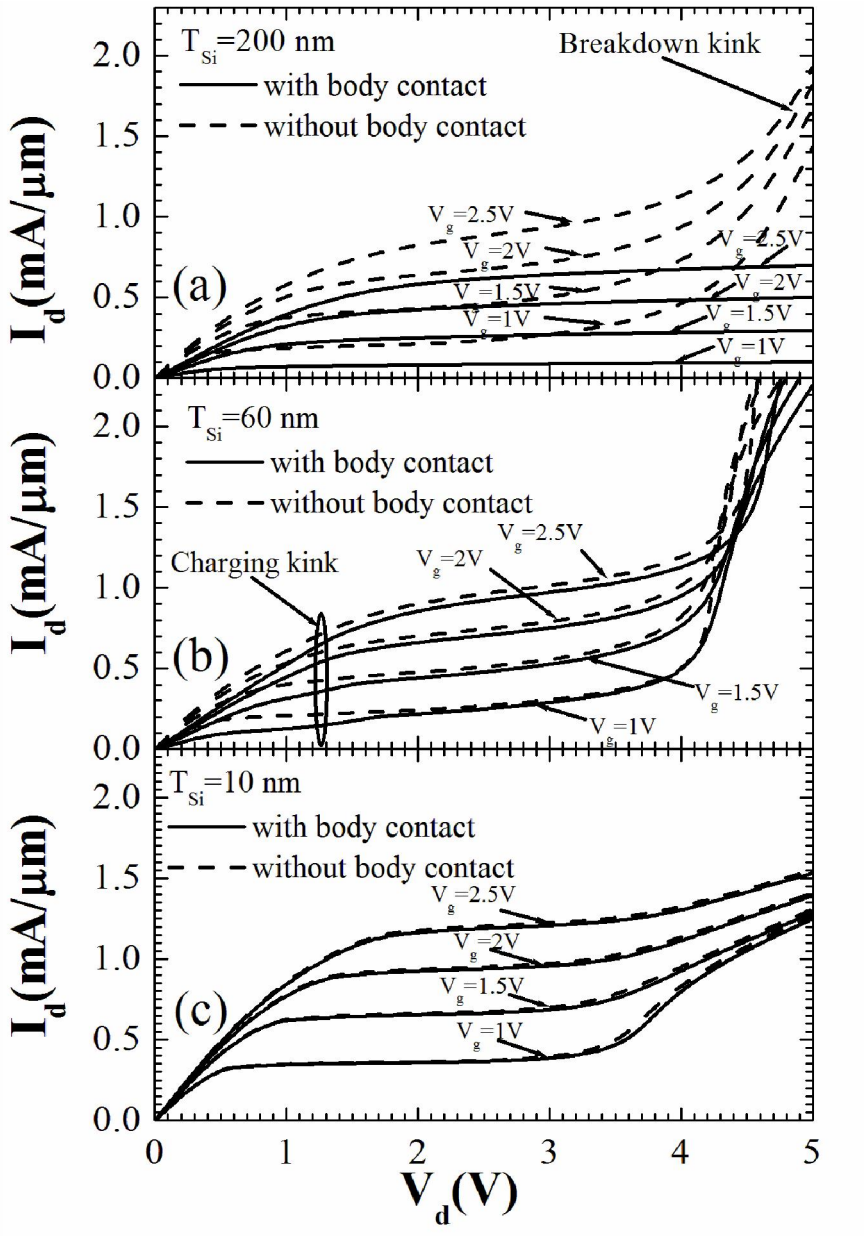

T_Si=200 nm
with body contact
without body contact
Breakdown kink
V_g=2.5V
V_g=2V
V_g=1.5V
V_g=1V
(a)
T_Si=60 nm
with body contact
without body contact
Charging kink
V_g=2.5V
V_g=2V
V_g=1.5V
V_g=1V
(b)
T_Si=10 nm
with body contact
without body contact
V_g=2.5V
V_g=2V
V_g=1.5V
V_g=1V
(c)
I_d(mA/μm)
V_d(V)
0.0
0.5
1.0
1.5
2.0
0
1
2
3
4
5

Fig. 3

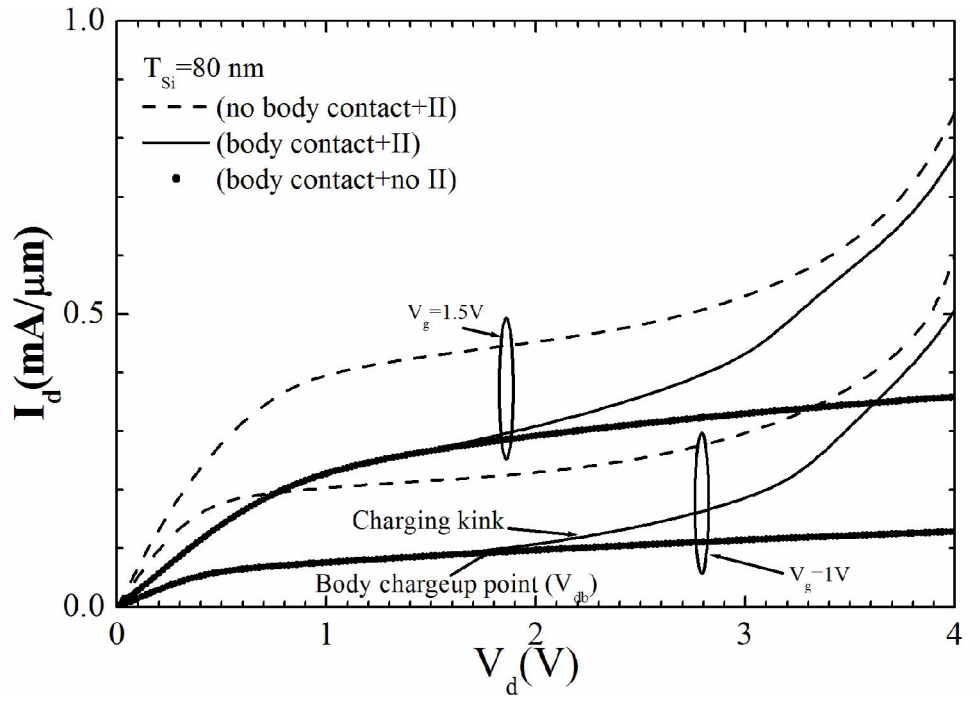

1.0
0.5
0.0
0
1
2
3
4
T_{Si}=80 nm
(no body contact+II)
(body contact+II)
(body contact+no II)
V_g=1.5V
V_g=1V
Charging kink
Body chargeup point (V_{db})
I_d(mA/μm)
V_d(V)

Fig. 4

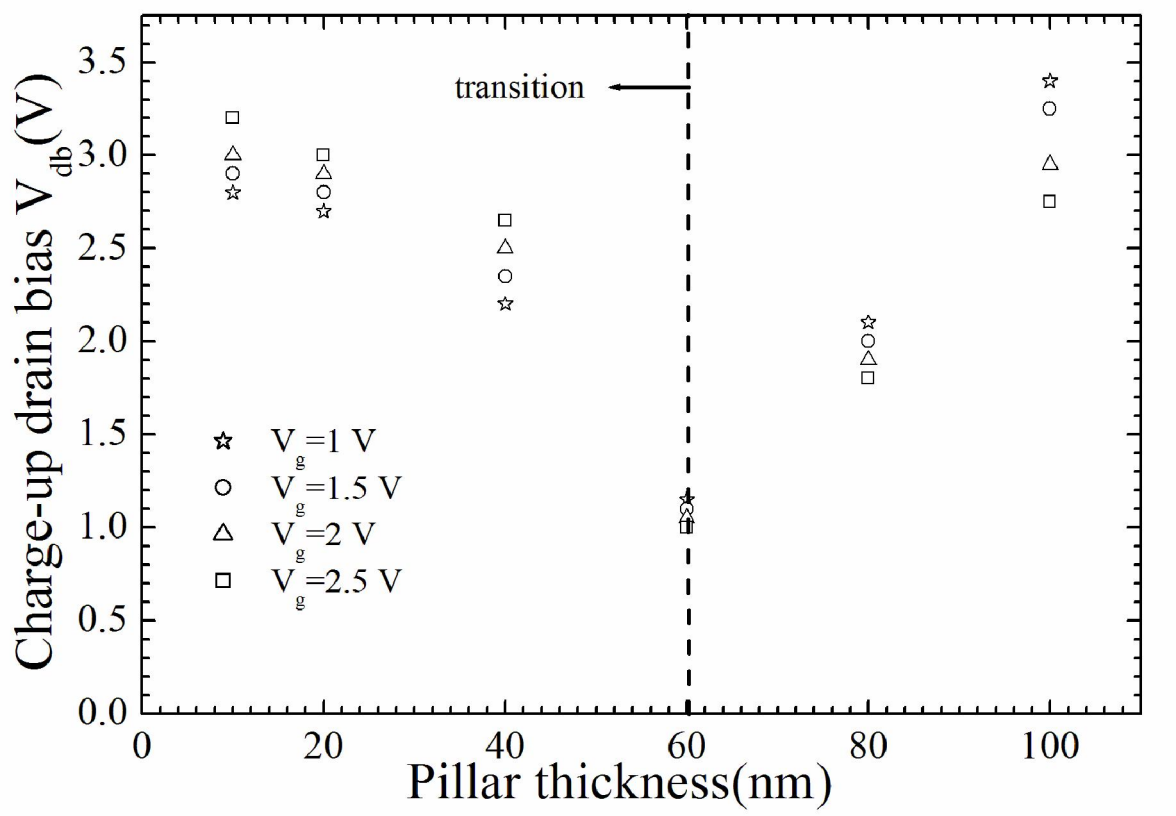

Charge-up drain bias V_{db}(V)
Pillar thickness(nm)
transition
V_g=1 V
V_g=1.5 V
V_g=2 V
V_g=2.5 V
0.0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
0
20
40
60
80
100

Fig. 5

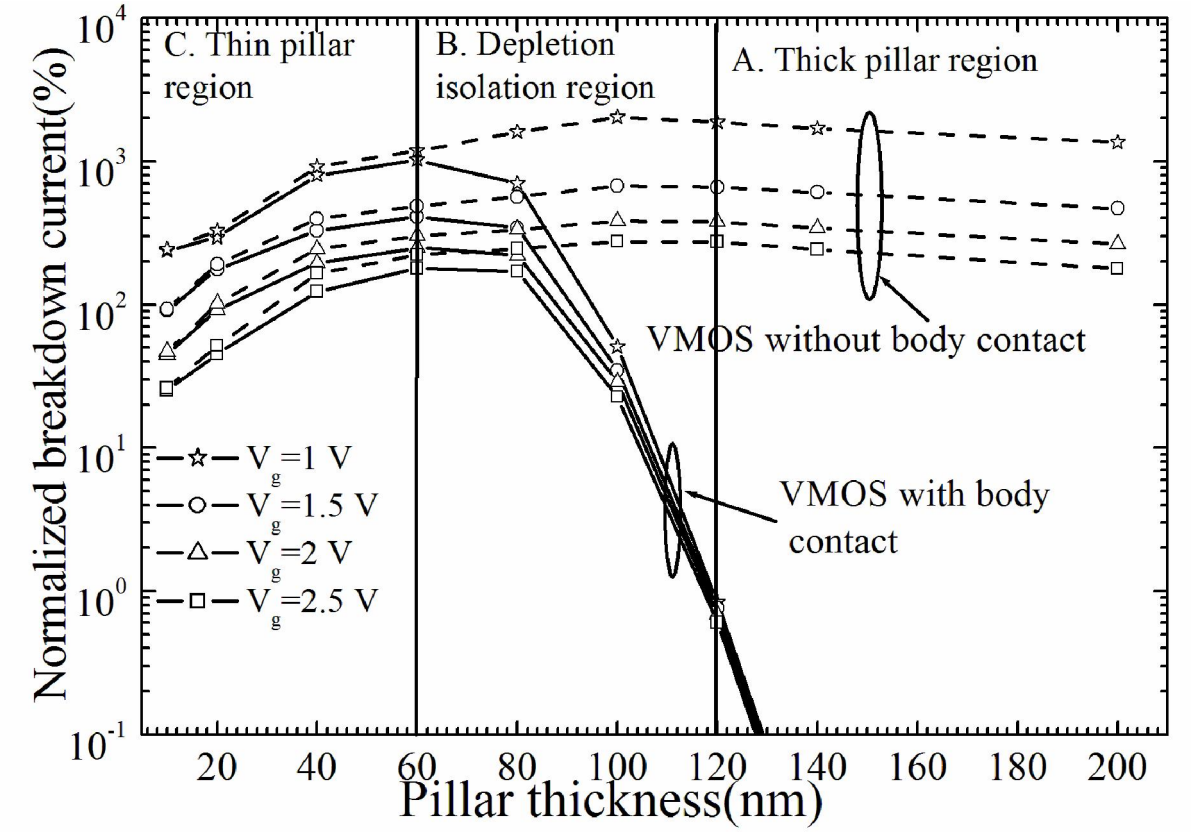

C. Thin pillar region
B. Depletion isolation region
A. Thick pillar region
VMOS without body contact
VMOS with body contact
V_g=1 V
V_g=1.5 V
V_g=2 V
V_g=2.5 V
Normalized breakdown current(%)
Pillar thickness(nm)
10^4
10^3
10^2
10^1
10^0
10^-1
20
40
60
80
100
120
140
160
180
200

Fig. 6

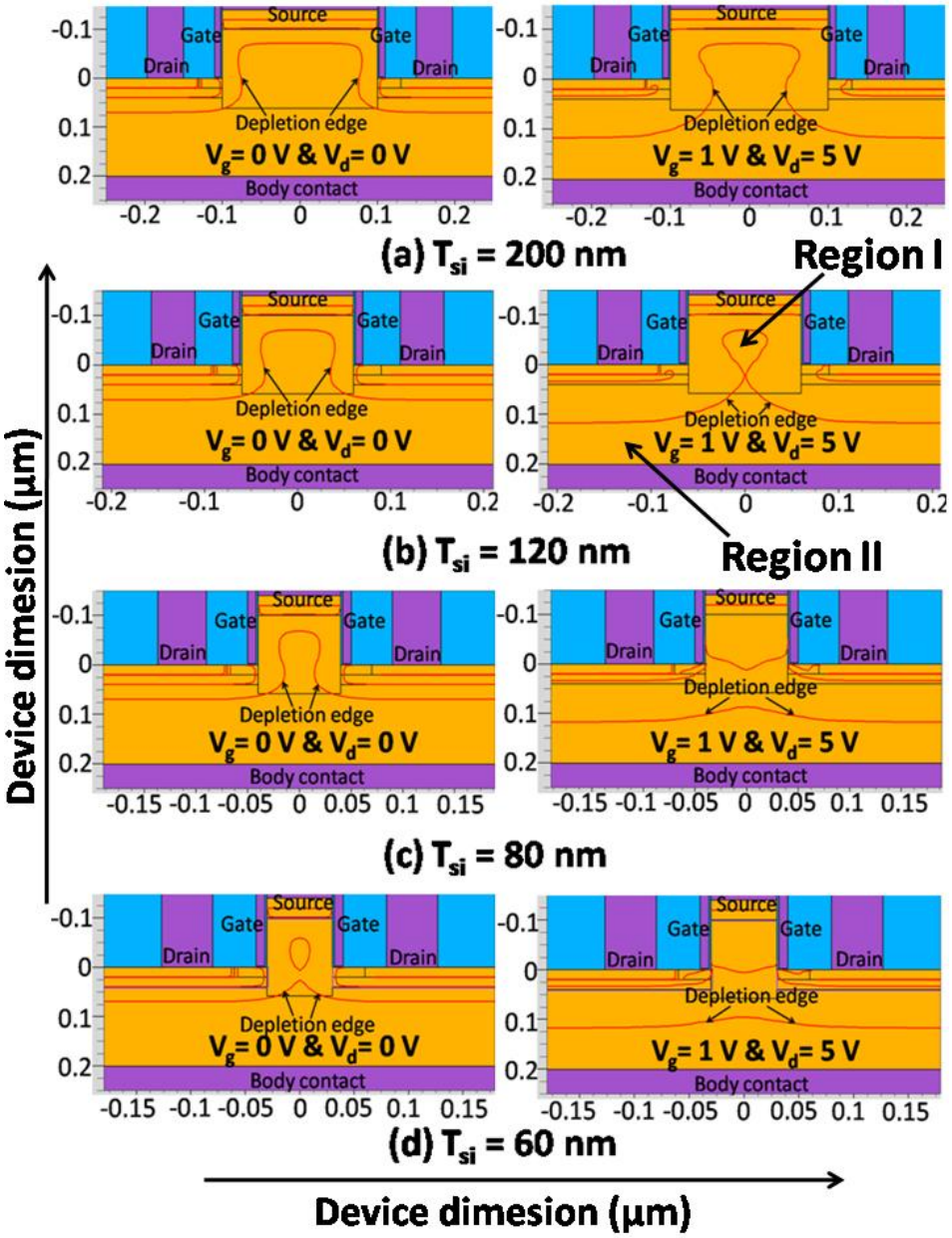

Source
Gate
Gate
Drain
Drain
Depletion edge
V_g= 0 V & V_d= 0 V
V_g= 1 V & V_d= 5 V
Body contact
(a) T_{si} = 200 nm
Region I
Region II
(b) T_{si} = 120 nm
(c) T_{si} = 80 nm
(d) T_{si} = 60 nm
Device dimesion (µm)
Device dimesion (µm)

Fig. 7

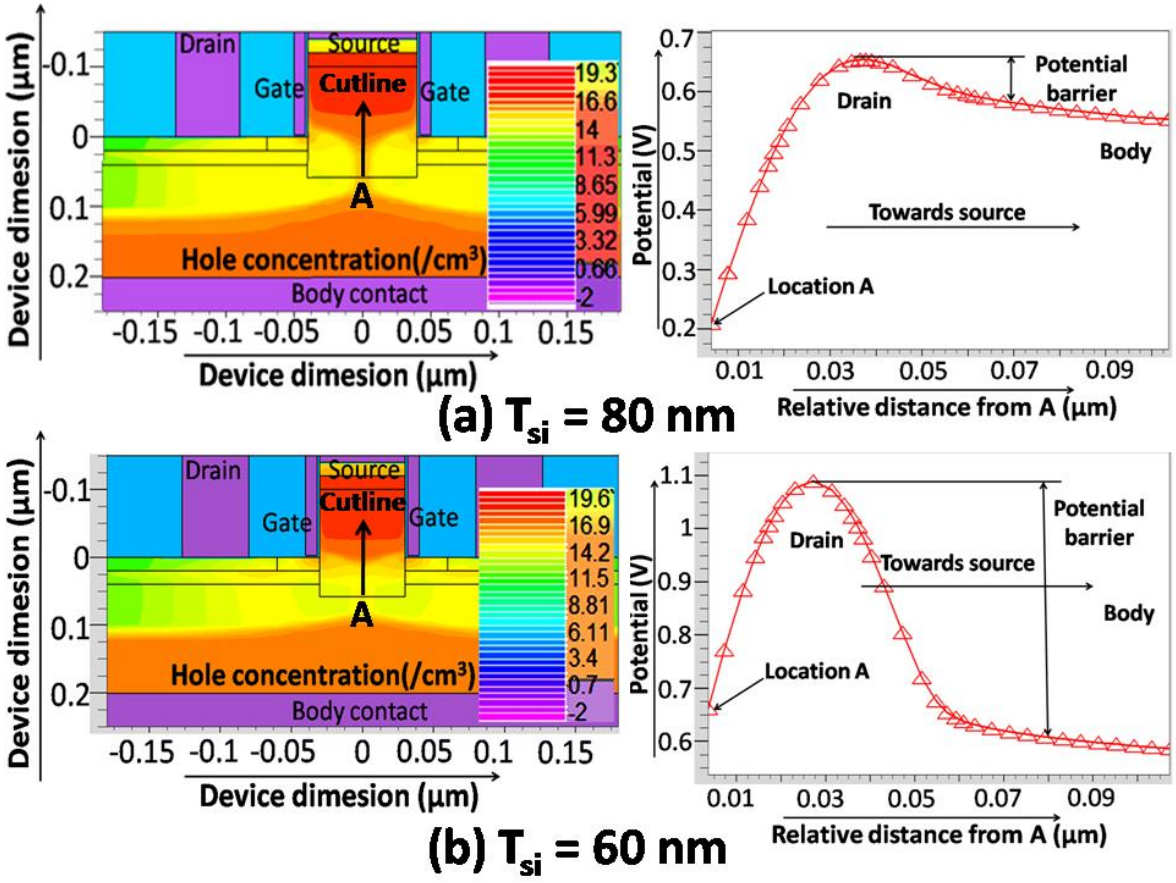

Device dimesion (µm)
Drain
Source
Gate
Cutline
Gate
A
Hole concentration(/cm³)
Body contact
19.3
16.6
14
11.3
8.65
5.99
3.32
0.66
-2
-0.15 -0.1 -0.05 0 0.05 0.1 0.15
Device dimesion (µm)
Potential (V)
Potential barrier
Drain
Body
Towards source
Location A
0.01 0.03 0.05 0.07 0.09
Relative distance from A (µm)
(a) T_si = 80 nm
19.6
16.9
14.2
11.5
8.81
6.11
3.4
0.7
-2
(b) T_si = 60 nm

Fig. 8

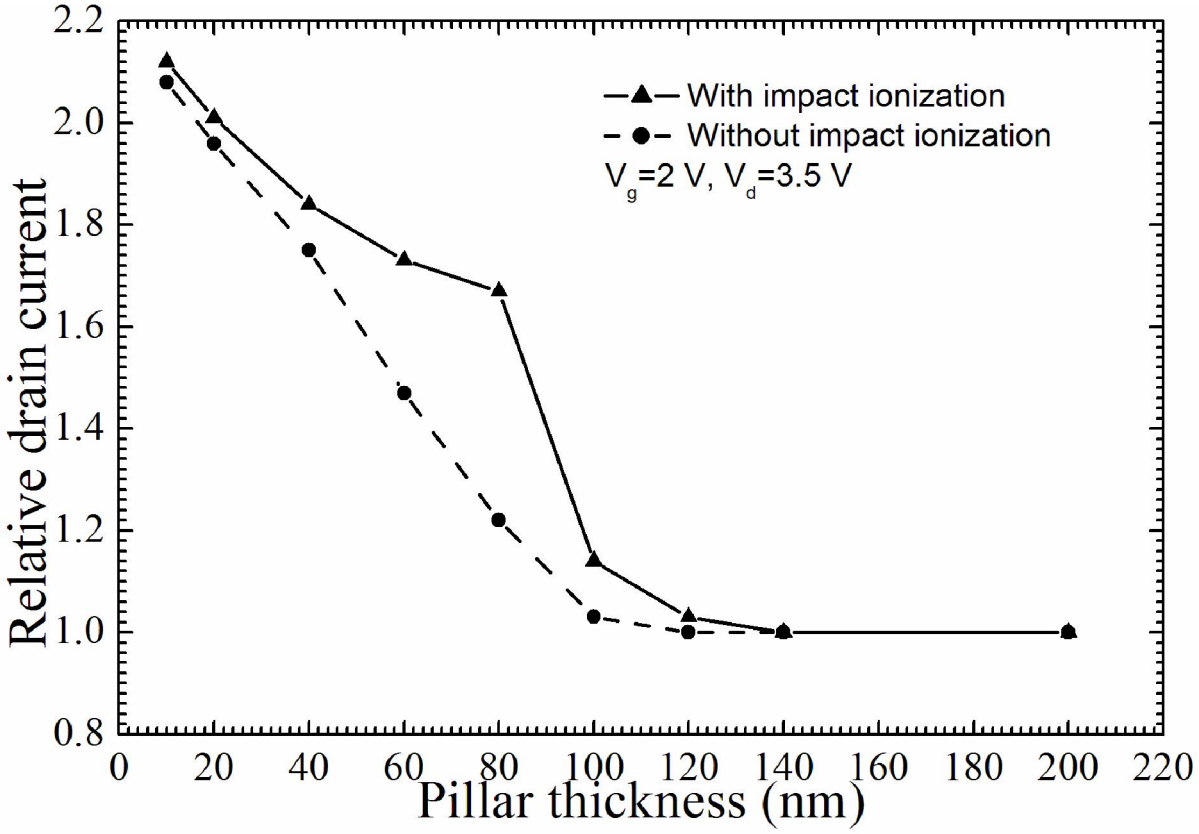

With impact ionization
Without impact ionization
V_g=2 V, V_d=3.5 V
Relative drain current
Pillar thickness (nm)
2.2
2.0
1.8
1.6
1.4
1.2
1.0
0.8
0
20
40
60
80
100
120
140
160
180
200
220

Fig. 9

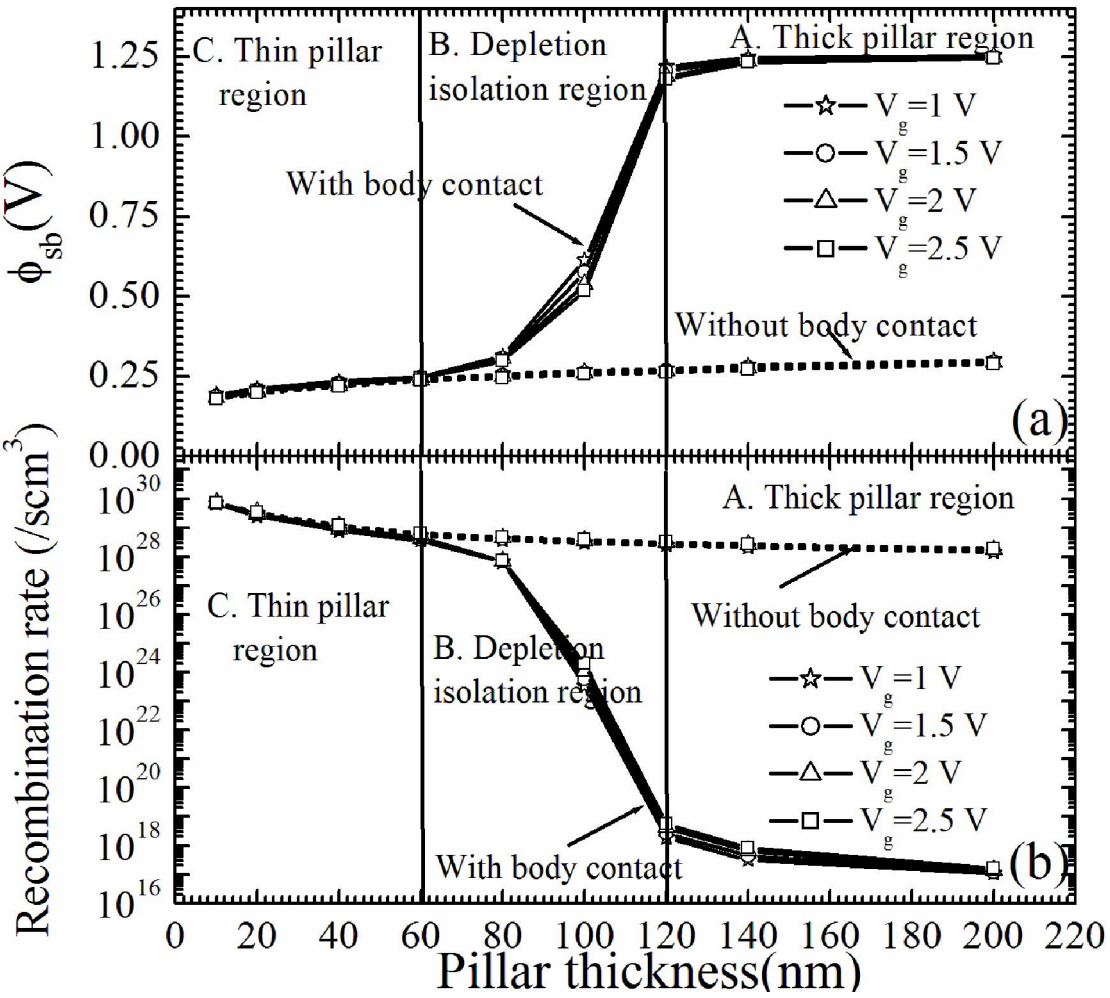
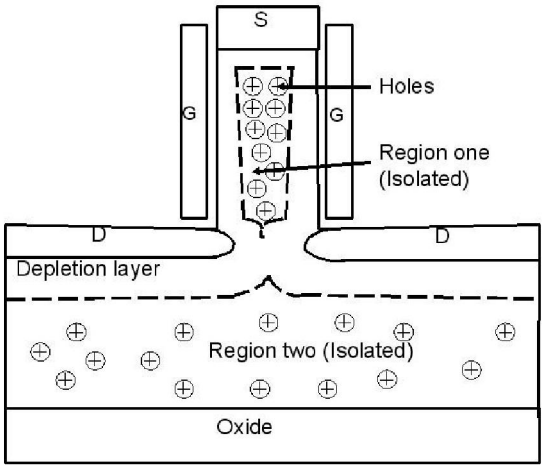
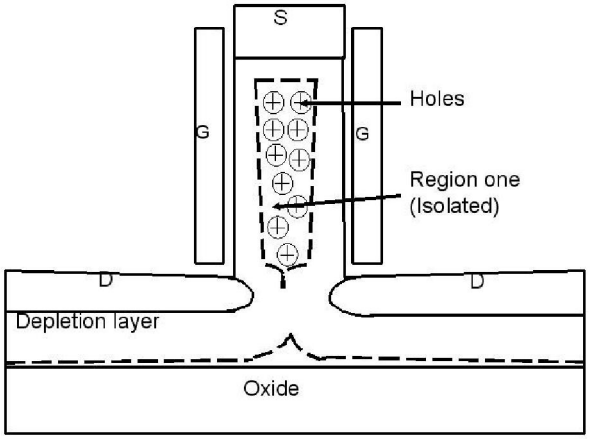

C. Thin pillar region
B. Depletion isolation region
A. Thick pillar region
With body contact
Without body contact
V_g=1 V
V_g=1.5 V
V_g=2 V
V_g=2.5 V
(a)
(b)
ϕ_{sb}(V)
Recombination rate (/scm^3)
Pillar thickness(nm)

Fig. 10



(a) Device with a large body region below the pillar



(b) Device with a small body region below the pillar

Fig. 11

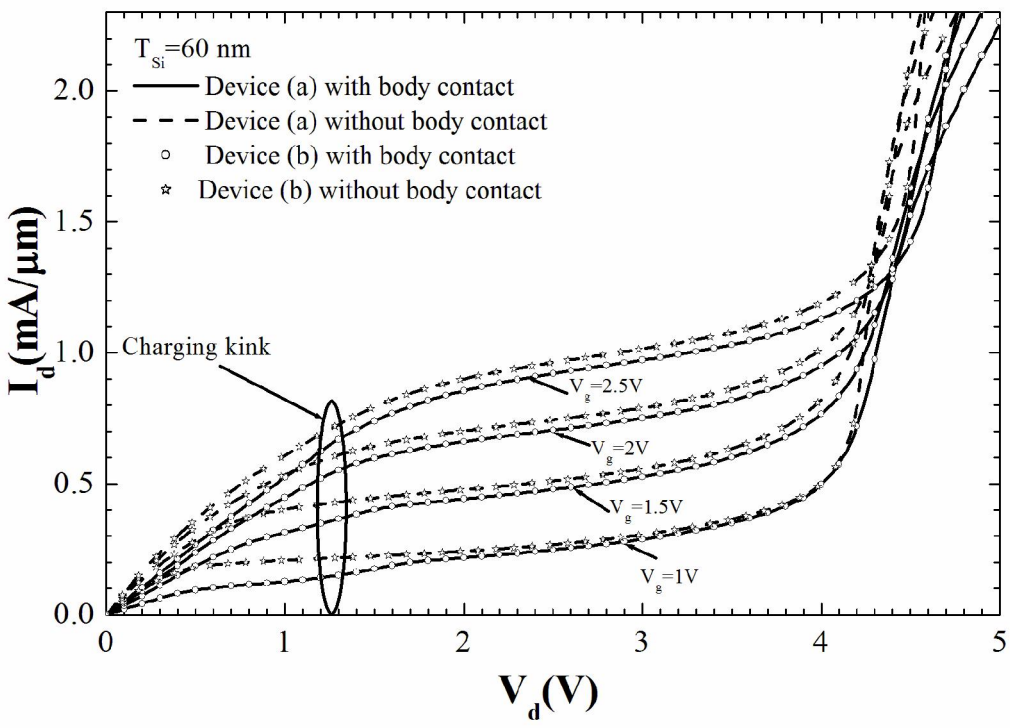

T_Si=60 nm
Device (a) with body contact
Device (a) without body contact
Device (b) with body contact
Device (b) without body contact
Charging kink
V_g=2.5V
V_g=2V
V_g=1.5V
V_g=1V
I_d(mA/μm)
V_d(V)
0.0
0.5
1.0
1.5
2.0
0
1
2
3
4
5

Fig. 12