

Guest Editors' Introduction:

Robust 3D-Stacked ICs

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Three-dimensional (3D) ICs have emerged as a promising technology that complements CMOS scaling through die stacking and allows higher transistor density, heterogeneous technology integration, and smaller footprint than 2D ICs. Despite potential advantages, a major obstacle to their proliferation is insufficient understanding of challenges caused by die stacking, and in particular due to thermal stress, reliability and physical failure analysis, all of which present exciting research opportunities for the design and test community. This special section is our attempt to provide better understanding of these challenges, and solutions that are currently being developed. We also recognised a growing need for a terminology overview to understand various acronyms and terminologies related with 3D ICs and interconnect technology. This special section consists of four articles, authored by our colleagues from three major European research institutes (CEA-LETI, Fraunhofer IWM, and IMEC) and a semiconductor company (STMicroelectronics). The last three articles originate from the 6th edition of Friday Workshop on 3D Integration, collocated with the DATE 2014 conference in Dresden, Germany. The guest editors had the distinct honour of organizing this longest running and most successful Friday Workshop collocated with the DATE conference for seven consecutive years, from 2009 to 2015.

The first article “The 3D Interconnect Technology Landscape”, written by Eric Beyne from IMEC, defines acronyms and terminologies frequently used to elaborate different technological aspects of 3D ICs.

The second article is co-authored by colleagues from CEA-LETI and STMicroelectronics, “Experimental Insights into Thermal Dissipation in TSV-Based 3D Integrated Circuits”, by Perceval Coudrain *et al.* This article describes heat dissipation challenges in 3D ICs; using two case studies, it also presents insights and design guidelines for 3D thermal management.

The next article is from IMEC, “Reliability Challenges Related to TSV Integration and 3D Stacking”, by Kristof Croes *et al.*, which identifies four major reliability challenges related with TSV-based 3D integrated circuits and their solutions that are being developed at IMEC.

Finally, the last article of this special edition is from Fraunhofer IWM, “Innovative Failure Analysis Techniques for 3D Packaging Developments”, by Frank Altmann and Matthias Petzold. This article presents an overview of challenges related with failure localization and pinpointing defect sites, within the 3D package. Using case studies, this article presents newly developed physical failure analysis techniques suitable for 3D packages.

Saqib Khurshheed is a Lecturer (Assistant Professor) in the Dept. of Electrical Engineering and Electronics, University of Liverpool, UK. Prior to joining Liverpool, he worked as a Senior Research Fellow at the University of Southampton, UK. He is engaged in research related to reliability, test and yield improvement of low-power, high-performance designs and 3D ICs.

From 2012 to 2015, he organized the Friday Workshop on 3D ICs, collocated with the DATE conference.

Pascal Vivet is a Senior Expert at CEA-LETI, Grenoble, France. His research interests include wide aspects from system level design to asynchronous design, Network-on-Chip, energy efficient multi-cores, 3D design, and related CAD aspects. He is a TPC member of a number of conferences, such as ASYNC, NOCS, DATE, ICCAD, and 3DIC. In the past, he served as a member of the organizing committee of the D43D Workshop (2011-15), and the Friday Workshop on 3D ICs (2013-15), collocated with DATE conference.

Fabian Hopsch is a researcher at Fraunhofer IIS/EAS in Dresden, Germany. He is a member of the German committee of "Test methods and reliability of circuits and systems". In 2013 he organized the "Test and Reliability" workshop and in 2014 he participated in the organization of the Friday Workshop on 3D ICs, collocated with DATE conference. His research interests include test development, analog fault simulation, diagnosis, DfT and test for 2.5D/3D circuits.

Erik Jan Marinissen is a Principal Scientist at IMEC, Leuven, Belgium. His research interests include all aspects of VLSI test and DfT. He has served as the Editor-in-Chief of the IEEE Std 1500 working group and chairs the IEEE Std P1838 working group. He holds a PDEng in computing science from Eindhoven University of Technology, Eindhoven, Netherlands. He is a Fellow of the IEEE and serves on the editorial board of IEEE Design & Test. From 2009 to 2015, he initiated and organized the Friday Workshop on 3D ICs, collocated with the DATE conference.